Experimental Stress Characterization and Numerical Simulation for Copper Pumping Analysis of Through-Silicon Vias

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(Invited Paper)

***Abstract*— In this paper, a 3-D thermomechanical model of through-silicon vias (TSVs) has been analyzed and verified with *in situ* microscale strain measurements by synchrotron X-ray microdiffraction. Thereafter, a comprehensive stress/strain analysis on copper pumping and back-end-of-line (BEOL) cracking issues has been carried out. In addition, a design-of-experiments-based approach has been used to understand the effect of various parameters on copper pumping and BEOL stress. The results show that the smaller TSV diameter and thinner silicon die help reduce the copper pumping and thus mitigate BEOL stress.**

***Index Terms*— Copper pumping, finite-element analysis, synchrotron X-ray diffraction, through-silicon vias (TSVs).**

I. Introduction

3-D INTEGRATION with stacked dice and through-silicon vias (TSVs) has been widely explored to meet the ever-increasing demands for electronic systems: better performance, more functionality, higher I/O density, smaller form factor, lower power consumptions, and lower cost [1], [2]. Among the numerous challenges associated with 3-D integration [3], reliability has attracted tremendous attention. TSV reliability issues arise due to high mismatch in the coefficient of thermal expansion (CTE) between the silicon substrate, dielectric layer, and copper. Fig. 1 shows a TSV cross section, and the arrows highlight regions with larger impact from the CTE mismatch. Due to the high CTE mismatch and the constraint between copper TSVs and surrounding structures, copper pumping occurs at a high temperature and copper sinking occurs at a low temperature [4]. The copper pumping and sinking may induce large stresses and lead to various reliability issues such as cohesive cracking and interfacial separation in TSVs [5]–[7]. Copper pumping, which can occur in various conditions, may also affect the back-end-of-line (BEOL) structures. To investigate the mechanism of copper pumping and reduce the associated failure risk on TSVs and neighboring structures, numerical analysis [4], [7]–[11] and various experimental techniques have been utilized, including scanning electron microscopy [12]–[14], atomic force microscopy [10], [11], [14], [15], surface profilometry [9], [10], [13], [15], [16], electron backscattered diffraction [7], [8], [10], and synchrotron X-ray microdiffraction (mXRD) [17]–[19]. Compared with other experimental techniques, synchrotron mXRD, which can penetrate a several hundred micrometer thick silicon, is able to do *in situ* strain measurements without cross section and thus no change to the mechanical boundary conditions of TSVs. Thus, mXRD is more attractive for quantitative studies of the CTE mismatch-induced thermomechanical stress and resulting copper pumping.

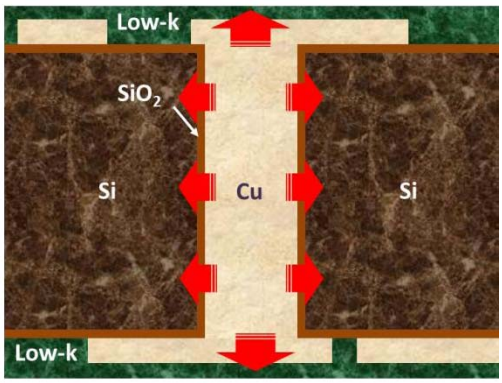

Fig. 1. CTE mismatch-induced stress in the TSV structure.

In this paper, a numerical model is developed and verified by mXRD measured strain maps. The model is then applied to analyze copper pumping and its influence on the TSV reliability and BEOL dielectric layers. In addition,

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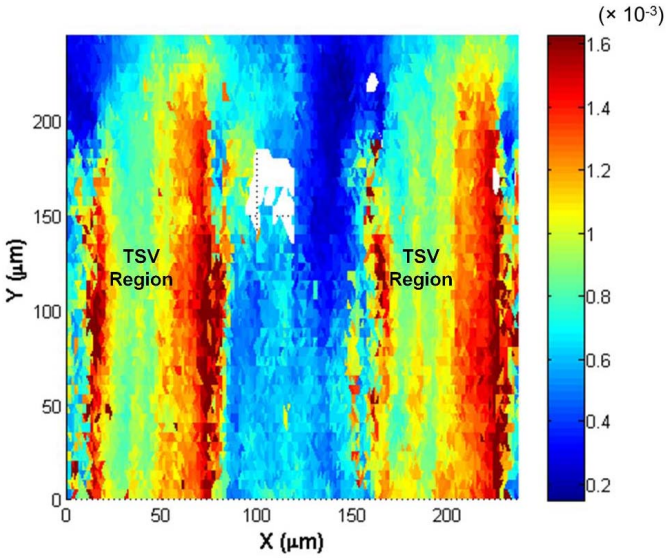


Fig. 2. Measured equivalent strain distribution map of the silicon surrounding TSVs at 150 °C.

TABLE I
MATERIAL PROPERTIES [17], [22]

	Cu	Si	SiO_2
Young's modulus (GPa)	TABLE 2	130.9	71.4
Poison ratio	0.3	0.28	0.16
CTE (ppm/°C)	17.3	2.6	0.5

a design-of-experiments (DOE)-based approach is applied to understand the effect of various geometrical and material parameters on copper pumping.

II. TSV STRESS CHARACTERIZATION

TSV *in situ* strain measurements using synchrotron mXRD were performed on Beamline 12.3.2 [20] at the Advanced Light Source, Lawrence Berkeley National Laboratory. The details about sample preparation, strain measurement, and data interpretation process can be found in [17] and [18]. Fig. 2 shows the measured 2-D equivalent strain map of silicon around two adjacent TSVs, as shown in (1), shown at the bottom of this page.

III. TSV THERMOMECHANICAL MODELING

A 3-D finite-element model with material set listed in Tables I and II has been built to simulate the aforementioned TSV fabrication and mXRD measurement conditions. To capture the process-induced stresses of the TSV samples, the thermal profiles of a standard TSV fabrication process are sequentially applied to the models. The thermal profiles are discussed in detail in [21]. In this model, all the materials are sequentially activated at their process stress-free temperature through the ANSYS element birth-and-death approach.

TABLE II
MATERIAL PROPERTIES OF Cu [22]

Young's modulus (GPa)	70
Plastic curve - Stress vs. Strain	0.003 @ 240 MPa 0.006 @ 250 MPa 0.010 @ 255 MPa 0.012 @ 255 MPa 0.020 @ 250 MPa

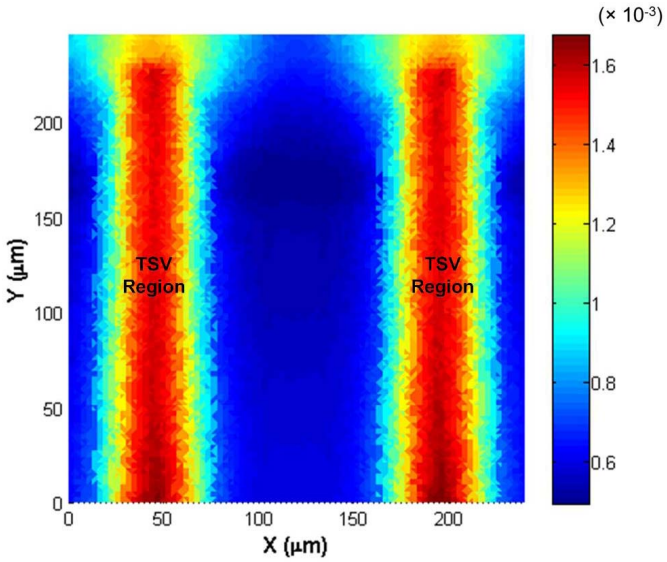


Fig. 3. Model-predicted equivalent strain distribution map of the the silicon surrounding TSVs at 150 °C.

The SiO_2 liner material is first activated stress-free at 1000 °C, which is the temperature of the thermal oxidation of silicon. Subsequently, the copper core is activated as stress-free at room temperature. Thereafter, the deviatoric strain components at 150 °C along the beam penetration direction are extracted and interpolated based on the previously proposed beam intensity-based averaging method [17], [18] to obtain strain map on the scanning plane as shown in Fig. 3. Compared with the measured strain map in Fig. 2, Fig. 3 shows that the model predicts the strain distribution well. Although there are some scattered highly strained points in the measured strain maps, which cannot be captured by the model as discussed in [18], these discrepancies do not affect the overall strain distribution.

IV. TSV COPPER PUMPING STUDY

To study the effect of copper pumping on TSV and BEOL reliability, a 2-μm-thick SiO_2 layer is added on the TSV top surface. Thereafter, the TSV temperature is ramped to solder reflow temperature at 250 °C. As shown in Fig. 4, copper tends to expand more than the surrounding silicon since the CTE of copper is about five times that of silicon. This higher CTE of copper results in copper pumping out of the TSV.

$$\varepsilon_{\text{eq}} = \frac{2}{3}\sqrt{\frac{\left(\varepsilon'_{xx}-\varepsilon'_{yy}\right)^2+\left(\varepsilon'_{yy}-\varepsilon'_{zz}\right)^2+\left(\varepsilon'_{zz}-\varepsilon'_{xx}\right)^2+6\left(\varepsilon'^2_{xy}+\varepsilon'^2_{yz}+\varepsilon'^2_{xz}\right)}{2}} \tag{1}$$

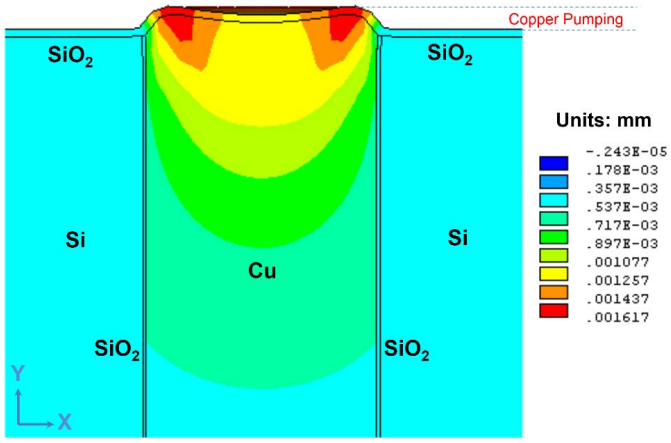


Fig. 4. Cross-sectional view of the copper pumping (U_y) at 250 °C.

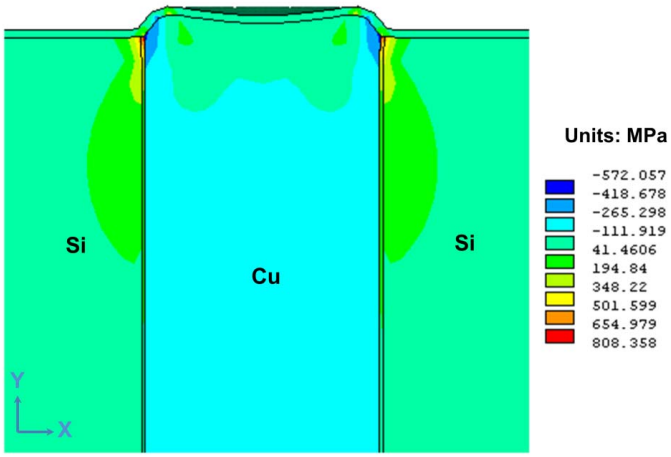


Fig. 5. Cross-sectional view of the axial stress (S_{yy}) at 250 °C.

TABLE III
FACTORS AND LEVELS OF THE DESIGN PARAMETER SCREENING FOR 3-D INTEGRATED PACKAGES

Design Factors	Levels				
TSV Pitch (μm)	80	100	120	150	200
TSV Height (μm)	50	80	100	200	300
TSV Diameter (μm)	10	20	30	40	60
Liner Thickness (μm)	0.5	1.0	1.5	2.0	3.0
Liner CTE (ppm/°C)	0.5	1.0	3.0	5.0	
Liner Modulus (GPa)	5	10	30	70	

As illustrated in Fig. 5, copper pumping leads to compressive axial stresses near the center of the copper via and tensile stress in the surrounding silicon. As shown in Fig. 6, the axial pumping force applied on the upper BEOL dielectric layer can also induce very high stress in the BEOL layer, which may eventually crack. In addition, this CTE mismatch can result in very high shear stress in the dielectric liner layer and upper BEOL layer near the via top edge (Fig. 7), which may cause interfacial cracking in these dielectric layers. Due to copper pumping at reflow temperatures, the reliability concerns include cohesive cracking of liner layer, interfacial cracking of Cu/SiO_2 interface, and top layer delamination. The plot of equivalent plastic strain (Fig. 8) indicates that Cu yielding is limited and occurs only near the via top corners.

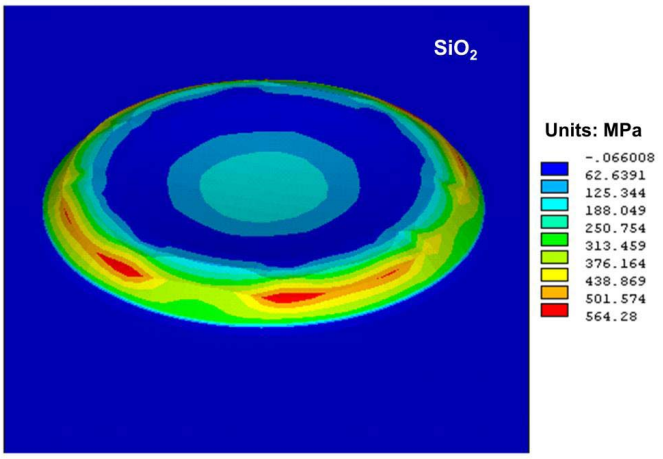


Fig. 6. Top view of the first principal stress ($S1$) in the BEOL dielectric layer at 250 °C.

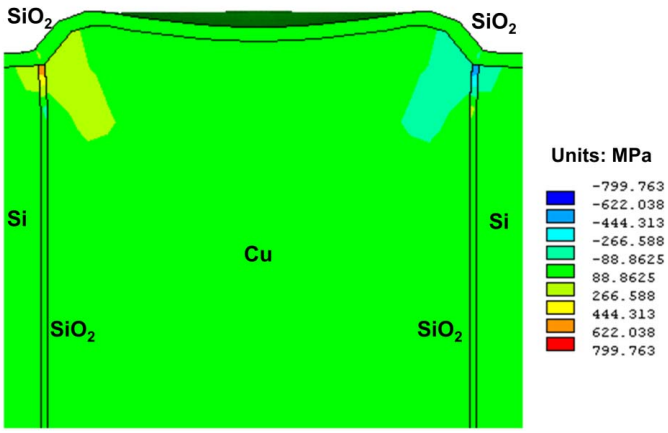


Fig. 7. Cross-sectional view of the shear stress (S_{xy}) at 250 °C.

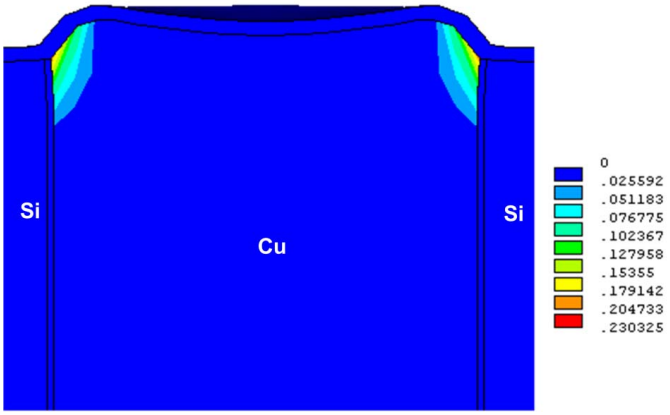


Fig. 8. Cross-sectional view of the equivalent plastic strain in the copper via at 250 °C.

V. EFFECT OF TSV GEOMETRY AND LINER MATERIAL PARAMETERS

To understand the effect of various parameters such as TSV pitch, height, diameter, liner thickness, liner CTE, and liner modulus, a DOE-based approach is implemented. As listed in Table III, for each parameter, four or five levels of values have been chosen.

TABLE IV
DOE DESIGN TABLE

Case	TSV Pitch	TSV Height	TSV Diameter	Liner Thickness	Liner Modulus	Liner CTE	Cu Pumping (um)	BEOL S1 (MPa)
1	120	50	40	3	70	1	0.408148	2.528221
2	100	100	60	1	70	5	0.986648	23.805381
3	120	300	10	1	30	0.5	0.137855	5.245288
4	100	50	10	2	5	3	0.200004	12.560467
5	200	100	40	3	30	5	0.772569	8.236905
6	120	100	20	2	30	3	0.357125	10.596249
7	200	200	10	2	30	1	0.134192	3.295228
8	150	50	60	0.5	30	0.5	0.822128	9.318335
9	100	300	20	3	5	0.5	0.623009	40.063412
10	80	100	10	0.5	5	1	0.142494	17.424649
11	100	200	40	0.5	30	1	0.819381	96.18225
12	150	200	40	1	5	3	0.871575	123.773093
13	80	300	60	3	30	3	1.160099	20.714598
14	80	50	20	1	30	5	0.2822	11.025961
15	80	200	40	2	70	0.5	0.691117	15.798026
16	200	300	20	0.5	70	3	0.300247	58.923562
17	120	200	60	0.5	5	5	1.230195	126.561145
18	200	50	60	1.5	5	0.5	0.860659	42.788378
19	150	200	10	3	70	5	0.064708	0.298968
20	150	300	40	2	5	5	1.008513	105.768185

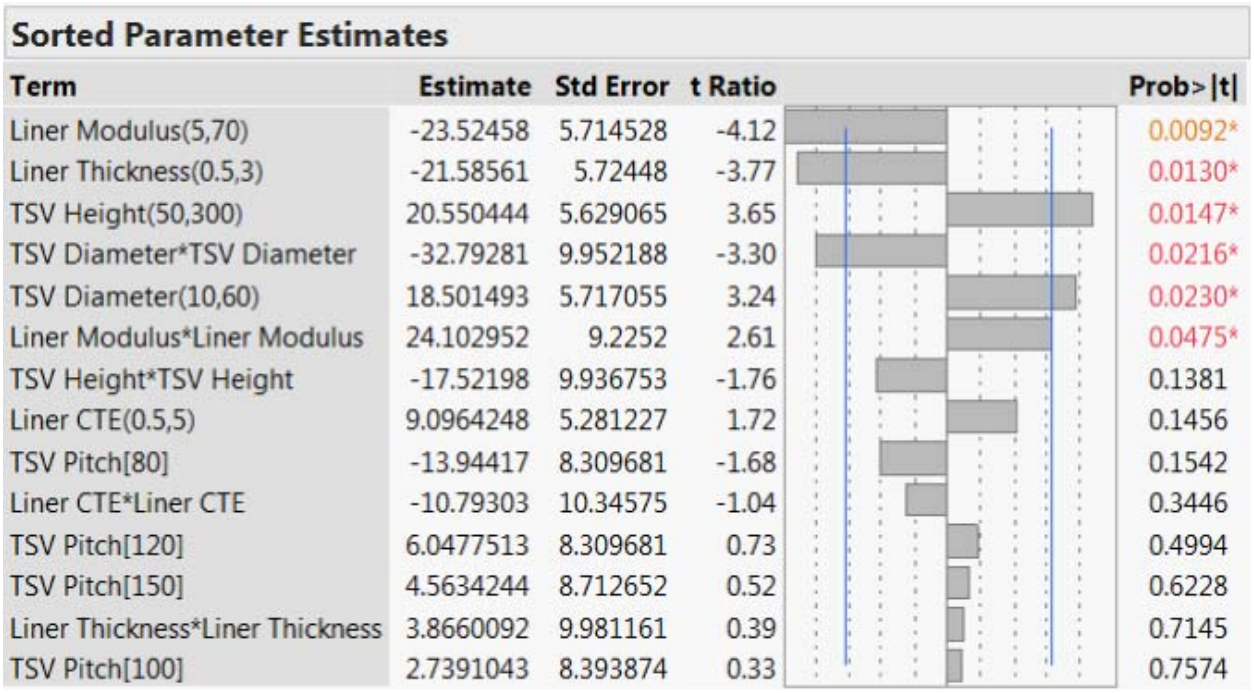


Fig. 9. Parameter effect estimate on the first principal stress of the BEOL dielectric layer.

As discussed in the previous sections, copper pumping and resulting dielectric cracking are the concern of the TSV structure at high temperatures. Therefore, copper pumping and dielectric first principal stress are used as index to compare different TSV designs in the DOE study. Here, the copper pumping amount is defined as the relative height (Fig. 4) of the extruded dielectric layer. The first principal stress of the BEOL layer is the volume-averaged value of a ring of BEOL elements above the via peripheral edge. Using the JMP software, 20 designs (Table IV) are generated from design factors and levels in Table III. As shown in Table IV, copper pumping values and BEOL first principal stress have been read out from the numerical models and input into JMP for parametric analysis.

Fig. 9 shows the effect test based on the response of the first principal stress in the BEOL dielectric layer. The dominating

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
TSV Diameter(10,60)	0.4508627	0.014254	31.63	<.0001*
TSV Height(50,300)	0.1209517	0.014034	8.62	0.0003*
Liner Modulus(5,70)	-0.11837	0.014247	-8.31	0.0004*
Liner CTE(0.5,5)	0.0591927	0.013167	4.50	0.0064*
TSV Diameter*TSV Diameter	-0.097129	0.024813	-3.91	0.0112*
TSV Pitch[100]	0.0809752	0.020928	3.87	0.0118*
TSV Height*TSV Height	-0.065743	0.024774	-2.65	0.0452*
TSV Pitch[150]	-0.038213	0.021722	-1.76	0.1389
Liner Thickness(0.5,3)	0.0141505	0.014272	0.99	0.3670
TSV Pitch[120]	-0.019811	0.020718	-0.96	0.3829
TSV Pitch[80]	0.015836	0.020718	0.76	0.4791
Liner Thickness*Liner Thickness	-0.014339	0.024885	-0.58	0.5894
Liner Modulus*Liner Modulus	0.0016071	0.023	0.07	0.9470
Liner CTE*Liner CTE	-0.00042	0.025794	-0.02	0.9876

Fig. 10. Parameter effect estimate on copper pumping.

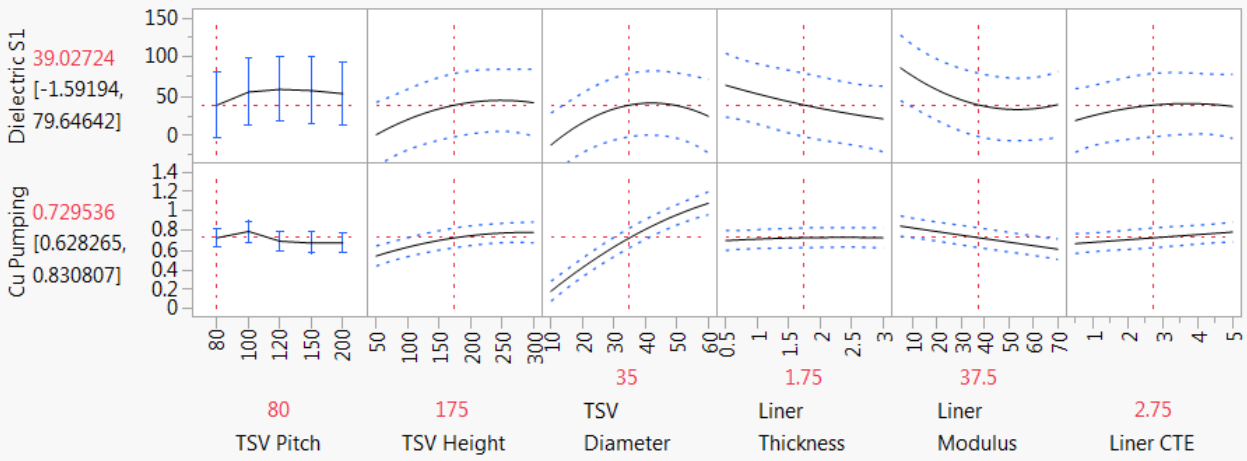


Fig. 11. Factor profiling results of copper pumping and BEOL dielectric principal stress (units: MPa).

factors affecting the dielectric stress are liner material Young's modulus, liner thickness, TSV height, and TSV diameter. On the other hand, as Fig. 10 shows, if the response of the copper pumping is considered, the dominating factors change to TSV diameter, TSV height, liner material Young's modulus, liner CTE, and TSV pitch. Comparison of the two kinds of responses in Figs. 9 and 10 indicates that copper pumping is dominated by TSV geometrical parameters. However, BEOL dielectric stress has more likely been affected by the properties of the neighboring structure of the copper protrusion region.

As illustrated in Fig. 11, the factor profiling results indicate that reducing the TSV diameter and TSV height (silicon thickness) generally decreases copper pumping and BEOL stress. This is good news for the current trend of microelectronics miniaturization with more I/O and thinner silicon dies.

VI. Conclusion

In situ microscale strain measurements by synchrotron mXRD, which does not change the TSV mechanical boundary condition, are ideal for TSV copper pumping study and TSV model calibration. Comprehensive thermomechanical numerical analysis indicates that copper pumping occurs at higher temperature. It can result in high stresses in the TSV and upper BEOL layer, especially near the via top edges. These high stresses can induce liner dielectric cracking, BEOL cracking, and interfacial separation. Further DOE parametric study shows that reducing the TSV size and height is very

effective to reduce copper pumping and mitigate stress in the BEOL dielectric layer.

REFERENCES

[1] J. U. Knickerbocker *et al.*, "2.5D and 3D technology challenges and test vehicle demonstrations," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 1068–1076.

[2] M. S. Bakir and J. D. Meindl, *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*. Norwood, MA, USA: Artech House, 2008.

[3] J. H. Lau, "Overview and outlook of through-silicon via (TSV) and 3D integrations," *Microelectron. Int.*, vol. 28, no. 2, pp. 8–22, 2011.

[4] X. Liu, Q. Chen, V. Sundaram, S. Muthukumar, R. R. Tummala, and S. K. Sitaraman, "Reliable design of electroplated copper through silicon vias," in *Proc. ASME Int. Mech. Eng. Congr. Expo. (IMECE)*, Vancouver, BC, Canada, 2010, pp. 497–506.

[5] X. Liu, Q. Chen, P. Dixit, R. Chatterjee, R. R. Tummala, and S. K. Sitaraman, "Failure mechanisms and optimum design for electroplated copper through-silicon vias (TSV)," in *Proc. 59th Electron. Compon. Technol. Conf.*, San Diego, CA, USA, May 2009, pp. 624–629.

[6] X. Liu, Q. Chen, V. Sundaram, R. R. Tummala, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test," *Microelectron. Rel.*, vol. 53, no. 1, pp. 70–78, Jan. 2013.

[7] J. Auersperg, D. Vogel, E. Auerswald, S. Rzepka, and B. Michel, "Nonlinear copper behavior of TSV and the cracking risks during BEoL-built-up for 3D-IC-integration," in *Proc. 13th Int. Conf. Thermal, Mech. Multi-Phys. Simulation Experim. Microelectron. Microsyst. (EuroSimE)*, Apr. 2012, pp. 1–6.

[8] F. X. Che, W. N. Putra, A. Heryanto, A. Trigg, S. Gao, and C. L. Gan, "Numerical and experimental study on Cu protrusion of Cu-filled through-silicon vias (TSV)," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Jan./Feb. 2011, pp. 1–6.

[9] J. De Messemaeker *et al.*, "Impact of post-plating anneal and through-silicon via dimensions on Cu pumping," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 586–591.

[10] A. Heryanto *et al.*, "Effect of copper TSV annealing on via protrusion for TSV wafer fabrication," *J. Electron. Mater.*, vol. 41, no. 9, pp. 2533–2542, Sep. 2012.

[11] T. Jiang *et al.*, "Plasticity mechanism for copper extrusion in through-silicon vias for three-dimensional interconnects," *Appl. Phys. Lett.*, vol. 103, no. 21, p. 211906, 2013.

[12] P. Kumar, I. Dutta, and M. S. Bakir, "Interfacial effects during thermal cycling of Cu-filled through-silicon vias (TSV)," *J. Electron. Mater.*, vol. 41, no. 2, pp. 322–335, Feb. 2012.

[13] D. Zhang, K. Hummler, L. Smith, and J. J.-Q. Lu, "Backside TSV protrusion induced by thermal shock and thermal cycling," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 1407–1413.

[14] C. Okoro *et al.*, "Elimination of the axial deformation problem of Cu-TSV in 3D integration," in *Proc. AIP Conf.*, vol. 1300. 2010, pp. 214–220.

[15] I. De Wolf *et al.*, "Cu pumping in TSVs: Effect of pre-CMP thermal budget," *Microelectron. Rel.*, vol. 51, nos. 9–11, pp. 1856–1859, Sep./Nov. 2011.

[16] S. Kang *et al.*, "TSV optimization for BEOL interconnection in logic process," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Jan./Feb. 2012, pp. 1–4.

[17] X. Liu *et al.*, "Thermomechanical strain measurements by synchrotron X-ray diffraction and data interpretation for through-silicon vias," *Appl. Phys. Lett.*, vol. 103, no. 2, p. 022107, 2013.

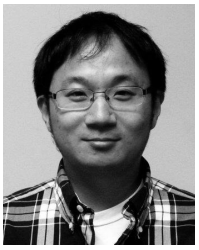
[18] X. Liu *et al.*, "*In-situ* microscale through-silicon via strain measurements by synchrotron X-ray microdiffraction exploring the physics behind data interpretation," *Appl. Phys. Lett.*, vol. 105, no. 11, p. 112109, 2014.

[19] C. Okoro, L. E. Levine, R. Xu, and Y. Obeng, "Experimental measurement of the effect of copper through-silicon via diameter on stress buildup using synchrotron-based X-ray source," *J. Mater. Sci.*, vol. 50, no. 18, pp. 6236–6244, Sep. 2015.

[20] M. Kunz *et al.*, "A dedicated superbend X-ray microdiffraction beamline for materials, geo-, and environmental sciences at the advanced light source," *Rev. Sci. Instrum.*, vol. 80, no. 3, pp. 035108-1–035108-10, 2009.

[21] X. Liu *et al.*, "Dimension and liner dependent thermomechanical strain characterization of through-silicon vias using synchrotron X-ray diffraction," *J. Appl. Phys.*, vol. 114, no. 6, p. 064908, 2013.

[22] D. T. Read, Y. W. Cheng, and R. Geiss, "Morphology, microstructure, and mechanical properties of a copper electrodeposit," *Microelectron. Eng.*, vol. 75, no. 1, pp. 63–70, Jul. 2004.



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