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IRVINE

Dual Resonant Switched-Capacitor Polarity Inverter

THESIS

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by

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ABSTRACT OF THE THESIS

Dual Resonant Switched-Capacitor Polarity Inverter

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This thesis presents a new dual resonant switched-capacitor converter topology that inverts the polarity of input voltages and can regulate the gain continuously between 0 and –1, even at light load operation. A literature review on the development and improvement of switched-capacitor converters over the years is presented in Chapter 1. The switched capacitor in the presented converter is charged and discharged through resonant inductors, eliminating large current spikes and charge sharing losses associated with pure switched-capacitor converters. This resonance allows for ZCS turn-on of all switches and ZCS turn-off of all diodes. Chapter 2 presents a detailed analysis of the dual resonant switched-capacitor polarity inverter, in which a voltage gain curve in four distinct operating modes is provided, along with a detailed discussion of boundary conditions between modes. Voltage and current stresses of all components are analyzed, and design guidelines for designing the presented converter from a specified input voltage, output voltage, and output power are presented. In addition, a regenerative snubber to eliminate undesirable parasitic ringing is provided. An 80V to –35V ~ –72V open loop prototype with peak efficiency 97.0% and maximum power 120W was built to verify the operation of the converter, and the experimental results from this prototype are presented in Chapter 3. Finally, in

Chapter 4, several extensions of the topology are presented to reduce the step-down ratio of the converter or to apply the topology to step-up applications.

INTRODUCTION

This thesis is part of a long tradition in the field of power electronics of pushing simultaneously for regulation, efficiency, and power density, three goals that are very often at odds. Conventional PWM converters are easy to regulate via duty cycle modulation. Over the years, the bulk of power electronics research has focused on PWM converters, leading to new switching methods and topologies that allow for efficiencies upwards of 99%. Today, inductor based PWM converters are still the work horses of a majority of applications. However, PWM converters require magnetic components to store energy via large DC bias currents, and thus often require air gaps, concentrated or distributed, to avoid saturation. These magnetic components constrain the power density of PWM converters and have spurred a push towards operating at higher and higher frequencies. This in turn has created a demand for new semiconductor components, made from materials such as SiC and GaN, as designers begin to run up against the high frequency limitations of Si power devices. The push for higher frequencies is also challenged by core loss in magnetic components, which increase with frequency.

Employing resonance has been a common approach in improving efficiency and power density in power converters. Resonant converters use resonant tanks to regulate voltage gain by modulating the switching frequency. The tank presents a capacitive or inductive impedance to an inverter, allowing the switches to achieve either zero-current switching (ZCS) or zero-voltage switching (ZVS). Hybrid PWM-resonant switching methods have also been devised to introduce ZVS or ZCS into existing PWM converters via a hybrid switching cell. Resonant converters do reduce switching losses, but often increase conduction losses as large rms currents flow in the tank. Many resonant converters also have issues with circulating currents at light load, leading to low efficiency and difficult regulation.

It is extremely desirable to get rid of bulky magnetic components. Switched-capacitor converters (SCCs) rose to the occasion with the promise of small size and lightweight designs. However, large transient current spikes during the charging and discharging of capacitors lead to EMI issues and limit the efficiency of SCCs. SCCs also have little to no regulation capability, unless one is willing to sacrifice efficiency for regulation. Resonant switched-capacitor converters (RSCCs) use small inductors to reshape these current spikes into sinusoids, eliminating one important issue and increasing efficiency, but they do little to address the problem of regulation. Thus, while excelling in the areas of power density and efficiency, RSCCs are far behind resonant and PWM converters in terms of regulation.

The subject of this thesis, the dual resonant switched-capacitor polarity inverter, is a topology that falls into the new class of RSCC topology referred to as dual resonant switched-capacitor converters pioneered by Dr. Slobodan Ćuk. These converters are based on SCC topologies, but employ resonances for the charging and discharging of the capacitor(s), and thus simultaneously achieve high efficiency, high power density, and, crucially, regulation capability, even at light load. The DRSC polarity inverter can be used in applications that require a negative power supply rail to be derived from a positive supply rail for a wide range of power levels. There are of course important drawbacks as well that will be discussed and addressed, such as parasitic ringing and large switching losses at high frequencies. The detailed operation of this converter will be analyzed in Chapter 2, and experimental verification will be presented in Chapter 3. In addition, this thesis will provide guidelines for designing a DRSC polarity inverter from a specified input voltage, output voltage, and output power. Topological extensions for smaller step-down ratios and for step-up applications are discussed in Chapter 4.

CHAPTER 1: Literature Review

Pure Switched-Capacitor Converters

Some of the earliest examples of switched-capacitor circuits being used as a means for power control arose in the 1970s [1] [2]. In Fig. 1.1 from [1], a four switch SC cell is used as a variable impedance to control the power delivered from the DC source E to the load Z_L. A similar concept is presented in [2] for motor control. The issue of regulation via modulating output impedance is an ever-present issue with SC power converters. Charging capacitors with other capacitors at even slightly different voltages is an inherently lossy process, as any electrical engineering student who has encountered the infamous "capacitor charging paradox", in which half of the initial energy on a capacitor is lost after charging another capacitor with no initial charge. In the literature, this loss is referred to as charge sharing loss [3], and is often a limiting factor on the efficiency of an SC converter. This charging is also done by means of a large current spike that exponentially decays. In practice, this current spike may be large enough to damage switches and cause EMI issues.

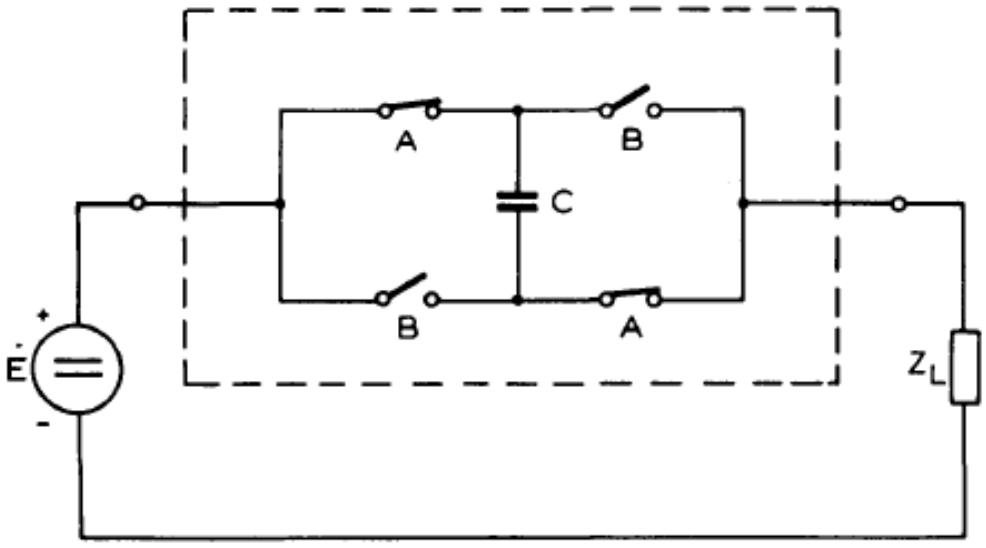


Fig. 1.1: Early example of SC circuits used in power regulation. Figure from [1].

Nevertheless, power electronics researchers were attracted to SC converters due to the potential for light weight and high power density when compared to traditional PWM converters requiring bulky magnetic components. Some of the earliest work on SC DC-DC converters as we know them today began in Kumamoto, Japan in the early 1980s [4]–[6]. These converters were typically limited to under 10W and efficiencies of below 90%. While the authors of [4] claim that their converter is regulated, this regulation comes at the cost of drastically reducing the efficiency. In fact, the authors themselves refer to the converter as a "switched-capacitor transformer", suggesting they understood the device to have a practically fixed voltage gain. Many varieties of SC converter emerged out of their and other researchers' work [7]. A collection of common SC DC-DC converters are shown in Figs 1.2 and 1.3.

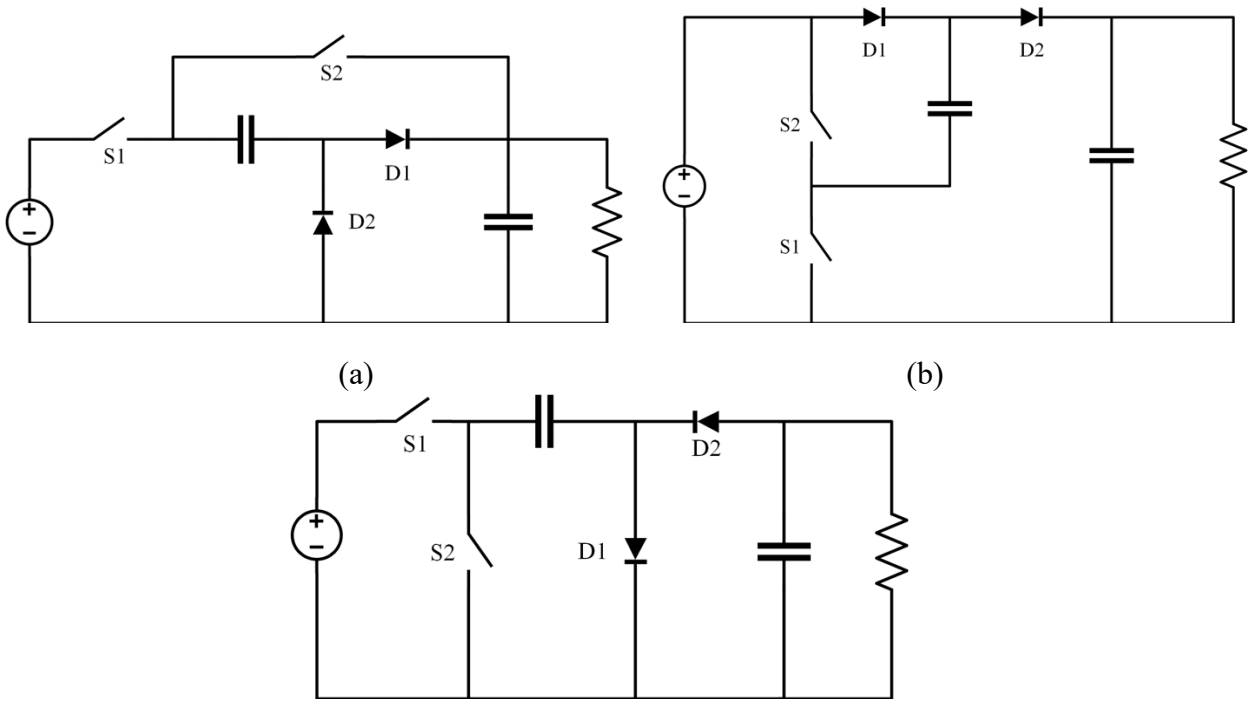


Fig. 1.2: Three common SC DC-DC converters: (a) 1/2X step-down converter, (b) 2X step-up converter, and (c) polarity inverter.

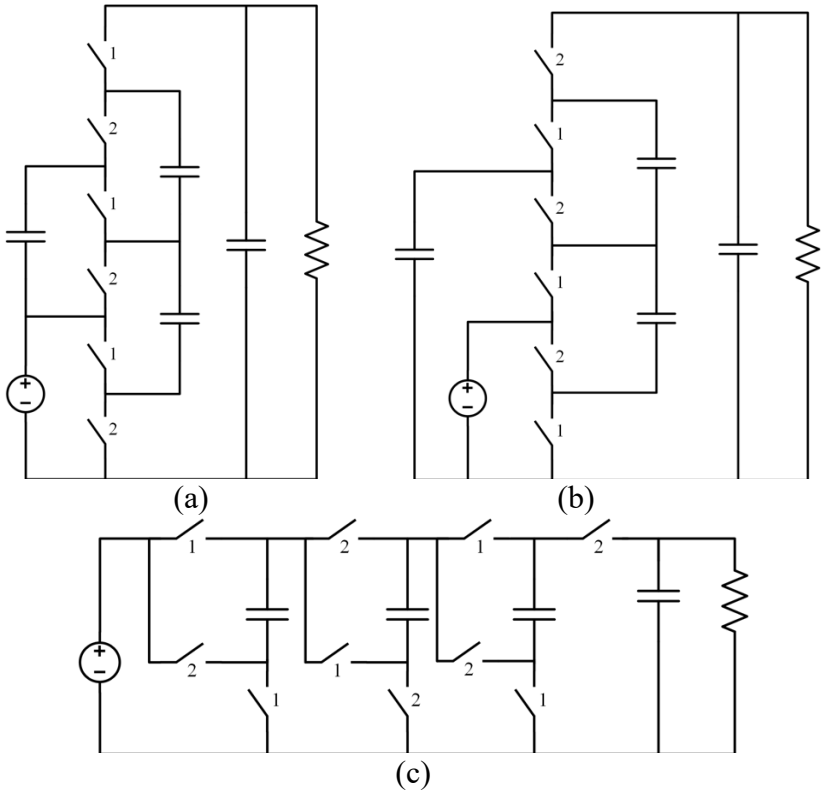


Fig. 1.3: Three common SC DC-DC converters: (a) 3X ladder converter, (b) 3X Dickson converter, and (c) 5X Fibonacci converter.

The converter in Fig. 1.2a operates by charging the switched capacitor in series with the output voltage, then discharging it in parallel, leading to the output being equal to one half of the input. Similarly, the converter in Fig. 1.2b charges the switched capacitor in parallel with the input voltage, then discharges it in series with the input voltage, thus doubling the input voltage. The converter in Fig. 1.2c charges switched capacitor to the input voltage, then discharges in parallel with the output, but with the opposite polarity, leading to a gain of –1.

The converters in Fig 1.3 are examples of slightly more complicated SC DC-DC converters. Only the step-up version of each converter is shown, but they can be converted to step-down as well. The ladder converter in Fig. 1.3a charges the capacitor on each rung in parallel with the previous rung, meaning the voltage stress is equally shared among all capacitors and is equal to the input voltage. The Dickson converter in Fig. 1.3b works similarly, except

there is a bypass capacitor that is charged to twice the input voltage. There are alternate versions of the Dickson converter that distribute the capacitor voltage stress differently as well. The Fibonacci converter in Fig. 1.3c works by charging each capacitor with the series combination of the two stages before it, hence leading to a gain that is equal to the *k*th Fibonacci number for *k* capacitors (indexing the first 1 in the Fibonacci sequence at 0). In this case there are 4 capacitors, so the gain is 5. In fact, Makowski and Maksimovic proved in [8] that the maximum achievable gain of any two-phase DC-DC SC converter with *k* capacitors is the *k*th Fibonacci number. While the Fibonacci converter can achieve large gains with relatively few capacitors, it has the disadvantage that the voltage stress on each capacitor also increases with the Fibonacci sequence.

Many more SC DC-DC converter topologies have arisen but have mostly been limited to low power applications by the inherent drawbacks of SC converters. In [9], Seeman and Sanders showed that every SC DC-DC converter can be modeled as a fixed DC transformer with a lossy output impedance. They also showed that this impedance can be modulated with frequency and duty cycle, thus demonstrating that the only way to regulate SC DC-DC converters is by increasing the output impedance, and thus lowering the efficiency.

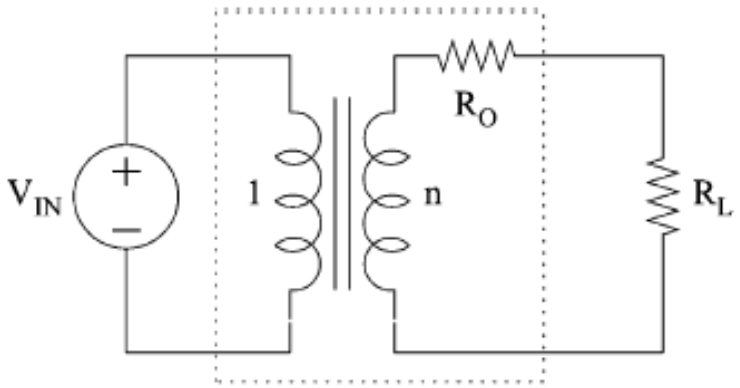


Fig. 1.4: In [9], Seeman and Sanders showed that all SC DC-DC converters can be modeled as fixed transformer followed by an output impedance. Figure from [9].

Hybrid PWM-SC Converters

The issues of pure SC converters were not lost on early SC researchers. In fact, the same Japanese group that was among the first groups to research SC converters was also among the first groups of researchers to try to address the issues of large current spikes and poor regulation. The natural point of entry in resolving these issues was hybridization with PWM converters, which have large inductors that conduct relatively constant current and achieve regulation very easily. In [10] and [11], one or two of the switches in the three basic SC DC-DC converters of Fig. 1.2 are replaced with large, low-ripple inductors, as shown in Fig. 1.5. All of these hybridizations have the desired affect of achieving voltage regulation. The converters on the rightmost portion of Fig 1.5 also achieve soft charging and discharging of the capacitors, as there is an inductor in both the charging and discharging path of the capacitor.

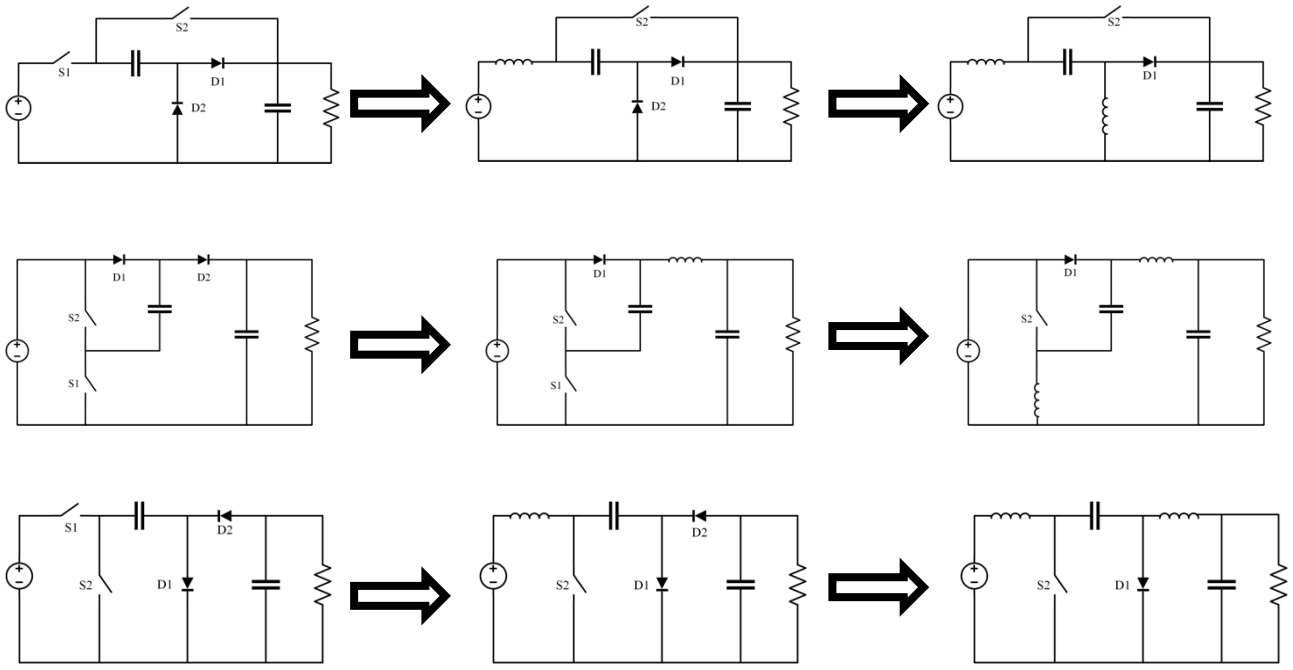


Fig. 1.5: Hybridizing the basic SC DC-DC converters in Fig 1.2.

While these hybrid PWM-SC converters achieve their goal of voltage regulation and eliminating current spikes, it comes at the cost of drastically reducing the power density compared to their pure SC counterparts. This is because the inductors store DC energy, and thus must be large and often air-gapped as in a PWM converter. In fact, the converter that results from the hybridization of an SC polarity inverter in Fig 1.5 is the well-known Ćuk converter. Thus, these first attempts at hybrid PWM-SCs fail to retain some of the chief advantages of SC converters, such as high power density and light weight.

In recent years, hybrid PWM-SC converters have emerged when approached from the PWM side, in other words, using switched-capacitor cells to extend the voltage gain of PWM converters, as opposed to using features of PWM converters to improve SC converters through hybridization. For example, in [12], a converter deemed a "hybrid DC-DC buck converter" was presented. This converter was created by observing that the bottom rung of a SC step-down ladder converter resembles a half-bridge with an input equal to the output voltage of the converter. Since the input to a buck converter is a DC voltage followed by a half-bridge, the authors combined the two converters at this point, resulting in the converter shown in Fig. 1.6 below. Just as with a ladder converter, the step-down ratio can be further reduced by adding more rungs with more capacitors. However, the capacitors in the SC cell are still connected in parallel as in a pure SC converter during their charging and discharging. Thus, although regulation can be achieved by duty cycle modulation, an ideal operating region of near $D = 0.5$ is recommended by the authors to avoid lowering the efficiency via increasing the output impedance of the SC cell. This converter, as with the converters in [10] and [11], also uses a large, low-ripple inductor at its output, meaning the power density is limited.

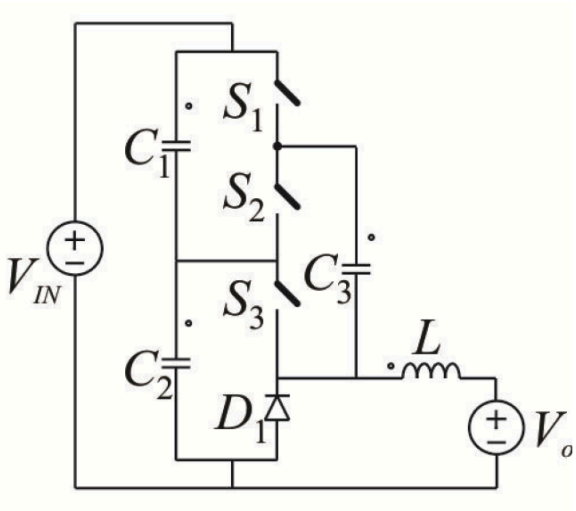


Fig. 1.6: Hybrid DC-DC buck converter. Figure from [12].

In [13], the authors observed that several common PWM converters, such as the Ćuk, SEPIC, and Zeta converters, can themselves be viewed as hybrid PWM-SC converters, since the main means of energy transfer between input and output is capacitive. Utilizing this fact, they replaced the capacitor in these converters with a step-down SC cell to allow for smaller step-down ratios. The result for the Ćuk converter is shown in Fig. 1.7 below. C_1 and C_2 are first charged in series, then discharged in parallel, reducing the voltage gain of the converter by a factor of ½. The gain is still easily regulated by modulating the duty cycle. In addition, unlike in [12], both the charging and discharging of the capacitors is via low-ripple inductors, eliminating undesirable current spikes. However, once again bulky magnetics are required to realize this converter. The authors in [13] also present a method for replacing the inductors with switched inductor cells to extend the voltage gain, but the resulting converters have an uncommon ground between their input and output, and also require even more low-ripple inductors for their realization.

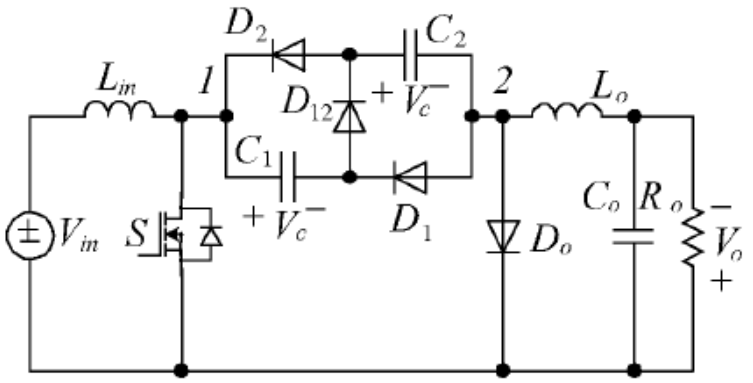


Fig. 1.7: Result of replacing the capacitor in a Ćuk converter with a step-down SC cell. Figure from [13].

Whereas the previous examples of hybridization observed a commonality between SC and PWM converters and hybridized based on that commonality, another common approach to hybridization is merely attaching an SC cell at the input or output of a PWM converter to extend the voltage gain. An example of this is [14], in which an SC cell is inserted at the output of a boost converter to extend the voltage gain. The SC cell still has large current spikes, but the gain of the converter is easily regulated. The boost inductor is once again required to be a bulky, low-ripple PWM inductor.

In general, hybrid PWM-SC converters are an effective method of extending the voltage gain of PWM converters, but do not retain many advantages of SC converters. In particular, the requirement of bulky magnetic components, similarly sized to those in regular PWM converters, limits the power density of these converters unless they are operated at very high frequencies. High frequency operation introduces a whole new set of issues, especially if the SC cell of the hybrid PWM-SC converter in question exhibits large current spikes during charging and/or discharging.

Resonant Switched-Capacitor Converters

In 1998, researchers in Hong Kong introduced a new type of switched-capacitor converter that eliminates the current spikes between charging capacitors while maintaining comparable power density and achieving ZCS for all switches and diodes [15]. These converters were derived by inserting a small resonant inductor in series with the capacitor in each of the basic SC DC-DC converters from Fig 1.2. The resulting converters are shown in Fig. 1.8 below. When operated at the resonant frequency with duty cycle $D = 0.5$, the current through the resonant network is a sinusoid, and every switch is turned on and off with ZCS. The resonant inductor can be small, both in inductance and in physical size, as it does not carry low-ripple current or store DC energy. Thus, resonant switched-capacitor converters (RSCCs) successfully eliminate current spikes without suffering a large reduction in power density. The three converters in Fig 1.8 were extended to larger or smaller voltage gains in [16].

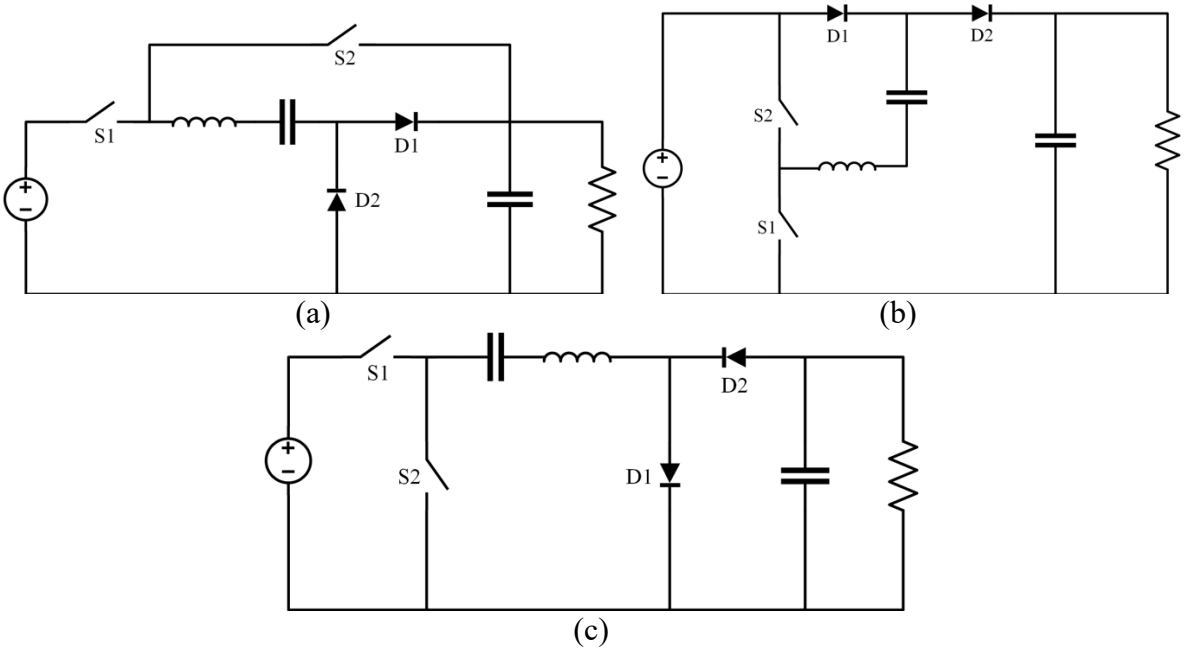
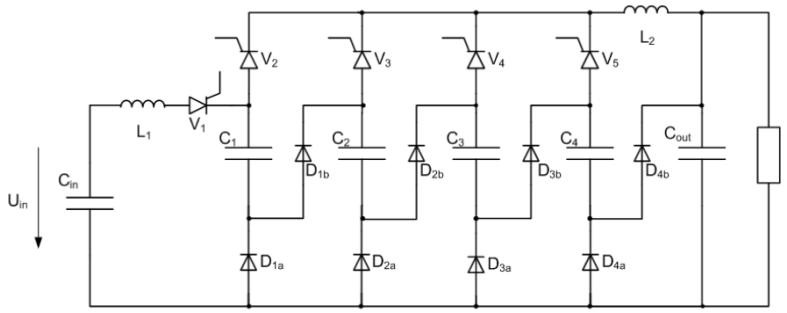
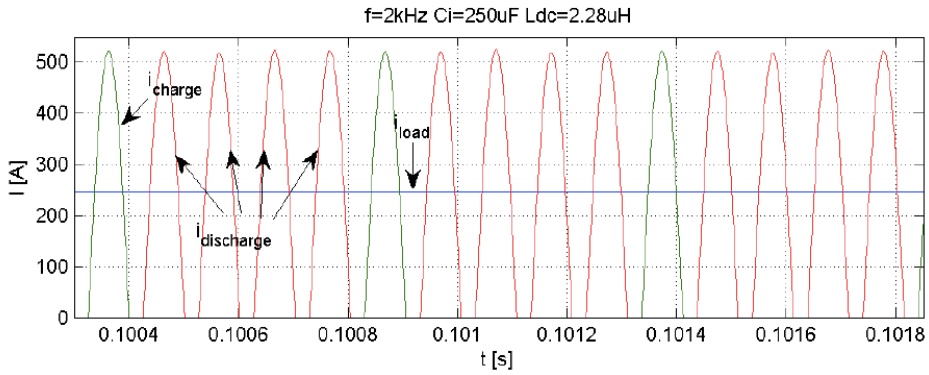


Fig. 1.8: Resonant versions of the basic SC DC-DC converters from Fig 1.2: (a) resonant 1/2X step-down, (b) resonant 2X step-up, and (c) resonant polarity inverter.

In both [15] and [16], the goal of introducing the resonant inductor was solely to eliminate current spikes and achieve ZCS, rather than to achieve regulation capability. The author in [15] specifically mentions that voltage regulation is poor, but slightly better than a pure SC converter. Nevertheless, researchers were attracted to RSCCs, as the soft switching and soft charging allowed them to take high power density SC topologies to much higher power applications. For example, in [17], a 12.5kW prototype of the topology shown in Fig. 1.9a was built. The step-down converter resonantly charges the capacitors in series, then discharges them in an interleaved fashion to the output, thus making the output current four times the input current. This converter also has poor regulation capability, and in fact was designed to be used open loop. Regardless, it demonstrates the capability of RSCCs to operate at much higher powers than possible with their pure SC counterparts.



(a)



(c)

Fig. 1.9: (a) Topology of converter in [17] and (b) the resonant inductor current waveforms. Figure from [17].

In [18], an interesting combination of RSC and hybrid PWM-SC is presented. The converter is basically two ladder converters interleaved and used as the inputs to a two-phase buck converter. However, the two inductors of the buck converter have been combined into a coupled inductor, and the leakage inductance is used as a resonant inductor for soft charging and discharging of the capacitors. The topology is shown in Fig. 1.10 below. This converter achieves very high efficiencies of around 99%, but as in [17] was designed for open-loop operation and has limited regulation capability.

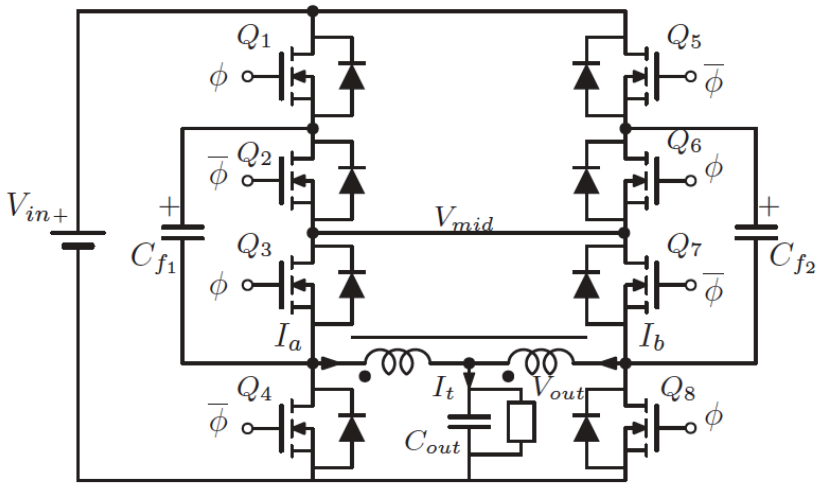


Fig. 1.10: Topology of converter presented in [18]. Figure from [18].

There have been attempts at designing RSCCs in which regulation can be achieved. One example is the converter presented in [19], which is a resonant version of the two-switch boosting switched-capacitor (TBSC) converter presented in [20]. The topology from [19] is shown in Fig 1.11. The authors in this paper completed a detailed analysis of the voltage gain of the converter as a function of switching frequency. The overall characteristic of the voltage gain is similar to a series resonant converter, that is to say regulation can be achieved at heavy load by modulating the switching frequency, but becomes much more difficult at light load. An important result from this paper is that the efficiency of the converter did not drop proportionally

with the drop in voltage gain, as shown in Fig. 1.12. This shows that the limited regulation that is available with RSCCs is not solely via modulation of the output impedance, as it is in pure SCCs.

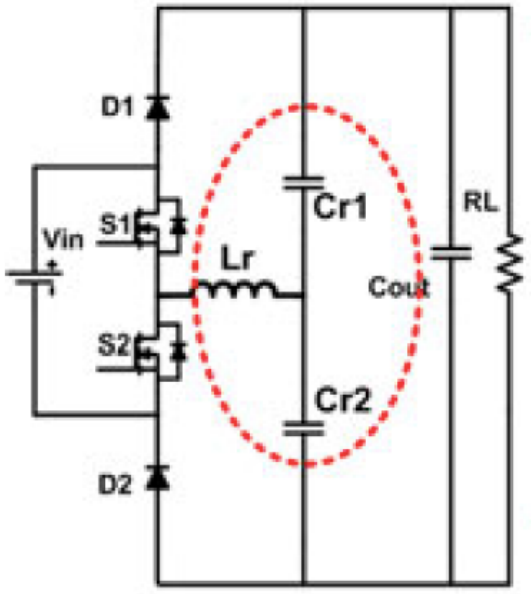


Fig. 1.11: 2X resonant TBSC topology from [19]. Figure from [19].

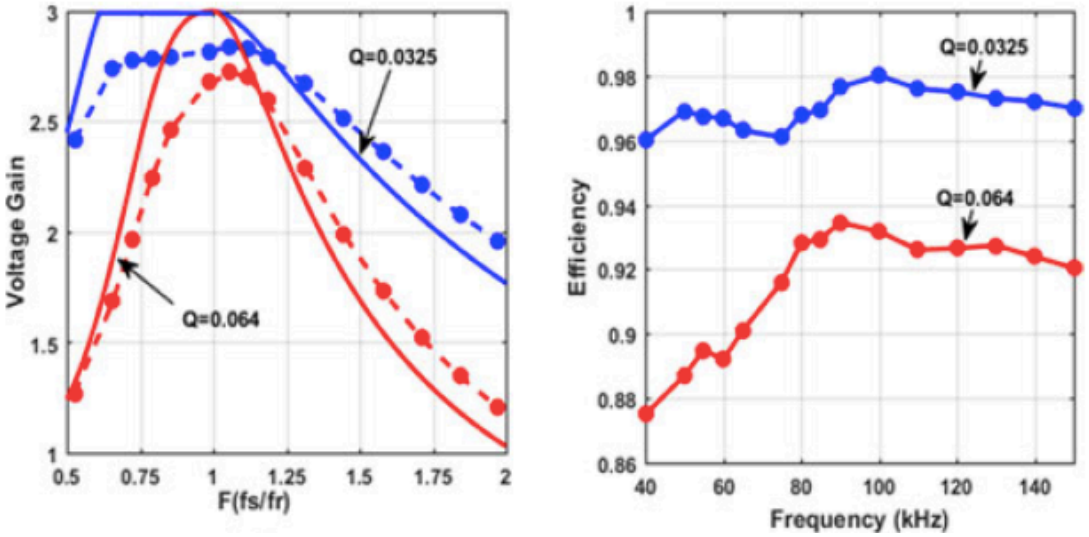


Fig. 1.12: Experimental voltage gain and efficiency versus switching frequency from [19]. Figure from [19].

This point is further underscored by [21], in which the output impedance of an RSCC and its non-resonant counterpart are analyzed in detail, resulting in the plot in Fig. 1.13. As it is shown, near the resonant frequency, the output impedance of the RSCC is much smaller than that of the SCC. Typically pure SCCs are operated at frequencies where the output impedance begins to flatten off to its fast switching limit (FSL), and can be regulated by lowering the frequency and increasing the output impedance. Interestingly, Fig. 1.13 shows that as the switching frequency is increased, the output impedance of RSCCs also increases. Intuitively this makes some sense, as above the resonant frequency the inductance begins to dominant the impedance of the resonant network. But as Fig. 1.12 showed, the efficiency does not drop proportionally with the gain as the switching frequency is increased. This suggests that if an RSCC were modeled using the same model as Fig. 1.4, the regulation that is achieved is done by modulating both the "turns ratio" of the virtual transformer as well as modulating the output impedance.

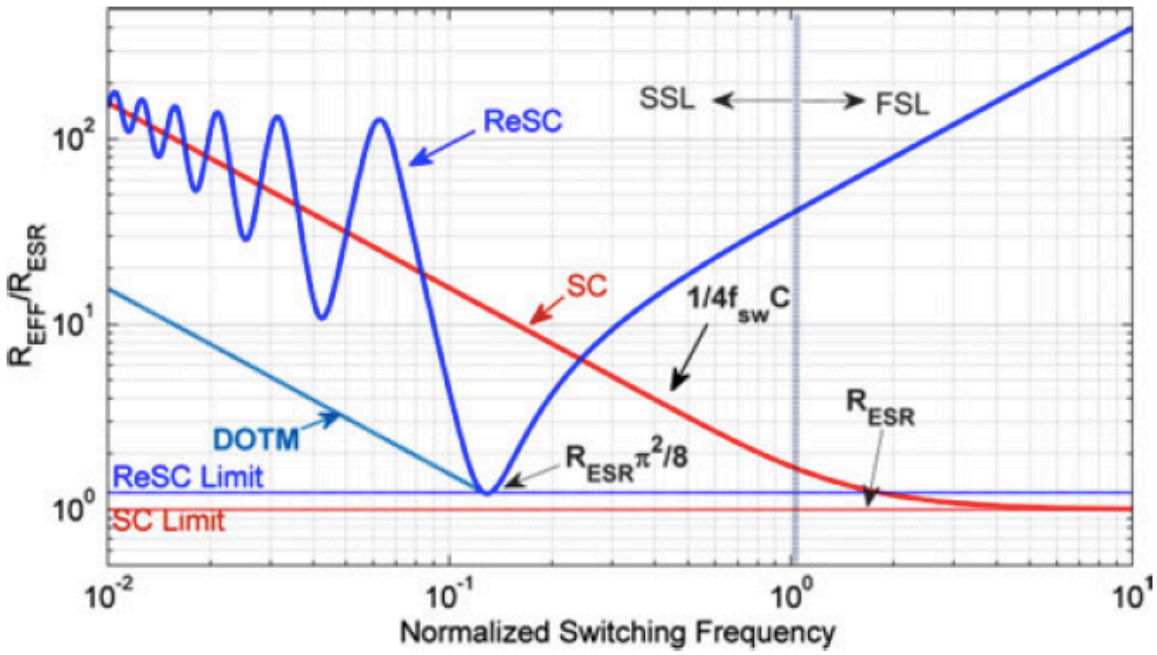


Fig. 1.13: Output impedance of an RSCC and its non-resonant counterpart. Figure from [21].

Dual Resonant Switched-Capacitor Converters

In 2012, Dr. Slobodan Ćuk patented a new technology that has since been deemed dual resonant switched-capacitor converters [22]. The first dual resonant switched-capacitor converter (DRSCC) was made in a similar way to the converters in Fig. 1.8. However, instead of inserting an inductor in series with the capacitor of an SC converter, Dr. Ćuk inserted two inductors into the circuit of Fig 1.2a, one in the charging path of the capacitor, and one in the discharging path. The result is shown in Fig. 1.14 below. At first glance the presence of an inductor in series with a switch may seem troubling, but the converter is designed to be operated with fixed off-time, such S2 is always turned on and off at zero current. Because there is no inductor in series with the resonant capacitor, the sinusoidal charging current can be cut short with no issue. The inductor L_{r1} then sees the DC output voltage, discharging its remaining energy to the load, while the resonant capacitor discharges to the load through L_{r2}. In this way, the input and output current waveforms can be shaped, and voltage regulation can be achieved through fixed off-time variable frequency modulation. Since the inductors do not store DC energy, they can be small as in an RSCC. Hence, the step-down DRSCC achieves voltage regulation and eliminates current spikes, while retaining the high power density of SCCs and RSCCs. The voltage gain of the step-down DRC is limited to the range 0 to ½ by the underlying SCC topology.

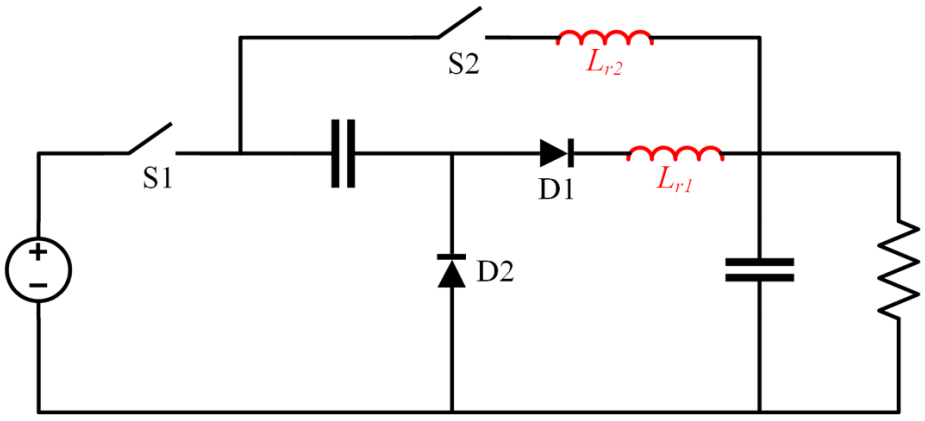


Fig. 1.14: Dual resonant switched-capacitor step-down converter topology (patented in [22]).

The DRSCC concept has been extended to step-up applications as well in [23], by observing that the same process can be applied to the 2X step-up converter from Fig 1.2b. The result is shown in Fig 1.15. The gain of this converter is limited to the range 1 to 2. The authors in [23] also provided several topological extensions that increase the voltage gain via additional SC stages in front of the resonant cell. The SC stages introduce large current spikes during the charging of the additional capacitors, limiting the practical use of these extensions. Fig. 1.16 shows an example of this issue. Extensions of the step-down DRC in Fig. 1.14 are similarly difficult to realize, due to the resonant inductors being embedded in the charging and discharging circuits of just one capacitor.

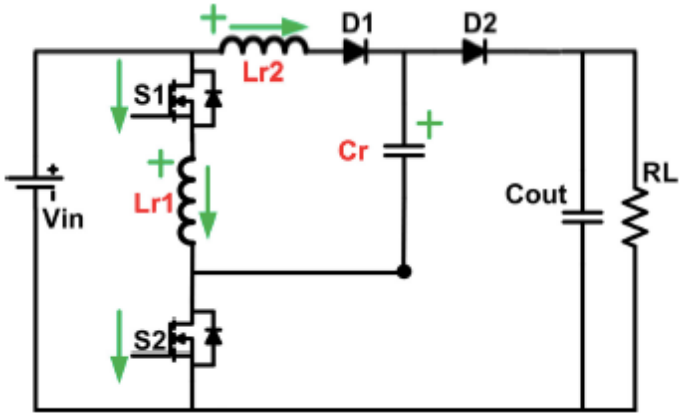


Fig. 1.15: Dual resonant switched-capacitor step-up converter topology. Figure from [23].

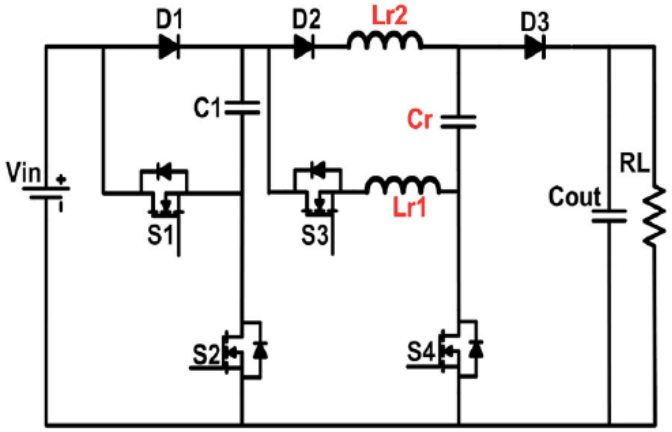


Fig. 1.16: Extension of the converter in Fig. 1.15 to 3X gain. Figure from [23].

In addition to a limited range of voltage gain and difficulty in extension, these two DRSCCs suffer from large magnitude high frequency ringing in the two branches with resonant inductors. This is due to the parasitic capacitances of the semiconductors in series with these inductors, which at turn-off can cause large voltage spikes and potentially damage the switch or diode. Snubbers are difficult to apply to these circuits, once again because the branches in question are so embedded in the resonant SC cell. The authors in [23] partially addressed this issue by adding a blocking diode in series with S2 in Fig. 1.15, which blocks the parasitic resonance from continuing. However, this does nothing to address the parasitic ringing of D1, and also adds conduction loss.

All of these issues were resolved in two papers by Wenhao Xie et al in [24] and [25]. The core observation that Xie et al made was that the resonant inductor locations in Figs. 1.14 and 1.15 were not unique. The inductors could be moved to the legs of the other two semiconductors without altering the operation of the converter; the only difference is that the off-time of a different switch is fixed. The resulting converters are shown in Fig. 1.17. With the inductors moved to these locations, the parasitic capacitances can more easily be clamped by connecting them to the input or output voltage via clamping diodes and capacitors. The converters in Fig 1.17 with regenerative snubbers applied are shown in Fig. 1.18. A comparison of the voltage waveforms of diode and switch with parasitic ringing is shown in Fig. 1.19. In Fig. 1.19a, when no snubber or blocking diode is present, the voltage across both the switch and diode reaches very large resonant peaks. In Fig. 1.19b, a blocking diode is in series with the switch, which successfully eliminates the large spike on the switch, but does not improve the diode waveform. Finally, Fig. 1.19c shows the switch and diode voltage with the regenerative snubber of Fig. 1.18b applied. Both the switch and diode experience no large voltage spikes or ringing.

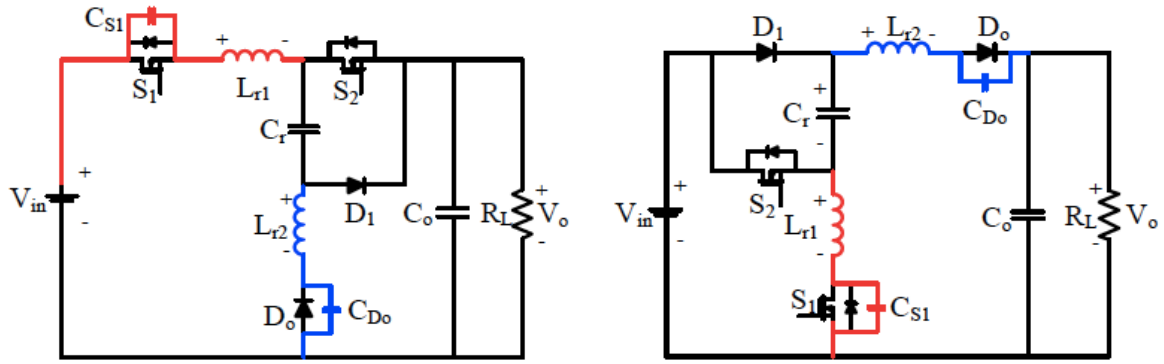


Fig. 1.17: Alternate versions of the DRSCCs in Figs. (a) 1.14 and (b) 1.15, with the branches that experience parasitic ringing highlighted. Figure from [24].

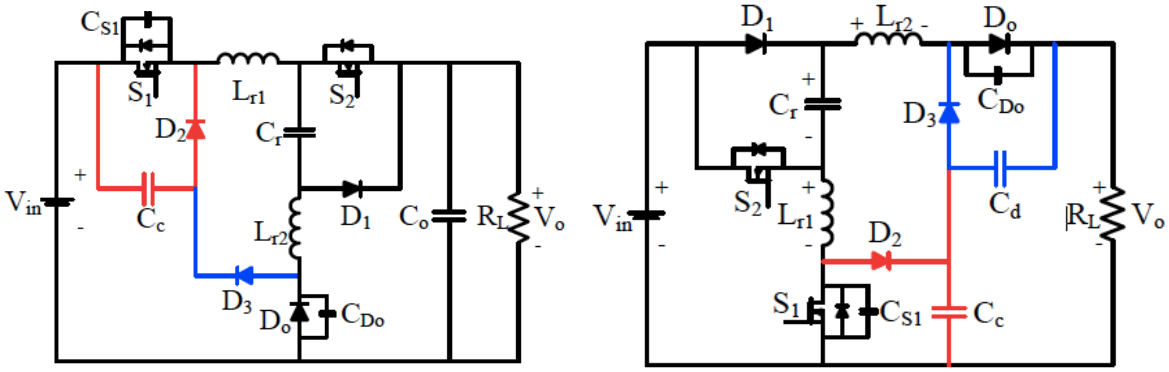


Fig. 1.18: Circuits in Fig. 1.17 with regenerative snubbers applied. Figure from [24].

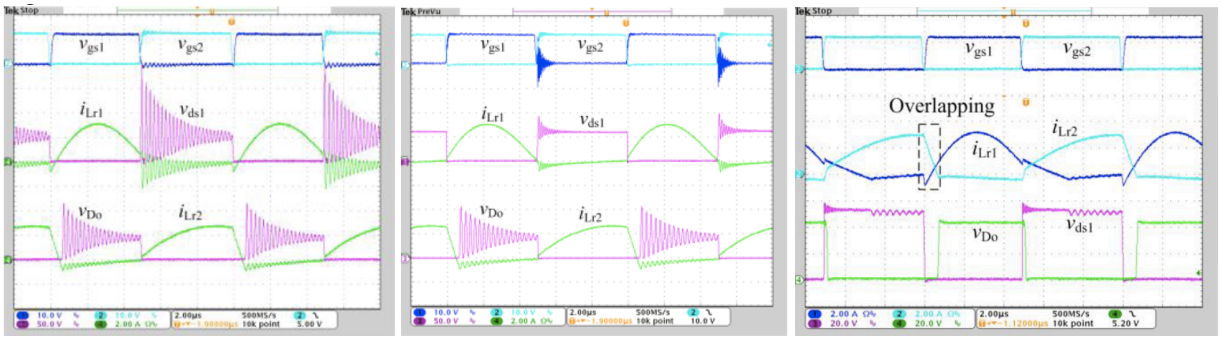
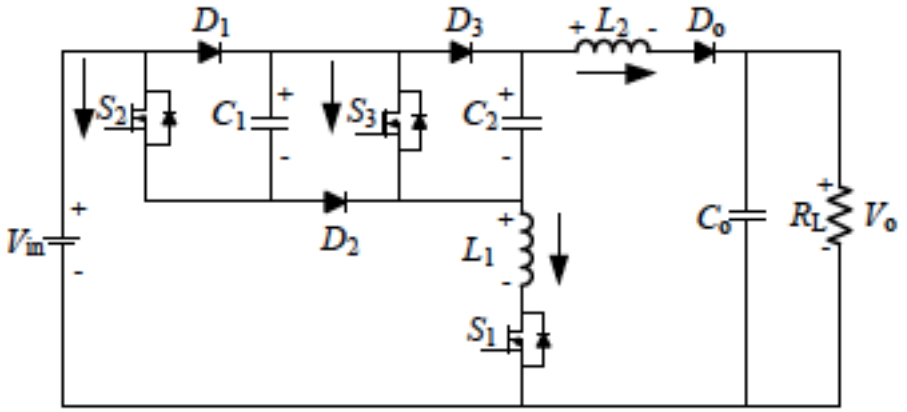
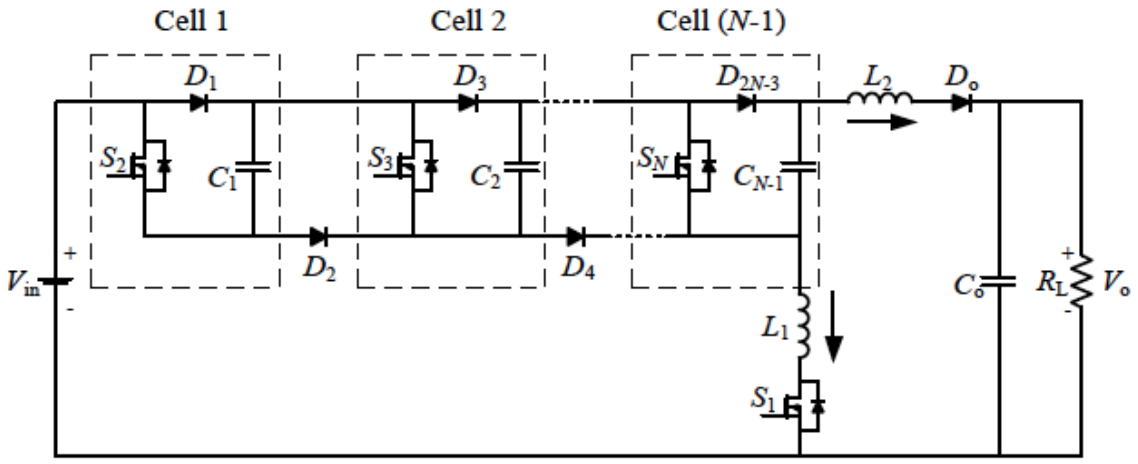


Fig. 1.19: Switch and diode voltage waveforms for the alternate DRSCC step-up of Fig. 1.17b with (a) no snubber of blocking diode, (b) blocking diode in series with S1, and (c) regenerative snubber of Fig. 1.18b applied. Figure from [24].

In addition to making it easier to eliminate parasitic ringing, the converter in Fig. 1.17b can easily be extended to larger step-up gains while maintaining resonant charging and discharging of all capacitors. The result of the 3X and *n*X extensions are shown in Fig. 1.20. During the charging of the capacitors, all of the capacitors appear in parallel and charge resonantly through L_1. During discharge, the capacitors appear in series and discharge resonantly through L_2. This discharge can be cut short, and a negative DC voltage will appear across L_2, allowing the current to ramp down and the energy to be recovered.



(a)



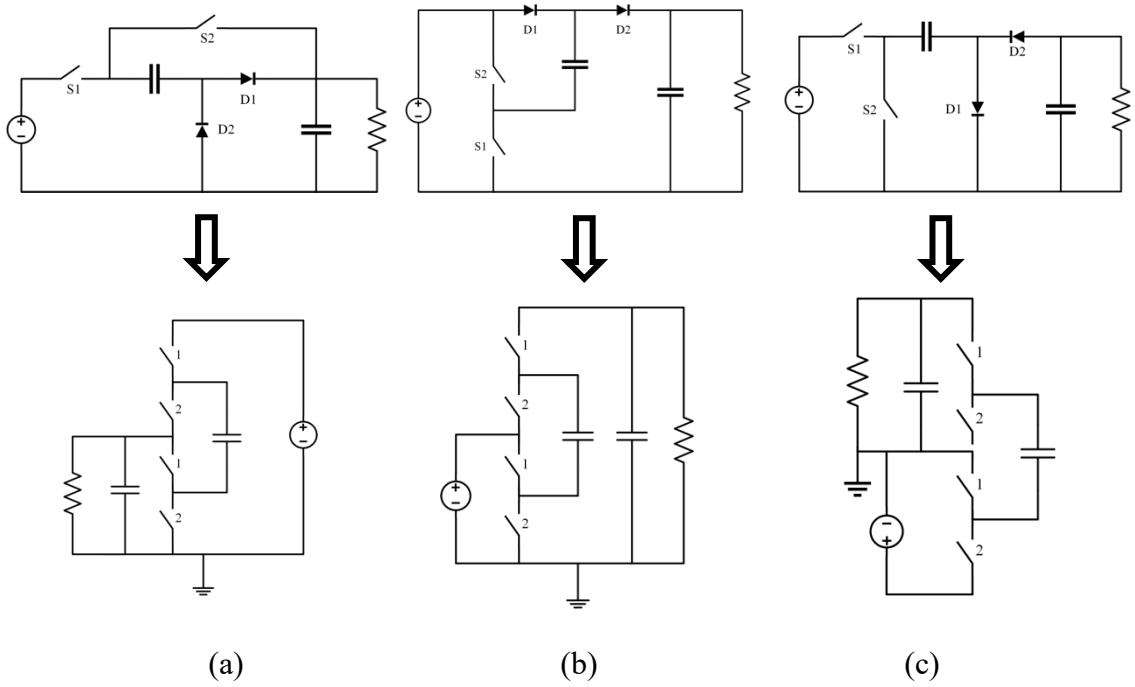
(b)

Fig. 1.20: Extension of the converter in Fig. 1.17b to (a) 3X and (b) *n*X. Figure from [25].

CHAPTER 2: Dual Resonant Switched-Capacitor Polarity Inverter

Development

The development of the dual resonant switched-capacitor polarity inverter, the subject of this thesis, began by an observation that the three basic SC converters of Fig. 1.2 could be viewed as a ladder converter with a single rung. If the semiconductors are replaced with ideal switches, these converters are then identical, the only difference being where the input, output, and common ground nodes are placed. This is illustrated in Fig. 2.1. With these three SC converters viewed in this way, it then becomes evident that the two original DRSCCs from Figs. 1.14 and 1.15 can be created by inserting an inductor in series with the innermost switches of the ladders in Fig. 2.1a and Fig. 2.1b, respectively. This re-drawing of these converters is shown in Fig. 2.2.



(a) (b) (c)

Fig. 2.1: The three basic SC converters of Fig. 1.2 drawn as a single rung ladder with ideal switches: (a) 1/2X step-down, (b) 2X step-up, and (c) polarity inverter.

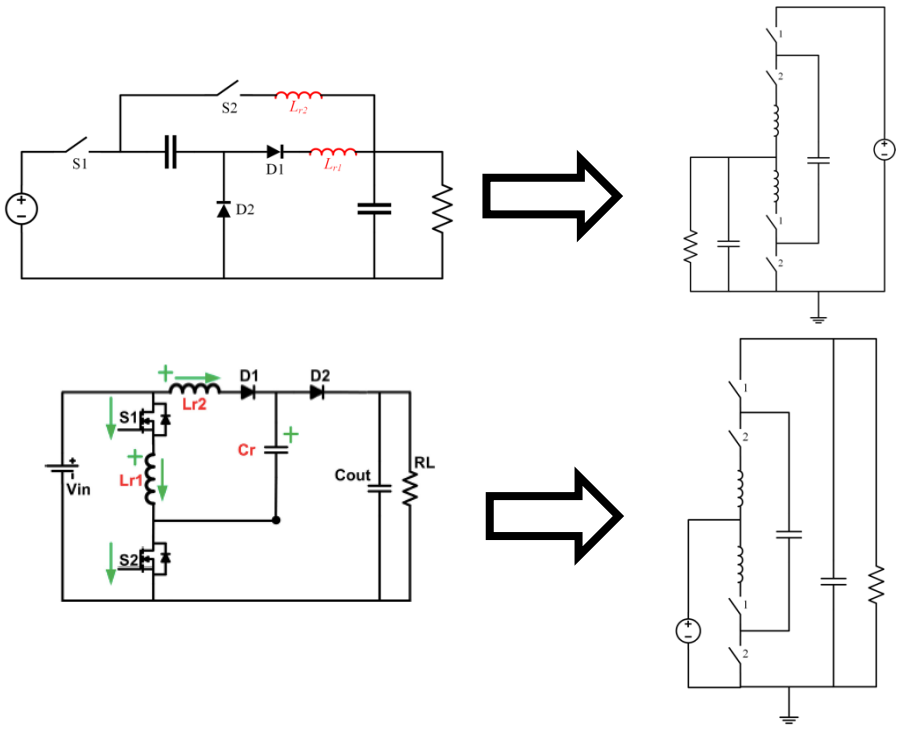


Fig. 2.2: Original DRSCCs from Figs. 1.14 and 1.15 re-drawn as single rung ladder converters, illustrating their equivalence.

Fig. 2.2 naturally leads to the question of what happens when one inserts a resonant inductor in series with innermost switches of Fig 2.1c. The result is in fact the dual resonant switched-capacitor polarity inverter, depicted in Fig. 2.3. As mentioned in Chapter 1, the gain of DRSCCs is limited by the maximum gain of the underlying SCC topology. For example, the DRSCC step-down converter can only regulate the conversion ratio from 0 to ½. Because the SC polarity inverter has unity gain, the resulting dual resonant converter can regulate the voltage gain over the entire range from 0 to –1. The observation in Fig. 2.2 also shows that the two alternate DRSCCs in Fig. 1.17 are equivalent to each other, and are created by moving the inductors in Fig. 2.2 to the outermost switches instead of the innermost. The dual resonant switched-capacitor polarity inverter thus also has an alternate form, a fact that will be discussed further in Chapter 4.

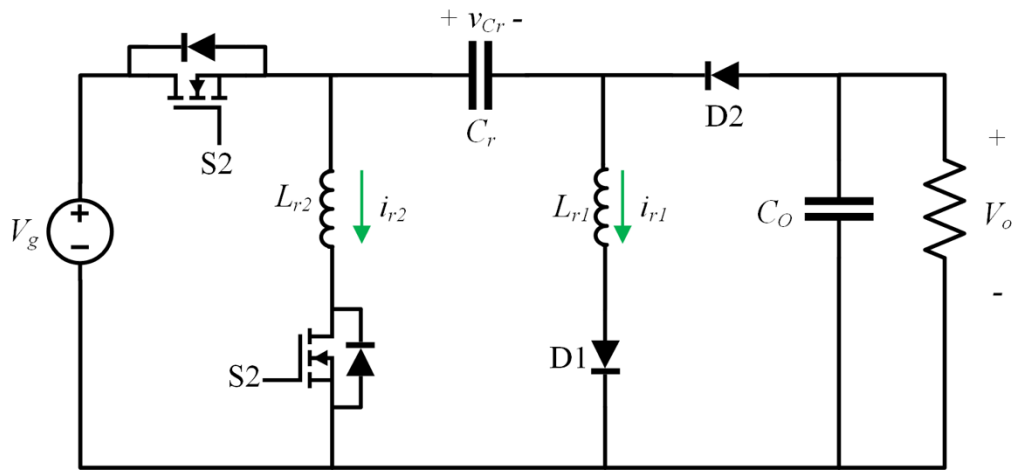


Fig. 2.3: The dual resonant switched-capacitor polarity inverter.

The operating principle of this converter is similar to other DRSCCs. When S1 is on, C_r is charged by the resonant current in L_{r1}. S1 can then be turned off before sinusoidal current reaches zero, and C_r begins discharging to the load through L_{r2}. The remaining energy in L_{r1} is recovered as the output voltage appears across L_{r1} when D2 turns on. This DC voltage is negative, thus causing the current in L_{r1} to linearly ramp down to zero. A detailed analysis and derivation of the dual resonant switched-capacitor polarity inverter voltage gain will be presented in the following section.

Detailed Analysis

The dual resonant switched-capacitor has four modes of operation that it may enter depending on the switching frequency and load. All four modes will be analyzed, although only modes 1 and 2 are desirable for practical use. Design guidelines will be presented in the next section on how to avoid the undesirable modes 3 and 4. There are several assumptions that will be used throughout this analysis for simplicity without loss of generality. First, the output capacitor C_O is assumed to be large enough that the output voltage V_O is approximately constant. Second, all components are assumed to be ideal, i.e. all diodes have a forward voltage drop of zero, the switches have zero on-resistance, and the ESRs of capacitors and inductors are neglected. Third, the converter is assumed to be in steady state. Finally, dead time between switching phases has been neglected. The two active switches are operated out of phase with each other, and the off-time of S1 is fixed such that i_{r2} is always a half sinusoid.

Mode 1 – Controlled Mode

The typical operating waveforms of the switch gate voltages, capacitor voltage, inductor currents, and diode currents in mode 1 are shown in Fig. 2.4. The different topological states are shown in Fig. 2.5.

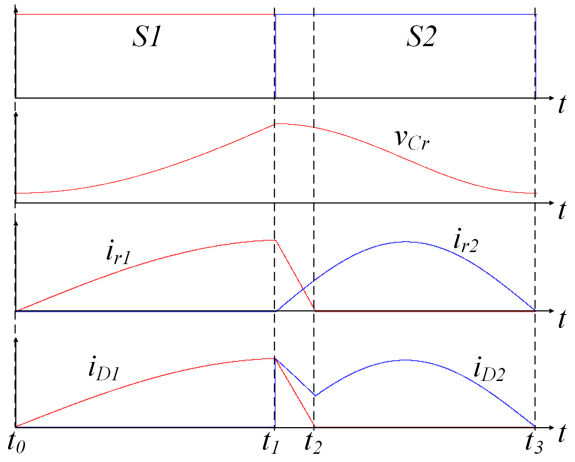


Fig. 2.4: Typical operating waveforms in mode 1.

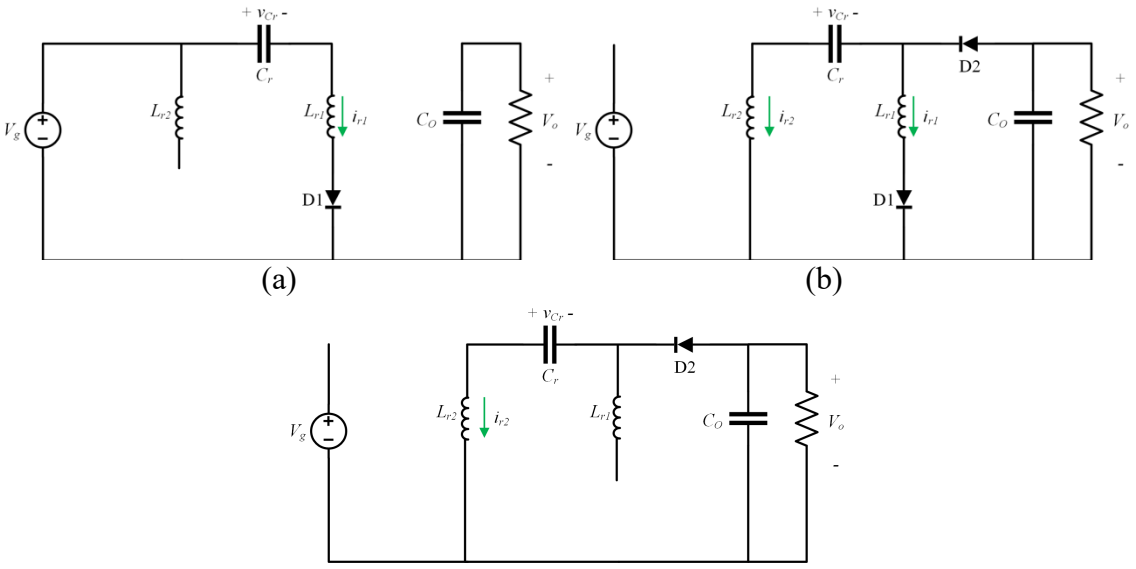


Fig. 2.5: Topological states of the DRSC step-down polarity inverter in mode 1 for (a) t_0 to t_1, (b) t_1 to t_2, and (c) t_2 to t_3.

[$t_0 - t_1$]: S1 turns on at t_0. D1 begins conducting and C_r is charged with the resonant current in the first resonant path. D1 and S1 both have ZCS turn-on. The KVL and KCL equations for the circuit in Fig. 2.5a are

$$V_g - v_{Cr}(t) = L_{r1}\frac{di_{r1}(t)}{dt} \tag{1}$$

$$i_{r1}(t) = C_r\frac{dv_{Cr}(t)}{dt}. \tag{2}$$

From Fig. 2.4, the boundary conditions for this state are

$$i_{r1}(t_0) = 0 \tag{3}$$

$$v_{Cr}(t_0) = V_{Crmin}, \tag{4}$$

where V_{Crmin} is the minimum voltage on capacitor C_r. Equations (1) and (2) can be solved for i_{r1} and v_{Cr} using the boundary conditions in (3) and (4), and using

$$\omega_{r1} = 2\pi f_{r1} = \frac{1}{\sqrt{L_{r1}C_r}} \tag{5}$$

$$R_{N1} = \sqrt{\frac{L_{r1}}{C_r}}, \tag{6}$$

the solutions can be expressed as

$$i_{r1}(t) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\left(\omega_{r1}(t - t_0)\right) \tag{7}$$

$$v_{Cr}(t) = V_g - \left(V_g - V_{Crmin}\right) \cos\left(\omega_{r1}(t - t_0)\right). \tag{8}$$

[$t_1 - t_2$]: S1 turns off at t_1 and S2 turns on with ZCS. The current i_{r1} is nonzero at t_1, as discussed previously, so it begins to conduct through D2. The capacitor C_r begins to be discharged by the resonant current i_{r2} in the second resonant path (also through D2) to the load. The DC output voltage is now imposed on L_{r1}, causing the current to linearly decrease, as the energy in L_{r1} is delivered to the load. The KVL and KCL equations of Fig. 2.5b are

$$V_O + v_{Cr}(t) = L_{r2} \frac{di_{r2}(t)}{dt} \tag{9}$$

$$V_O = L_{r2} \frac{di_{r1}(t)}{dt} \tag{10}$$

$$-i_{r2}(t) = C_r \frac{dv_{Cr}(t)}{dt}. \tag{11}$$

As previously mentioned, the off-time is fixed at half the second resonant period. The normalized switching frequency F_S is defined based on this period. The ratio between the two resonant frequencies k is also defined below

$$F_S = \frac{f_S}{2f_{r2}} = \frac{\pi}{T_S \omega_{r2}} \tag{12}$$

$$k = \frac{f_{r2}}{f_{r1}} = \sqrt{\frac{L_{r1}}{L_{r2}}} \tag{13}$$

From Fig. 2.4, (7), (12), and (13), the boundary conditions at t_1 can be found to be

$$i_{r1}(t_1) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\left(\frac{\pi}{k}\left(\frac{1}{F_s} - 1\right)\right) \tag{14}$$

$$i_{r2}(t_1) = 0 \tag{15}$$

$$v_{Cr}(t_1) = V_{Crmax}, \tag{16}$$

where V_{Crmax} is the maximum voltage on C_r. Based on (9) – (11) and (14) – (16), as well as

$$\omega_{r2} = 2\pi f_{r2} = \frac{1}{\sqrt{L_{r2}C_r}} \tag{17}$$

$$R_{N2} = \sqrt{\frac{L_{r2}}{C_r}}, \tag{18}$$

the solutions for i_{r1}, i_{r2}, and v_{Cr} can be obtained:

$$i_{r1}(t) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\left(\frac{\pi}{k}\left(\frac{1}{F_s} - 1\right)\right) + \frac{V_O}{L_{r1}}(t - t_1) \tag{19}$$

$$i_{r2}(t) = \frac{V_O + V_{Crmax}}{R_{N2}} \sin\big(\omega_{r2}(t - t_1)\big) \tag{20}$$

$$v_{Cr}(t) = -V_O + (V_O + V_{Crmax}) \cos\big(\omega_{r2}(t - t_1)\big). \tag{21}$$

$[t_2 - t_3]$: At t_2, i_{r1} reaches zero, and D1 turns off with ZCS. C_r continues to be discharged by the resonant current through L_{r2}. The solutions for i_{r2} and v_{Cr} are the same as in $[t_1 - t_2]$ as D1 turning off does not interrupt the resonance between C_r and L_{r2}. At t_3, S2 and D2 turn off with ZCS and the cycle repeats.

The charge delivered to C_r in $[t_0 - t_1]$ is

$$q_{ch} = C_r(V_{Crmax} - V_{Crmin}) = \int_{t_0}^{t_1} i_{r1}(t)dt. \tag{22}$$

From (22) and (7), the following expression can be obtained

$$\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) = \frac{V_{Crmax} - V_g}{V_{Crmin} - V_g} = \frac{M_{Crmax} - 1}{M_{Crmin} - 1}, \tag{23}$$

where M_{Crmax} and M_{Crmin} are V_{Crmax} and V_{Crmin} normalized to V_g.

Similarly, the charge removed from C_r during its discharge in $[t_1 - t_3]$ is

$$q_{dis} = C_r(V_{Crmax} - V_{Crmin}) = \int_{t_1}^{t_3} i_{r2}(t)dt. \tag{24}$$

From (24) and (20), and using the fact that the off-time of S1 is fixed at one half of the resonant period of the second resonant network, or equivalently

$$t_3 - t_1 = \frac{\pi}{\omega_{r2}} \tag{25}$$

the following is obtained

$$V_O = -\frac{1}{2}(V_{Crmin} + V_{Crmax}), \tag{26}$$

or in words, from steady state charge balance of C_r it can be shown that the output voltage is equal to the average voltage on the resonant capacitor. In terms of the conversion ratio, M, (26) can be rewritten as

$$M = -\frac{1}{2}(M_{Crmin} + M_{Crmax}). \tag{27}$$

To solve for M_{Crmin} and M_{Crmax} (and thus for M), it is useful to examine the output current of the converter I_O:

$$I_O = -\frac{1}{T_S}\left[\int_{t_0}^{t_3} i_{Cout}(t) + \int_{t_1}^{t_2} i_{r1}(t)dt - \int_{t_1}^{t_3} i_{Cr}(t)dt\right]. \tag{28}$$

The first term of (28) is equal to zero due to the charge balance of the output capacitor C_O. The third term in (28) is the charge removed from C_r, which from the charge balance of C_r must be equal to q_{ch} from (22). Therefore, the output current is equal to the negative of the average current through the inductor L_{r1}:

$$I_0 = -\frac{1}{T_S}\int_{t_0}^{t_3} i_{r1}(t)dt. \tag{29}$$

Using (19), (23), and (29), the following expression can be obtained

$$M = -\frac{2}{\pi}\frac{k}{Q}F_S\left[\frac{M_{Crmax} - M_{Crmin}}{M_{Crmax} + M_{Crmin}}\right], \tag{30}$$

where Q is defined as the quality factor of the first resonant path

$$Q = \frac{R_{N1}}{R}. \tag{31}$$

Solving the resulting systems of equations (23), (27), and (30) for M_{Crmax} and M_{Crmin}, we obtain

$$M_{Crmax} =$$

$$\frac{\left(\frac{1}{\pi Q}k F_S - \frac{1}{2}\right)\cos\left(\frac{2\pi}{k}\left(\frac{1}{F_S}-1\right)\right) - \frac{2}{\pi Q}k F_S \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right) + \frac{1}{\pi Q}k F_S + \frac{1}{2} + 2\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\sqrt{\frac{1}{\pi Q}k F_S\left(\frac{1}{2\pi Q}k F_S - 1\right) - 2\left(\frac{1}{\pi Q}k F_S\right)^2 \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right) + \frac{1}{\pi Q}k F_S\left(\frac{3}{2\pi Q}k F_S + 1\right)}}{\frac{1}{2}\cos\left(\frac{2\pi}{k}\left(\frac{1}{F_S}-1\right)\right) + 2\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right) + \frac{3}{2}} \quad (32)$$

$$M_{Crmin} = \frac{\left(M_{Crmax} + \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)-1\right)}{\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}, \quad (33)$$

from which M can be calculated from (27). The full expression for M is not written out due to its complexity. Voltage gain curves are more instructive, and will be examined in a later section.

Mode 2 – Uncontrolled Mode

If the switching frequency is low enough that both the charging and discharging currents are half-sinusoids, the converter enters the uncontrolled mode 2. The typical operating waveforms of the switch gate voltages, capacitor voltage, inductor currents, and diode currents in mode 2 are shown in Fig. 2.6. The different topological states are shown in Fig. 2.7.

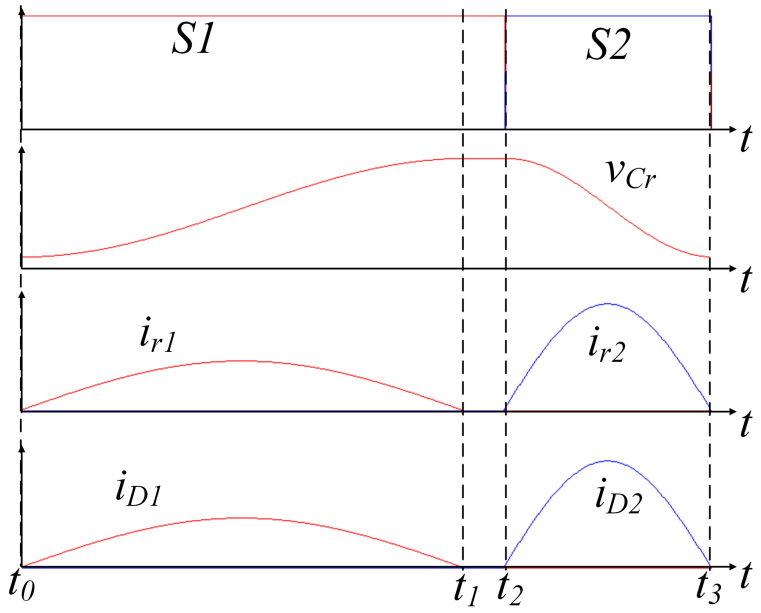


Fig. 2.6: Typical operating waveforms in mode 2.

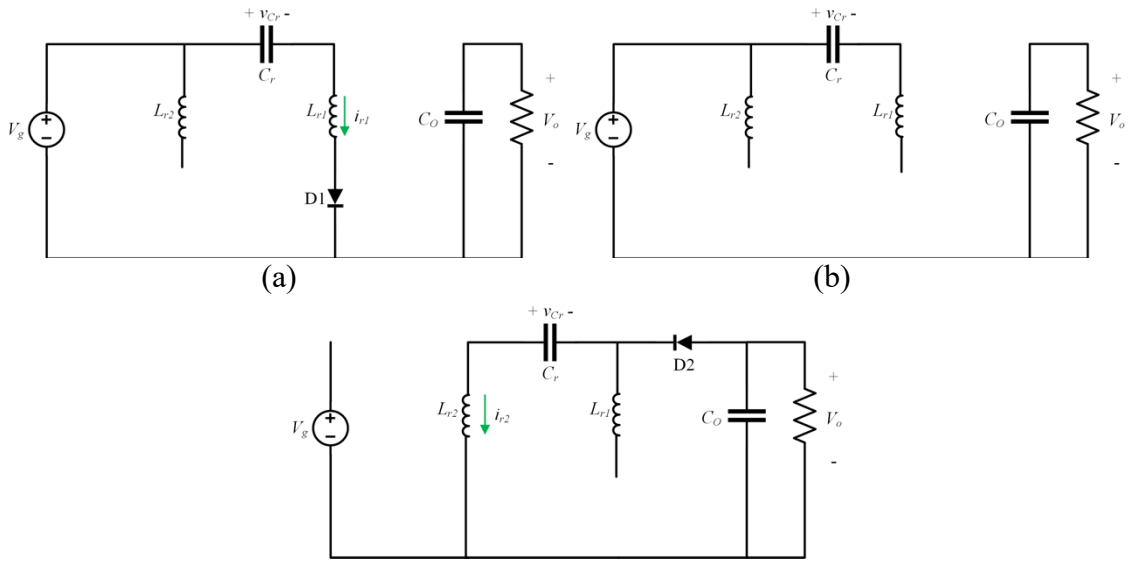


Fig. 2.7: Topological states of the DRSC step-down polarity inverter in mode 2 for (a) t_0 to t_1, (b) t_1 to t_2, and (c) t_2 to t_3.

The analysis of mode 2 is very similar to that of mode 1, except that now the time duration $[t_0 - t_1]$ is equal to half the resonant period of the first resonant path:

$$t_1 - t_0 = \frac{\pi}{\omega_{r1}} \tag{34}$$

The resulting time domain expressions for i_{r1} and i_{r2} during the states in which they are nonzero are the same as (19) and (20). Charge balance of C_r can be applied in mode 2 as well, but due to (34) the equation for q_{ch} from (22) simplifies to

$$q_{ch} = C_r(V_{Crmax} - V_{Crmin}) = 2C_r\big(V_g - V_{Crmin}\big), \tag{35}$$

from which the following can be obtained

$$V_g = \frac{1}{2}(V_{Crmax} + V_{Crmin}) \tag{36}$$

Since the discharge is unchanged from mode 1, (26) still holds in mode 2, thus the gain M can be found to be

$$M = -1 \tag{37}$$

To solve for M_{Crmax} and M_{Crmin}, once again analyzing the output current is useful. In mode 2, since the current in L_{r1} drops to zero before D2 turns on, the expression for the average output current reduces to

$$I_O = -\frac{1}{T_S}\left[\int_{t_0}^{t_3} i_{Cout}(t)dt - \int_{t_1}^{t_3} i_{Cr}(t)\,dt\right]. \tag{38}$$

Once again, the first term reduces to zero by the charge balance of C_O. The second term is equal to the charge removed from C_r during its discharge, which by charge balance is equal to the right-hand side of (35). Thus, the following expression can be derived

$$-\frac{2}{T_S}\left(C_r\left(V_g - V_{Crmin}\right)\right) = I_O = \frac{V_O}{R} \tag{39}$$

Using (12), (13), (31), (37), and (39), the following solution for M_{Crmin} in mode 2 can be found:

$$M_{Crmin} = 1 - \frac{\pi}{2}\frac{Q}{k}\frac{1}{F_S}. \tag{40}$$

From (36) and (40), M_{Crmax} can be found to be

$$M_{Crmax} = 1 + \frac{\pi}{2}\frac{Q}{k}\frac{1}{F_S}. \tag{41}$$

Thus, in mode 2, the converter behaves similarly to an indirect RSCC like those in Fig. 1.8, with a fixed voltage gain and ZCS turn-on and turn-off of all semiconductors.

Mode 3 – Heavy Load

Since the average current in L_{r1} is equal in magnitude to the load current, with heavy loads the average current of L_{r1} may be large enough that L_{r1} must store energy throughout the switching cycle. Thus, mode 3 is defined by the mode in which L_{r1} has a nonzero DC bias. The typical operating waveforms of the switch gate voltages, capacitor voltage, inductor currents, and diode currents in mode 3 are shown in Fig. 2.8. The different topological states are shown in Fig. 2.9.

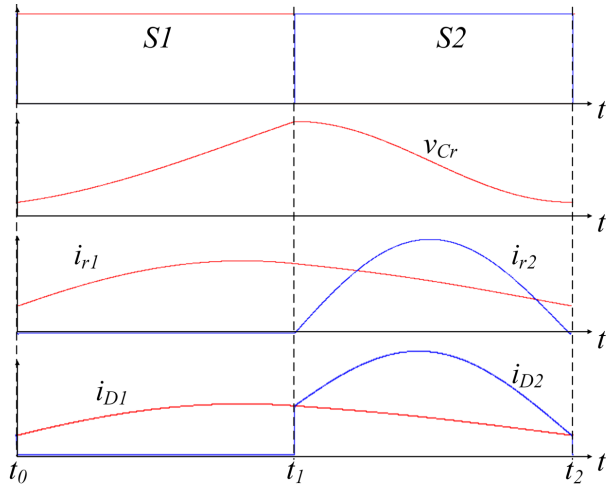


Fig. 2.8: Typical operating waveforms in mode 3.

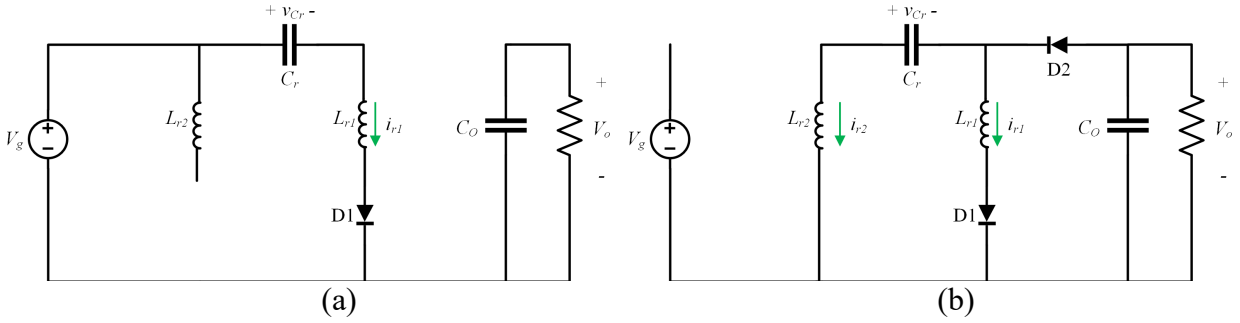


Fig. 2.9: Topologitcal states of the DRSC step-down polarity inverter in mode 3 for (a) t_0 to t_1 and (b) t_1 to t_2.

$[t_0 - t_1]$: This state is the same as in modes 1 and 2, except that the current in L_{r1} does not start at zero. Instead, it has a nonzero minimum I_{r1min}. The KVL and KCL equations are the same as (1) and (2). However, the boundary conditions become

$$i_{r1}(t_0) = I_{r1min} \tag{42}$$

$$v_{Cr}(t_0) = V_{Crmin}. \tag{43}$$

These different boundary conditions result in the following solutions from (1), (2), (42), and (43)

$$i_{r1}(t) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\big(\omega_{r1}(t - t_0)\big) + I_{r1min} \cos\big(\omega_{r1}(t - t_0)\big) \tag{44}$$

$$v_{Cr}(t) = V_g - \big(V_g - V_{Crmin}\big) \cos\big(\omega_{r1}(t - t_0)\big) + I_{r1min} R_{N1} \sin\big(\omega_{r1}(t - t_0)\big). \tag{45}$$

[$t_1 - t_2$]: This state is the same as in mode 1, except the current in L_{r1} does not drop to zero. The KVL and KCL equations are the same as in (9) – (11), but the boundary conditions are now

$$i_{r1}(t_1) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) + I_{r1min} \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) \tag{46}$$

$$i_{r2}(t_1) = 0 \tag{47}$$

$$v_{Cr}(t) = V_{Crmax}. \tag{48}$$

The solutions to (9) – (11) and (46) – (48) are

$$i_{r1}(t) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) + I_{r1min} \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) + \frac{V_O}{L_{r1}}(t - t_1) \tag{49}$$

$$i_{r2}(t) = \frac{V_O + V_{Crmax}}{R_{N2}} \sin\big(\omega_{r2}(t - t_1)\big) \tag{50}$$

$$v_{Cr}(t) = -V_O + (V_O + V_{Crmax}) \cos\big(\omega_{r2}(t - t_1)\big). \tag{51}$$

There is now one more variable to solve for, the minimum inductor current of L_{r1}, which can be normalized to V_g as an admittance

$$Y_{r1min} = \frac{I_{r1min}}{V_g}. \tag{52}$$

Because of the fixed off-time, (27) holds in mode 3 as well. Solving for the charge delivered to C_r in [$t_0 - t_1$] using an equation just like (22), the following expression can be obtained after some simplification

$$-M_{Crmin} \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) + M_{Crmax} - Y_{r1min} R_{N1} \sin\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right) = 1 - \cos\left(\frac{\pi}{k}\left(\frac{1}{F_S} - 1\right)\right). \tag{53}$$

As in modes 1 and 2, the average current of L_{r1} is equal in magnitude to the output current, so an expression similar to (29) can be obtained

$$I_O = -\frac{1}{T_S}\int_{t_0}^{t_2} i_{r1}(t)dt \tag{54}$$

From (44), (49), and (54), and substituting $I_O = \frac{V_O}{R}$, the following expression is obtained

$$M - M_{Crmin}\left(\frac{k}{\pi Q}F_S + \frac{1}{2Q}F_S \sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right) + M_{Crmax}\frac{k}{\pi Q}F_S + Y_{r1min}R_{N1}\left(\frac{1}{2}F_S\frac{R_{N1}}{Q}\left(1+\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right)\right) = -\frac{1}{2Q}F_S \sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right). \quad (55)$$

In steady state, both inductors must be volt-second balanced each cycle. The voltage on L_{r1} during $[t_0 - t_1]$ is

$$v_{Lr1}(t) = V_g - v_{Cr}(t), \quad (56)$$

and during $[t_1 - t_2]$ is

$$v_{Lr1}(t) = V_O \quad (57)$$

From the volt-second balance of L_{r1}, we can write the following from (56) and (57)

$$\int_{t_0}^{t_2} v_{Lr1}(t)dt = \int_{t_0}^{t_1}\left(V_g - v_{Cr}(t)\right)dt + \int_{t_1}^{t_2} V_O dt = 0. \quad (58)$$

Solving (58) by substituting (45) for v_{Cr}, the following is obtained

$$\frac{\pi}{k}M - M_{Crmin}\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right) - Y_{r1min}R_{N1}\left(1-\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right) = \sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right). \quad (59)$$

Solving the system of equations formed by (27), (53), (55), and (59), the following solutions for M, M_{Crmin}, M_{Crmax}, and Y_{r1min} can be found

$$M = \frac{-\left(\frac{2k}{\pi}\left(1-\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right)+\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right)}{\frac{4k^2+\pi^2}{2k\pi}+\left(\frac{\pi^2-4k^2}{2k\pi}\right)\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)+2\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)} \quad (60)$$

$$M_{Crmin} = \frac{\left(\frac{2kF_S-\pi Q}{\pi F_S}\right)\left(1-\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right)+\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}{\frac{4k^2+\pi^2}{2k\pi}+\left(\frac{\pi^2-4k^2}{2k\pi}\right)\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)+2\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)} \quad (61)$$

$$M_{Crmax} = \frac{\left(\frac{2kF_S+\pi Q}{\pi F_S}\right)\left(1-\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\right)+\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}{\frac{4k^2+\pi^2}{2k\pi}+\left(\frac{\pi^2-4k^2}{2k\pi}\right)\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)+2\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)} \quad (62)$$

$$Y_{r1min} = \frac{1}{R_{N1}}\frac{-1+\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)+\left(\frac{2kQ-\pi F_S}{2kF_S}\right)\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}{\frac{4k^2+\pi^2}{2k\pi}+\left(\frac{\pi^2-4k^2}{2k\pi}\right)\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)+2\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}. \quad (63)$$

Note that the conversion ratio M in mode 3 becomes independent of the load (i.e. there is now Q term in the expression). While this is an advantage, it is offset by the fact that the converter loses its natural ZCS, with the exception of S2 which retains ZCS turn-on and turn-off. In addition, under heavy load conditions the maximum voltage gain of the converter is limited, as will be shown below. Thus, mode 3 is generally undesirable and should be avoided. The boundary between modes 1 and 3 can be numerically calculated by solving for when $Y_{r1min} = 0$.

Mode 4 – Early Freewheeling

At low switching frequencies, S1 may be on long enough for the voltage on C_r to resonate to a value large enough to forward bias D2 before S1 turns off. If this happens, the converter enters mode 4. The typical operating waveforms of the switch gate voltages, capacitor voltage, inductor currents, and diode currents in mode 4 are shown in Fig. 2.10. The different topological states are shown in Fig. 2.11.

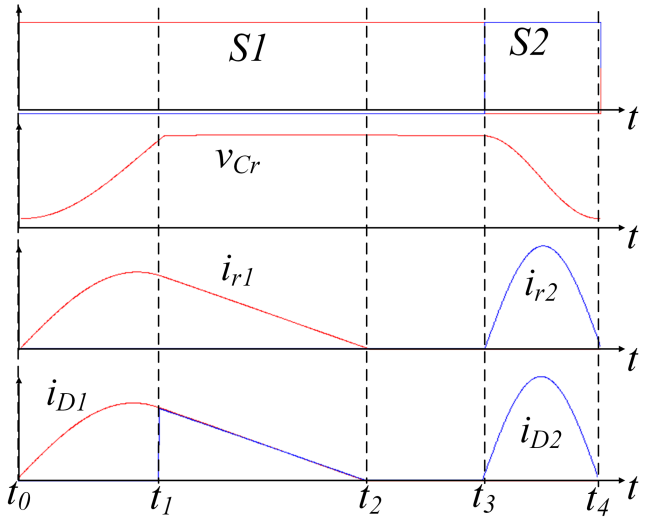


Fig. 2.10: Typical operating waveforms in mode 4.

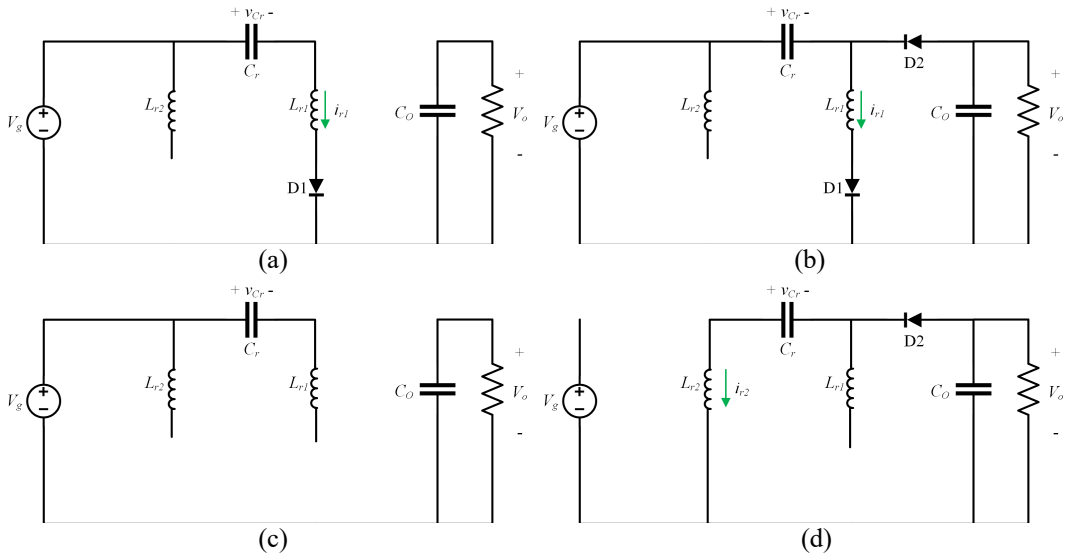


Fig. 2.11: Topological states of the DRSC step-down polarity inverter in mode 4 for (a) t_0 to t_1, (b) t_1 to t_2, (c) t_2 to t_3, and (d) t_3 to t_4.

Unlike in the modes previously analyzed, the charging of C_r is cut short by a diode turning on rather than an active switch. In other words, the time duration $[t_0 - t_1]$ is no longer a fixed length of time at a given switching frequency. Because of this, the analysis of mode 4 will be done slightly differently than the other three modes, instead employing conservation of energy to find the conversion ratio.

First, we notice that the KVL and KCL equations, as well as the boundary conditions, during the charging and discharging intervals of C_r (i.e. $[t_0 - t_1]$ and $[t_3 - t_4]$) are exactly the same as in mode 1. Thus, the solutions for i_{r1} and i_{r2} during these intervals are also the same as in mode 1. For convenience, these solutions are rewritten below

$$i_{r1}(t) = \frac{V_g - V_{Crmin}}{R_{N1}} \sin\big(\omega_{r1}(t - t_0)\big) \tag{64}$$

$$i_{r2}(t) = \frac{V_O + V_{Crmax}}{R_{N2}} \sin\big(\omega_{r2}(t - t_3)\big). \tag{65}$$

The reverse voltage across D2 during the charging interval $[t_0 - t_1]$ is

$$v_{D2} = V_g - v_{Cr}(t) - V_O. \tag{66}$$

Since mode 4 is defined by v_{Cr} becoming large enough that v_{D2} drops to zero during this charging phase, we can write from (66)

$$0 = V_g - V_{Crmax} - V_O, \tag{67}$$

or equivalently,

$$V_{Crmax} = V_g - V_O \tag{68}$$

In other words, the maximum voltage on C_r is constrained in mode 4 to $V_g - V_O$. To find V_{Crmin}, we can solve for the charge removed for C_r during its discharge phase [$t_3 - t_4$]

$$q_{dis} = C_r(V_{Crmax} - V_{Crmin}) = \int_{t_3}^{t_4} i_{r2}(t)dt. \tag{69}$$

Substituting (65) for i_{r2}, (68) for V_{Crmax}, and noting that since the off-time is fixed,

$$t_4 - t_3 = \frac{\pi}{\omega_{r2}}, \tag{70}$$

V_{Crmin} can be found from (69) to be

$$V_{Crmin} = -\left(V_g + V_O\right). \tag{71}$$

Energy is only drawn from the source during the charging of C_r in [$t_0 - t_1$]. Thus, the input energy can be written as

$$W_{IN} = V_g \int_{t_0}^{t_1} i_{r1}(t)dt = V_g C_r(V_{Crmax} - V_{Crmin}). \tag{72}$$

By substituting (68) for V_{Crmax} and (71) for V_{Crmin}, the following is obtained

$$W_{IN} = 2C_r V_g^2. \tag{73}$$

Assuming ideal components (as we are during this analysis) and 100% efficiency, input power and output power can be equated

$$W_{IN} f_s = 2C_r V_g^2 f_s = \frac{V_O^2}{R}, \tag{74}$$

from which the conversion ratio M can easily be solved

$$M = -\sqrt{2RC_r f_s} = -\sqrt{\frac{2}{\pi}\frac{k}{Q}F_S} \tag{75}$$

In mode 4, every semiconductor has ZCS turn-on and turn-off (as in mode 2), except for the hard turn-on of D2 at t_1. The magnitude of the voltage gain in modes 1 and mode 3 monotonically decreases as F_S increases, and it is fixed in mode 2. In mode 4, on the other hand, the magnitude of the voltage gain is monotonically increasing towards 1. In order to construct the complete voltage gain curve for all loads, which will illustrate the importance of this fact, some important boundary conditions must be discussed.

Boundary Conditions

Mode 1 and Mode 2 Boundary

The boundary frequency between mode 1 and mode 2 is defined to be the frequency at which the on-time of S1 is exactly equal to one of the first resonant period, or

$$\frac{1}{2f_{r1}} = \frac{1}{f_{SB}} - \frac{1}{2f_{r2}}, \tag{76}$$

where f_{SB} is the boundary frequency. Using (13), (76) can be rewritten as

$$\frac{k}{2f_{r2}} = \frac{1}{f_{SB}} - \frac{1}{2f_{r2}}. \tag{77}$$

Multiplying both sides of (77) by $2f_{r2}$ and using (12), one obtains

$$k = \frac{1}{F_{SB}} - 1, \tag{78}$$

where F_{SB} is the normalized boundary frequency. Solving (78) for F_{SB} results in

$$F_{SB} = \frac{1}{k+1}. \tag{79}$$

As (79) shows, this boundary is fixed with respect to load and solely dependent on the ratio between the two resonant frequencies. The inductor current waveforms just below, at, and just above the boundary are shown in Fig. 2.12.

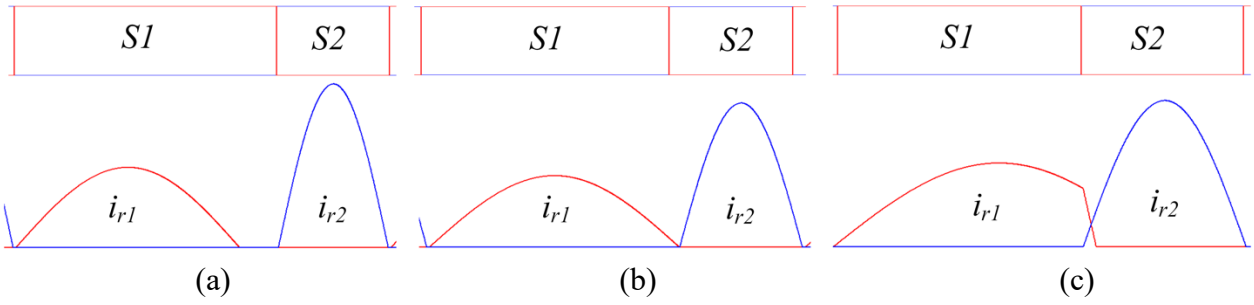


Fig. 2.12: Inductor current waveforms for frequencies (a) just below, (b) exactly at, and (c) just above the boundary frequency between mode 1 and mode 2.

Mode 2 and Mode 4 Boundary

Mode 4 occurs for nearly all loads at low frequencies, and as mentioned above, the magnitude of the voltage gain monotonically increases as the frequency increases. The converter enters mode 2 once the gain from (75) reaches –1. Defining this boundary frequency as F_{S24}, one obtains

$$-\sqrt{\frac{2}{\pi}\frac{k}{Q}F_{S24}} = -1, \tag{80}$$

which can easily be solved for F_{S24}, obtaining

$$F_{S24} = \frac{\pi}{2}\frac{Q}{k}. \tag{81}$$

Unlike F_{SB}, this boundary frequency is load dependent, and moves to higher frequencies as the load gets heavier. Physically, this is because with heavier loads, the resonant current charging C_r is larger, so less time is required for C_r resonate to a large enough voltage to forward bias D2.

Critical Load Q_{crit}

Since F_{S24} increases with frequency while F_{SB} is fixed, a natural question is what happens in the converter if F_{S24} moves to frequencies at or above F_{SB}. In fact, as the load gets heavy enough for this to occur, the converter no longer enters mode 2 from mode 4, but instead goes directly into mode 1. This has the effect of limiting the maximum magnitude of the voltage gain, as well as making the gain above F_{SB} no longer monotonic by introducing a knee into the curve. Both of these conditions are highly undesirable and should be avoided. Thus, the important boundary in this case is the heaviest load the converter can withstand before this phenomenon starts to occur, rather than the frequency at which the knee occurs, which is load dependent and has no simple analytical solution.

This critical load, with quality factor Q_{crit}, is defined as the load at which F_{S24} is equal to F_{SB}, or from (79) and (81)

$$\frac{\pi}{2}\frac{Q_{crit}}{k} = \frac{1}{k+1}, \tag{82}$$

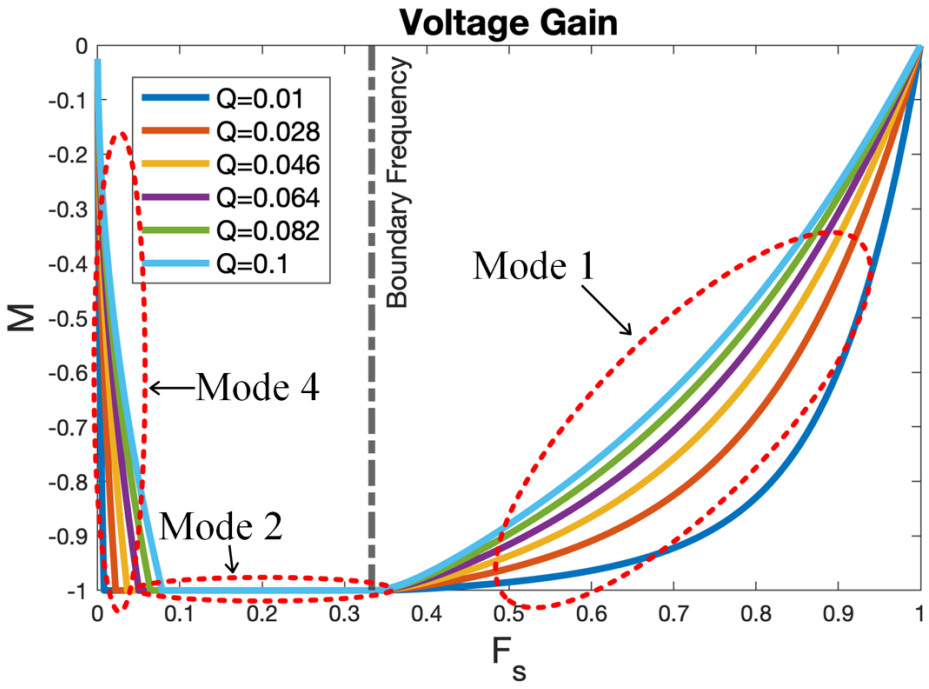
which can easily be solved for Q_{crit}

$$Q_{crit} = \frac{2}{\pi}\frac{k}{k+1}. \tag{83}$$

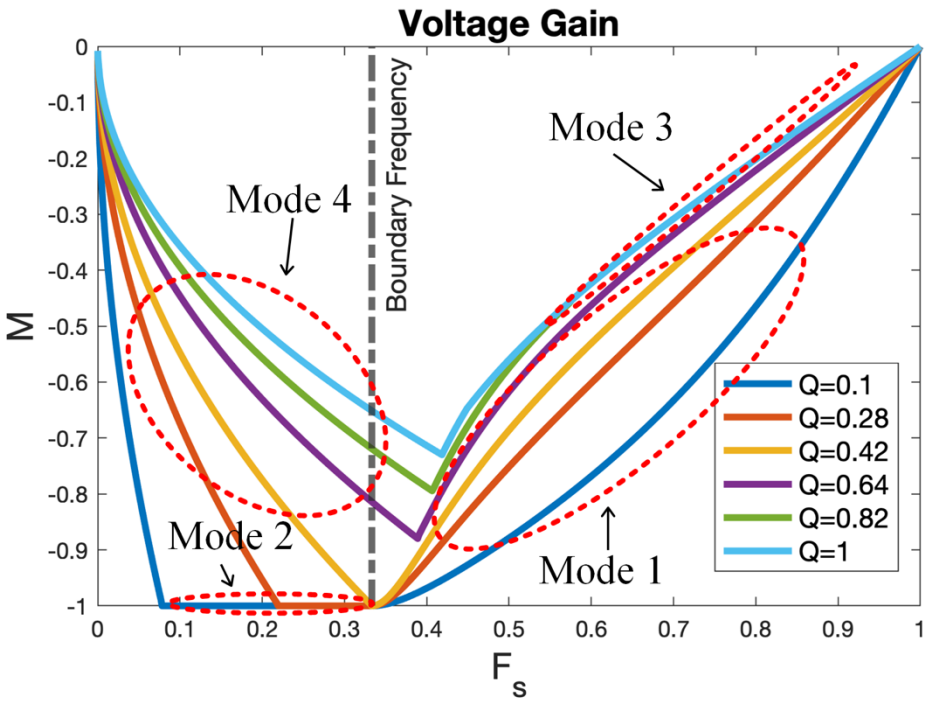
Using the definition of Q in (31), the critical load resistance R_{crit} can also be written

$$R_{crit} = \frac{\pi}{2}\frac{k+1}{k}R_{N1}. \tag{84}$$

For $Q > Q_{crit}$ (or $R < R_{crit}$), a knee begins to appear in the voltage gain curve as described above, limiting the maximum voltage gain and making the gain above F_{SB} no longer monotonic. The final voltage gain curves for two sets of loads are shown in Fig. 2.13 for k =2. The green and light blue curves in Fig. 2.13b show the load independent behavior of mode 3, as the two curves converge at higher frequencies. Q_{crit} is a very important design parameter, as it sets the heaviest load at which the converter can operate.



(a)



(b)

Fig. 2.13: Voltage gain for (a) loads well below Q_{crit} and (b) loads below and above Q_{crit}. In these curves, $k = 2$ and $Q_{crit} = \frac{4}{3\pi} \approx 0.424$.

Design Guidelines

In this section, guidelines on how to design a dual resonant switched-capacitor step-down polarity inverter from a specified input voltage, output voltage, and maximum output power will be presented. Before the details of these guidelines can be presented, the important design parameters of voltage and current stresses must be calculated. As part of the design process, we will ensure that $Q < Q_{crit}$ for all expected loads, such that the converter is always in mode 1 for $F_S > F_{SB}$.

Voltage Stress

The peak voltage stress of C_r was in fact already calculated in the Detailed Analysis section above as M_{Crmax}. M_{Crmax} is plotted in Fig. 2.14 for the same range of loads is in Fig. 2.13a. The absolute maximum occurs in mode 2, and is never more than $2V_g$. The maximum stress in mode 1 always occurs at F_{SB}, so it can be solved for by setting F_S in (41) with F_{SB} from (79)

$$M_{Crmax\_max1} = 1 + \frac{\pi}{2}\frac{k+1}{k}Q. \tag{85}$$

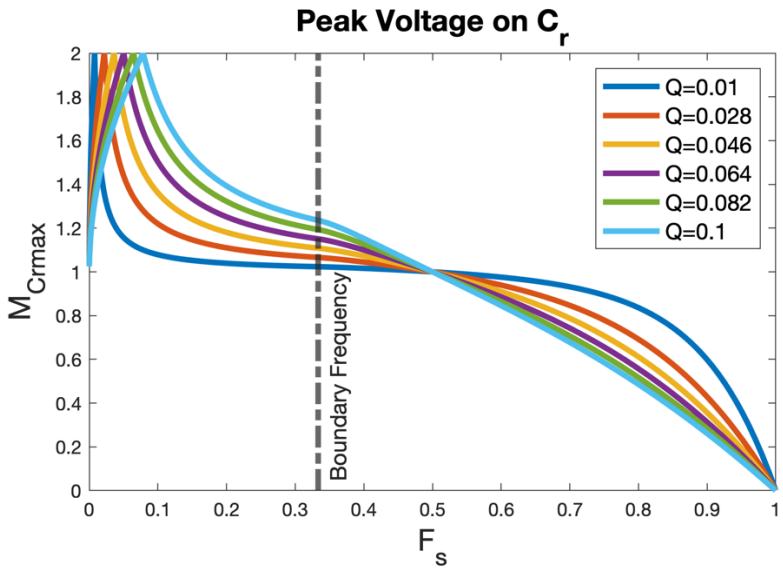


Fig. 2.14: Peak voltage stress on C_r normalized to V_g for several loads.

The voltage stress of the semiconductor components can be written in terms of M, M_{Crmax}, and M_{Crmin}. From Fig. 2.5a (or equivalently 2.7a, 2.9a, or 2.11a), when D2 is off its reverse voltage is

$$v_{D2}(t) = V_g - v_{Cr}(t) - V_O, \tag{86}$$

which is evidently at its maximum value at t_0 when $v_{Cr}(t) = V_{Crmin}$, so the maximum normalized voltage stress of D2 can be written from (86) as

$$M_{D2} = \frac{V_{D2}}{V_g} = 1 - M_{Crmin} - M. \tag{87}$$

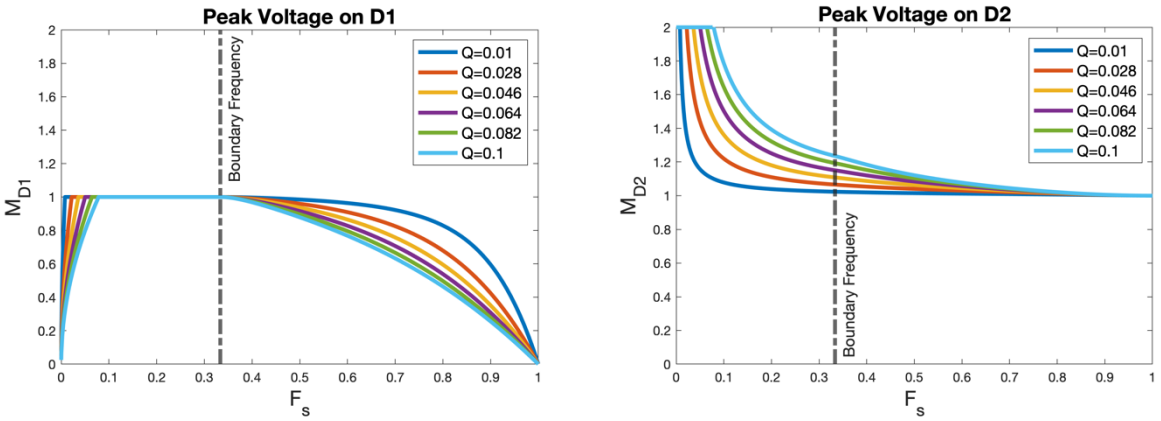
Similarly, from Fig. 2.5a, when D1 is off its reverse voltage is

$$v_{D1}(t) = -V_O, \tag{88}$$

or normalized to V_g,

$$M_{D1} = \frac{V_{D1}}{V_g} = -M. \tag{89}$$

The voltage stresses of D1 and D2 are plotted in Fig. 2.15. The absolute maximum voltage stress for D1 occurs in mode 2 and is V_g, while the max voltage stress of D2 occurs at the boundary between modes 2 and 4 and is $2V_g$.



(a) (b)

Fig. 2.15: Peak normalized voltage stress of (a) D1 and (b) D2.

As with the voltage stress of C_r, the maximum mode 1 voltage stress of both D1 and D2 occurs at F_{SB}. Substituting (37), (40), and (79) into (87), M_{D2} can be obtained below

$$M_{D2\_max1} = 1 + \frac{\pi}{2}\frac{k+1}{k}Q, \tag{90}$$

which is equivalent to the maximum mode 1 voltage stress of C_r in (85). For the maximum D1 voltage stress, since M is fixed at –1 at F_{SB},

$$M_{D1\_max1} = 1 \tag{91}$$

From Fig. 2.5b (or equivalently 2.5c, 2.7c, 2.9b, and 2.11d), the blocking voltage of S1 is

$$v_{S1}(t) = v_{Cr}(t) + V_O, \tag{92}$$

which, since V_O is a DC voltage, is at its maximum at t_1 in Fig. 2.4 when $v_{Cr}(t) = V_{Crmax}$. Thus, the maximum normalized voltage stress of S1 can be written from (92) as

$$M_{S1} = \frac{V_{S1}}{V_g} = M_{Crmax} + M \tag{93}$$

It is evident from Figs. 2.5, 2.7, 2.9, and 2.11 that when S2 is off its blocking voltage is equal to the input voltage V_g.

$$M_{S2} = \frac{V_{S2}}{V_g} = 1 \tag{94}$$

The voltage stress of S1 and S2 are plotted from (93) and (94) in Fig. 2.16. M_{S2} is just a constant value, but is plotted for completeness regardless.

As with the voltage stresses derived above, the maximum mode 1 value of M_{S1} occurs at F_{SB}, as can be seen from Fig. 2.16a. Substituting (37), (41), and (79) into (93), the maximum mode 1 voltage stress of S1 can be found

$$M_{S1\_max1} = \frac{\pi}{2}\frac{k+1}{k}Q. \tag{95}$$

Since M_{S2} is a constant, we can also write the trivial result for maximum mode 1 voltage stress

$$M_{S2\_max1} = 1 \tag{96}$$

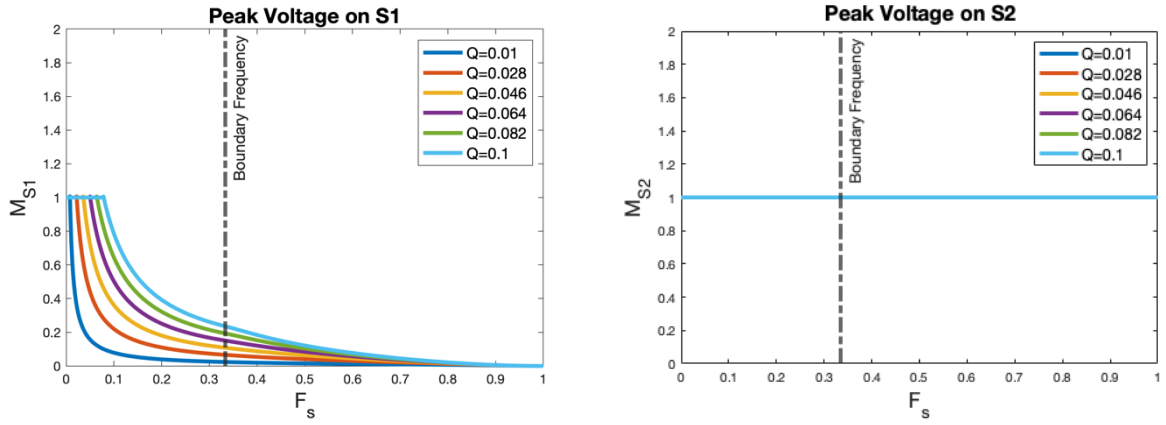


Fig. 2.16: Peak normalized voltage stress of (a) S1 and (b) S2.

The voltage stress equations in terms of M, M_{Crmax}, and M_{Cmin}, absolute maximum voltage stresses, and maximum mode 1 voltage stresses are summarized in Table 2.1 below. Ultimately it is the designer's choice whether to base their voltage stresses solely on the maximum mode 1 stress or to consider the absolute maximum, which for C_r, S1, and D2 occurs in mode 2. One advantage of using absolute maximum stresses is that they are not load or k dependent and can be calculated directly from the specified input voltage. For these reasons, the design guidelines presented in this section will use the last column of Table 2.1 for calculating voltage stresses.

Table 2.1: Normalized Voltage Stresses

Component	Voltage Stress Equation	Maximum Mode 1 Stress	Absolute Maximum Stress
C_r	M_{Crmax}	$1+\frac{\pi}{2}\frac{k+1}{k}Q$	2
S1	$M_{Crmax}+M$	$\frac{\pi}{2}\frac{k+1}{k}Q$	1
S2	1	1	1
D1	$-M$	1	1
D2	$1-M-M_{Crmin}$	$1+\frac{\pi}{2}\frac{k+1}{k}Q$	2

Current Stress

For convenience, all current stresses will be normalized to a base current defined by the input voltage V_g and circuit parameters:

$$I_B = \frac{V_g}{R_{N1}} = \sqrt{\frac{C_r}{L_{r1}}} V_g. \tag{97}$$

In this section, only mode 1 current stresses will be considered. This is because, unlike with voltage stress, the rms current stresses are universally larger in mode 2 than in mode 1. This is because in mode 2, all of the energy is transferred via the capacitor C_r, whereas in mode 1 a portion of the energy is transferred from input to output by L_{r1}. Thus, half sinusoidal currents with larger peaks are necessary for both the charging and discharging of C_r in mode 2, increasing rms current stresses throughout the converter. This is also the reason that M_{Crmax} is always higher in mode 2 versus mode 1, as shown in Fig. 2.14.

The simplest current stress to calculate is that of L_{r2} (or equivalently S2), since its current is always half-sinusoidal with fixed off-time variable frequency control. From the expression for i_{r2} in (20), the rms current stress can be calculated

$$I_{Lr2rms} = \sqrt{f_S \int_{t_1}^{t_3} |i_{r2}(t)|^2 dt} = \frac{V_O + V_{Crmax}}{R_{N2}} \sqrt{\frac{f_S}{4 f_{r2}}}, \tag{98}$$

which when normalized to I_B from (97) (and using the definition of F_S in (12)) becomes

$$H_{Lr2rms} = k(M + M_{Crmax}) \sqrt{\frac{F_S}{2}}. \tag{99}$$

The current stress of L_{r1} is slightly more complicated, as it is composed of a partial sinusoid and a linearly decreasing current. The component of the stress due to the partial sinusoid can be calculated from the expression for i_{r1} in (7)

$$I_{Lr1rma} = \sqrt{f_S \int_{t_0}^{t_1} |i_{r1}(t)|^2 dt} = \frac{V_g - V_{Crmin}}{R_{N1}} \sqrt{\left(\frac{1-F_S}{2}\right)\left(1 - \frac{\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}{\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)}\right)}. \quad (100)$$

Equation (100) normalized to I_B becomes

$$H_{Lr1rmsa} = (1 - M_{Crmin}) \sqrt{\left(\frac{1-F_S}{2}\right)\left(1 - \frac{\sin\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)\cos\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}{\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)}\right)}. \quad (101)$$

The component of the rms current due to the linear portion of i_{r1} expressed in (19) can similarly be calculated as

$$H_{Lr1rmsb} = (1 - M_{Crmin}) \sqrt{\frac{F_S}{3}\left(\frac{M_{Crmin}-1}{M}\right)\sin^3\left(\frac{\pi}{k}\left(\frac{1}{F_S}-1\right)\right)}. \quad (102)$$

The total rms current stress of L_{r1} then becomes

$$H_{Lr1rms} = \sqrt{H_{Lr1rmsa}^2 + H_{Lr1rmsb}^2}. \quad (103)$$

H_{Lr1rms} and H_{Lr2rms} are plotted in Figs. 2.17 and 2.18 for k = 2 and k = 3. The current stress in both inductors increases with load, as one would expect. Figs. 2.17 and 2.18 also show that increasing k has the effect of steering current stress from L_{r1} to L_{r2}, as the peak currents in L_{r2} need to be higher to discharge the capacitor during the shorter off-time.

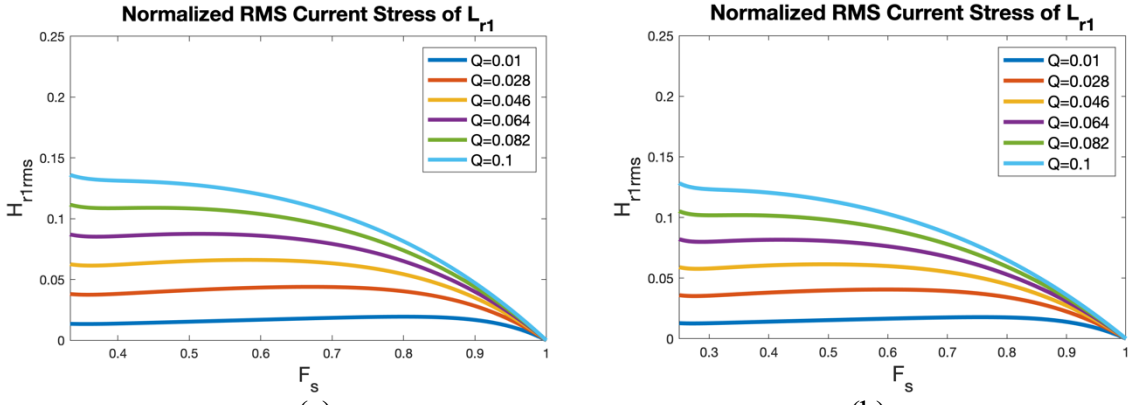


Fig. 2.17: Mode 1 rms current stress of L_{r1} for (a) k = 2 and (b) k = 3.

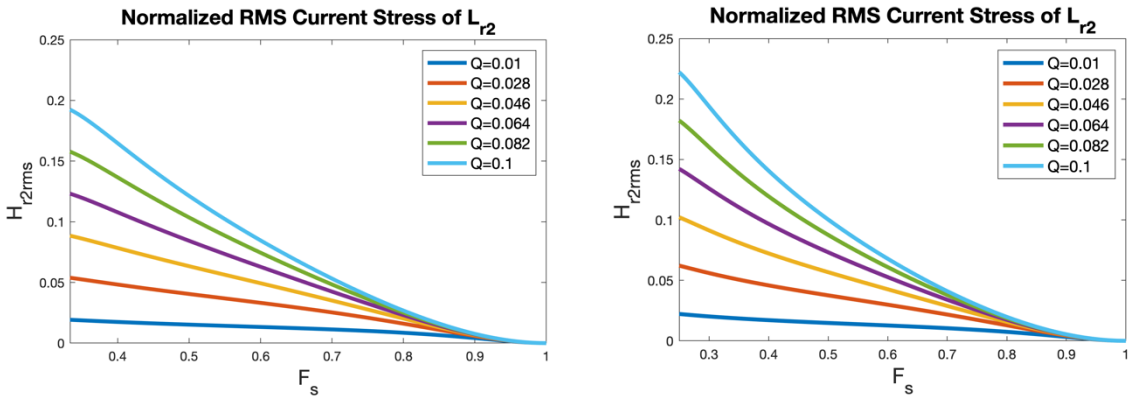


Fig. 2.18: Mode 1 rms current stress of L_{r2} for (a) $k = 2$ and (b) $k = 3$.

The rms current stress of C_r, S1, and S2 can be written in terms of (99), (101), and (102). Since the dominant loss mechanism in diodes is related to average current through their forward voltage drop, and not rms current through an equivalent on-resistance as with MOSFETs, the diode current stresses will be calculated as averages, not as rms values. The charging current of C_r is equal to the sinusoidal portion of i_{r1}, while its discharging current is equal to the half-sinusoidal current of i_{r2}. Thus, the normalized current stress of C_r can be written in terms of (99) and (101) as

$$H_{Crrms} = \sqrt{H_{Lr1rmsa}^2 + H_{Lr2rms}^2}. \tag{103}$$

The current in S1 is just equal to the sinusoidal portion of i_{r1}, or

$$H_{S1rms} = H_{Lr1rmsa}. \tag{104}$$

S2 is in series with L_{r2}, so

$$H_{S2rms} = H_{Lr2rms}. \tag{105}$$

As we saw in the Detailed Analysis section above, the average current in L_{r1} is equal to the average output current. Since D1 is in series with L_{r1}, we have

$$I_{D1avg} = -I_O, \tag{106}$$

or normalized to I_B,

$$H_{D1avg} = -MQ. \tag{107}$$

The average current in D2 is

$$I_{D2} = -\frac{1}{T_S}\left[\int_{t_0}^{t_3} i_{Cout}(t)dt + \int_{t_0}^{t_3} I_O dt\right] = -I_O, \tag{107}$$

where the charge balance of the output capacitor has been used to set the first term in the brackets to zero. Thus we also have

$$H_{D2avg} = -MQ. \tag{108}$$

This means that diode current ratings can be easily calculated from a specified output voltage and maximum power. Plots of H_{Crrms}, H_{S1rms}, and H_{D1avg}/H_{D2avg} are shown in Fig. 2.19 for $k = 2$. H_{S2rms} is not plotted as it is the same as Fig. 2.18.

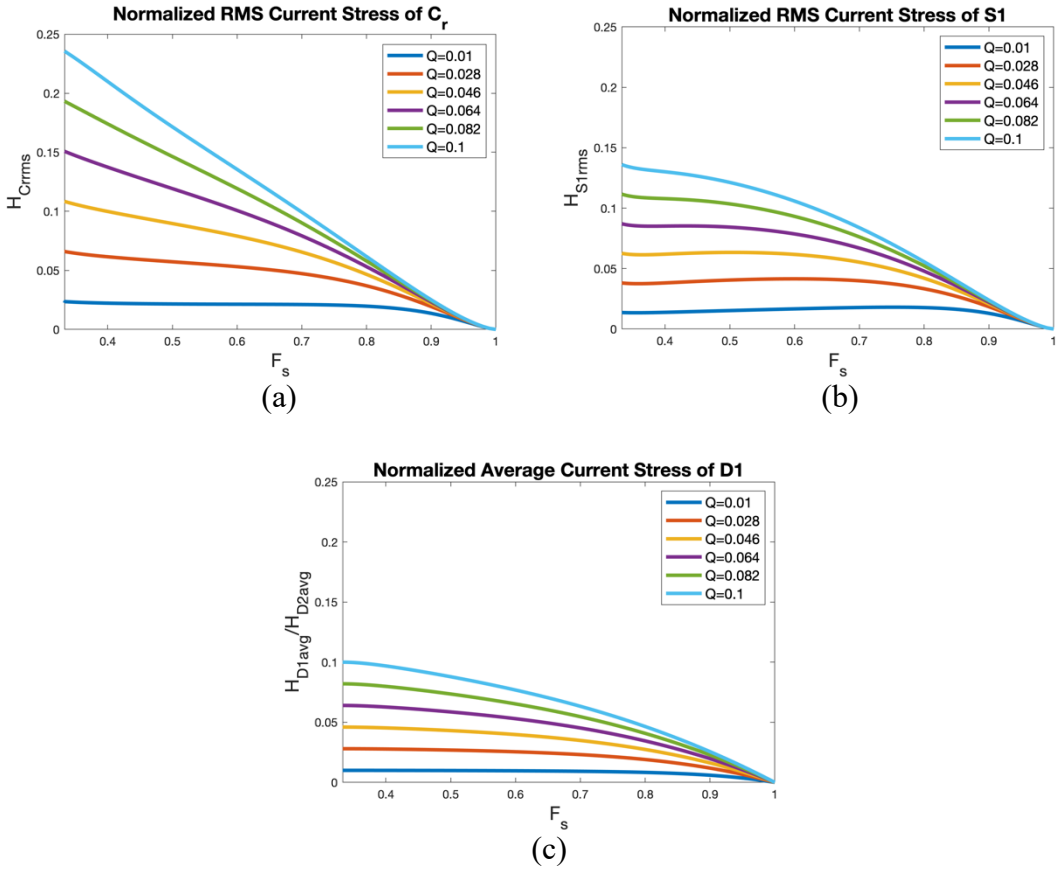


Fig. 2.19: Current stresses of (a) C_r (rms) (b) S1 (rms) and (c) D1 and D2 (average).

The current stresses derived above are summarized below in Table 2.2.

Table 2.2: Normalized Current Stresses

Component	Current Stress
L_{r1}	H_{Lr1rms} (103)
L_{r2}	H_{Lr2rms} (99)
C_r	H_{Crrms} (103)
S1	$H_{Lr1rmsa}$ (101)
S2	H_{Lr2rms} (99)
D1	H_{D1avg} (107)
D2	H_{D2avg} (108)

Design Procedure

Now that the voltage and current stresses have been derived, this section will describe how a dual resonant switched-capacitor polarity inverter can be designed given a specified input voltage, output voltage, and maximum power. The design process presented is iterative, as changing one design parameter will often affect many others. A flowchart of the design process is shown in Fig. 2.20, and will be explained in more detail in this section using the example of the experimental prototype that was built for this thesis. The prototype is open-loop with input voltage 80V and output voltage in the range –35V ~ –78V, with maximum output power 120W at –78V. The paragraphs below are numbered for ease of reference in the flowchart in Fig. 2.20.

1. As shown in Table 2.1, the absolute maximum voltage stresses of all components can be calculated directly from the input voltage specification. Alternatively, one could calculate just the maximum mode 1 voltage stresses later once k, C_r, L_{r1}, and L_{r2} have been chosen.

2. As this design process is iterative, a starting point for the resonant frequencies and k value are chosen, but they may be changed as the process continues. While high resonant frequencies do allow for higher power density, they are not necessary to achieve high power density as they would be for a PWM based step-down converter. For this reason, resonant frequencies in the range of 50kHz to 250kHz are recommended.

3. The choice of k controls three important parameters of the converter: the boundary frequency, the current stresses, and Q_{crit}. As (79) shows, for smaller k, the boundary frequency between mode 2 and mode 1, F_{SB}, moves to higher frequencies. This may be desirable as it limits the range of operating frequencies of the converter. However, as (83) shows, a smaller k also means a smaller Q_{crit}, so the range of loads may be limited if k is too small. As mentioned above, increasing k steers the current stress from L_{r1} to L_{r2}, and thus may increase the current stress of S2 too much for practical use. Based on these issues, a k value between 1 and 5 is recommended. The choice of $k = 1$ has the particular advantage of both inductances being equal, lowering the required inventory for manufacturing a large number of converters. Once the k value has been chosen, Q_{crit} and F_{SB} can be calculated using (83) and (79). For the prototype in this work, the values f_{r1} = 50kHz, f_{r2} = 100kHz, and $k = 2$ were chosen, leading to $Q_{crit} = \frac{4}{3\pi} \approx 0.424$ and $F_{SB} = \frac{1}{3}$.

4. After the resonant frequencies have been chosen, an initial C_r value should be chosen. The most important thing to keep in mind when choosing C_r is the characteristic impedance R_{N1}. In general, current stresses through the converter will be inversely proportional to this impedance. The critical load, R_{crit}, on the other hand, is directly

proportional to R_{N1} from (84). Thus, a small C_r may lower your current stresses, but may also make R_{crit} large, limiting the maximum power of the converter. Smaller C_r also means that L_{r1} and L_{r2} need to be larger, in general lowering the power density as the magnetics grow. Once a C_r value is selected, L_{r1}, L_{r2}, R_{N1}, R_{crit}, and I_B can be calculated from (5), (17), (6), (84), and (97), respectively. In addition, the minimum load resistance R_{min} and corresponding maximum Q Q_{max} can be calculated. For the prototype in this paper, C_r = 5μF was selected. The resulting inductances are L_{r1} = 2μH and L_{r2} = 0.5μH, with a characteristic impedance R_{N1} = 0.632Ω. The minimum load resistance is 48Ω, with corresponding Q_{max} of 0.0132. The critical load R_{crit} is 1.5Ω. Since 48Ω >> 1.5Ω, there is a safe margin with this choice of C_r. If the choice of C_r leads to an R_{crit} too large, the designer may increase C_r, thus lowering R_{crit}. Alternatively, one might increase k, which in turn will increase Q_{crit} and thus lower R_{crit}. As discussed previously, increasing k may lead to other issues, so it is recommended to increase C_r in most cases.

5. Once the capacitances and inductances have been selected such that $Q_{max} < Q_{crit}$, the current stresses can be calculated using the equations in Table 2.2. The maximum stresses do not always occur at the boundary frequency F_{SB}, and thus should be calculated numerically using MATLAB or a similar program. If these stresses are larger than desired, then lower resonant frequencies should be chosen while keeping C_r the same. This will increase L_{r1} and L_{r2}, thus increasing R_{N1}. The maximum calculated voltage and current stresses for the prototype in this thesis are tabulated in Table 2.3. As the rms current stress of C_r can be relatively high, multiple capacitors may be paralleled depending on the type of capacitor used. For example, for the design of this prototype,

five 1μF multilayer ceramic chip capacitors were paralleled. Once capacitances and inductances have been finalized and the current stresses calculated, appropriate components can be selected based on the stresses.

Table 2.3: Calculated Voltage and Current Stresses for Prototype

Component	**Voltage Stress (V)**	**Current Stress (A)**
L_{r1}	–	3.2 (rms)
L_{r2}	–	3.4 (rms)
C_r	160	4.2 (rms)
S1	80	3.0 (rms)
S2	80	3.4 (rms)
D1	80	1.8 (avg)
D2	160	1.8 (avg)

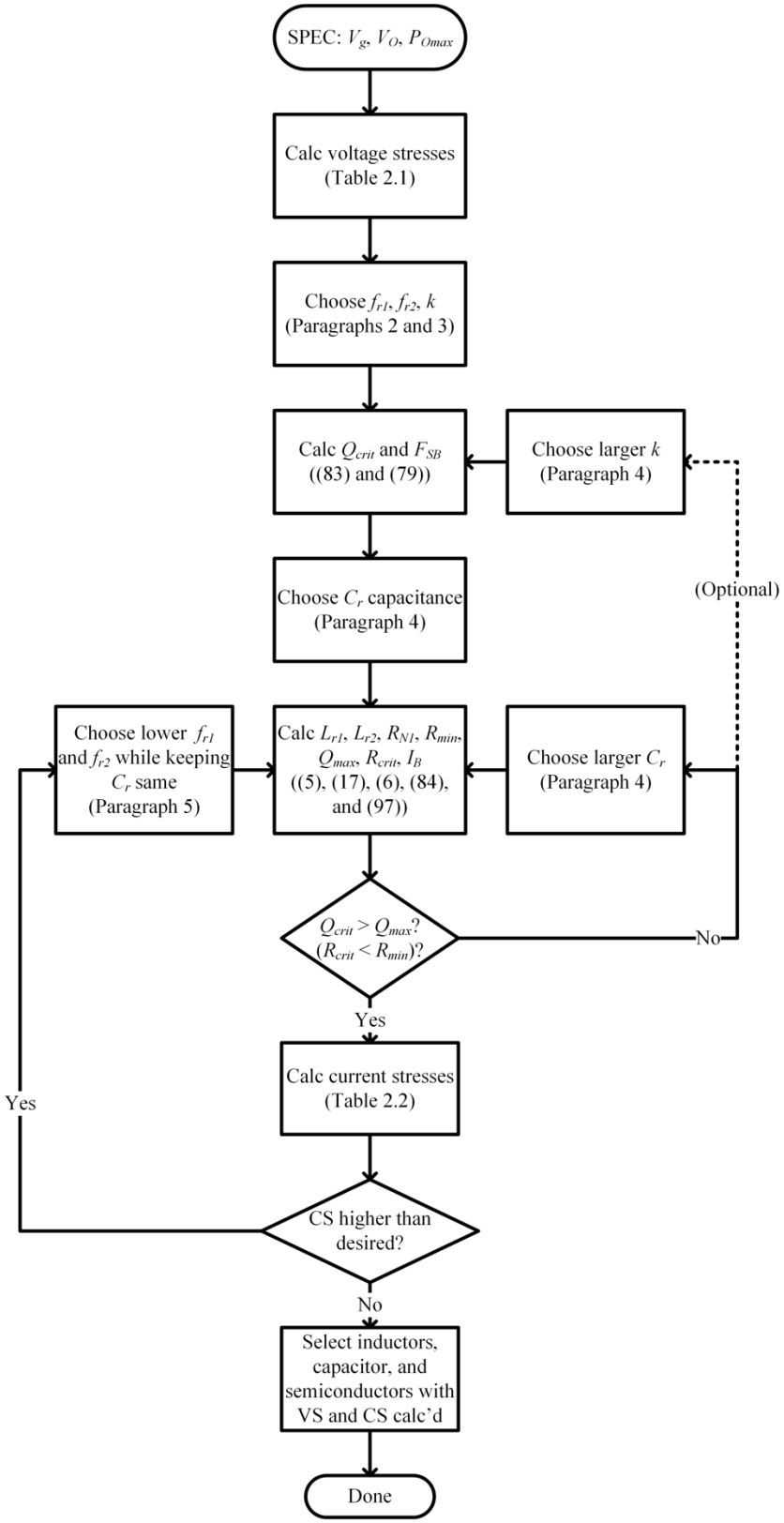


Fig. 2.20: Design guidelines for the dual resonant switched-capacitor polarity inverter.

Regenerative Snubber

As mentioned in Chapter 1, an important drawback of DRSCCs is high frequency ringing due to the presence on inductors in series with semiconductor components with parasitic capacitances. The DRSC step-down polarity inverter is no different. Fig. 2.21 shows the simulated switch and diode voltages when parasitic capacitances are added in parallel with all semiconductors. As expected, the two semiconductors in series with inductors, S2 and D1, experience very significant ringing at turn-off, when their parasitic capacitances are no longer shorted. This simulation does not include ESRs of components, so the ringing is undamped. In reality, the ringing looks more like Fig. 1.19a, i.e. a large spike followed by decaying magnitude. A partial solution that was used in [23] is inserting a blocking diode in series with S2, as shown in Fig. 2.22.

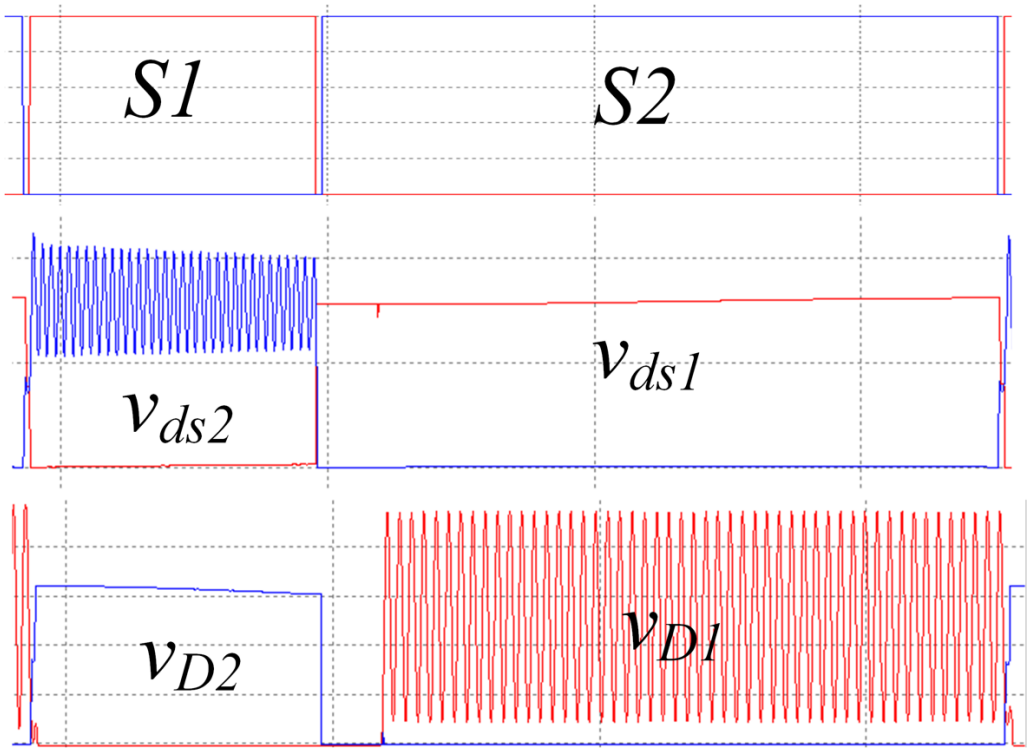


Fig. 2.21: Semiconductor voltage waveforms when parasitic capacitors are added to simulation.

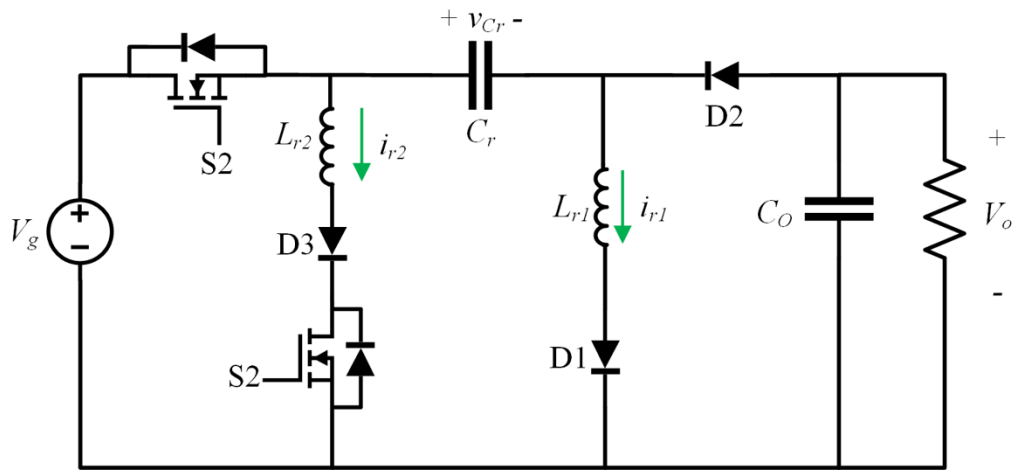


Fig. 2.22: DRSC step-down polarity inverter with blocking diode D3 in series with S2 to suppress parasitic ringing.

However, as we saw in Chapter 1, while this is effective for suppressing the ringing of S2, it does nothing to the ringing on D1. This is once again confirmed in simulation of the circuit in Fig. 2.22. In addition, this method reduces efficiency as D3 adds to the conduction loss during the discharge phase.

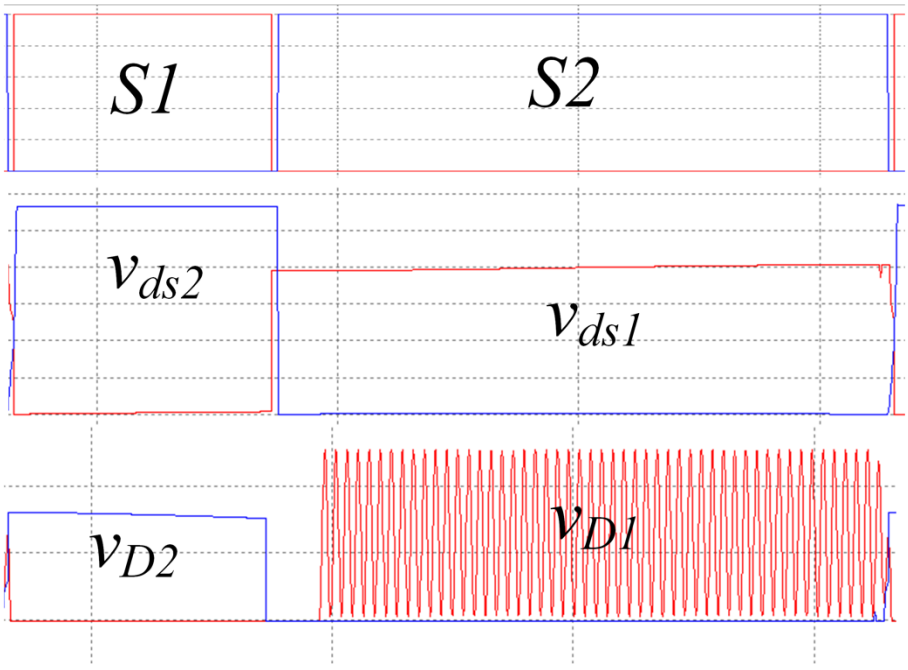


Fig. 2.23: Simulated semiconductor voltage waveforms with a blocking diode in series with S2.

Thus, the most effective way to ameliorate this problem would be to devise a snubber similar to that in [24] which simultaneously eliminates parasitic ringing and recovers energy from parasitic components. In the case of the DRSC step-down polarity inverter, this can be done very easily with the addition of only two diodes by using the input and output capacitors as snubber capacitors. The resulting converter with regenerative snubber is shown in Fig. 2.24. At turn off of D1, its parasitic capacitance begins to resonant with L_{r1}. However, when v_{D1} rises to be equal to $-V_O$, D3 is forward biased and clamps v_{D1} to be equal to $-V_O$, cutting off any further resonance. The same process happens at the turn-off of S2 with D4 turning on and clamping the voltage on S2 to V_g. The efficacy of the snubber was confirmed in simulation, shown in Fig. 2.25. In addition to eliminating parasitic ringing, with a small amount of deadtime the circuit in Fig. 2.24 also achieves ZVS turn-on of S2. This is because a portion of the current in L_{r1} at turn-off conducts as a reverse current in L_{r2}, discharging the output capacitance of S2. Thus, the energy stored in C_{ds2} is recovered to C_r through this reverse current. At turn-on of D1, C_{D1} is discharged to the load. S1 and D1 retain ZCS turn-on and D2 retains ZCS turn-off.

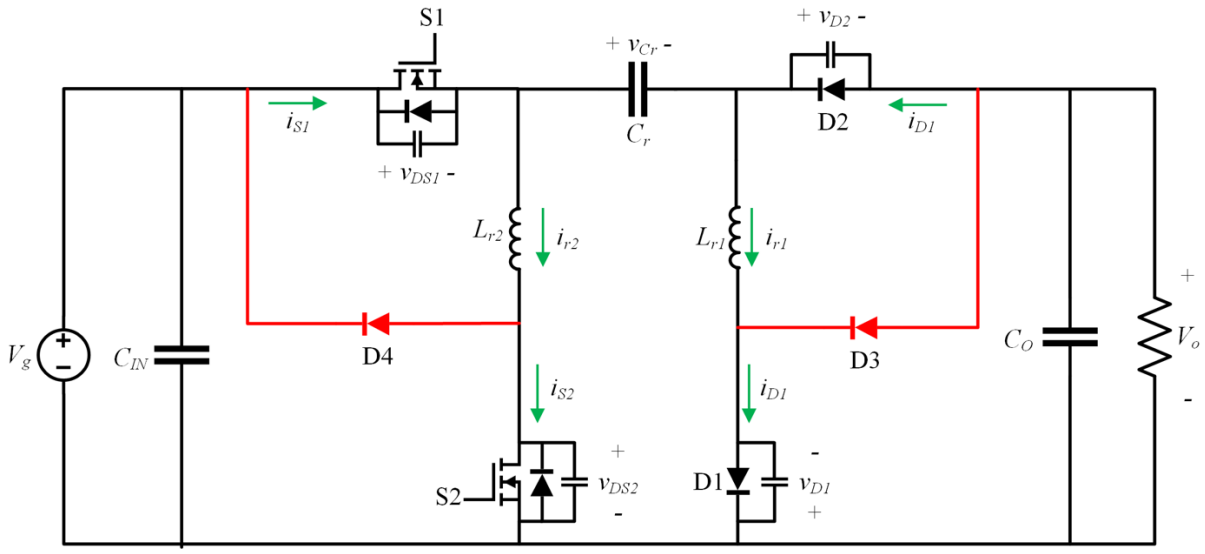


Fig. 2.24: DRSC step-down polarity inverter with regenerative snubber.

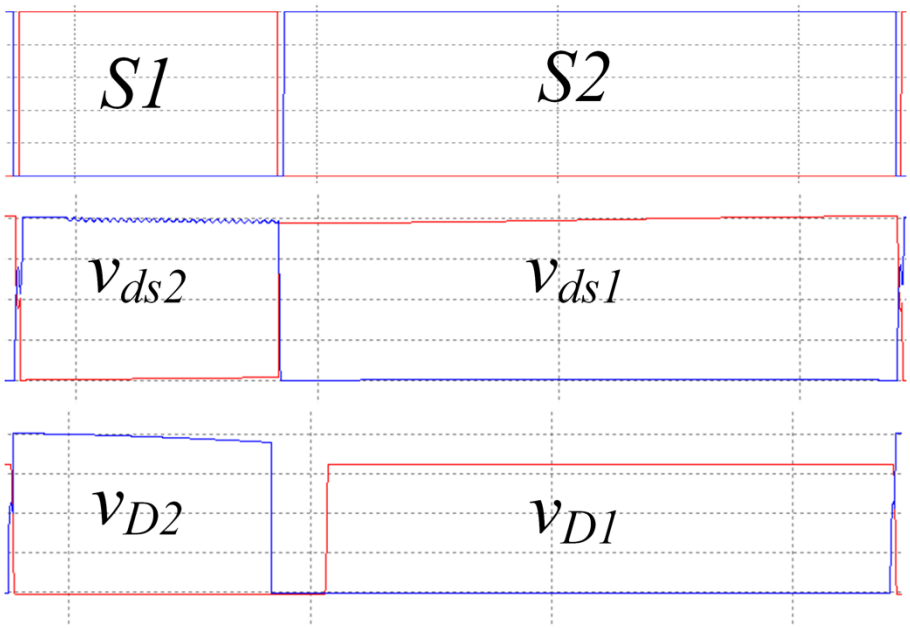


Fig. 2.25: Simulated semiconductor voltage waveforms with the regenerative snubber from Fig. 2.24.

While the addition of the regenerative snubber does change the inductor current waveforms slightly, the fundamental operating principle of the converter remains the same. In fact, as we will see in Chapter 3, the experimental voltage gain very nearly matches the theoretical voltage gain of an ideal DRSC step-down polarity inverter with no snubber. The prototype for this thesis was built with the snubber of Fig. 2.24 included. In terms of design, D3 and D4 can be selected to have the same rating as D2.

CHAPTER 3: Experimental Results

Prototype Details

As discussed in the previous chapter, an open-loop prototype of the dual resonant switched-capacitor step-down polarity inverter was built to verify its operation. The specifications of the prototype are an input voltage of 80V and output voltage in the range –35V ~ –78V, with a maximum power of 120W. The resonant frequencies selected were f_{r1} = 50kHz and f_{r2} = 100kHz. The components for the prototype were selected using the design guidelines from Chapter 2 (with some slight changes discussed below), and are summarized in Table 3.1.

Table 3.1: Selected Components for Prototype

Component	Value	Part No.	Voltage Rating	Current Rating
C_r	5µF	C5750X7T2W105K250KA × 5	450V	$2A_{rms}$ (each)
C_O	10µF	CGA9N3X7SA106M230KB × 4	100V	$3A_{rms}$ (each)
L_{r1}	2µH	SER2010-202MLB	–	$36A_{rms}$
L_{r2}	0.5µH	SER1590-501MLB	–	$27A_{rms}$
D1	–	SBR10200TR	200V	$10A_{avg}$
D2, D3, D4	–	20CTQ150	150V	$20A_{rms}$
S1, S2	–	STD25NF20	200V	$18A_{rms}$

Note that C_r has a much higher voltage rating than the 160V that was calculated as its absolute maximum stress in Table 2.3. This is because the capacitance of multilayer ceramic capacitors significantly reduces as the DC bias voltage increases. The DC bias characteristic from the datasheet of C_r is shown in Fig. 3.1. Notice that at half of the maximum rated voltage, the capacitance is reduced by as much as 60%. The DC bias of C_r is always equal to the output voltage, so a large enough voltage rating was selected such that with a maximum output of –78V, the capacitance would not change by more than 20%.

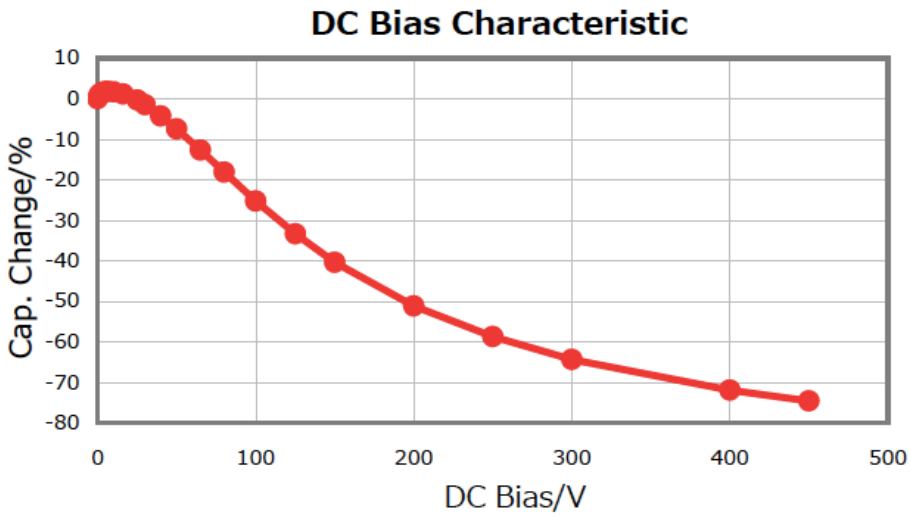


Fig. 3.1: Capacitance change versus DC bias voltage for C5750X7T2W105K250KA capacitor from [26].

The other important value to note in Table 3.1 is the low voltage rating of D2, D3, and D4, which is indeed smaller than the stress of 160V calculated in Table 2.3. The prototype was originally built with 400V diodes for D2, D3, and D4, but the large forward voltage drop of these higher voltage diodes significantly increased conduction losses in the converter. As mentioned in Chapter 2, the designer may choose to use the maximum mode 1 stress for component selection instead of the absolute maximum stress, which occurs at low frequencies in mode 2. Since this prototype was only going to be used in mode 1, (90) was used to calculate the maximum mode 1 voltage stress of D1 with the heaviest load $Q_{max} = 0.0132$

$$V_{D2\_max1} = \left(1 + \frac{\pi}{2}\frac{3}{2}(0.0132)\right)80V \approx 82.5V, \tag{109}$$

which is nearly half of the absolute maximum. Thus, using this calculated stress instead of 160V, 150V Schottky diodes with a much lower forward voltage drop were selected to increase efficiency.

Experimental Waveforms

The voltage regulation capability of the DRSC step-down polarity inverter is shown in Fig. 3.2. The input voltage, output voltage, and inductor currents are shown for the same load (Q = 0.0132) at three different frequencies. As the frequency is increased, we see the charging current of L_{r1} is cut off, and the output voltage decreases as expected. We can see from Fig. 3.2a that at F_{SB}, both inductor currents are approximately half-sinusoids. The waveforms of i_{Lr2} do not look half-sinusoidal as they would in the ideal case as F_S is increased. This is partially due to the ESRs of the capacitor and inductors, and partially due to the addition of the snubber, which, as mentioned, alters the current waveforms slightly without changing the fundamental operation. All waveforms below were captured on a Tektronix DPO 3014 Oscilloscope.

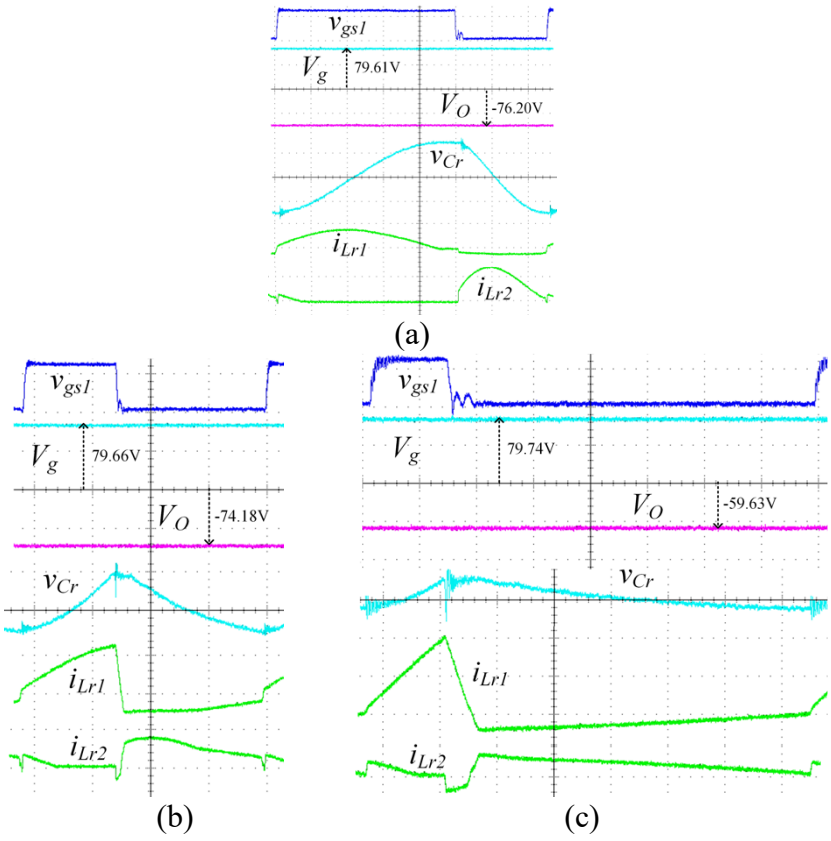


Fig. 3.2: Input voltage, output voltage, and resonant inductor current waveforms for Q = 0.0132 and (a) F_S = 0.33, (b) F_S = 0.6, and (c) F_S = 0.8. v_{gs1}: 10V/div, V_g and V_O: 50V/div, v_{Cr}: 2V/div, i_{Lr1}: 5A/div, and i_{Lr2}: 5A/div.

The switch voltage and current waveforms are shown in Fig. 3.3 for Q = 0.0132 and F_S = 0.6. The turn-on slope of i_{S1} in Fig. 3.3a is relatively large, but the switch still has ZCS turn-on. ZVS turn-on and ZCS turn-off of S2 are clearly visible in Fig. 3.3b.

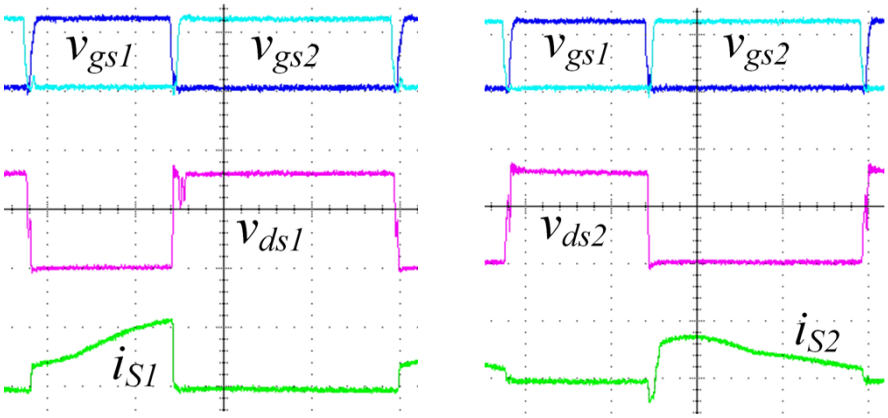


Fig. 3.3: Switch voltage and current waveforms for Q = 0.0132 and F_S = 0.6 for (a) S1 and (b) S2. v_{gs1} and v_{gs2}: 10V/div, v_{ds1} and v_{ds2}: 50V/div, i_{S1} and i_{S2}: 5A/div.

The voltage and current waveforms of D1 and D2 are shown in Fig. 3.4 for Q = 0.0132 and F_S = 0.6. ZCS turn-on and turn-off of D1 can be seen in Fig. 3.4a. The current waveform of D1 may be mistaken to show reverse recovery, but this is just the beginning of the parasitic ringing that is then clamped by the snubber diode D3. D2 retains its ZCS turn-off as expected.

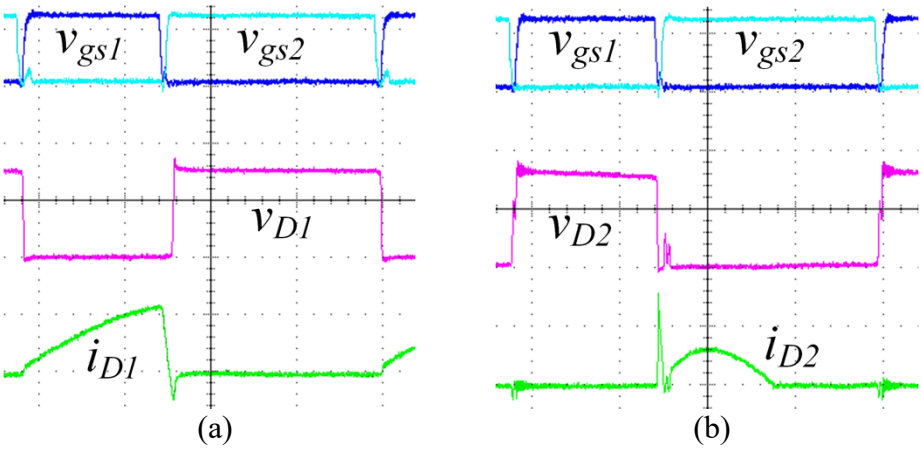


Fig. 3.4: D1 and D2 voltage and current waveforms for Q = 0.0132 and F_S = 0.6 for (a) D1 and (b) D2. v_{gs1} and v_{gs2}: 10V/div, v_{D1} and v_{D2}: 50V/div, i_{D1} and i_{D2}: 5A/div.

Gain and Efficiency

The input and output voltage and power were measured with two Chroma 66202 Digital Power Meters for four different loads at six different switching frequencies. The experimental voltage gain is plotted in Fig. 3.5 along with the theoretical voltage gain derived in Chapter 2 by equation (27) for an ideal converter. The experimental voltage gain very closely matches the theoretical, especially at light load when it is nearly equal for most frequencies.

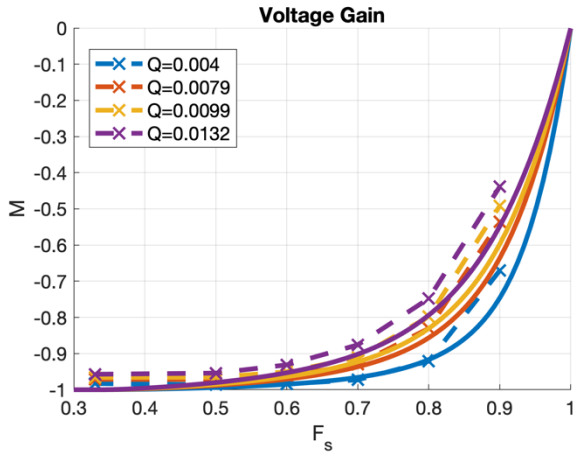


Fig. 3.5: Voltage gain versus frequency for 4 different loads. The solid lines are the theoretical ideal gain of the converter with no snubber, and the dashed lines are the experimental gain of the converter with the snubber.

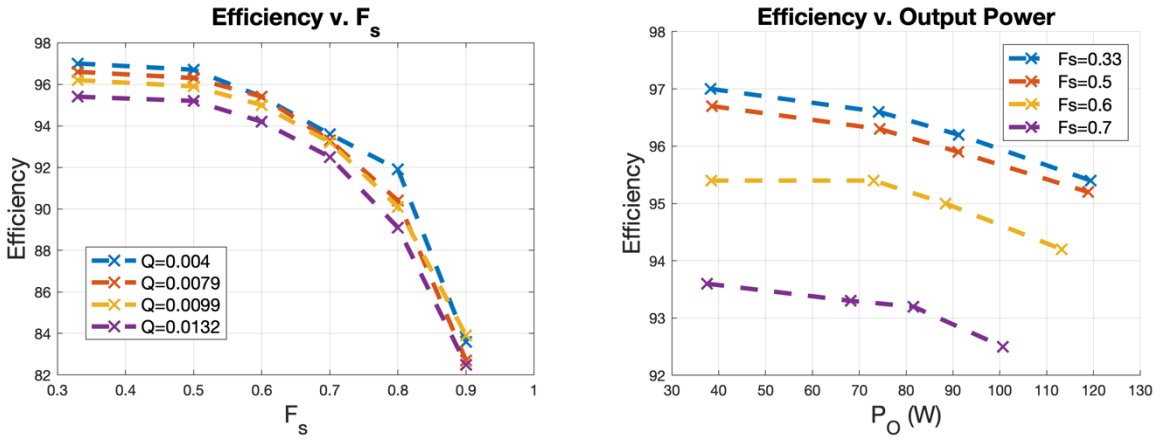


Fig. 3.6: Measured efficiency versus (a) frequency and (b) output power.

The measured efficiency versus both frequency and load is shown in Fig. 3.6. The peak efficiency is 97.0% at 38.3W of output power and appears at the boundary frequency of 67kHz. At the maximum rated power of 120W, the maximum efficiency is 95.4%. The efficiency varies by less than 2% over a 3 times increase in load. The efficiency also begins to drastically decrease as the switching frequency gets very high. This is most likely due to the large peak current values in S1 and D2. S1 and D2 are the only semiconductors that have a transition that is not ZCS or ZVS. As the frequency increases, the charging phase becomes shorter and thus the peak charging current is larger, as can be seen in Fig. 3.2. This peak charging current is the hard turn-off current of S1 and hard turn-on current of D2. Switching losses are inherently proportional to frequency, but in this case the magnitude of the energy lost in each cycle is also increasing with frequency, resulting in the steep drop off in efficiency at high frequencies.

CHAPTER 4: Topology Extensions

*n*X Step-Down

Because of the large drop off in efficiency at higher frequencies, it is recommended that a standard DRSC step-down polarity inverter be operated at no more than $F_S = 0.8$. Unfortunately, this limits the smallest step-down ratio that can be achieved, especially with light loads. This problem was the motivation behind extending the DRSC step-down polarity inverter to smaller step-down ratios. If an application requires a DC voltage to be stepped down and have its polarity inverted, and only needs regulation over part of the range from 0 to –1, then the resonant capacitor C_r can be replaced by a series-parallel switched capacitor cell with n capacitors. The resulting converter is called the nX step-down dual resonant switched-capacitor polarity inverter. The maximum voltage gain will be reduced to $-1/n$ from –1, allowing the new nX step-down version to operate closer to its boundary frequency where the efficiency is higher. The topology of the nX step-down DRSC polarity inverter is shown in Fig. 4.1.

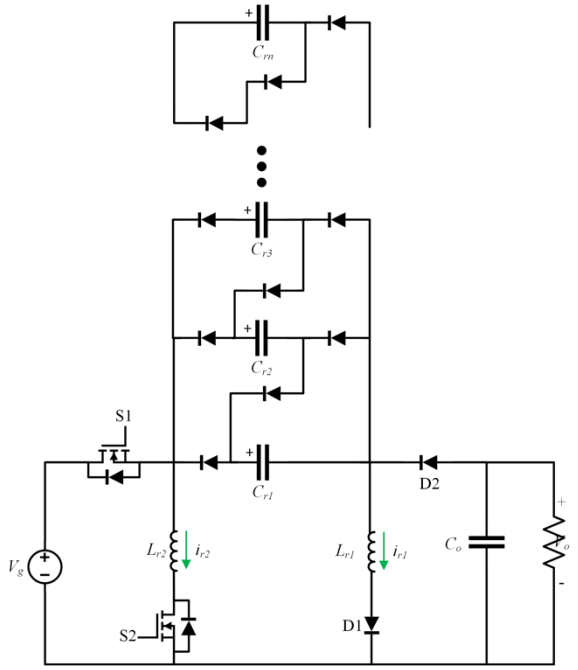


Fig. 4.1: Topology of the nX step-down DRSC polarity inverter.

Each additional capacitor requires 3 diodes and reduces the maximum gain by one integer step (i.e. 1/2, 1/3, 1/4, etc.). Notably, regardless of how many capacitors are added, only two inductors are needed for resonant charge and discharge. If the voltage gain is extended to very small step-down ratios, the diode forward voltage drops may become comparable to the output voltage. If this is the case, synchronous rectifiers can be used to replace the diodes and increase efficiency. The typical mode 1 topological states are shown in Fig. 4.2 for the simplest example, the 2X step-down DRSC polarity inverter.

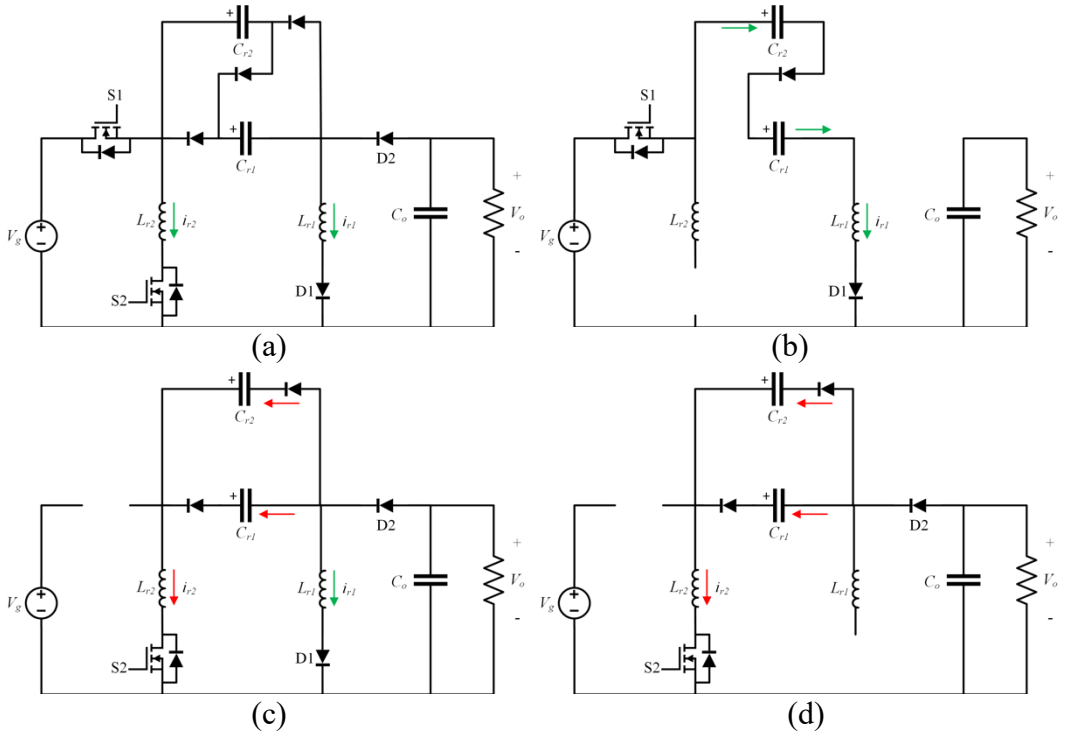


Fig. 4.2: (a) Topology of the 2X step-down DRSC polarity inverter. Operating states during (b) capacitors charging in series, (c) capacitors discharging in parallel, and (d) continued capacitor discharge.

Evidently, with the capacitors charging in series and discharging in parallel, the resonant frequencies of the *n*X step-down DRSC polarity inverter will be different than (5) and (17). Assuming that $C_{r1} = C_{r2} = C_{r3} = \ldots = C_{rn} = C$, the charging resonant frequency f_{r1} and discharging resonant frequency f_{r2} can be calculated below

$$f_{r1} = \frac{1}{2\pi\sqrt{L_{r1}\frac{C}{n}}} \tag{110}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{L_{r2}nC}}. \tag{111}$$

Crucially, the parameter *k*, the ratio between the two resonant frequencies, also changes to be equal to

$$k = \frac{f_{r2}}{f_{r1}} = n\sqrt{\frac{L_{r1}}{L_{r2}}}, \tag{112}$$

while the boundary frequency F_{SB} is unchanged from (79). Thus, if a standard DRSC step-down polarity inverter is being extended to an *n*X version, but the same boundary frequency is desired, then the ratio of the inductors must be changed accordingly. For example, if $k = 2$ is desired, previously this implied L_{r1} needed to be 4 times larger than L_{r2}, as it was in the prototype in Chapter 3. When extending to a 2X version, $k = 2$ is now achieved when L_{r1} and L_{r2} are equal.

*n*X Step-Up

In addition to extending to smaller step-down ratios, the DRSC polarity inverter can also be extended to step-up applications. Instead of replacing C_r with an SC cell that charges in series in discharges in parallel, C_r is replaced by an SC cell that charges in parallel and discharges in series, thus stepping up the voltage. Unfortunately, due to the polarity inversion, this extension requires 3 MOSFETs for every additional capacitor added, as shown in Fig. 4.3. Because of this, the *n*X step-up extension may not be as practical as the *n*X step-down extension. Just as in the *n*X step-down case, only two resonant inductors are required regardless of the number of capacitors added to the SC cell. The *n*X step-up extension is able to regulate the voltage gain between –1 and –*n*. The typical mode 1 topological states of a 2X step-up dual resonant polarity inverter are shown in Fig. 4.4.

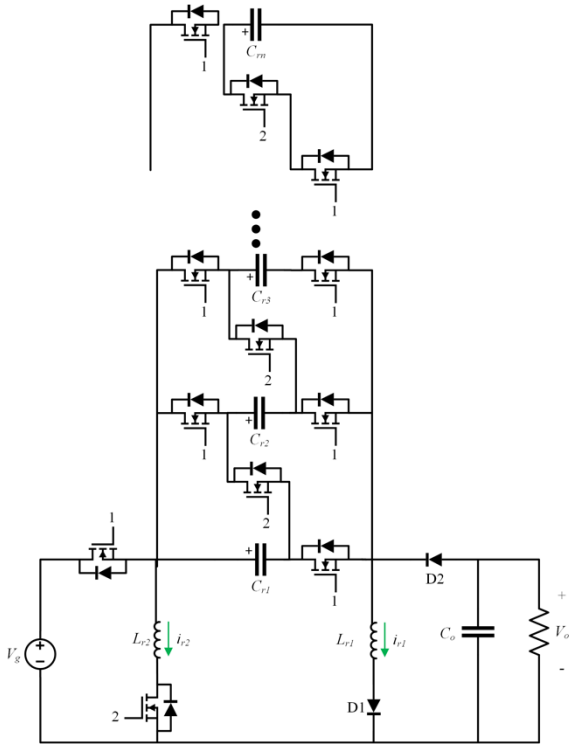


Fig. 4.3: Topology of the *n*X step-up DRSC polarity inverter.

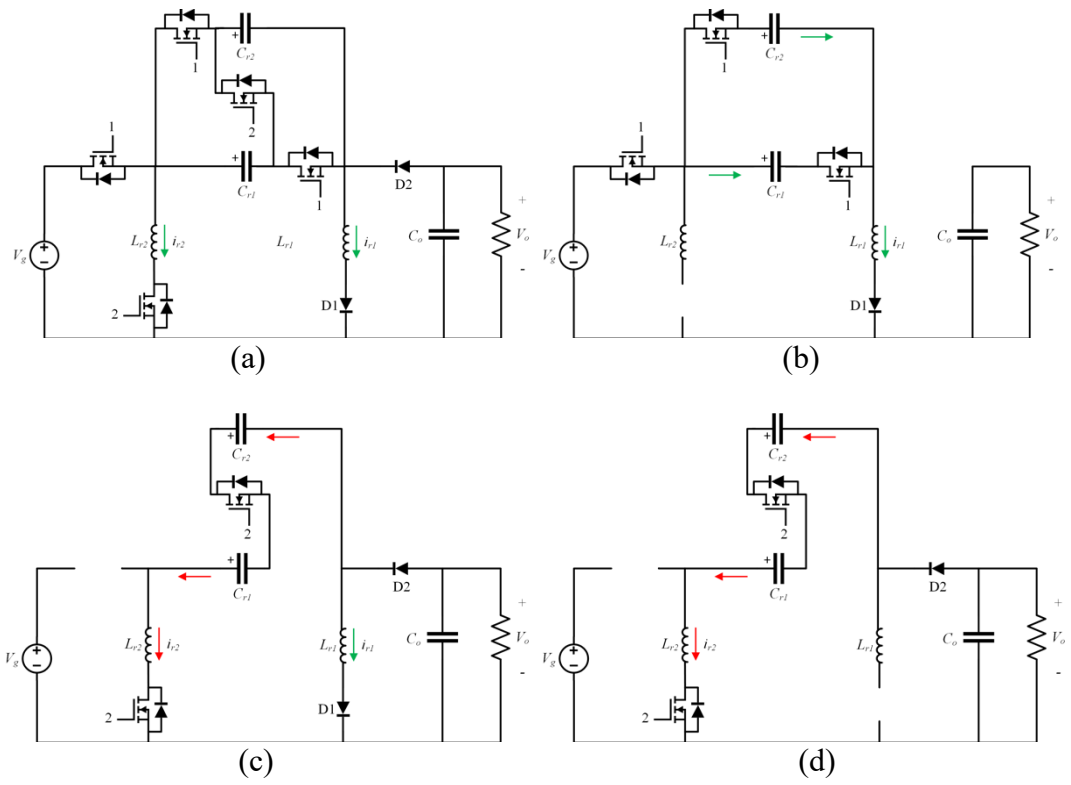


Fig. 4.4: (a) Topology of the 2X step-up DRSC polarity inverter. Operating states during (b) capacitors charging in parallel, (c) capacitors discharging in series, and (d) continued capacitor discharge.

Just as with the *n*X step-down extension, the resonant frequencies change from the standard DRSC step-down polarity inverter to the *n*X step-up DRSC polarity inverter. Once again assuming all resonant capacitors are equal to a value *C*, the resonant frequencies can be calculated as

$$f_{r1} = \frac{1}{2\pi\sqrt{L_{r1}nC}} \tag{113}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{L_{r2}\frac{C}{n}}}. \tag{114}$$

The new value of *k* can be then be found to be

$$k = \frac{f_{r2}}{f_{r1}} = \frac{1}{n}\sqrt{\frac{L_{r1}}{L_{r2}}}, \tag{115}$$

with the boundary frequency remaining unchanged from (79).

Equation (115) is another indicator that the *n*X step-up DRSC polarity inverter may not be practical. Because k is inversely proportional to n, as the step-up ratio n is increased, the ratio between L_{r1} and L_{r2} must be very large to keep k from becoming very small. Even in the example of keeping $k = 2$ for a 2X step-up DRSC polarity inverter, L_{r1} must be 16 times larger than L_{r2}, compared to 4 times larger for the standard DRSC step-down polarity inverter. As n increases, the ratio between the two inductances grows like n^2 for a fixed k. Due to this fact, along with the number of MOSFETs necessary for large step-up ratios, the *n*X step-up DRSC polarity inverter may only be practical for small step-up ratios in the range of 2 or 3 at most.

Both the *n*X step-up and *n*X step-down extensions also inherit the parasitic ringing issue due to inductors appearing in series with semiconductors. However, because the number of inductors and their location do not change regardless of the step-down (or step-up) ratio, the same snubber used in Fig. 2.24 can be applied to the extended topologies as well.

Moving Inductors

As discussed in Chapter 1, in [24] it was shown that alternate versions of the original DRSC converters presented in [22] and [23] can be created by moving the locations of the resonant inductors to the other two semiconductors. The DRSC step-down polarity inverter is no different, and the result of moving the inductors to S1 and D2 is shown in Fig. 4. 5. Immediately the similarity between the circuit in Fig. 4.5 and the traditional PWM Ćuk converter is obvious. As mentioned in Chapter 1, the Ćuk converter can in fact be viewed as a hybrid switched-capacitor converter based on the SC polarity inverter.

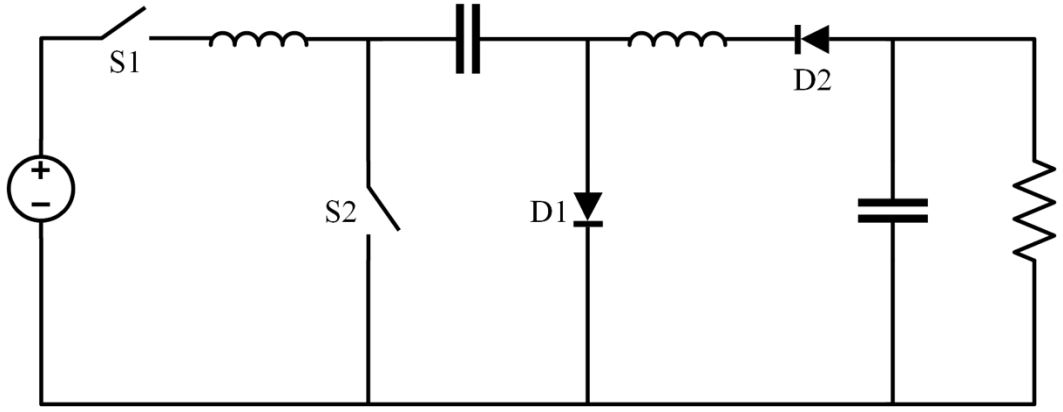


Fig. 4.5: Alternate form of DRSC step-down polarity inverter with inductors moved to be in series with S1 and D2.

Just as with the extensions in [24], the on-time of S1 must now be fixed instead of its off-time, so that the charging current of the resonant capacitor is always a half-sinusoid and S1 can safely turn-on and turn-off with zero current. Interestingly, just as the Ćuk converter has the advantage of continuous input and output current, the input and output current waveforms are the chief advantage of this topology over the standard DRSC step-down polarity inverter. They are not continuous as in a Ćuk converter, but they do have generally better features than the standard DRSC step-down polarity inverter. In the standard topology, the input current is a partial sinusoid that is cut short, and the output current through D2 has a large spike at turn-on followed

by a half-sinusoid. In the converter in Fig. 4.5, on the other hand, the input current is always a half-sinusoid, and D2 has ZCS turn-on and turn-off. Thus, neither the input source nor the load experience sudden changes in current. This may be especially advantageous if the input source is a battery, for example, where large current spikes can introduce more loss in the ESR of the battery and more quickly deplete its energy.

However, the alternate DRSC step-down polarity inverter also has an important disadvantage. Just as with all dual resonant switched-capacitor converters, it experiences parasitic ringing in the branches where inductors and semiconductors are in series. Applying a regenerative snubber to S1 and D2 in Fig. 4.5 is a much more challenging issue than in the standard DRSC step-down polarity inverter, where parasitic ringing could be eliminated by the introduction of only two diodes. In addition, if the parasitic ringing cannot be eliminated, it appears in branches that are connected directly to the input and output, meaning the ringing may damage the input source or the load in addition to potentially destroying the semiconductors inside the converter.

CHAPTER 5: Summary and Conclusions

Switched-capacitor DC-DC converters first arose in Japan as a compact and lightweight alternative to traditional PWM converters, but their high output impedance, large current spikes, and lack of regulation held them back from applications requiring more than 1 to 10W [4]–[6]. In an effort to extend the range of applications for which SC converters could be used, researchers began to hybridize them with PWM converters by adding large low-ripple inductors into the charging/discharging path of flying capacitors [10] [11]. These hybridizations often lost the inherent size and weight advantage of SC converters, and over time this research effort shifted towards applying SC cells to extend the voltage gain of PWM converters in high step-up or step-down applications [12]–[14].

In order to eliminate current spikes while maintaining small size and weight, researchers in Hong Kong began employing inductors in a different way [15]. Instead of the large, low-ripple inductors of PWM converters, small resonant inductors were placed in series with the flying capacitors of SC converters. These new resonant switched-capacitor converters proved very effective at their desired goal of introducing ZCS of all switches and soft charging of all capacitors. They also allowed, as [17] shows, for SC topologies to be extended to high power applications. However, RSCCs, just like the underlying SCCs, have limited ability to regulate the output voltage. Thus, the problem of regulation in SC converters while retaining power density remained unsolved.

Dual resonant SC converters, first introduced in 2012, are the solution to this problem. Just as with RSCCs, they employ small resonant inductors to allow for soft charging and discharging of the flying capacitor. However, with the inductors placed in series with switches instead of the capacitor, the charging (or discharging) interval can be cut short, allowing for

voltage regulation. The energy leftover in one of the resonant inductors when the charging is cut short is then recovered to the output. This technology was first applied to the traditional 1/2X series-parallel step-down SC converter of Fig. 1.2a [22]. It has since been extended to the 2X parallel-series step-up SC converter of Fig. 1.2b [23], and further extended to general nX step-up applications [25]. The two major disadvantages of DRSCCs are that the maximum voltage gain is limited by the underlying SC topology and the inductors in series with semiconductors invariably leads to undesirable high frequency ringing with parasitic capacitances. The former is addressed for step-up applications in [25] by introducing a method to extend the voltage gain with additional capacitor cells, the latter in [24] with the implementation of a regenerative snubber for both step-down and step-up applications.

However, up until now the issue of limited regulation range had not been addressed for step-down applications. In addition, no DRSCC had been invented for applications that require an output voltage of opposite polarity. Both of these issues are solved by the converter examined in this thesis, which is derived by introducing dual resonance to the traditional SC polarity inverter of Fig. 1.2c. As the underlying SC converter has unity gain with inverted polarity, the resulting DRSCC can regulate the voltage gain from 0 to –1.

The resulting converter has been analyzed in detail in Chapter 2, including deriving the voltage gain curve of four distinct modes of operation. The boundary conditions between several modes have also been discussed. Using these boundary conditions and a complete analysis of voltage and current stresses throughout the converter, design guidelines have been created to take a specified input voltage, output voltage, and maximum power and design a DRSC polarity inverter. A simple, two diode regenerative snubber has been employed for practical implementation of the converter.

In Chapter 3, a 120W prototype of the converter was built and tested to verify the operation of the topology. The prototype achieved a peak efficiency of 97.0% at light load and 95.4% at full load. The experimental results verified the converter's ability to regulate versus variation in both line and load. These results also verified the ZVS turn-on operation of S2, and the ZCS operation of S1 (turn-on), D1 (turn-on), D2 (turn-off), and S2 (turn-off). However, it was observed that the efficiency dropped off very quickly as the frequency increases due to the large switching losses incurred by S1 and D2.

This issue was addressed in Chapter 4 by extending the topology to have a maximum gain of $-1/n$ with the addition of n SC cells. With the nX extended topology, applications that do not require regulation over the entire range from 0 to –1 can lower the maximum gain of the converter, thus allowing it to operate at lower, more efficient frequencies. Both the original DRSC polarity inverter and its nX step-down extension only require two small resonant inductors, so lightweight designs and high power density can be achieved. An nX step-up extension is also presented, though is likely of little practical use. An alternate form of the DRSC polarity inverter with the inductors placed at the input and output is discussed, along with its advantages and disadvantages.

In conclusion, a complete discussion of the development, operation, and design of a new dual resonant switched-capacitor converter topology is presented in this thesis. I hope to continue the research effort on resonant and dual resonant switched-capacitor converters to expand the reach of these types of converters. In particular, one of the most important and least explored areas related to resonant switched-capacitor converters is small-signal modeling for control loop design. The development of state space averaging by Ćuk and Middlebrook [27] was one of the key breakthroughs in understanding PWM converters and making robust closed loop controller

design feasible. As of yet, little to no work has been done in modeling the small signal behavior of dual resonant SC converters, or resonant SC converters in general. Having gained a deeper understanding of resonant switched-capacitor converters through the development of this work, I hope to explore this new territory in the future and help to bring resonant switched-capacitor converters into the limelight.

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