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Abstract

We study signal integrity effects on statistical timing analysis, e.g., interconnect and gate delay variations induced by crosstalk aggressor alignment, i.e., difference in signal arrival times in coupled neighboring interconnects. Such effects bring significant source of variation, and must be taken into account in statistical timing analysis. We establish a functional relationship between signal propagation delay and crosstalk alignment by deterministic circuit simulation, and derive closed form formulas for statistical distributions of output signal arrival times. Our proposed method can be smoothly integrated into a static timing analyzer, which runtime is dominated by sampling deterministic delay calculation, while probabilistic computation and updating take constant time. Our experimental results on 70*nm* technology global interconnect structures and 130*nm* technology industry designs show that lack of statistical crosstalk alignment consideration could lead to up to 114.65% (71.26%) differences in interconnect delay means (standard deviations), and 159.4% (147.4%) differences in gate delay means (standard deviations), while our method gives within 1.28% (3.38%) mismatch in interconnect output signal arrival time means (standard deviations), and within 2.57% (3.86%) mismatch in gate output signal arrival time means (standard deviations), respectively.

I. Introduction

VLSI manufacturing processes today face increased variations of layout geometries and circuit performance. Limits on manufacturing equipment include (1) lithographic issues, e.g., optical proximity, defocus, and lens aberration, which affect feature dimensions, such as wire width or transistor channel length; (2) the chemical-mechanical planarization (CMP) process which varies feature thickness for different local layout density; and (3) dopant variations in chemical processes. On the other hand, aggressive VLSI designs induce increased variations on system performance. Integration of increased number of components in a single chip results in increased supply voltage drop and temperature variation; higher operating frequencies observe increased capacitive and inductive couplings on silicon surface and through substrate; and aggressive performance opti-

mization could result in a large number of near-critical paths with increased probability of timing failure.

In the above context, timing verification moves away from the traditional over-pessimistic best/worst case analysis and explicitly addresses increased variability. (1) Traditional minimum/maximum based timing analysis, which verifies timing requirements between either minimum or maximum path delays, captures only die-to-die variations. (2) Corner based timing analysis, which allows timing verification between minimum and maximum path delays, captures intra-die variations. (3) Statistical static timing analysis (SSTA), which computes delay distribution for each pin (block-based) or path (path-based), provides "timing yield" or probability for a chip to meet timing requirements.

Block-based SSTA [1], [28] represents signal arrival time variation at each pin as a probability distribution function (pdf). Assuming symmetry or normality of signal arrival time distributions, these probability distribution functions are computed based on simple formulas in a breadth-first netlist traversal, which is efficient, incremental, and suitable for optimization. Path-based SSTA [17], [18] provides more accurate statistical analysis on a set of near-critical paths, e.g., in corner-based or Monte Carlo analysis, signal arrival time at a pin could have different distributions in different paths, where correlations due to path-sharing can be better captured. Timing criticality probabilities and correlations of the near-critical paths are computed for signoff analysis.

Correlations come from (1) path-sharing in the presence of reconvergent fanouts, and (2) dependence on common variational parameters. Correlated pdf's can be propagated in conditional probabilities [1]. Correlated parameters can be broken down into uncorrelated random variables via principle component analysis (PCA) [5], [15], [26]. Layout geometrical variations can be translated into performance variations by sensitivity-based[3], interval-valued [14], or matrix-perturbation-theory-based [13] analysis through interconnect model order reduction [16].

Including more sources of variation into consideration has significantly improved accuracy of statistical timing analysis. For example, the mean and the standard deviation of the delay of a gate observe significant deviation when multiple inputs of the gate are switching at the same time [2]. According to [2], neglecting this multiple-input switching effect could underestimate the mean delay of a gate by up to 20% and overestimate the standard deviation of the delay of a gate by up to 26%.

In this paper, we propose signal integrity effects aware statistical timing analysis, and consider

an equally significant source of variation in SSTA, i.e., crosstalk aggressor alignment effect on signal propagation delay for a driver gate and its load interconnect. A crosstalk aggressor signal transition injects a noise into a victim net, and causes (1) interconnect delay variation, and (2) driver gate effective load capacitance hence driver gate delay variation. The arrival time of a crosstalk aggressor signal transition affects the victim net interconnect delay and its driver gate delay variations. Therefore, the statistical properties (e.g., pdf's) of signal arrival times in coupled interconnects are interdependent. Existing publications address this effect based on the traditional "timing window" concept, which is oversimplified and inadequate [12], [24]. Our present work is the first in proposing an analytical statistical delay calculation method which takes signal integrity effects into account.

Our proposed method includes the following steps. We base our statistical timing analysis on process variation extraction results, and represent signal propagation delays in polynomial of random variables. We establish functional relationships between signal propagation delays and crosstalk aggressor alignments, and derive closed form formulas for output signal arrival time distributions. We verify our theoretical signal integrity aware statistical delay calculation methods by SPICE Monte Carlo simulation on BPTM 70*nm* global interconnect structures and instances from 130*nm* technology industry test cases. Our experiments show that lack of statistical crosstalk consideration could lead to up to 114.65% (71.26%) mismatch of interconnect delay means (standard deviations), and 159.4% (147.4%) mismatch of driver gate delay means (standard deviations); while our method gives interconnect output signal arrival times means (standard deviations) within 1.28% (3.38%), and driver gate output signal arrival times means (standard deviations) within 2.57% (3.86%) of SPICE Monte Carlo simulation results.

We organize the rest of this paper as follows. We presents our proposed signal integrity aware statistical timing analysis method in Section II and describes several implementation techniques in Section III. We presents experimental results which verifies our theoretical derivations in Section IV, before we conclude this paper with our ongoing research directions in Section V.

II. THEORY

A. *Problem Formulation*

Several signal integrity effects have significant impacts on signal propagation delay in a nanometer-scale VLSI design. For example, a signal transition in an (aggressor) interconnect

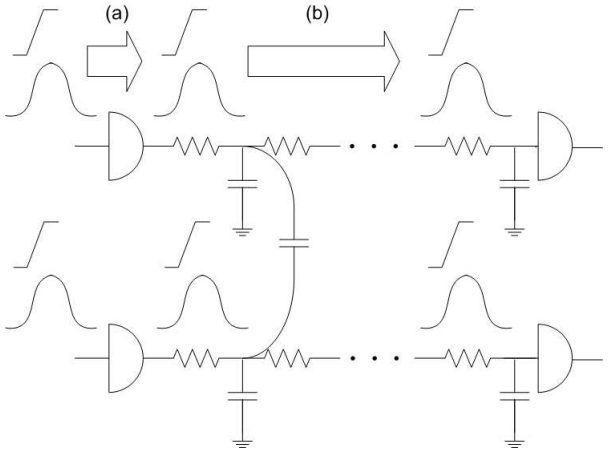

Fig. 1. Statistical timing analysis in the presence of crosstalk aggressor alignment effect (SSTA-SI) includes (a) computing gate delay and gate output signal arrival time distribution, and (b) computing interconnect delay and interconnect output signal arrival time distribution.

would inject a noise to a neighboring (victim) interconnect via capacitive coupling. Such a injected noise distorts a signal transition waveform in the victim interconnect, and affects signal propagation delay in the victim interconnect, if the injected noise arrives before the signal transition in the victim interconnect reaches its delay threshold, e.g., $50\%V_{dd}$. The victim interconnect delay alteration depends on the timing of the injected noise, for example, the maximum delay alteration takes place when the signal transitions at the crosstalk aggressors are aligned such that an injected noise with the maximum peak value is formed, which is then aligned with the victim net signal transition for the maximum delay alteration of the victim interconnect [8].

Moreover, the gate delay for the driver of the victim interconnect also depends on the timing of the injected noise. This is because (1) an injected noise affects the gate output voltage, which leads to gate output current variation, and (2) an injected noise affects the resistive shielding of the load interconnect, and leads to different "effective capacitance" for the driver gate, hence different driver gate delay [25].

Such signal integrity effects, i.e., of crosstalk aggressor alignment on interconnect and gate delays, have been taken into consideration in traditional deterministic timing analysis, and they must also be taken into consideration in statistical timing analysis. Several existing publications include crosstalk coupling effect in statistical delay calculation [12], [24], but they are only based on the transitional timing window concept, and did not provide an analytical statistical model for crosstalk aggressor alignment effect on signal propagation delays.

In this paper, we take signal integrity effects, e.g., of crosstalk aggressor alignment on interconnect and gate delays, in statistical timing analysis, and consider the following problem.

Problem 1[Signal Integrity Aware Statistical Delay Calculation]
Given

1. *a system of capacitively coupled interconnects with their driver gates,*
2. *statistical signal arrival time variations at the inputs of the driver gates, and*
3. *statistical process parameter variations for the interconnects and their driver gates,*

find *statistical signal arrival time variations at the output of the system.*

We list some of the notations that we use in this paper as follows.

- $x_1(x_2)$ = input signal arrival time
- $x' = x_2 - x_1$ = crosstalk alignment
- D_g = driver gate delay
- y_1 = output signal arrival time
- $\mu_1(\mu_2) = \mu_{x_1}(\mu_{x_2})$ = mean of input signal arrival time
- $\sigma_1(\sigma_2) = \sigma_{x_1}(\sigma_{x_2})$ = standard deviation of input signal arrival time
- $cov(x_1, x_2)$ = covariance of inputs signal arrival times
- $\mu'(\sigma') = \mu_{x'}(\sigma_{x'})$ = mean (standard deviation) of crosstalk alignment
- $N(\mu, 3\sigma)$ = normal distribution of mean μ and standard deviation σ

In the following sections, we present our signal integrity aware statistical delay calculation method which computes statistical signal arrival times at the outputs of a coupled interconnect system. We adopt a recently developed general representation in statistical timing analysis, and consider input signal arrival time distributions in polynomials of possibly correlated random variables [9]. We apply deterministic delay calculation and establish a functional relationship between signal propagation elay and crosstalk alignment, which serve as a foundation for statistical delay calculation in consideration of crosstalk alignment effect. In particular, we derive closed form formulas for output signal arrival time distributions for given statistical crosstalk alignments.

We present the details of our proposed method as follows.

B. Process Variation Extraction

A signal arrival time in nanometer VLSI designs may not be in a Gaussian distribution. A random variable is observed to be in a Gaussian distribution if it is affected by one or more uncorrelated variational parameters. A signal arrival time in a nanometer-scale VLSI designs is affected by multiple correlated variational parameters, including inter-die, location dependent, and purely random variations. I.e., a parameter variation includes components of (1) variations between dies, (2) purely random variation, and (3) variations which are functions of locations of the components [15]. E.g., in Pelgrom's model [21], the standard deviation of a process parameter p, e.g., transistor channel length, is proportional to the square of the distance between the two transistors on a chip.

$$\sigma_p^2 = \frac{A_p}{WL} + S_p^2 D^2 \tag{1}$$

where W and L are respectively transistor channel width and length of the two devices, D is the distance between the two devices, A_p and S_p are coefficients.

The number of parameter variations $\vec{x}$ can be reduced by principle component analysis (PCA) to a smaller set of uncorrelated standard Gaussian random variations $\vec{z}$ (Gaussians with zero means and unit variance) [5], [15], [26], e.g.,

$$x_i = \sum_j a_{ij} z_j \tag{2}$$

such that

$$\sigma_{x_i}^2 = \sum_j a_{ij}^2 \tag{3}$$

A signal arrival time x in a nanometer VLSI design is a function of these parameter variations. Such a function can be approximated in a polynomial function [9], e.g., of uncorrelated standard Gaussian random variables (by applying PCA).

$$\begin{aligned} x &= f_i(r_1, r_2, ...) \\ P(r_i) &= \frac{1}{\sqrt{2\pi}\sigma_{r_i}} e^{-\frac{(r_i - \mu_{r_i})^2}{2\sigma_{r_i}^2}} \end{aligned} \tag{4}$$

Here are two dimensions of complexity: the number of random variables and the degree of the polynomial approximation. Our proposed method can handle up to quartic polynomial approximation, as long as an analytical solution of a polynomial is available which is needed in our closed form derivation. Our method can be applied to an increased number of random variables, although with decreasing efficiency. We present our method in the following sections.

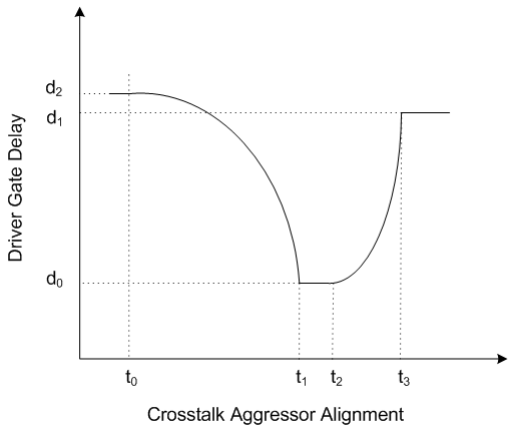

Fig. 2. Interconnect or driver gate delay as a function of crosstalk alignment. $d_1 = d_2$ for interconnect delay.

C. Performance Characterization

To enable statistical propagation of signal arrival times across a coupled interconnect and its driver gate, we establish a functional relationship between a driver gate (load interconnect) delay and a crosstalk aggressor alignment. This is achieved by performing deterministic delay calculation for a set of "sampled" crosstalk alignments, and extract a piecewise polynomial function based on the sampling data. Such a characterization method is common, e.g., in analog design analysis and optimization which is known as the "training" process to establish functional relationships among variables [27].

We apply SPICE simulation for the most accurate delay calculation results, while interconnect model order reduction [16] and voltage controlled current source based gate modeling [7] techniques can be applied for efficiency improvement without significant accuracy loss.

A gate/interconnect delay as a function of crosstalk aggressor alignment is shown in Fig. 2 (as well as Fig. 3 and Fig. 5 in Section IV). We observe that the effect of crosstalk aggressor alignment on gate/interconnect delay is more complex than the traditional timing window based model, i.e., crosstalk effect takes place and affects the victim net driver gate/interconnect delay when the two coupled interconnect have their timing windows overlap with each other. A timing window is defined by the earliest and the latest signal arrival times of a net. Timing window based crosstalk aggressor alignment model states that victim net driver gate/interconnect delay is a pulse function of the crosstalk aggressor alignment. Instead, we observe a more complex function, i.e., crosstalk effect increases gradually as the victim and the aggressor signal transition times are aligned to each other.

This effect has long been observed, and interconnect delay is adjusted, e.g., by table lookup with index of relative timing window [22], by closed-form expressions based on specific waveform assumption and first-order [23] or second-order Taylor expansion [6] in solving an exponential equation of interconnect delay variation.

We apply (e.g., least-mean-square) regression and approximate the victim net driver gate/interconnect delay as a piecewise quadratic function as follows (where $d_1 = d_2$ for interconnect delay).

$$D_g = \begin{cases} d_2 & x' \le t_0 \\ a_0 + a_1 x' + a_2 x'^2 & t_0 \le x' \le t_1 \\ d_0 & t_1 \le x' \le t_2 \\ b_0 + b_1 x' + b_2 x'^2 & t_2 \le x' \le t_3 \\ d_1 & t_3 \le x' \end{cases} \tag{5}$$

D. Probabilistic Symbolic Analysis

Traditional statistical timing analysis approaches compute moments (e.g., means, standard deviations, skewnesses, etc.) and correlations of signal arrival times in a design. It is critical to include correlations in these statistical timing analysis approaches to achieve meaningful, accurate estimation results. Correlations in timing variation come from (1) circuit design, e.g., signals propagated from the same fanout net are correlated, and (2) manufacturing process, e.g., signal propagation delays for two components are affected by the same global or location correlated process parameter.

Complexity arises in addressing an increasingly large degree of correlations, e.g., an n-th order covariance of $n+1$ random variables is defined as follows.

$$cov(r_0, r_1, ..., r_n) = E((r_0 - E(r_0)) \cdot (r_1 - E(r_1))...(r_n - E(r_n))) \tag{6}$$

which is needed for occurrence probability of a $n+1$-th order polynomial of random variables, for example, the occurrence probability of a quadratic polynomial of two random variables is given by the first order covariance as follows.

$$P(x_1 \cdot x_2) = P(x_1) \cdot P(x_2) + cov(x_1, x_2) \tag{7}$$

The number of correlations could be extremely large, e.g., for n random variables, $O(n^2)$ first-order

correlations, and much more higher-order correlations are needed to compute exact probabilities. Truncating higher-order correlations gives accuracy-efficiency tradeoff.

Alternative to moments and correlation computation, signal arrival times in a design can be computed symbolically, e.g., in closed form expressions of variational parameters, such that their probabilistic distributions are accessible by, e.g., Monte Carlo simulation without the need of correlation computation. Such techniques include polynomial computation [9], affine arithmetics [14], probabilistic interval analysis [20], etc., where variational delays are computed by either derivation of closed-form formulas [14], [20], or by sampling analysis and regression [9], [10], [11]. We call these methods *probabilistic symbolic analysis* approaches.

For example, in the principle of symbolic analysis, the signal arrival time distribution at the output of a driver gate or an interconnect is given by

$$y_1 = \begin{cases} x_1 + d_2 & x' \le t_0 \\ x_1 + a_0 + a_1 x' + a_2 x'^2 & t_0 \le x' \le t_1 \\ x_1 + d_0 & t_1 \le x' \le t_2 \\ x_1 + b_0 + b_1 x' + b_2 x'^2 & t_2 \le x' \le t_3 \\ x_1 + d_1 & t_3 \le x' \end{cases} \tag{8}$$

Given a symbolic representation, its statistical moments and correlations can be computed simply by Monte Carlo simulation. We derive closed form statistical signal arrival time distributions for improved efficiency over Monte Carlo simulation in the following section.

E. Signal Integrity Aware Statistical Delay Calculation

Given input arrival timing variations in closed form formulas of random variables and the functional relationship between the output and the input signal arrival times, we rewrite the signal integrity aware statistical delay calculation problem as follows.

Problem 2[Probability Density Function Propagation]
Given

1. *joint probability density function of k random variables* $\vec{x} =< x_1, ..., x_k >$, *and*
2. *a piece-wise polynomial function* $y_1 = f(\vec{x})$,

find *probability density function of* y_1.

The output y_1 stands for the signal arrival time distribution at the output of the coupled intercon-

nect system. The random variables $\vec{x}$ include variational process parameters, e.g., gate length and threshold voltage for the driver gates and interconnect widths and spacings for the load interconnects, and previous stage variations which give input signal arrival time variations. The piece-wise polynomial function combines process variation extraction and performance characterization results.

We partition the variable space of the function $y_1 = f(\vec{x})$ into regions $R_i \in \mathcal{R}$, within each region the output y_1 has a consistent polynomial representation f_{R_i}. We compute conditional probabilities for the output y_1 for each region as follows.

$$\begin{aligned} P(y_1 = \tau) &= \sum_{R_i \in \mathcal{R}} \int_{\vec{x} \in R_i} P(\vec{x} \mid y_1 = \tau) d\vec{x} \\ &= \sum_{R_i \in \mathcal{R}} \int_{\vec{x} \in R_i} P(x_1) \cdot P(x_2|x_1) ... P(x_k = f_{R_i}^{-1}(y_1 = \tau, x_1, x_2, ..., x_{k-1})) dx_1 dx_2 ... dx_{k-1} \end{aligned} \quad (9)$$

For each $y_1 = \tau$, its occurrence probability is given by the joint probability density function $P(\vec{x})$ of $\vec{x}$ to satisfy $y_1 = f(\vec{x}) = \tau$. To guarantee $y_1 = \tau$, we perform integration on $k-1$ dimensions, while the last variable x_k is given by the inverse function $x_k = f^{-1}(y_1, x_1, x_2, ..., x_{k-1})$. Such an analytical inverse function x_k is available for any order-d polynomial approximation, where $d \leq 4$.

For example, consider a piece-wise quadratic approximation (8) of an output signal arrival time of two coupled interconnects, the probability density function of the output signal arrival time is given by:

$$\begin{aligned} P(y_1) &= \int_{-\infty}^{\infty} P(x_1 = y_1 - D_g) P(D_g) dD_g \\ &= \int_{t_0}^{t_1} P(x_1 = y_1 - a_0 - a_1 x') P(x'|x_1) dx' \\ &+ \int_{t_2}^{t_3} P(x_1 = y_1 - b_0 - b_1 x') P(x'|x_1) dx' \\ &+ P(x_1 = y_1 - d_0) \int_{t_1}^{t_2} P(x'|x_1 = y_1 - d_0) dx' \\ &+ P(x_1 = y_1 - d_1)(1 - \int_{0}^{t_3} P(x'|x_1 = y_1 - d_1) dx') \\ &+ P(x_1 = y_1 - d_2) \int_{0}^{t_0} P(x'|x_1 = y_1 - d_2) dx' \end{aligned} \quad (10)$$

For the input signal arrival times in Gaussian distributions (i.e., in linear representation of Gaussian random variables), the crosstalk alignment $x' = x_2 - x_1$ is also in a Gaussian distribution.

$$P(x_1) = \frac{1}{\sqrt{2\pi}\sigma_1} e^{-\frac{(x_1 - \mu_1)^2}{2\sigma_1^2}}$$

$$\begin{aligned} P(x_2) &= \frac{1}{\sqrt{2\pi}\sigma_2} e^{-\frac{(x_2-\mu_2)^2}{2\sigma_2^2}} \\ P(x') &= P(x_2 - x_1) \\ &= \frac{1}{\sqrt{2\pi}\sigma'} e^{-\frac{(x'-\mu')^2}{2\sigma'^2}} \end{aligned} \tag{11}$$

where

$$\begin{aligned} \mu' &= \mu_2 - \mu_1 \\ \sigma'^2 &= \sigma_1^2 + \sigma_2^2 + cov(x_1, x_2) \end{aligned}$$

Note that the conditional probabilities of the input alignment x' for each input signal arrival time x_1 have different means but the same variance.

$$\begin{aligned} \mu_{x'|x_1} &= \mu_{x_2} - x_1 \\ \sigma_{x'|x_1} &= \sigma_{x'} \end{aligned}$$

Substituting the probability density functions $P(x_1)$ and $P(x' \mid x_1)$ in (11) to (10) gives

$$\begin{aligned} P(y_1) &= \frac{1}{\sqrt{2\pi}\sigma_{ya}} e^{-\frac{(y_1-\mu_{ya})^2}{2\sigma_{ya}^2}} \frac{1}{2}(F(y_1, t_1, a_0, a_1, \sigma_{ya}) - F(y_1, t_0, a_0, a_1, \sigma_{ya})) \\ &+ \frac{1}{\sqrt{2\pi}\sigma_{yb}} e^{-\frac{(y_1-\mu_{yb})^2}{2\sigma_{yb}^2}} \frac{1}{2}(F(y_1, t_3, b_0, b_1, \sigma_{yb}) - F(y_1, t_2, b_0, b_1, \sigma_{yb})) \\ &+ \frac{1}{2} P(x_1 = y_1 - d_0)(erf(\frac{t_2 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}) - erf(\frac{t_1 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'})) \\ &+ \frac{1}{2} P(x_1 = y_1 - d_1)(2 - erf(\frac{t_3 - \mu_2 + y_1 - d_1}{\sqrt{2}\sigma'})) \\ &+ \frac{1}{2} P(x_1 = y_1 - d_2)(erf(\frac{t_0 - \mu_2 + y_1 - d_2}{\sqrt{2}\sigma'}) \end{aligned} \tag{12}$$

where

$$\begin{aligned} F(y, t, k_0, k_1, \sigma_{yk}) &= erf(\frac{t\sigma_{yk}^2 - (1-k_1)(k_0 + \mu_2 - y)\sigma_1^2 + k_1(k_0 + \mu_1 - y)\sigma'^2}{\sqrt{2}\sigma'\sigma_1\sigma_{yk}}) \\ \mu_{ya} &= \mu_1 + a_0 - a_1(\mu_1 - \mu_2) \\ \sigma_{ya} &= \sqrt{(1-a_1)^2\sigma_1^2 + a_1^2\sigma'^2} \\ \mu_{yb} &= \mu_1 + b_0 - b_1(\mu_1 - \mu_2) \\ \sigma_{yb} &= \sqrt{(1-b_1)^2\sigma_1^2 + b_1^2\sigma'^2} \end{aligned}$$

From here we can (1) compute the moments of the output signal arrival time and the correlations between the output signal arrival time and the other signal arrival times, or (2) approximate the output signal arrival time in a polynomial, and proceed to the next stage in the netlist.

F. Summary

Algorithm 1 summarizes our proposed signal integrity aware statistical timing analysis method.

Algorithm 1: Signal Integrity Aware Statistical Timing Analysis

Input: Coupled interconnects in RC networks,
input signal arrival time distributions,
other process/environment variations

Output: Output signal arrival time distributions

1. Process variation extraction
2. Performance characterization
3. Probabilistic symbolic analysis
4. Signal integrity aware statistical delay calculation

III. IMPLEMENTATION

A. Runtime Analysis

Our proposed method takes $O(N)$ time for performance characterization for N crosstalk alignment samples. For each crosstalk alignment sample, we compute output signal arrival time by either SPICE simulation, or gate modeling and interconnect model order reduction based delay calculation techniques [16]. Regression takes $O(N)$ time. Statistical delay calculation for the coupled interconnect system takes constant time once the closed form formulas are present.

Given process variation extraction results, the overall runtime is dominated by performance characterization. For a linear system, e.g., an RLC coupled interconnect system, where superposition can be applied, we need performance characterization for each alignment sample for each crosstalk aggressor; while for a non-linear system, e.g., when the driver gates are considered, superposition in general cannot be applied, and we need performance characterization for each of the crosstalk alignment combination for the multiple crosstalk aggressors. The number of crosstalk alignment configurations is given by $N = O(\prod_{i=n} m_i)$ ($N = O(\sum_{i=n} m_i)$) for n crosstalk aggressors, each with m_i sampling alignments, when additivity cannot (can) be applied. For each crosstalk aggressor, the number of sampling alignments $m_i = MIN(t_3 - t_0, 6\sigma')/l$ is given by the smaller of

(1) $t_3 - t_0$ the time frame within which an aggressor signal transition makes a difference on the victim net driver gate delay, and (2) the $6\sigma'$s of the crosstalk alignment (which can be based on the input signal "timing windows"), for a given time step l between sampling crosstalk alignments. When our method is implemented in a statistical timing analyzer, the regression coefficients can be saved, such that re-calculation of gate delay requires only constant time, e.g., in an iteration of signal arrival time pdf refinement, as follows.

B. Efficiency Improvement

As we see, the runtime of our proposed signal integrity aware statistical delay calculation method is dominated by performance characterization, and increases with the number of crosstalk aggressors. Superposition can be applied to an RLC interconnect which is a linear system, however, it generally cannot be applied to driver gate delay calculation which is a nonlinear system, because the driver gate output resistance varies with load and the number of crosstalk aggressors. In certain cases, e.g., for certain long interconnects which are driven by large drivers of small output resistance, the driver gate output resistance variation is small, and superposition can be applied with acceptable inaccuracy for efficiency improvement. Filtering also helps in reducing the number of crosstalk aggressors which need to take into consideration.

Performance of a driver gate and its load interconnect is affected by a variety of factors, including (1) variational process parameters, e.g., interconnect width/thickness, transistor channel length, gate oxide thickness, and threshold voltage, (2) operation condition, e.g., temperature variation, (3) input signal transition time variation, and (4) multiple-input switching effect and power/ground supply voltage degradation which affect signal propagation delay of a gate. To combine the effects of correlated multiple variation sources, one can (1) enumerate all the conditions, e.g., all possible crosstalk alignments, (2) compute interconnect delay variation for each condition, and (3) combine the conditional probabilities, as in [2].

However, we achieve improved efficiency by (1) applying PCA to reduce the random variables to a smaller set of uncorrelated random variables, and (2) applying superposition for the contribution on performance variation of the uncorrelated random variables. Having uncorrelated random variables significantly simplifies statistical computation. Of uncorrelated random variables $\vec{x}$, the joint probability density function is given by the product of each individual random variable's probability density function $P(\vec{x}) = \prod_i P(x_i)$, and the sum of uncorrelated random variables $\vec{x}$ has

its mean and variance given by $\mu_{\sum_i x_i} = \sum_i \mu_i$ and $\sigma^2_{\sum_i x_i} = \sum_i \sigma_i^2$, respectively.

We present verification for these approaches in Section IV.

C. Multiple Iterations

Our proposed signal integrity aware statistical delay calculation is implemented in a statistical timing analyzer, which goes through an iteration of pessimism reduction and estimation refinement, as is in traditional deterministic signal integrity aware static timing analysis.

In traditional min/max-based STA, delay calculation for coupled interconnects goes through an iteration of pessimism reduction and timing window refinement. The iteration starts with the worst-case assumptions that signals could arrive at any time for each interconnect, and all neighboring interconnects have possible cross-coupling effects. Timing windows are computed to bound signal arrival times at each interconnect. If the timing windows do not overlap for two neighboring interconnects, cross-coupling effects between them need to be taken out of consideration and their delays need to be re-calculated to give updated timing windows and reduced pessimism.

In SSTA, iterations of pessimism reduction can also be applied. This is because STA proceeds in a topological order of the netlist, which guarantees that all input signal arrival times are computed before the output signal arrival times for any component in a netlist. However for physically coupled interconnects, their exact input signal arrival time distributions may not be known at the time of signal integrity aware delay calculation. Thus, a pessimistic distribution can be assumed and refined later during iteration.

IV. Experiments

Our experimental test cases include 16X inverters which drive coupled interconnect instances which are extracted from 130*nm* industry designs, or based on Berkeley Predictive Technology Model (BPTM) 100*nm* and 70*nm* technologies [4].

A. Interconnect Delay as a Function of Input Signal Alignment

We apply two signal transitions to a pair of 1000μm coupled global interconnects in 70*nm* technology given by BPTM. Fig. 3 shows the interconnect delay as a function of input signal alignment for different input signal transition times for two signals in the same direction, where interconnect delay decreases when crosstalk effect occurs. For two signals in the opposite directions, interconnect delay increases when crosstalk effect occurs.

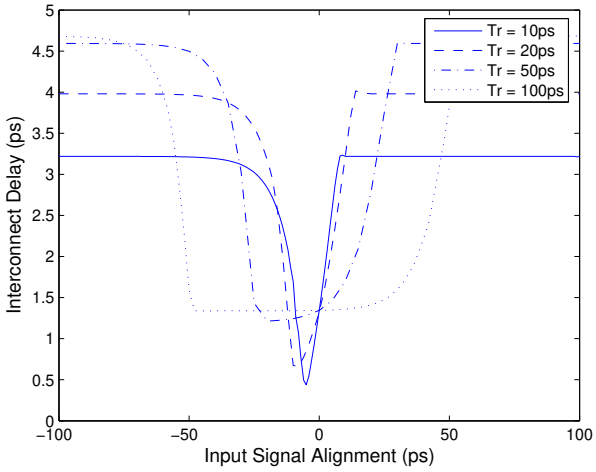

Fig. 3. Coupled interconnect delay as a function of input signal alignment for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM.

We observe that increased input signal transition time leads to increased interconnect delay. Crosstalk effect occurs when the input signal transitions overlap (i.e. from $-T_r$ to $\frac{1}{2}T_r$), which leads to reduced interconnect delay in this case with two rising signal transitions. The maximum delay variation occurs if the aggressor signal completes its transition when the victim signal reaches the 50% delay threshold (i.e. at $-\frac{1}{2}T_r$). For signals with large transition times (i.e. $\geq 50ps$ here), interconnect delay is less sensitive to signal transition time variation, either with or without crosstalk effect. It is also less sensitive to most of the possible input signal alignments when a crosstalk effect occurs, i.e., although crosstalk effect occurs over a larger range of input signal alignment with a larger signal transition time, interconnect delay is only sensitive to a certain range of input signal alignment (see the nearly identical slope of the rising and falling edges in Fig. 3).

We approximate the coupled interconnect delay as a piecewise-quadratic function of input signal alignment. Table I gives the coefficients and the variance of the quadratic fits of the interconnect delay in Fig. 3.

B. Interconnect Delay Variation due to Varied Input Signal Alignment

Based on the piecewise-quadratic approximation of interconnect delay as a function of input signal alignment, we compute interconnect delay variation due to varied input signal alignment, and compare with SPICE Monte Carlo simulation results in Fig. 4.

As we showed in Section II-E, *an interconnect delay distribution with normally distributed*

TABLE I

COEFFICIENTS AND STANDARD DEVIATIONS OF QUADRATIC FITS OF INTERCONNECT DELAY (PS) AS A FUNCTION OF INPUT SIGNAL ALIGNMENT FOR A PAIR OF $1000\mu m$ COUPLED GLOBAL INTERCONNECTS IN $70nm$ TECHNOLOGY GIVEN BY BPTM.

Tr	a_0	a_1	a_2	std. dev.	b_0	b_1	b_2	std. dev.
10	-1.26	-0.36	-7.47E-3	0.38	1.35	0.22	4.93E-3	0.10
20	-2.49	-0.41	-6.79E-3	0.55	1.34	0.13	5.61E-3	0.05
50	-4.51	-0.34	-3.10E-3	0.80	1.22	0.03	2.70E-3	0.04
100	-8.53	-0.31	-1.81E-3	1.04	1.66	-0.04	1.41E-3	0.07

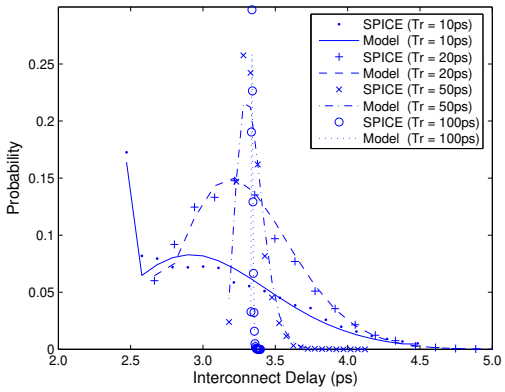

Fig. 4. Interconnect delay distributions for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM. Input signal transition time is 10, 20, 50, or $100ps$. Input signal alignment is in a normal distribution $N(0, 10ps)$.

input signal arrival times may not be a normal distribution; the accuracy of approximating an interconnect delay distribution by a normal distribution depends on the variance of the input signal alignment, e.g., the "timing windows" of the input signals. For small timing windows and large signal transition times, the input signal alignment is more likely to fall within a region of the piecewise-quadratic function (in Fig. 3) where an insignificant quadratic term is found, and the coupled interconnect delay is more likely to resemble a normal distribution. If the input signal alignment falls in more than one regions of the piecewise-quadratic function, e.g., for $T_r = 10ps$ in Fig. 4, the coupled interconnect delay distribution deviates from a normal distribution.

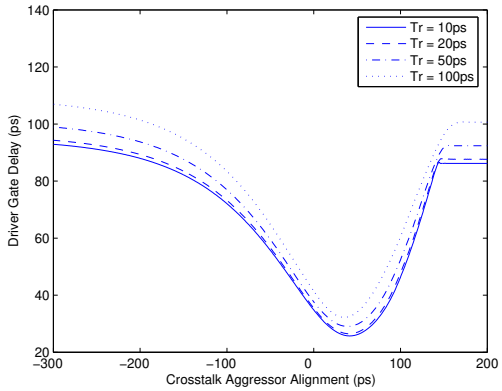

Fig. 5. Driver gate delay as a function of crosstalk alignment for a pair of 1000μm coupled global interconnects in BPTM 70nm technology.

C. Driver Gate Delay Variation due to Crosstalk Alignment

We apply two rising signals to the drivers of a pair of 1000μm coupled global interconnects in BPTM 70nm technology. Fig. 5 shows the driver gate delay variation due to crosstalk alignment with different input signal transition times.

A crosstalk aggressor signal transition in the same (opposite) direction leads to a decreased(increased) effective capacitive load for the driver of the victim net, and a victim net driver gate delay decrease (increase). Crosstalk effect takes place for a wide range of aggressor alignment, because the injected crosstalk noise takes longer time to discharge, and the driver gate delay varies with any remaining crosstalk noise charge. The victim net driver gate delay differs after a crosstalk aggressor signal transition as a result of different aggressor driver output resistance, and gives a different load interconnect configuration for the victim net driver. The signal transition times at the inputs of the victim and the aggressor net drivers do not have significant effect on the driver gate delay variation, because the signal transition times at the outputs of the driver gates do not vary much, where crosstalk effect takes place.

Therefore, we approximate the coupled interconnect delay as a piecewise-quadratic function of crosstalk alignment, and compute driver gate delay variation due to varied crosstalk alignment based on the method as is presented in Section II. Fig. 6 shows that our computed driver gate delay variations match well with the SPICE Monte Carlo simulation results.

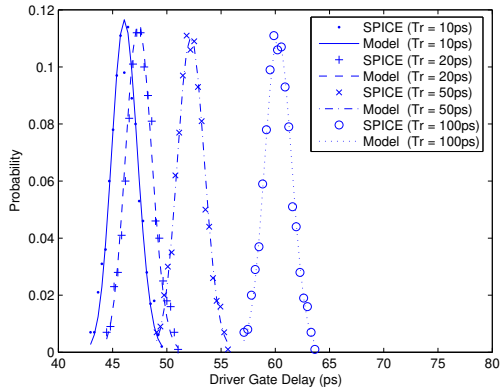

Fig. 6. Driver gate delay distributions for a pair of $1000\mu m$ coupled global interconnects in BPTM $70nm$ technology. Input signal transition time is 10, 20, 50, or $100ps$. Input signal alignment is in a normal distribution $N(0,10ps)$.

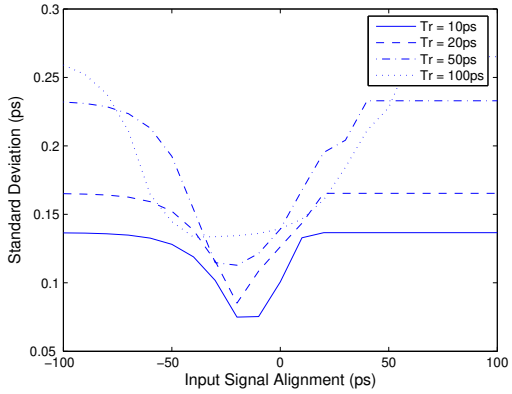

Fig. 7. Interconnect delay standard deviation due to varied wire width as a function of input signal alignment for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM. The transition times of two rising input signals are 10, 20, 50, or $100ps$. Wire width variation is in a normal distribution $N(0,0.1Width)$.

D. Interconnect Delay Variation in the Presence of Wire Width Variation and Crosstalk Alignments

We study the effect of wire width variation on coupled interconnect delay for each input signal alignment with a given signal transition time. We assume a 100% width correlation among local wire segments [19], and compute interconnect resistances and capacitances using closed form formulas [4] for normally distributed wire widths in SPICE Monte Carlo simulation. We observe that *wire width variation induced interconnect delay variance is in a pulse function of input signal alignment* in Fig. 7, which differs with multiple input switching gate delay variance that is in a ramp function [2]. For input signals which take transitions in the same (opposite) direction(s),

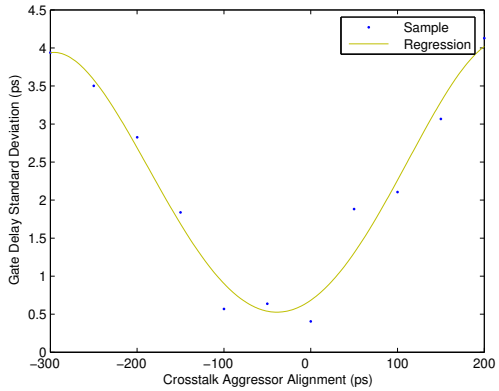

Fig. 8. Driver gate delay standard deviation due to gate length variation as a function of crosstalk alignment for a pair of $1000\mu m$ coupled global interconnects in BPTM $70nm$ technology. The transition times of two rising input signals are $100ps$. Gate length variation is in a normal distribution $N(0, 15\%)$.

interconnect delay variance due to varied wire width decreases (increases) when crosstalk effect occurs.

We separate the effects of wire width variation with input signal alignment variation on coupled interconnect delay. Table IV demonstrates that *results of our model based on superposition of the two effects match within* 1.96% *with SPICE Monte Carlo simulation results in the presence of wire width variation and input signal alignment variation.* This validates the superposition approach in the presence of independent variation sources.

We compare the impact of wire width variation in our proposed crosstalk aggressor alignment aware statistical delay calculation, and crosstalk aggressor alignment oblivious statistical delay calculation. In the latter case, we consider the worst case scenario, i.e., the maximum interconnect delay takes place when there is no crosstalk, and all coupling capacitors are grounded in our test case. Table IV shows that *crosstalk aggressor alignment oblivious statistical delay calculation results in up to* 114.65% *mismatch in mean interconnect delay, and up to* 71.26% *underestimate in standard deviation of interconnect delay in this case.*

E. Gate Delay Variation in the Presence of Process Variations and Crosstalk Alignments

We bring into account the effect of manufacturing process variations on gate delay variation, such an effect differs with different crosstalk aggressor alignments. As an example, we consider gate length (effective transistor channel length) variation, and study its effect on gate delay for

different load interconnect crosstalk aggressor alignments. We consider a gate length variation in a normal distribution which 3σ is 15% of the minimum gate length [2]. We observe that *gate length variation induced gate delay variance is in a piecewise-quadratic function of load interconnect crosstalk alignment* (Fig. 8), similar with mean gate delay variation. For input signals which take transitions in the same (opposite) direction(s), gate delay variance due to varied wire width decreases (increases) when crosstalk effect occurs.

We separate the effects of gate length variation with load interconnect crosstalk alignment variation on driver gate delay. Table II demonstrates that *gate delay standard deviation obtained by superposition of the two effects match within* 2.20% *with SPICE Monte Carlo simulation results in the presence of gate length and crosstalk alignment variations.* This validates the superposition approach in the presence of independent variation sources.

Traditional timing window based crosstalk analysis does not fit into statistical timing analysis. Approximating a signal arrival time pdf by a timing window could lead to significant inaccuracy, since crosstalk effect grows gradually with aggressor alignment as Fig. 2 shows, instead of turning into crosstalk mode when two timing windows start to overlap.

We evaluate statistical driver gate delay calculation without statistical crosstalk consideration, i.e., assuming a unit Miller factor by grounding all coupling capacitors. Compare the impact of gate length variation on gate delay. Table II shows that *without statistical crosstalk consideration assuming a unit Miller factor results in up to* 159.4% *mismatch in mean driver gate delay, and up to* 147.4% *underestimate in standard deviation of driver gate delay in this case.*

F. Interconnect Output Signal Arrival Time Variation

We compare our computed output signal arrival time distribution with SPICE Monte Carlo simulation results for a typical BPTM global interconnect structure in Fig. 9.

We apply our method to a variety of input signal transition times and input signal arrival time deviations from 50, 100, to 200ps. To cover different technology nodes, our test cases include 16X inverters which drive (I) a pair of 1000μm coupled global interconnects in 70nm technology given by BPTM, and (II) a pair of coupled interconnects which are extracted from a 130nm industry design with 451 resistors and 1637 ground and coupling capacitors. We take a 2ps time step between two sampling crosstalk alignments. and compare with 1000 SPICE Monte Carlo simulation runs. The results are shown in Table V.

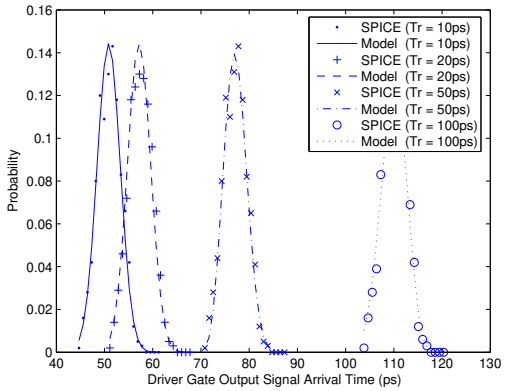

Fig. 9. Output signal arrival time distribution for a pair of $1000\mu m$ coupled global interconnect in $70nm$ technology given by BPTM with the input signal arrival times in normal distributions $N(0,10ps)$.

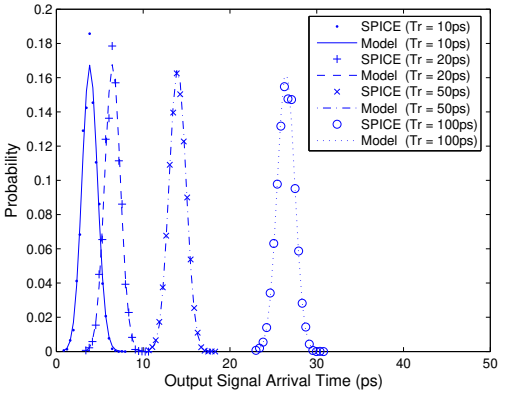

Fig. 10. Output signal arrival time distribution for a pair of $1000\mu m$ coupled global interconnect in $70nm$ technology given by BPTM with the input signal arrival times in normal distributions $N(0,6ps)$.

We observe that increased input signal arrival time deviations lead to increased driver gate delay and output signal arrival time deviations; while mean driver gate delay decreases with increased input signal transition time. *Over a variety of technology nodes, input signal transition times and arrival time deviations, our method gives the means and the standard deviations of gate output signal arrival times within* 2.57% *and* 3.86% *of SPICE Monte Carlo simulation results, respectively.*

G. Gate Output Signal Arrival Time Variation

We compare our computed output signal arrival time distribution with SPICE Monte Carlo simulation results for a typical BPTM global interconnect structure in Fig. 10.

We apply our model to a variety of input signal transition times and input signal arrival time

deviations from 50, 100, to 200ps. To cover different technology nodes, our test cases include (I) a pair of 1000μm coupled global interconnects in 70nm technology given by BPTM, and (II) a pair of coupled interconnects which are extracted from a 130nm industry design with 451 resistors and 1637 ground and coupling capacitors. We take a 2ps time step between two sampling input signal alignments, so that the number of delay calculation for different input signal alignment $N = MIN(1.5T_r, 6\sigma')/2$. We compare with 1000 SPICE Monte Carlo simulation runs. The results are shown in Table III.

We observe that increased input signal arrival time deviations lead to increased interconnect delay and output signal arrival time deviations; mean interconnect delay decreases with increased input signal transition time, because more input signal alignments bring crosstalk effect which reduces interconnect delay. *Over a variety of technology nodes, input signal transition times and arrival time deviations, our model gives the means and the standard deviations of output signal arrival times within* 2.09% *and* 3.38% *of SPICE Monte Carlo simulation results, respectively.*

V. Conclusion

We propose SSTA-SI: signal integrity effect aware statistical static timing analysis in this paper. We study interconnect and gate delay variations due to load interconnect crosstalk aggressor alignment, i.e., signal arrival time difference at a coupled neighboring interconnect. This is a significant source of variation, which must be taken into consideration in statistical timing analysis. We present closed-form formulas for probabilistic gate delay calculation based on deterministic delay calculation for sampling crosstalk alignment configurations. After sampling delay calculation, probabilistic delay calculation and updating take constant time. Our experimental results based on SPICE Monte Carlo simulation verifies our method, which achieves within 1.28% (3.38%) mismatch for interconnect output signal arrival time means (standard variations), and within 2.57% (3.86%) mismatch for gate output signal arrival time means (standard variations), while lack of statistical crosstalk alignment consideration could lead to up to 114.65% (71.26%) differences in interconnect delay means (standard deviations), and up to 159.4% (147.4%) differences in gate delay means (standard variations), respectively.

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TABLE II

THE MEANS (μ) AND THE STANDARD DEVIATIONS (σ) OF GATE DELAY (ps) (1) FOR FIXED GATE LENGTH AND INPUT SIGNAL ARRIVAL TIME, (2) WITH GATE LENGTH VARIATION, (3) WITH CROSSTALK ALIGNMENT VARIATION, (4) WITH BOTH GATE LENGTH AND CROSSTALK ALIGNMENT VARIATIONS, (5) WITH GATE LENGTH VARIATION AND GROUNDED COUPLING CAPACITORS (ASSUMING A UNIT MILLER FACTOR), ALL BY SPICE MONTE CARLO SIMULATION, AND (6) OUR METHOD'S ESTIMATES WITH BOTH GATE LENGTH AND CROSSTALK ALIGNMENT VARIATIONS. INPUT SIGNAL TRANSITION TIMES T_r ARE $10ps, 20ps$, OR $50ps$. MEAN CROSSTALK ALIGNMENT $\mu' = -10ps, 0ps$, OR $10ps$.

		(1)	(2)	(3)	(4)	(5)	(5) - (4)	(6)	(6) - (4)
$T_r = 10$		none	length	skew	both	$f_{miller} = 1$	%diff	our	%diff
$\mu' = -10$	μ	50.14	50.17	50.12	50.19	120.23	139.5	50.15	-0.08
	σ	-	2.11	1.31	2.44	5.81	138.3	2.48	1.78
$\mu' = 0$	μ	46.30	46.32	46.27	46.34	120.21	159.4	46.29	-0.11
	σ	-	2.11	1.25	2.41	5.81	141.2	2.45	1.76
$\mu' = 10$	μ	42.66	42.67	42.65	42.72	120.23	181.4	42.66	-0.14
	σ	-	2.10	1.15	2.35	5.81	147.4	2.39	1.88
$T_r = 20$		none	length	skew	both	$f_{miller} = 1$	%diff	our	%diff
$\mu' = -10$	μ	51.65	51.66	51.60	51.67	121.68	135.5	51.61	-0.12
	σ	-	2.11	1.31	2.44	5.81	138.3	2.48	1.78
$\mu' = 0$	μ	47.74	47.75	47.71	47.78	121.72	154.7	47.72	-0.13
	σ	-	2.11	1.25	2.41	5.81	141.3	2.45	1.76
$\mu' = 10$	μ	44.14	44.16	44.11	44.18	121.72	175.5	44.13	-0.11
	σ	-	2.10	1.15	2.35	5.81	147.4	2.39	1.88
$T_r = 50$		none	length	skew	both	$f_{miller} = 1$	%diff	our	%diff
$\mu' = -10$	μ	56.24	56.26	56.20	56.27	126.29	124.4	56.22	-0.09
	σ	-	2.11	1.31	2.43	5.81	139.2	2.48	2.20
$\mu' = 0$	μ	52.40	52.41	52.36	52.42	126.30	140.9	52.37	-0.09
	σ	-	2.11	1.25	2.40	5.81	142.2	2.45	2.18
$\mu' = 10$	μ	48.75	48.76	48.71	48.78	126.28	158.9	48.72	-0.12
	σ	-	2.10	1.17	2.36	5.81	146.3	2.40	1.86

TABLE III

THE MEANS (μ) AND THE STANDARD DEVIATIONS (σ) OF GATE DELAY AND OUTPUT SIGNAL ARRIVAL TIMES (ps) OF AN $16X$ INVERTER WHICH DRIVES (I) A $1000\mu m$ INTERCONNECT OF TYPICAL $70nm$ BPTM GLOBAL STRUCTURE, OR (II) A COUPLED INTERCONNECT EXTRACTED FROM A $130nm$ INDUSTRY DESIGN WITH 451 RESISTORS AND 1637 GROUND AND COUPLING CAPACITORS. INPUT SIGNAL ARRIVAL TIME DEVIATION 3σ AND TRANSITION TIME T_r ARE $50ps$, $100ps$, OR $200ps$.

input		delay				output					
3σ	T_r	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
$70nm$		SPICE		Model		SPICE		Model		%diff	
50	50	52.83	8.86	52.74	8.42	78.6	12.19	77.3	12.66	-1.65	3.86
50	100	60.66	8.71	60.52	8.37	111.4	12.21	110.8	12.64	-0.54	3.52
50	200	74.63	8.75	73.81	8.86	175.4	12.18	174.9	12.36	-0.29	1.48
100	50	54.31	16.31	55.12	16.16	80.8	25.04	79.6	24.37	-1.49	-2.68
100	100	61.38	16.03	61.85	15.87	112.9	24.97	113.7	24.43	0.71	-2.16
100	200	74.19	16.66	74.04	16.84	175.7	24.64	178.3	23.98	1.48	-2.68
200	50	57.06	22.84	56.64	22.75	85.1	55.49	84.1	54.72	-1.18	-1.39
200	100	63.39	23.39	63.17	23.51	116.5	54.86	117.9	55.91	1.20	1.91
200	200	74.3	23.19	74.13	23.07	177.4	52.92	173.8	53.83	-2.03	1.72
$130nm$		SPICE		Model		SPICE		Model		%diff	
50	50	169.67	0.81	168.84	0.8	195.4	16.41	193.6	16.24	-0.92	-1.03
50	100	178.77	0.81	177.23	0.81	229.5	16.41	226.8	16.32	-1.17	-0.55
50	200	197.74	0.79	198.45	0.8	298.5	16.42	295.4	16.29	-1.04	-0.79
100	50	169.98	1.49	170.71	1.48	196.5	32.98	192.9	32.82	-1.83	-0.49
100	100	179.07	1.5	178.46	1.51	230.6	32.97	232.7	32.73	0.91	-0.73
100	200	198.01	1.5	197.68	1.52	299.5	32.96	291.8	33.49	-2.57	1.61
200	50	170.95	2.55	169.42	2.54	199	66.57	196.8	67.01	-1.11	0.66
200	100	180.01	2.56	178.92	2.52	233.1	66.53	231.2	66.07	-0.81	-0.69
200	200	198.87	2.52	198.73	2.51	301.9	66.49	297.8	65.87	-1.36	-0.93

TABLE IV

THE MEANS (μ) AND THE STANDARD DEVIATIONS (σ) OF INTERCONNECT DELAY (ps) (1) FOR FIXED WIRE WIDTH AND INPUT SIGNAL ARRIVAL TIME, (2) WITH WIRE WIDTH VARIATION, (3) WITH INPUT SIGNAL ALIGNMENT VARIATION, (4) WITH BOTH WIRE WIDTH AND INPUT SIGNAL ALIGNMENT VARIATIONS, (5) WITH WIRE WIDTH VARIATION AND GROUNDED COUPLING CAPACITORS (IN CROSSTALK AGGRESSOR ALIGNMENT OBLIVIOUS DELAY CALCULATION), ALL BY SPICE MONTE CARLO SIMULATION, AND (6) OUR MODEL'S ESTIMATES WITH BOTH WIRE WIDTH AND INPUT SIGNAL ALIGNMENT VARIATIONS. INPUT SIGNAL TRANSITION TIMES T_r ARE $10ps, 20ps$, OR $50ps$. MEAN INPUT SIGNAL ALIGNMENT $\mu' = -10ps, 0ps$, OR $10ps$.

		(1)	(2)	(3)	(4)	(5)	(5) - (4)	(6)	(6) - (4)
$T_r = 10ps$		none	width	skew	both	w/o xtalk	%diff	model	%diff
$\mu' = -10$	μ	3.08	3.08	3.12	3.13	5.65	80.51	3.12	-0.64
	σ	-	0.08	0.37	0.38	0.17	-55.94	0.38	-0.10
$\mu' = 0$	μ	3.27	3.27	3.37	3.38	5.63	66.57	3.38	0.00
	σ	-	0.10	0.56	0.58	0.17	-71.26	0.57	-1.96
$\mu' = 10$	μ	5.00	5.00	4.85	4.85	5.64	16.29	4.85	-0.00
	σ	-	0.13	0.28	0.31	0.17	-47.01	0.31	-0.23
$T_r = 20ps$		none	width	skew	both	w/o xtalk	%diff	model	%diff
$\mu' = -10$	μ	2.92	2.92	3.12	3.14	6.52	114.65	3.12	-0.96
	σ	-	0.11	0.35	0.37	0.19	-47.51	0.37	1.29
$\mu' = 0$	μ	3.61	3.61	3.66	3.67	6.53	77.93	3.66	-0.00
	σ	-	0.13	0.45	0.47	0.19	-58.62	0.47	-0.99
$\mu' = 10$	μ	5.22	5.23	5.23	5.22	6.52	24.90	5.22	0.00
	σ	-	0.14	0.52	0.55	0.19	-64.96	0.54	-1.48
$T_r = 50ps$		none	width	skew	both	w/o xtalk	%diff	model	%diff
$\mu' = -10$	μ	3.44	3.44	3.45	3.46	7.19	108.38	3.45	-0.29
	σ	-	0.12	0.05	0.13	0.13	1.97	0.13	0.77
$\mu' = 0$	μ	3.68	3.68	3.70	3.71	7.19	93.80	3.70	-0.27
	σ	-	0.14	0.12	0.19	0.13	-27.91	0.18	-0.13
$\mu' = 10$	μ	4.22	4.22	4.26	4.27	7.18	68.15	4.27	-0.23
	σ	-	0.17	0.28	0.32	0.13	-58.70	0.32	-0.27

TABLE V

THE MEANS (μ) AND THE STANDARD DEVIATIONS (σ) OF INTERCONNECT DELAYS AND OUTPUT SIGNAL ARRIVAL TIMES (ps) FOR (I) A $1000\mu m$ INTERCONNECT OF TYPICAL $70nm$ BPTM GLOBAL STRUCTURE AND (II) A COUPLED INTERCONNECT EXTRACTED FROM A $130nm$ INDUSTRY DESIGN WITH 451 RESISTORS AND 1637 GROUND AND COUPLING CAPACITORS. INPUT SIGNAL ARRIVAL TIME DEVIATION 3σ AND TRANSITION TIME T_r ARE $50ps$, $100ps$, OR $200ps$.

input		delay				output					
3σ	$T_r(ps)$	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
(I) $70nm$		SPICE		Model		SPICE		Model		%diff	
50	50	3.83	0.85	3.82	0.83	29.44	16.25	29.67	16.65	0.78	2.46
50	100	3.39	0.16	3.41	0.12	53.77	16.33	53.70	16.65	-0.13	1.96
50	200	3.34	0.00	3.34	0.00	103.57	16.49	103.48	16.52	-0.09	0.18
100	50	4.59	1.23	4.59	1.19	30.44	32.87	30.97	33.48	1.74	1.86
100	100	3.82	0.92	3.84	0.83	54.75	32.85	55.58	33.96	1.52	3.38
100	200	3.35	0.07	3.38	0.04	103.94	32.91	104.23	33.63	0.28	2.19
200	50	5.30	1.18	5.25	1.14	31.43	65.97	31.69	66.17	0.83	0.30
200	100	4.70	1.34	4.64	1.25	56.04	65.91	56.91	66.58	1.55	1.02
200	200	3.78	0.96	3.78	0.82	105.18	65.90	106.30	66.99	1.06	1.65
(II) $130nm$		SPICE		Model		SPICE		Model		%diff	
50	50	4.29	0.16	4.31	0.16	29.53	16.40	29.41	16.52	-0.41	0.73
50	100	4.29	0.16	4.30	0.15	54.52	16.39	53.38	16.06	-2.09	-0.05
50	200	4.13	0.08	4.17	0.09	104.39	16.43	104.29	16.41	-0.10	-0.12
100	50	4.33	0.17	4.34	0.17	29.81	32.94	29.66	33.03	-0.50	0.27
100	100	4.30	0.18	4.30	0.17	54.76	32.89	54.12	32.95	-1.17	0.18
100	200	4.19	0.18	4.21	0.14	104.68	32.89	104.40	32.88	-0.27	-0.03
200	50	4.39	0.16	4.42	0.14	30.33	65.96	29.81	65.94	-1.71	-0.03
200	100	4.33	0.18	4.31	0.17	55.27	65.93	54.64	65.97	0.06	0.06
200	200	4.25	0.18	4.25	0.16	105.18	65.89	104.89	66.12	-0.28	0.35