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Modeling, Fabrication, and Analysis of Vertical Conduction Gallium Nitride Fin MOSFET

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy

in

Electrical and Computer Engineering

by

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September 2017

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August 2017

Modeling, Design, and Analysis of

Vertical Conduction Gallium Nitride Fin MOSFET

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by

Maher Bishara Tahhan

DEDICATION

This dissertation is dedicated to my parents, Bishara and Wafaa Tahhan,

and my sister, Manal Tahhan.

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There are many people who I need to thank for aiding me on my journey to get to where I am as I write this. Most prominently, I thank Professor Umesh Mishra for taking me as his student, and giving me the option to work on this project. I also thank him for the support he's given me and others in his group. Outside of research, he also taught me how to understand the physics of electronic devices, which has led me to modeling transistors for the project as well as a few side projects related to simulation, growing my interest in computation and theory. In addition, I thank Stacia Keller for all the work she puts in to support all the members of the group, even those who don't grow crystals. She has been there when Umesh was not available. I have enjoyed the meetings with her, and her insights into materials have been extremely helpful. She has also helped keep the group working together by being another advisor to us.

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"Self-aligned source-first process for vertical conduction GaN fin MOSFETs" *International Conference on Nitride Semiconductors.* July 2017

ABSTRACT

Modeling, Fabrication, and Analysis of

Vertical Conduction Gallium Nitride Fin MOSFET

by

Maher Bishara Tahhan

Gallium Nitride has seen much interest in the field of electronics due to its large bandgap and high mobility. In the field of power electronics, this combination leads to a low on-resistance for a given breakdown voltage. To take full advantage of this, vertical conduction transistors in GaN can give high breakdown voltages independent of chip area, leading to transistors with nominally low on resistance with high breakdown at a low cost.

Acknowledging this, a vertical transistor design is presented with a small footprint area. This design utilizes a fin structure as a double gated insulated MESFET with electrons flowing from the top of the fin downward. The transistor's characteristics and design is initially explored via simulation and modelling. In this modelling, it is found that the narrow dimension of the fin must be sub-micron to allow for the device to be turned off with no leakage current and have a positive threshold voltage.

Several process modules are developed and integrated to fabricate the device. A smooth vertical etch leaving low damage to the surfaces is demonstrated and characterized, preventing micromasking during the GaN dry etch. Methods of removing damage from the dry etch are tested, including regrowth and wet etching. Several hard masks were developed to be used in

conjunction with this GaN etch for various requirements of the process, such as material constraints and self-aligning a metal contact. Multiple techniques are tested to deposit and pattern the gate oxide and metal to ensure good contact with the channel without causing unwanted shorts.

To achieve small fin dimensions, a self-aligned transistor process flow is presented allowing for smaller critical dimensions at increased fabrication tolerances by avoiding the use of lithographic steps that require alignments to very high accuracy. In the case of the device design presented, the fins are lithographically defined at the limit of i-line stepper system. From this single lithography, the sources are formed, fins are etched, and the gate insulator and metal are deposited.

The first functional fabricated devices are presented, but exhibit a few differences from the model. A threshold voltage of -6 V, was measured, with an I_D of 5 kA/cm^2 at 3 V, and R_{on} of 0.6 mΩ/cm^2. The current is limited by the Schottky nature of the top contacts and show a turn-on voltage as a result. These measurements are comparable to recently published GaN fin MOSFET data, whose devices were defined by e-beam lithography. This dissertation work sought to show that a vertical conduction fin MOSFET can be fabricated on GaN. Furthermore, it aimed to provide a self-aligned process that does not require e-beam lithography. With further development, such devices can be designed to hold large voltages while maintaining a small footprint.

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Chapter 1: Introduction

Power electronics has been a critical field of research for the automotive industry, even more so in recent years due to the increased number of electric motor driven cars, such as hybrids and fully electric vehicles. As many manufacturers begin to manufacture full electric vehicles, the inefficiencies and cost of the power conversion circuits become a more important issue to tackle.

In the computing industry, large data centers and supercomputers use massive amounts of power to run. As the number of these centers increases, research into reducing the inefficiencies of power delivery will become important. These two industries are not the only ones to be able to benefit from reducing power losses due to conversion, and improving power conversion and delivery will reduce the overall energy requirements of any system.

A fundamental power conversion system is the power supply, which delivers the available input power at the voltage necessary for the load. Linear power supplies will typically apply the excess voltage across a resistive element. This causes large amounts of the input power to be dissipated as waste heat through the device. This in turn requires large heat sinks to continue operating properly. Switching power supplies, on the other hand, use switching transistors and a controller to deliver almost all the input power at the necessary voltage. Other than power losses in the controller, any power losses come from parasitic resistances in the circuit or losses from the transistor.

1.1 Switching Power Supply Operation

Switching power supplies are typically categorized by their circuit topology. Two of the most common are the buck and boost topologies. Buck power supplies take a DC input voltage

and reduce it for the load, whereas boost power supplies increase the voltage from the input to the output. Both use an inductor to store energy and release it to the load. To understand where power losses can occur, one needs to understand how the circuit works, so we will describe the operation of a buck converter. The operation of most hard switched power supply topologies are similar, and the important effects the transistor characteristics have on the efficiency are therefore similar.

1.1.1 Buck Converter Operation

Figure 1.1 shows the circuit for a buck converter. On the left is the input voltage, V_{in}, typically comes from a rectified AC source or another DC source. Two transistors are used in the topology though the bottom transistor, known as the low-side switch, can be replaced with a diode, though this results in comparatively poor efficiency. With two controlled switched transistors, one achieves synchronous operation. On the right is the load or output voltage, V_{out}. A controller will apply the switched biases to the gates of the transistors. This controller may receive input from V_{out} to compare to a reference voltage and adjust the duty cycles of the switched phases to compensate.

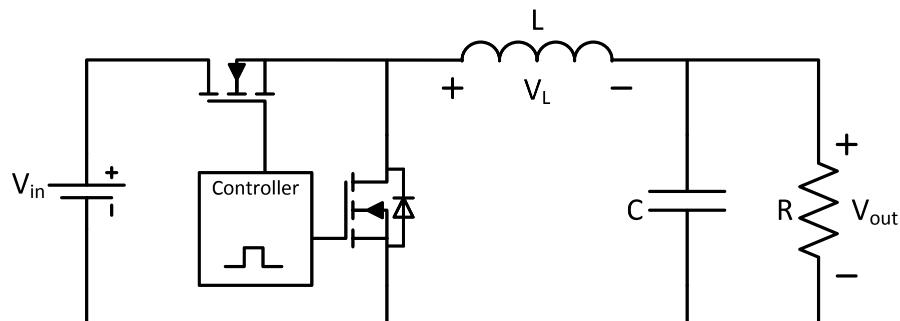


Figure 1.1 Buck converter circuit

In phase one of operation, the transistor at the top of the diagram, or the high-side switch, is closed, while the low-side switch is left open. This is illustrated in Figure 1.2. The low-side

switch holds the total input voltage across it, while all the current flows through the inductor. This charges the inductor with energy related by 1.1. The value of current that the inductor reaches is dependent on the length of time spent in this phase since the derivative of the current is directly proportional to the inductor voltage, as stated in 1.2. The voltage across the inductor is equal to V_{in}–V_{out} during phase one. 1.3 gives the change in inductor current in phase one with t_1 as the time spent in phase one.

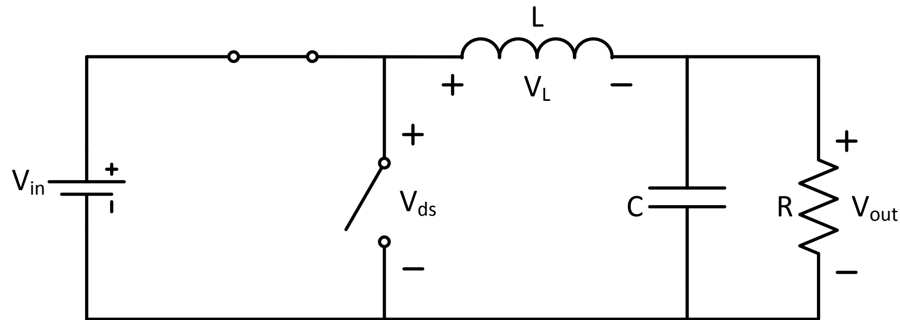


Figure 1.2 Phase one of a buck converter

$$E = \frac{1}{2} L \cdot I^2 \qquad 1.1$$

$$\frac{d}{dt} I = \frac{1}{L} V_L \qquad 1.2$$

$$\Delta I_{L1} = \frac{V_{in} - V_{out}}{L} \cdot t_1 \qquad 1.3$$

Phase two of operation reverses the states of the two switches, so that the input voltage is disconnected from the circuit, and the left side of the inductor, as shown in Figure 1.3, is connected to the common voltage. The inductor releases its energy and its current decreases at a rate determined by V_{out}, resulting in a change of current described by 1.4, with T as the period of the operating cycle. Figure 1.4 shows the output current and voltage during operation. The two phases operate while maintaining a constant output voltage, and when phase two

completes, the inductor current returns to the starting current at phase one. Setting the total change in current over one cycle to zero, the output voltage relation can be derived, resulting in 1.5, where *D* is the duty cycle.

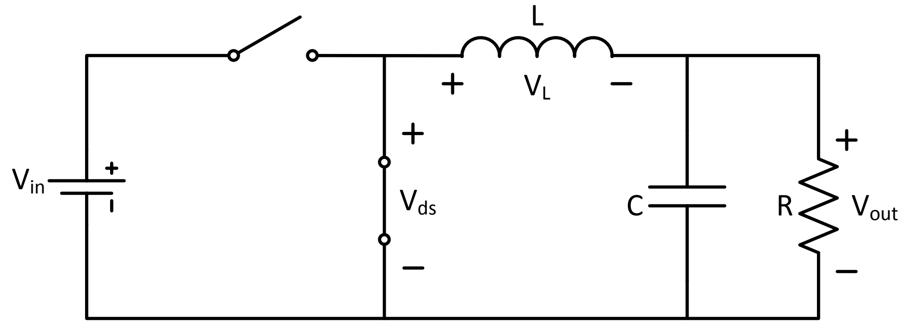


Figure 1.3 Phase two of a buck converter

$$\Delta I_{L2} = \frac{-V_{out}}{L} \cdot \left(T - t_1\right) = -\Delta I_{L1} \tag{1.4}$$

$$\frac{V_{out}}{V_{in}} = \frac{t_1}{T} = D \tag{1.5}$$

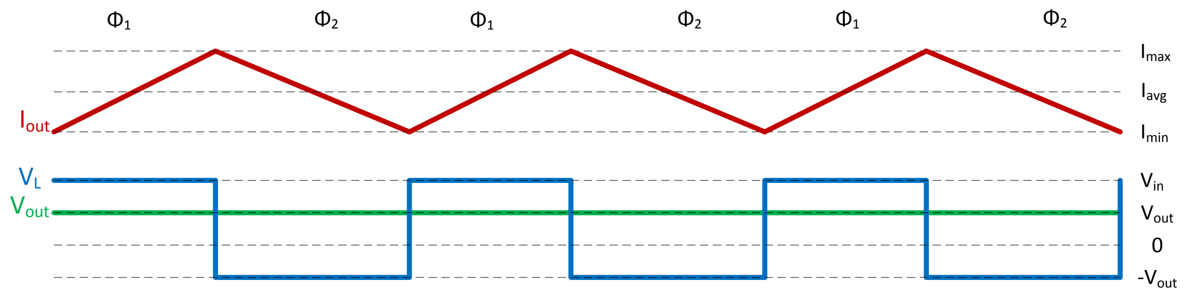


Figure 1.4: Output voltage and current with respect to time in a buck converter

1.1.2 Buck Converter Losses

As all the power in the ideal example described above is transferred from the input to the load, there are no losses inherent in the design. Losses in the circuit can come from parasitics of the components and the connections, as well as the transistor nature of the switches. Looking

at the transistor as the primary source of inefficiency, four significant sources of power dissipation can be identified.

As the transistor has a finite resistance in both the on and off states, the conduction losses can be expressed as the sum of the power dissipated in both phases of operation. 1.6 gives an expression with respect to the voltages and currents and on resistance, R_{on}, along with the duty cycle. In addition to the steady state conduction losses, power is also dissipated during switching while the voltage and current have yet to stabilize. If one assumes linear changes in current and voltage, the switching losses can be estimated by the expression in 1.7, where t_r and t_f are the rise and fall times respectively, and f_s, is the switching frequency. To reduce these two sources of power dissipation from the transistor, the R_{on}, off state current, and rise and fall times should be reduced. Figure 1.4 shows the voltages, current, and power dissipation across the low-side transistor in each of the phases.

$$P_{cond} = R_{on} \cdot I_{out}^{2} \cdot D + I_{off} \cdot V_{in} \cdot (1 - D) \qquad 1.6$$

$$P_{sw} = \frac{I_{out} \cdot V_{in}}{2} \cdot \left(t_r + t_f\right) \cdot f_s \qquad 1.7$$

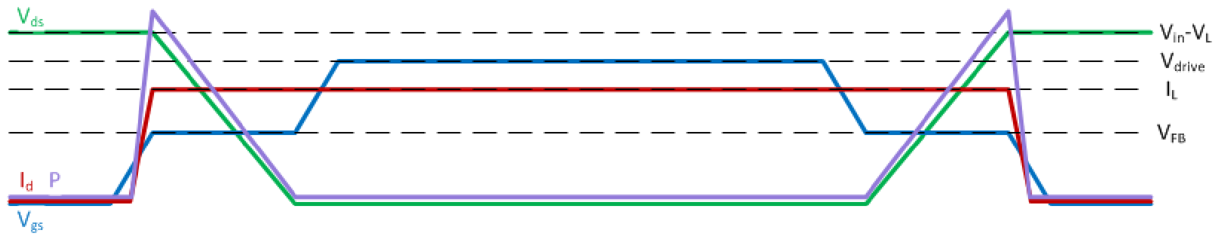


Figure 1.5: Voltage, current, and power dissipation from phase one to phase two and back

To turn on the transistor, charge accumulates at the gate, which is imaged on the channel, providing free carriers to carry the current. This results in a displacement gate current as the

transistor switches, and the associated power loss is expressed in 1.8. To reduce this power loss, either the gate charge to turn on, or threshold voltage can be decreased.

$$P_{Qg} = Q_g \cdot V_{gs} \cdot f_s \qquad 1.8$$

For a typical silicon power transistors, there is an intrinsic body diode across the source to drain, which is depicted in Figure 1.1 for the low-side switch. When switching from phase two to phase one, the inductor continues to pull current, while the diode on the low-side switch must deplete charge to hold the input voltage. [1] The total charge depleted is called the reverse recovery charge, or Q_{rr}, as in 1.9. To improve on this source of power dissipation, the diode of the transistor needs to be modified or eliminated, such that the reverse recovery charge is reduced or eliminated.

$$P_{rr} = Q_{rr} \cdot V_{in} \cdot f_s \qquad 1.9$$

Even though these transistor losses are derived from an application in a buck converter, transistors in most topologies will dissipate power in the same manner. Some topologies and controllers are designed to reduce or eliminate sources of loss. For instance, zero voltage switching, ZVS, sets the voltage to zero during the switching between phases, reducing one side of the switching loss to nearly zero as well as reduce the reverse recovery charge. However, many of these topologies fail or degrade in performance, or require large or expensive components, for high voltages, and improving the switching transistors becomes the best way to improve the efficiency.

1.2 Semiconductors for High Voltage Switching

Transistors used in high voltage power converters can vary significantly depending on the applications requirements. For many, a silicon insulated gate bipolar transistor (IGBT) is

sufficient. These IGBTs however, have several downsides, including a significant leakage current when turned off, as well as a slow response times. To improve on some of these characteristics, silicon power MOSFETs were developed which improve upon some of the poor characteristics, however, much of the inefficiencies remain significant.

Looking towards which new materials to use for improving power transistors, some important metrics need to be derived and understood. Most significantly is the specific on-resistance. This relates the on-resistance to breakdown voltage, and depends on mobility, dielectric constant, and critical field. Lower on-resistances improve the maximum power density, as well as switching speeds. To derive the relationship, we start with the depletion width, W_d, at breakdown as shown in 1.10, where V_d is the breakdown voltage, ε is the dielectric constant, q is the unit charge of an electron, and N is the doping density. The breakdown electric field, E_{crit}, is related to the breakdown voltage by 1.11.

$$V_d = \frac{q \cdot N \cdot W_d^{2}}{\varepsilon} \quad (1.10)$$

$$V_d = W_d \cdot E_{crit} \quad (1.11)$$

Combining the two, we get the following:

$$W_d = \frac{E_{crit} \cdot \varepsilon}{q \cdot N} \quad (1.12)$$

The resistivity, ρ, of the semiconductor is related by 1.13, where μ is the carrier mobility. The on resistance is the by the product of depletion width and resistivity as in 1.14.

$$\rho = \frac{1}{q \cdot \mu \cdot N} \quad (1.13)$$

$$R_{on} = W_d \cdot \rho \qquad 1.14$$

Combining 1.10 through 1.14, we get a final expression relating on resistance to breakdown voltage with only material properties.

$$R_{on} = \frac{W_d}{q \cdot \mu \cdot N} = \frac{W_d^2}{\mu \cdot E_{crit} \cdot \varepsilon} = \frac{V_d^2}{\mu \cdot E_{crit}^3 \cdot \varepsilon} \qquad 1.15$$

The power density can also be found from this expression, and is shown in 1.16.

$$P = \frac{V_d^2}{R_{on}} = \mu \cdot E_{crit}^3 \cdot \varepsilon \qquad 1.16$$

For transistors that use a drift region to hold the majority of the voltage, the specific on resistance determines a maximum breakdown voltage achievable for the material. Table 1.1 shows several semiconductors and their calculated maximum power density. Figure 1.6 plots the on-resistance to breakdown relationship for the various semiconductors in the table.

Material	**ε_r**	**μ** $cm^2/V \cdot s$	**E_{crit}** V/cm	**V_d^2/R_{on}** W/cm^2
Ge	16.2	3900	$1.0 \cdot 10^5$	$5.6 \cdot 10^6$
Si	11.7	1500	$3.0 \cdot 10^5$	$4.2 \cdot 10^7$
GaAs	12.9	8500	$4.0 \cdot 10^5$	$6.2 \cdot 10^8$
4H-SiC	9.7	1000	$2.5 \cdot 10^6$	$1.3 \cdot 10^{10}$
GaN	8.9	1200	$3.3 \cdot 10^6$	$3.4 \cdot 10^{10}$
Ga_2O_3	10	300	$8.0 \cdot 10^6$	$1.4 \cdot 10^{11}$
Diamond	5.7	1800	$1.0 \cdot 10^7$	$9.1 \cdot 10^{11}$

Table 1.1 Material properties and power density limits for standard drift regions of semiconductors

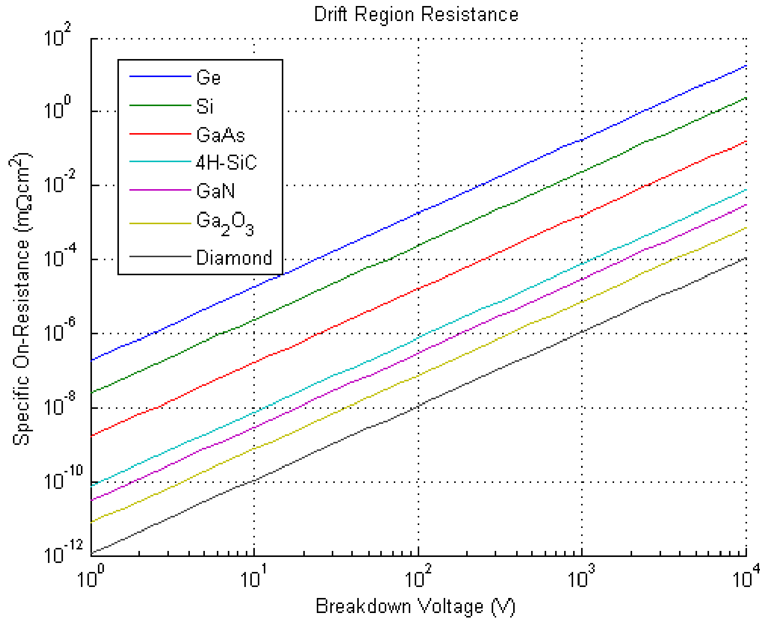


Figure 1.6 Standard limits of R_{on} and V_{BD} for various semiconductors

GaN should give a large improvement in power density over Si, and some improvement over SiC. Of those listed in the table, GaN has the best on-resistance of the developed materials. Ga_2O_3 and diamond are still in their early stages of research, and will take several years before they can compete with GaN and SiC.

1.3 Power Transistor Designs

Many types of structures are used for power transistors, and silicon is still the most commonly used material for power devices. With respect to high voltage, lateral Si MOSFETs are no longer practical, and vertical designs are used to be able to hold the high voltage without having an excessive die size. Alternately, other materials are used to achieve the same. A few vertical power transistor designs are currently manufactured, as well as several in various stages of development.

1.3.1 High Voltage Transistors in the Market

To hold a large voltage, vertical transistors utilize thick drift regions which will hold the potential drop. For a power MOSFET, a channel at the surface is inverted by the gate to allow current to pass through. Once it enters the drift region, the electric field from the voltage at the drain causes the electrons to drift down. To hold a greater voltage, the drift region thickness is increased, which in turn increases R_{on}. However, since the voltage is held across a depleted drift region, if the depletion thickness is too small for the voltage applied, the field may exceed breakdown at a specific voltage, dependent on the doping. This limit is can be calculated from 1.12. A thicker drift region will not improve the breakdown beyond this point, and only increase the R_{on} of the transistor.

To improve upon the breakdown, an IGBT, or insulated gate bipolar transistor, replaces the n+ drain with a p+ collector. As a p-n junction will provide a depletion region, it can hold a greater potential. This comes at the cost of a turn on voltage to exceed the built-in barrier of the diode, as well as an increased on-resistance. Figure 1.7 shows the power MOSFET and the IGBT structures.

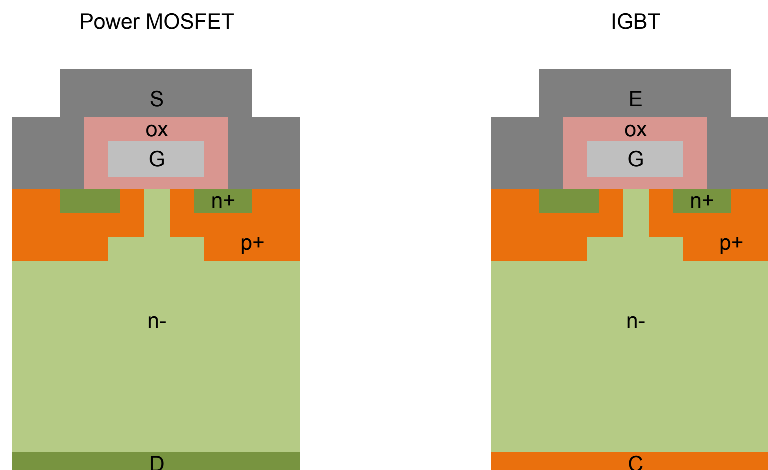


Figure 1.7 Structures for the Power MOSET and IGBT

Superjunction transistors [2] are another modification on the power MOSFET, improving on the breakdown with an adjusted field profile in the drift region by juxtaposing p- columns. This causes the field to be constant along this superjunction, and the voltage to vary linearly. The transistor can exceed the limit to breakdown described by 1.12.

For SiC transistors, in addition to the DMOS structure as used in Si, a different structure based on JFETs is also used for high voltage. These transistors have a double gated n-type fin, with p-type material on the sidewalls which provide the gating. Since SiC has a much higher critical field, the breakdown voltage is greatly improved, while maintaining a low R_{on}. However, as this is with SiC, substrate and epitaxial growth costs increase with respect to Si, and these transistors are used when specific performance characteristics need to be achieved. Structures for both the superjunction MOSFET and the SiC JFET are shown in Figure 1.8.

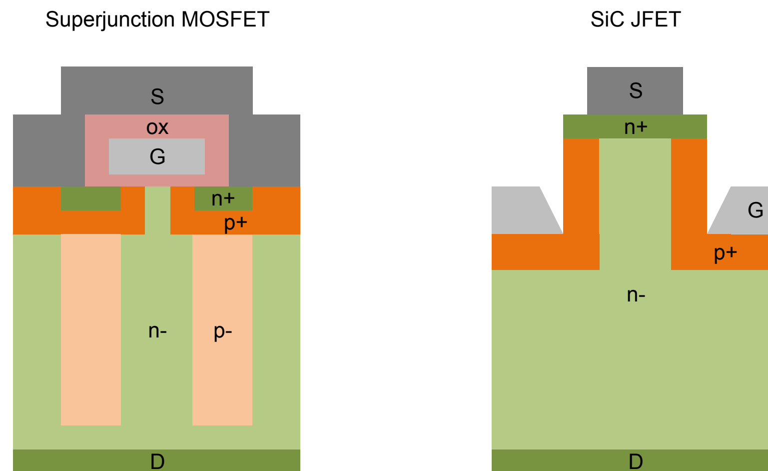


Figure 1.8 Superjunction MOSFET and SiC JFET structures

1.3.2 Vertical GaN Transistors in Development

As GaN's theoretical limit to the power density is greater than SiC, research into vertical GaN has yielded a few different structures. Some of the challenges are from the poor mobility for active p-type regions, however GaN benefits from being able to form a 2DEG from a

HEMT stack. The variations in structure address the gating mechanism, and attempt to give a low I_{off} and low R_{on} simultaneously. Four vertical GaN structures are shown in Figure 1.9.

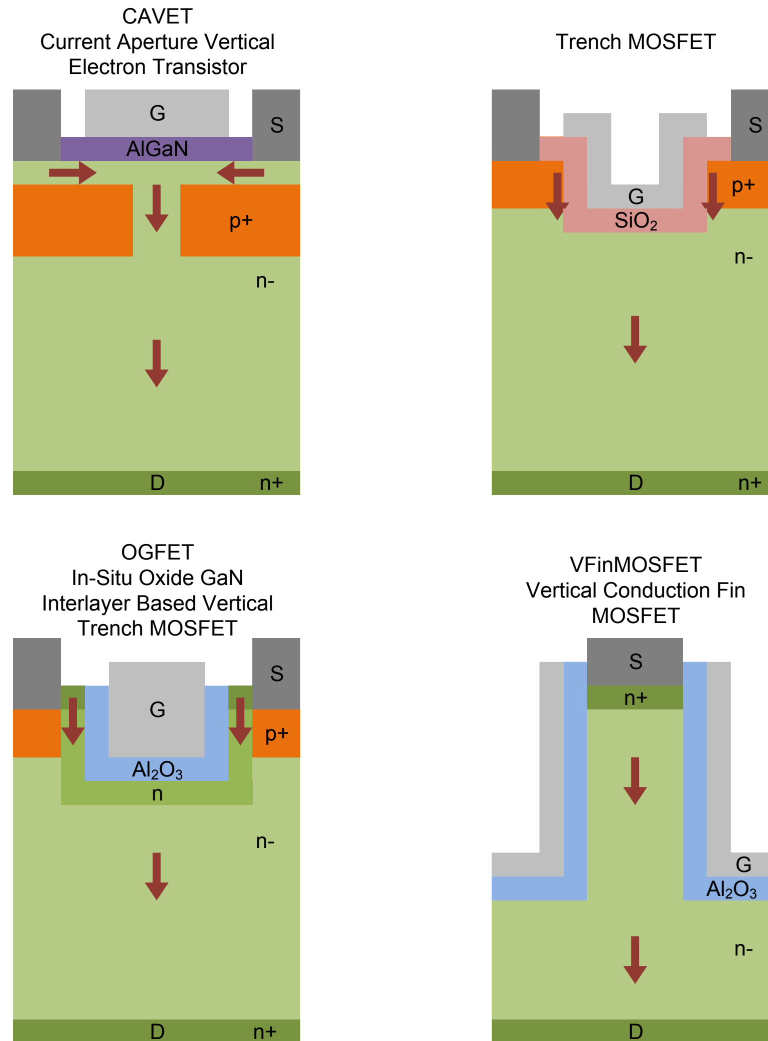


Figure 1.9 Structures for vertical GaN transistors. The arrows indicate the direction of flow of electrons.

The CAVET [3], or current aperture vertical electron transistor, is like the power MOSFET structure, except that instead of inverting a p-type layer to form an n-channel, an AlGaN/GaN HEMT is used. Current flows laterally along the induced 2DEG, then down an n-type aperture in the p-type blocking layer. While this lateral channel is easy to achieve, the buried p-type layers pose some difficulties with dopant activation.

The trench MOSFET [4] attempts to correct this by having a vertical channel, and keeping the p-regions at the surface. A trench is etched through the p-layers, then gated along with an oxide. However, since the polarization induced 2DEG is not present in the vertical faces, the channel is a traditional MOSFET utilizing an inversion layer to create the charge layer. The OGFET [5] is a variation on this concept where a thin n-type layer is regrown in the trench before oxide deposition. This provides a higher mobility n-channel to improve R_{on}.

Taking a similar approach to the SiC JFET, the vertical conduction fin MOSFET, VFinMOSFET, uses a double gated fin to control the current. However, to avoid using a p-layer, the fin is gated with a MOSFET. This requires narrow dimensions for the fin as well as a method of maintaining a good interface quality along the fin sidewalls. When the device is turned on, a 2DEG is formed on the sidewalls as a MOSFET, and to pinch off current, the fin depletes, acting as a MESFET. The remainder of this dissertation will deal with modeling, fabrication, and analysis of and relating to the VFinMOSFET.

Chapter 2: Simulation and Modeling

An understanding of the physics in the transistor significantly aids in both the original design of the transistor and the analysis of measured characteristics of processed devices. Simple calculations supplemented by simulations provide a basis for choosing dimensions and materials for an initial processing attempt. More advanced models can be used to quickly change parameters to diagnose issues that may be seen in processed devices, without running long simulations.

The VFinMOSFET operation can be described by looking at the current control within the fin. Taking the fin as two unipolar MOS gates, we can see the different modes of operation. When the gate bias is such that the MOS depletion width is at least half the width of the fin at the source, the whole fin is depleted and current cannot flow. Increasing the gate bias, a 2DEG is formed along the oxide semiconductor interface, which forms a channel for current flow. With an applied drain bias, the potential along the channel is not uniform and the portion of the channel near the source may be accumulated, while the bottom of the fin is partially depleted, or even pinched off. When the bottom of the fin is pinched off, the current saturates. This will be considered hybrid mode as the operation of the transistor in this mode exhibits the characteristics of both a MOSFET and a MESFET. Figure 2.1 shows these three modes of operation.

It is also possible for the transistor to operate without an accumulated channel near the source. To remain on, some of the fin width must not be depleted at the source, allowing current to flow. This mode of operation acts like a double gated MESFET. Simulating the transistor can determine which modes exist for typical bias conditions. Understanding the current flow

in each of these modes, as well as the conditions for when each occur, is necessary when developing a model for the device.

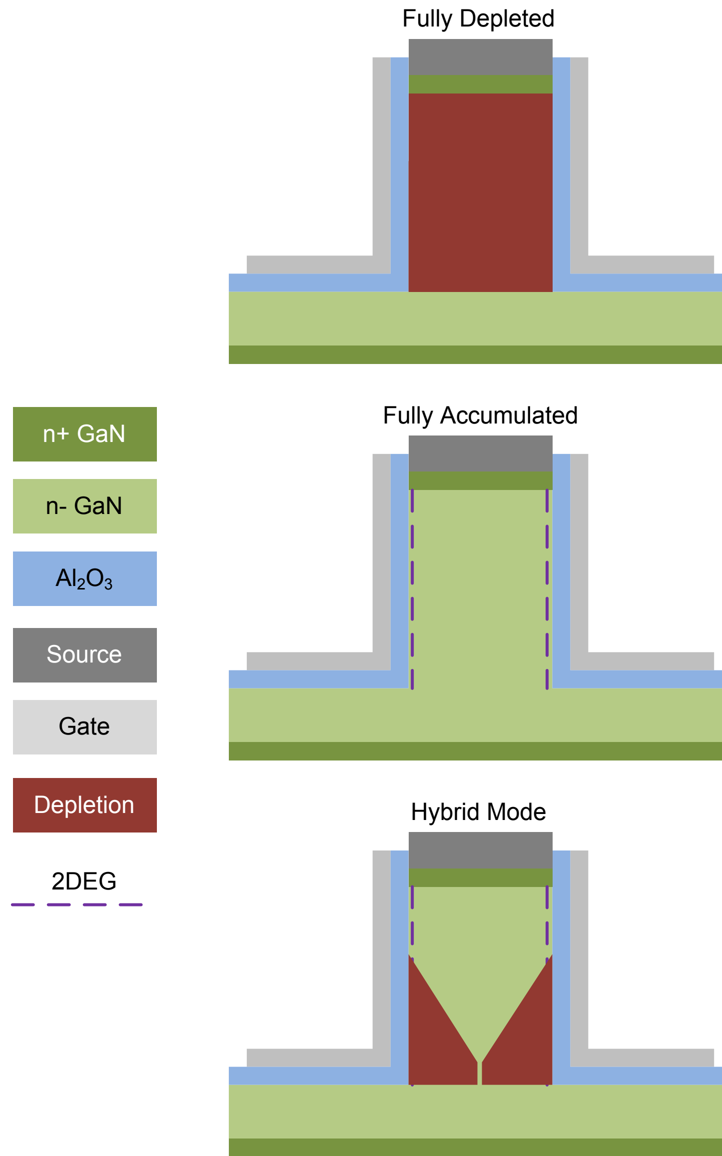


Figure 2.1: Modes of operation for the VFinMOSFET.

2.1 Finite Element Simulations

Utilizing a package by Silvaco called Atlas [6], several properties can be simulated with the built-in solvers. Of note, the band structure, charge density, current density, and electric fields can be calculated for various potentials to structures. This aids in understanding the

different modes of operation for the transistor as it gives an image into points of interest in the cross section of the fin for the VFinMOSFET.

Atlas uses finite element analysis to solve the various equations including Poisson, Schrodinger, continuity, and transport equations in a mesh defined by the user. The code used to generate the mesh for the VFinMOSFET and solve the structure is located in Appendix B. Simulation of the transistors allows for optimizing transistor dimensions without the expense of growing wafers and fabricating devices in addition to the ability to dissect the fin and measure properties with respect to position.

In order to confirm the modes of operation of the transistor, the structure was simulated and values extracted for both the on-state and the off-state. The drain was biased at 20 V, while the gate was set to 0 V and 5 V for off and on-states respectively. The fin thickness, a, is 300 nm, while the fin height, L_f, is 3 μm. The doping in the fin and drift layers is 1e15 cm^{-3}, and the Al_2O_3 thickness, t_{ox}, is 50 nm. The drift region thickness, D, is 4 μm, and the spacing between fins is 4 μm, with repeating boundary conditions to emulate several fins in parallel.

Figure 2.2 and Figure 2.3 show the electron concentrations in both states. When in the off-state, the electrons are depleted from the fin with the few remaining electrons in the center, where we would expect the lowest potential, due to the band bending. For the on-state, there is an increased concentration of electrons in the fin, with a peak at the sidewalls, indicating a 2DEG. Current density is related to the electron concentration, shown in Figure 2.4 and Figure 2.5. In the off-state, leakage current passes through the center of the fin, while in the on-state, the majority of current is along the sidewalls of the fin where there is an accumulated 2DEG. Simulations of wider fins also inform us that the current through the center of the fin can still be a significant component of the total current measured.

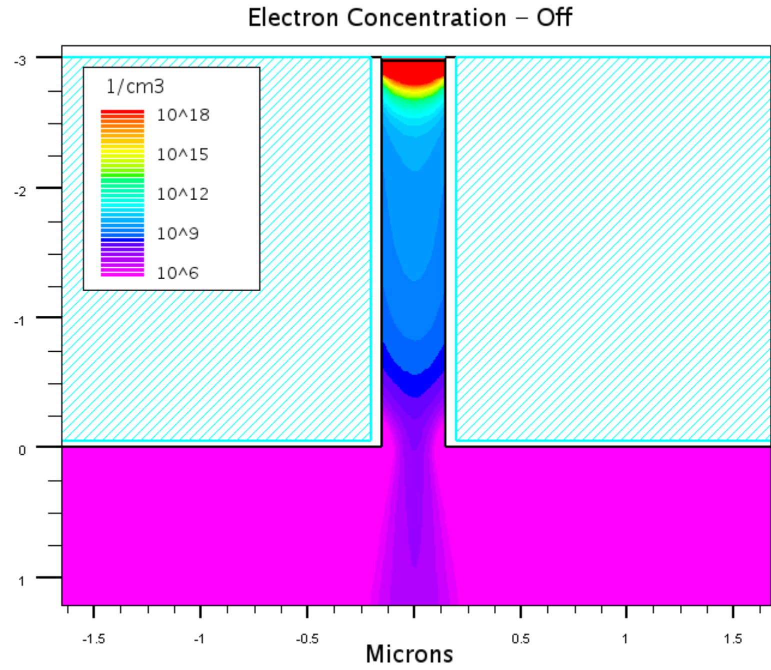


Figure 2.2: Simulation of electron concentration in off-state.

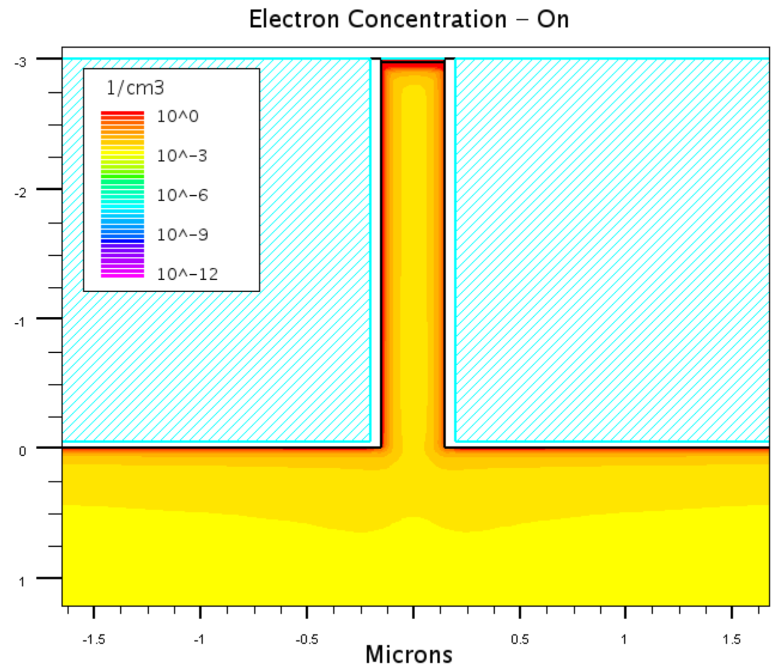


Figure 2.3: Simulation of electron concentration in on-state.

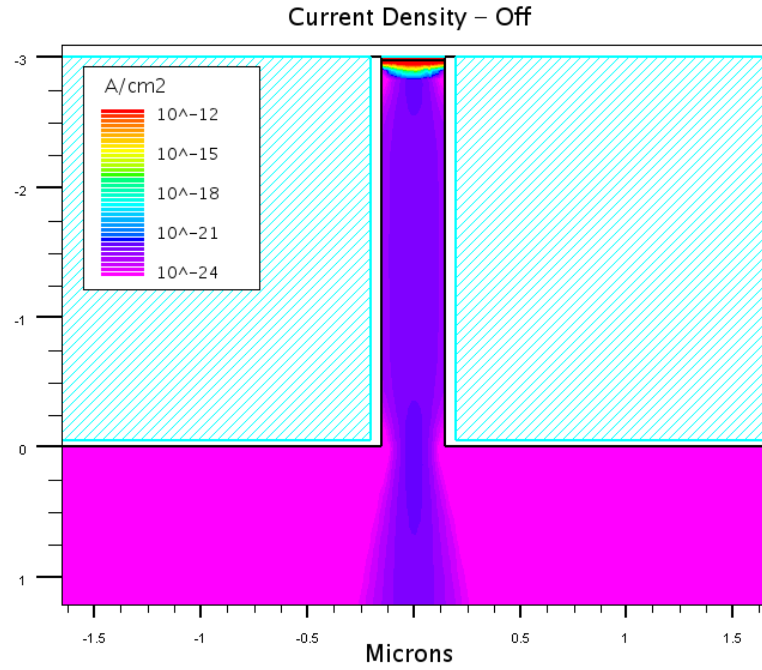


Figure 2.4: Simulation of current density in off-state.

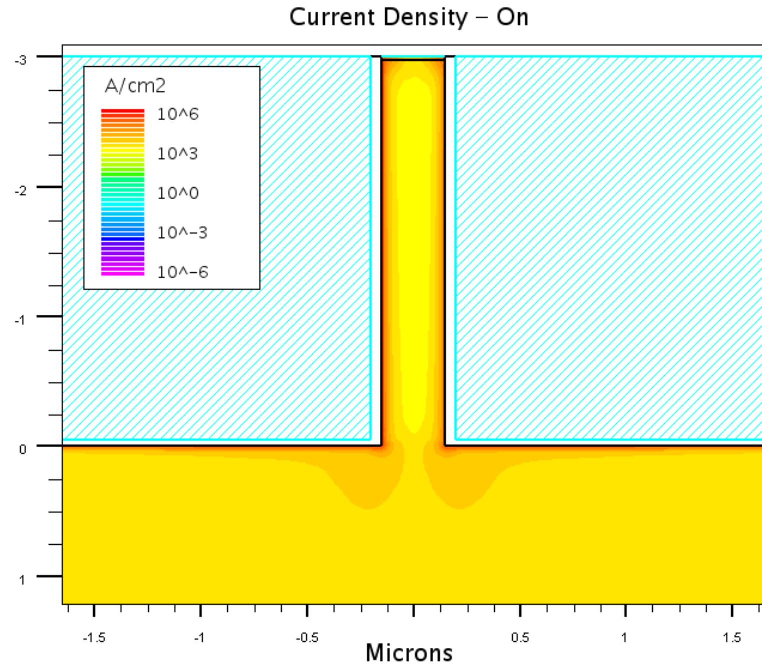


Figure 2.5: Simulation of current density in on-state.

Figure 2.6 and Figure 2.7 show the voltage at each point in the fin with a 20 V drain bias applied. When in off-state, the voltage appears to be held from the gate to the drain. This is

expected since both the source and gate are at the same voltage. In the on-state, there is a voltage drop along the fin, though the majority appears to be in the drift region. The electric field plots in Figure 2.8 and Figure 2.9 help explain the voltages, with the largest electric field indicating the locations of largest change in potential. In the off-state, the peak field is at the corner of the fin, indicating that is the most likely point to break down. In the on-state, the magnitude of the peak field is lower, and is now located below the gate between adjacent fins.

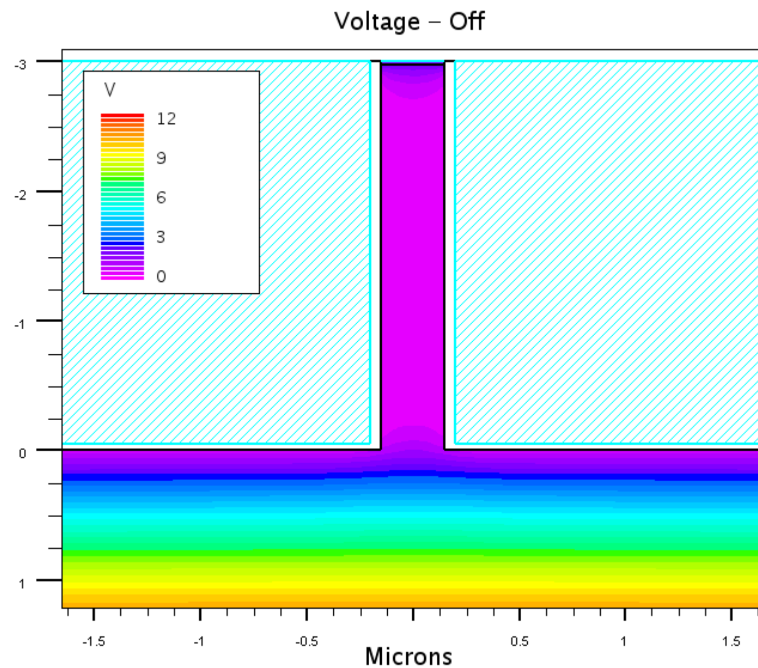


Figure 2.6: Simulation of voltage in off-state.

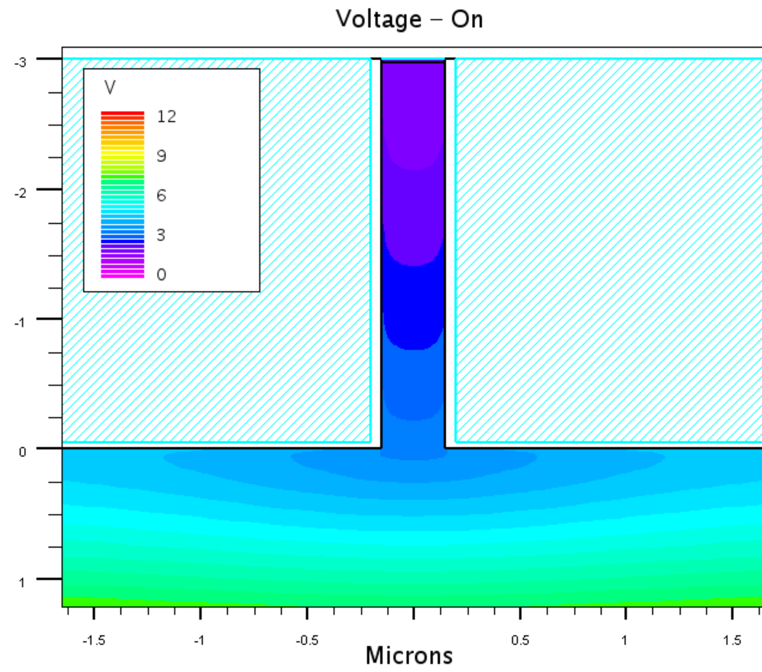


Figure 2.7: Simulation of voltage in on-state.

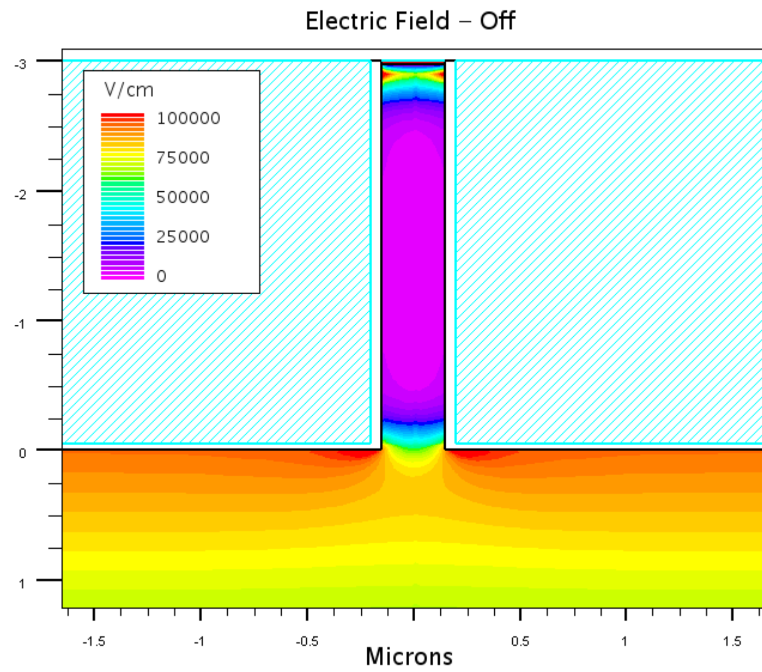


Figure 2.8: Simulation of electric field in off-state.

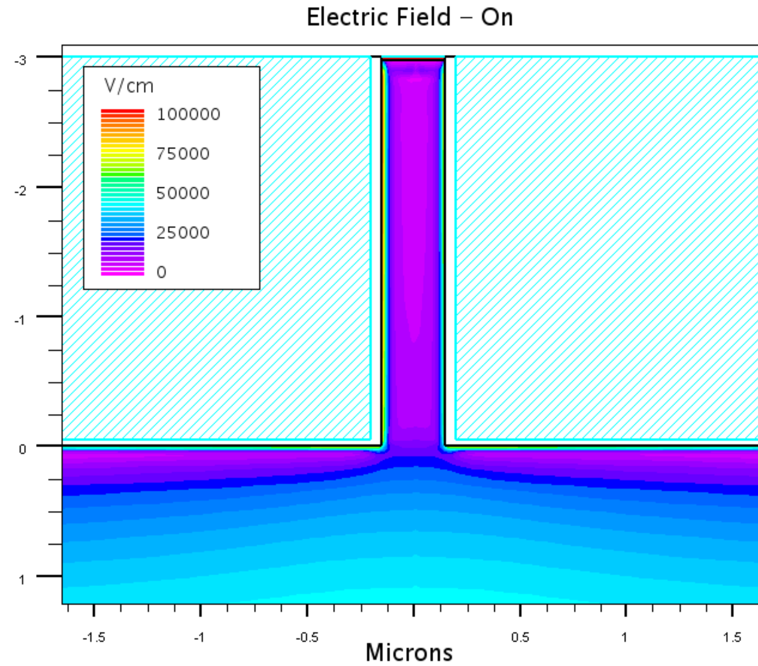


Figure 2.9: Simulation of electric field in on-state.

In addition to simulating at the previously mentioned bias voltages, a full I-V curve was calculated using the simulated structure. Figure 2.10 shows that the current density expected in the device should be around 1 A/cm, giving a current density of 2.3 kA/cm^2 using the product of the pitch between fins and the length of the fin as the device area. For a single fin, 10 Ω·cm is the extracted R_{on} per µm of fin width from the linear region, giving a specific R_{on} of 4.3 mΩ·cm^2, normalized to the same device area. A threshold voltage of 1.03 V and I_{on}/I_{off} ratio of about 10^{12} can be extracted from the gate sweep in Figure 2.11.

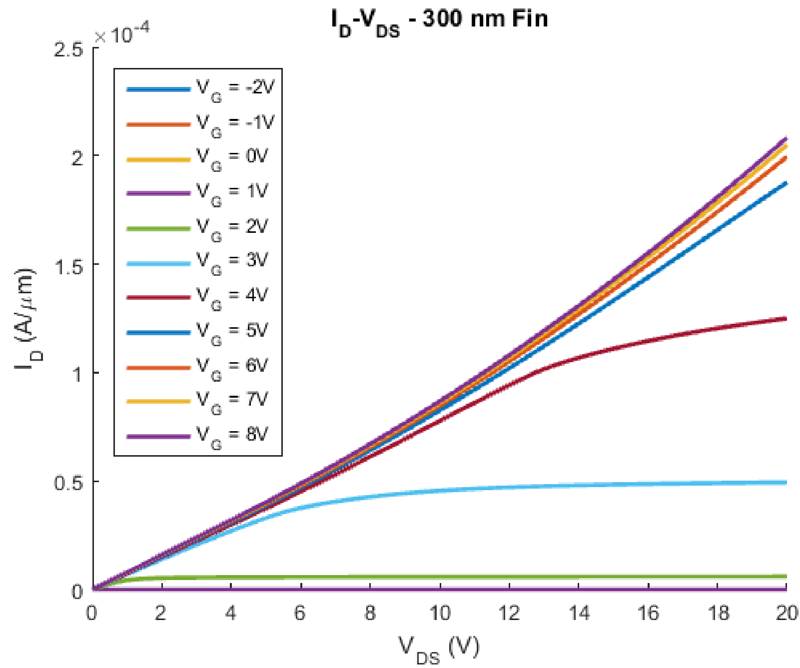


Figure 2.10: I-V curve of simulated 300 nm fin, normalized to the length of the fin.

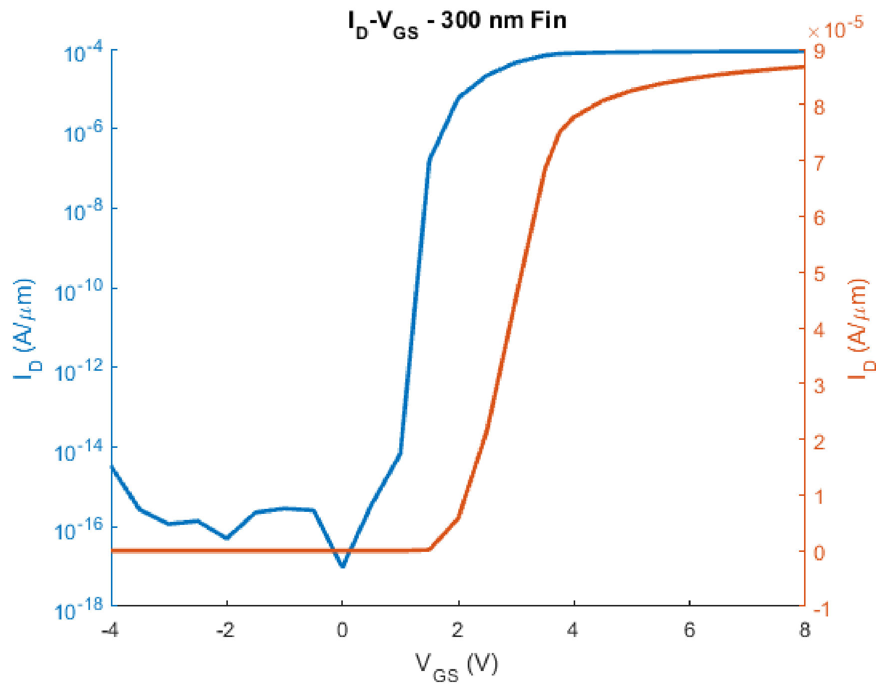


Figure 2.11: Gate sweep of simulated 300 nm fin, normalized to the length of the fin. V_{DS}=10 V.

Using the simulation code, we can compare devices of different dimensions, and examine the expected effect on device characteristics. Simulating fins of various widths from 300 nm

to 3 µm and sweeping the gate voltage, the effect on the threshold voltage has been extracted. Figure 2.12 and Figure 2.13 show the curves for these transistors in linear and log scale respectively. For larger fins, the threshold voltage decreases, which is to be expected since a lower gate voltage would be required to fully deplete wider fins and close off all the current. However, for the smaller fins, the threshold voltage appears to remain at around 1 V, with decreasing size not affecting V_T further. This may be due to a small difference between the voltage to fully deplete the fin, and the voltage to form a 2DEG. Figure 2.14 plots the extracted threshold voltage and compares it to calculated values which will be derived in Section 2.2.3. The extracted threshold voltage is defined as the gate voltage when the current is crosses 10^{-8} A/µm.

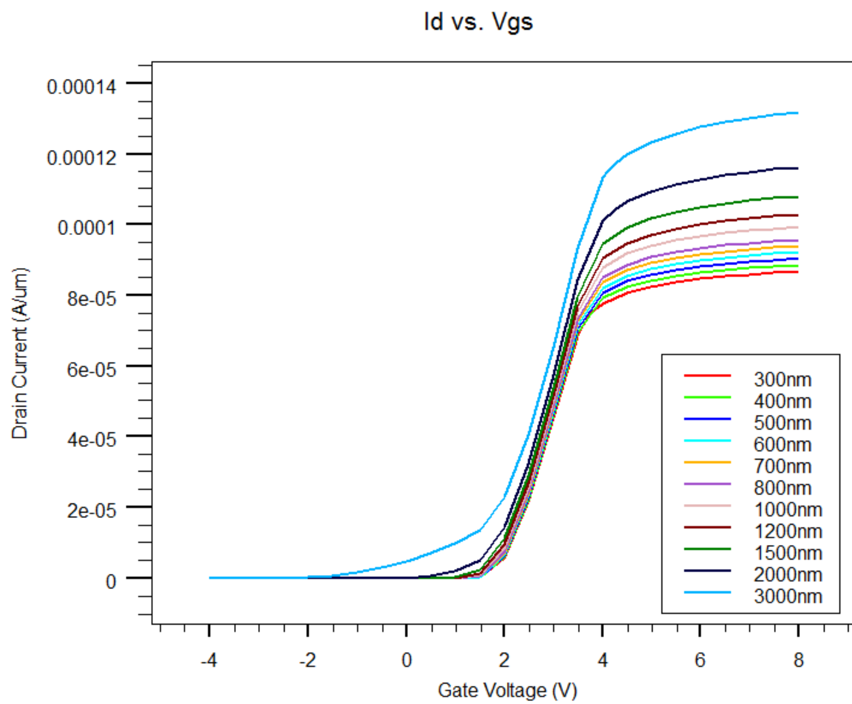


Figure 2.12: Simulated gate sweep for various fin widths in linear scale.

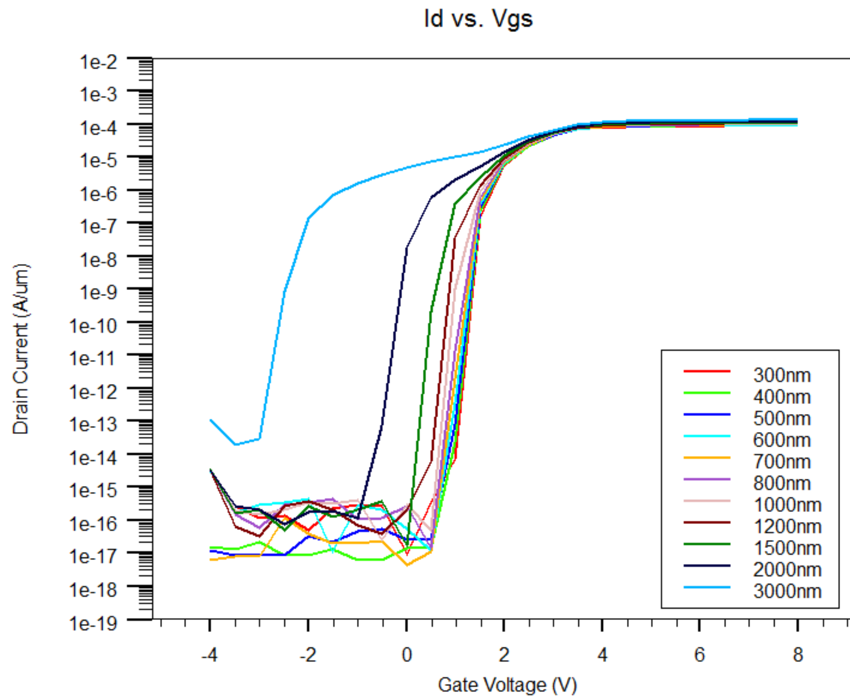


Figure 2.13: Simulated gate sweep for various fin widths in log scale.

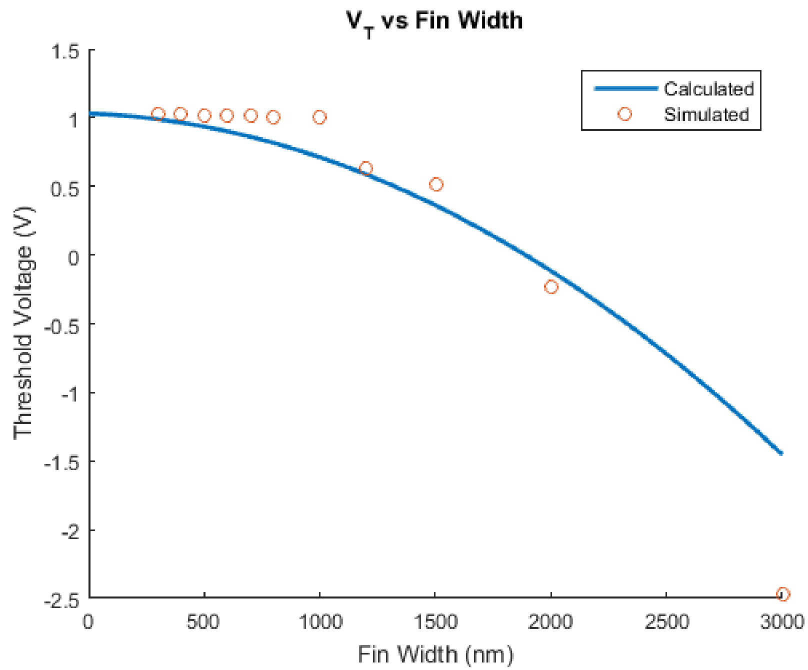


Figure 2.14: Threshold voltages for various fin widths, extracted from simulation, and calculated.

2.2 Fin Region I-V Calculations

A 1-dimensional model for the transistor can be derived by dividing the transistor into different regions of operation and solving for the current in each one individually. Assuming that there is no gate leakage, and that recombination and generation are not significant contributors of current, the current throughout the different regions must be equal. As this device is unipolar, and operates with majority carriers only, recombination and generation should remain insignificant. By measuring the leakage of the gate oxide on test structures and devices when processing the transistors, the former assumption can also be verified. Figure 2.15 shows the transistor with the defined regions and labels the dimensions and voltages associated with them.

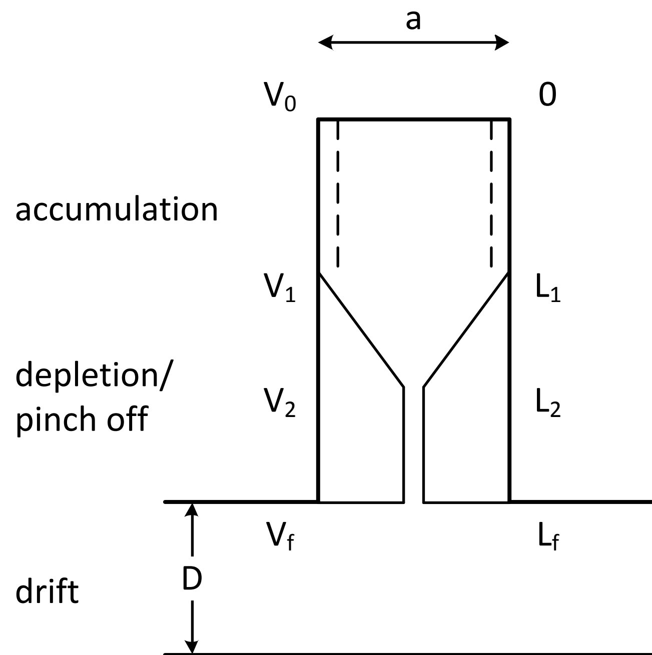


Figure 2.15: Regions of various types of operation along the fin to be modeled.

2.2.1 Accumulated Channel

The accumulation region can be modeled very similarly to a MOSFET using the gradual channel approximation. The current through the fin can be described by 2.1, where Z is the length of the fin, n_s is the accumulated sheet charge, μ_n is the electron mobility, and V_{ch} is the voltage at the channel with respect to position along the fin. x is defined as the vertical distance from the top of the fin. This expression comes from the product of charge, $q \cdot Z \cdot n_s$, and velocity, $\mu_n \cdot dV_{ch}/dx$. The factor of two is added since there is an accumulated channel on both sides of the fin.

$$I_D \cdot dx = 2q \cdot Z \cdot n_s \cdot \mu_n \cdot dV_{ch} \qquad 2.1$$

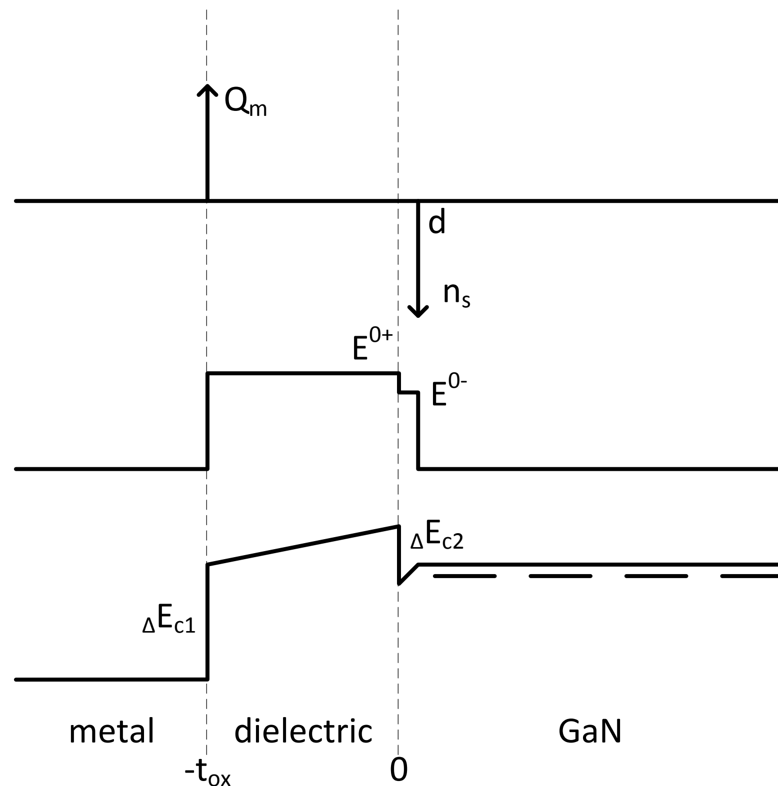


Figure 2.16: Charges, field, and conduction band across the MOS in accumulation.

n_s is dependent on V_{ch}, and is derived by solving for the MOS accumulated charge using Poisson's equation, and charge conservation. Figure 2.16 shows the charge, field, and conduction band across the oxide. Setting the accumulated charges in the metal and semiconductor equal, and adding the potential changes, we get 2.2 and 2.3.

$$Q_m = q \cdot n_s \tag{2.2}$$

$$0 = -q \cdot V_{gs} + \Delta E_{c1} + q \cdot \frac{Q_m}{\varepsilon_{ox}} \cdot t_{ox} - \Delta E_{c2} + q^2 \cdot \frac{n_s}{\varepsilon_{GaN}} \cdot d - k \cdot T \cdot \ln\left(\frac{N_c}{N_D}\right) \tag{2.3}$$

These expressions assume that there are no fixed charges in the oxide, or trap states at the oxide semiconductor interface. From this we get an expression for n_s, 2.4, and setting this equal to zero gives us the gate threshold voltage, V_T, defined as when there is no more charge in the 2DEG. ΔE_c is defined as the electron affinity difference between the metal and semiconductor, or ΔE_{c1}-ΔE_{c2}. This threshold voltage, expressed in 2.5, will be used to determine the boundary between the accumulated region and the depleted region in the model.

$$q \cdot n_s = \frac{V_{gs} - V_{ch} - \Delta E_c + \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_C}{N_D}\right)}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{d}{\varepsilon_{GaN}}} \tag{2.4}$$

$$V_T = V_{gs} - V_{ch} \quad \text{at} \quad \left(n_s = 0\right) = \Delta E_c - \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_C}{N_D}\right) \tag{2.5}$$

To solve for the current in this region, we substitute 2.4 into 2.1 and integrate both sides as in 2.6. This results in 2.7 for an expression of the current in the region for accumulation.

$$\int_0^{L_1} I_D\,dx = -\frac{2\cdot Z\cdot\mu_n}{\frac{t_{ox}}{\varepsilon_{ox}}+\frac{d}{\varepsilon_{GaN}}}\cdot\int_{V_o}^{V_1} V_{ch}+V_T-V_{gs}\,dV_{ch} \qquad 2.6$$

$$I_D = \frac{Z}{L_1}\cdot\frac{2\cdot\mu_n}{\frac{t_{ox}}{\varepsilon_{ox}}+\frac{d}{\varepsilon_{GaN}}}\cdot\left[V_1\cdot\left(V_{gs}-V_T\right)-\frac{1}{2}\cdot V_1^{\,2}-V_o\cdot\left(V_{gs}-V_T\right)+\frac{1}{2}\cdot V_o^{\,2}\right]\cdot \qquad 2.7$$

2.2.2 Channel Depletion and Pinch Off

While the modelling of the channel in accumulation is very similar to a MOSFET, the modelling for when the channel is depleting or pinched off is similar to the model for a MESFET. To get the current flow in the channel, we once again take the product of the charge and the velocity, as shown in 2.8, where the charge is now determined by the undepleted width $a\text{-}2\cdot W_D$ and the doping in the fin, N_D.

$$I_D = q\cdot\left(a-2\cdot W_D(x)\right)\cdot N_D\cdot Z\cdot v(x) \qquad 2.8$$

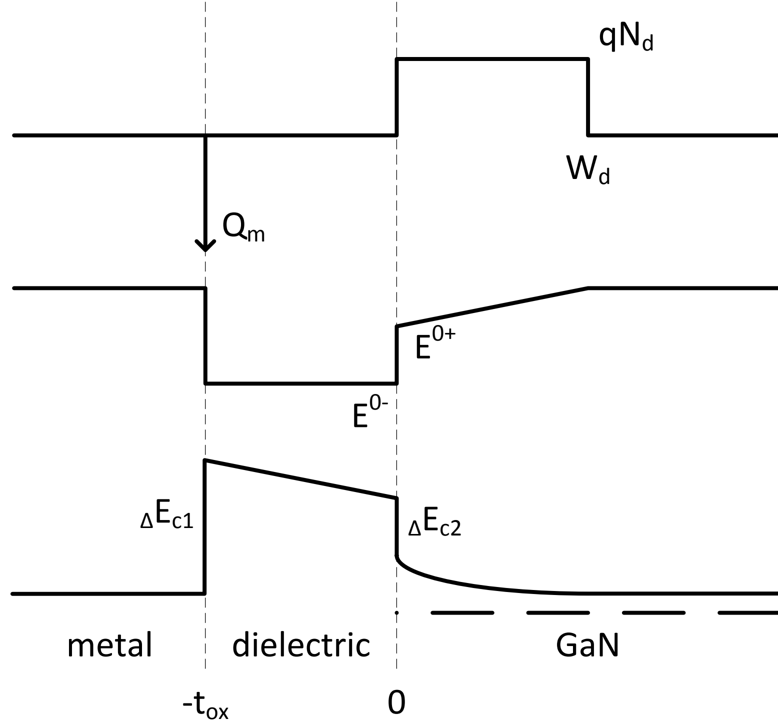


Figure 2.17: Charges, field, and conduction band across the MOS in depletion.

W_D is the depletion width from the MOS capacitor on one side of the fin. As this varies with the channel voltage, it therefore varies along the height of the fin. An expression for the depletion width can be derived from Poisson's equation and charge conservation. Figure 2.17 shows the charge, field, and potential of the MOS in depletion. Charge conservation gives us 2.9, while adding the potentials we get 2.10. A full expression for the depletion width with respect to V_{ch} is given by 2.11. Setting the depletion width to zero determines the accumulation threshold, which matches up with the expression for V_T in 2.5.

$$Q_m = q \cdot N_D \cdot W_D \tag{2.9}$$

$$0 = -q \cdot V_{gs} + \Delta E_{c1} - q \cdot \frac{Q_m}{\varepsilon_{ox}} \cdot t_{ox} - \Delta E_{c2} - \frac{q^2 \cdot N_D \cdot W_D^{\,2}}{2 \cdot \varepsilon_{GaN}} - k \cdot T \cdot \ln\left(\frac{N_C}{N_D}\right) \tag{2.10}$$

$$W_D = -\frac{\varepsilon_{GaN}}{\varepsilon_{ox}} \cdot t_{ox} + \sqrt{\frac{\varepsilon_{GaN}^2}{\varepsilon_{ox}^2} \cdot t_{ox}^2 - \frac{2 \cdot \varepsilon_{GaN}}{q \cdot N_D} \cdot \left(V_{gs} - V_{ch} - \Delta E_c + \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_C}{N_D}\right)\right)} \qquad 2.11$$

While the channel was operating in accumulation, the field does not go high enough that the velocity begins to saturate, whereas in depletion, and more specifically pinch off, velocity saturation needs to be included. A simple way to do this is to use an expression for *v* that is not a linear relationship with electric field. Sze [7] provides a useful empirical fitting curve for the velocity, 2.12. Using data from Bhapkar [8], who simulated the velocity curves for GaN, a somewhat reasonable fit can be achieved for fields below $2 \cdot 10^5$ V/cm by using $4 \cdot 10^7$ cm/s as v_s. Figure 2.18 shows a piecewise approximation of Bhapkar's data, and the fitted curve.

$$v_{model}(E) = \frac{\mu_n \cdot E}{1 + \mu_n \cdot \frac{E}{v_s}} \qquad 2.12$$

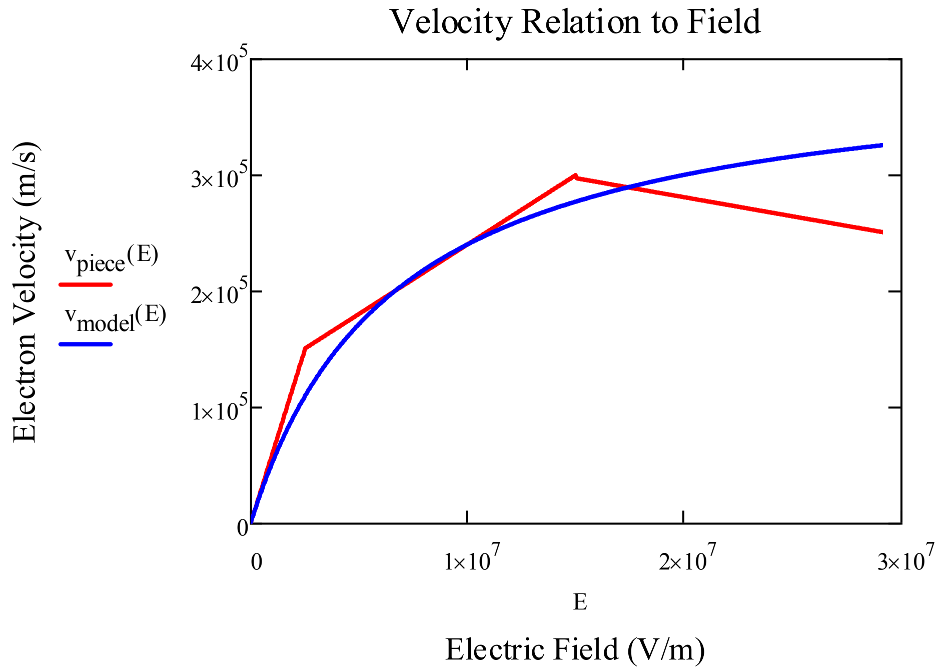


Figure 2.18: Piecewise approximation and fit for GaN velocity curve.

We can now combine the expressions for W_D and v into 2.8 and integrate as in 2.13. This results in a long expression for current described by 2.14. While this will give us the current in the linear regime, approaching saturation, the saturation current itself must be derived from this expression by finding the maximum value. The derivation of the maximum point results in an expression that must be solved implicitly for I_D.

$$\int_{L_1}^{L_2} I_D \cdot \left(1 + \frac{\mu_n}{v_s} \cdot \frac{d}{dx} V_{ch}\right) dx = -q \cdot \mu_n \cdot N_D \cdot \int_{V_1}^{V_f} \left(a - 2 \cdot W_D\right) dV_{ch} \qquad 2.13$$

$$I_D = \frac{q \cdot \mu_n \cdot N_D \cdot Z}{L_f - L_1 + \frac{\mu_n}{v_s} \cdot \left(V_f - V_1\right)} \cdot \left[\left(V_f - V_1\right) \cdot \left(a + 2 \cdot t_{ox} \cdot \frac{\varepsilon_{GaN}}{\varepsilon_{ox}}\right) \ldots + \frac{-2 \cdot q \cdot N_D}{3 \cdot \varepsilon_{GaN}} \cdot \left[\left[t_{ox}^2 \cdot \frac{\varepsilon_{GaN}^2}{\varepsilon_{ox}^2} + 2 \cdot \frac{\varepsilon_{GaN}}{q \cdot N_D} \cdot \left(V_f + V_T - V_{gs}\right)\right]^{\frac{3}{2}} \ldots + - \left[t_{ox}^2 \cdot \frac{\varepsilon_{GaN}^2}{\varepsilon_{ox}^2} + 2 \cdot \frac{\varepsilon_{GaN}}{q \cdot N_D} \cdot \left(V_1 + V_T - V_{gs}\right)\right]^{\frac{3}{2}}\right]\right] \qquad 2.14$$

2.2.3 Transistor Threshold Voltage

To find the threshold voltage of the transistor, as opposed to the threshold to switch between accumulation and depletion, we determine when the fin is fully depleted at the source. To distinguish this from the channel threshold V_T, this is labeled V_P, or pinch off voltage. Setting the total depletion width from both sides of the fin to the width of the fin, we get 2.15. This is related to V_T by 2.16 and is used to calculate values in Figure 2.14. The latter term of this expression indicates the sensitivity of the transistor threshold voltage on the width of the fin.

$$V_P = V_{gs} - V_{ch} \text{ at } (2W_D = a) = \Phi_B - \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_c}{N_D}\right) - \frac{q \cdot N_D \cdot a}{2} \cdot \left(\frac{a}{4 \cdot \varepsilon_{GaN}} + \frac{t_{ox}}{\varepsilon_{ox}}\right) \quad 2.15$$

$$V_P = V_T - \frac{q \cdot N_D \cdot a}{2} \cdot \left(\frac{a}{4 \cdot \varepsilon_{GaN}} + \frac{t_{ox}}{\varepsilon_{ox}}\right) \quad 2.16$$

When the gate to source voltage, V_{gs}, is less than V_P, we expect no current to flow through the device due to the lack of charge. In reality, the current would be a finite value I_{off}, which could be derived by calculating the thermal current over the barrier in the channel at the source. However, this would require a two-dimensional calculation of Poisson's equation for the fin and drift region to determine the barrier height induced by the gate. The model presented here does not venture further in calculating the sub-threshold current and merely assumes the current to be zero when the source is pinched off.

2.2.4 Drift Region Current

The final region shown in Figure 2.15 is the drift region. In this layer, there is no longer a gated channel and the electrons are limited by the resistivity of the material. It can be expected that there will be some current spreading. The simulated current flow in Figure 2.5 verifies this. To calculate the resistance added by the drift region, we assume that the profile of the current flow is a trapezoid, as described by Baliga [9]. We examine two cases; for the first, the current spreading distance, L_s, is less than the distance to the next fin, and in the second, an adjacent fin limits the current spreading distance. Figure 2.19 and Figure 2.20 illustrate the assumed current spreading profile for the two situations respectively.

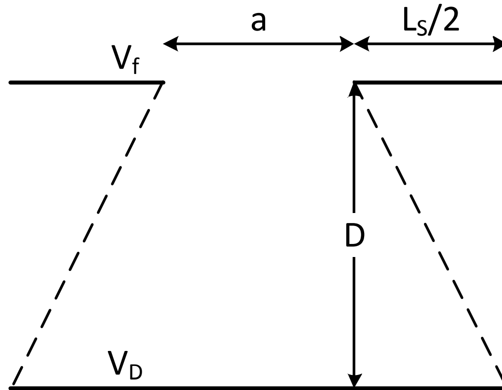


Figure 2.19: Drift region current spreading profile for *Ls* < *fin spacing*.

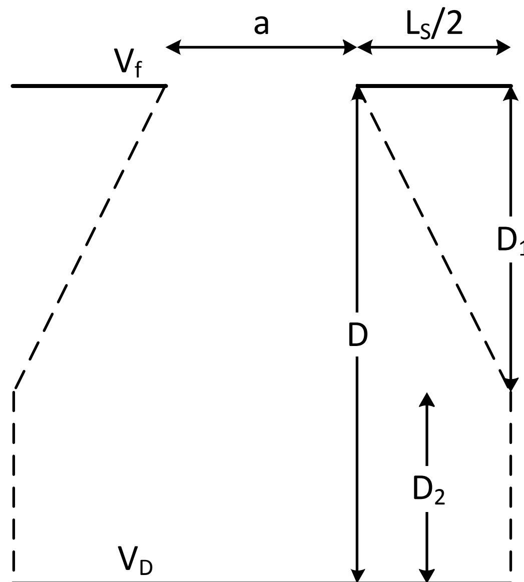


Figure 2.20: Drift region current spreading profile for *Ls* > *fin spacing*.

To find the resistance, R_D, of the current profile, we must integrate the resistivity through the depth of the drift region, giving us 2.17, where ρ is the vertical resistivity. This derivation assumes we know the current spreading profile. Baliga assumes that the spreading profile is 45°, so that L_s would be D. While this may be a close approximation, it may not be the case and should be verified.

$$R_D = \int_0^D \frac{\rho}{Z} \cdot \frac{1}{a + \frac{L_s}{D} \cdot x} \, dx = \frac{\rho}{Z} \cdot \frac{D}{L_s} \cdot \ln\left(\frac{a + L_s}{a}\right) \qquad 2.17$$

For the later scenario, where adjacent fins limit the current spreading, L_s is now the distance from one fin to the next, resulting in a pitch of L_s+a. The trapezoid region remains down to a depth of D_1, and becomes a rectangular profile for the remainder of the drift region depth, D_2. The total resistance is the sum of the resistances of the two regions, and derived in 2.18. Assuming a profile of 45° results in $2D_1=L_s$, which is also the fin spacing.

$$R_D = \frac{\rho}{Z} \cdot \left(\int_0^{D_1} \frac{1}{a + \frac{L_s}{D} \cdot x} \, dx + \frac{D_2}{a + L_s} \right) = \frac{\rho}{Z} \cdot \left(\frac{D_1}{L_s} \cdot \ln\left(\frac{a + L_s}{a}\right) + \frac{D_2}{a + L_s} \right) \qquad 2.18$$

2.2.5 Combined Intrinsic Model

As explained previously, the current through each of the regions will be equal, with the assumptions made. Therefore, the expressions for current can be set equal to each other, and the intermediate voltages, or accumulated and depleted lengths can be calculated. Unfortunately, these equations must be solved implicitly and a single expression for the current through the whole device cannot be derived. In addition, one of the modes of operation may not exist for certain bias conditions, and so the solver used must determine if certain conditions exist, and account for any changes.

Code was written for MATLAB utilizing its function solvers, which is presented in Appendix C. Conditions are included in the function modules, in particular, the condition of whether the fin is in full accumulation, no accumulation, or in hybrid operation, as well as whether the current is saturated. Figure 2.21 shows the modeled I-V curve for a fin with the

same dimensions as that in Figure 2.10. The increasing current in saturation shown in the figure is due to channel length modulation resulting from the velocity saturation model used.

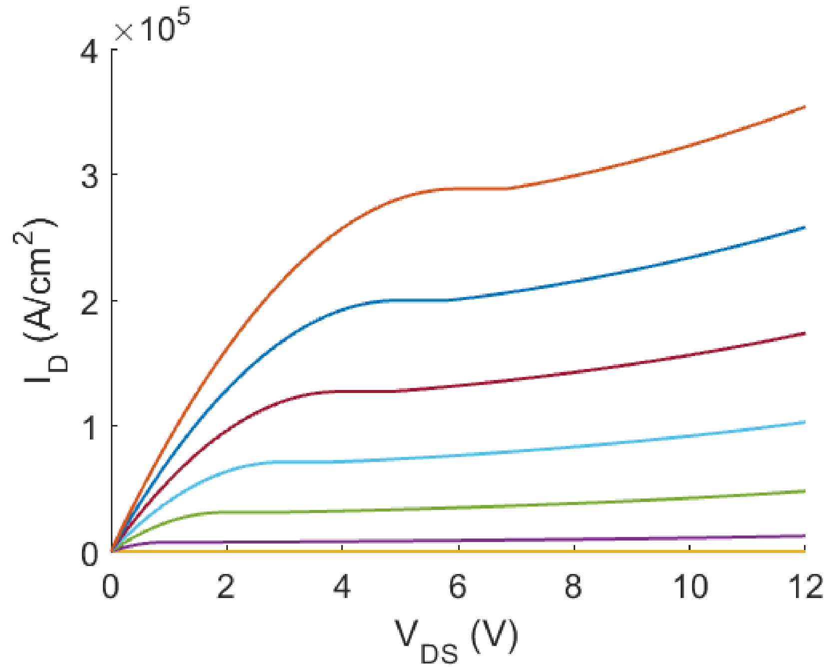


Figure 2.21: I-V curves for a 300 nm fin from the model, normalized to lateral fin area.

2.3 Schottky Contact Modeling

In the case of Schottky contacts, there are two main sources of current to consider. First is the thermal current; electrons with a high enough energy pass over the barrier to the other side. The other source of current is electrons tunneling through the barrier. Diffusion current is possible, but for contacts that are relevant to the VFinMOSFET, thermal emission dominates the current. The thermal current can be described by 2.19, where A is the Richardson constant which equals 120 $C \cdot cm^{-2} \cdot K^{-2} \cdot s^{-1}$. Φ_B is the barrier height from the metal to the semiconductor conduction band, and V_o is the applied voltage across the contact.

$$I_D = a \cdot Z \cdot A \cdot \frac{m_{eff}}{m_e} \cdot T^2 \cdot e^{-\frac{q \cdot \Phi_B}{k \cdot T}} \cdot \left(e^{-\frac{q \cdot V_o}{k \cdot T}} - 1 \right) \quad 2.19$$

In reverse bias, the tunneling current overshadows the thermal current. To get the tunneling current, we need to find the product of the electron velocity and tunneling probability and integrate over the available electrons. The tunneling probability from WKB for a triangular barrier which approximates the junction is given by 2.20, where E_{max} is the electric field induced at the interface, which leads to the slope in potential. For a triangular barrier, this is Φ_B divided by the tunneling width, or the portion of the depletion width that the electrons need to tunnel across. The effective mass is that of the source of electrons, which for reverse bias is the metal. The electron energy in terms of wavenumber is given by 2.21.

$$\Theta = e^{-2 \cdot i \cdot \sqrt{\frac{8 \cdot m_{efff}}{E_{max} \cdot \hbar}} \cdot \left(E - \Phi_B\right)^{\frac{3}{2}}} \quad 2.20$$

$$E\left(k_x\right) = \frac{\hbar^2 \cdot {k_x}^2}{2 \cdot m_{eff}} \quad 2.21$$

The electron velocity is dependent on the wavenumber of the electron in the direction of travel, k_x, given by 2.22. The distribution of available electrons must be organized by wavenumber to be able to integrate. The required relation can be derived from density of states calculations and is given in 2.23. Combining these all together in an integral gives the tunneling current relation 2.24, which is solved as part of the model calculations.

$$v\left(k_x\right) = \frac{\hbar \cdot k_x}{m_{eff}} \quad 2.22$$

$$n(k_x) = \frac{m_{eff}}{\hbar^2 \cdot \pi^2} \cdot dk_x \qquad 2.23$$

$$J_s = \frac{q \cdot k \cdot T \cdot m_{eff}}{2 \cdot \hbar^3 \cdot \pi^{\frac{5}{2}}} \cdot \int_0^{\Phi_B} e^{-2 \cdot \frac{\sqrt{8 \cdot m_{eff}}}{E_{max} \cdot \hbar \cdot q} \cdot (u + \Phi_B)^{\frac{3}{2}}} \cdot e^{\frac{u}{k \cdot T}} du \qquad u = \frac{\hbar^2 \cdot k_x^{\,2}}{2 \cdot m_{eff}} \qquad 2.24$$

The total current is the sum of the tunneling and thermal currents. In forward bias, an extrinsic series resistance typically limits the measured current. To account for this, the applied voltage is reduced by the product of the current and this series resistance. This results in a set of equations that must be self-consistently solved. This is taken care of in the code for the model, given in Appendix C. A plot of the I-V characteristics of a Schottky diode with a 0.5 V barrier is shown in Figure 2.22. Note the limiting of the current by a series resistance in forward bias, as well as the tunneling current in reverse bias below -3 V.

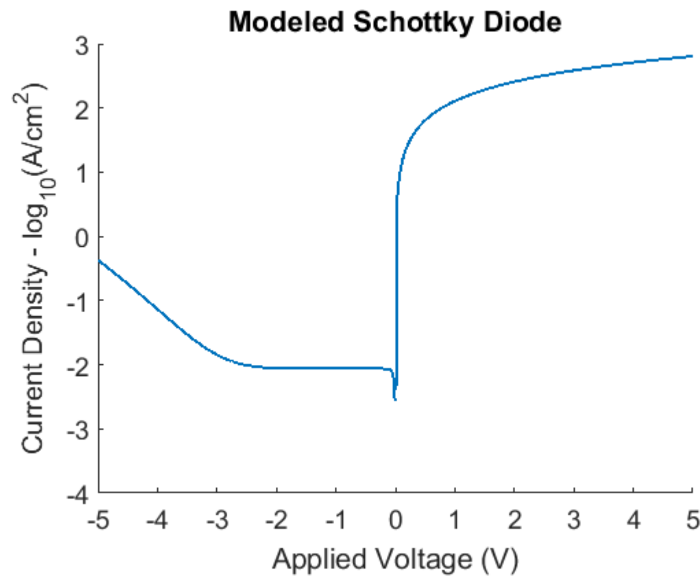


Figure 2.22: Plot of resulting I-V curve for Schottky diode model.

Chapter 3: Processing Modules

It takes several interdependent processing steps to fabricate the VFinMOSFET. The process flow can be split up into modules which can be independently developed before integrating them together. Since the VFinMOSFET was very different than other GaN devices, many of the modules had to be developed from scratch. Also, several pre-existing modules had to be adjusted to be compatible with the remainder of the process. Conditions were determined for each module to be able to work with the process including surface roughness, pattern transferability, and etch selectivity.

The process flow centers around the formation of the gated fin. This begins by creating and patterning an etch mask. Next the unmasked material is etched away leaving only the fins. Damage from the plasma etch must be considered, and damage removal or material recovery may be required. Finally, the gate oxide and metals are deposited, resulting in the desired gated fin structure. The alignment of the source to the top of the fin, and the formation of the insulated probe pads are also significant modules, but they differ depending on the fabrication method used. As such these will be discussed in the integration portion of the dissertation, Chapter 4.

3.1 Regrown GaN Interface

With the expectation of damage to the GaN crystal during etching, experiments were performed to quantify the damage via hall measurements, giving sheet resistance, number of carriers, and mobility. [10] To determine whether the GaN surface was recovered, the mobility of an etched and regrown sample was compared to that which was not etched prior to regrowth. A rectangle of each sample was cleaved, and an indium dot contact was placed in each corner

to prepare for hall measurement. The measurement and value extraction follows that described by van der Pauw [11].

Prior to each regrowth, a cleaning process was used to prepare the sample immediately before loading into the MOCVD chamber. This consisted of a 15 minute exposure in the UV ozone chamber, followed by 1 minute in 48% HF and a DI rinse, repeated three times. Once complete, the sample is then vacuum sealed and handed off for regrowth. This cleaning was inspired by the experiment performed by Chowdhury [12], and was extended from two to three cycles to allow for process variation. The transfer of the samples was coordinated to minimize the time the sample was exposed to air, and possible silicon contamination, as silicon acts as an n-type dopant in GaN. Vacuuming the samples does decrease the rate of silicon surface accumulation.

All the samples that were etched, were etched to a depth of about 500 nm using a Cl_2/Ar etch at 25 W RF bias power, and 100 W ICP source power. A low power BCl_3 pre-etch was used to clean the surface before the Cl_2/Ar etch. 20 nm of AlGaN was grown to create the HEMT structure whose mobility is measured. Some of the experiments add a GaN interlayer before the AlGaN growth. One sample, to be used as a benchmark, was grown from the template to the AlGaN in a single growth. This resulted in a HEMT mobility of 1569 $V \cdot s/cm^2$, which will be taken as the maximum possible mobility to be achieved by these recovery experiments.

3.1.1 Choice of Post-Etch

A post-etch is a low power etch performed after the higher power deep GaN etch before removing it from the chamber, to remove some of the damaged surface. Two possible low power etch chemistries were considered, BCl_3/Cl_2 and Cl_2/Ar. Four samples were prepared and

their mobilities compared, one without etching, one with only the GaN etch, and one for each of the post etch chemistries. The measured mobilities showed that while both post-etches helped recover some of the mobility, the BCl_3/Cl_2 etch gave greater improvement. The experiment was rerun with the addition of a 2 nm GaN interlayer, giving the same conclusion. Table 3.1 describes the conditions and results of both sets of samples.

Etch			Regrowth Layers		Measurements			
HPE	LPE	Depth	GaN	AlGaN	RMS	R_{sh}	n_s	μ_n
		nm	nm	nm	nm	Ω/□	cm^{-2}	$V \cdot s/cm^2$
				20	1.123	614	9.06E+12	1122
Cl/Ar		453		20	0.78	1899	1.26E+13	261
Cl/Ar	BCl/Cl	508		20	0.718	1103	8.86E+12	639
Cl/Ar	Cl/Ar	498		20	0.617	1477	9.41E+12	449
			2	20	1.093	998	7.03E+12	890
Cl/Ar		453	2	20	1.838	1471	1.22E+13	349
Cl/Ar	BCl/Cl	508	2	20	0.639	1101	7.49E+12	757
Cl/Ar	Cl/Ar	498	2	20	1.05	1090	8.09E+12	708

Table 3.1: Regrown HEMT measurements for various LP post-etches.

3.1.2 Pre-Growth Anneal

As an attempt to improve the surface before growth, the samples were annealed prior to growth in NH_3 and N_2 at near growth temperatures. The first series looked at the effect of anneal time on mobility. Table 3.2 shows that the maximum benefit occurs at around 30 minutes of anneal time. This may be due to the GaN decomposing at longer anneal times. Returning to a regrowth with a 2 nm GaN interlayer, the temperature was varied around 930ºC, which is just less than the growth temperature of GaN. Table 3.2 shows that at growth temperatures, the anneal causes the mobility to drop significantly.

Etch				Anneal		Regrowth		Measurements		
Pre-Etch	HPE	LPE	Depth	Time	Temp	GaN	AlGaN	R_{sh}	n_s	μ_n
			nm	min	°C	nm	nm	Ω/□	cm^{-2}	$V\cdot s/cm^2$
BCl	Cl/Ar	BCl/Cl	447	20	930	0	20	982	8.60E+12	739
BCl	Cl/Ar	BCl/Cl	447	30	930	0	20	813	8.9E+12	863
BCl	Cl/Ar	BCl/Cl	447	40	930	0	20	1007	9.23E+12	672
BCl	Cl/Ar	BCl/Cl	447	30	930	2	20	830	8.168E+12	921
BCl	Cl/Ar	BCl/Cl	447	30	910	2	20	955	8.43E+12	775
BCl	Cl/Ar	BCl/Cl	447	30	950	2	20	1595	9.373E+12	417

Table 3.2: Regrown HEMT measurements for various anneal conditions.

3.1.3 GaN Interlayer Thickness

A thickness of 2 nm for the GaN interlayer was chosen since most of the charge in the 2DEG should be contained in the first 2 nm. This would allow the electron gas to reside in regrown material, which may be of significantly better quality than that which remains after the deep GaN etch. The interlayer thickness was varied from 0 to 10 nm, and the resulting mobilities are plotted in Figure 3.1. The values are grouped by GaN on sapphire template as it had been found that the mobility may be dependent on the template and must be compared to like samples for a valid conclusion. The figure show that between 2 and 4 nm, the mobility improves significantly, nearly approaching the benchmark value of 1569 $V\cdot s/cm^2$. Increasing the interlayer thickness to 10 nm does not provide further improvement to the mobility.

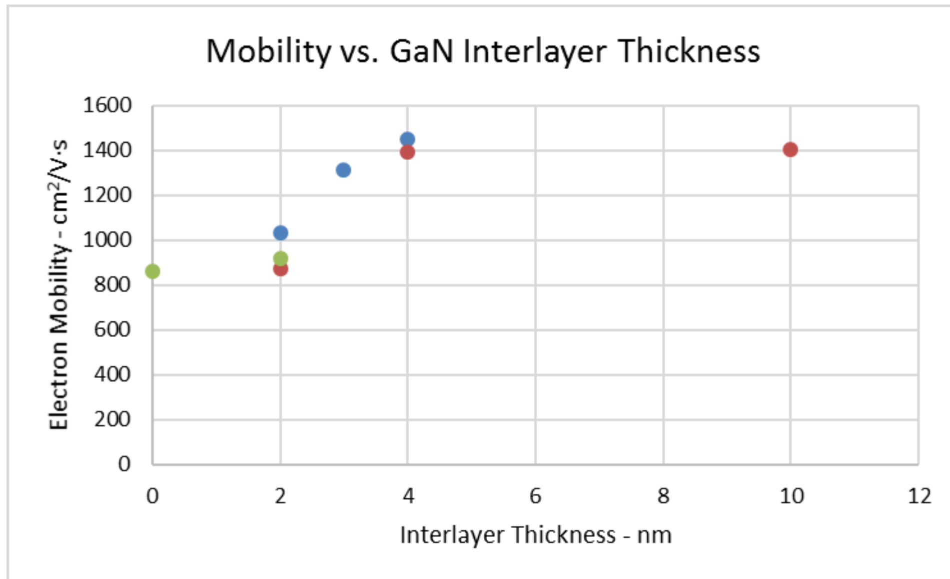


Figure 3.1: HEMT mobility recovery for various GaN interlayer thicknesses as part of regrowth.

3.2 Deep GaN Etch

To form the fins, a deep vertical GaN etch that results in low damage and low roughness is required. Remaining damage can be removed via additional processing, but if the extent of the damage is too high, low defect surface material may not be recoverable. Low roughness is required for good coverage when depositing additional material on the sample, such as in regrowth or oxide deposition. Previously developed etches in the facilities available at UCSB did not meet the requirements for deep etches in the range of 2 to 4 µm. As such, a new etch process was developed on the ICP to reach these depths based on the etch chemistry described by Nedy et al.. [13] The Cl_2/Ar etch was developed and optimized via several series of etches varying the conditions in the etch chamber and comparing the resulting surfaces. [14]

3.2.1 Experimental Process

Samples consisted of epitaxially grown 4-6 µm Ga-face GaN on 2 inch sapphire (0001) wafers by metal organic chemical vapor deposition, MOCVD. The roughness of the unetched

GaN was approximately 0.23 nm rms. The wafers were each cleaved into six pieces before processing.

Before processing, all samples were cleaned in an ultrasonic bath in acetone and isopropanol for 3 minutes each, and rinsed in de-ionized water. Either a photoresist or hard mask was defined on the samples. For samples with a photoresist mask, they underwent a dehydration bake before coating, exposing, and developing the resist. The resist used was SPR 220-7.0 coated to a thickness of 7.9 μm and patterned with an i-line stepper. For samples with a hard mask, 50 nm of SiO_2 was first deposited via plasma enhanced chemical vapor deposition, PECVD, to provide a barrier layer to prevent metal contamination. Then the samples were cleaned again and patterned with nLOF 2020 before 10 nm of titanium and 180 nm of nickel were deposited via an electron beam evaporation and lift off procedure. Titanium was used as an adhesive layer to the oxide. Nickel was chosen for its low etch rate in Cl_2/Ar in comparison to GaN. [15] These samples were then etched using CHF_3 to remove the exposed SiO2 before the deep GaN etch.

All etching was performed using a Panasonic E626I ICP etching system. This system allows for the changing of both the RF bias power and the ICP source power. The gas flows and the chamber pressure can also be modified. Throughout the experiment, the ratio between the RF and ICP powers was kept at 1:4. In addition to varying the powers, the total gas flow, the ratio of the gasses, and the chamber pressure during etching was also varied for the experiment. The samples were mounted on a 6 inch silicon wafer before loading into the etching system.

Analysis of the samples included atomic force microscopy (AFM) to measure the roughness of the etched lateral surface. This also provided information on pit size and density.

Roughness values are reported for scans of 10 x 10 μm^2 areas unless otherwise specified. Scanning electron microscopy (SEM) was used to measure etch depth and sidewall angles, as well to observe sidewall roughness and large pillar and pit formation. A Dektak profilometer and a confocal microscope were used to confirm the etch depth in addition to AFM and SEM. Photoluminescence (PL) was used to detect changes in the crystal quality near the surface by measuring samples before and after etching.

For each variable experiment series, pieces from the same two inch wafer were used and measurements were made in the center of each piece. This was done in order to insure that variations in growth between samples did not affect conclusions made about the effects of parameters on the resulting etch.

3.2.2 Bias and Source Power Variation

For When varying the bias and source powers, the etch time for each was set such that the etch depth reached approximately 2 μm. This is done to reasonably compare results of etches with different rates. As seen in Figure 3.2, as the power increases, the etch rate increases linearly for the range tested. In addition, the surface roughness decreases with increasing power for equivalent etch depths. These results are in contrast with results from Hahn et al. [16] which may have compared different powers for equal time. They show that increasing the source power alone increases the roughness, whereas changing the bias power alone did not affect roughness. Instead the experiment shows that increasing both the source and bias powers simultaneously resulted in lower surface roughness. Figure 3.3 shows the features that contribute the most to the surface roughness. Morphology change from ridges to pits can be seen for samples etched at 200 W and 400 W ICP power, respectively. For the lowest power of 100 W, relatively large hills form with peaks on the order of 40 nm. For all further

experiments, an ICP source power of 300 W and RF bias power of 75 W is used. This power, in between the highest two powers in this series, does not form ridges or hills, and has smaller pits. For this series, flow rates of 20 sccm each of chlorine and argon were used at 1 Pa.

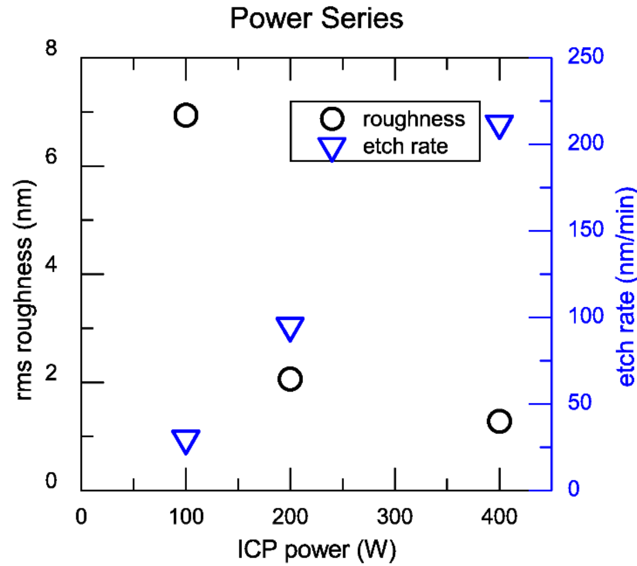


Figure 3.2: Comparison of roughness and etch rate for increasing ICP source power. Note that the RF bias power is set to 25% of the source power. The roughness presented here is calculated from 2 μm x 2 μm AFM scans.

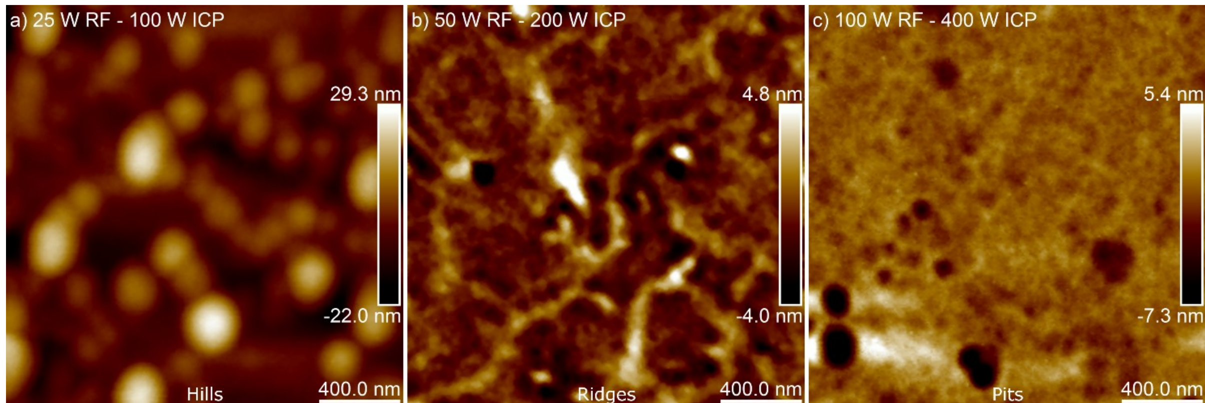


Figure 3.3: 2 μm x 2 μm AFMs showing the surface features of the lateral etched regions for the various powers tested.

3.2.3 Gas Flow and Pressure Variation

The total gas flow rate was changed from 20 sccm to 60 sccm while keeping the Cl_2/Ar ratio at 1:1. Figure 3.4 shows SEM and AFM micrographs for various flow rates. As the flow

rate increases, the size and density of pits decrease, leading to decreased surface roughness. These trends are shown in Figure 3.5. This indicates that gas flow rate is a major factor for improving the smoothness of the surface. In order to differentiate the contributions of the individual gasses, the ratio of Cl_2 and Ar was varied as well, while keeping a constant total flow rate of 40 sccm. From the same wafer as the total flow rate variation series, one piece was etched with 30/10 sccm Cl_2/Ar, and another with 10/30 sccm Cl_2/Ar. Figure 3.6 show that with increased argon content, the pit size increases, and appears to also impact the nickel masking the surface. With increased chlorine content, the pits become much smaller and the roughness decreases to approximately 1.48 nm rms at an etch depth of 3.4 μm. It is suspected that while the argon is useful to provide physical etching as a compliment to the reactive etching of chlorine, a large ratio of argon with respect to chlorine creates too much physical etching, especially along dislocations which expose loose bonds, forming pits.

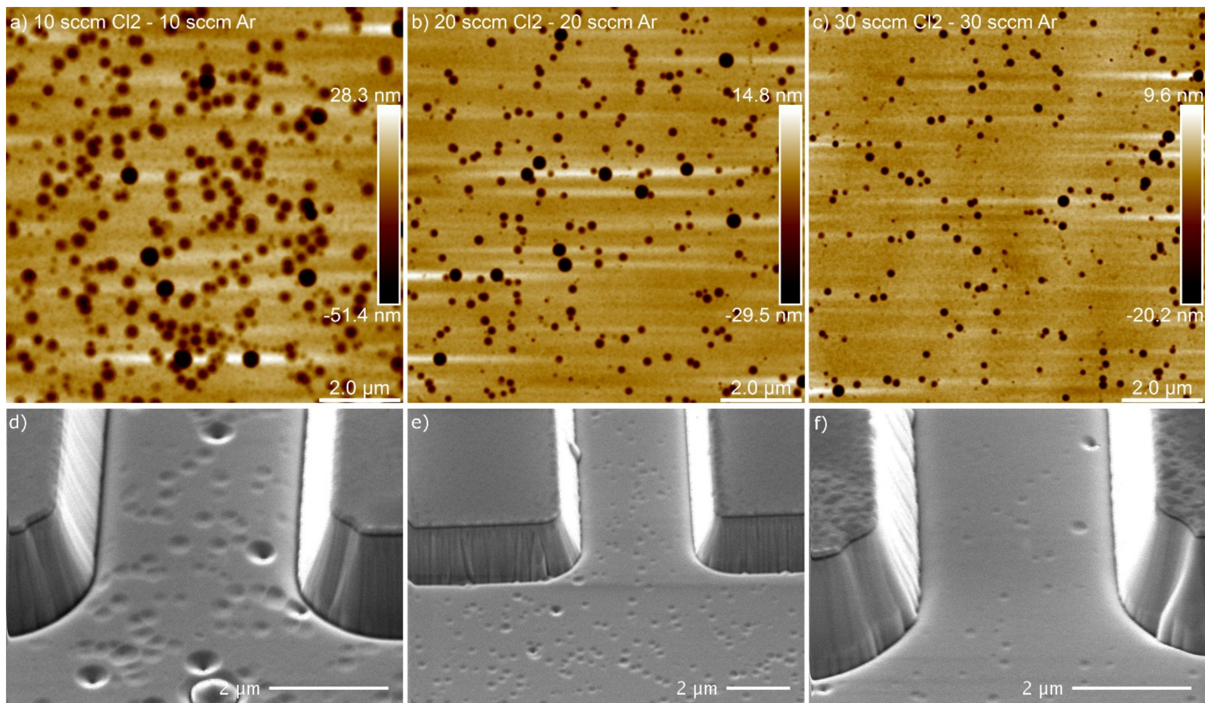
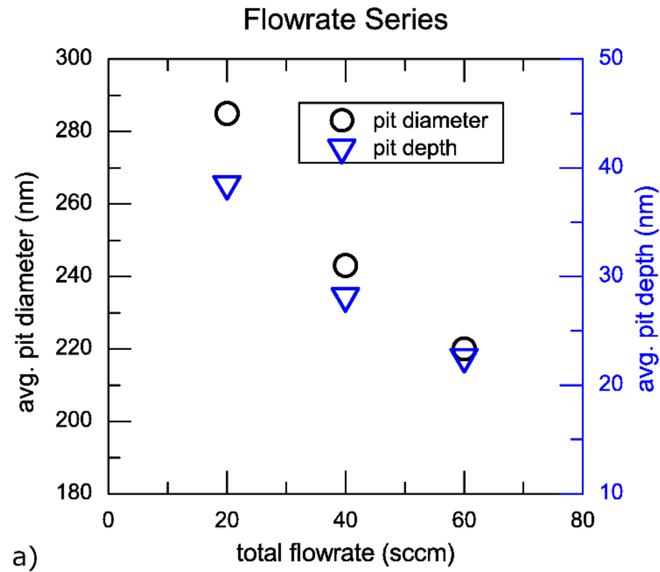


Figure 3.4: a-c) 10 μm x 10 μm AFM scans of flow rate variation series. d-f) SEMs of the same samples.



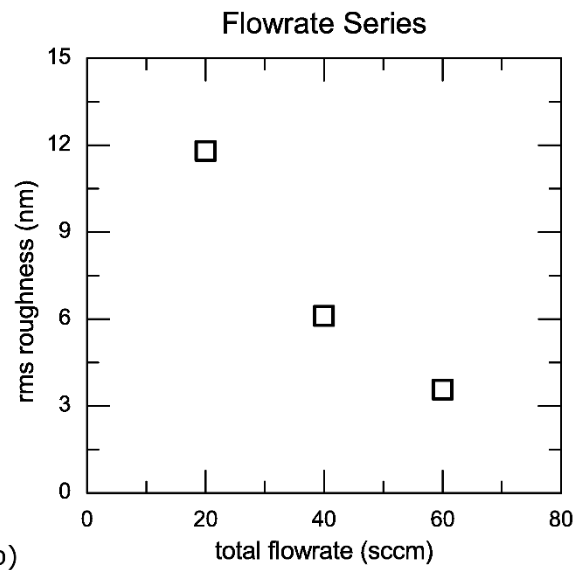


Figure 3.5: Comparison of pit dimensions and roughness for varying total flow rate. The ratio between Cl_2 and Ar was kept constant at 1:1.

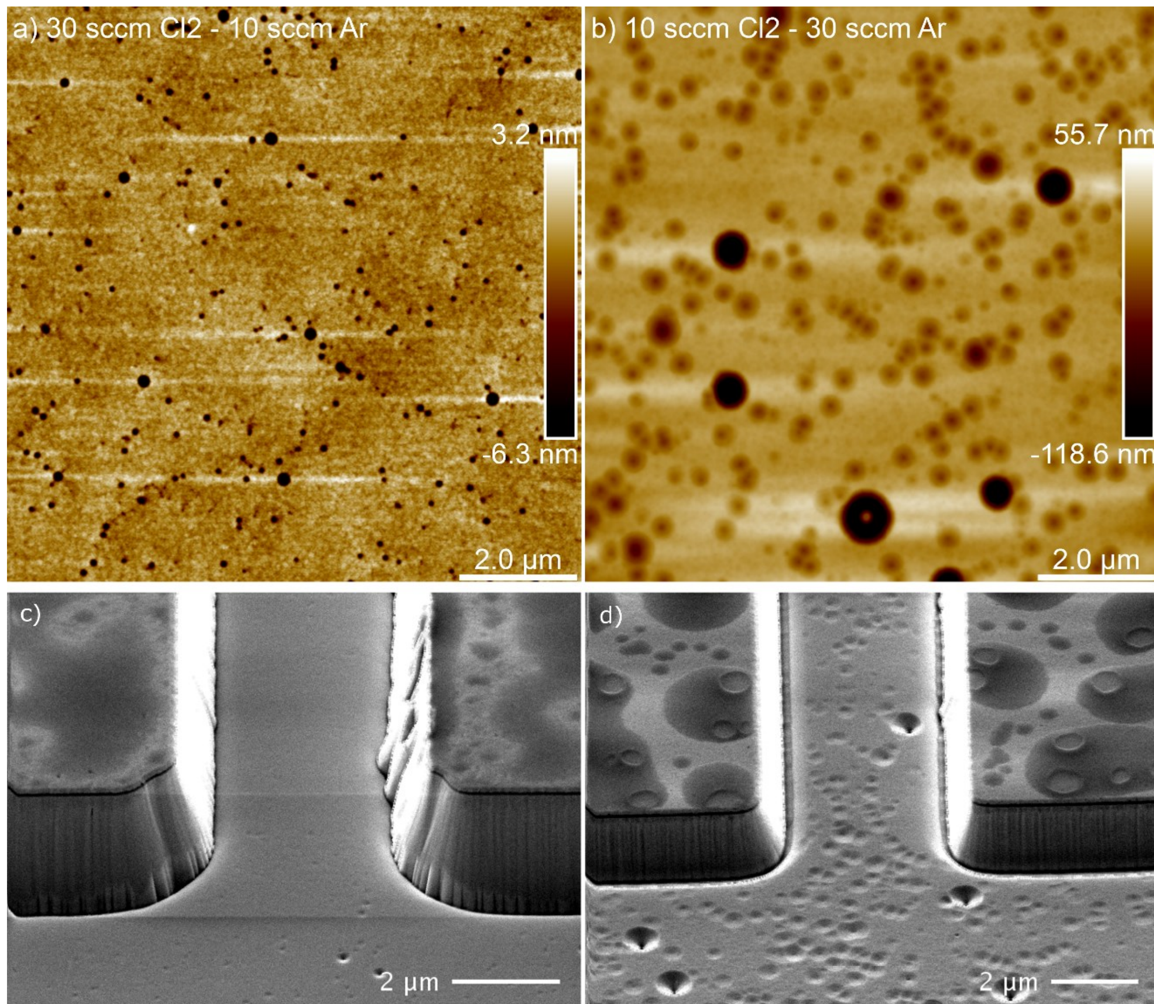
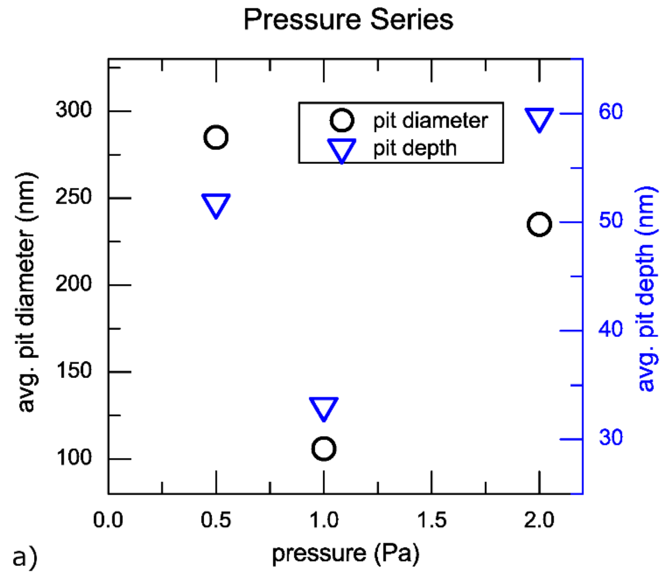


Figure 3.6: a-b) 10 µm x 10 µm AFM scans of gas composition variations. c-d) SEMs of the same samples.

To determine the effect of chamber pressure on etching, three etches were performed with pressures of 0.5 Pa, 1 Pa, and 2 Pa. Figure 3.7 shows that the surface roughness was lowest at 1 Pa. It appears that at lower pressures the surface forms ridges, while etching of pits increases at higher pressures, as shown in Figure 3.8. Consequently, 1 Pa was used as the chamber pressure during the Cl_2/Ar etch for the rest of the study.



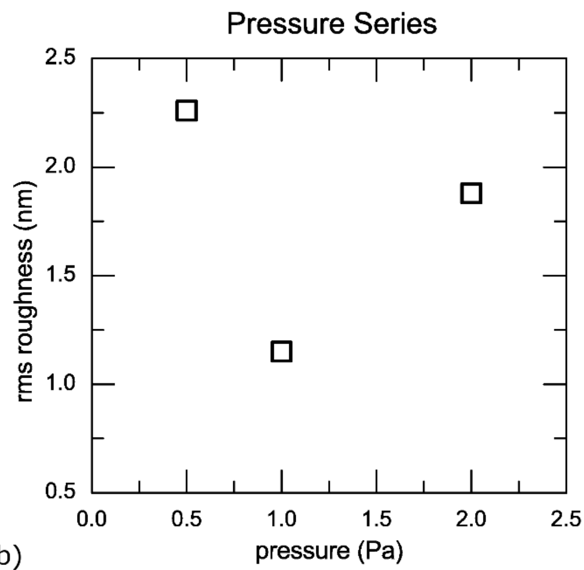


Figure 3.7: Comparison of pit dimensions and roughness for varying pressure.

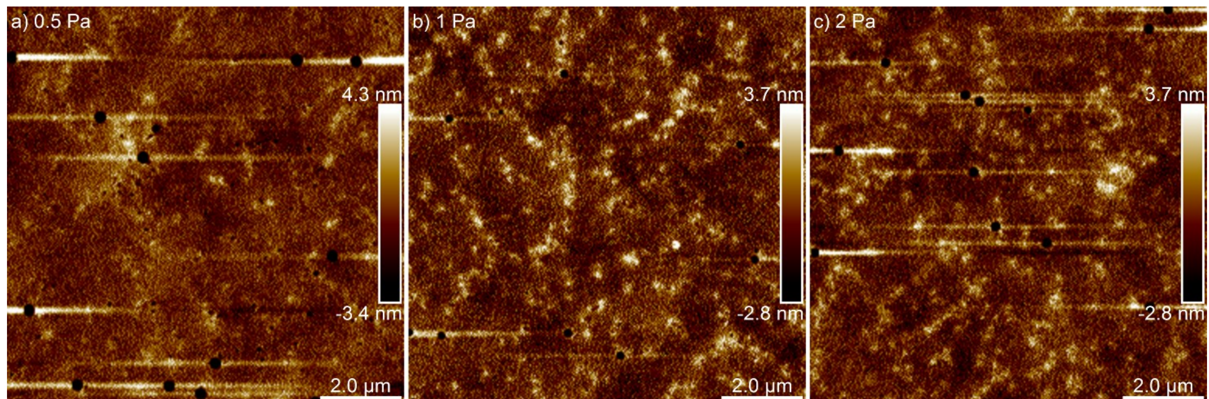


Figure 3.8: 10 µm x 10 µm AFM scans of pressure variations.

3.2.4 Post-Etch Effect on Photoluminescence

In order to evaluate crystal damage near the surface, photoluminescence measurements were performed on samples before and after etching. In addition, some samples were subjected to a very low power BCl_3/Cl_2 post-etch of varying times. Bias and source powers of 15 W and 50 W respectively were used with flow rates of 20 sccm and 5 sccm for BCl_3 and Cl_2 respectively at 2 Pa. An etch rate of approximately 10 nm/min was measured. This post-etch was intended to remove damaged material without causing more damage. By varying the post-etch depths, the depth of the damage from the Cl_2/Ar etch should be able to be determined.

To measure photoluminescence, a 325 nm wavelength HeCd laser with a penetration depth of about 995 Å was used to excite the states near the surface of the GaN. However, when this was done, the post-etch decreased the PL intensity significantly more than the Cl_2/Ar etch alone. Figure 3.9 shows that the GaN peak decreases by 32% after the Cl_2/Ar etch, and an additional 23-39% more so with the post-etch. This gives evidence that the Cl_2/Ar etch causes less damage to the crystal near the surface than the low power BCl_3/Cl_2 etch per time. The decrease in photoluminescence intensity due to the Cl_2/Ar etch is much less than that of the BCl_3/Cl_2 etch described by Qui et al. [17] Further investigation is required to determine the electrical properties of the etched GaN, as well as the sidewalls.

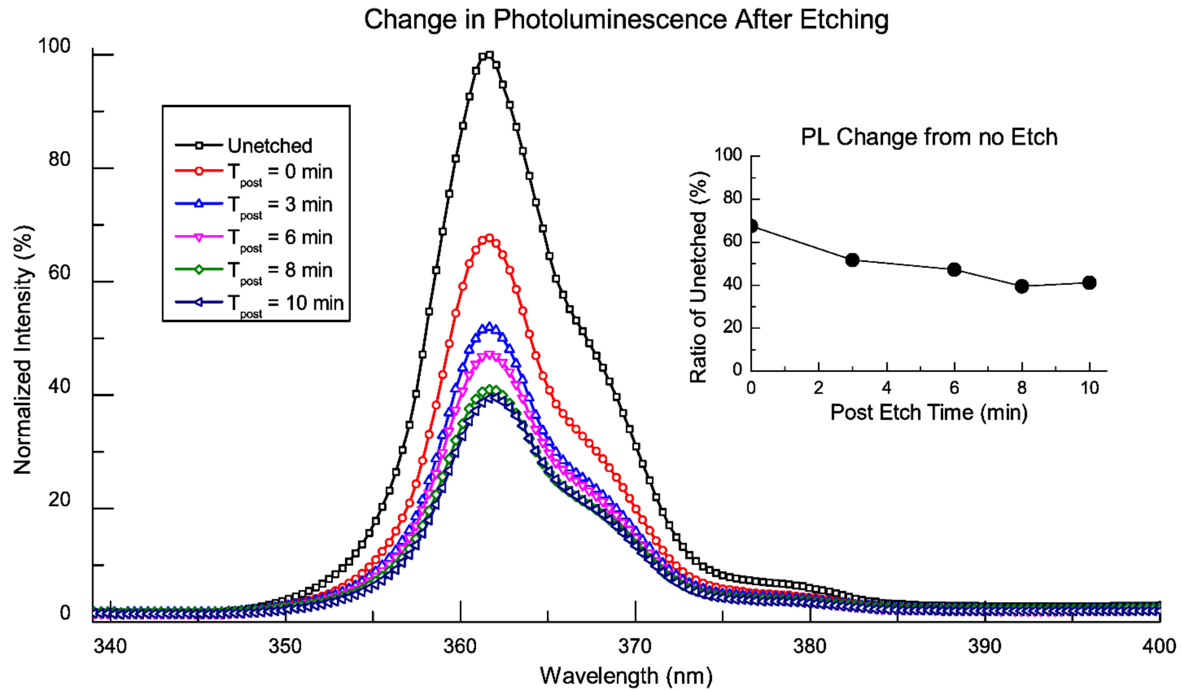


Figure 3.9: Comparison of photoluminescence of Cl_2/Ar etched samples with different post-etch times and an unetched sample as a reference. The peak value of the GaN peak at 365 nm was used to calculate the PL change.

3.3 Hard Mask Development

The choice of a hard mask affects many aspects of the process. The fin pattern is transferred to the sample via the hard mask definition. The process to form the hard mask must maintain as well as possible, the clear lines as they are lithographically exposed on the sample. Also important in the formation of the mask, the surface that will be etched must be free of contamination and residue. In addition, during etching, the ions may sputter portions of the hard mask leading to micromasking or contamination of the etch surface. This could also affect the angle of the etched structures via other affects such as charges in the etched sidewall affecting the trajectory of ions to the surface.

Several possible etch masks were explored, many of which resulted in useful processes. Unfortunately, depending on the requirements for fabrication, some mask processes may not

be suitable. Of importance is the compatibility of materials used in the hard mask stack in later process steps as well as the ability to remove portions or all of the hard mask without removing other materials on the sample that need to remain.

3.3.1 Photoresist vs. Ni Hard Mask

Photoresist is a very convenient etch mask to use since the pattern is exposed directly into the mask layer. However, one of the main downsides is a poor etch ratio with GaN for deep etches. This means that a very thick resist is required to be able to withstand the high power etch. Also, during the etch cross-linking due to the ion bombardment will harden the resist and make it very difficult to remove afterwards. An alternative, whose process is described in Section 3.2.1, was developed and compared to results from the photoresist mask.

Initial etching of samples with an SiO_2/Ti/Ni hard mask resulted in approximately 1 micron high pillar formation as seen in Figure 3.10. It was suspected that even after the CHF_3 etch to remove SiO_2 in exposed regions, some residual material remained which acted as a micro-mask during the Cl_2/Ar etch leading to these large pillars. To confirm, two samples were etched with different masks, one with SPR 220-7.0 photoresist, one with Ti/Ni as the mask without an SiO_2 interlayer. Both the photoresist and Ti/Ni masked samples showed no pillar formation, while the control sample with an SiO_2 interlayer continued to show the same pillar formation. This confirms that the SiO_2 interlayer was causing the micro-masking, and that nickel sputtering was not the cause.

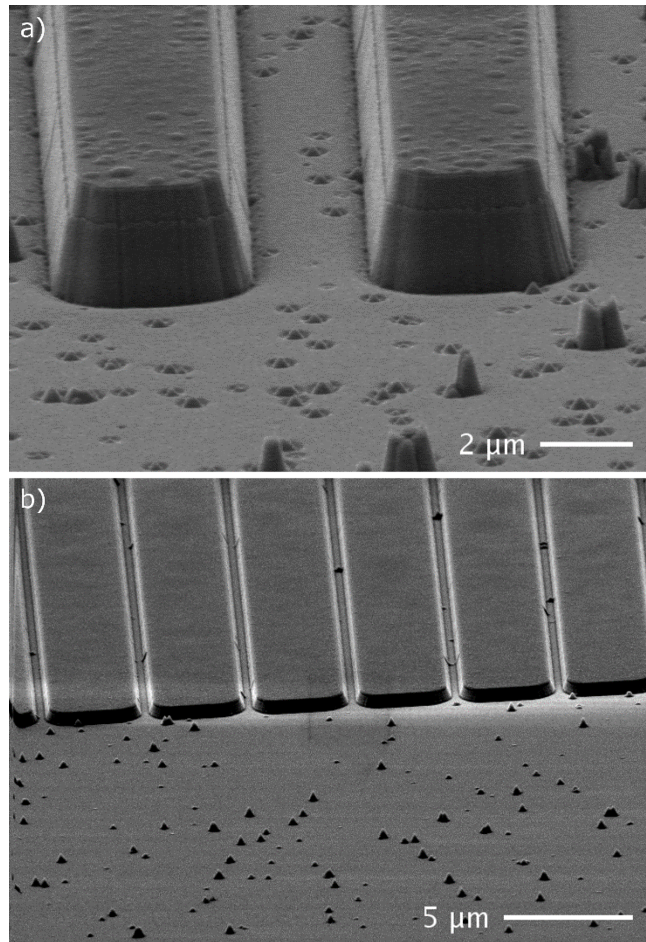


Figure 3.10: SEM images of pillars formed during the etch when a mask with SiO_2 contacting GaN is used.

An SiO_2 interlayer may be required to protect from metal contamination. In order to keep the SiO_2 as part of the hard mask process, a BCl_3 pre-etch similar to that used by Nedy et al. [13] was developed to clean the GaN surface before the Cl_2/Ar etch, but after the CHF3 etching of the oxide. The pre-etch conditions used were 10 sccm of BCl_3 at 1.33 Pa with ICP power of 200 W, RF power of 40 W, for 6 minutes. This was found to be sufficient to prevent the micro-masking that led to pillar formation. Figure 3.11 shows an SEM micrograph of the etch using an SiO_2/Ti/Ni hard mask leading to 1.07 nm roughness and 13.2^{o} sidewall angle from vertical. In addition, Figure 3.12 shows the final etch using SPR 220-7.0 as the mask, also utilizing the pre-etch for only 100 seconds. This etch had an angle of 7.6^{o}, with rms roughness of 0.831 nm

at an etch rate of 201.8 nm/min. Throughout the study, it was found that using a photoresist mask consistently improved the verticality of the etch over the use of a hard mask. Measurements of the patterned resist gave resist angles of 2.5° from vertical and an etch rate of about 400 nm/min, twice that of the GaN. In comparison, the nickel has been measured to have an etch selectivity of 1:30 with respect to GaN. It is important to note that the Ni must be removed prior to additional processing as sputtered Ni residue may result in undesired connections. This has been done by bathing the sample in the HNO_3 based Ni Etchant TFB from Transene. [18]

As predicted earlier, the photoresist left residue at the edge of the pillars due to cross-linking from the ion bombardment which conventional resist strippers could not remove. To remove the residue, the samples were dipped piranha, 3:1 H_2SO_4:H_2O_2, for five minutes. Piranha is typically used to etch away organics and would be ideal to remove remaining photoresist. The electrical measurements of capacitors however gave indication that the piranha may be causing surface contamination. Figure 3.13 shows the C-V curve for a device with a piranha exposure step. These samples were regrown Al_2O_3 MOS capacitors with a 4 nm GaN interlayer. It appears that the GaN will not deplete more than the first 4 nm if exposed to piranha, implying that fixed charges have been introduced at the regrowth interface. The lack of a good method to remove the strongly cross-linked resist leads to the need to use a hard mask.

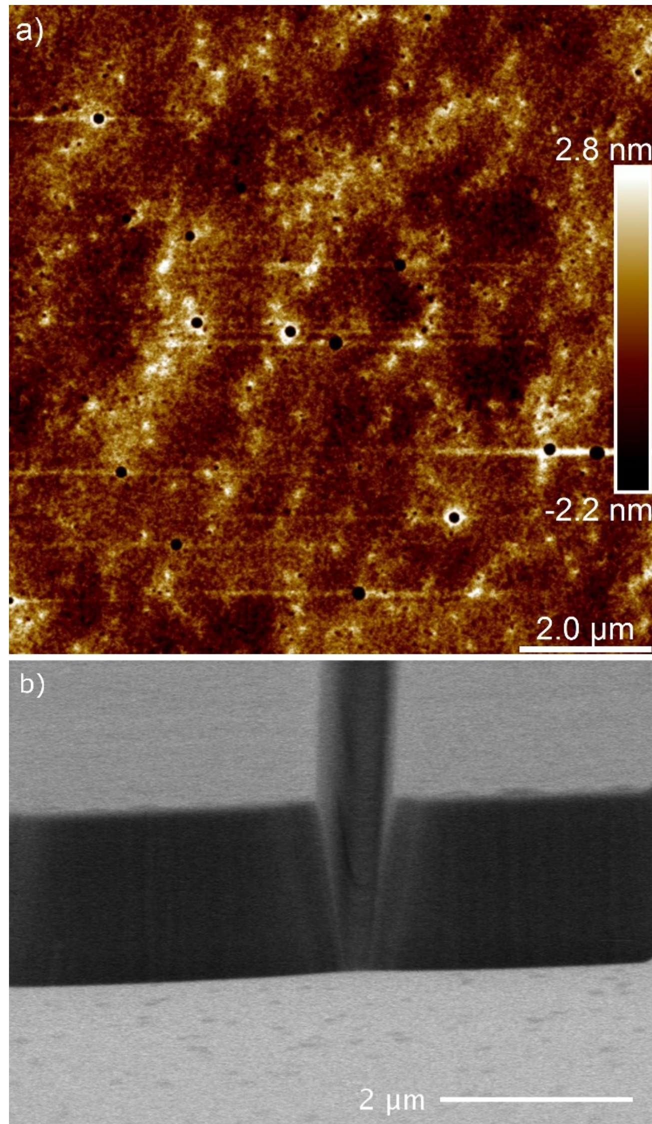


Figure 3.11: AFM and SEM of sample etched with an SiO_2/Ti/Ni hard mask using an optimized Cl_2/Ar etch with a BCl_3 pre-etch.

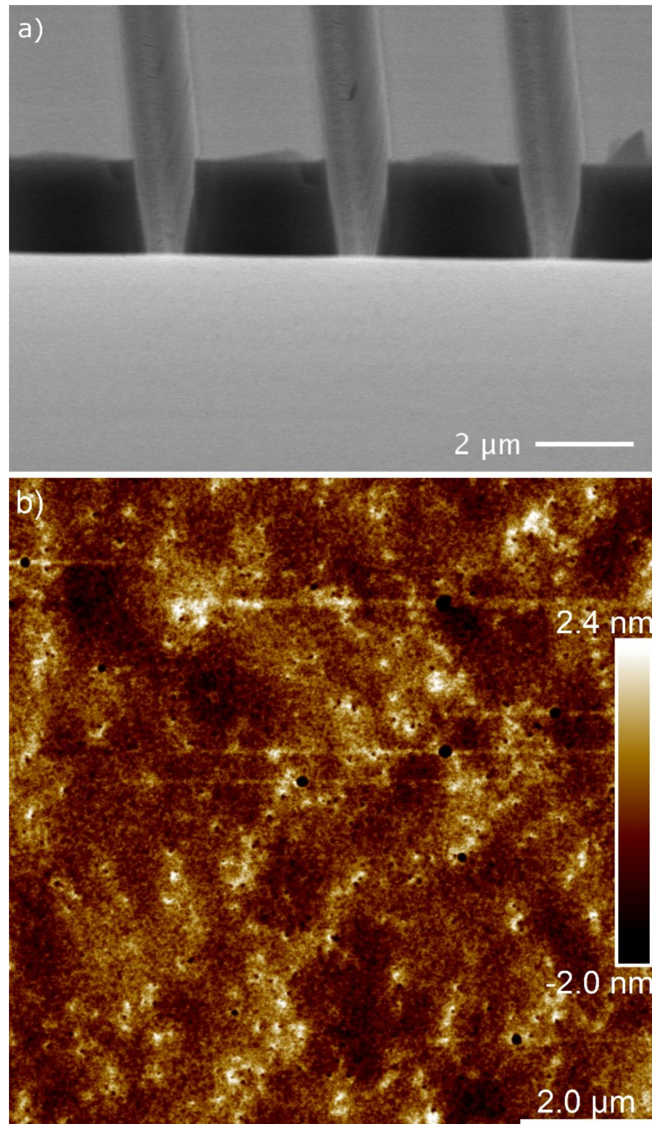


Figure 3.12: AFM and SEM of sample etched with an SPR 220-7.0 photoresist mask using an optimized Cl_2/Ar etch with a BCl_3 pre-etch.

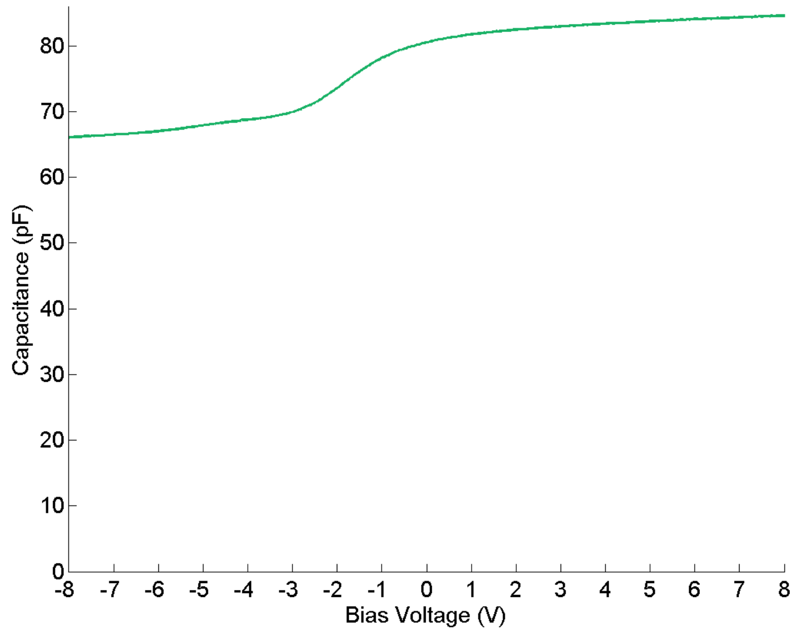


Figure 3.13: Regrown Al_2O_3 MOS capacitor C-V with piranha exposure before growth.

3.3.2 Source-First Tungsten Mask for High-T Regrown Oxide

While the Ni etch mask process is sufficient for most deep etches, development of a self-aligned process required that the source metal be part of the hard mask and remain during oxide deposition and the remainder of the process. Tungsten was chosen as the source metal as it has the closest workfunction to the electron affinity of GaN of the refractory metals at around 4.5 eV, resulting in about a 0.4 eV barrier. In addition to the use of tungsten as the first layer of the mask, SiO_2 spacers was used to protect the metal inside the MOCVD chamber.

The process flow is illustrated in Figure 3.14. On top of the n+ GaN layer, deposited in order are: 1500 Å of tungsten by e-beam deposition, 10 nm of Al_2O_3 by ALD, and 100 nm of SiO_2 by PECVD. The sample is patterned with SPR 955-0.9 with LOL 2000 as an underlayer, and 1800 Å of nickel are deposited by e-beam and lifted off leaving the fin pattern. The lower layers of the mask are etched by CHF_3/CF_4 for the SiO_2, AZ300 MIF for the Al_2O_3, and SF_6/Ar

for the tungsten. To form the spacers, 50 nm of PECVD SiO_2 is deposited, and then anisotropically etched in CHF_3. This forms the mask used during the deep GaN etch, after which the Ni is removed using TFB.

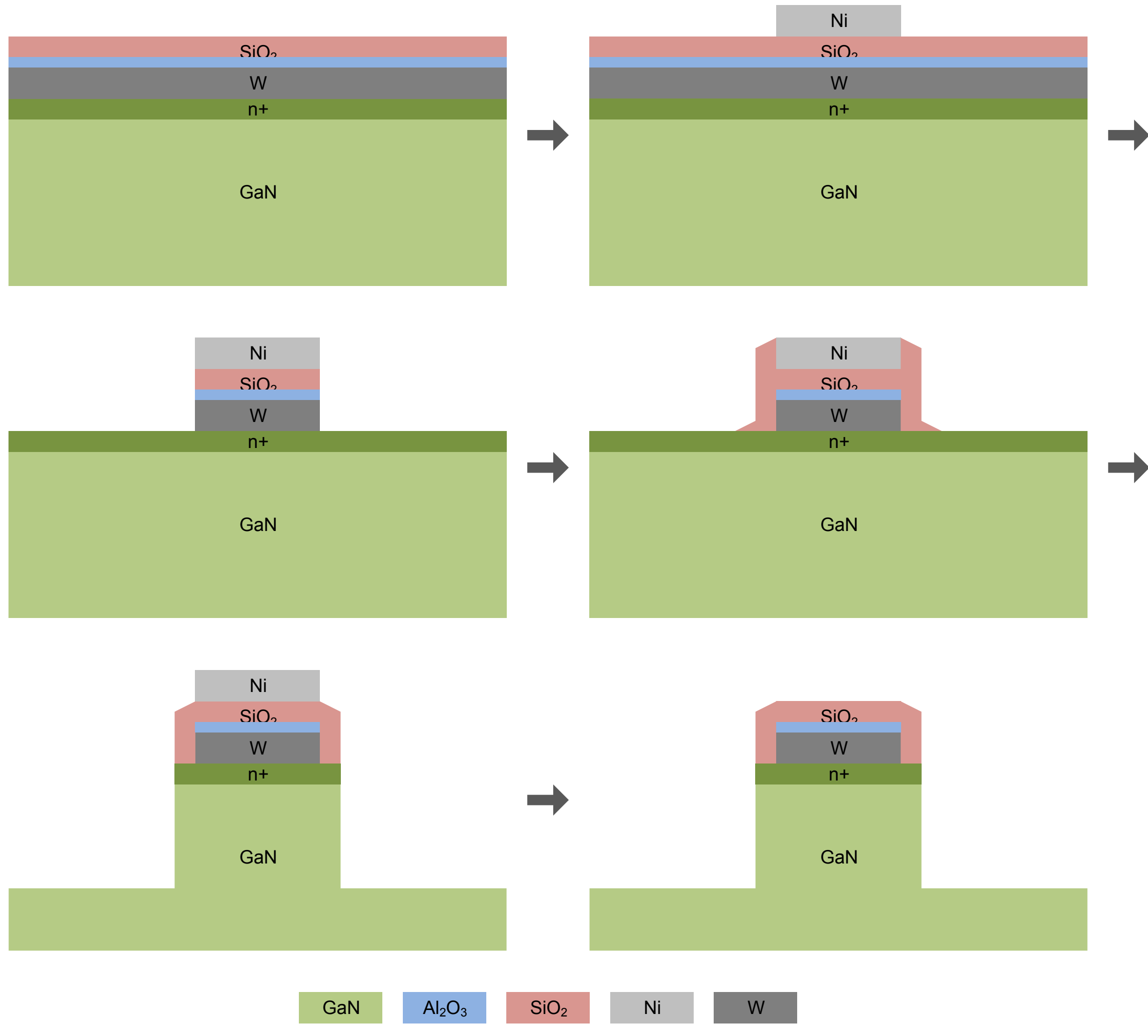


Figure 3.14: Hard mask process flow with a tungsten source contact first layer and SiO_2 spacer.

This process was designed such that a source metal remains in contact with the n+ GaN at the end. The source metal is chosen to be refractory in order to be able to withstand the high temperatures in the MOCVD during GaN and Al_2O_3 regrowths. The spacers act both to insulate the source metal and to prevent GaN interlayer regrowth along the top of the fin. Al_2O_3 acts as an etch stop for the SiO_2 etch so that the surface of the tungsten is smooth before it is etched.

Figure 3.15 shows the hard mask after the tungsten is etched before the spacers are formed. The etches somewhat roughen the definition of the fin edges. In addition to the roughened edges, it is suspected that the Ar in the W etch causes the pitting seen in the Ni which is the topmost layer.

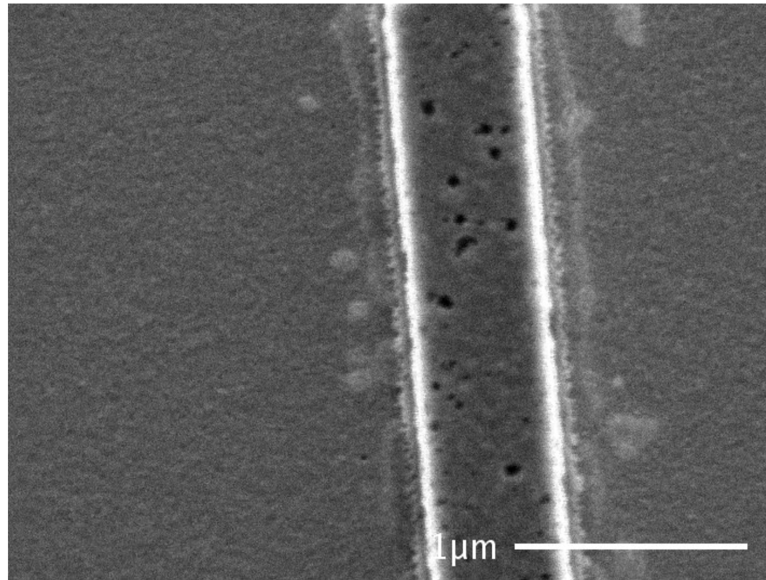


Figure 3.15: SEM of W-source hard mask after W etch and before spacer deposition.

3.3.3 Hard Mask with a Titanium Source

We decided to move away from a high temperature oxide to increase the parameter space on the hard mask process and improve on the fin definition. With an ALD oxide, the sample sees a maximum temperature of 300ºC for the entirety of the fabrication. The space of metals that are compatible with the process increases, allowing for better choices as far as etch selectivity and workfunction. With the intention of using TMAH to remove the etch damage from the sidewalls, the source metal needs to either be fully protected or not etch in the basic solution. It is well known that TMAH etches aluminum rapidly, so while aluminum would be an almost ohmic contact, it would complicate the process in trying to add several spacers to protect it from etching.

The move away from a spacer process is influenced by the desire to simplify the fabrication steps and to allow for smaller fin dimensions. With a spacer, the fin width increased by twice the spacer thickness from the patterned nickel width, as well as decreasing the verticality of the sidewalls. Removing the spacer from the process should result in narrower and more vertical fins. The choice of Ti is due to its workfunction of 4.33 eV, which is an improvement on tungsten, and the fact that it is very susceptible to etching in Cl_2/Ar. This however limits the use of HF in further processing as it will rapidly etch away the metal.

As an initial attempt at a Ti source metal, an all metal etch mask was tried. This would allow for an easy mask formation as all the metals would be defined by a single liftoff. The stack, Ti/Pt/Ni with thicknesses 100 Å/500 Å/1500 Å, would continue to use Ni as the etch mask. The metals however had a lot of strain and peeled off the sample during lift off, seen in Figure 3.16. This was repeated with thinner metals, and while this did improve the sticking, it was not enough. An oxide layer between the metals would relax the strain between layers, so the SiO_2 returned to the process. Additionally, as seen in Figure 3.15, the Ni is susceptible to damage and sputtering during the ICP etches. To prevent this, a move was made towards using a thick PECVD SiO_2 as the mask during the fin etch. Ni is still used to pattern the mask layers but is removed just prior to the deep etch.

Figure 3.16: Delaminated all-metal hard mask.

This simplified process flow with Ti as the source metal is shown in Figure 3.17. The process flow begins similarly to the tungsten-source process, but with a much thicker SiO_2. The following layers are deposited: 1500 Å of Ti by e-beam, 30 nm of ALD Al_2O_3, and 1600 nm of PECVD SiO_2. The SiO_2 is sufficiently thick to remain after the GaN etch. Then the sample is patterned using SPR 955-0.9 with LOL 2000 as an underlayer, and 1800 Å of Ni is deposited by e-beam and lifted off as it was described for the tungsten-source process. The SiO_2 is etched by a very vertical CHF_3/CF_4 ICP that stops on Al_2O_3, seen in Figure 3.18. The increased thickness of Al_2O_3 accounts for an increased absolute error in the etch time. The Al_2O_3 is etched by AZ 300 MIF developer, exposing a clean Ti surface as shown in Figure 3.19. With an SF_6 etch, whose development is described in the next section, a smooth GaN surface is exposed with well-defined fins, as shown in Figure 3.20.

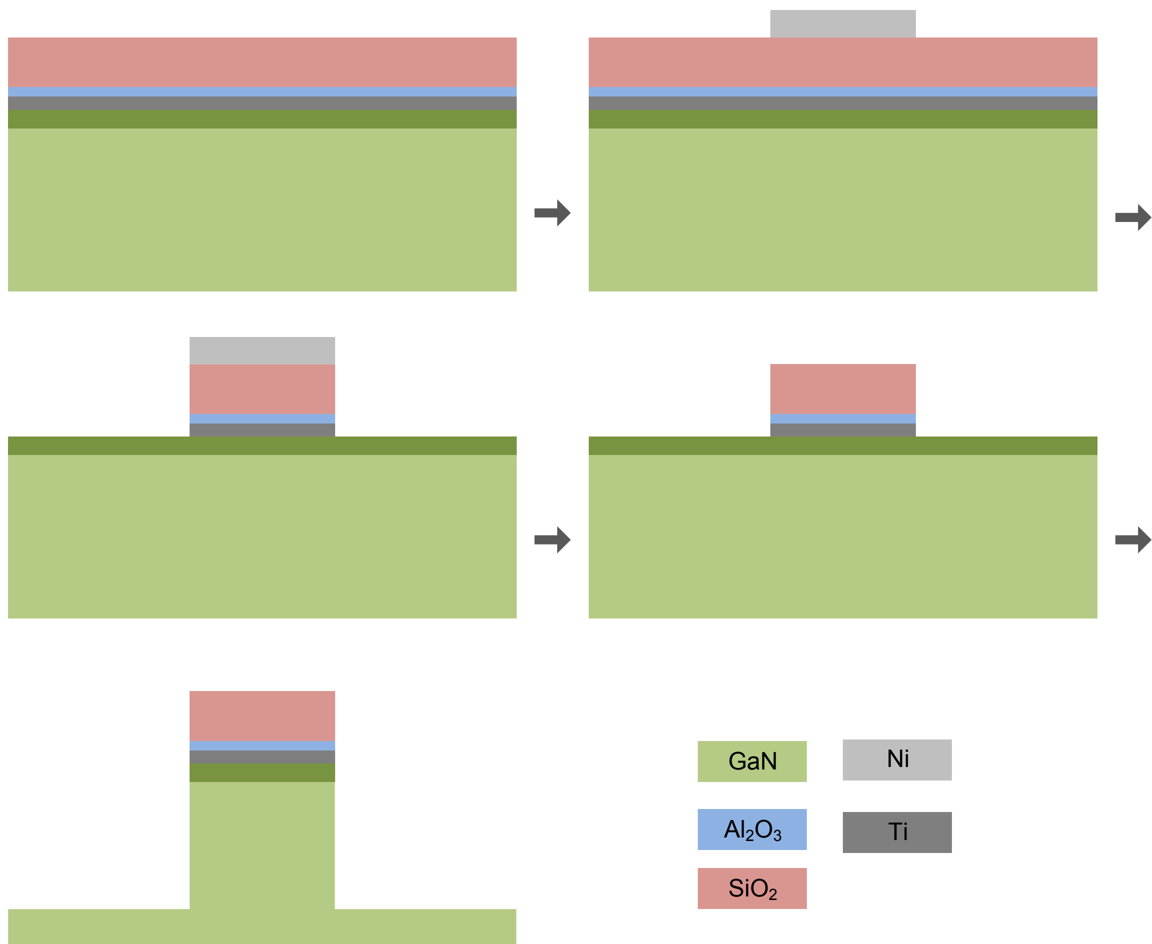


Figure 3.17: Hard mask process flow with a titanium source contact first layer.

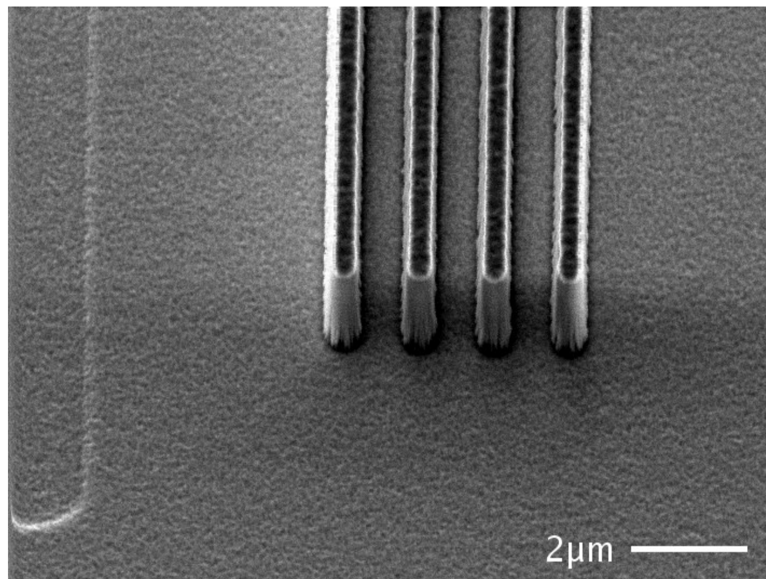


Figure 3.18: SEM of hard mask after SiO_2 etch stopping on Al_2O_3.

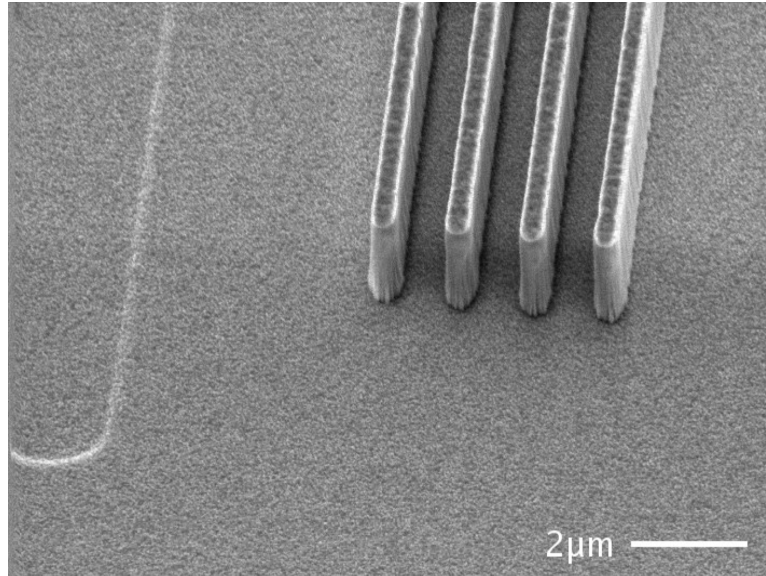


Figure 3.19: SEM of hard mask after wet etching of Al_2O_3.

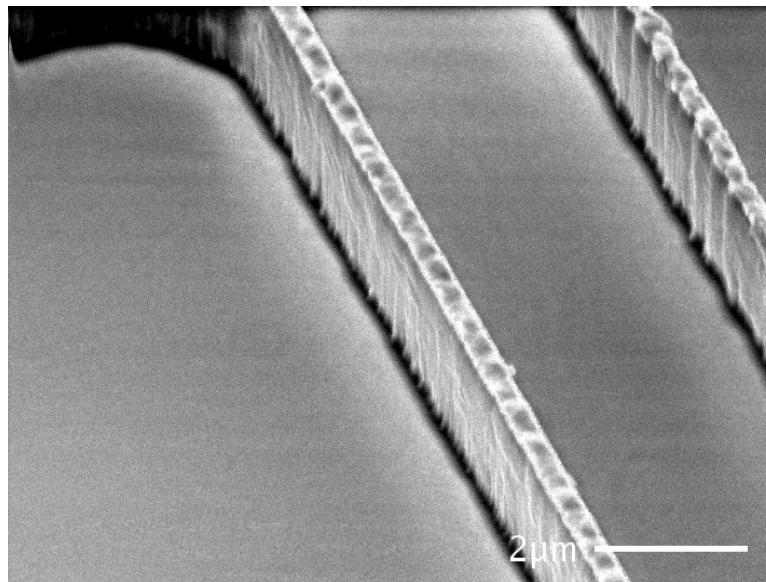


Figure 3.20: SEM of complete Ti-source hard mask for the GaN fin etch.

3.3.4 Titanium Dry Etch

The development of the Ti-source hard mask requires a vertical Ti etch that is selective against GaN. The primary etching ions in an ICP system are typically Cl or F. As the chlorine is a chemical reactant with GaN, a fluorine etch is desired to ensure selectivity. Conveniently,

the Cl_2/Ar etch used for the GaN etch results in a very fast vertical titanium etch. [19] While it cannot be used as a selective etch, this ensures that Ti sputtering will not micro-mask the surface, and will not undercut the Ti.

Belt [20] had previously developed a vertical SiO_2 etch using a Ti hard mask. This etch, using $CF_4/CHF_3/He/O_2$, showed a consistent etch rate of 55 nm/min of the Ti. This was used as the first candidate for a Ti etch. The gas flows were $CF_4/CHF_3/He/O_2$ at 35/35/50/1.4 sccm at a pressure of 0.25 Pa, and 1000 W source and 300 W bias powers.

As an alternative, a much lower power etch was developed using only SF_6 as an etching gas. This was developed on a different ICP system, whose chuck is set to 100ºC as opposed to 50ºC. This is because the partial pressure at 100ºC of TiF_4 is just greater than the minimum pressure of 0.1 Pa for the system, extrapolated from experimental data. [21] This allows the TiF_4 to evaporate without any additional ion bombardment, such as Ar, O, or He. The conditions of the etch were 50 sccm of SF_6 at 0.1 Pa with 75 W source and 25 W bias power. This resulted in an etch rate of about 75 nm/min. While this etch is much slower, it is expected to have a much higher selectivity against GaN and should leave an undamaged surface.

Figure 3.21 and Figure 3.22 show the Ti-source hard mask with the $CF_4/CHF_3/He/O_2$ and SF_6 Ti etches respectively. From the images, the former etch appears to cause some roughening of the GaN surface. The roughened surface appears to follow along crystal plane directions and is an indication that it is highlighting defects in the GaN. This does not appear in the latter etch, indicating that the low power SF_6 etch does not visibly affect the GaN surface. After this comparison, the latter etch is deemed to be more appropriate for the fabrication requirements.

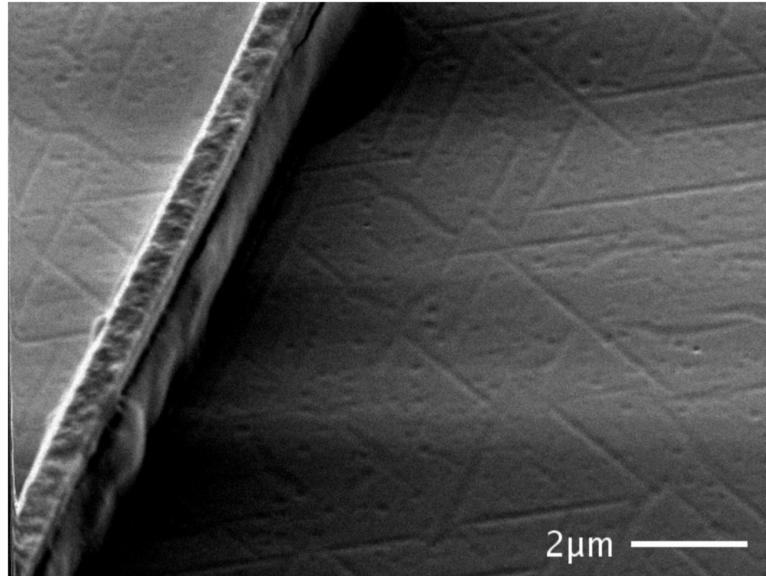


Figure 3.21: SEM of Ti-source hard mask with CF_4/CHF_3/He/O_2 Ti etch.

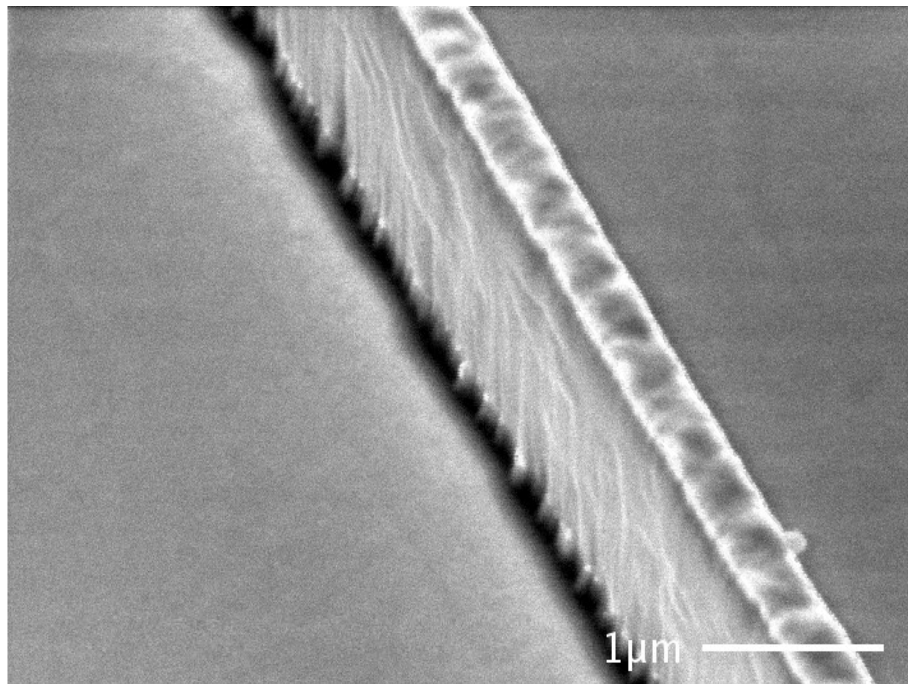


Figure 3.22: SEM of Ti-source hard mask with SF_6 Ti etch.

3.4 TMAH Etch

Measurements of devices fabricated using the tungsten-source hard mask and MOCVD oxide regrowth showed debilitating memory effects. The device would only pass current from

source to drain if the gate had never been charged. More details on the results are in Section 5.2. This implies a very large trap state density at the GaN surface after etching. The remaining etch damage on the surface must be removed before oxide deposition. As c-plane GaN has very few wet etches, hot TMAH presents itself as the only candidate that is compatible with the fabrication process. Simple testing with Ti and SiO_2 films indicate that TMAH at 85^oC does not appreciably etch either film. This confirms the compatibility of the etchant with the rest of the process. The use of TMAH on etched GaN had previously been demonstrated to improve leakage along damaged sidewalls [22] by removing damaged material.

3.4.1 Anisotropic Etching of GaN

TMAH, tetramethyl ammonium hydroxide, acts as an anisotropic etchant on GaN. By testing several samples in the chemical, the effect on the different planes can be observed. Each sample was placed in >80^oC TMAH for 30 minutes or when it appeared by SEM that the etching had stopped on a plane. It was measured by glass thermometer to ensure that the solution reached the desired temperature. The temperature measured by the hot plate is much higher than the liquid in the beaker. To improve thermal conduction, a small pool of water was placed between the beaker and the hot plate.

Using the fin layer pattern, samples underwent the Ti-source hard mask process followed by a deep etch for 12 minutes resulting in 2.5-3 μm tall fins. SEMs were taken before and after the described TMAH bath. Figure 3.23 compares the fin etch before and after TMAH treatment. The vertical ripples seen in the sample post ICP etch appear to have been removed in the TMAH bath. Instead, roughness associated with crystal planes appears on the sidewall, but the fins are much smoother overall. There does not seem to be any visible roughening of the c-plane etched floor.

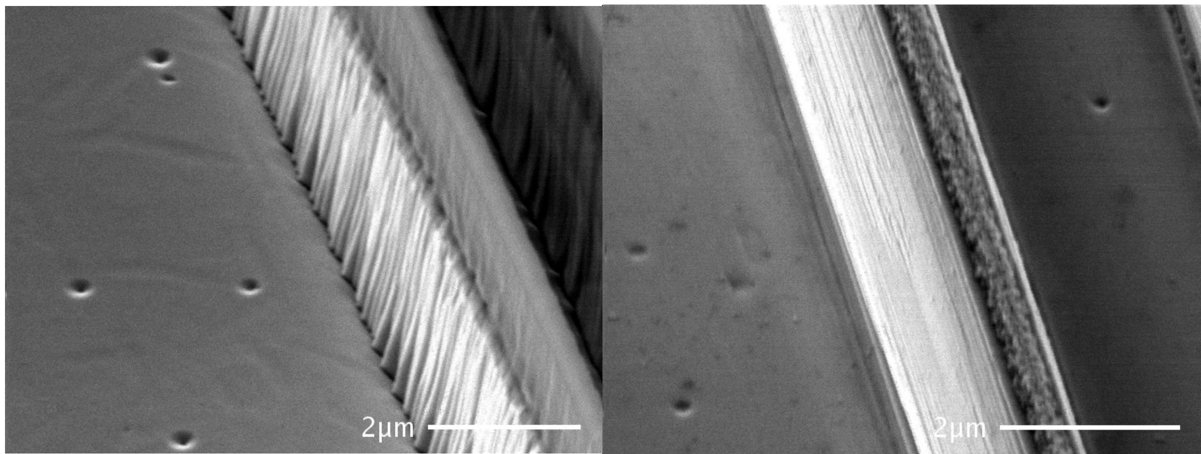


Figure 3.23: SEMs of fin etch before (left) and after (right) TMAH treatment.

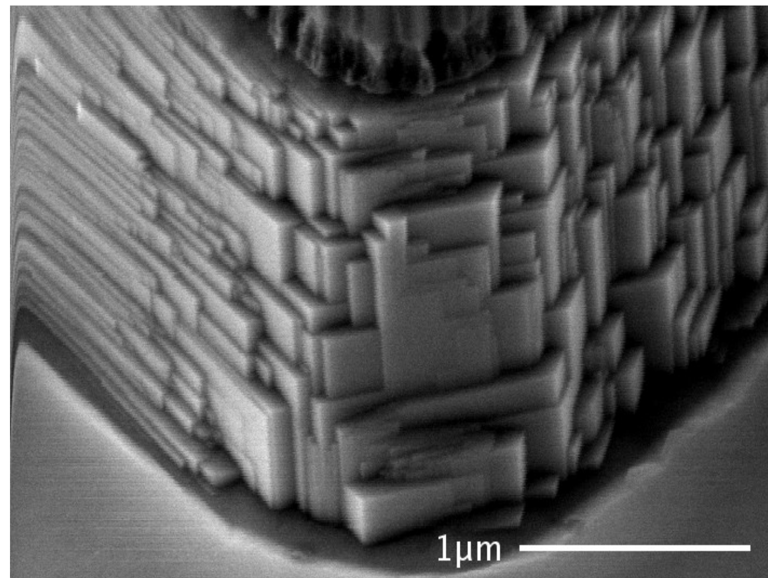


Figure 3.24: SEM of etched GaN structure treated with TMAH showing crystal planes.

The SEM in Figure 3.24 shows that TMAH preferentially stops on specific planes. Knowing the orientation of the sample, and the etched patterns, allows us to identify the exposed planes as m-plane. The figure also shows the importance of the angle of the starting structures before TMAH. With a shallower angle, more faceting occurs as on the left side of the image. Also, the alignment of the pattern to the crystal plane is critical in minimizing the visible roughness seen in the post TMAH bath fin of Figure 3.23.

3.4.2 Etched Surface Roughness between ICP and TMAH

The roughness of the c-plane surface can be characterized by AFM and compared as well. The TMAH treatment decreases the roughness after the ICP etch. The fin fabrication, without TMAH, starts with a very low roughness. With the W-source mask, it is measured to be 3.55 nm rms. After the TMAH treatment, the roughness is 2.34 nm rms. Figure 3.25 shows both AFM scans. The TMAH does not highlight any new features, especially since the ICP etch with optimized conditions and hard mask process does not show many defects or pits. It does remove the mounds seen in the scan from before the TMAH treatment, resulting in the decreased rms roughness measurement.

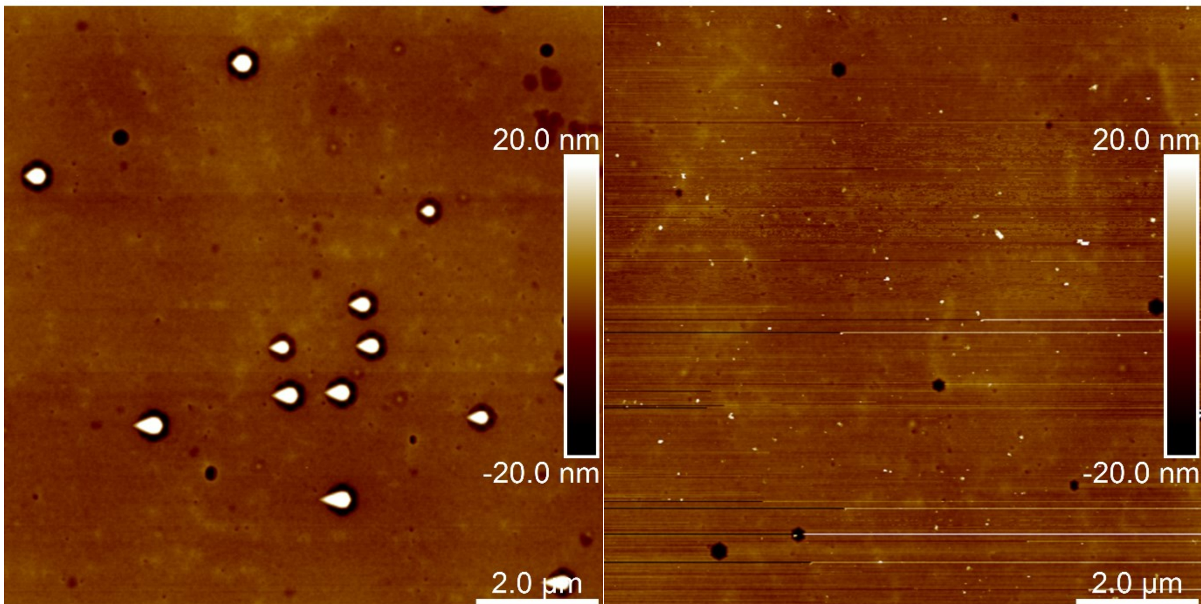


Figure 3.25: AFM scans of etched surface before (left) and after (right) TMAH treatment.

Chapter 4: Process Integration

When developing the full fabrication process for the device, several challenges arose from the interaction of the different process modules. Some of these challenges caused the requirements on the modules to change, and so many of the modules were redesigned several times. In other cases, the entire process flow had to be reworked to get around its limits.

4.1 Mask Pattern Design

When designing a new transistor such as this for fabrication, the process flow and the mask pattern must be developed simultaneously. Changes to the process flow affect the mask pattern, adding new layers, changing what is exposed at various stages. In addition, the mask pattern is effectively a two-dimensional puzzle one puts together to be able to form the three-dimensional structures. The limits of this 2D-3D transformation will force the process flow to adjust so that the 3D structure can be realized.

4.1.1 Transistor Design

The main component of the VFinMOSFET is the fin structures. These should be aligned to the m-plane direction in the GaN. This informs us that the fins must be parallel to each other or 120° apart, however, since that would be crystallographically equivalent, it is easier to have all of them in parallel. The standard length of the fin structures is 50 µm. While the theory indicates that the width of the fins affects the off state performance, several devices of various widths are used. Depending on the iteration of the lithography mask and process flow, the range of widths goes from 300 nm to 8 µm. Figure 4.1 shows the fin layer in an early mask design. Later designs merged the source pad and fin layers.

Figure 4.1: Layout with parallel fins. The solid blue is the source metal, and teal as the fin.

The connection of fins to the source pad varied between designs, but was always placed at one end of the fins. At the other end was the gate pad, which connected to the wrap-around gate. Some form of isolation is to be used under the source pad metal. In some processes, this was implant isolation, while in others it was an oxide. It was not necessary to insulated the gate pad as the metal should be sitting on top of the gate oxide, however early iterations did use additional insulation as a safeguard to leakage through the oxide. To test out the scalability of the process with higher current designs, fins were placed in parallel and connected to the same source and gate pads. Figure 4.2 shows a single transistor with 4 parallel fins demonstrating the scalability of the design. Care was taken to ensure that the un-gated portion of the fin was minimized or eliminated.

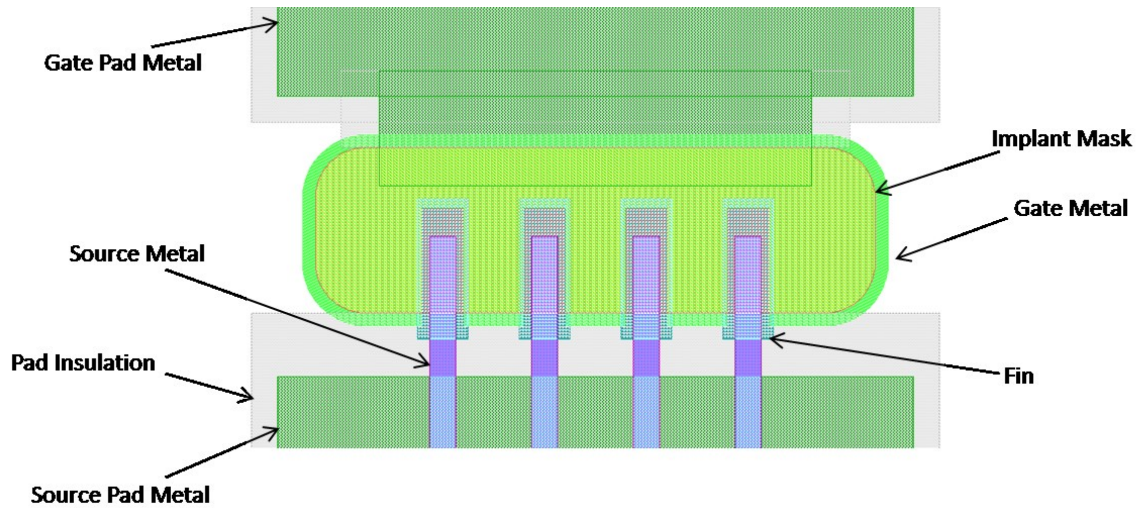


Figure 4.2: Transistor layout including insulated source and gate probe pad connections.

Later designs of the layout merged the patterns of the source and gate pads with their respective metals. This was enabled by changes in the process flow. Additionally, the number of right angles was minimized to proactively improve breakdown performance. The latest design is shown in Figure 4.3. The design of the layout was made using Tanner L-Edit software [23], which allows the use of C++ to create procedurally generated patterns. This was utilized extensively in the design of the mask and the code is in Appendix D.

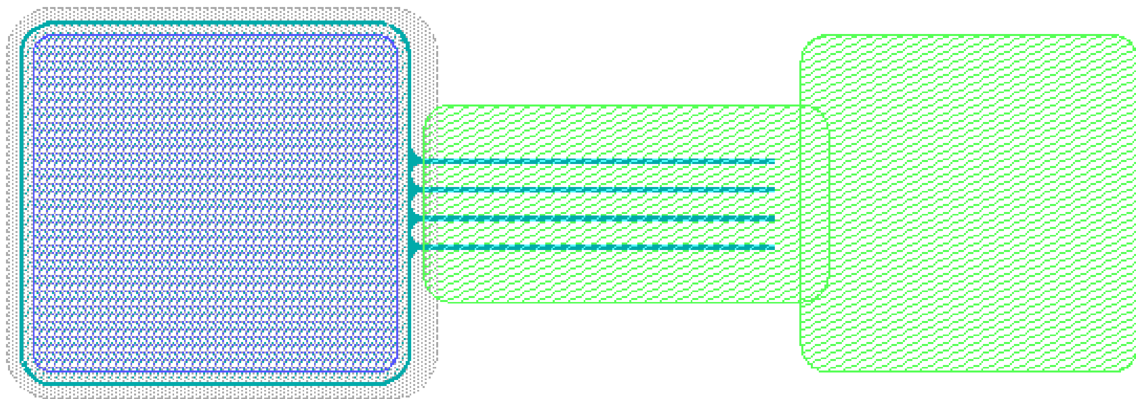


Figure 4.3: Final transistor layout for the VFinMOSFET with a merged source and gated metals and pads, and rounded corners.

4.1.2 Test Structures, Series, and Arrays

Various test structures, that do not consist of transistors were placed in the mask design to characterize specific aspects of the transistor. The same process steps would be used on the test structures as the full devices, giving measurements that can be used as an accurate representation of the corresponding transistor component. There were dummy source and gate pads for pad leakage measurements. Gate-source capacitors measured the gate oxide properties, as well as trapped charges at the regrowth interface. TLM, transmission line measurement, structures were included in the design to determine the ohmic nature of the source contact and measure the contact resistance, and the sheet resistance of the top n+ layer.

To be able to experimentally determine the current spreading in the drift layer, an array of transistors was created that varied the fin width in one direction and the spacing between parallel fins in the other direction. Other series included single-fin transistors with varying widths, as well as varying lengths. One series had devices with 1 to 12 fins. Figure 4.4 shows the locations of the various series and test structures on the final mask design.

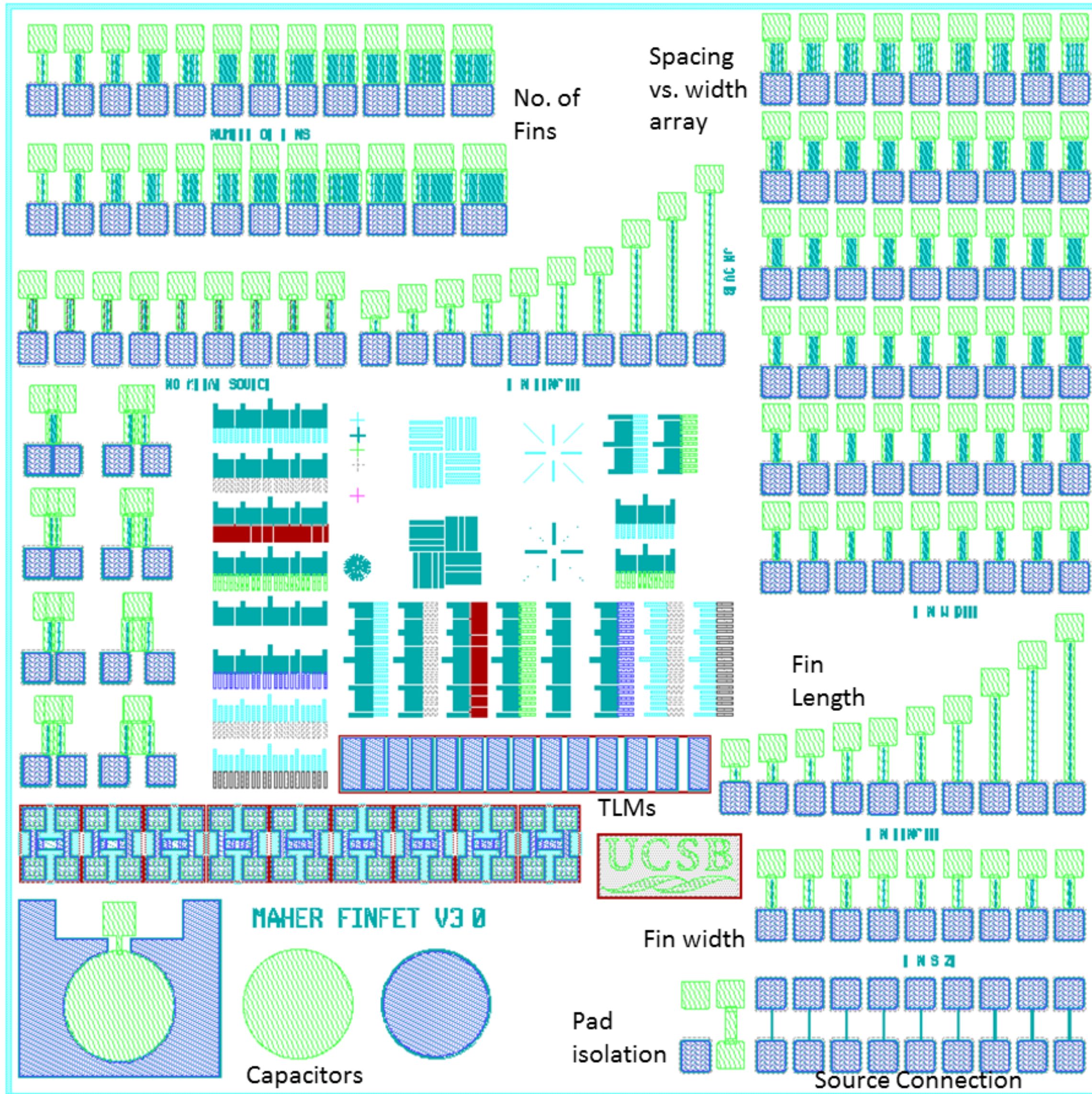


Figure 4.4: Mask pattern showing the various series, arrays, and test structures on the die.

4.1.3 Mask Plate and Lithography

All the layers for the transistor were placed on a single mask plate for each design iteration. Not all locations on the mask plate are equal. Since the UV lamp is centered on the center of the plate in the lithography stepper, there is minor distortion for patterns further from the center. Because of this, layers with very small dimensions and tight alignments should be

placed in or near the center. Extra layers were added to flexibly allow either a positive and negative exposure for most layers.

Additionally, the auto-focus function of the stepper adjusts so that the pattern at the center of the mask would be in focus for each die. This means that off-center patterns may be slightly out of focus, and dies that lie near the edge of the sample may have the focus determined such that it is in focus off the sample. For such layers where one wants to resolve miniscule features, it may be necessary to use manual focus when exposing. The process includes a test pass without exposing a pattern where the sample height is measured and recorded on the stepper screen. In the exposure pass, the height of the optics is manually adjusted to match the values that correspond to the correct location.

4.2 Source-Last Process Flow

Without an expectation of many of the issues that will arise, an initial process flow was designed to fabricate the VFinMOSFET. The process is shown in Figure 4.5, and begins with n- GaN with a 200 nm n+ GaN top layer. The SiO_2/Ti/Ni hard mask is used to etch the fins and subsequently removed in $HF+HNO_3$. The sample is then cleaned with three cycles of UV ozone – HF treatments, and handed off for a 50 nm Al_2O_3 regrowth with a 4 nm GaN interlayer. Then the gate is patterned and metal is deposited conformally on the sides of the fins using planetary rotation in the e-beam. Both platinum and nickel were used as gate metals, with a thicker gold probing layer. Later iterations of this process used 20 nm of ALD platinum to make contact with the gate oxide. This is followed by exposing the top of the fin, removing the gate metal, if any, and the oxide. Lastly, by carefully aligning to this opening, a source metal, typically aluminum or titanium, is deposited.

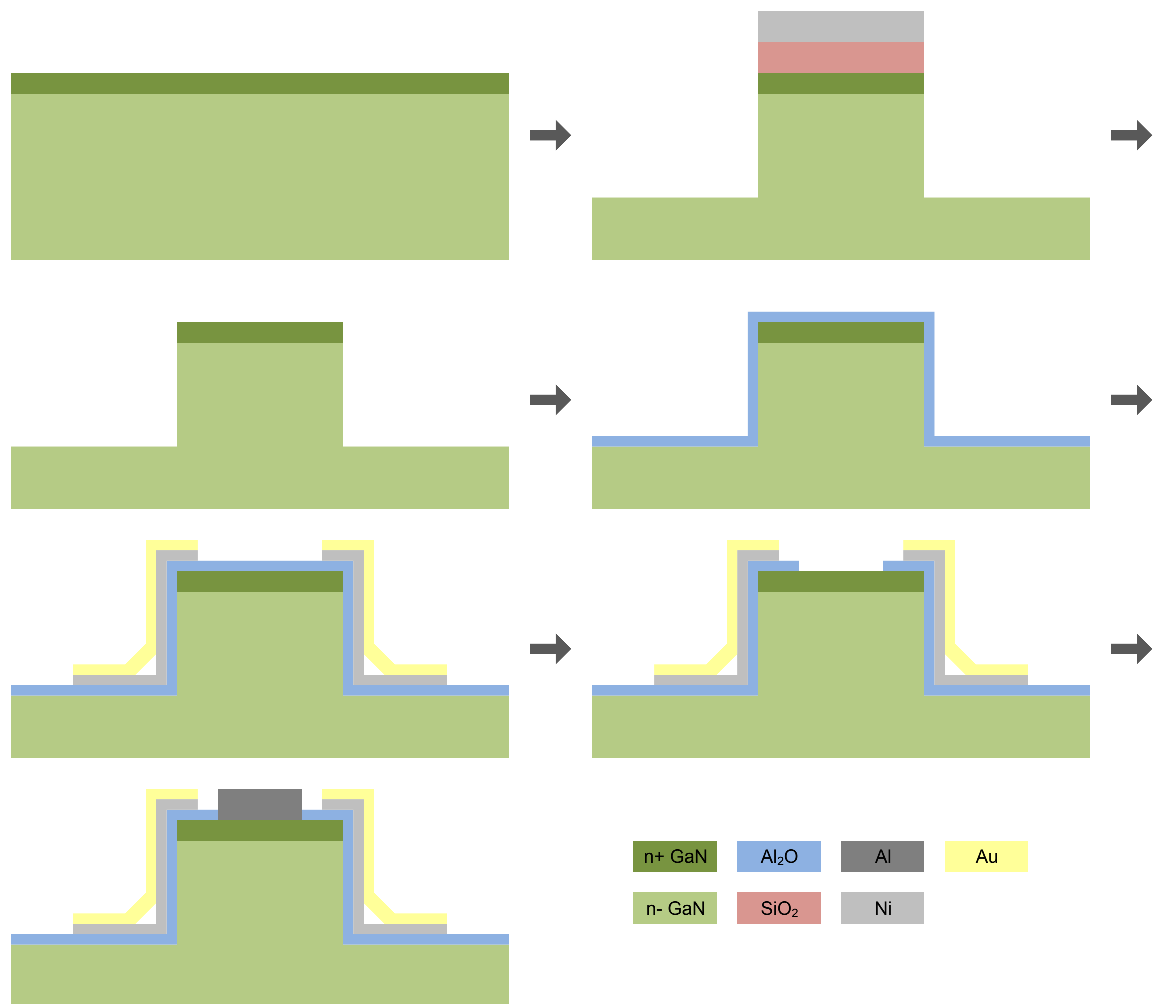


Figure 4.5: Source-last process flow diagram showing the cross section of the fin throughout the process.

This process uses techniques that have been regularly used in GaN processing, or developed and calibrated prior to the design of this process. Unfortunately, many of those standard techniques had not been used on such scales. Metal connections from the top of a mesa to the bottom are common, but not with such verticality, or with heights of about 2 µm. Alignments of layers with such tight tolerances, such as the fin opening, or source deposition to the fin, presented many difficulties. The choice of resist and metal thickness and deposition method became very critical to successful fabrication.

4.2.1 Pad Connection

The first source-first processes called for the source metal to come down the end of one of the fins to an insulated pad at the bottom. The oxide pad extended to the top of the fin to prevent leakage from the source into the center or bottom of the fin. This acted as an oxide bridge for the source to come down. Figure 4.6 shows the process flow for the connection of the source to the pad, including the formation of the oxide bridge.

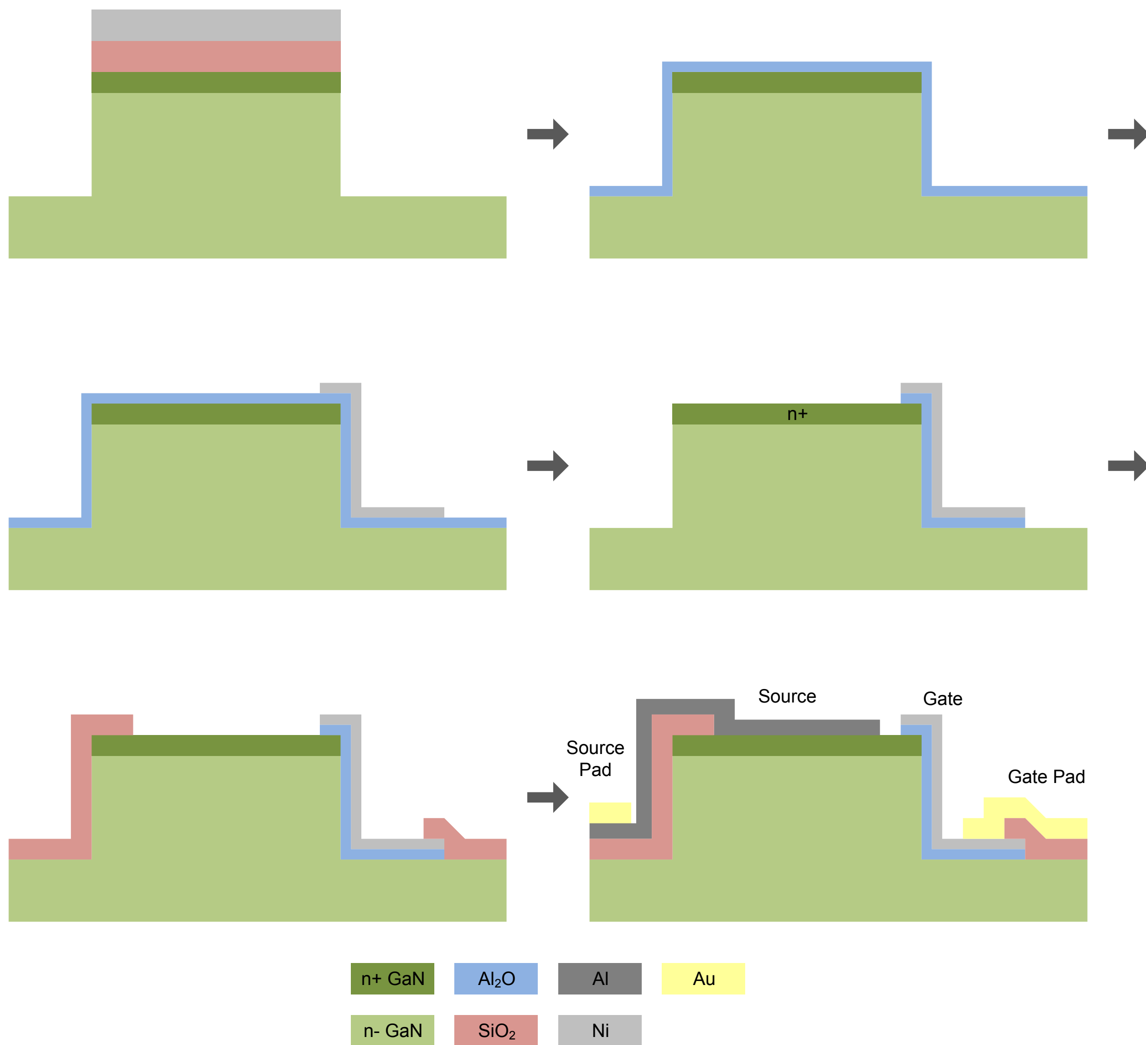


Figure 4.6: Fabrication flow of the pad connections for the oxide bridge source process.

This process also included a connection of the gate to an independently insulated gate pad. Unfortunately, the source and gate metals had trouble connecting over the step formed by the

oxide pads. As an alternative that does not create any steps that the metal has trouble connecting over, implant was used to isolate the gate and source pads. The process flow utilizing implant isolation is shown in Figure 4.7. A 10^{15} cm^{-2} dose of Al was implanted at 90 keV, with a 7° tilt from normal to expose the source end of the fin to the implantation.

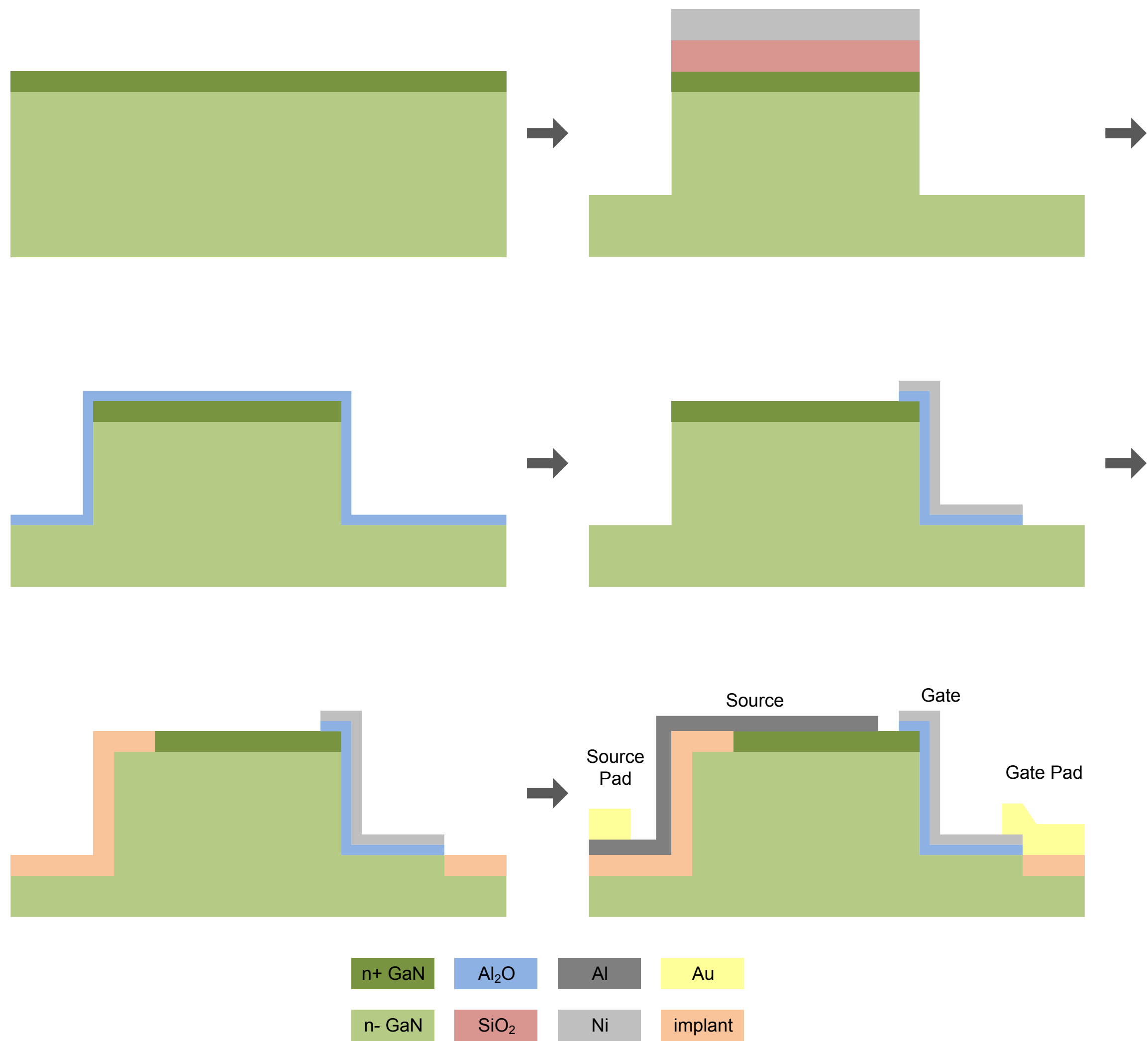


Figure 4.7: Fabrication flow of the pad connections for the implant isolated pad process.

Two observed issues led to changing the pad connection process again. First, the measured leakage through the implanted isolation via the test structures was significant, and much higher than the measured leakage through the insulating oxide. Second, the source metal did not connect down the end of the fin for smaller widths. This would be a problem as the calculations

show that smaller fin dimensions will give better gate control. Figure 4.8 shows the disconnect in the source metal. This occurs because the focus offset during exposure is set to be in focus at the top of the fin. At the level of the etched surface, the source exposure is out of focus, so the resist is not exposed enough to allow for a continuous metal. Because of the large height difference, there is no focus offset that would provide enough exposure to both planes.

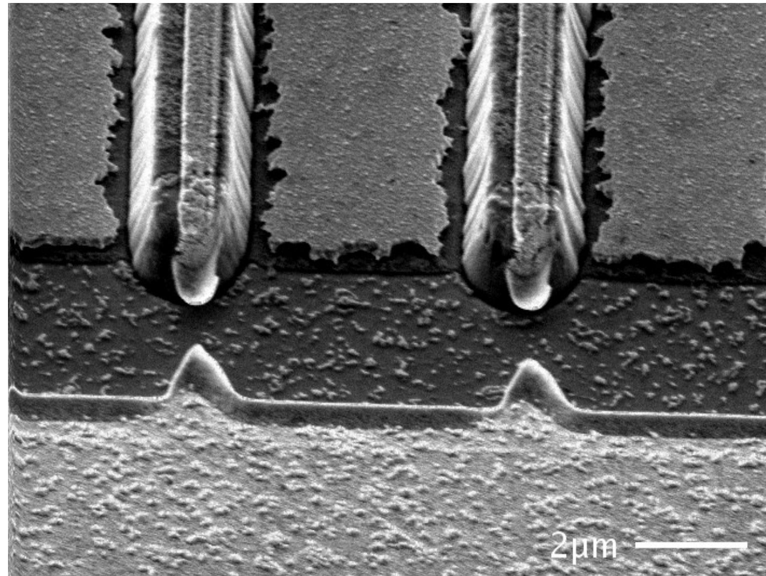


Figure 4.8: SEM of source disconnect down end of fin because of the focus discrepancy.

While a double exposure at two focus offsets should resolve this issue, another solution is to move the level of the source pad to that of the source, keeping the source metal nearly level throughout. Figure 4.9 shows the process flow to isolate the pads and connect to the metals. The oxide pad is formed by first etching the gate oxide and 300 nm of GaN and then back-filling with 400 nm of e-beam deposited oxide. This is done with the same exposure, the resist acting to lift off the pattern for the e-beam oxide. The gate pad metal thickness is increased to be greater than the step of the oxide pad to ensure a connection.

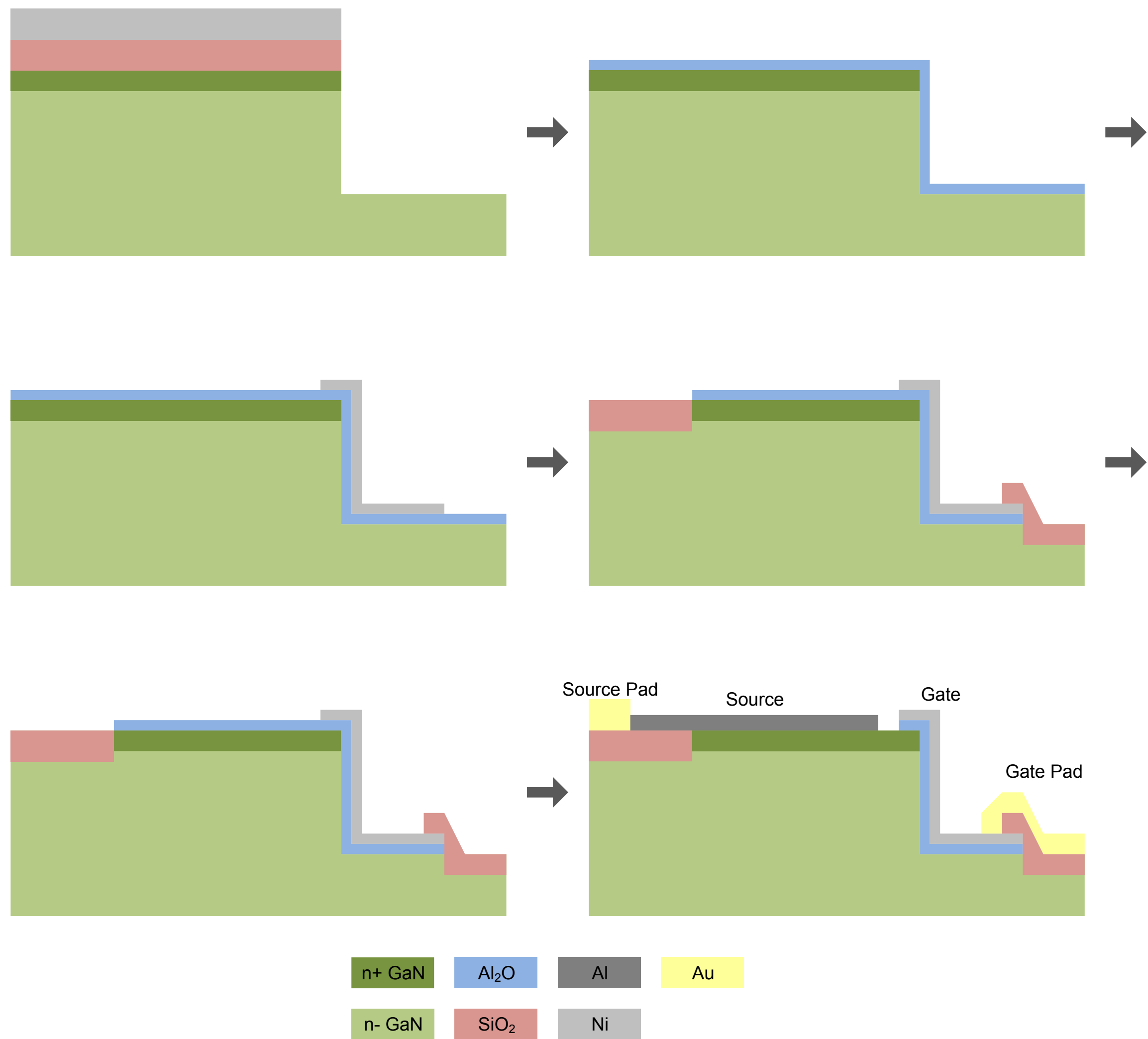


Figure 4.9: Fabrication flow of the pad connections for the raised source pad process.

4.2.2 Source Alignment to Fin

The placement of the source at the top of the fin requires two parts, first the removal of material from the top of the fin including gate oxide, and second, the alignment of the source to the opening from the first part. Multiple variations on both these process steps were tested to find a viable option for a working transistor. The dimension of the fin width varied from 2 to 8 µm, to allow for a 0.5 µm tolerance between alignments. This tolerance is the smallest alignment that can be reproduced on the optical i-line (365 nm wavelength) stepper. With two optically aligned layers, 2 µm fins are possible, with three layers, 3 µm fins are possible.

For the first attempt to expose the top of the fin, resist remains at the top of the fin in the exposed pattern for the gate, preventing metal deposition at the top of the fin. The metal could then be used as a mask to etch the oxide, before the source metal was deposited. While such tight alignments as 0.5 μm can be met with a vertical deposition of metal using resist for liftoff, the conformal deposition used resulted in significant extension of the metal in the undercut. Along with the conformal deposition of the source metal extending in its resist's undercut, a short between the source and gate forms, rendering the transistor useless. Figure 4.10 shows a diagram of how the short forms. Figure 4.11 shows the fins before and after source deposition, showing both a misalignment and the metal extension. The requirement of a conformal depositions is that both metal layers extend from the top of the fin to the bottom and need a solid connection between the two.

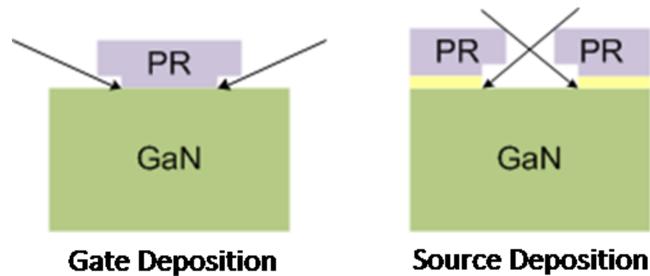


Figure 4.10: Diagram showing how two conformal depositions with tight alignments form a short.

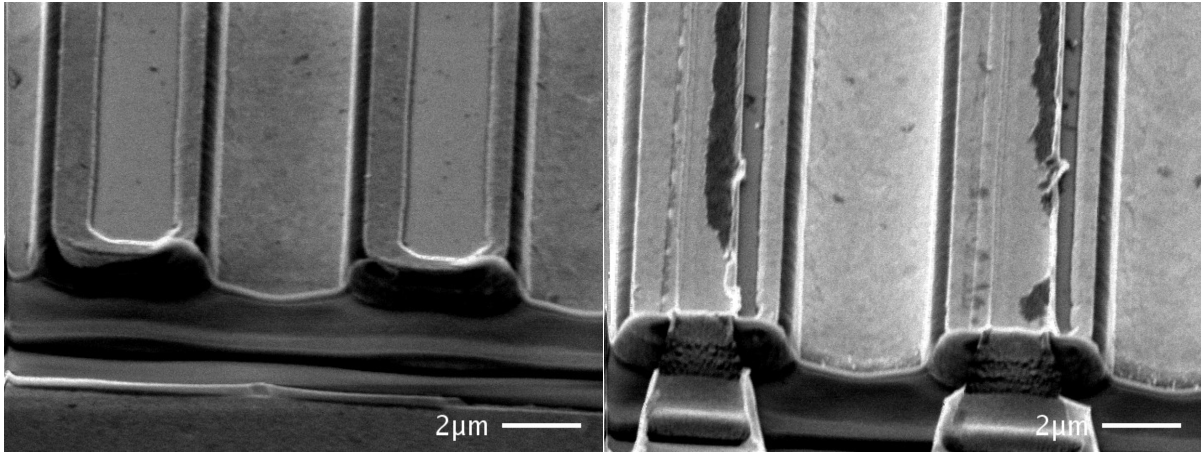


Figure 4.11: Gate metal extension after liftoff (left), and source metal extension and short to gate metal (right). The overlap of the gate on the fin is intended to be only 0.5 µm on each side.

To correct for this, metal wet etches were calibrated to remove some of the gate metal, with the expectation of leaving no gate metal at the top of the fin. This allowed for smaller fins by not requiring the exposed gate layer be tightly aligned to the fins as the metal would be etched away. A major disadvantage to wet etching is the lack of control and consistency, which is especially true for metal etchants. The etch rate for the gold etchant, Transene TFA, [24] is very dependent on stirring, where the etch rate is almost zero without, and very fast with stirring. In addition, the etchant tends to remove whole metal grains at a time, which leaves a very roughened outline, and wicks between the resist and metal etching metal that is supposed to be protected by the resist.

As an attempt to minimize the risk from the wet etch difficulties, when the resist was opened at the top of the fin, the samples were placed in the O_2 ashing chamber for a few minutes at 200 W to expand the opening and ash away the resist from the top of the fin. This reduces the expected time to remove sufficient metal in the wet etch, decreasing the total amount of uncontrolled etching. Figure 4.12 shows the fin opening resist layer before and after ashing. As seen in Figure 4.13, there is the expected roughening of the outline of the exposed gate

metal. Despite the precautions taken, wet etching was unviable and would regularly remove all the gate metal on the sidewall of the fins. This is seen in Figure 4.14.

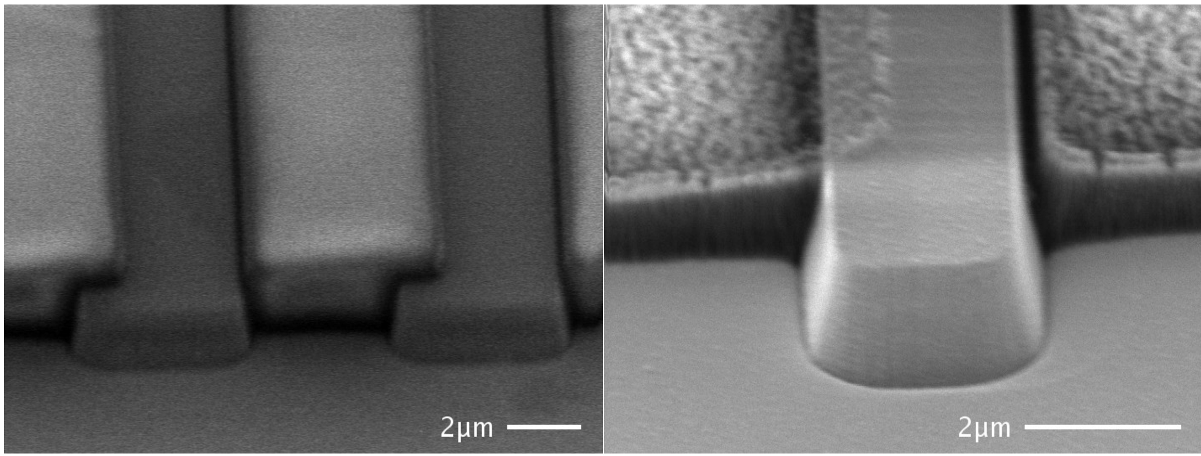


Figure 4.12: Fin top opening resist before (left) and after (right) ten minutes of ashing.

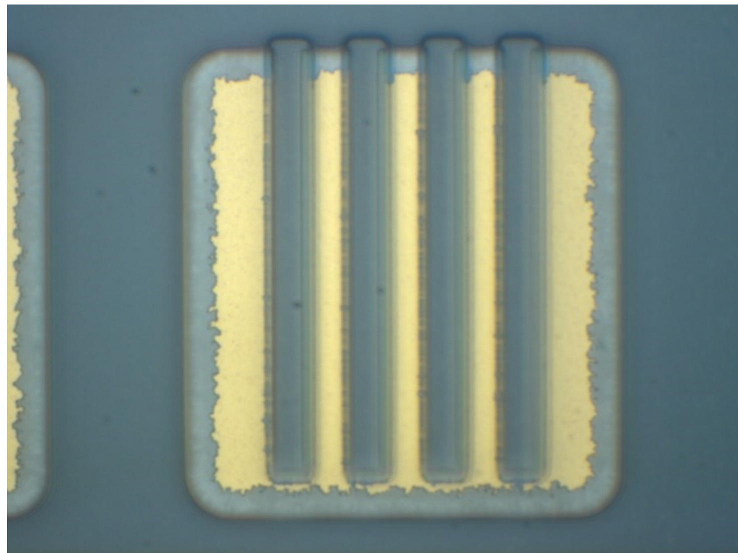


Figure 4.13: Roughened edges of pattern due to wicking and grain removal during wet etch.

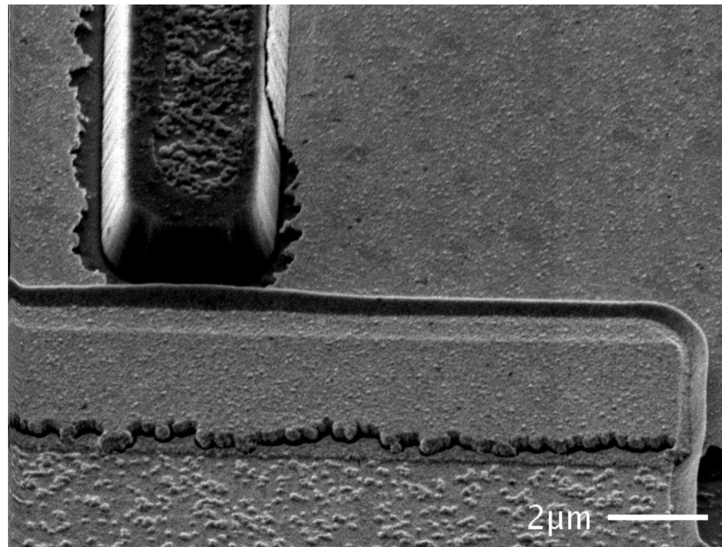


Figure 4.14: SEM showing gate metal removal from the fin sidewalls during wet etch.

With wet etching no longer under consideration, attention is turned to Ar milling as a solution. After some calibration and testing, it was found that the gold tends to redeposit on the sample during milling. With the flexibility of the newly installed Oxford ion mill, the sample was tilted downward during the milling to prevent this, with the result shown in Figure 4.14. This gave a much better looking transistor than the previous processes, showing clean definition of all layers and no visible shorts between source and gate at the top of the fin.

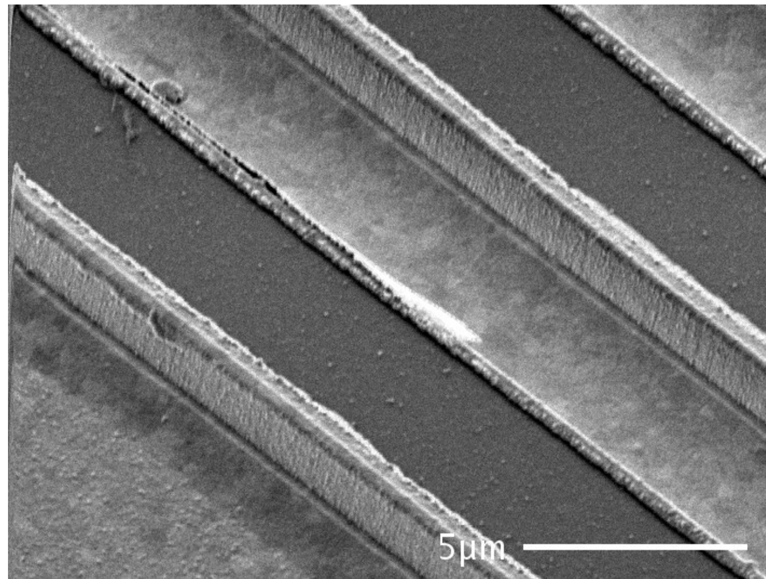


Figure 4.15: SEM of the top of the fin with gate metal and oxide removed by milling.

Figure 4.16 shows both an optical microscope and SEM image of the completed transistor. Figure 4.17 shows a cross section of the completed transistor showing a good contact of the metal deposited by ALD to the oxide. After measurements of the transistors, the devices showed some small gate control but no saturation, which could be due fins that are too wide that the current cannot be controlled within the center of the fin. Modeling and simulation confirmed this as the cause, the entire process flow needs to be redesigned to enable much smaller fin dimensions. The measurements of the transistors are described in Section 5.1.

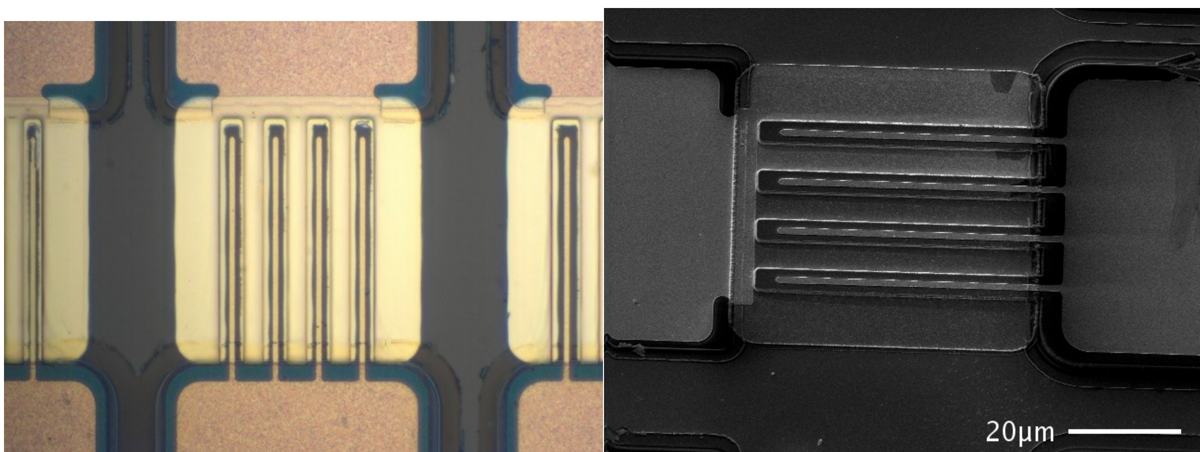


Figure 4.16: Optical and electron microscope images of finished devices using the source-last process.

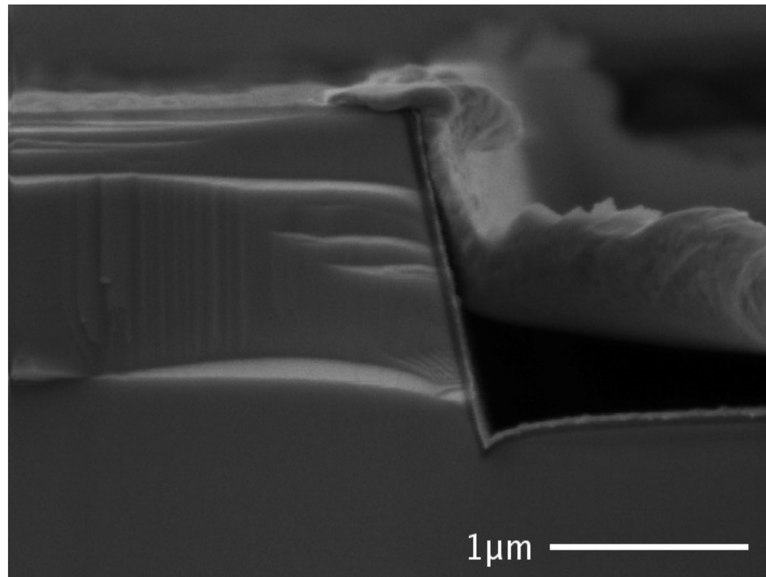


Figure 4.17: SEM of a cross section of fin using source last process showing conformal deposition of gate oxide and metal.

4.3 Self-Aligned Process

With the source-last process having several obstacles to a working device, as well as being limited to 2 µm fins at the smallest, the entire process flow was reworked to enable smaller dimensions. With a self-aligned process, small dimensions are achieved with at most one critical exposure. For the VFinMOSFET, this requires a redesign of the fin etch hard mask, as described in Sections 3.3.2 and 3.3.3, such that the source is formed as part of the etch process module. This eliminates the need to align a source metal to the fin, as well as the need to remove material from the top of the fin.

The change in how the source metal is formed allows for several simplifications to the process in terms of the number of lithographic steps and their complexity. The gate is now a continuous oxide and metal wrapped around and over the top of the fin. The source contact to the GaN is buried underneath the gate. While this may create a significant capacitance between the two, the primary concern is to create a working transistor first, and not to provide optimized

characteristics on the first attempt. A cross section of the resulting structure should look like the diagram of Figure 4.18.

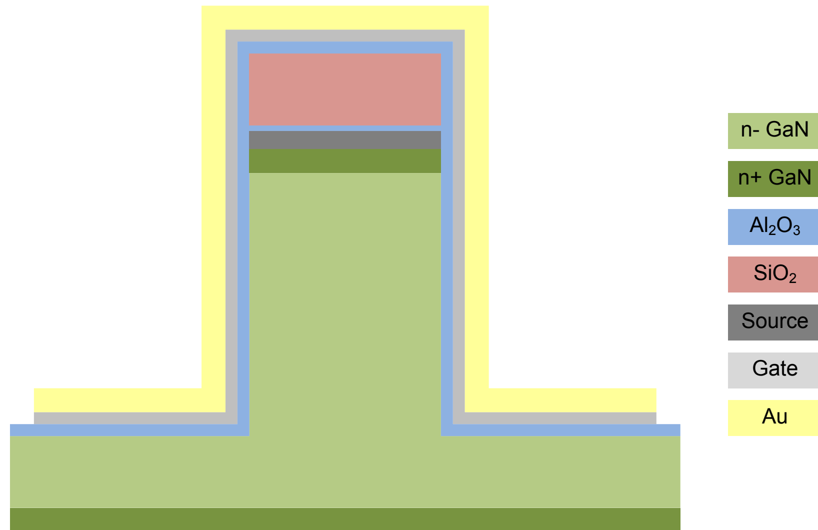


Figure 4.18: Cross section diagram of final structure for self-aligned VFinMOSFET.

While the gate and source/fin layers appear to be the only exposures necessary to produce this device, other exposures are also necessary. To be able to probe the gate and source, corresponding pads need to be formed. The gate pad is a simple matter, formed by extending the lateral portion of the gate to make a large pad, using the gate oxide as insulation. The source pad is another matter entirely, requiring the n+ source to be isolated, as well as the source metal.

4.3.1 Source Pad Isolation and Connection

Using techniques developed in the source-last process, described in Section 4.2.1, the first source pads were formed by etching the n+ and back filling with e-beam deposited SiO_2. This needed to be done before any other processing, so that the source metal will sit on top of it. This meant that the source metal would go over the interchange between n+ GaN to oxide, which optimistically would be a smoot transition, but in reality is quite rough, as seen in Figure 4.19 and could cause disconnects. To alleviate some of the issues, a shallow RIE GaN etch is

used to create a more gradual interface, as opposed to forming a steep step. Additionally, the thickness of the GaN etch and deposited oxide need to be set up such that the source metal remains connected. Failure to do so can result in the disconnect seen in Figure 4.20.

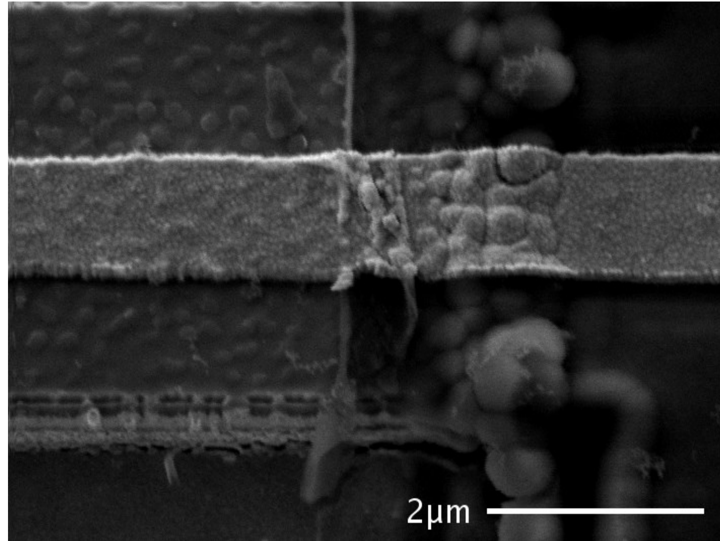


Figure 4.19: Source metal crossing from the oxide pad on the left, to the n+ on the right. From source-last process, but illustrates issues with connecting to the source pad.

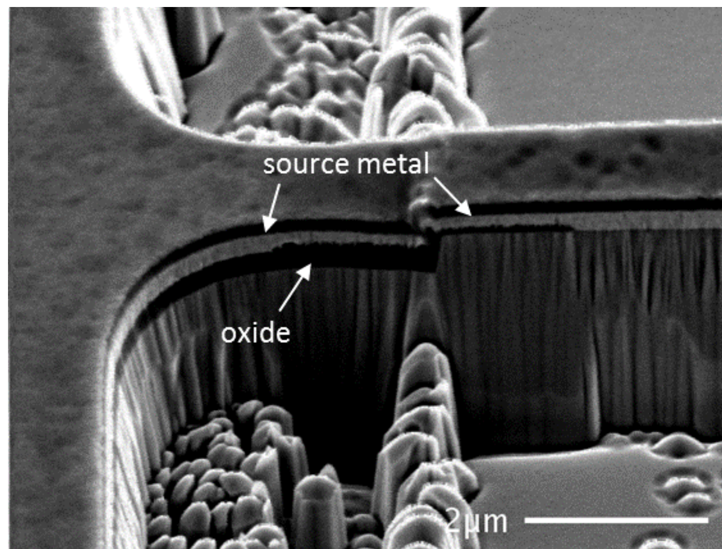


Figure 4.20: Source metal disconnect crossing from SiO_2 pad to GaN.

To prevent such further issues, the thickness of the source metal needs to be greater than the oxide step height. Instead of depositing the oxide in the same lithographic step as the etch,

the oxide is deposited by PECVD and etched by a timed wet etch to create an even more gradual slope. This should allow the metal to cross the now reduced step without breaking. Both SEM and electrical measurements confirmed the continuity of the source metal.

When the process is completed, the source pad will be buried underneath the gate metal and oxide, as well as the oxide in the hard mask. A final exposure opened a region over the source pad and allowed for milling of the metals and etching of the oxides to reach the source metal. Optionally, additional metal could be added to the source pad to increase its thickness and the hardness to probing. Figure 4.3 illustrates the gate and source pad connections in terms of exposures. The steps for the source pad fabrication are shown in Figure 4.21.

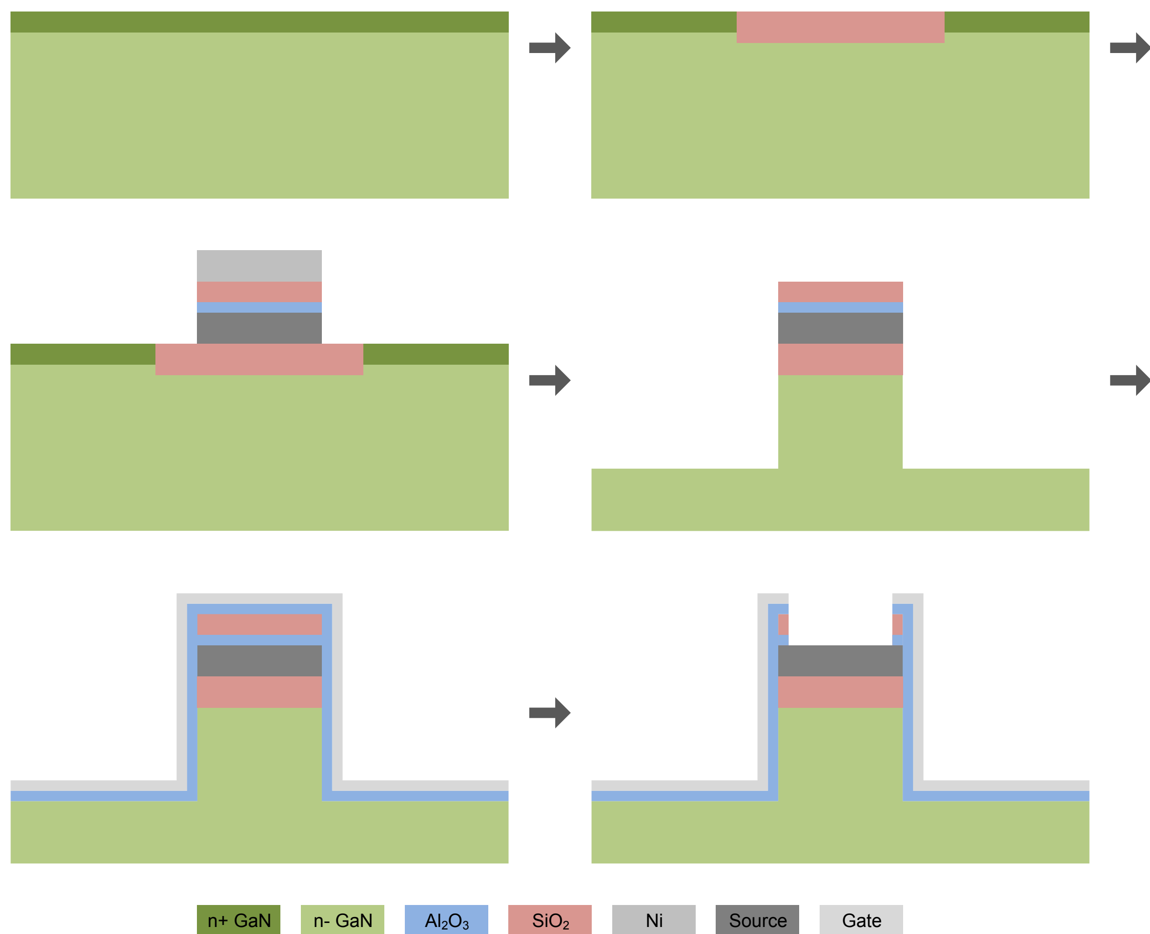


Figure 4.21: Source pad formation and opening for self-aligned process.

4.3.2 Tungsten-Source with MOCVD Oxide

Using a tungsten source, an attempt at fabricating transistors was made. The process flow is shown in Figure 4.22 and begins with 200 nm of 2.6e18 n+ GaN on 4 μm of 5e15 n- GaN, beneath which is 2 μm of 2.6e18 n+ GaN as the drain. The source pad oxide is formed, as described in the previous section. The fins are patterned and etched with the hard mask process described in Section 3.3.2. While initially the SiO_2 spacer was used, later the mask was formed without it. Some samples were processed using a TMAH treatment to remove ICP etch damage, while others were not.

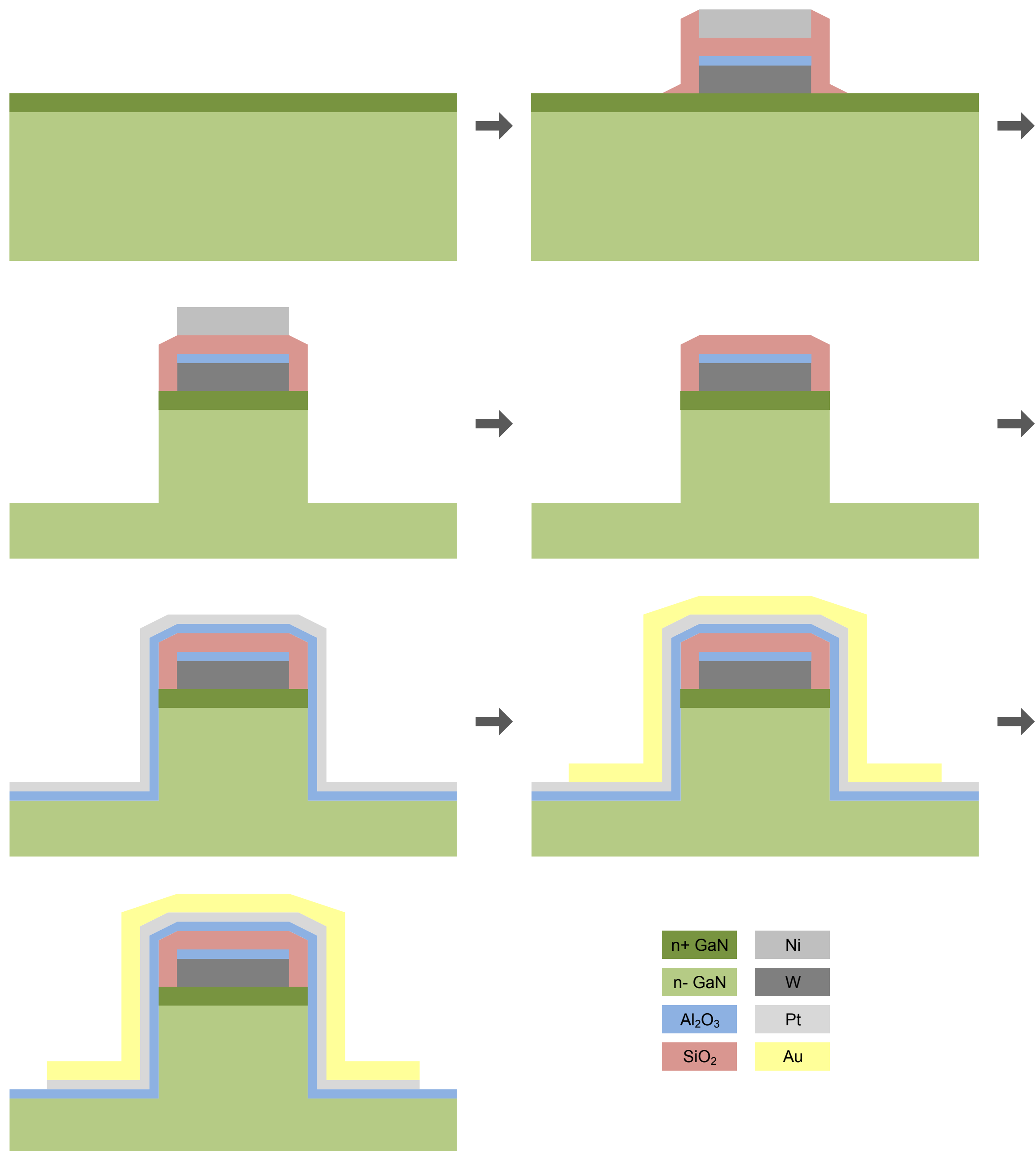


Figure 4.22: Tungsten source VFinMOSFET process flow.

The gate oxide was 50 nm of Al_2O_3 deposited using MOCVD at 700°C, along with a 4 nm GaN interlayer for some samples. 20 nm of ALD platinum was deposited as the gate metal, followed by a patterned gold deposition via liftoff. Using the gold as a mask, the exposed platinum was removed by an Ar mill. To complete the process, metal and oxide are removed from the source pads as described in the above section, allowing for probing of the source.

A couple of issues arose from the tungsten source process. The deposition of the gold via planetary rotation in the e-beam deposition system left void pockets at the corner of the fins. Figure 4.23 shows a cross section of the transistor showing the gold clearly raised in the corners. While this should not be an issue due to the ALD Pt making contact throughout the fin, the void formation was prevented by depositing 20 nm of Ni in addition to the gold. It is suspected that the gold lifts when cooling due to thermal expansion, and nickel's lower thermal expansion holds the gold to its shape when depositing.

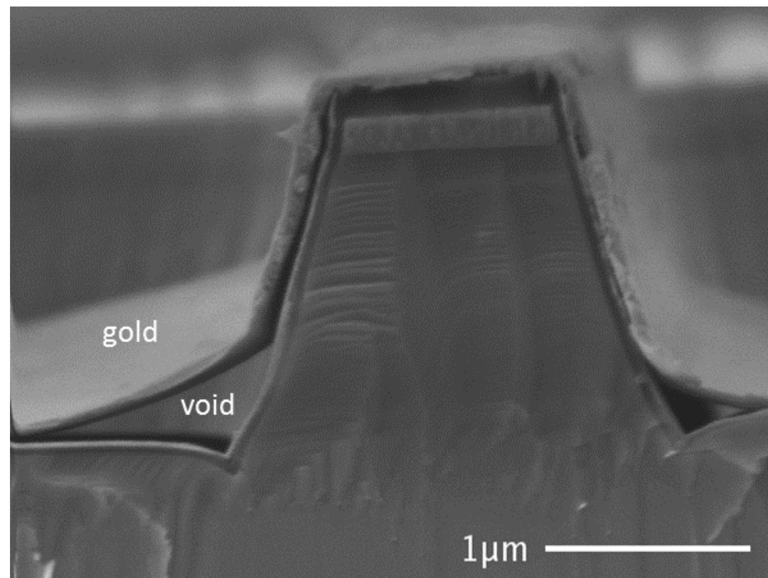


Figure 4.23: Tungsten source fin cross section showing voids formed below the gold in the corners.

When measuring devices without a TMAH treatment, while the devices allowed current to flow from source to drain on the first measurement, once a bias was applied to the gate, the source and drain became electrically disconnected. This is attributed to large amounts of surface traps from the ICP etching. Because the devices are normally on, there would initially be mobile carriers to carry current. With the applied bias, the gate capacitor charges, filling these traps, and these trapped charges cannot be removed. This prevents the sidewalls from

accumulating mobile carriers, cutting off current through the fin. Evidence of rough sidewalls is seen in Figure 4.24.

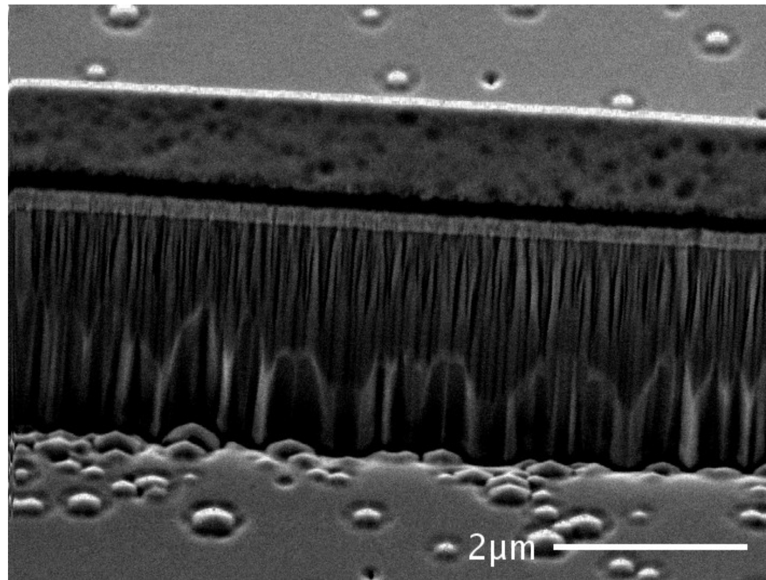


Figure 4.24: Rough sidewall from fin etch.

Using TMAH to remove the damaged surface before oxide deposition resulted in new issues related to the treatment. Because of an initially rough sidewall, the TMAH highlighted large steps in the sidewall, as seen in Figure 4.25. The faceting prevents the formation of a continuous channel, drastically reducing mobility in the accumulated sidewalls.

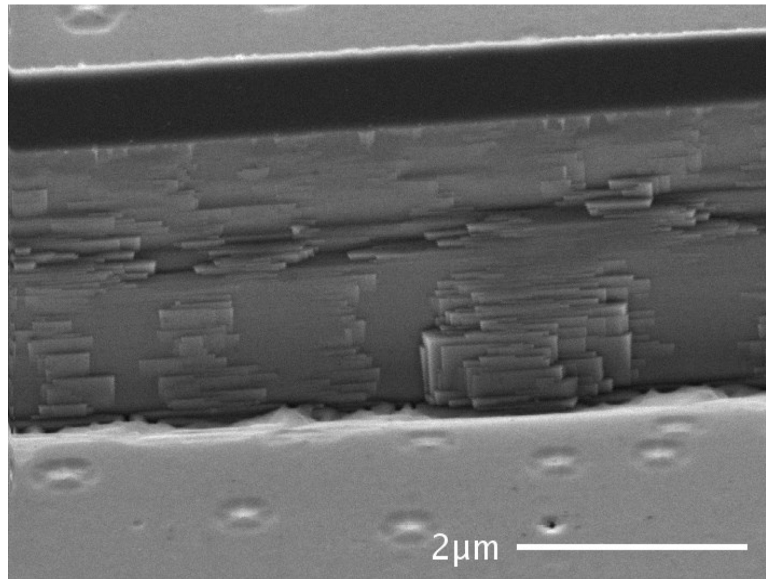


Figure 4.25: Faceting after TMAH treatment when starting with an initially rough sidewall.

Images such as Figure 4.26 show that the hard mask caused micromasking and roughened lateral etched regions near masked regions. It was suspected that either the tungsten dry etch did not fully remove the metal from the unmasked regions, or that the tungsten was sputtered during etching. The pattern of bumps forming in close proximity to the mask suggest the latter is present, however the presence of metallic particles before the fin etch, seen in Figure 4.27, suggest the former cause is also present. Changing the source metal to titanium should eliminate micromasking as Ti is rapidly etched by the Cl_2/Ar etch used to form the fins.

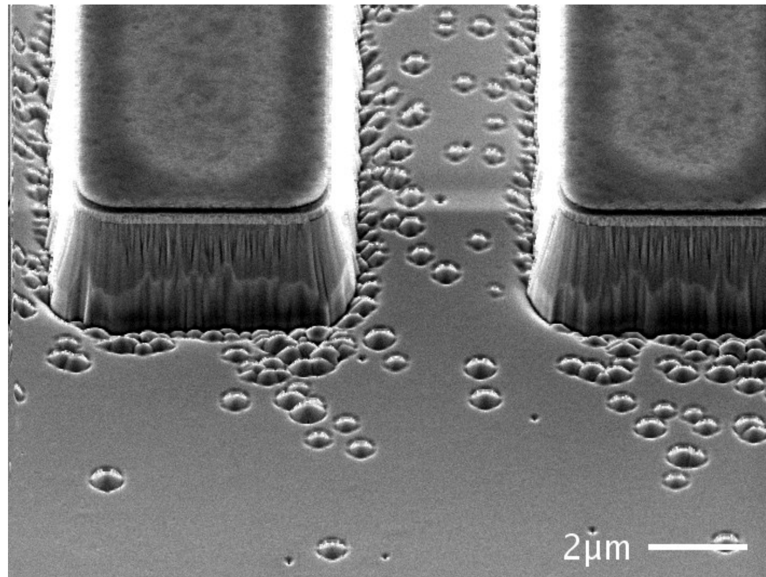


Figure 4.26: SEM after ICP etch showing bumps formed due to micromasking.

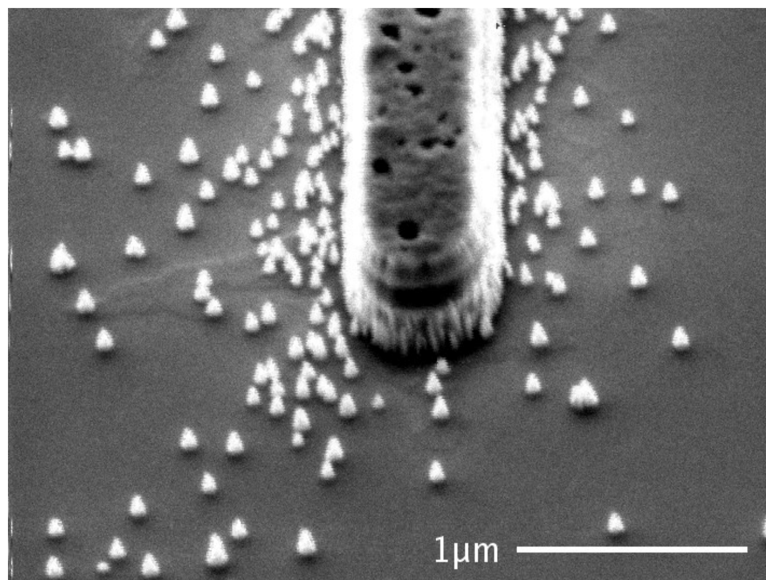


Figure 4.27: Metal particles surrounding hard mask before the fin etch. Evidence of incomplete etching or sputtering during mask formation.

4.3.3 Titanium-Source with ALD Oxide

The process flow for the Ti-source VFinMOSFET was very similar to the W-source flow, but with the hard mask described in Section 3.3.3. The initial growth is 2 µm of 2.6e18 n+ GaN, followed by 4 µm of 5e15 n- GaN, capped with 20 nm of 2.6e18 n+ GaN. The source

isolation is formed by etching through the n+ everywhere except for the active fins, depositing SiO_2 everywhere, and then etching it with a timed diluted HF dip. The resulting etch and oxide is seen in Figure 4.28.

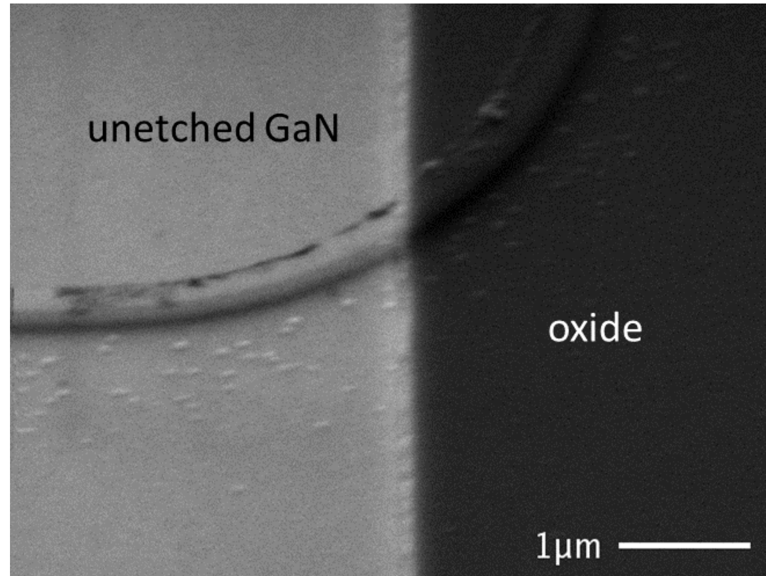


Figure 4.28: Source isolation etch and oxide.

This is followed by the deposition of the layers for the hard mask, and then patterning by Ni, which is removed once the hard mask is formed. This is shown in Figure 4.29, Figure 4.30, and Figure 4.31 alongside the isolation etch and oxide. The GaN is etched about 3 μm deep using this mask, seen in Figure 4.32, followed by a TMAH treatment. With a quick transfer to vacuum, to prevent oxidation and silicon deposition on the surface, 50 nm of ALD Al_2O_3, followed by 40 nm of ALD Pt are deposited as the gate. Gold capped with 20 nm of nickel are deposited by e-beam deposition and patterned by liftoff. The exposed platinum is milled by an Ar mill using the gold and nickel as a mask. Finally, the material on top of the source pad is removed to expose the source metal for probing. This process is outlined in Figure 4.33.

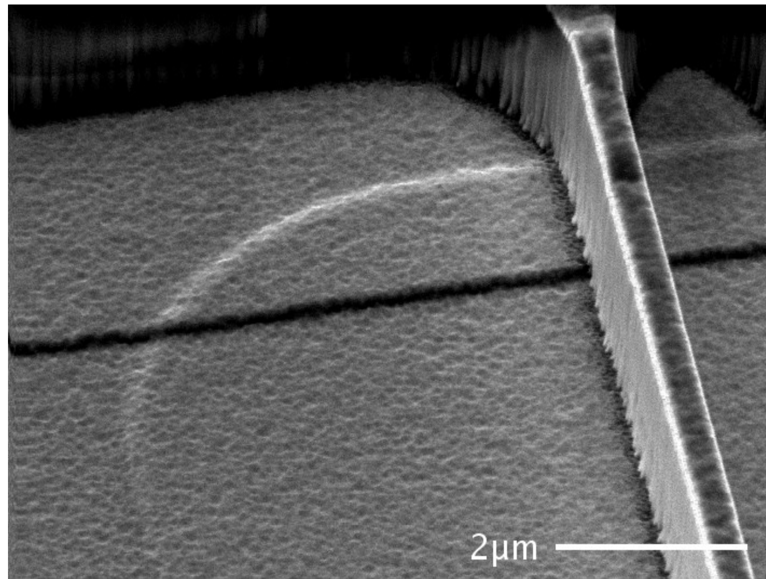


Figure 4.29: Fin etch hard mask during formation, before Al_2O_3 wet etch, alongside source pad isolation etch and oxide.

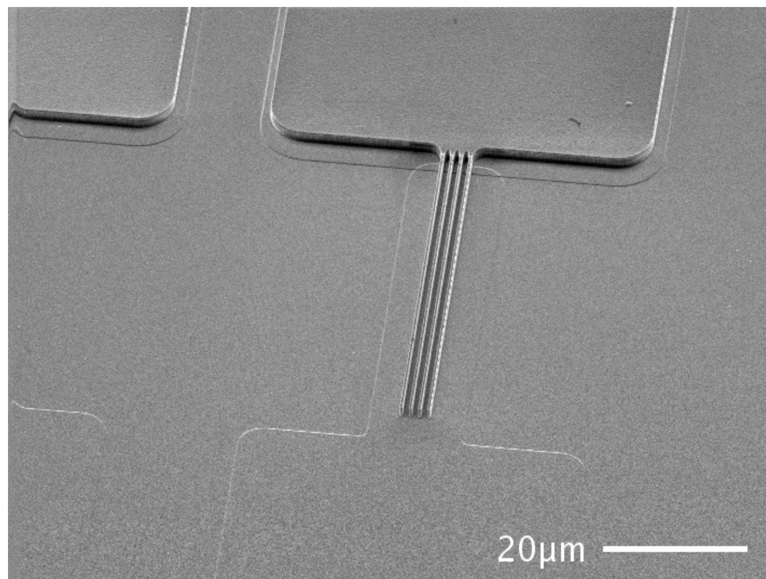


Figure 4.30: Fin etch hard mask during formation, after Al_2O_3 wet etch, alongside source pad isolation etch and oxide.

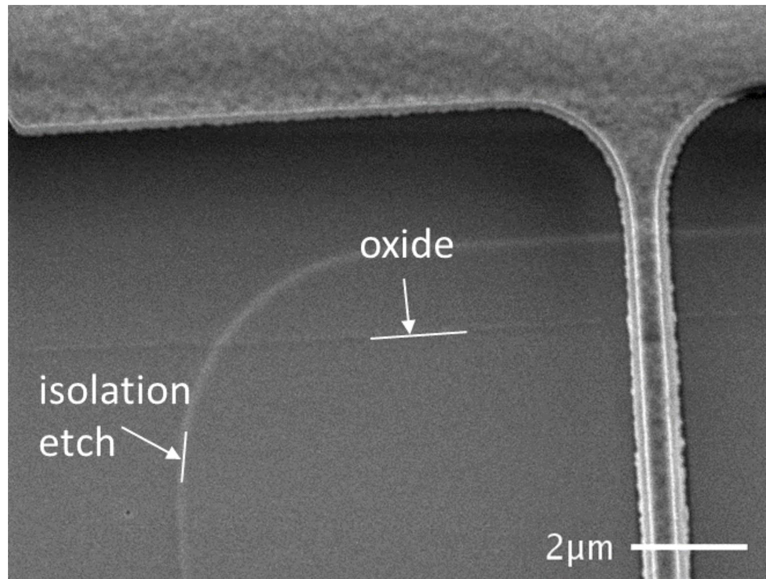


Figure 4.31: Fin etch hard mask alongside source pad isolation etch and oxide.

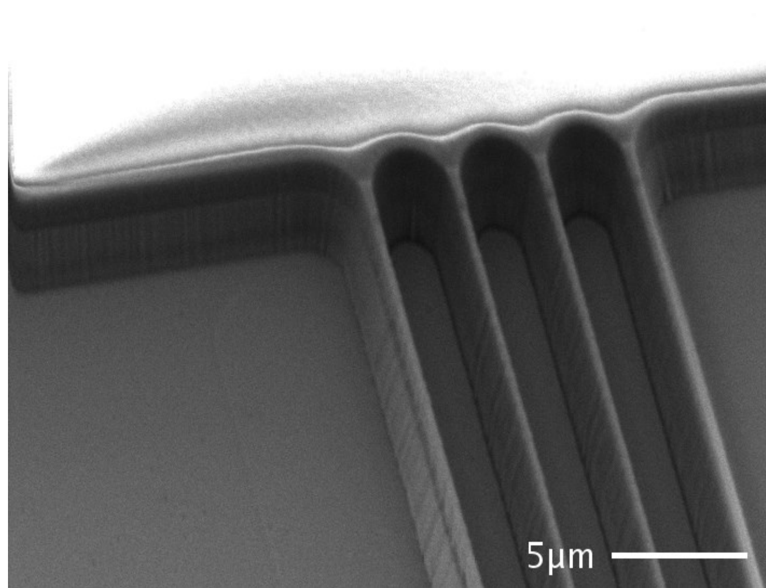


Figure 4.32: Etched fins before TMAH treatment. Note the faint outline of the pad isolation etch, transferred down in the deep GaN etch.

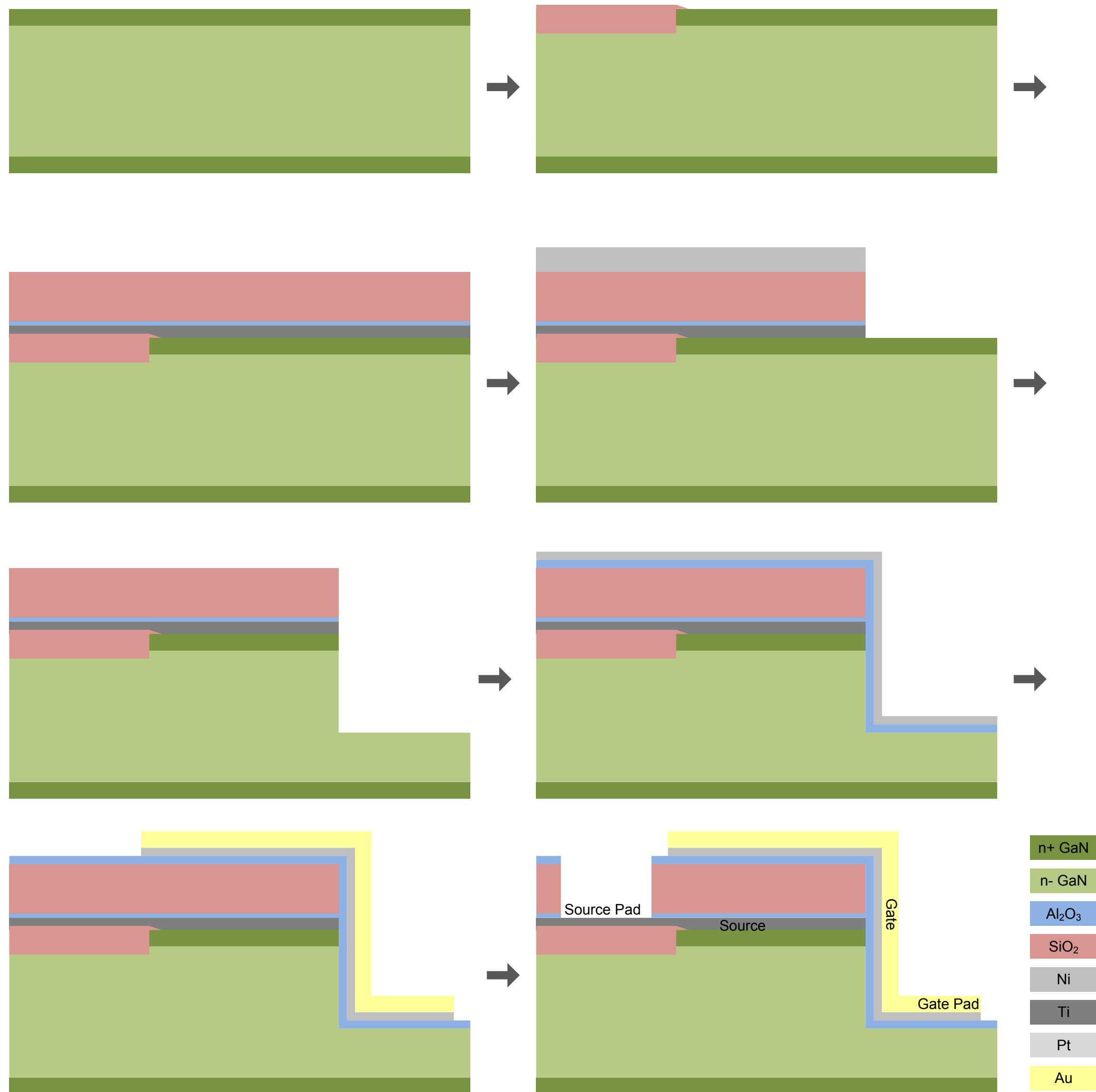


Figure 4.33: Cross section along the length of the fin showing the flow for Ti-source VFinMOSFET fabrication.

Despite testing of the hard mask for the etch, ICP etching of the GaN resulted in a large amount of roughness, seen in Figure 4.34. Blame was placed on the pad isolation process as that was not part of the prior testing of the Ti-source hard mask which had resulted in smooth etches. By observing the locations of the roughness and comparing it to the exposed patterns, the roughness did not match any exposure, and most likely resulted from the blanket deposited SiO_2. The exposed SiO_2 had not been fully removed during the timed HF etch, leaving residue

that would micro-mask during the ICP etch. This explanation was confirmed when a short SiO_2 CHF_3/CF_4 etch was added to the process just before the GaN Cl_2/Ar etch. With this additional SiO_2 etch, the GaN ICP etch resulted in a smooth surface as originally expected.

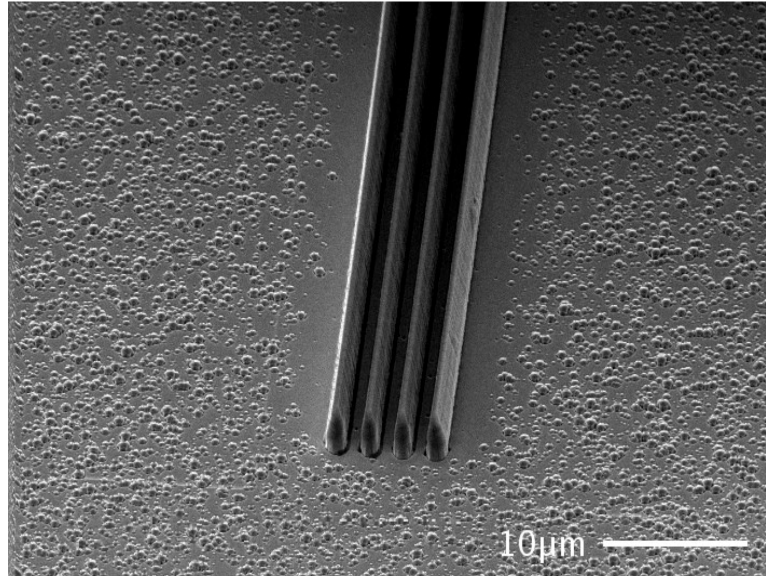


Figure 4.34: Roughness after GaN ICP etch.

TMAH, as a rapid etchant of aluminum and alumina, should etch the very narrow layer of Al_2O_3 used as an etch stop in the hard mask. While in larger structures this is not a problem as some undercut is tolerated, narrow structures like the fins show this etching clearly. Figure 4.35 shows the SiO_2 hard mask lifting partially off the fins due to the Al_2O_3 etching in TMAH. As the next step is ALD Al_2O_3 and Pt, this poses little to no obstacles to processing working devices. The conformal nature of ALD ensures uniform deposition around the GaN fin and Ti source, and the SiO_2 is not needed any further. A possible consideration for future processing would be intentional removal of the SiO_2 hard mask by lifting off in TMAH. With sufficient time in TMAH, the SiO_2 from larger structures can be removed, as shown in Figure 4.36.

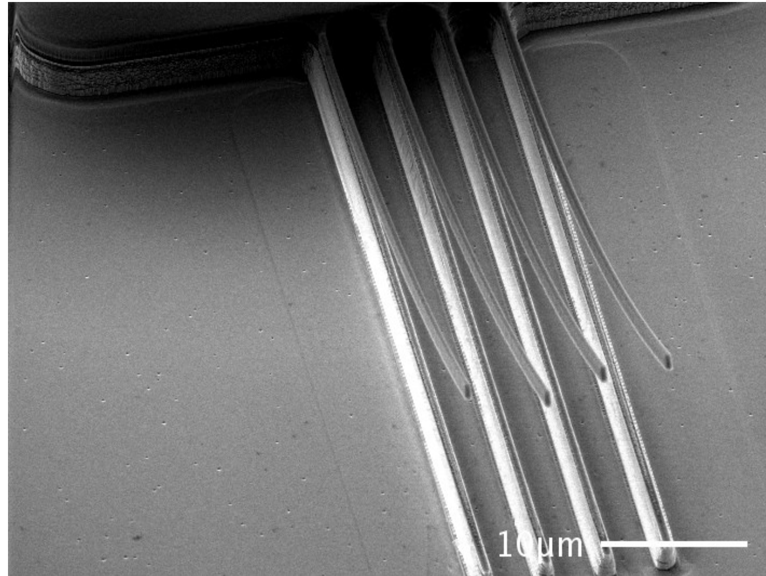


Figure 4.35: Partial liftoff of SiO_2 from fins during TMAH etch.

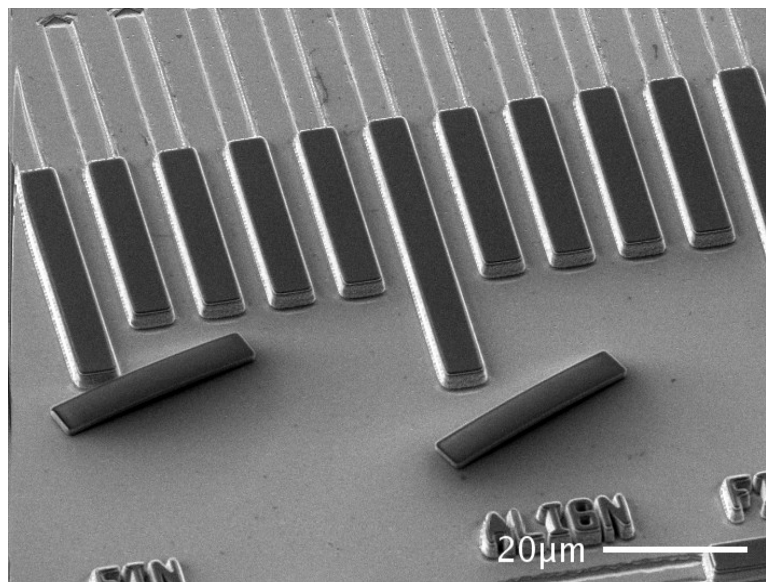


Figure 4.36: SiO_2 hard mask re-adhered to the sample after lifting off by TMAH etching the underlying Al_2O_3.

Once the transistors were fabricated and measured, some select devices were cut using a focused ion beam, FIB, and cross section images were taken using the attached SEM, seen in Figure 4.37, Figure 4.38, and Figure 4.39. The fins are not as vertical as hoped for, but with TMAH, are better than using the ICP GaN etch alone. The measured width of the fin at the top is larger than intended as the pattern is transferred through more than 2 μm of material in the

hard mask. Due to that transfer, the 300 nm fins measure 480 nm wide at the source and 1.4 μm at the bottom, and the 400 nm fins measure ~650 nm at the source and 1.6 μm at the bottom. A thinner hard mask, or more vertical transfers may be able to correct this in future devices.

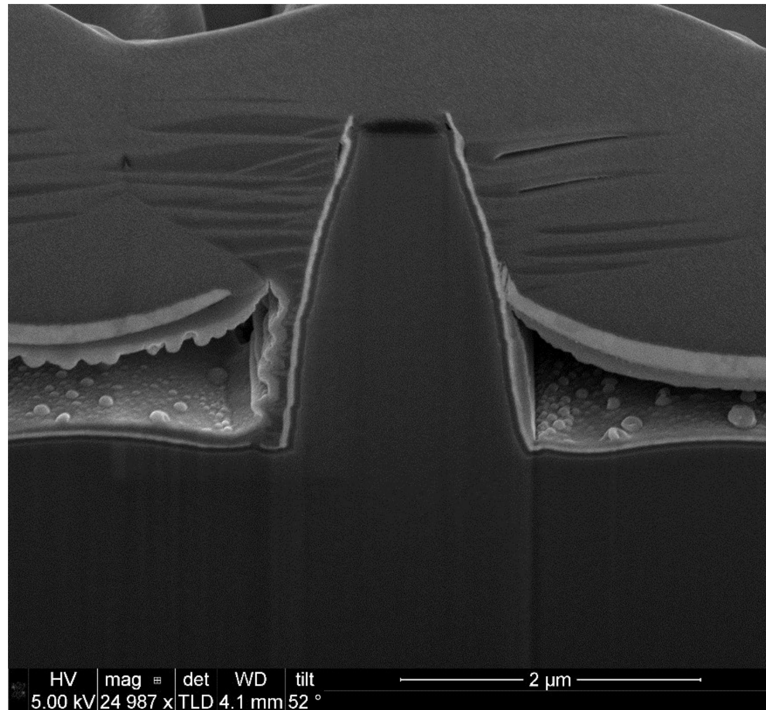


Figure 4.37: Cross section of a 300 nm fin.

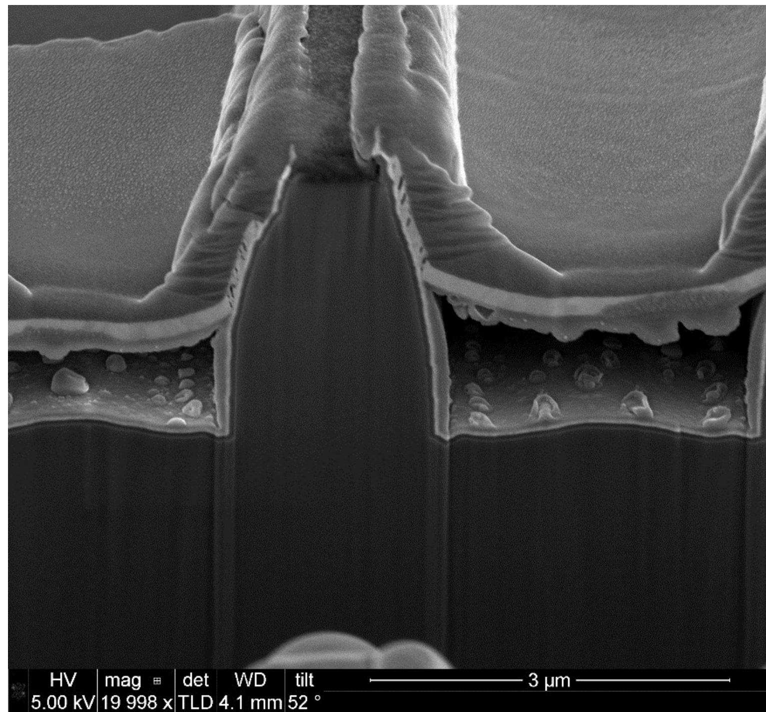


Figure 4.38: Cross section of a 400 nm fin.

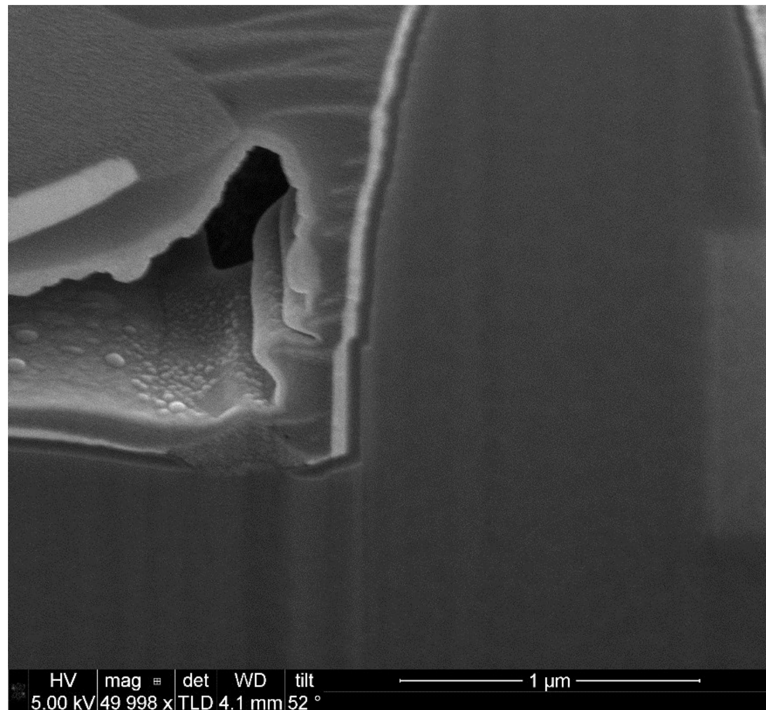


Figure 4.39: Cross section of the bottom of the fin showing conformal coverage of the gate oxide and both the Pt and Au gate metals.

Chapter 5: Device Analysis

While several iterations of the VFinMOSFET were fabricated, many had severe flaws due to the processing that prevented measurement of the transistor. These flaws, described in Chapter 4, included missing gate metal as well as disconnected source from the source pad. After the move to a self-aligned process, many such issues were resolved, while a few others were resolved in further development of the fabrication. With all the debilitating fabrication flaws resolved, the later iterations of the VFinMOSFET could be measured and characterized.

5.1 Source-Last Devices

The final source-last devices had raised source pads and used ion milling to expose the top of the fin, after an alignment by lithography. Only devices larger than 4 μm allowed for enough separation between the source and gate metals for there not to be a short. Measuring single fins of various sizes, triode-like characteristics were observed, as seen in Figure 5.1. The gate did control the amount of current flow, however the devices did not appear to saturate. This is explained by the large amount of leakage current flowing through the center of the fin, uncontrolled by the gates. This meant that smaller fins needed to be fabricated, prompting the move to a self-aligned process.

Measured gate leakage was high, on the order of 5% of the total drain current. This could be due to surface currents on the un-passivated top of the fin, going between the gate and source metals. This is resolved with a self-aligned process as it inherently passivates the source metal and fins with the gate oxide deposition.

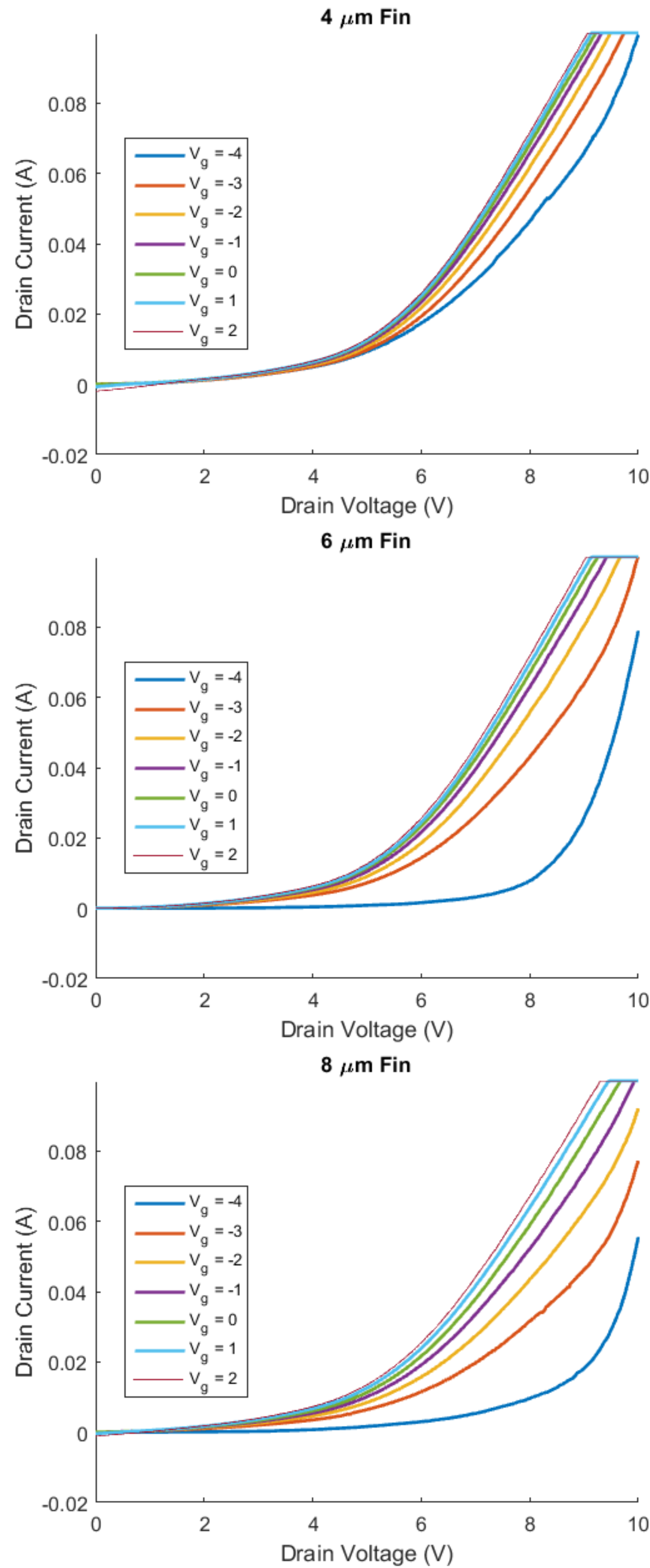


Figure 5.1: 4 μm (top), 6 μm (mid), and 8 μm (bottom) fin I-V characteristics.

5.2 Tungsten-Source Devices

The first tungsten source devices to be measured had been fabricated using SiO_2 spacers in the hard mask and did not have a TMAH treatment to remove damage. The first measurements performed was of the test structures, confirming that the source and gate pads were insulating, and that the source metal was connected to the source pad. With this being the case, some transistors were measured, first without a gate bias. Some of these measurements are shown in Figure 5.2. The 400 nm fin transistor showed much smaller current than its larger counterparts, with the larger ones allowing current to flow through the center, with the total current limited in some other manner. A test structure measuring the current through an ungated fin from the source metal indicates that there is no turn-on voltage, shown in Figure 5.3, however the devices show a turn-on voltage, which could be due to the gating of the fin creating a small barrier. Do note that the fin sizes correspond to the size of the pattern and not the actual dimensions of the GaN fin. The actual size needs to be measured via a cross-section.

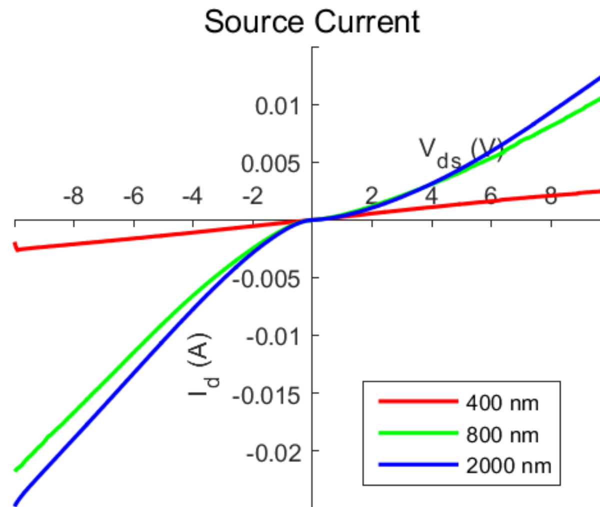


Figure 5.2: Measured current for different sized fins with the gate floating.

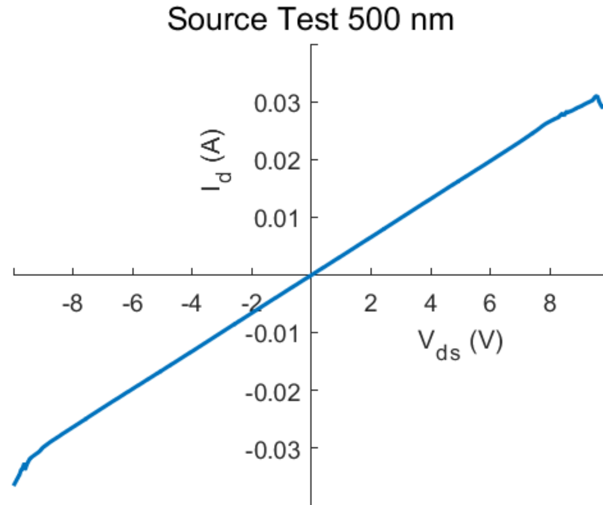


Figure 5.3: Measured current through an un-gated 500 nm fin.

When a bias is applied to the gate, however, the device no longer allows current to flow from the source to drain. In addition, gate leakage measured is on the same order as the originally measured source current. Several possible explanations exist, but the most likely is that large amounts of surface traps being filled by biasing the gate, causing the channel to remain closed. Measuring the source current with a floating gate again shows that the traps are still filled and source current is blocked. Improvements to the etched surface are necessary to remove the traps, leading to using a TMAH treatment to remove the damaged GaN crystal. As explained in Section 4.3.2, severe faceting prevented further tungsten-source devices from completion and measurement.

5.3 Titanium-Source Devices

After developing and fabricating Ti-source VFinMOSFETs, the test structures showed good connections between the contacts and their respective pads, as well as very little leakage through the pad oxides. While not all devices had working connections, there were sufficiently many of each size that did to make any intended measurements. The drain contact was

originally a large circle pad with no oxide below at the same level as the source. Due to some difficulty with current flow, a couple new drain contacts were formed by scratching a corner of the sample and placing an indium dot. The current flow problem most likely resulted from the 4 µm of n- GaN below the drain pad to get to the drain n+ at the bottom of the epi layers. By scratching and using an indium dot, this n- layer was bypassed.

5.3.1 Top Source Contact

Initial measurements showed clear MOSFET curves, but with severely reduced current from expected by modeling and simulation. This is shown in Figure 5.4. While the expected current for a transistor of this size is on the order of 100 kA/cm^2, as modeled in Section 2.2.5, the current measured was on the order of 10 A/cm^2. The source contact was found to be the cause of the severe discrepancy in the order of magnitude. Measurements of source contact test structures to the indium dot drains showed that the titanium formed a 0.4 V Schottky barrier with the n+ GaN. By measuring the transistor with the source on the top of the fin, the source contact is a reverse biased Schottky diode. In reverse bias, thermal current flow is very small, and only tunneling current can carry significant current. This Schottky source contact was limiting current to the fin, preventing good measurements of the intrinsic device.

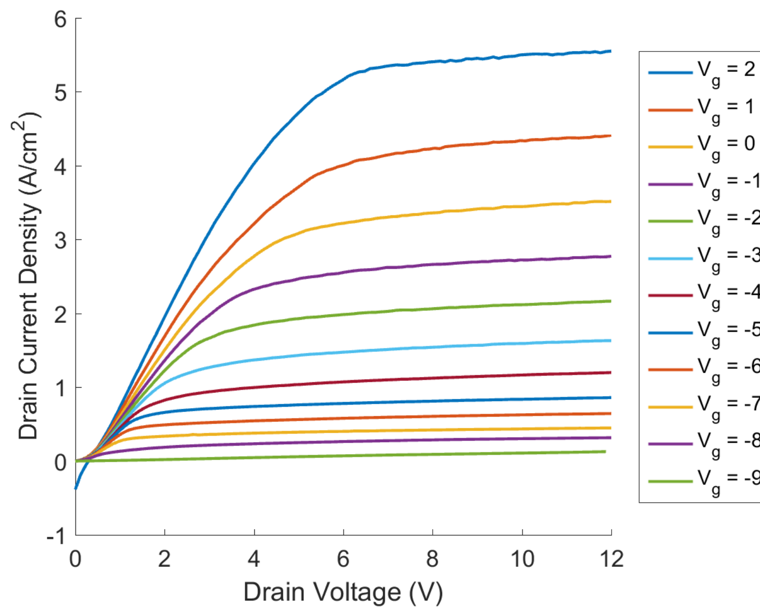


Figure 5.4: I-V of a 4x300 nm fin transistor, measured with the source on top.

Taking what can be learned from these measurements, the gate could handle significant negative voltages relative to the source before breaking down or leaking. Measurements could be made with V_{GS} at -9 V. The threshold voltage of the transistor is very negative at around -7 V for a 300 nm device. A sweep of the gate voltage is shown in Figure 5.5.

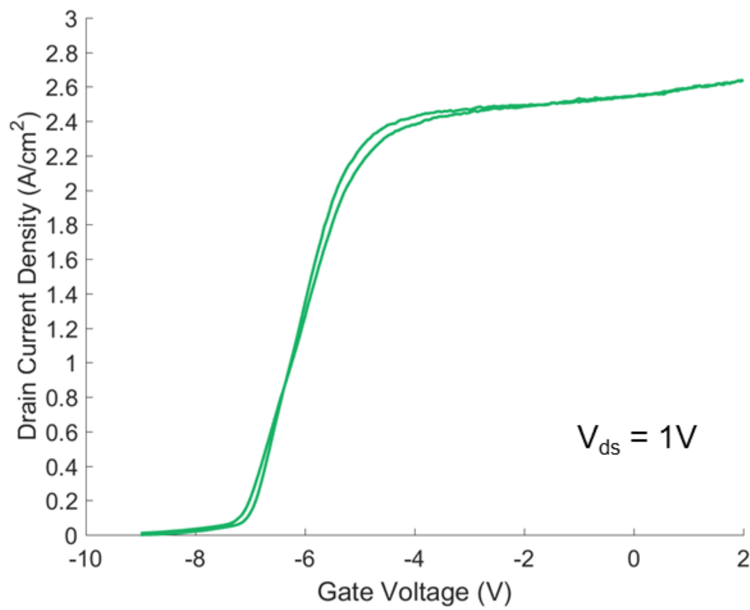


Figure 5.5: Gate voltage sweep of a 4x400 nm fin transistor, measured with the source on top.

The drain current does appear to saturate, but combining the Schottky model with the JFET model indicates this might be an effect of the series Schottky diode. The devices appear to have no intrinsic turn-on voltage, but the linear region has some kinks before saturation, noticeable in the larger fins. These kinks may be a result of shifting between a mostly open fin, a pinched off fin, and accumulated sidewall current, or from the increasing tunneling current in the Schottky contact. I-V characteristics for larger fins are shown in Figure 5.6 and Figure 5.7.

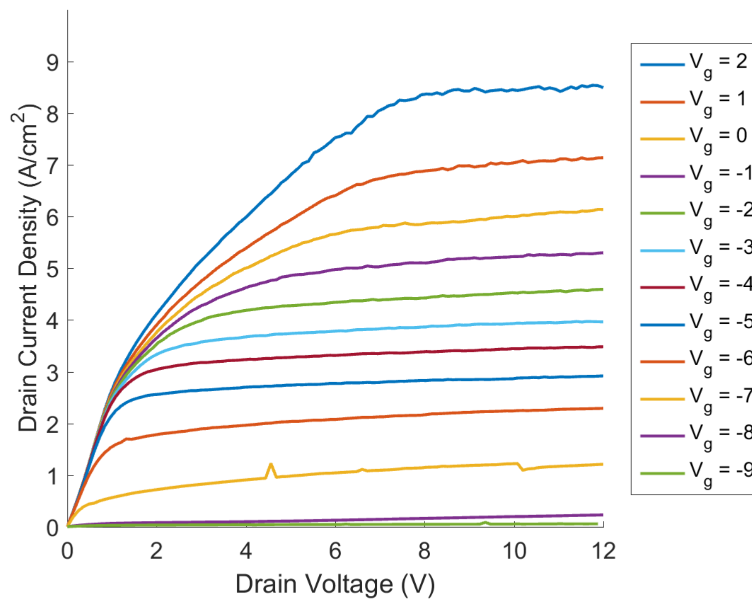


Figure 5.6: I-V of a 4x400 nm fin transistor, measured with the source on top.

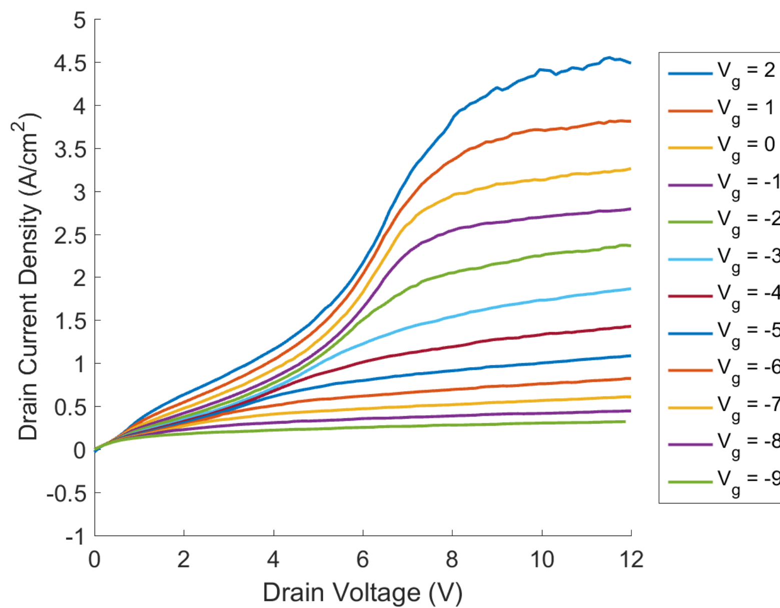


Figure 5.7: I-V of a 4x800 nm fin transistor, measured with the source on top.

5.3.2 Top Drain Contact

If the devices are measured in reverse, such that the source is at the indium dot contact, and the drain is measured as the top of the fin, the Schottky diode at the top of the fin would be in

forward bias as opposed to reverse bias. In this mode, the Schottky diode allows a large amount of current, more than the expected device current, to pass. However, a turn-on voltage of about 0.4 volts should be expected from the diode. Figure 5.8 confirms both the increased current and the turn-on voltage. The threshold voltage remains very negative, around -6 V. Drain voltages greater than 5 V could not be applied without risking the gate to drain leakage, preventing the observation of saturation. The gate voltage sweep is shown in Figure 5.9, with the I-V of larger fin devices in Figure 5.10, Figure 5.11, and Figure 5.12.

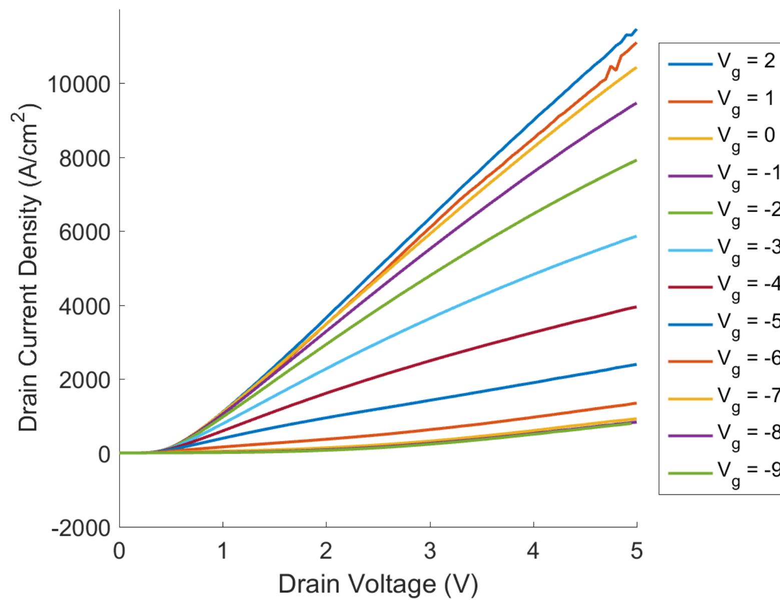


Figure 5.8: I-V of a 4x300 nm fin transistor, measured with the drain on top.

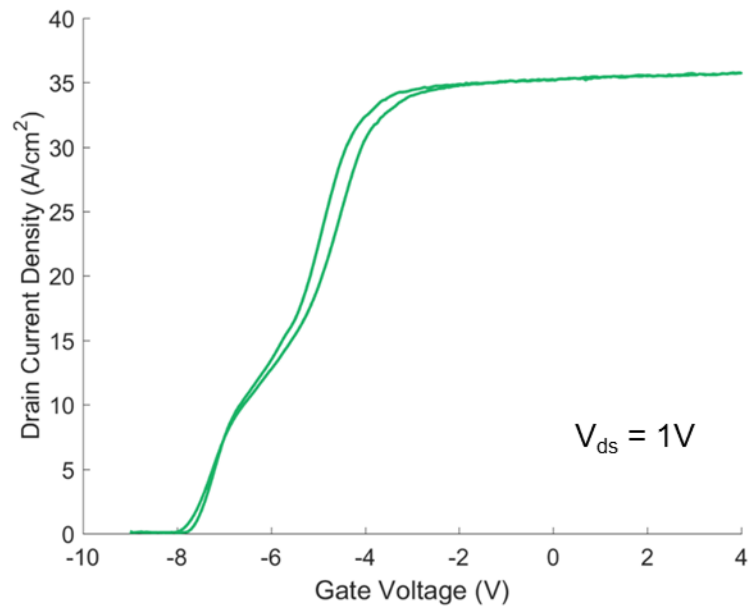


Figure 5.9: Gate voltage sweep of a 4x 400 nm fin transistor, measured with the drain on top.

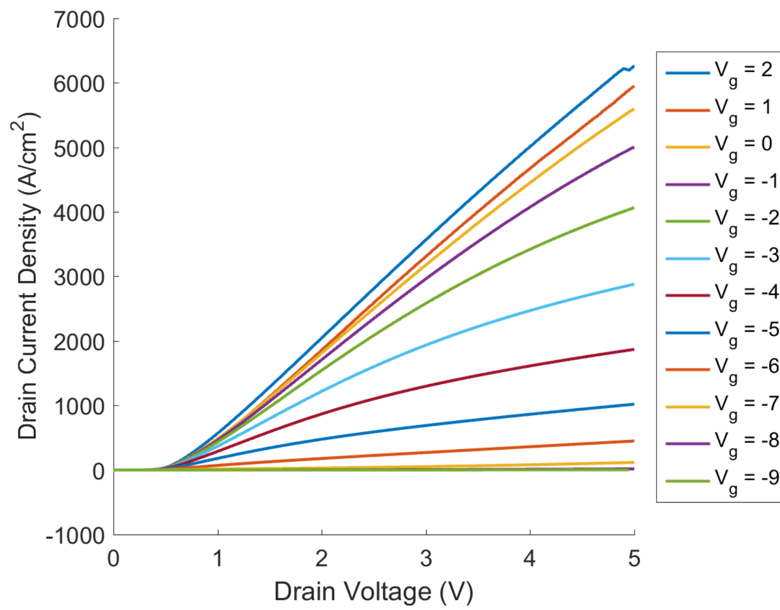


Figure 5.10: I-V of a 4x400 nm fin transistor, measured with the drain on top.

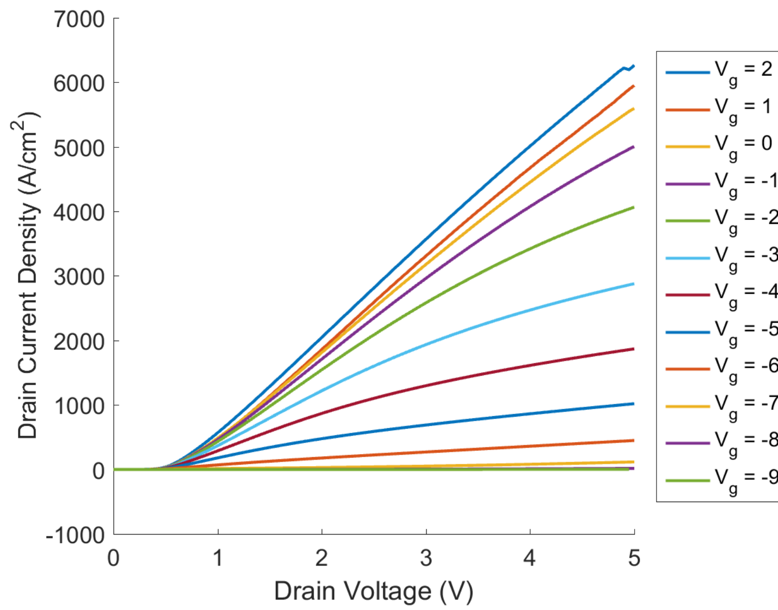


Figure 5.11: I-V of a 4x500 nm fin transistor, measured with the drain on top.

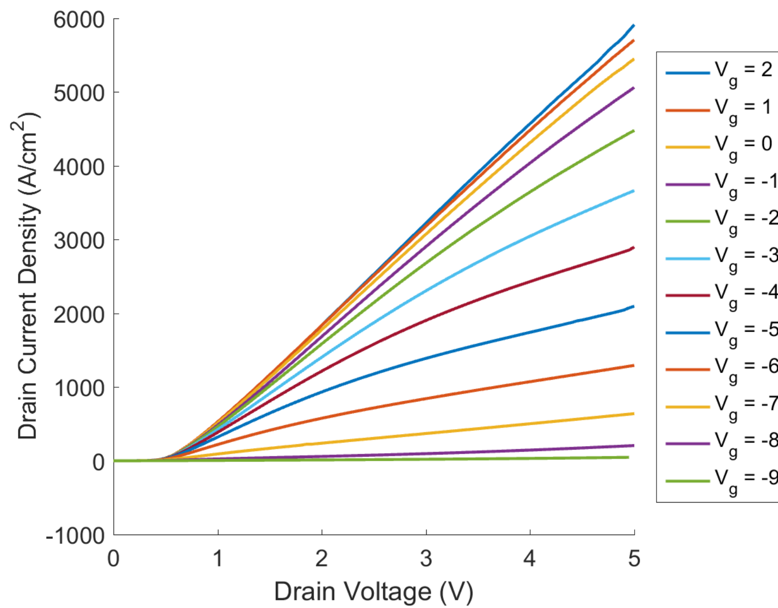


Figure 5.12: I-V of a 4x600 nm fin transistor, measured with the drain on top.

These devices show that at a drain voltage of 3 V, the current is about 5 kA/cm^2. This gives an R_{on} of about 0.6 mΩ/cm^2 using the only the area of the fins, which assumes no current spreading. These values are comparable to results from Sun et al. [25] which uses a e-beam

lithography to pattern the fins and a planarization and etch back process to open up the sources for contact. While the compared transistors show breakdown measurements of up to 800 V, the fabricated devices presented here were not designed with a thick drift layer to handle such high voltages. However, the devices show that the active portion of the transistor can be fabricated without e-beam lithography.

5.3.3 Proposed Solutions to Source Schottky

With all the development of the hard mask, a titanium source contact was determined to be the best fit for the process. Unfortunately, this is causing the Schottky barrier limiting current flow. Reversing the polarity allows for better measurements of the intrinsic fin, however, large drain voltages cannot be applied, and result in a turn-on voltage, and therefore is not a good solution. One solution that has been proposed is to increase the doping of the n+ GaN source contact. This would reduce the depletion width, increasing tunneling current through the barrier. Another possible solution is to use $In_{.23}Ga_{.77}N$ graded to GaN as the contact. This composition should reduce the Schottky barrier to zero, leading to a true ohmic contact. The 20 nm graded layer also needs to be doped at 1.5e19 cm^{-3} to counter the polarization charge and prevent a polarization barrier from forming.

Appendix A: Process Traveler

Vertical Fin MOSFET Traveler

Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115ºC	3 min
PR Spin				
	SPR 955-0.9	Spin	3500 rpm	30 sec
	Bake		90-95ºC	1 min
	Cool			1 min
Expose				
	[10,36]	FINFET3	ALIGN_P 3,0	
	Stepper 1	F/O = 5		1.8 sec
Post-Exposure				
	Bake		100ºC	2 min
Develop				
	AZ300MIF			55 sec
	DI Water	Running		2 min
Observe				
Etch				
	RIE 5	MAHR_HPE	~50 nm/min	6 min
Strip				
	NMP		80ºC	> 2 hrs
Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115ºC	3 min
PR Spin				
	HMDS	Spin	4000 rpm	30 sec
	Bake		95ºC	1 min
	Cool			1 min

	nLOF 2020	Spin	4000 rpm	30 sec
	Bake		110ºC	1 min
	Cool			1 min
Expose				
	[10,36]	FINFET3	GATE 0,3	
	Stepper 1	F/O = 0		0.75 sec
Post-Exposure				
	Bake		110ºC	1 min
Develop				
	AZ300MIF			1 min 30 sec
	DI Water	Running		2 min
Observe				
Etch				
	RIE 5	MAHR_LPE	~5 nm/min	8 min
Strip				
	NMP		80ºC	> 2 hrs
Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Oxide Deposition				
	PECVD 1	SiO_2	100 nm	_SIO_10
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115ºC	3 min
PR Spin				
	HMDS	Spin	3000 rpm	30 sec
	Bake		100ºC	1 min
	Cool			1 min
	SPR 955-0.9	Spin	3500 rpm	30 sec
	Bake		90-95ºC	1 min
	Cool			1 min
Expose				
	[10,36]	FINFET3	OXIDE 3,3	

	Stepper 1	F/O = 5		1.8 sec
Post-Exposure				
	Bake		100ºC	2 min
Develop				
	AZ300MIF			55 sec
	DI Water	Running		2 min
Observe				
Wet Etch				
	DI:BHF	Stirred	200 mL:11 mL	2 min
Strip				
	NMP		80ºC	> 2 hrs
Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Acid Dip				
	$HCl:H_2O$ 1:3	Stirred		1 min
	DI Water	Running		1 min
Metal Deposition				
	E-Beam 4	Ti	1500 A	Planetary
ALD - Dielectric				
	TMA	Al_2O_3	TMA+H2O-300C	300 cy, 30 nm
Ellipsometer				
Oxide Deposition				
	PECVD 1	SiO_2	1600 nm	_SIO_160
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115ºC	3 min
PR Spin				
	LOL 2000	Spin	1500 rpm	30 sec
	Bake		210ºC	5 min
	Cool			1 min
	SPR 955-0.9	Spin	3500 rpm	30 sec
	Bake		90-95ºC	1 min

	Cool			1 min
Expose				
	[10,36]	FINFET3	FINP 0,0	
	Stepper 2	F/O = 5		0.6 sec
Post-Exposure				
	Bake		100ºC	2 min
Develop				
	AZ300MIF			55 sec
	DI Water	Running		2 min
Observe				
Descum				
	PE II	O_2	300 mTorr, 100 W	40 sec
Metal Deposition				
	E-Beam 4	Ni	1800 A	
Liftoff				
	NMP		80ºC	> 2 hrs
Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115ºC	3 min
SiO_2 Etch				
	ICP 1	145	CHF_3/CF_4 cond	1 min
		145 ~85 nm/min	CHF_3/CF_4	24 min
		121	O_2 Clean	25 min
Al_2O_3 Wet Etch				
	AZ300MIF	~1.5 nm/min	500 rpm	30 min
	DI Water	Running		2 min
Ellipsometer				
Ti Etch				
	ICP 2	133	SF_6 cond	1 min
		133	SF_6	25 min
			O_2 Clean	26 min
Surface Clean				
	ICP 1	145	CHF_3/CF_4 cond	1 min
		145 ~85 nm/min	CHF_3/CF_4	1 min

		121	O_2 Clean	2 min
Mask Removal				
	Nickel Etchant TFB			20 min
	DI Water	Running		2 min
Etch				
	ICP 1	192	BCl_3	6 min
		164	Cl_2/Ar	12 min
		105	CF_4/O_2 Clean	8 min
GaN Wet Etch				
	TMAH	80°C		
	DI Water	Running		2 min
ALD - Dielectric				
	TMA	Al_2O_3	TMA+H2O-300C	500 cy, 50 nm
ALD - Metal				
	TMCpPt	Al_2O_3	TMCpPt+O3-300C	500 cy, 50 nm
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	LOL 2000	Spin	1500 rpm	30 sec
	Bake		210°C	1 min
	Cool			1 min
	LOL 2000	Spin	1500 rpm	30 sec
	Bake		210°C	5 min
	Cool			1 min
	SPR 955-1.8	Spin	3000 rpm	30 sec
	Bake		95°C	1 min 30 sec
	Cool			1 min
Expose				
	[10,36]	FINFET3	GATE 0,3	
	Stepper 1	F/O = 5		1.5 sec
Post-Exposure				
	Bake		110°C	1 min

Develop				
	AZ300MIF			1 min 30 sec
	DI Water	Running		2 min
Observe				
Descum				
	PE II	O_2	300 mTorr, 100 W	30 sec
Acid Dip				
	$HCl:H_2O$ 1:3	Stirred		1 min
	DI Water	Running		1 min
Metal Deposition				
	E-Beam 4	Au/Ni	2500/250 A	
Liftoff				
	NMP		80°C	> 2 hrs
Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Etch				
	Ion Mill	Gentle_Ar_Mill	40°C, 10° tilt	3 min 15 sec
Clean				
	Acetone	Ultrasonic		3 min
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min
Dehydration				
	Bake		115°C	3 min
PR Spin				
	SPR 955-1.8	Spin	3000 rpm	30 sec
	Bake		95°C	1 min 30 sec
	Cool			1 min
Expose				
	[10,36]	FINFET3	SOPEN 0,3	
	Stepper 1	F/O = 5		1.6 sec
Post-Exposure				
	Bake		110°C	1 min
Develop				
	AZ300MIF			1 min 30 sec
	DI Water	Running		2 min

Observe				
SiO_2 Etch				
	ICP 1	145	CHF_3/CF_4 cond	1 min
		145 ~85 nm/min	CHF_3/CF_4	22 min 30 sec
		121	O_2 Clean	24 min
Al_2O_3 Wet Etch				
	AZ300MIF	~1.5 nm/min	500 rpm	30 min
	DI Water	Running		2 min
Strip				
	NMP		80°C	> 2 hrs
Clean				
	Isopropyl	Ultrasonic		3 min
	DI Water	Running		1 min

Appendix B: ATLAS Simulation Code

Presented here is the ATLAS code used to simulate VFinMOSFET. Units for mesh definition is in µm. This code will calculate the I-V characteristics of a device, as well as give a view of the fin at specified biases. *.set files were generated by configuring the view of a structure or plot, and saving it to the associated file name.

```
go atlas

#parameters
set sp=4
set tox=.05
set tc=.02
set h=3
set d=4
set W=.4
set dsub=1

#structure specification
mesh space.mult=1.0 periodic

##mesh
x.mesh loc=-.5*$sp-$tox-.5*$W width=.5*$sp h1=.1*$sp h2=$tox/5
x.mesh width=$tox n.spaces=5
x.mesh width=$W h1=$tox/5 h2=$tox/5 h3=.02 n.spaces=40
x.mesh width=$tox n.spaces=5
x.mesh width=.5*$sp h1=$tox/5 h2=.1*$sp
y.mesh loc=-$h depth=$tc h1=$tc/4 h2=$tc/8
y.mesh depth=$h-$tox-$tc n.spaces=40
y.mesh depth=$tox n.spaces=5
y.mesh depth=$d h1=$tox/5 h2=$d/10 h3=$d/10
y.mesh depth=$dsub n.spaces=5

##region
region num=1 material=gan polari
region num=2 material=gan y.max=-$h+$tc polari
region num=3 material=gan y.min=$d polari
region num=5 material=Al2O3 y.max=0 x.max=-$W/2
region num=5 material=Al2O3 y.max=0 x.min=$W/2
##electrode
electrode name=gate y.max=-$tox x.max=-$W/2-$tox
electrode name=gate y.max=-$tox x.min=$W/2+$tox
electrode name=source x.min=-$W/2 x.max=$W/2 top
electrode name=drain substrate
##doping
doping unif conc=1e15 n.type x.min=-$W/2 x.max=$W/2 y.min=-$h+$tc y.max=0
doping unif conc=1e15 n.type y.min=0
doping unif conc=1e19 n.type x.min=-$W/2 x.max=$W/2 y.max=-$h+$tc
doping unif conc=1e19 n.type y.min=$d
```

```
#material models specification
##material
material name=gan KP.SET2 POL.SET3

##models
models print calc.strain fermi

##contact
##Aluminum
contact name=source workfun=4.08
contact name=drain workfun=4.08
##Platinum
contact name=gate workfun=5.93

#numerical method selection
##models
models print calc.strain fermi
##method
method gummel newton carriers=2

output charge con.band val.band polar.charge
save outf=mesh.str
solve outfile=out0
save outf=out0.str

#Bias Point - off
set Vd=20
set Vg=0

solve initial
solve Vdrain=0 Vgate=0 vstep=1 vfinal=$Vg name=gate

log outf=biasVdoff.log
solve Vdrain=0 Vgate=$Vg vstep=1 vfinal=$Vd name=drain
log off

tonyplot biasVdoff.log -set Vdsweep.set

solve Vdrain=$Vd Vgate=$Vg
save outf=BiasPoff.str

extract init infile="BiasPoff.str"
extract outf="con_band" 2d.conc.file impurity="Conduction Band Energy"
  material="All"
extract outf="val_band" 2d.conc.file impurity="Valence Band Energy"
  material="All"
tonyplot BiasPoff.str -set e-conc.set
tonyplot BiasPoff.str -set current-log.set
tonyplot BiasPoff.str -set E-field.set
tonyplot BiasPoff.str -set potential.set

#Bias Point - on
#set Vd=20
set Vg=5

#solve initial
#solve Vdrain=0 Vgate=0 vstep=1 vfinal=$Vg name=gate
```

```
log outf=biasVdon.log
#solve Vdrain=0 Vgate=$Vg vstep=1 vfinal=$Vd name=drain
solve Vdrain=$Vd Vgate=0 vstep=.5 vfinal=$Vg name=gate
log off

tonyplot biasVdon.log -set Vdsweep.set

solve Vdrain=$Vd Vgate=$Vg
save outf=BiasPon.str

extract init infile="BiasPon.str"
extract outf="con_band" 2d.conc.file impurity="Conduction Band Energy"
  material="All"
extract outf="val_band" 2d.conc.file impurity="Valence Band Energy"
  material="All"
tonyplot BiasPon.str -set e-conc.set
tonyplot BiasPon.str -set current-log.set
tonyplot BiasPon.str -set E-field.set
tonyplot BiasPon.str -set potential.set

#Vg Sweep
set Vg1=-4
set Vg2=8
set Vd=10

solve initial
solve Vgate=0 vstep=-1 vfinal=$Vg1 name=gate
solve Vdrain=0 vstep=1 vfinal=$Vd name=drain

log outf=Vgsweep.log
solve Vdrain=$Vd Vgate=$Vg1 vstep=.5 vfinal=$Vg2 name=gate
log off

tonyplot Vgsweep.log

#Vd Sweep
set Vd1=0
set Vd2=20
set dVd=.2

solve initial
solve Vdrain=0 Vgate=-2 vstep=1 vfinal=8 name=gate outfile=Vd0Vg0

log outf=Vdsweep.log
load infile=Vd0Vg0
solve Vdrain=0 Vgate=-2 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg1
solve Vdrain=0 Vgate=-1 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg2
solve Vdrain=0 Vgate=0 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg3
solve Vdrain=0 Vgate=1 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg4
solve Vdrain=0 Vgate=2 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg5
solve Vdrain=0 Vgate=3 vstep=$dVd vfinal=$Vd2 name=drain
```

```
load infile=Vd0Vg6
solve Vdrain=0 Vgate=4 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg7
solve Vdrain=0 Vgate=5 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg8
solve Vdrain=0 Vgate=6 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0Vg9
solve Vdrain=0 Vgate=7 vstep=$dVd vfinal=$Vd2 name=drain
load infile=Vd0VgA
solve Vdrain=0 Vgate=8 vstep=$dVd vfinal=$Vd2 name=drain
log off

tonyplot Vdsweep.log -set Vdsweep.set

quit
```

Appendix C: MATLAB Model Code

The model consists of three files. The first file solves for I-V by sending the bias conditions to the functions in the other two files, and solving for the combination of multiple models if necessary. It is split up into different segments with each segment solving one set of models together and plotting them. The second and third files are the models solving for the fin current and the Schottky diode current respectively. They take the bias voltages and optionally temperature as inputs, and output current as the output.

```
% Fin Current
clear
j = 0;
figure
hold on
a = 300e-7; % cm
Z = 50e-4; % cm
for Vgs=0:8
    j=j+1;
    i = 0;
    for Vds=0:.1:12
        i=i+1;
        Id(j,i)=jfet_model(Vgs,Vds,300);
    end
    plot(0:.1:12,Id(j,:)/(a*Z),'LineWidth',1.5)
    leg(j) = cellstr(sprintf('V_g_s = %G V',Vgs));
    %leg[j,:] = sprintf('V_g_s = %f V',Vgs);
end
legend(leg,'Location','Best')

% Plot Labels
xlabel('V_D_S (V)','FontSize',20)
ylabel('I_D (A/cm^2)','FontSize',20)
set(gca,'Box','off','FontSize',16)
% title('2DEG on Sidewalls','FontSize',20)
% title('Open Fin Current','FontSize',20)

L = get(gca,'YLim');
set(gca,'YLim',L,'YTick',def_ticks(L))

% Vgs Sweep
clear
j = 0;
figure
hold on
a = 300e-7; % cm
Z = 50e-4; % cm
Vds = 1; % V
```

```
vgs = 0:.1:8;
for Vgs = vgs
    j=j+1;
    Id(j)=jfet_model(Vgs,Vds,300);
end
[hax,hl1,hl2] = plotyy(vgs,Id/(a*Z),vgs(1:end-
1),diff(Id)./(diff(vgs)*(a*Z)));
set(hl1,'LineWidth',1.5);
set(hl2,'LineWidth',1.5);
xlabel('V_G_S (V)','FontSize',20)
ylabel(hax(1),'I_D (A/cm^2)','FontSize',20)
ylabel(hax(2),'g_m (S/cm^2)','FontSize',20)
L1 = hax(1).YLim;
L2 = hax(2).YLim;
set(hax(1),'Box','off','FontSize',16,'YLim',L1,'YTick',def_ticks(L1))
set(hax(2),'Box','off','FontSize',16,'YLim',[0 L2(2)],'YTick',def_ticks([0
L2(2)]))
% title('2DEG on Sidewalls','FontSize',20)
% title('Open Fin Current','FontSize',20)

% Source Diode Current
clear
Vd = -5:.01:5;
for i = 1:length(Vd)
    Id(i)=source_model(-Vd(i),300);
end
a = 300e-7; % cm
Z = 50e-4; % cm
figure
plot(Vd,Id/(a*Z))
figure
plot(Vd,log10(abs(Id)/(a*Z)),'LineWidth',1.5)
% xlabel('Voltage Across Source - V')
% ylabel('Current - log_1_0(A)')
xlabel('Schottky Voltage (V)','FontSize',16)
ylabel('Current Density - log_1_0(A/cm^2)','FontSize',16)
L = [-4 3];
set(gca,'Box','off','FontSize',14,'YLim',L,'YTick',def_ticks(L))
set(gca,'XLim',[-5 1])

% Device
clear
options = optimset('Display','none','TolFun',1e-12,'TolX',1e-12);
j = 0;
f1 = figure;
hold on
f2 = figure;
hold on
f3 = figure;
hold on
for Vgs=0:5
    j=j+1;
    i = 0;
    vo = 0;
    for Vds=0:.1:12
        i=i+1;
```

```
%           V = fminbnd(@(v)(jfet_model(Vgs-v,Vds-v) -
source_model(v)),0,Vds,options);
        V = fsolve(@(v)(jfet_model(Vgs-v,Vds-v) -
source_model(v)),vo,options);
        Id(j,i) = jfet_model(Vgs-V,Vds-V);
        Vs(j,i) = V;
        err(j,i) = Id(j,i) - source_model(V);
        vo = V;
    end
    figure(f1)
    plot(0:.1:12,Id(j,:))
    figure(f2)
    plot(0:.1:12,Vs(j,:))
    figure(f3)
    plot(0:.1:12,err(j,:))
end

% Fin with drain resistance
clear
options = optimset('Display','none','TolFun',1e-12,'TolX',1e-12);
j = 0;
f1 = figure;
hold on
f2 = figure;
hold on
f3 = figure;
hold on
mun = 600; % cm^2/Vs
q = 1.602e-19; % C
N = 5e15; % cm^-3
a = 300e-7; % cm
Z = 50e-4; % cm
D = 1e-4; % cm
% Rd = 8; % ohms
Rd = D/(q*a*Z*N*mun); % ohms
% Rd = 1e-2/(a*Z); % ohms - ohm-cm^2 by cross section
for Vgs=0:8
    j=j+1;
    i = 0;
    vo = 0;
    for Vds=0:.1:12
        i=i+1;
%           V = fminbnd(@(v)(jfet_model(Vgs-v,Vds-v) -
source_model(v)),0,Vds,options);
        V = fsolve(@(v)(jfet_model(Vgs,v) - (Vds-v)/Rd),vo,options);
        Id(j,i) = jfet_model(Vgs,V);
        Vs(j,i) = V;
        err(j,i) = Id(j,i) - (Vds-V)/Rd;
        vo = V;
    end
    figure(f1)
    plot(0:.1:12,Id(j,:)/(a*Z),'LineWidth',1.5)
    figure(f2)
    plot(0:.1:12,Vs(j,:))
    figure(f3)
    plot(0:.1:12,err(j,:))
end
```

```
% Device - Parallel
clear
options = optimset('Display','none','TolFun',1e-12,'TolX',1e-12);
j = 0;
f1 = figure;
hold on
f2 = figure;
hold on
f3 = figure;
hold on
parfor Vgs=0:5
    Id = [];
    Vs = [];
    err = [];
    i = 0;
    vo = 0;
    for Vds=0:.1:12
        i=i+1;
%         V = fminbnd(@(v)(jfet_model(Vgs-v,Vds-v) -
source_model(v)),0,Vds,options);
        V = fsolve(@(v)(jfet_model(Vgs-v,Vds-v) -
source_model(v)),vo,options);
        Id(i) = jfet_model(Vgs-V,Vds-V);
        Vs(i) = V;
        err(i) = Id(i) - source_model(V);
        vo = V;
    end
    figure(f1)
    plot(0:.1:12,Id(j,:))
    figure(f2)
    plot(0:.1:12,Vs(j,:))
    figure(f3)
    plot(0:.1:12,err(j,:))
end
```

```
function [Id] = jfet_model(Vgs,Vds,temperature)

    if verLessThan('matlab', '8.2')
        options = optimset('Display','none','TolFun',1e-10,'TolX',1e-10);
    else
        options = optimoptions('fsolve','Display','none','TolFun',1e-10,
...
            'TolX',1e-10,'FinDiffType','central');
    end
    options2 = optimset('Display','none','TolFun',1e-10,'TolX',1e-10);

    k = 8.62e-5; % eV/K
    eps = 8.84e-14; % F/cm
    q = 1.602e-19; % C
    phi_b = 6.3-4.1; % eV
    Nc = 2.3e18; % cm^-3
    eps_gan = 8.9*eps; % F/cm
    eps_ox = 7*eps; % F/cm
    a = 300e-7; % cm
    Z = 50e-4; % cm
    Nd = 5e15; % 1/cm^3
    Lf = 3e-4; % cm
    tox = 50e-7; % cm
    mu_n = 600; % cm^2/V*s
    d = 1e-7; % cm
    vs = 4e7; % cm/s

    % temperature
    if nargin == 3
        T = temperature; % K
    else
        T = 300; % K
    end
    kT = k*T;

    % threshold voltage
    Vt = phi_b - kT*log(Nc/Nd);

    function id = Id1(L,V)
        % resistive
%         id = q*a*mu_n*Nd*Z*(V)/L;
        % accumulative
        id = Z/L * 2*mu_n/(tox/eps_ox + d/eps_gan) * (V*(Vgs - Vt) -
.5*V^2);
    end

    function id = Id2(L,V,Vg)
        % find saturation voltage
        Vsat = fsolve(@(x)(-mu_n/(vs*(L+mu_n/vs*x)) *
(x*(a+2*tox*eps_gan/eps_ox) ...
            - 2*q*Nd/(3*eps_gan)*((tox^2*eps_gan^2/eps_ox^2 +
2*eps_gan/(q*Nd)*(x + Vt - Vg))^(3/2) ...
            - (tox^2*eps_gan^2/eps_ox^2 + 2*eps_gan/(q*Nd)*(Vt -
Vg))^(3/2))) ...
            + 1/(L+mu_n/vs*x) * (a + 2*tox*eps_gan/eps_ox ...
            - 2*(tox^2*eps_gan^2/eps_ox^2 + 2*eps_gan/(q*Nd)*(x+Vt-
Vg))^(1/2))),V,options);
```

```
        % check if saturated and set current
        Vsat = real(Vsat);
        if V >= Vsat
            u = Vsat;
        else
            u = V;
        end
        id = q*mu_n*Nd*Z/(L + mu_n/vs*(u)) * ((u)*(a +
2*tox*eps_gan/eps_ox) ...
            - 2*q*Nd/(3*eps_gan)*((tox^2*eps_gan^2/eps_ox^2 +
2*eps_gan/(q*Nd)*(u + Vt - Vg))^(3/2) ...
            - (tox^2*eps_gan^2/eps_ox^2 + 2*eps_gan/(q*Nd)*(Vt -
Vg))^(3/2)));
    end

    % Determine if off
    if Vgs < Vt - (q*Nd*a/2)*(a/(4*eps_gan) + tox/eps_ox)
        Id = 0;
        return
    end

    % Determine Mode of Operation
    if Vt < Vgs - Vds
        % accumulation or resistive
        Id = Id1(Lf,Vds);
    elseif Vt < Vgs
        %Id1(L1,Vgs-Vt)
        %Id2(Lf-L1,Vds-(Vgs-Vt))
        f = @(l)(Id1(l,Vgs-Vt) - Id2(Lf-l,Vds-(Vgs-Vt),Vt));
        L1 = fminbnd(f,0,Lf,options2);
        Id = Id1(L1,Vgs-Vt);
    else
        % depletion
        Id = Id2(Lf,Vds,Vgs);
    end

end
```

```
function [Id] = source_model(Vd,temperature)

    options = optimset('Display','none','TolFun',1e-10,'TolX',1e-10);
    k = 8.62e-5; % eV/K
    eps = 8.84e-14; % F/cm
    q = 1.602e-19; % C
    hbar = 6.626e-34; % eV*s
    me = 9.11e-31; % kg
    %phi_Bn = 4.33-4.1; % eV
    phi_Bn = .5; % eV
    Nc = 2.3e18; % cm^-3
    eps_gan = 8.9*eps; % F/cm
    a = 300e-7; % cm
    Z = 50e-4; % cm
%      a = 100e-4; % cm
%      Z = 314e-4; % cm
    m_e = .2; % electron masses
    Ar = m_e*120; % A/cm^2-K^2
    Ndn = 2.6e18; % 1/cm^3
    Rs = .0078/(a*Z);

    % temperature
    if nargin == 2
        T = temperature; % K
    else
        T = 300; % K
    end
    kT = k*T;

    % Schottky Source Contact
    function id = thermal(V)
        id = -a*Z*Ar*T^2*exp(-phi_Bn/kT)*(exp(-V/kT)-1);
        if -V > 1*kT
            f = @(i)(i+a*Z*Ar*T^2*exp(-phi_Bn/kT)*(exp(-(V-i*Rs)/kT)-1));
            id = fminbnd(f,V/Rs,0,options);
            %id = fsolve(f,-1e-2,options);
        end
    end

    % Tunneling Integral Calculation
    function id = tunnel_int(Emax)
        %integral
        m_ = 2;
        B = 2*sqrt(8*me*m_)/(q*hbar*Emax);
        u = 0:phi_Bn/100000:phi_Bn;
        integrand = (q^2*kT*me*m_/(2*hbar^3*pi^2.5))*exp(-
B*(q*(u+phi_Bn)).^1.5).*exp(u/kT);
        id = a*Z*sum(integrand)*(u(2)-u(1))*q*1e-4;
    end

    % Tunneling Schottky Current
    function id = tunnel(V)
        Ws = 1e-2*sqrt(2*eps_gan*(phi_Bn + V - kT*log(Nc/Ndn))/(q*Ndn)); %
m
        Ws_rev = Ws * phi_Bn/(phi_Bn + V - kT*log(Nc/Ndn)); % m
        Emax = phi_Bn/Ws_rev; % V/m
        if Emax >= 0
```

```
%               id = Z*a*1e-
4*q^2*kT*me/(3*hbar^3*pi^2.5)*((q*hbar*Emax)^2/(32*me))^(1/3) ...
%                    *
gammainc(2/3,(2*sqrt(8*me)*(q*(phi_Bn))^1.5)/(q*hbar*Emax));
            id = tunnel_int(Emax);
        end
    end

    function id = rev_curr(V)
        id = tunnel(V) + thermal(V);
        if V > 1*kT
            f = @(i)(-i + tunnel(V-id*Rs) + thermal(V-id*Rs));
            %id = fminbnd(f,0,V/Rs,options);
        end
    end

    % Determine Mode of Operation
    if Vd == 0
        Id = 0;
    elseif Vd < 0
        Id = thermal(Vd);
    else
        %Id = thermal(Vd) + tunnel(Vd);
        Id = rev_curr(Vd);
    end
end
```

Appendix D: L-Edit Code for Mask Pattern

Multiple C++ files were created to generate the transistors for layout. Each file is a T-cell which generates a pattern that can be instanced in the layout GUI or another T-cell. The first file creates the layout for a single VFinMOSFET. The second file procedurally generates text of various sizes. The third file generates Vernier patterns, used to determine alignment of layers. The fourth file automatically generates a series of devices varying one parameter, while the fifth file generates an array of transistors of varying fin widths and spacings.

```
/*************************************************************************
 * Cell Name: FinFET
 * Creator  : (null)
 *
 * Revision History:
 * 23 Oct 2015    Generated by L-Edit
 *************************************************************************/
module FinFET_code
{
#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
#include "ldata.h"

/* Begin -- Remove this block if you are not using L-Comp. */
#include "lcomp.h"
/* End */

    /* TODO: Put local functions here. */
    double minim(double a, double b)
    {
        if(a<b)
        {
            return a;
        }
        else
        {
            return b;
        }
    }

    double maxim(double a, double b)
    {
        if(a>b)
        {
            return a;
        }
```

```
        else
        {
            return b;
        }
    }

    LObject sq_box(LCell cell, LLayer layer, double x0, double y0, double
x1, double y1)
    {
        LObject box;

        box = LBox_New(cell, layer, x0*1000, y0*1000, x1*1000, y1*1000);

        return box;
    }

    LObject torus(LCell cell, LLayer layer, double x0, double y0, double
r0, double r1, double th_st, double th_end)
    {
        LObject tor;
        LTorusParams s_tor;
        LPoint center;

        center = LPoint_Set(x0*1000, y0*1000);
        s_tor.ptCenter = center;
        s_tor.nInnerRadius = r0*1000;
        s_tor.nOuterRadius = r1*1000;
        s_tor.dStartAngle = th_st;
        s_tor.dStopAngle = th_end;
        tor = LTorus_CreateNew(cell, layer, &s_tor);

        return tor;
    }

    LObject pie(LCell cell, LLayer layer, double x0, double y0, double r,
double th_st, double th_end)
    {
        LObject pie;
        LPieParams s_pie;
        LPoint center;

        center = LPoint_Set(x0*1000, y0*1000);
        s_pie.ptCenter = center;
        s_pie.nRadius = r*1000;
        s_pie.dStartAngle = th_st;
        s_pie.dStopAngle = th_end;
        pie = LPie_CreateNew(cell, layer, &s_pie);

        return pie;
    }

    LObject round_box(LCell cell, LLayer layer, double x0, double y0,
double x1, double y1, double r)
    {
        LTorusParams s_tor;
        LPoint center;
        LObject box;
```

```
        LObject tors [4];

        box = sq_box(cell, layer, x0, y0, x1, y1);

        tors[0] = torus(cell, layer, minim(x0,x1)+r, minim(y0,y1)+r, r,
2*r, 180, 270);
        tors[1] = torus(cell, layer, minim(x0,x1)+r, maxim(y0,y1)-r, r,
2*r, 90, 180);
        tors[2] = torus(cell, layer, maxim(x0,x1)-r, maxim(y0,y1)-r, r,
2*r, 0, 90);
        tors[3] = torus(cell, layer, maxim(x0,x1)-r, minim(y0,y1)+r, r,
2*r, 270, 360);

        LCell_BooleanOperation(cell, LBoolOp_SUBTRACT, 0, &box, 1,
&tors[0], 4, layer, LTRUE);

        box = LObject_GetList(cell, layer);
        return box;
    }

    void FinFET_main(void)
    {
        /* Begin DO NOT EDIT SECTION generated by L-Edit */
        LCell          cellCurrent    = (LCell)LMacro_GetNewTCell();
        int             n               =
(int)LCell_GetParameter(cellCurrent, "n");
        double          w               = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "w"));
        double          l               = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "l"));
        double          s               = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "s"));
        /* End DO NOT EDIT SECTION generated by L-Edit */

        /* Begin -- Remove this block if you are not using L-Comp. */
        LC_InitializeState();
        LC_CurrentCell = cellCurrent;
        /* End */

        /* TODO: Put local variables here. */
        LFile pFile         = LCell_GetFile( cellCurrent );

        LLayer oxide         = LLayer_Find(pFile, "Oxide");
        LLayer source         = LLayer_Find(pFile, "Source");
        LLayer regrowth    = LLayer_Find(pFile, "Regrowth");
        LLayer gate          = LLayer_Find(pFile, "Gate");
        LLayer pad            = LLayer_Find(pFile, "Source Pad");
        LLayer fin            = LLayer_Find(pFile, "Fin");
        LLayer finmask        = LLayer_Find(pFile, "Fin Mask");
        LLayer align         = LLayer_Find(pFile, "Align");
        LLayer implant        = LLayer_Find(pFile, "Implant");
        LLayer ebsource    = LLayer_Find(pFile, "Ebeam Source");
        LLayer gate2         = LLayer_Find(pFile, "Gate2");

        LObject box,box_g,box_i;

        double x_cont, y_cont, c;
```

```
        int i;
        double r;

        LTorusParams s_tor;
        LPoint center;
        LObject pies [2];

        /* TODO: Begin custom generator code.*/

        LCell_SetLock(cellCurrent, 0);

        x_cont = n*(s + w) + s;
        if (x_cont < 50)
        {
            x_cont = 50;
        }
        y_cont = 50;

        r = 2;

        c = (n*(s+w)-s)/2;

        for (i=0; i<n; i++)
        {
            box = sq_box(cellCurrent, fin, i*(s+w), -4, i*(s+w)+w, l);

            // Rounding source to pad connection
            pies[0] = pie(cellCurrent, fin, i*(s+w)-r, -4+r, r, 270, 0);
            pies[1] = pie(cellCurrent, fin, i*(s+w)+w+r, -4+r, r, 180,
270);
            box = sq_box(cellCurrent, fin, i*(s+w)-2, -4, i*(s+w)+w+2, -
2);
            LCell_BooleanOperation(cellCurrent, LBoolOp_SUBTRACT, 0, &box,
1, &pies[0], 2, fin, LTRUE);
        }

        // Source Pad
        round_box(cellCurrent, fin, c-2-x_cont/2, -4-y_cont-8,
c+2+x_cont/2, -4, 5);
        round_box(cellCurrent, source, c-x_cont/2, -4-y_cont-6,
c+x_cont/2, -6, 3);
        round_box(cellCurrent, oxide, c-4-x_cont/2, -4-y_cont-10,
c+4+x_cont/2, 0, 7);
        round_box(cellCurrent, pad, c+2-x_cont/2, -4-y_cont-4, c-
2+x_cont/2, -8, 3);

        // Gate
        round_box(cellCurrent, gate2, -s-4, -2, n*(s+w)+4, l+8, 4);
        round_box(cellCurrent, gate2, c-x_cont/2, l+4, c+x_cont/2,
l+y_cont+4, 4);

        /* End custom generator code.*/
    }
}
FinFET_main();
```

```
/**************************************************************************
 * Cell Name: Text
 * Creator  : (null)
 *
 * Revision History:
 * 25 Nov 2015    Generated by L-Edit
 **************************************************************************/
module Text_code
{
#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
#include "ldata.h"

/* Begin -- Remove this block if you are not using L-Comp. */
#include "lcomp.h"
/* End */

    /* TODO: Put local functions here. */

    void PlaceCharacter(char ch)
    {
        if ( isalnum( ch ) )
            LC_Position( LFormat("_alphabet_%c", toupper( ch )));
        /* otherwise, need to special-case it */
        else if (isspace( ch ))
            LC_Position("_alphabet_space");
        else {
            switch ( ch ) {
                case '+': LC_Position("_alphabet_+"); break;
                case '-': LC_Position("_alphabet_-"); break;
                case '_': LC_Position("_alphabet__"); break;
                case '*': LC_Position("_alphabet_*"); break;
                case ':': LC_Position("_alphabet_colon"); break;
                case '\'': LC_Position("_alphabet_apostrophe"); break;
                case '/': LC_Position("_alphabet_slash"); break;
                //case '\\': LC_Position("_alphabet_backslash"); break;
                case '.': LC_Position("_alphabet_period"); break;
                case ',': LC_Position("_alphabet_comma"); break;
                case '(': LC_Position("_alphabet_("); break;
                case ')': LC_Position("_alphabet_)"); break;
                default:
                    LDialog_MsgBox ( LFormat ( "Unknown character '%c'
(code %d)\n", ch, ch ));
            }
        }
    }

    void convert_string(char *s)
    {
        while (*s)
        {
            /* note hardwired check for \ */
            if (*s == 92 && *(s+1) == 'n')
            {
                char *f = s;
```

```
                *f++ = '\n';
                for ( ; *(f+1) ; f++)
                *f = *(f+1);
                *f = '\0';
            }
            s++;
        }
    }

    void Text_main(void)
    {
        /* Begin DO NOT EDIT SECTION generated by L-Edit */
        LCell          cellCurrent    = (LCell)LMacro_GetNewTCell();
        const char*     text           = (const
char*)LCell_GetParameter(cellCurrent, "text");
        /* End DO NOT EDIT SECTION generated by L-Edit */

        /* Begin -- Remove this block if you are not using L-Comp. */
        LC_InitializeState();
        LC_CurrentCell = cellCurrent;
        /* End */

        /* TODO: Put local variables here. */
        char s[1000];
        char *t;
        int first = 1;

        /* TODO: Begin custom generator code.*/
        LCell_SetLock(cellCurrent, 0);

        strcpy(s,text);
        convert_string(s);

        LC_SetCompositionDirection(HORIZONTAL);
        LC_SetReferencePoint(LL);

        for (t = s; *t; t++)
        {
            if ( *t == '\n' )
            {
                LC_SetXPlacementPosition(0);
                LC_IncrementYPlacementPosition(-
LC_GetElementHeight("_alphabet_A"));
            }
            else {
                PlaceCharacter(*t);
            }
        }
        LC_CellClose(UPDATE_ABUT);

        /* End custom generator code.*/
    }
}
Text_main();
```

```
/**********************************************************************
 * Cell Name: Vernier
 * Creator  : (null)
 *
 * Revision History:
 * 2 Dec 2015    Generated by L-Edit
 **********************************************************************/
module Vernier_code
{
#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
#include "ldata.h"

/* Begin -- Remove this block if you are not using L-Comp. */
#include "lcomp.h"
/* End */

    /* TODO: Put local functions here. */
    LObject sq_box(LCell cell, LLayer layer, double x0, double y0, double
x1, double y1)
    {
        LObject box;

        box = LBox_New(cell, layer, x0*1000, y0*1000, x1*1000, y1*1000);

        return box;
    }

    LInstance text_gen(LCell cell, char* tex, double x, double y, int num,
int den, int rot)
    {

        char* texts[3];
        LMagnification mag;
        LOrientation_Ex99 orient;
        LTransform_Ex99 scale;
        LInstance t;

        mag.denom = den;
        mag.num = num;
        texts[0] = "text";
        texts[1] = tex;
        texts[2] = NULL;

        t = LC_Generate("Text","Text_A",texts);

        switch (rot)
        {
            case 0: orient = LRotate0; break;
            case 90: orient = LRotate90; break;
            case 180: orient = LRotate180; break;
            case 270: orient = LRotate270; break;
            default:
                LDialog_MsgBox ( LFormat ( "Text Rotation Not Valid:
'%d'\n", rot));
```

```
        }

        scale = LTransform_Set_Ex99(x,y,orient,mag);

LInstance_Set_Ex99(cell,t,scale,LPoint_Set(1,1),LPoint_Set(1000,1000));

        return t;
    }

    void Vernier_main(void)
    {
        /* Begin DO NOT EDIT SECTION generated by L-Edit */
        LCell           cellCurrent     = (LCell)LMacro_GetNewTCell();
        int              res             =
(int)LCell_GetParameter(cellCurrent, "res");
        LLayer           layer1          =
(LLayer)LCell_GetParameter(cellCurrent, "layer1");
        const char*      tex1            = (const
char*)LCell_GetParameter(cellCurrent, "tex1");
        LLayer           layer2          =
(LLayer)LCell_GetParameter(cellCurrent, "layer2");
        const char*      tex2            = (const
char*)LCell_GetParameter(cellCurrent, "tex2");
        /* End DO NOT EDIT SECTION generated by L-Edit */

        /* Begin -- Remove this block if you are not using L-Comp. */
        LC_InitializeState();
        LC_CurrentCell = cellCurrent;
        /* End */

        /* TODO: Put local variables here. */
        LFile pFile          = LCell_GetFile( cellCurrent );

        LLayer oxide          = LLayer_Find(pFile, "Oxide");
        LLayer source          = LLayer_Find(pFile, "Source");
        LLayer regrowth     = LLayer_Find(pFile, "Regrowth");
        LLayer gate          = LLayer_Find(pFile, "Gate");
        LLayer pad              = LLayer_Find(pFile, "Source Pad");
        LLayer fin              = LLayer_Find(pFile, "Fin");
        LLayer finmask          = LLayer_Find(pFile, "Fin Mask");
        LLayer align          = LLayer_Find(pFile, "Align");
        LLayer implant          = LLayer_Find(pFile, "Implant");
        LLayer ebsource     = LLayer_Find(pFile, "Ebeam Source");
        LLayer gate2          = LLayer_Find(pFile, "Gate2");

        /* TODO: Begin custom generator code.*/

        double h;
        double pos;
        int i;

        for(i=0;i<=10;i++)
        {
            if(i==0)
            {
                sq_box(cellCurrent, layer1, -2.5, 0, 2.5, 50);
                sq_box(cellCurrent, layer2, -2.5, 0, 2.5, -30);
```

```
            }
            else
            {
                h = 30;
                if(i==5||i==10)
                {
                    h = 40;
                }

                sq_box(cellCurrent, layer1, -2.5-10*i, 0, 2.5-10*i, h);
                sq_box(cellCurrent, layer1, -2.5+10*i, 0, 2.5+10*i, h);
                sq_box(cellCurrent, layer2, -2.5-(10+(double)res/1000)*i,
0, 2.5-(10+(double)res/1000)*i, -30);
                sq_box(cellCurrent, layer2, -2.5+(10+(double)res/1000)*i,
0, 2.5+(10+(double)res/1000)*i, -30);
                pos = 2.5+(10+res/1000)*i;
            }
            if((res<100)&&(i==5))
            {
                break;
            }
        }

        text_gen(cellCurrent, tex1, (-pos-5)*1000, 5000, 1, 3, 90);
        text_gen(cellCurrent, tex2, (-pos-5)*1000, -30000, 1, 3
        , 90);


        /* End custom generator code.*/
    }
}
Vernier_main();
```

```
/***************************************************************************
 * Cell Name: Series
 * Creator  : (null)
 *
 * Revision History:
 * 30 Nov 2015    Generated by L-Edit
 ***************************************************************************/
module Series_code
{
#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
#include "ldata.h"

/* Begin -- Remove this block if you are not using L-Comp. */
#include "lcomp.h"
/* End */

#define Nn 12
#define Nw 9
#define Nl 10
#define Ns 6

    /* TODO: Put local functions here. */
    LInstance text_gen(LCell cell, char* tex, double x, double y, int num,
int den, int rot)
    {

        char* texts[3];
        LMagnification mag;
        LOrientation_Ex99 orient;
        LTransform_Ex99 scale;
        LInstance t;

        mag.denom = den;
        mag.num = num;
        texts[0] = "text";
        texts[1] = tex;
        texts[2] = NULL;

        t = LC_Generate("Text","Text_A",texts);

        switch (rot)
        {
            case 0: orient = LRotate0; break;
            case 90: orient = LRotate90; break;
            case 180: orient = LRotate180; break;
            case 270: orient = LRotate270; break;
            default:
                LDialog_MsgBox ( LFormat ( "Text Rotation Not Valid:
'%d'\n", rot));
        }

        scale = LTransform_Set_Ex99(x,y,orient,mag);

LInstance_Set_Ex99(cell,t,scale,LPoint_Set(1,1),LPoint_Set(1000,1000));
```

```
        return t;
    }

    void Series_main(void)
    {
        /* Begin DO NOT EDIT SECTION generated by L-Edit */
        LCell          cellCurrent     = (LCell)LMacro_GetNewTCell();
        const char*      title            = (const
char*)LCell_GetParameter(cellCurrent, "title");
        int              n                =
(int)LCell_GetParameter(cellCurrent, "n");
        double           w                = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "w"));
        double           l                = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "l"));
        double           s                = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "s"));
        const char*      var              = (const
char*)LCell_GetParameter(cellCurrent, "var");
        /* End DO NOT EDIT SECTION generated by L-Edit */

        /* Begin -- Remove this block if you are not using L-Comp. */
        LC_InitializeState();
        LC_CurrentCell = cellCurrent;
        /* End */

        /* TODO: Put local variables here. */
        LFile pFile          = LCell_GetFile( cellCurrent );

        LLayer oxide          = LLayer_Find(pFile, "Oxide");
        LLayer source          = LLayer_Find(pFile, "Source");
        LLayer regrowth    = LLayer_Find(pFile, "Regrowth");
        LLayer gate          = LLayer_Find(pFile, "Gate");
        LLayer pad             = LLayer_Find(pFile, "Source Pad");
        LLayer fin             = LLayer_Find(pFile, "Fin");
        LLayer finmask         = LLayer_Find(pFile, "Fin Mask");
        LLayer align          = LLayer_Find(pFile, "Align");
        LLayer implant         = LLayer_Find(pFile, "Implant");
        LLayer ebsource    = LLayer_Find(pFile, "Ebeam Source");
        LLayer gate2          = LLayer_Find(pFile, "Gate2");

        LInstance fet,t;

        int n_[Nn] = {1,2,3,4,5,6,7,8,9,10,11,12};
        double w_[Nw] = {.3,.4,.5,.6,.8,1,1.2,1.5,2};
        double l_[Nl] = {20,30,40,50,60,80,100,150,200,250};
        double s_[Ns] = {1,2,3,4,5,6};
        double x,pitch;
        int i, N;
        char* params[9];

        params[0] = "n";
        params[1] = LFormat("%d",n);
        params[2] = "w";
        params[3] = LFormat("%f",w);
        params[4] = "l";
```

```
        params[5] = LFormat("%f",l);
        params[6] = "s";
        params[7] = LFormat("%f",s);
        params[8] = NULL;

        /* TODO: Begin custom generator code.*/
        LCell_SetLock(cellCurrent, 0);

        switch (var[0])
        {
            case 'n':
                N = Nn;
                break;
            case 'w':
                N = Nw;
                break;
            case 'l':
                N = Nl;
                break;
            case 's':
                N = Ns;
                break;
            default:
                LDialog_MsgBox ( LFormat ( "Series type not valid:
'%s'\n", var));
        }

        x = 0;

        for(i=0;i<N;i++)
        {
            switch (var[0])
            {
                case 'n':
                    params[1] = LFormat("%d",n_[i]);
                    t =
text_gen(cellCurrent,LFormat("%d",n_[i]),x*1000+25000,-15000,1,2,0);
                    break;
                case 'w':
                    params[3] = LFormat("%f",w_[i]);
                    t = text_gen(cellCurrent,LFormat("%.1f
um",w_[i]),x*1000+10000,-15000,1,2,0);
                    break;
                case 'l':
                    params[5] = LFormat("%f",l_[i]);
                    t = text_gen(cellCurrent,LFormat("%.0f
um",l_[i]),x*1000+10000,-15000,1,2,0);
                    break;
                case 's':
                    params[7] = LFormat("%f",s_[i]);
                    t = text_gen(cellCurrent,LFormat("%.1f
um",s_[i]),x*1000+10000,-15000,1,2,0);
                    break;
                default:
                    LDialog_MsgBox ( LFormat ( "Series type not valid:
'%s'\n", var));
            }
```

```
            if((2*i==N-1)||(2*i==N-2))
            {
                LC_SetXYPlacementPosition(0,0);

                t = text_gen(cellCurrent,title,x*1000,-45000,2,2,0);
            }

            LC_SetXYPlacementPosition(x*1000,0);
            fet = LC_Generate("FinFET","FinFET_A",params);
            pitch = LC_GetElementWidth("FinFET_A");
            x = x + pitch/1000 + 10;
            //LDialog_MsgBox ( LFormat ( "Pitch: '%f'\n", pitch));
        }

        /* End custom generator code.*/
    }
}
Series_main();
```

```
/***********************************************************************
 * Cell Name: Fin v Spacing Array 2
 * Creator  : (null)
 *
 * Revision History:
 * 25 Nov 2015    Generated by L-Edit
 ***********************************************************************/
module Fin_v_Spacing_Array_2_code
{
#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
#include "ldata.h"

/* Begin -- Remove this block if you are not using L-Comp. */
#include "lcomp.h"
/* End */

    /* TODO: Put local functions here. */
    LInstance text_gen(LCell cell, char* tex, double x, double y, int num,
int den, int rot)
    {

        char* texts[3];
        LMagnification mag;
        LOrientation_Ex99 orient;
        LTransform_Ex99 scale;
        LInstance t;

        mag.denom = den;
        mag.num = num;
        texts[0] = "text";
        texts[1] = tex;
        texts[2] = NULL;

        t = LC_Generate("Text","Text_A",texts);

        switch (rot)
        {
            case 0: orient = LRotate0; break;
            case 90: orient = LRotate90; break;
            case 180: orient = LRotate180; break;
            case 270: orient = LRotate270; break;
            default:
                LDialog_MsgBox ( LFormat ( "Text Rotation Not Valid:
'%d'\n", rot));
        }

        scale = LTransform_Set_Ex99(x,y,orient,mag);

LInstance_Set_Ex99(cell,t,scale,LPoint_Set(1,1),LPoint_Set(1000,1000));

        return t;
    }

    void Fin_v_Spacing_Array_2_main(void)
```

```
    {
        /* Begin DO NOT EDIT SECTION generated by L-Edit */
        LCell          cellCurrent    = (LCell)LMacro_GetNewTCell();
        int            n              =
(int)LCell_GetParameter(cellCurrent, "n");
        double         l               = LAtoF((const
char*)LCell_GetParameter(cellCurrent, "l"));
        /* End DO NOT EDIT SECTION generated by L-Edit */

        /* Begin -- Remove this block if you are not using L-Comp. */
        LC_InitializeState();
        LC_CurrentCell = cellCurrent;
        /* End */

        /* TODO: Put local variables here. */
        LFile pFile         = LCell_GetFile( cellCurrent );

        LLayer oxide         = LLayer_Find(pFile, "Oxide");
        LLayer source         = LLayer_Find(pFile, "Source");
        LLayer regrowth     = LLayer_Find(pFile, "Regrowth");
        LLayer gate          = LLayer_Find(pFile, "Gate");
        LLayer pad            = LLayer_Find(pFile, "Source Pad");
        LLayer fin            = LLayer_Find(pFile, "Fin");
        LLayer finmask        = LLayer_Find(pFile, "Fin Mask");
        LLayer align          = LLayer_Find(pFile, "Align");
        LLayer implant        = LLayer_Find(pFile, "Implant");
        LLayer ebsource     = LLayer_Find(pFile, "Ebeam Source");
        LLayer gate2         = LLayer_Find(pFile, "Gate2");

        LInstance fet,t;

        double w[9] = {.3,.4,.5,.6,.8,1,1.2,1.5,2};
        double s[6] = {1,2,3,4,5,6};
        double x,y;
        int i,j;
        char* params[9];

        params[0] = "n";
        params[1] = LFormat("%d",n);
        params[2] = "w";
        params[4] = "l";
        params[5] = LFormat("%f",l);
        params[6] = "s";
        params[8] = NULL;


        /* TODO: Begin custom generator code.*/
        LCell_SetLock(cellCurrent, 0);

        for(i=0;i<9;i++)
        {
            params[3] = LFormat("%f",w[i]);
            x = (58+10)*i;
            for(j=0;j<6;j++)
            {
                params[7] = LFormat("%f",s[j]);
                y = (168+10)*j;
```

```
                LC_SetXYPlacementPosition(x*1000,y*1000);
                fet = LC_Generate("FinFET","FinFET_A",params);
                if(i==0)
                {
                    t = text_gen(cellCurrent,LFormat("%.1f um",s[j]),-
15000,y*1000+10000,1,2,90);
                }
            }
            t = text_gen(cellCurrent,LFormat("%.1f
um",w[i]),x*1000+10000,-15000,1,2,0);
        }


        LC_SetXYPlacementPosition(0,0);

        t = text_gen(cellCurrent,"Spacing",-
45000,3*(168+10)*1000+10000,2,2,90);
        t = text_gen(cellCurrent,"Fin Width",4*(58+10)*1000+10000,-
45000,2,2,0);

        /* End custom generator code.*/
    }
}

Fin_v_Spacing_Array_2_main();
```

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