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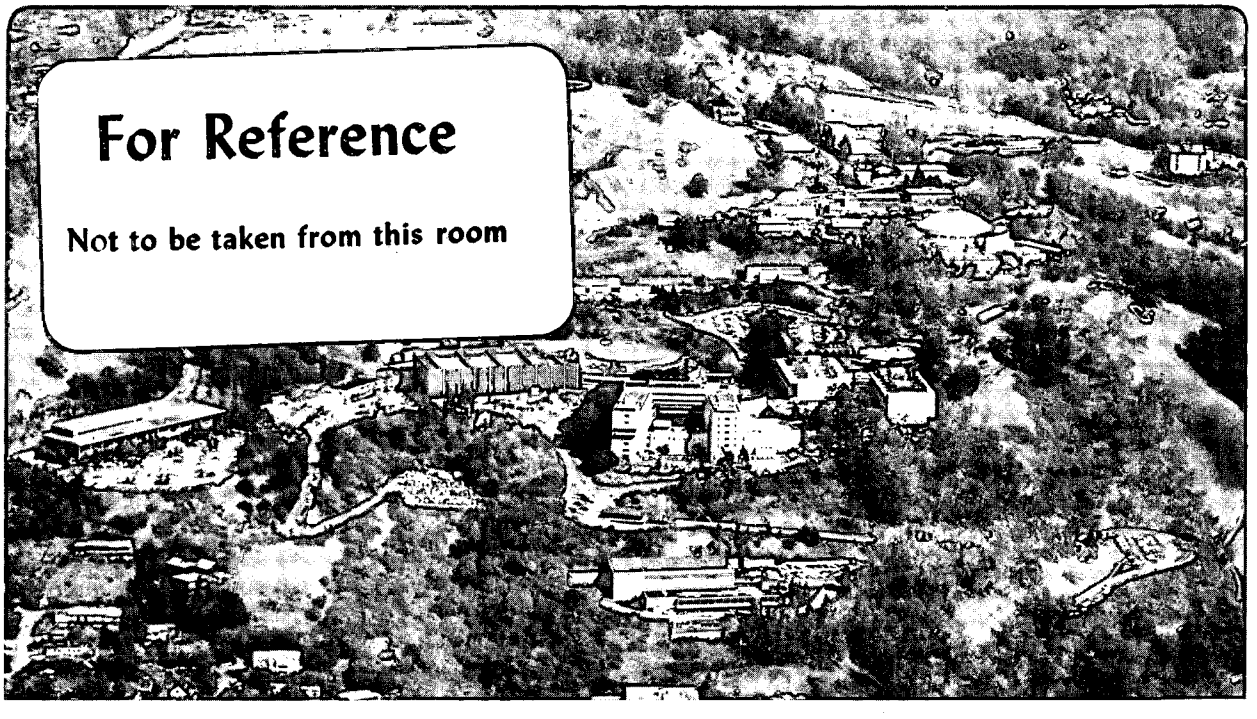

DISCLAIMER

SELECTION OF THE PROPER CCD DEVICE AND CONDITIONS OF OPERATION

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An application such as the Time Projection Chamber**, requires a Charge-Coupled Device (CCD) having the following characteristics:

Dynamic Range ≈200

Frequency of Operation 10 MHz

Number of Cells 200<N<250

Note 1:

The frequency of 10 MHz is related to a given shape of the pulse appearing on the wire. It allows at least three samples on each (typical) signal, without pile-up effects on the wire. This frequency is also related to the time slice on Z axis: that is, drift-time measurement. However, it might be useful to review the frequency criteria - tolerance margin.

Actually, two devices can, according to preliminary tests, fulfill the requirements on the Time Projection Chamber. Both are Fairchild devices:

FSC - CCD 311

FSC - CCD 321

Both have been tried on a very preliminary basis and evaluated in terms of read-in, read-out schemes - driver requirements, energy consumption. These evaluations have allowed the demonstration of the feasibility and conditions of operation of the project, as well as to obtain price information on that part of the electronic data acquisition system.

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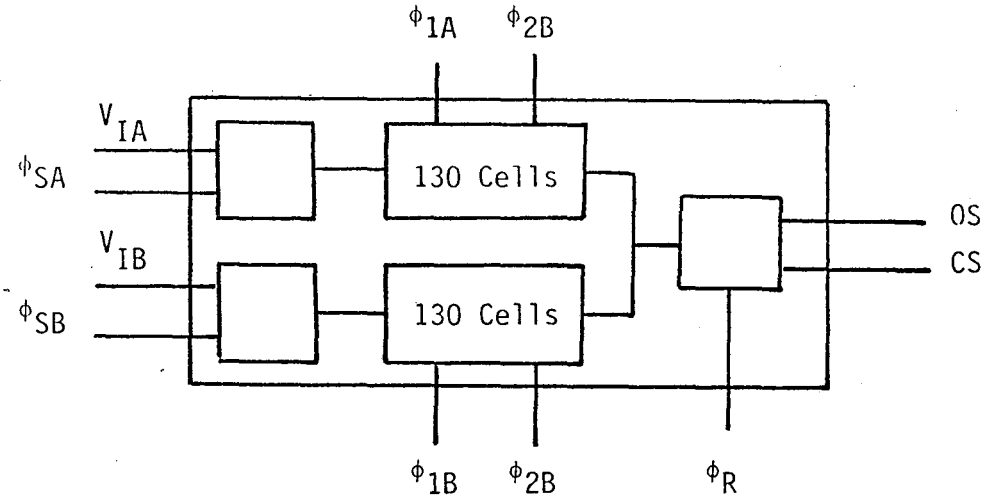
**Reference to TPC.

Internal Organization of CCD 311 and CCD 321

CCD 311

DC inputs not shown



Notes:

1. This device has the capacity to memorize one analog data channel

   ϕ_{SA}, ϕ_{SB} } are two different waveforms

   $\phi_{1A} = \phi_{2B}$

   $\phi_{1B} = \phi_{2A}$

   ϕ_R is the only clock at 10 MHz - due to the dual transport organization; all other clocks are at 5 MHz.

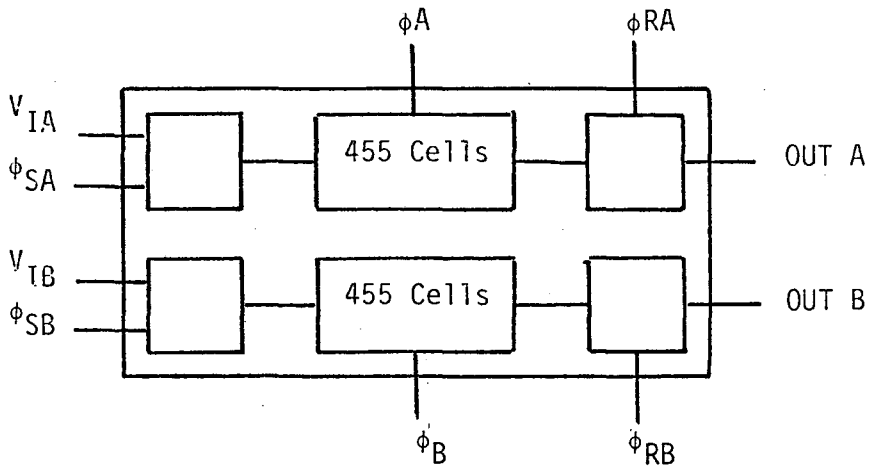
2. This organization presents the advantage of a fairly low shift frequency (5 MHz), although, the device has, in fact, an 8 MHz capability. For the same transport shift-register capacitance, the power consumption is halved.

3. The main disadvantages lies in the fact that the two channels have different responses: linearity, dark current, leading to a more intricate set of corrections at the computer level, and that five different clocks have to be distributed. There is also the need for a differential amplifier at the output.

4. Two analog channels are multiplexed on to each CCD channel input. Thus four channels can be stored in one device but the clock frequency had to go up to 20 MHz. This principle is shown in Appendix I, Figure AI-3. The total number of drivers is decreased; although, the requirements on each driver are more stringent.

Internal Organization of CCD 321

DC inputs not shown



Notes:

1. This device has a sufficiently large number of cells to allow up to four analog data channels (each of 225 samples) to be memorized.

2. The system is a dual independent transport shift register. The number of clock signals needed to operate a device in this application is only two (taking into consideration that all channels will work in parallel). However, the clock speed must be at least 10 MHz.

$$\phi_{SA} = \phi_{SB} = \phi_{RA} = \phi_{RB}$$
$$\phi_A = \phi_B$$

3. Two analog channels as input, one to each CCD channel. The cell capacity is underused by a factor of two - clock frequency is 10 MHz.

4. Two analog channels are multiplexed on to each CCD channel input. Thus four channels can be stored in one device but the clock frequency has to go up to 20 MHz. This principle is described in Appendix 1-3. The total number of drivers is decreased; although, the requirements on each driver are more stringent.

The principal limitation resides in the non-zero transfer inefficiency which can induce a spillover from a sample of an analog channel onto the following sample of the other analog channel. This spillover might be corrected, however, assuming that they are measured by a previous or separate test.

Read-out Schemes

The read-out scheme is dependent on three elements:

1. The maximum conversion speed for 9 bits A.D.C. taking into account speed/price tradeoffs.
2. The maximum dead-time due to a full read-out of all memories. Although the counting rate is fairly low, i.e., one event per second, a capability of 100 triggers per second (that is, 10 msec dead-time) may allow relaxed requirements on the trigger.
3. The capability of the CCD device to retain the information without too much degradation due to the dark current originating from thermally generated carriers filling the potential wells.

Speed/price trade-offs for A.D.C. is heavily dependent on the technology. Price is likely to decrease as technology matures. Usually, these fast A.D.C.'s are built from discrete components or hybrids and hence much less susceptible to price drops than integrated circuits. A survey of speed and prices in mid-1976 resulted in the price/speed distribution given in Appendix II. It can be seen that the price per analog channel increases with decreasing A.D.C. speed due to the fact that less channels can be multiplexed on the same A.D.C. The price per channel has been

obtained by dividing the msec dead-time requirement by the A.D.C. speed. This should normally be corrected due to the need of a modular sharing.

Note 2:

It has been assumed that the dark current during the 10 msec should remain within 5% of the total dynamic range in order not to decrease too much the dynamic range through saturation of the device. That is:

CCD 311 - 5% x 200 mv = 10 mv

CCD 321 - 5% x 1,000 mv ≃50 mv

These figures imply that the 311 would meet the maximum dark current requirement at 25°C. That would not be the case for the 321 which would have to be cooled to 15°C (assuming that the dark current drops by a factor of two every 8°-10°C).

It must be noted at this point that the dark current may have to be subtracted from each of the cells content (with preliminary measurement). This is independent of the maximum 10 mv/50 mv maximum value which is related to the narrowing of the dynamic range.

Distribution of Clock Signals

Parallel Read-out versus Sequential Read-out:

These schemes are shown in Appendix III.

Parallel Read-out - Figure AIII-1: Column scanning clocks are common to all channels - that is all rows (cells) are shifted at the same time. The output information from each transport shift register is then scanned by output multiplexer and data converted in A.D.C.

Sequential Read-out - Row scanning: Each transport is read out entirely. The next transport is selected and so on. This scheme

requires a slower scanner [$f_s = f_p/N_c$ where N_c is the number of cells of the transport register ≥ 200 and f_p the frequency of the parallel scanner]; such a multiplexing system can be implemented very easily. However, it requires an individual clock driver (or clock de-multiplexer) per transport system - which is very costly and takes a lot of power, particularly with the 311 which has five different clocks. Moreover, that mode could result in more noise spikes due to the halting of clocks on all of the transports tied to a common A.D.C., but one set. The dark current contribution to each cell is represented in Appendix, Figure AIII-4, 5 for both modes. For the sake of simplicity, it has been assumed that dark current is the same for each cell of each transport and increases linearly with time.

B Clocks Timing:

Independently of the CCD's internal organization and clock distribution, two read-out timings are conceptually feasible.

Systematic Cell Content Conversion:

In this mode, the content of each cell of each transport register is converted to digital form. Any rejection of information corresponding to an empty cell will be done at the digital level through some kind of fast preprocessing equipment - then forwarded to the computer(s). This has two consequences:

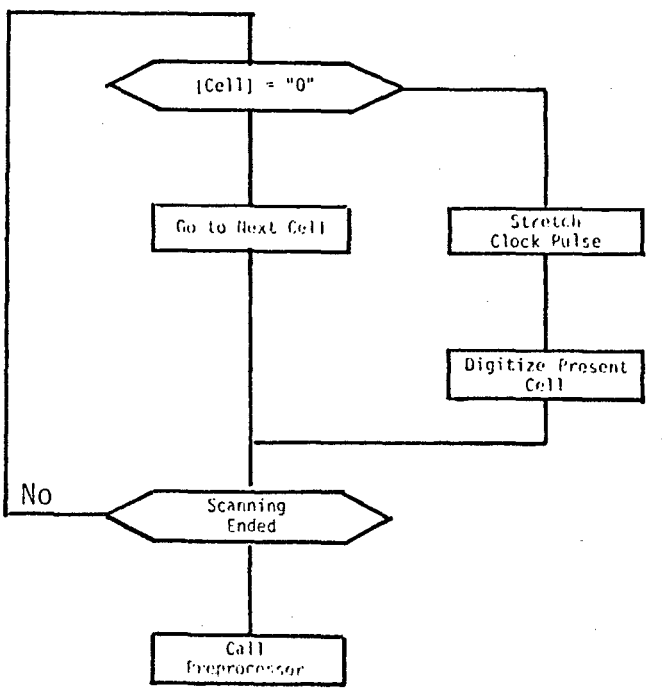
The timing being fixed; the read-out time will be constant.

The memory capacity needed to buffer the A.D.C. and store data before any processing has to fit the maximum cell capacity, at least if there is no simultaneous processing of the data in the memory, i.e., for example, a 32 channel module with 256 bit per channel with a 9 bit (including sign) data size requires an 8K - 9 bit memory module.

Selective Data Conversion:

Only a small percentage of the cells are likely to contain some information, 10%-20% could be an average maximum value, if particle noise background is not too high. It is then conceivable to reject the "empty cells" upstream of the A.D.C. This could also decrease the dead-time and, in principle, the size of the buffer memory.

Inserting a dual comparator for positive and negative signal at the output of the transport would allow detection of whether the cell content is within a narrow window centered on the "rest level" of the cells. Assuming that the comparators are fast enough compared to the A.D.C., it is possible, according to their responses, to carry on the conversion if data is non-zero and on the contrary skip any conversion if data level is within the window. The logic loop is:



For example:

One μsec conversion time A.D.C.'s - would result in associating 200 nsec comparators with an average dead-time (D.T.) over the systematic conversion mode.

Cell Rate of Occupancy:	5%	10%	20%
D.T. Reduced to:	24%	28%	36%

$$\left[\frac{\text{D.T. Sel}}{\text{D.T. Sys}}\right] = [\text{Rate of Occupancy} + 1/5\ (1 - \text{Rate of Occupancy})]$$

In the same way, the average memory buffer capacity would be for a similar module:

$$32 \times 256 \times (\text{Rate of Occupancy}) \underbrace{(\text{data}}_{9\text{ bits}} + \underbrace{\text{transport number}}_{5\text{ bits}} + \underbrace{\text{cell number})}_{8\text{ bits}}$$

and average

	Rate of Occupancy		
	5%	10%	20%
$\left[\frac{\text{M Size Sel}}{\text{M Size Sys}}\right]$	(5 x 22)/9≃ 11%	(10 x 22)/9≃ 25%	(20 x 22)/9≃ 50%

However, the average values are meaningless due to the random track patterns which can be obtained. Thus, identical 300 x 32 channels module could result in a total occupancy rate well under the average 10% - 20% with rate of occupancy much higher at the module level, as the R.O. dead-time is equal to the read-out of the "slower" module. That is, for the module having the higher rate of occupancy, benefits are much lower than expected. As to the memory size the absolute requirement to avoid any information loss would practically impose a memory buffer of the maximum capacity - unless some data management technique allows allocation of memory capacity from under-average-filled module to over-average-filled module. The feasibility and real interest of such a technique is still to be demonstrated.

Note 1:

Real-time preprogramming could well be the limiting factor in terms of read-out time.

Note 2:

It has been assumed that each transport would have such a comparator. This is quite costly and increases the power consumption per channel. Moreover, the potential need for window adjustment is related to device differences in:

- gain
- dark current
- transport inefficiency, the sum of which

could result in the need to vary the window width with time (during R.O. cycle) and possibly from one device to another one. This would be costly and could slow considerably the whole process.

Table AIII-1 in Appendix III summarizes the pros and cons of the possible R.O. schemes. It seems at this point of the evaluation that a brute force approach of the parallel systematic R.O. would conserve the simplicity of the design and debugging as well as modularity at the possibly expense of certain parameters, such as the R.O. dead-time.

Detailed Comparison of the CCD 311 and CCD 321

The devices will be compared according to:

1. Parameters
2. Ease of Utilization

Parameter Comparison

The respective values of the different parameters, excepting transfer inefficiency are summarized in Appendix IV. Numbers are taken from data sheets except for transfer inefficiency. Transfer inefficiency is not specified by the

data sheet; preliminary measurements are indicated. However, not too much confidence should be given to present measurements, particularly for the CCD 321, due to the fact that in this case at 20 MHz the shape of the clocks may have not been optimized. Furthermore, CCD 311 production seems to be quite reliable. The CCD 321 which was available apparently came from an early batch - when all parameters of production were not tuned accurately; recent devices seem to be much better.

To measure the transfer inefficiency, the loss on the leading edge has been taken as indication parameter. This loss represents quite well the NEM of the transport (see Charge Transfer Device, Sequin and Tompsett, Advances in Electronics and Electronic Physics, Academic Press, 1975).

From Table A.4.1, it is possible to see that the CCD 321 has a leading advantage nearly on all characteristics but the following:

- Rate of Output Signal Offset
- Frequency of Operation
- Transfer Losses

The price will be also discussed although the two devices are priced comparably, even if two channels only are stored in the 321.

Rate of Output Signal Offset (R.S.O.)

The 321 has ten times more dark current at the output than the 311, but the absolute value does not mean much. The ratio RSO/Saturation voltage is a better indication than the R.S.O. itself, due to the fact that it measures how much the dark current can degrade the dynamic range. Using that ratio indicates that the 321 is only two times higher in dark current than the 311. As previously mentioned, cooling the 321 device to $+15^{o}C$ should equalize the two values while decreasing also some contribution to the noise level. Dark current varies by a factor two every $8^{o}C$-$10^{o}C$.

It is to be noted that the 311 requires more area on a PC board and would be probably more difficult to cool because of the large volume.

Frequency of Operation

The 321 requires a transport frequency two times higher if used as a dual channel. If used as a quad data channel the frequency is four times higher. The requirements on the driver are certainly more stringent taking in account the faster rise and fall times, leading to higher drive currents through the relationship:

$$I = \frac{dQ}{dt} = \frac{CdV}{dt}$$

Assuming 5 nsec rise and fall time for the 321 at 20 MHz and 15 nsec rise and fall time for the 311 at 5 MHz

$$I = \frac{15 \cdot 10^{-12} \times 16}{5 \cdot 10^{-9}} = 48 \text{ ma (321, per channel)}$$

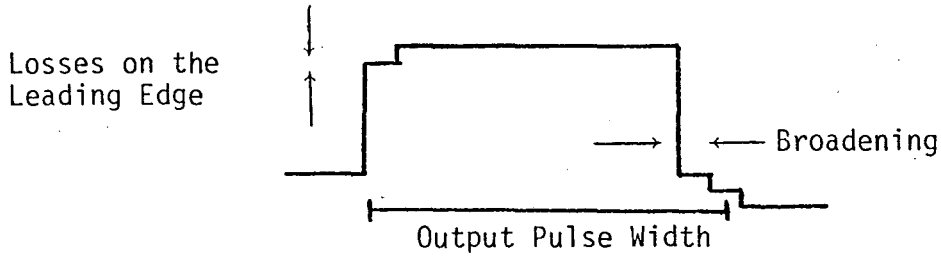
$$I = \frac{200 \cdot 10^{-12} \times 15}{15 \cdot 10^{9}} = 200 \text{ ma (311, per channel)}$$

Certainly, taking into account a 200 nsec period for the transport clock of the 311, 15 nsec may be a little conservative. But even doubling these figures to 30 nsec would still require 100 ma in terms of total amount of current to be handled by the drivers. The current required by the 321, due to its low capacitance, is not higher than for the 311. This does not reflect completely the difficulties in the design of the driver. This point will be reviewed further in the chapter related to drivers.

Transfer Losses

It has been pointed out what part transfer losses have in the distortion of the information stored. The two devices (on the basis of mid-August 1976 data) have comparable losses. How are those losses measured? If one considers the leading edge of a square wave signal pulse, the difference

between the leading edge and the "flat of the pulse" reflects the loss, at least for a wide enough signal pulse.



These losses are equal to $(1-\varepsilon)^n$ where n is the number of wells. The value of n is twice the number of memory cells; these devices being two-phase CCD's.

CCD

$$(1-\varepsilon)^n = \sum_{i=0}^{n} C_n^i \varepsilon^i$$

if $\varepsilon \ll 1$ $\quad (1-\varepsilon)^n \simeq 1-n\varepsilon$

for 5% loss $\quad \varepsilon 311 \simeq 5 \times 10^{-2}/260 \simeq 2 \times 10^{-4}$

$\varepsilon 321 \simeq 5 \times 10^{-2}/910 \simeq 5.5 \times 10^{-5}$

Fairchild agree that the measurement of the loss on the leading edge is a fairly good way to assess the value of ε. Their measurements on the 321 are repeatable to 1% but they actually do not know with what accuracy. This point will be clearer as the production line reaches a plateau and more data on the statistical distribution of ε is known. They point out that most of the devices presently fabricated are within 10% loss on the leading edge. However, the knowledge of the exact distribution of ε from devices of the production line is essential to know if the purchase of devices selected for ε is to be economically interesting for the TPC project, and if the quad channel per device scheme can be implemented without costs runaways. Actually, Fairchild is probably not now able to select devices with an $n\varepsilon<5\%$ due to a lack of calibration of

of their on-line equipment, but that situation is likely to change in the next few months.

It must also be noted that the production of the 321 is still in a learning stage and that improvements are likely to be made on the obtainable ε as well as on the test equipment. This is less obvious for the 311 which is an older device (18-24 months) and a by-product of the CCD 110 linear image sensor in which the photosites have been detected as defectives on the test line.

Cost Comparison

Prices of the CCD 311 and 321 are listed in Appendix IV. Taking into account the overall costs of this part of the data acquisition system, it is obvious that the driving requirements - number of clocks, power consumption complexity of layout leading to fewer channels per board as well as the need for a differential output amplifer-makes the 311 more costly than the 321, even for a two channels per 321 scheme. The difference is obviously increased if 4 channels per 321 can be used. It is certainly too early to have an accurate measurement of the costs relative to each device, but it is possible to take an advantage of the price of the 321 to select devices having transfer losses less than 5%, for example. The affordable limits for each of the connecting schemes for the 321 - 2 or 4 channels per device - has to be determined by the physicists. But as soon as these limits are known, the number of devices filling these requirements will be known and consequently the effect on price.

It must be noted that the price of the CCD 321, being aimed at television applications, should decrease considerably in the future, if this application is successful.

Driving the CCD

Requirements on the Driver:

1. The distribution of the propagation delays tpd01 and tpd10 must be maintained as narrow as possible mainly on the sampling clock, but also on the transport clock to maintain a time and amplitude measurement with as little spread as possible over the thousands of channels, and to conserve the timing requirement, between clocks. The amplitude distortion will be integrated in the linearity corrections, but the timing would require a different type of correction. One can possibly neglect this correction if the spreading is very low.
2. The tpd01 and tpd10 should be as close as possible to avoid any widening or narrowing of the clocks pulses.
3. The clock driver must be able to handle the high current requested by the CCD.

It is obvious that this current is dependent on the number of transports per driver. For the 311, it is 100 pf per clock pulse. For the 321, it depends on how many transports are hooked to the same driver. Two transports, that is 60 pf, seems to be the minimum but one could think of driving 120 pf (four transports) without too much difficulty.

The following figures apply to CCD 311 at 5 MHz and CCD 321 at 10 MHz and 20 MHz.

CCD 311, 100 ma/transport clock phase (two phases per device)
$t_r = t_f = 15$ nsec

CCD 321, 96 ma/two transports $t_r = t_f = 10$ nsec

CCD 321, 192 ma/two transports $t_r = t_f = 5$ nsec

It might be very difficult to hook more than two devices to the same

driver, because of the large amount of current to be transported along the clock lines.

Short clock lines are mandatory in order to avoid electromagnetic interferences on the CCD's and pre- or post-amplifiers. A scheme using a common driver for two devices would probably be satisfactory even for the 311 (the pinning of which is not very convenient for multiple device driving). The number of drivers per channel would be then:

311	0.5
321, 10 MHz	0.25
321, 20 MHz	0.125

which means that the overall static power consumption of the driver is decreased.

Also, sharing a driver between several analog channels ensures also less spreading of characteristics for the same "amount" of adjustment. In particular with the 321 of 20 MHz (multiplexed inputs), four analog channels will have identical timing characteristics, and if two devices are driven in parallel it would be eight.

Technology for Drivers:

There exist a certain number of integrated circuits sold as clock drivers. The only one really able to run at 5 MHz, and possibly at 10 MHz, is the MMH0026 hybrid circuit from several sources, mainly National Semiconductor and Motorola. Its main disadvantage is certainly the spreading in propagation delays and need for an input shaping network which has to be adjusted for a constant output pulse width. They could be used only for the 311 and for about $3 to $6 per channel (transport clock only).

Another approach would be to use complementary logic, either with discrete bipolar transistors (but it appears to be more costly than the MH0026 for

comparable performances) or with CMOS in paralleling several outputs. However, CMOS speed is actually too low in tpd's even at 15 volts. CMOS on sapphire or the generation of CMOS logic described by RCA could eventually fit the needs.

The approach which has been taken for the preliminary tests is to use very fast MOS discrete transistors. MOS devices can be very fast. They do not show any storage time of carriers, or thermal runaway and their current capability improves when cooled, which can be very interesting if CCD's are cooled for decreasing the dark current and noise. Moreover, being voltage controlled devices, they do not require much power at the input. So the main factors limiting the speed are the R.C. time constant of the resistive load and capacitive load and the ability of a device to allow the current to get through for a certain V_{GS} voltage.

Devices Used:

Two types of devices are being or likely to be used in a driver.

- DMOS Type SD210 from Signetics
- Type VMP11 from Siliconex

} enhancement mode devices

They will be described here in very general terms.

The amount of current they can handle is roughly proportional to V_{GS}.

SD210 P = 15 ma/V

VMP11 P ≈ 270 ma/V

Cut-off voltages are both in the 1V range. Maximum current capability are:

SD210 $\leq$100 ma
VMP11 <2A.

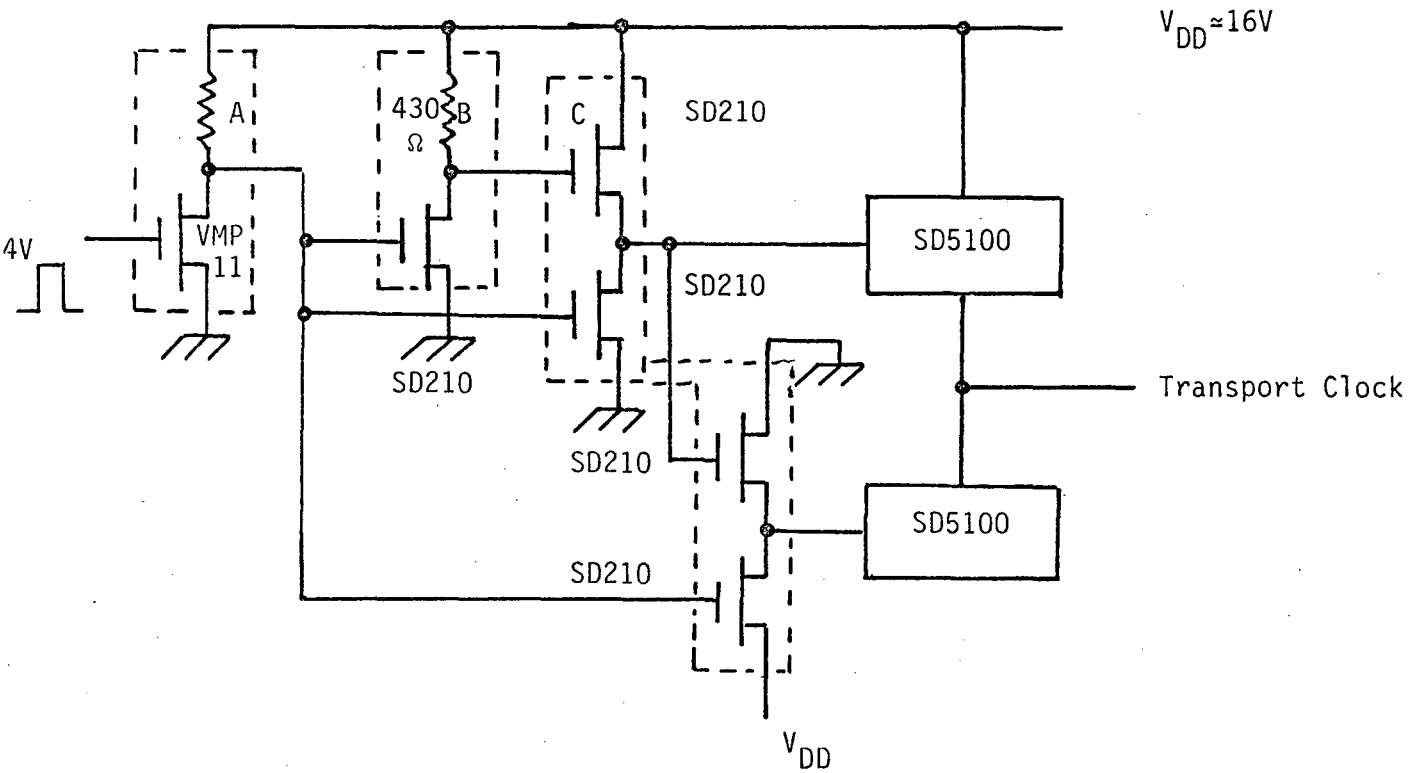
} at 10V

Propagation delays are in the few nanoseconds range for both, and switching times are also in the nanoseconds (1 nsec for the SD210, 4 nsec for the VMP11).

The VMP11 has a very high current capability and very high speed. Moreover, it can be driven from TTL levels. However, its high input and output capacitance hamper somewhat a direct drive possibility.

Driver Scheme

This scheme has been tested at 20 MHz and works fine. The only drawback being that the level shifter stage takes some power.



The SD5100 is a quad SD210 device with all sources connected. That type of symmetrical output is very good for capacitive drive.

A - is the level shifter. Actually, it is a VMP11 but should be changed for a more standard bipolar device. The resistor in the drain of the VMP11 is around 80 ohms (depending on load capacity). The power consumption can be decreased when using a device having much less output capacitance. The three SD210 inputs have a

maximum of 9 pf, compared to 40 pf for the VMP11.

B - is an inverter stage.

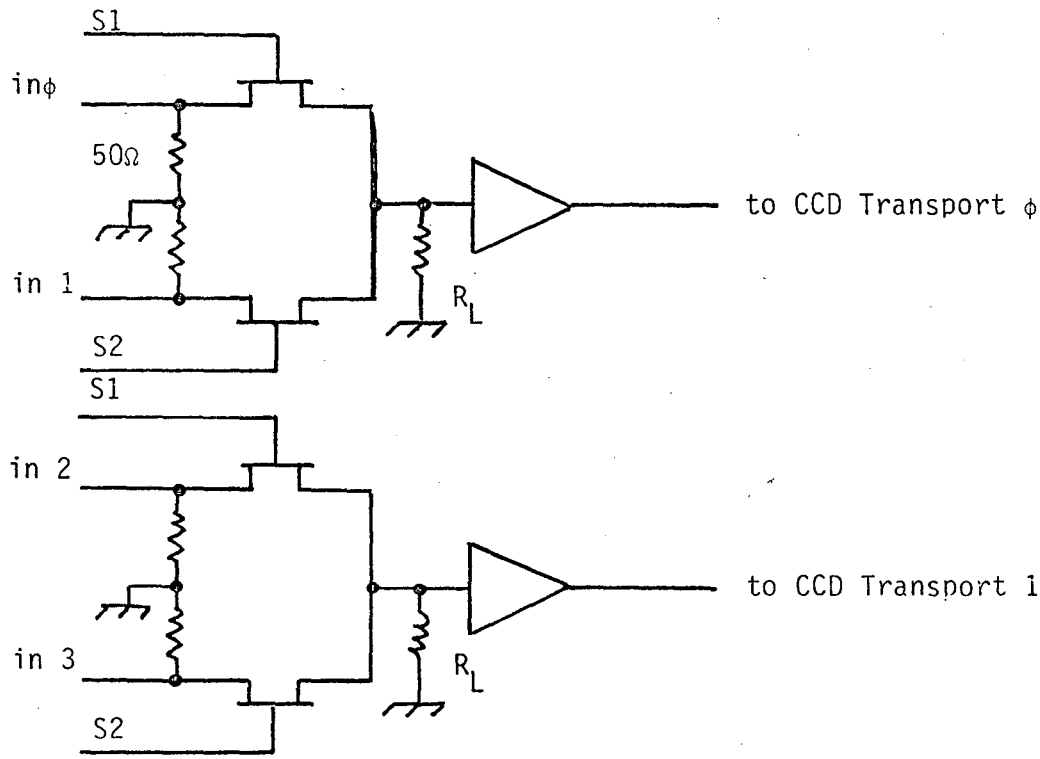
C - are pre-drivers. They could probably drive the CCD at 10 MHz with 10 to 15 nsec rise and fall time.

The output stage is a high current buffer which delivers the 200 ma required without any difficulty. Driving two CCD's might be tried with that scheme, but it appears short of current. Using one more symmetrical stage with two VMP11's would deliver the needed current for two 321's and more if the layout is feasible. Doubling the SD5100 would also allow driving two 321's in parallel and might be a cheaper solution.

The total number of stages in the design is two for the symmetrical output stage and two for level shifter or inverter. At 1 to 2 nsec/stage in propagation delay, the maximum spreading is within 4 nsec which is fairly good. The broadening of the pulse is dependent on the R in A and B resistors and input capacitance of following stages so it remains also relatively low. The main problem to be solved at this level appears to be the power consumption at the A or B level. The possibility of having active load to replace the resistors would serve that purpose efficiently if the gains are not offset by more complexity. The final choice of the structure will derive from the feasible layout as well as from the modifications which would be required by a more complete analysis of the CCD.

Input Multiplexing for the 321

Input multiplexing may be used with the 321 in order to take a better profit from the 321 cell capacity. The scheme used would be:



All transistors are DMOS devices*; R_L = 1kΩ insures a nearly 100% efficiency. S1 and S2 are 10 MHz complementary waveforms - an amplitude of 10-12V would give a better linearity mainly at the upper range of the input dynamic range (from 1V to 2V).

This scheme has been tested with a clock amplitude of 7V and works fine in terms of linearity and limited capacitive coupling either from clock S1 or S2 to output signal or channel to channel interference. As mentioned before, increasing the clock voltage would insure a better linearity by lowering the R_{ON} of the selected channel and working in an area of the R_{ON} = F(CVGS) characteristics which is quite flat.

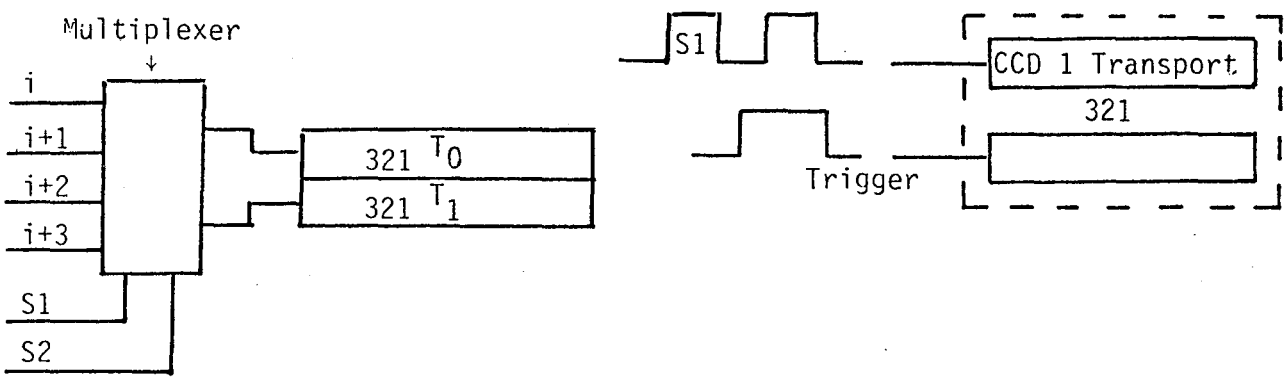
*SD210 type, or better, SD5200/5000 types.

It is to be noted that inserting a multiplexer at the input reduces by the same amount the number of multiplexing transistors at the output. Only the working speed is 10 MHz instead of a ≈1 MHz read-out frequency (if faster A.D.C.'s cannot be used). Thus, those input multiplexers do not add any supplementary cost.

As the gate input capacitance of a DMOS transistor is in the 2.5 pf range, driving several channels from the same driver appears very easy. Four to eight channels could be driven in parallel with a driver of the type described for the clocks, but limited to the first symmetrical output stages.

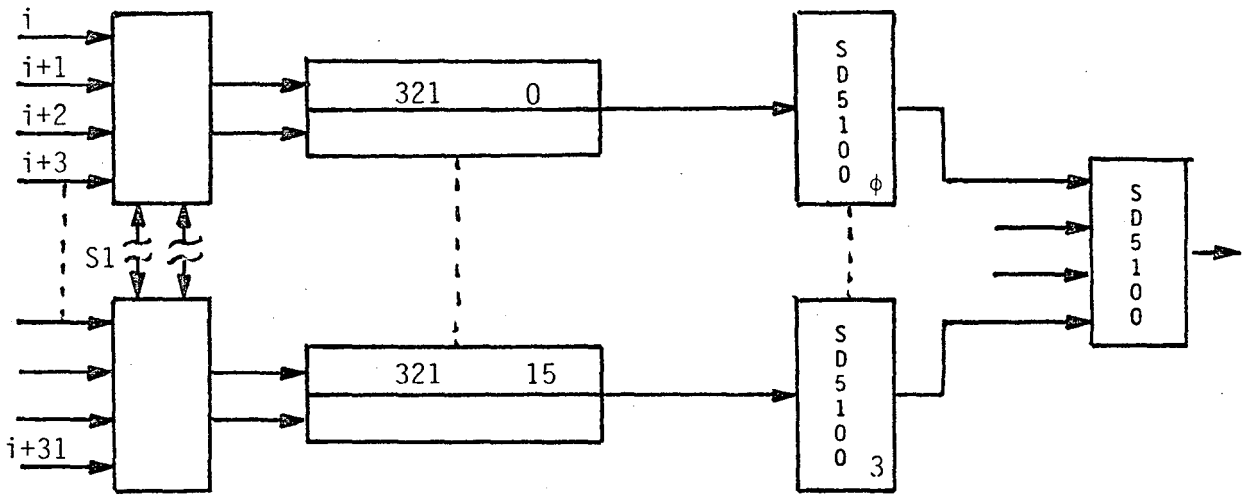
Multiplexing at the input presents the advantage of parallel driving of the DMOS transistor gates which is not true for output multiplexing when each gate has to be driven individually.

There is obviously a need for a special mark in order to know which of the cells in the CCD corresponds to which input channel. That can be done by using another CCD to store the information relative to channel selection. It is also possible to store the time of arrival of the trigger.



Output Multiplexing

Here again it would be possible to use the SD210 transistor as a component of the output multiplexer.

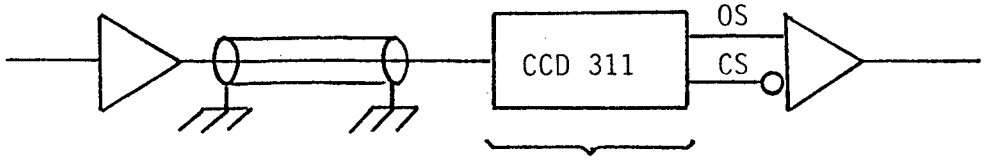


With a 1 MHz read-out frequency and 32 channels (with 227 cells each) would give complete R.O. in 7.3 msec.

The output multiplexer would require no more than 20 clocks.

APPENDIX I

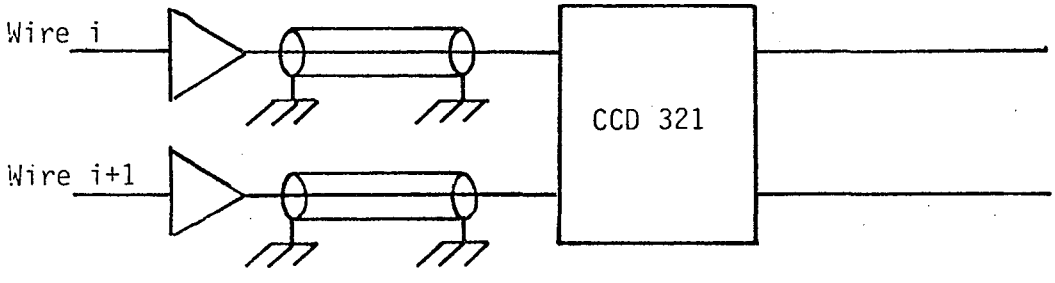
AI-1



Five different clocks ϕ_{SA}, ϕ_{SB}, ϕ, $\bar{\phi}$, ϕ_R

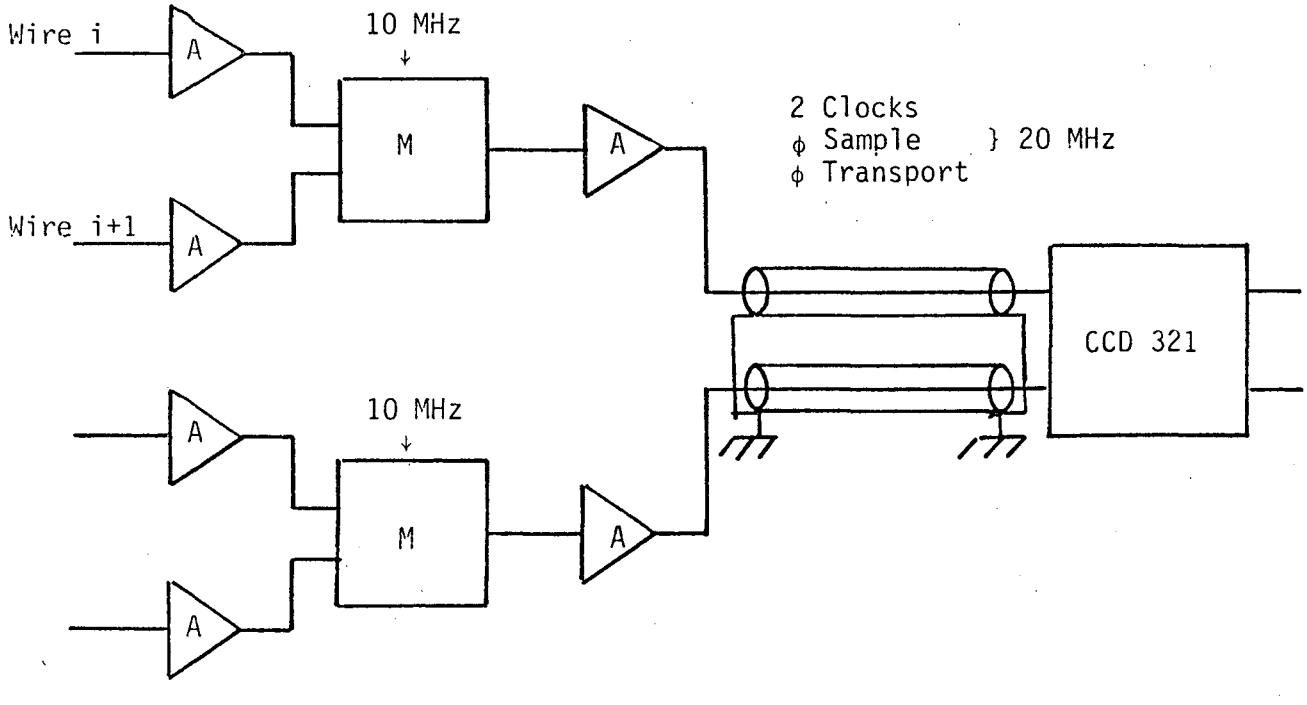
ϕ_R = 10 MHz; others 5 MHz

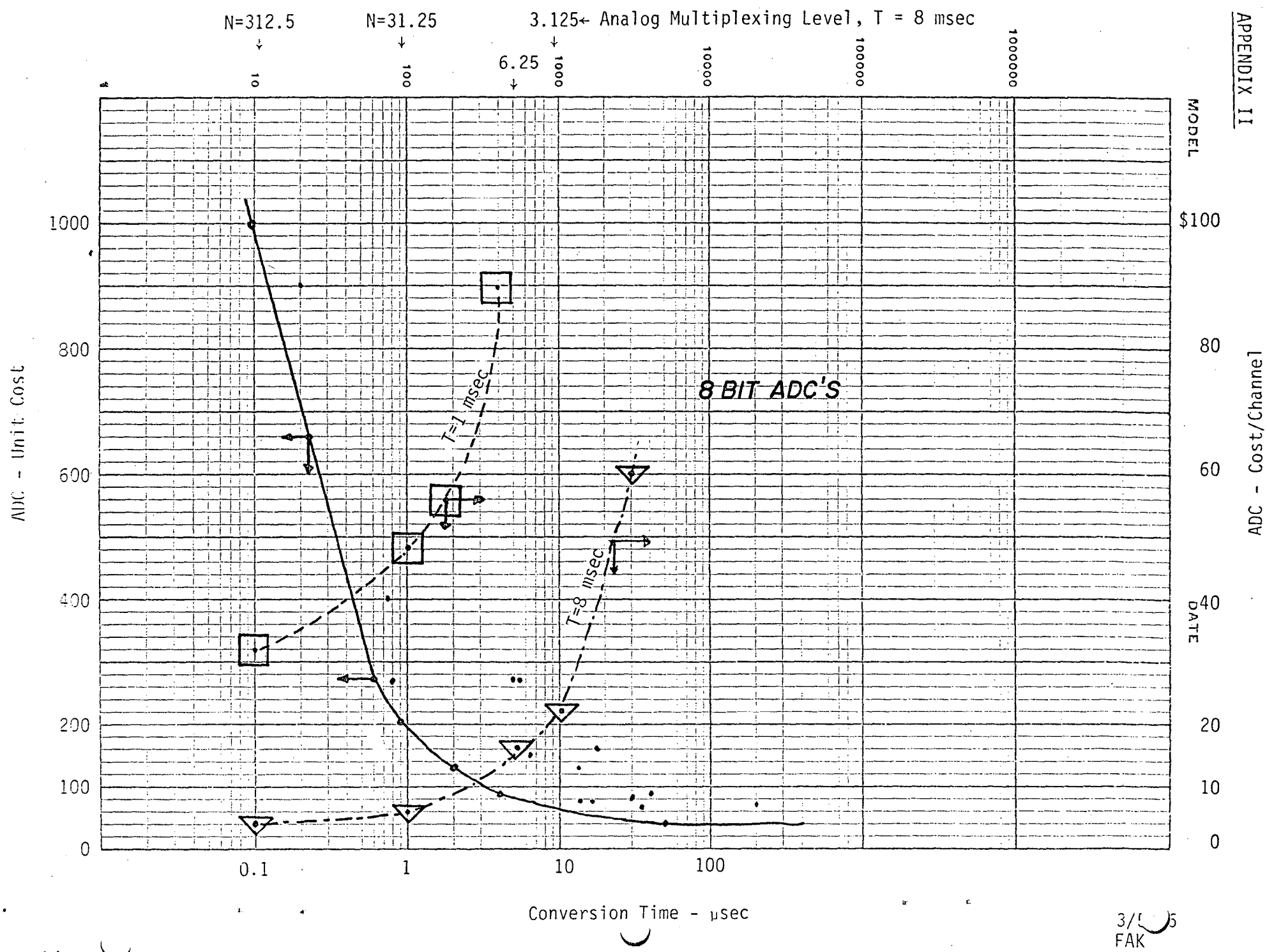
AI-2



2 Clocks ϕ Sample, ϕ Transport } 10 MHz

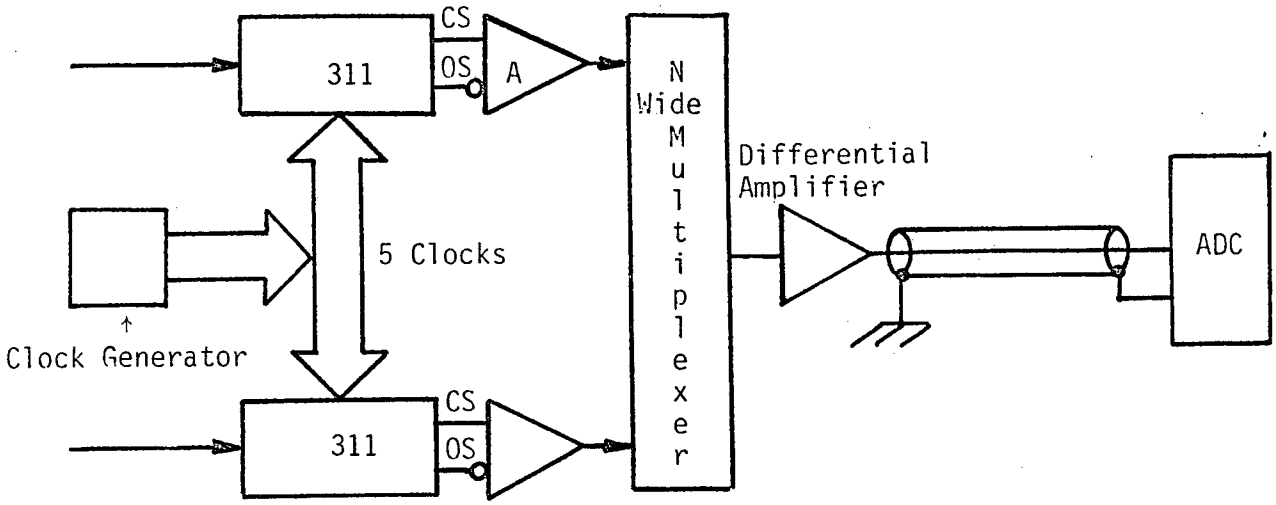
AI-3



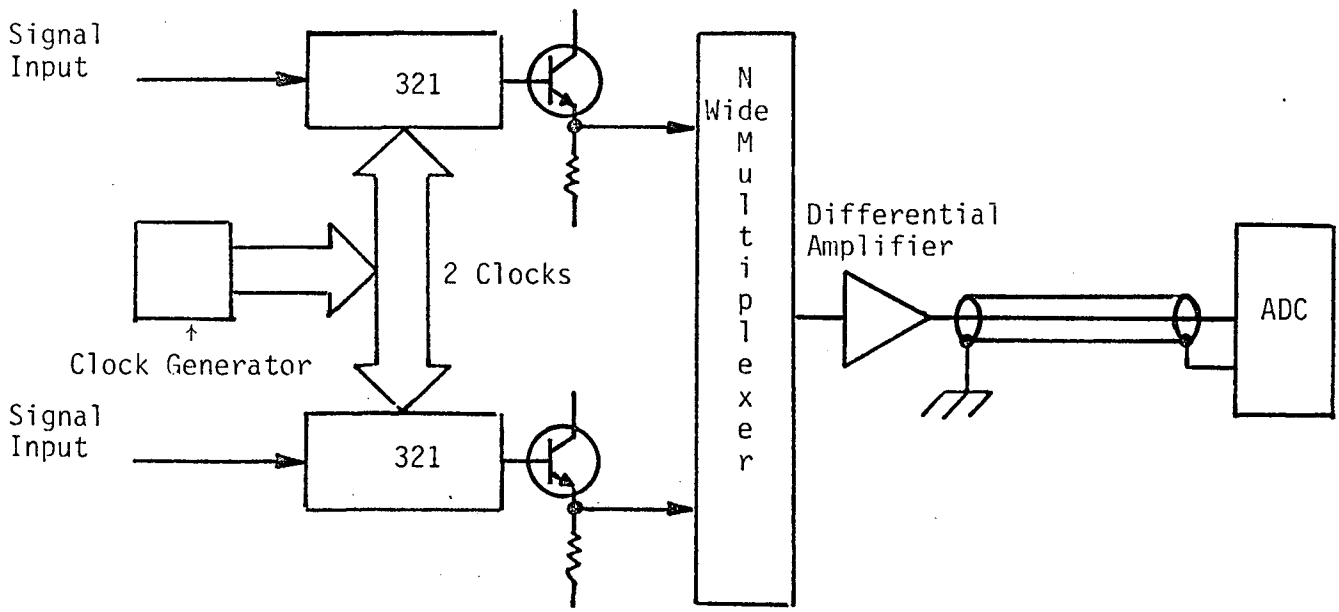


Read-out Schemes
A - Constant Frequency: parallel readout

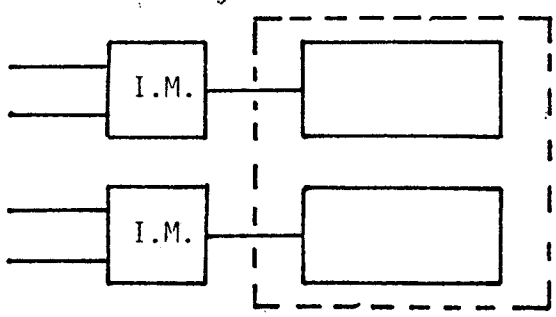
AIII-1 CCD 311



AIII-2 CCD 321



AIII-3 CCD 321 at maximum usable capacity



For sake of simplicity, only a symbolic representation of CCD's has been drafted.

APPENDIX III (con't)

Table AIII-1

Systematic Cell Content Conversions

- Maximum Read-out Time
- Maximum Storage Capacity
- "Brute Force" approach but simplest design and excellent modularity

Selective Cell Content Conversions

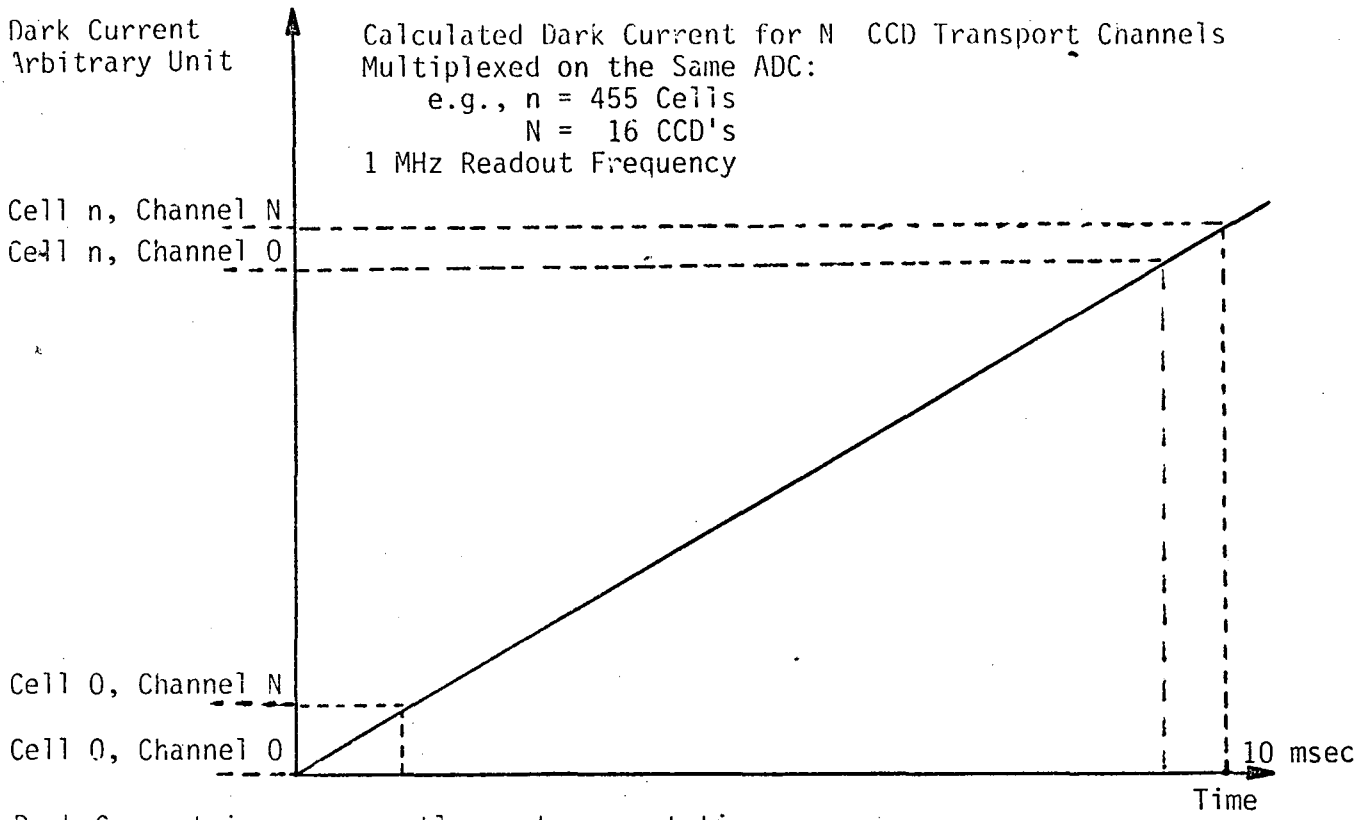
- Faster Read-out Time
- Less Memory Storage
- Higher Hardware Complexity

Parallel Read-out

- Requires fast output multiplexer

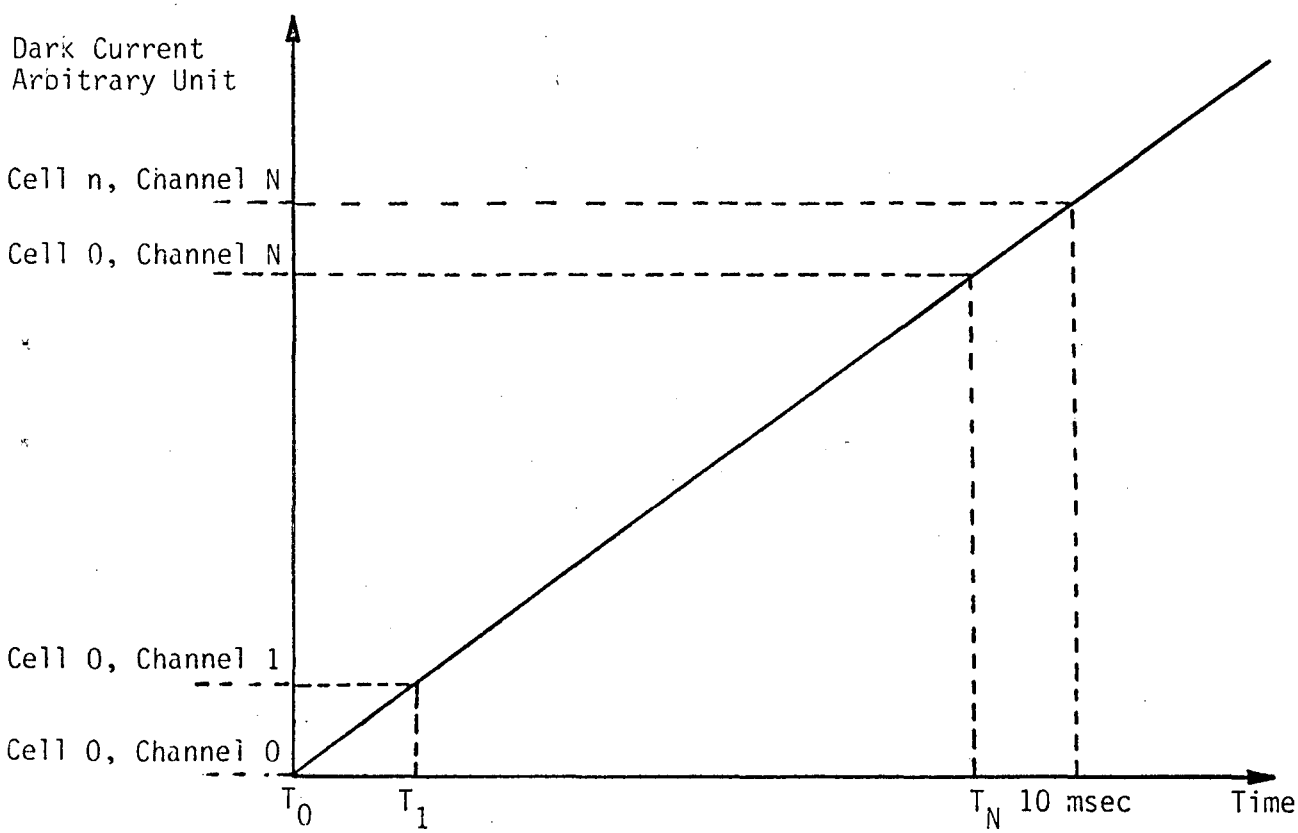
Sequential Read-out

- Can be used with slow output multiplexer that is integrated circuit multiplexer.



Dark Current increase mostly as transport time

Figure AIII-4 Parallel Mode



Dark Current increase as transport time + offset x Ni Ni([0,N-1])

Figure AIII-5 Serial Mode

APPENDIX IV

Comparison between CCD 311 and CCD 321

Parameters	CCD 311	CCD 321
Insertion Loss	15dB	6dB
Rate of Output Signal Offset	1 mv/ms	10 mv/ms
Signal to Noise Ratios	50dB	55dB
Saturation Voltage	200 mv	1000 mv
Transport Clock Capacitance/ Data Acquisition Channel	200 pf	30 pf* 15 pf**
Sample and Reset Clocks per Data Acquisition Channel	Non-Specified	20 pf* 10 pf**
Transport Clock Frequency READ IN	5 MHz	10 MHz* 20 MHz**
Sample Clock Frequency	5 MHz	10 MHz* 20 MHz**
Reset Clock Frequency	10 MHz	10 MHz* 20 MHz**
Number of Clocks/Channel	5	2* 1**
Dynamic Power Consumption/ Channel	VDD = 15v ≃110 mw	VDD = 16v/64 mw * VDD = 16v/64 mw **
Need for Differential Output Amplifier	Yes	No
CCD Price/Channel	20S/5000	22.50/5000* 11.25/5000**
Transfer Loss Measured at Missing Charge on Leading Stage	≃5%	40% a <10%

* One channel per transport

** Input multiplexing: two channels per transport

a Preliminary devices from FSC

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