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Los Angeles

Nitride Based Metal Insulator Semiconductor Heterostructure

Material and Device Design and Characterization

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Materials Science and Engineering

by

Jiechen Wu

2014

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ABSTRACT OF THE DISSERTATION

Nitride Based Metal Insulator Semiconductor Heterostructure

Material and Device Design and Characterization

by

Jiechen Wu

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2014

Professor Dwight C. Streit, Chair

$\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ metal-insulator-semiconductor-heterostructures (MISH) were designed, fabricated and characterized. The effects of different dielectric deposition techniques, surface treatments and post deposition treatments were investigated by comprehensive material and electrical characterization to understand the Al_2O_3 dielectric and $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfacial properties.

Thermal ALD and PEALD Al_2O_3 thin films were successfully deposited on MBE grown $\text{AlGaIn}/\text{GaIn}$ layers. An XPS study reveals the band offset of $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. In addition, pre-deposition treatments show a reduction of Ga-O bonds at the interface after ALD growth.

The fabrication of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISH diodes were achieved with deposition of Ti/Al/Ni/Au ohmic contacts and Ni/Au gate contacts. C-V characterization of MISH diodes was applied to

evaluate $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states. Traps with different energy levels were differentiated by C-V hysteresis curves and multi-frequency C-V. C-V analysis suggests that PEALD provides better film quality with lower defect densities than thermal ALD. The implementation of NH_3 and N_2 pre-deposition surface plasma treatment and N_2 post-deposition annealing can also improve interfacial properties.

Al_2O_3 dielectric thin film leakage current and conduction mechanisms were also studied by I-V characterization. PEALD Al_2O_3 thin films exhibit better leakage current suppression compared to thermal ALD films. Temperature dependent I-V characterization shows that Poole-Frenkel emission dominates in dielectric current transport at medium electric fields, while at high electric fields, Fowler-Nordheim tunneling and trap-assisted tunneling dominate at low and high temperatures, respectively. Various dielectric reliability tests were employed on Al_2O_3 thin films. The results of time dependent dielectric breakdown (TDDB) test can be fit into $1/E$ field dependent model and a Weibull slope of 2.87 is extracted for PEALD Al_2O_3 thin films. The dielectric breakdown field distribution statistics show that PEALD Al_2O_3 films have a larger average dielectric breakdown field than thermal ALD films, and the plasma N_2O post deposition annealing improves the average breakdown field. The improvements from integration of pre-deposition and post deposition treatments may offer a better device performance and reliability in MIS-HEMTs, and enable further progress and development of nitride based power electronics.

The dissertation of Jiechen Wu is approved.

Mark S. Goorsky

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University of California, Los Angeles

2014

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Chapter 1 Introduction

1.1 Motivation

With the continuous development of power conversion technology and rapid growth of wireless communication market, high power and high frequency transistors are arousing significant interests for emerging applications.

The expectation for modern power transistors becomes higher and higher as new technologies are boosted up rapidly. The next generation mobile phone needs a wider bandwidth. The receiver requires a lower noise while maintaining a high gain. The broadband wireless internet connection and TV broadcasting require a higher frequency for faster data transmission. The traditional power switch and diode also need to improve power handling and minimize energy loss, and therefore achieve a higher efficiency [1], [2].

To summarize, modern power semiconductor devices require higher efficiency, better power handling, lower noise and wider bandwidth. Due to these demands, significant research efforts and investments have been made to develop high power and high frequency transistors. And it has been found that GaN based power devices are the solution to this problem.

1.2 GaN

Gallium Nitride (GaN) is considered one of the most important semiconductor materials after silicon. It has three possible structures: wurtzite, zinc blende and rock salt. Among them, wurtzite structure is thermodynamically favorable under ambient atmosphere. The wurtzite GaN is constructed from two interpenetrating hexagonal close packed structures of gallium and nitrogen

atoms displaced from each other by $\frac{3}{8}$ c. The typical 2H type structure material has very strong polar bonds because of strong electronegativity of nitrogen atoms.

GaN is a perfect candidate in high power transistor domain. It possesses supreme electronic properties such as wide bandgap (3.42eV), excellent electron saturation velocity (2.7×10^7 cm/s), good electron mobility ($2000 \text{ cm}^2/\text{Vs}$), high 2 dimensional electron gas (2DEG) density (10^{13} cm^{-2}), high breakdown field ($3.3 \times 10^6 \text{ V/cm}$) and good thermal conductivity (170 W/mK). Table 1-1 shows a comparison of electronic properties of four widely used power transistor materials from high power device perspective. There is no doubt that GaN owns excellent properties compared to other semiconductor materials. Table 1-2 lists Baliga's figure of merit and Johnson's figure of merit, two calculated parameters based on material properties such as electron saturation velocity and breakdown field, which are normally used for high power and high frequency transistors comparison [2]. An intuitive comparison of device properties can be reflected on the following graph (figure 1-1). At the regime that requires both high power and high frequency operating, the GaN transistor owns unique advantages and few techniques can compete with it.

Table 1-1 Semiconductor material properties at high frequency and high power operation.

Properties	Si (----)	GaAs (AlGaAs / InGaAs)	4H-SiC (----)	GaN (AlGaN / GaN)
Bandgap (eV)	1.11	1.42	3.26	3.42
μ_e (cm ² /Vs)	1500	8500 (10000)	700	900 (2000)
V_{sat} ($\times 10^7$ cm/s)	1	1 (2.1)	2	1.5 (2.7)
2DEG density (cm ⁻²)	NA	$< 4 \times 10^{12}$	NA	$1-2 \times 10^{13}$
E_B (10 ⁶ V/cm)	0.3	0.4	2	3.3
Dielectric constant	11.8	12.8	10	9
Thermal conductivity (W/mK)	150	50	490	170

Table 1-2 Power semiconductor devices Figure of Merit

	Si	GaAs	SiC	GaN
Tmax	300	300	600	700
BFOM	1	9.6	3.1	24.6
JFM	1	3.5	60	80

$BFOM = k\mu n ECR^3$
Baliga's figure-of-merit
 Evaluate resistive loss [3]

$JFM = ECR V_{sat} / 2\pi$
Johnson's figure-of-merit
 Evaluate switching delay [4]

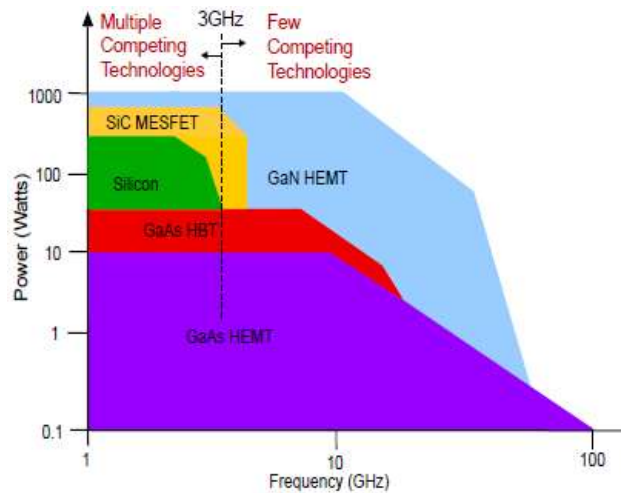


Figure 1-1 Operation range of high power and high frequency transistors.

1.3 GaN HEMT

The AlGaN/GaN heterojunction enables the development of GaN high electron mobility transistors (HEMT). Owing to spontaneous polarization and piezoelectric effect, a high density 2DEG is formed at AlGaN/GaN heterointerface, and it makes the GaN HEMT possible. The high electron density, combining with a high electron mobility due to reduced ionized impurity scattering, provides large current and high speed in device operations. GaN based HEMT offers many advantages comparing to existing technologies. Besides the advantages of high power handling, high frequency and high efficiency, the wide bandgap nature and its growth on SiC substrate allow good thermal management and high temperature operation of devices. In addition, the high power density feature makes transistor size and number much smaller. Low channel resistance and high electron saturation velocity offer the potential of low noise application. From the fabrication aspect, the chemical inertness of GaN and good ohmic contacts facilitate a reliable device fabrication. In the end, the potential of forming a good dielectric/GaN interface holds a promising future for insulated gate transistors.

Figure 1-2 shows a conventional GaN based HEMT structure. It uses a schottky gate to control 2DEG at AlGaIn/GaN channel. However, some problems that degrade transistor performance have to be overcome [5]. First of all, dangling bonds at AlGaIn surface form surface states. Charges are trapped in these states during device operation, which causes the reduction of the output current [6]. This phenomenon is called current collapse, one of the major obstacles in developing GaN HEMT. Another critical issue of GaN HEMT is the gate leakage current at high voltage operation. Electrons may jump over the potential barrier or directly tunnel through AlGaIn barrier into gate electrode when they have high energy or local electric field is large enough [7]. Escaped electrons not only increase power consumption, but also accumulate at AlGaIn surface to form a virtual gate, thereby resulting in loss of gate control at the channel [6]. Both surface states and gate leakage significantly limit the operation of GaN HEMT. To solve this problem, a new structure that combines advantages in insulated gate and heterostructure transistors, has been proposed for GaN power devices [8], [9], [10].

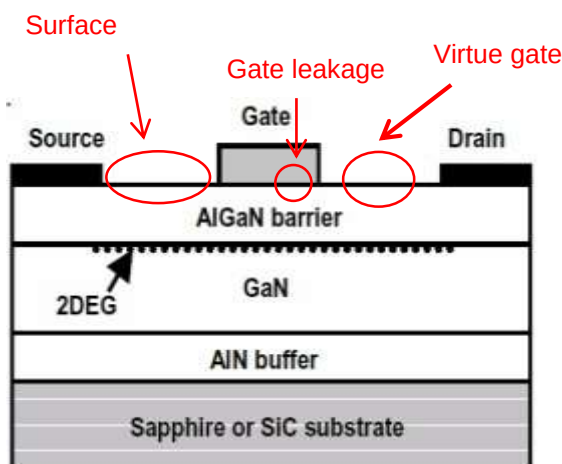


Figure 1-2 Conventional HEMT structure and problems.

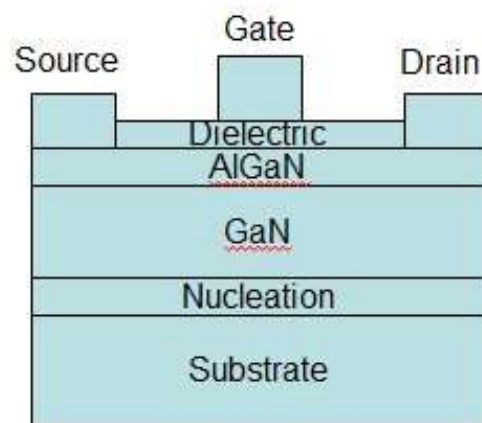


Figure 1-3 MIS-HEMT structure.

1.4 MIS-HEMT

1.4.1 MISH devices and interfaces

Figure 1-3 shows a general MIS-HEMT structure. A dielectric layer is added on top of AlGaIn/GaN heterostructure. This layer acts as a gate dielectric separating gate metal and semiconductor and preventing the gate leakage, and it also passivates the semiconductor surface, eliminating surface dangling bonds and minimizing traps. One of the earliest papers of GaN MIS-HEMT published in 2003 shows a tremendous improvement of gate leakage without decreasing device performance by adding a dielectric layer (figure 1-4) [11]. The drain voltage ($V_{ds} = 20V$) here is a typical operating voltage for a power transistor. It was also reported that the SiN passivation layer in HEMT can eliminate current collapse and dispersion between the large signal direct current and alternating current characteristics [12].

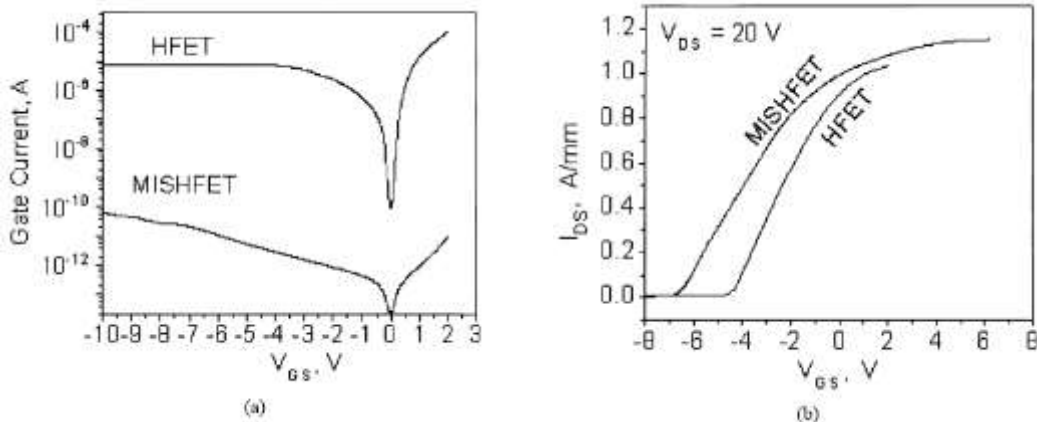


Figure 1-4 Gate leakage current (a) and transfer characteristic (b) of HFET and MISHFET [11].

The dielectric layer may influence device performance by changing 2DEG density at AlGaIn/GaN interface. The mechanism behind this effect is not fully understood. Some groups suggested stress induced piezoelectric effect due to the additional dielectric layer causes a 2DEG density change

[13], [14], [15] while other groups considered that the surface states reduction [16], [17], [18] in passivation leads to surface trapped electrons transferring to AlGaIn/GaN interface.

Another important point that we are interested in is the characterization of the dielectric/semiconductor interface [19], [20], [21], [22]. Although the dielectric layer decreases semiconductor surface states by reducing dangling bonds, it still leaves a small amount of unsatisfied bonds at the interface due to the material heterogeneity (figure 1-5). This type of bonds also behaves as interface states and traps electrons during device operation. Therefore, it is very important to characterize the dielectric/semiconductor interface to achieve a good device control. However, since there are two interfaces in this structure (dielectric/AlGaIn interface and AlGaIn/GaN interface), it is especially hard to study the former one in MIS-HEMT structure because the potential modulation is essentially fairly complicated between the two interfaces. In this work, we focus on the dielectric/AlGaIn interface characterization and study the physics inside and effects on device performance.

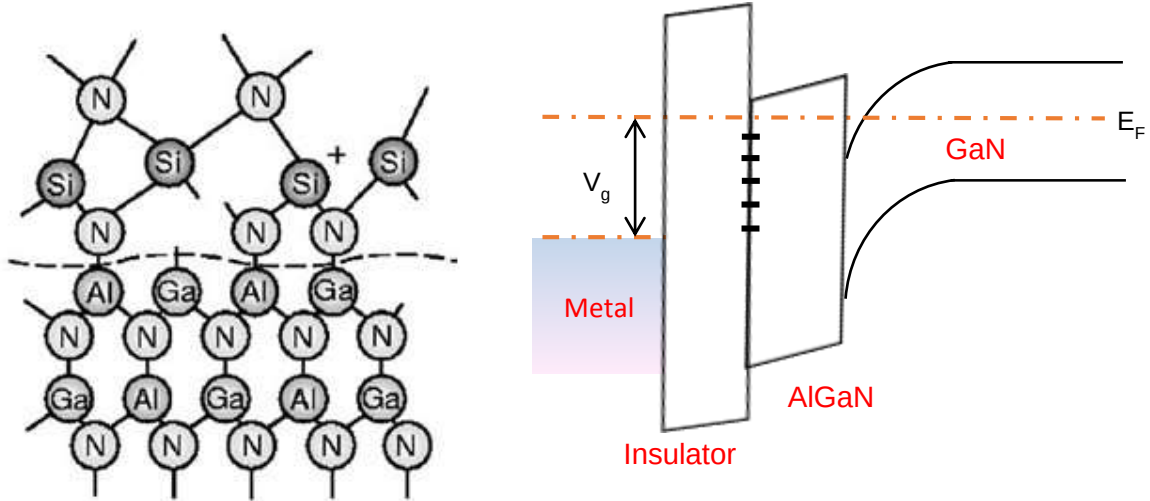


Figure 1-5 Schematic models of (a) atomic arrangements at SiN/AlGaIn interface [17] and (b) band alignment.

Several techniques have been developed to characterize interface states. The conductance method was proposed by Nicollian and Goetzberger to relate a measured admittance with interface trap states in a silicon MOS capacitor [31]. The trap information can be extracted from the measured admittance by an equivalent circuit. This technique can also be applied in GaN MISH structure for interface study. Shih et al. reported an analysis of AlN/AlGaN interface properties using the conductance method and found an interface state density larger than $10^{13}\text{cm}^{-2}\text{eV}^{-1}$ [29]. Gregusova et al. applied frequency dependent conductance measurement to characterize $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface in MISH structure, and the trap state density decreased from $10^{12}\text{cm}^{-2}\text{eV}^{-1}$ at 0.27 eV to $3\times 10^{10}\text{cm}^{-2}\text{eV}^{-1}$ at 0.45 eV [32]. Generally speaking, conductance method is more sensitive and accurate than capacitance method, but with more complexity.

C-V technique is the most frequently used technique that evaluates insulator/semiconductor interface [33]. However, conventional methods, such as Gray-Brown technique and Terman method have met some difficulties in extracting interface state density due to the pyroelectric and wide bandgap nature of nitride based materials. Therefore, several modified C-V characterization techniques such as photo-assisted C-V and frequency dependent C-V measurements have been developed in both nitride based MIS and MISH structures.

Shih et al. also studied AlN/AlGaN interface using multi-frequency C-V measurement with frequency from 100Hz to 1MHz [22]. It was found that C-V curves disperse significantly at high forward bias, probably due to a large amount of electrons trapping at AlN/AlGaN interface states. The interface state density was not extracted in this characterization method. With this technique, an elaborated investigation of the dielectric/semiconductor interface is necessary. In this work, we perform frequency dependent C-V technique extensively to study interface states at $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface.

1.4.2 Dielectrics

The study of GaN dielectric materials benefits from the continuous progress in silicon transistor scaling, which pushes forward the development of various dielectric materials. Hafnium based dielectrics have emerged as next generation dielectrics for silicon with a careful balance of various requirements, while the best dielectric for GaN remains to be investigated.

The ideal candidate material for GaN based device should have a high bandgap ($E_g > 5$ eV), high dielectric constant comparable to AlGaIn ($k \sim 9.5$), high breakdown field ($E > 10$ MV/cm) and high thermal conductivity. The most important criteria, as we discussed above for the dielectric material, is to form a good interface with AlGaIn since a good gate control of the transistor depends on dielectric/AlGaIn interfacial properties.

Insulating materials such as SiO_2 , SiN , Al_2O_3 , HfO_2 , AlN , Ga_2O_3 and Sc_2O_3 have been reported as gate dielectrics and passivation layers [8], [9], [10], [22], [23], [24]. Table 1-3 summarizes related properties and research progresses of several frequently investigated materials. Until now none of these materials performs significantly better than the others. Our study mainly focus on ALD Al_2O_3 dielectric thin films.

Table 1-3 Dielectric material properties, growth techniques and electrical performance.

	Materials Properties				Growth Technique	D_{it} ($\text{cm}^{-2}\text{eV}^{-1}$)
	E_g (eV)	ϵ_r	E_{bd} (MV/cm)	κ (W/mK)		
SiO ₂	9	3.9	10	1.4	PECVD Photo-CVD	$\sim 10^{12}$ [25] 1.1×10^{11} [26]
SiN	4.9	7	10	15-30	ECR-CVD MOCVD	1×10^{11} [20] 5×10^{12} [27]
✓ Al ₂ O ₃	7-9	8-10	>10	28-35	ALD	$3.1-14 \times 10^{12}$ [23] $> 1 \times 10^{12}$ [19]
HfO ₂	5.7	22-25	3.9-6.7	23	ALD PLD	$1.2-3.4 \times 10^{13}$ [23] 8.9×10^{11} [28]
AlN	6.2	8-10	10-15	285	Sputter MOCVD	$> 10^{13}$ [29] $10^{11}-10^{13}$ [30]

The ALD Al₂O₃ thin film is one of the pioneer materials studied in this field and it has made impressive progress recently. Many groups have demonstrated GaN based MISH, MIS-HEMT and similar structures using Al₂O₃ as the insulating material. As a gate dielectric material, the high band gap (7 eV – 9 eV), high dielectric constant (8 – 10) and high breakdown field (> 10 MV/cm) properties are especially attractive to high power and high voltage devices. However, although ALD Al₂O₃ techniques are rather mature, the discrepancies existing between thermal ALD films and plasma enhanced ALD (PEALD) films are still worth investigating. Furthermore, interfacial properties of the Al₂O₃/AlGaN are far from perfect and a large number of problems need to be resolved in terms of pre-deposition treatments and post-deposition annealing. This work on Al₂O₃/AlGaN/GaN structures compares Al₂O₃ thin films using thermal ALD and PEALD techniques, and discusses film qualities and interfacial properties using material and electrical characterization methods. Several solutions are provided to improve the dielectric material and dielectric/semiconductor interface as well.

1.5 Dissertation outline

In this thesis, the full picture of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISH structure fabrication and characterization is provided. Chapter 2 emphasizes on materials and fabrication. Al_2O_3 thin films grown by thermal ALD and PEALD are studied and the films are investigated by different material characterization tools. The device fabrication and process flow are discussed in the same chapter. Chapter 3 focuses on electrical characterization using capacitance voltage measurements. The C-V curves are interpreted, and the information on carrier concentration, dielectric constant and interface state density are extracted. Special emphases are given to $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states characterization using frequency dependent C-V tests. In chapter 4, Al_2O_3 dielectric conduction mechanisms are investigated with temperature dependent measurements in the first part. Dielectric reliability is studied and analyzed in the second part of chapter 4. Chapter 5 concludes the entire work and proposes several ideas for the future work.

1.6 References

- [1] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.
- [2] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaIn/GaIn HEMTs - An overview of device operations and applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.
- [3] B. J. Baliga, "Semiconductors for high-voltage, vertical channel FETs," *J. Appl. Phys.*, vol. 53, no. 3, pp. 1759–1764, Mar. 1982.
- [4] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, pp. 163–177, 1965.
- [5] J. H. Leach and H. Morkoc, "Status of reliability of GaIn-based heterojunction field effect transistors," *Proc. IEEE*, vol. 98, no. 7, pp. 1127–1139, Jul. 2010.

- [6] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.
- [7] H. Morkoc, *Handbook of Nitride Semiconductors and Devices*, vol. 3. New York: Wiley, 2008, ch. 3.
- [8] M. A. Khan, X. Hu, G. Simin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, "AlGaIn/GaN metal-oxide-semiconductor heterostructure field effect transistor," *IEEE Electron Device Lett.*, vol. 21, pp. 63–65, Feb. 2000.
- [9] X. Hu, A. Koudymov, G. Simin, J. Yang, M. A. Khan, A. Tarakji, M. S. Shur, and R. Gaska, "Si₃N₄/AlGaIn/GaN-metal-insulator-semiconductor heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 79, pp. 2832–2834, 2001.
- [10] T. Hashizume, T. Ootomo, and H. Hasegawa, "Suppression of current collapse in insulated gate AlGaIn/GaN heterostructure field-effect transistors using ultrathin Al₂O₃ dielectric," *Appl. Phys. Lett.*, vol. 83, no. 14, pp. 2952–2954, Oct. 2003.
- [11] V. Adivarahan, M. Gaevski, W. H. Sun, H. Fatima, A. Koudymov, S. Saygi, G. Simin, J. Yang, M. Asif Khan, A. Tarakji, M. S. Shur, and R. Gaska, "Submicron gate Si₃N₄/AlGaIn/GaN-metal-insulator-semiconductor heterostructure field-effect transistors," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 541–543, Jul. 2003.
- [12] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaIn/GaN HEMT's," *IEEE Electron Devices Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000.
- [13] W. Wang, J. Derluyn, M. Germain, M. Leys, S. Degroote, D. Schreurs, and G. Borghs, "Effect of surface passivation on two-dimensional electron gas carrier density in AlGaIn/GaN structures," *Jpn. J. Appl. Phys.*, vol. 45, no. 8, pp. L224–L226, 2006.
- [14] C.M. Jeon and J.-L. Lee, "Effects of tensile stress induced by silicon nitride passivation on electrical characteristics of AlGaIn/GaN heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 86, no. 17, pp. 172101, 2005.
- [15] Chen D J, Tao Y Q, Chen C, et al. Improved transport properties of the two-dimensional electron gas in AlGaIn/GaN heterostructures by AlN surface passivation layer. *Appl. Phys. Lett.*, vol. 89, no. 25, pp. 252104– 252106, 2006.
- [16] M. Higashiwaki, N. Onojima, T. Matsui, and T. Mimura, "Effects of SiN passivation by catalytic chemical vapor deposition on electrical properties of AlGaIn/GaN heterostructure field-effect transistors," *J. Appl. Phys.*, vol. 100, no. 3, pp. 033 714-1–033 714-6, Aug. 2006.
- [17] N. Onojima, M. Higashiwaki, J. Suda, T. Kimoto, T. Mimura, and T. Matsui, "Reduction in potential barrier height of AlGaIn/GaN heterostructures by SiN passivation," *J. Appl. Phys.*, vol. 101, no. 4, pp. 043 703-1–043 703-6, Feb. 2007.

- [18] X. Z. Dang, E. T. Yua, E. J. Piner, and B. T. McDermott, "Influence of surface processing and passivation on carrier concentrations and transport properties in AlGaIn/GaN heterostructures," *J. Appl. Phys.*, vol. 90, no. 3, pp. 1357–1361, Aug. 2001.
- [19] C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, "Capacitance–Voltage Characteristics of Al₂O₃/AlGaIn/GaN Structures and State Density Distribution at Al₂O₃/AlGaIn Interface," *Jpn. J. Appl. Phys.*, vol. 50, pp. 021001, 2011.
- [20] M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, "Effects of interface states and temperature on the C–V behavior of metal/insulator/AlGaIn/GaN heterostructure capacitors," *J. Appl. Phys.*, vol. 103, no. 10, p. 104510, May 2008.
- [21] M. Fagerlind, F. Allerstam, E. O. Sveinbjörnsson, N. Rorsman, A. Kakanakova-Georgieva, A. Lundskog, U. Forsberg, and E. Janzén, "Investigation of the interface between silicon nitride passivations and AlGaIn/AlN/GaN heterostructures by C(V) characterization of metal-insulator–semiconductor-heterostructure capacitors," *J. Appl. Phys.*, vol. 108, no. 1, p. 014 508, Jul. 2010.
- [22] H.-A. Shih, M. Kudo, and T. Suzuki, "Analysis of AlN/AlGaIn/GaN metal-insulator-semiconductor structure by using capacitance-frequency-temperature mapping," *Appl. Phys. Lett.*, vol. 101, pp. 043501, 2012.
- [23] E. Miyazaki, Y. Goda, S. Kishimoto, T. Mizutani, "Comparative study of AlGaIn/GaN metal–oxide–semiconductor heterostructure field-effect transistors with Al₂O₃ and HfO₂ gate oxide," *Solid State Electron.* Vol. 62, pp. 152-155, 2011.
- [24] R. Mehendru, B. Luo, J. Kim, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, D. Gotthold, R. Birkhahn, B. Peres, R. Fitch, J. Gillespie, T. Jenkins, J. Sewell, D. Via, and A. Crespo, "AlGaIn/GaN metal–oxide–semiconductor high electron mobility transistors using Sc₂O₃ as the gate oxide and surface passivation," *Appl. Phys. Lett.*, vol. 82, no. 15, pp. 2530–2532, Apr. 2003.
- [25] M. A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, and M. S. Shur, "AlGaIn/GaN metal-oxide-semiconductor heterostructure field effect transistor on SiC substrates," *Appl. Phys. Lett.*, vol. 77, pp. 1339–1341, 2000.
- [26] Y. Z. Chiou, S. J. Chang, Y. K. Su, C. K. Wang, T. K. Lin, and B.R. Huang, "Photo-CVD SiO₂ layers on AlGaIn and AlGaIn-GaN MOSHFET," *IEEE Trans. Electron Device*, vol. 50, no. 11, pp. 1748–1752, Nov. 2003.
- [27] B. L. Swenson and U. K. Mishra, "Photoassisted high-frequency capacitance–voltage characterization of the Si₃N₄/GaN interface," *J. Appl. Phys.*, vol. 106, no. 6, pp. 064902-1–064902-5, Sep. 2009.
- [28] F. Tian, E.F. Chor, "Physical and electrical characteristics of hafnium oxide films on AlGaIn/GaN heterostructure grown by pulsed laser deposition," *Thin Solid Films*, vol. 518, no. 241, pp. 121-124, 2010.

- [29] H.-A. Shih, M. Kudo, M. Akabori, and T. Suzuki, "Application of Sputtering-Deposited AlN Films to Gate Dielectric for AlGa_N/Ga_N Metal–Insulator–Semiconductor Heterojunction Field-Effect Transistor," *Jpn. J. Appl. Phys.*, vol. 51, pp. 02BF01, 2012.
- [30] T. Hashizume, E. Alekseev, D. Pavlidis, K. S. Boutros, and J. Redwing, "Capacitance-voltage characterization of AlN/GaN metal-insulator-semiconductor structures grown on sapphire substrate by metalorganic chemical vapor deposition," *J. Appl. Phys.*, vol. 88, pp. 1983–1986, 2000.
- [31] E. H. Nicollian and A. Goetzberger, "The Si-SiO₂ interface-electrical properties as determined by the metal-insulator-silicon conductance technique," *Bell. Syst. Tech. J.* vol. 46, pp. 1055-1133, 1967.
- [32] D. Gregušová, R. Stoklas, C. Mizue, Y. Hori, J. Novák, T. Hashizume, and P. Kordoš, "Trap states in AlGa_N/Ga_N metal-oxide-semiconductor structures with Al₂O₃ prepared by atomic layer deposition," *J. Appl. Phys.*, vol. 107, pp. 106104, 2010.
- [33] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

Chapter 2 Materials and Fabrication

2.1 AlGaN/GaN epitaxial layer

In a GaN based material system, an AlGaN/GaN heterostructure is widely used in high speed devices due to the high density of 2D electron gas (2DEG) confined at AlGaN/GaN interface. The quality of the GaN epitaxial layer and the AlGaN pseudomorphic cap plays a significant role on device performance and reliability. Usually, metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) are the two methods of growing AlGaN/GaN epi-layers. MOCVD involves a dynamic process of semiconductor formation. Gaseous reactants flow into the chamber, and the chemical reaction occur onto a heated substrate. MBE employs an ultrahigh vacuum and non-equilibrium growth condition at which reactions happen between atomic, molecular or ionized beams of corresponding elements [1].

Our AlGaN/GaN epi sample was obtained from Northrop Grumman and grown by MBE technique. The epitaxial growth was performed on a three inches sapphire substrate. A 30 nm AlN nucleation layer was first formed on sapphire, followed by a 500 nm GaN buffer layer. The AlGaN/GaN heterostructure was then grown on the GaN buffer layer, with a film thickness of 23 nm of $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$ and 140 nm of GaN. The entire epi-film structure is illustrated below in figure 2-1.

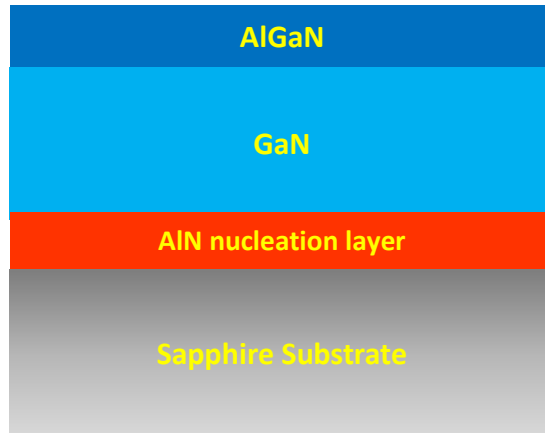


Figure 2-1 Schematic cross section of AlGaN/GaN/AlN nucleation layer/Sapphire substrate epitaxial layer.

Several material and surface characterization including atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM) and X-ray diffraction (XRD) techniques were performed on the epitaxial sample to analyze the film quality, surface properties and constituents.

Cross section TEM graphs of the epi-layer are shown in figure 2-2. We can clearly find the GaN, AlN nucleation layer and sapphire substrate in the left image. The right picture shows a small scale image of the AlGaN and GaN layer.

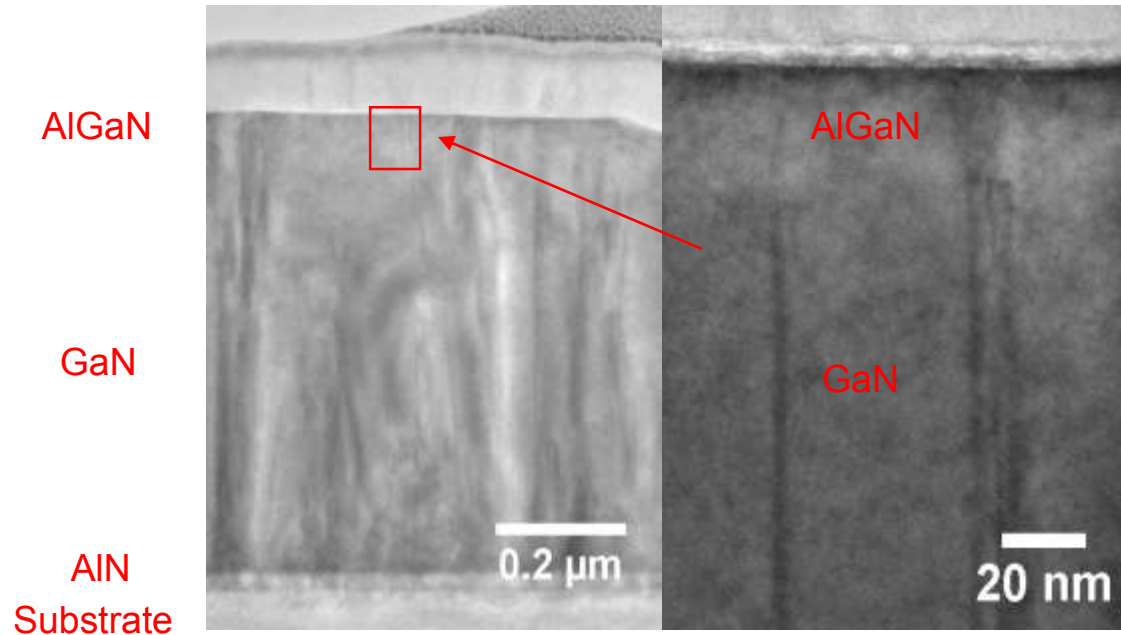


Figure 2-2 Cross section TEM image of (a) AlGaIn/GaN/AlN nucleation layer/Sapphire substrate and (b) AlGaIn/GaN epitaxial layer in a small scale.

AFM scans were also carried out on the bare epi-film surface after necessary surface cleaning, but without any surface treatment. Figure 2-3 shows an image of a 10 micron by 10 micron square area scan of the AlGaIn/GaN/AlN nucleation layer/Sapphire sample. A root mean squared (RMS) surface roughness of this area is 18.1Å.

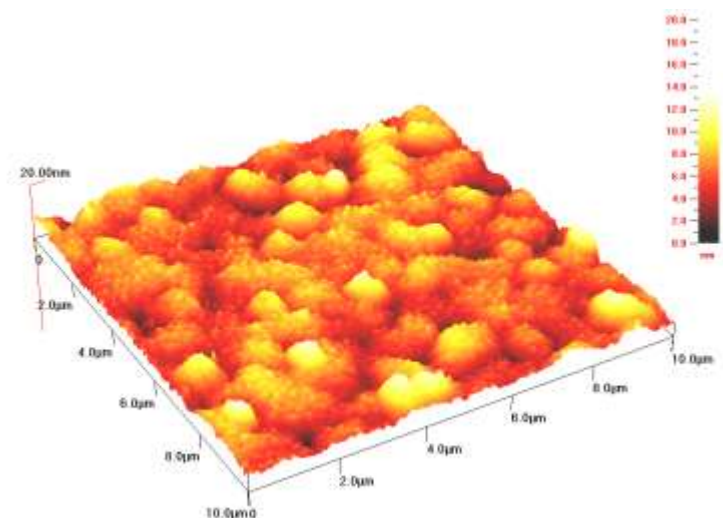


Figure 2-3 AFM graph of the AlGaIn surface of the AlGaIn/GaN/AlN nucleation layer/Sapphire substrate epitaxial layer.

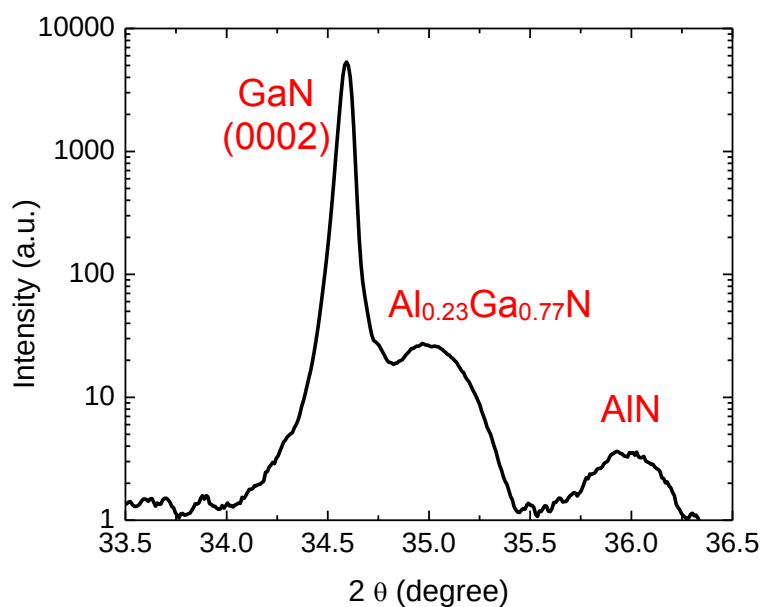


Figure 2-4 Triple axis crystal X-ray diffraction curve of AlGaIn/GaN/AlN nucleation layer/Sapphire substrate epitaxial layer.

Omega-2theta X-ray diffraction scan was performed using triple axis crystal diffractometer. There are three peaks in this picture in a given scanning range. From the scan, we can observe the presence of epitaxially grown AlGa_N and GaN films. The highest intensity peak corresponds to GaN epi-film. It also exhibits a small full width at half maximum since the GaN film has a large thickness of 640 nm. The more broaden peak next to the GaN is the AlGa_N peak with the AlGa_N thickness of only 23 nm. The peak at right of the picture indicates the signal from AlN nucleation layer. It has a low intensity and a broad width because the nucleation layer locates at the bottom of the epitaxial layer and only has 30 nm thickness.

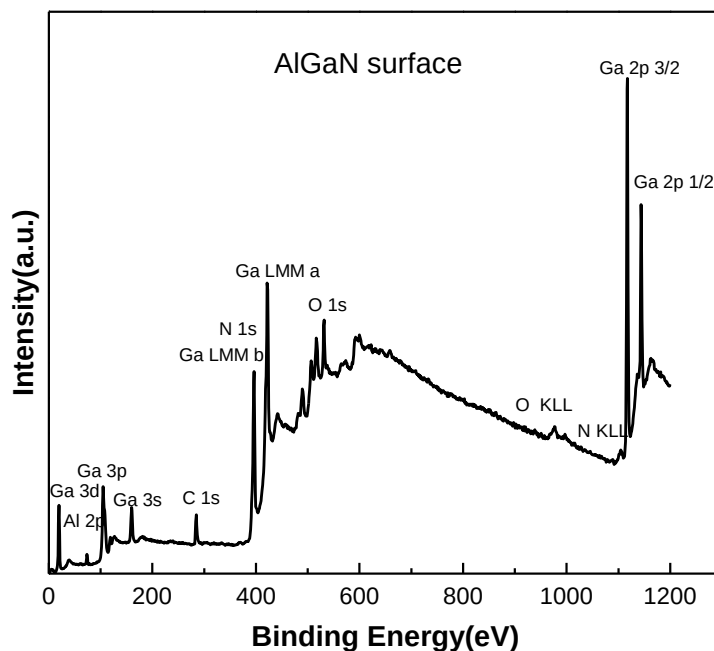


Figure 2-5 XPS survey of the AlGa_N surface.

X-ray photoelectron spectroscopy (XPS) measurements were carried out using a monochromatic Al K α X-ray source of energy 1486.7 eV (Axis Ultra DLD, Kratos Analytical). The XPS spectra

reported here are referenced to the surface C 1s peak at the binding energy (BE) of 285.0 eV and the spectra are curve-fitted with a combination of Gaussian and Lorentzian line shapes (GL30), using a Shirley-type background subtraction. Figure 2-5 shows an XPS survey of the AlGaIn surface. A stoichiometry analysis suggests an Al to Ga composition ratio of ~1:3, very close to the given ratio of the $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$ compound.

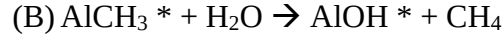
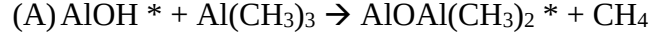
2.2 ALD Al_2O_3 thin film

2.2.1 Thin film growth

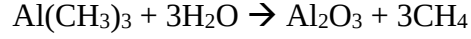
The atomic layer deposition (ALD) technique has been developed and accepted by semiconductor industry for high K dielectric application. It has a deposition process that consists a sequent of self-terminating chemical reaction steps and each limiting step dominates in the formation and saturation of a monolayer. In each of the partial reaction, a surface functional group reacts with a gas phase precursor. This reaction keeps forming a new functional group on the surface until it fully replaces the previous group. Therefore, only one monolayer is generated.

In our work, the ALD technique was implemented to Al_2O_3 dielectric thin film growth. Al_2O_3 films grown by thermal ALD and plasma enhanced ALD (PEALD) were evaluated using several material characterization methods. We also fabricated similar device structures for these two films and compared electrical performance of the devices. The chemical reaction and precursors for thermal ALD and PEALD Al_2O_3 techniques are actually different from each other.

The thermal ALD Al_2O_3 process is conducted in a heated chamber using trimethylaluminum (TMA) as precursor and H_2O as oxidizing agent [2]. The surface reaction formula is described as following:



where surface groups are expressed with asterisks. The self-limiting Al_2O_3 growth occurs during TMA and H_2O alternating exposures. The overall reaction chemistry is:



PEALD has a unique process that a self-limiting deposition is followed by a surface activation or ligand extraction step with radicals generated from a plasma. The radical in the plasma induces the reaction with surface ligands with a low activation energy and therefore it increases the deposition rate and allows a lower deposition temperature. The PEALD Al_2O_3 process is conducted using TMA as precursor and plasma oxygen as oxidizing agent.

In this work, all the dielectric deposition processes were performed at UCLA Nanolab. We utilized two ALD systems: Savannah and Fiji both from Cambridge Nanotech Inc. Savannah was only used for thermal ALD while Fiji for both thermal and plasma ALD. The recipes are shown in the following tables.

Table 2-1 Thermal ALD Al_2O_3 process in Savannah system.

Valve	Time (s)	Pump (s)	Sccm	Delay (min)
0 (H_2O)	0.1	15	20	10
2 (Al)	0.05	15		

Table 2-2 Thermal ALD Al₂O₃ process in Fiji system.

	Instruction	#	Value	
0	flow	0	20	Set precursor manifold stand-by Ar flow rate
1	flow	1	40	Set plasma source stand-by Ar flow rate
2	heater	12	200	Set trap/cone temperature
3	heater	13	200	Set reactor zone 1 temperature
4	heater	14	200	Set reactor zone 2 temperature
5	heater	15	200	Set chuck temperature
6	heater	16	150	Set precursor delivery line to 150°C
7	heater	17	150	Set precursor manifold to 150°C
8	stabilize	12		Wait for trap/cone temperature to stabilize
9	stabilize	13		Wait for reactor zone 1 temperature to stabilize
10	stabilize	14		Wait for reactor zone 2 temperature to stabilize
11	stabilize	15		Wait for chuck temperature to stabilize
12	wait		600	Wait for substrate temperature to stabilize
13	flow	0	30	Set precursor manifold Ar for expo step
14	flow	1	100	Set plasma source Ar for expo step
15	APC		9	Set throttle valve.
16	wait		10	Wait for Ar MFC's to stabilize
17	pulse	1	0.06	Begin loop. Pulse TMA. TMA = TMA ALD valve number
18	wait		10	Purge TMA and reaction by-products
19	pulse	0	0.06	Pulse H ₂ O. H ₂ O = H ₂ O ALD valve number
20	wait		10	Purge H ₂ O and reaction by-products
21	goto	17	X	Input # of cycles, number, x = cycles, GPC ~ 1A/cycle
22	flow	0	5	Set precursor manifold stand-by Ar flow rate
23	flow	1	10	Set plasma source stand-by Ar flow rate
24	APC		100	Open throttle valve. If no throttle valve, remove this line
25	Turbopurge		0	
26	Doorpurge		0	

Table 2-3 PEALD Al₂O₃ process in Fiji system.

	Instruction	#	Value	
0	flow	0	20	Set precursor manifold stand-by Ar flow rate
1	flow	1	40	Set plasma source stand-by Ar flow rate
2	heater	12	200	Set trap/cone temperature
3	heater	13	200	Set reactor zone 1 temperature
4	heater	14	200	Set reactor zone 2 temperature
5	heater	15	200	Set chuck temperature
6	heater	16	150	Set precursor delivery line to 150°C
7	heater	17	150	Set precursor manifold to 150°C
8	stabilize	12		Wait for trap/cone temperature to stabilize
9	stabilize	13		Wait for reactor zone 1 temperature to stabilize
10	stabilize	14		Wait for reactor zone 2 temperature to stabilize
11	stabilize	15		Wait for chuck temperature to stabilize
12	wait		600	Wait for substrate temperature to stabilize
13	flow	0	30	
14	flow	1	100	
15	APC		9	Set throttle valve
16	wait		10	Wait for Ar MFCs to stabilize
17	MFCvalve	3	1	Set precursor manifold Ar for expo step
18	wait		20	
19	pulse	1	0.06	Begin loop. Pulse TMA. TMA = TMA ALD Valve number
20	wait		10	Purge TMA and reaction by-products
21	flow	3	50	Start O ₂ flow
20	plasma		300	Turn on plasma.
23	wait		20	
24	plasma	0	0	Turn off plasma.
25	flow	3	0	Start O ₂ flow.
26	wait		5	Purge O ₂ and reaction by-products
27	goto	19	X	Input # of cycles, number, x = cycles, GPC ~ 1A/cycle
28	flow	0	5	
29	flow	1	10	
30	flow	3	0	Turn off O ₂
31	APC		100	Open throttle valve. If no throttle valve, remove this line
32	turbopurge		0	
33	doorpurge		0	

2.2.2 Al₂O₃ thin film characterization

2.2.2.1 Surface morphology

AFM was applied to study surface morphology for Al₂O₃ films grown by different techniques. Figure 2-6 presents four surface images that compare Al₂O₃ films on the AlGaIn/GaN layer. The surface of thermal ALD Al₂O₃ films is shown in figure (a) and (b) and the surface of PEALD Al₂O₃ films is shown in figure (c) and (d). Samples in figure (a) and (c) were as-deposited condition while samples in figure (b) and (d) were annealed for 5 minutes in 1000°C nitrogen atmosphere after deposition. Compared with bare AlGaIn/GaN surface in figure 2-3, all the deposited Al₂O₃ films exhibit much lower surface roughness, which indicates a conformal and smooth coating of thin film by ALD. Among them, PEALD films show a slightly lower roughness than thermal ALD films. But the difference between the as-deposited samples and annealed samples is within 0.5Å, which is almost negligible.

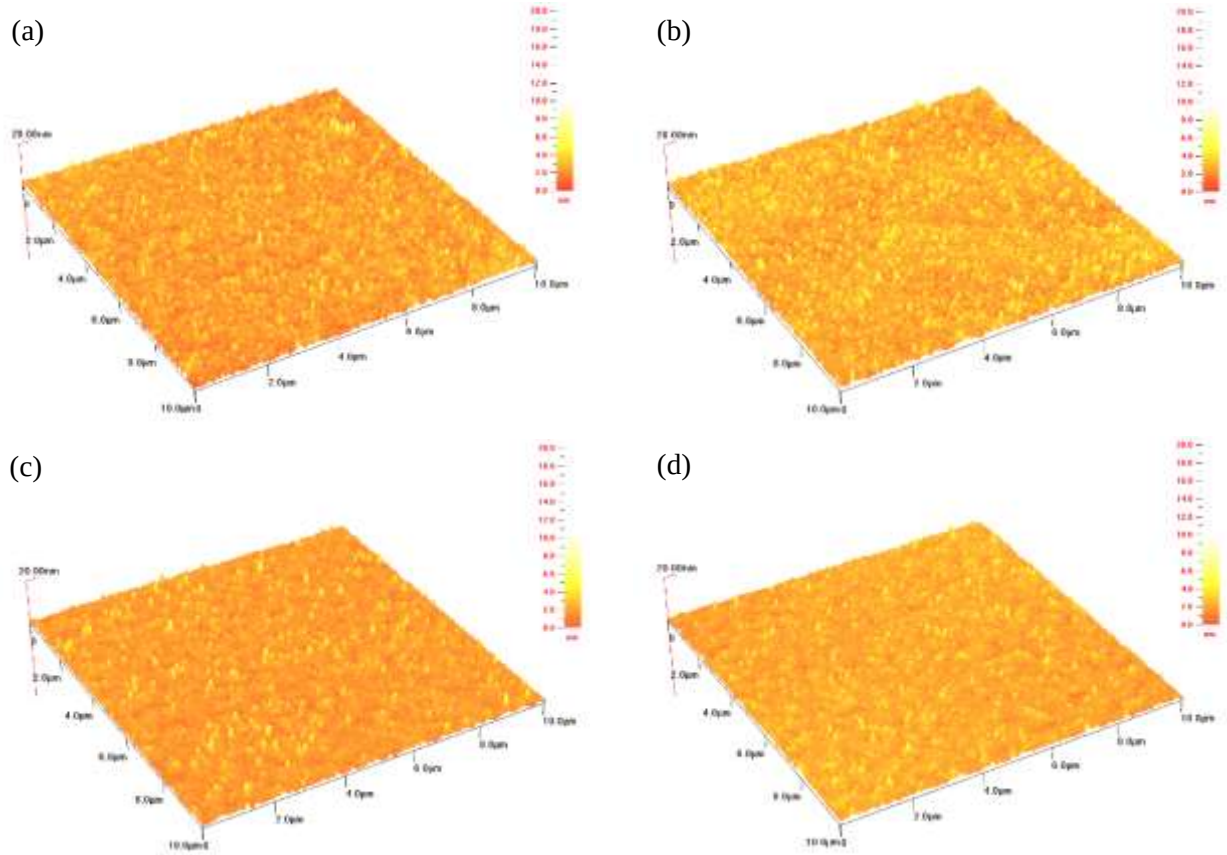


Figure 2-6 AFM image of (a) thermal ALD 50 nm Al_2O_3 thin film as-deposited, (b) thermal ALD 50 nm Al_2O_3 thin film annealed at 1000°C for 5 minutes, (c) PEALD 50 nm Al_2O_3 thin film as-deposited and (d) PEALD 50 nm Al_2O_3 thin film annealed at 1000°C for 5 minutes. RMS roughness of (a), (b), (c) and (d) are 6.7Å, 7.0Å, 6.1Å and 5.6Å, respectively.

2.2.2.2 XPS

XPS measurements were carried out to study bonding information and band alignment for both Al_2O_3 thin films and $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces. To observe the signal from $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces, very thin Al_2O_3 layers were deposited by both thermal ALD and PEALD techniques [3], and the results were compared with those on AlGaIn layer surface and thick Al_2O_3 films.

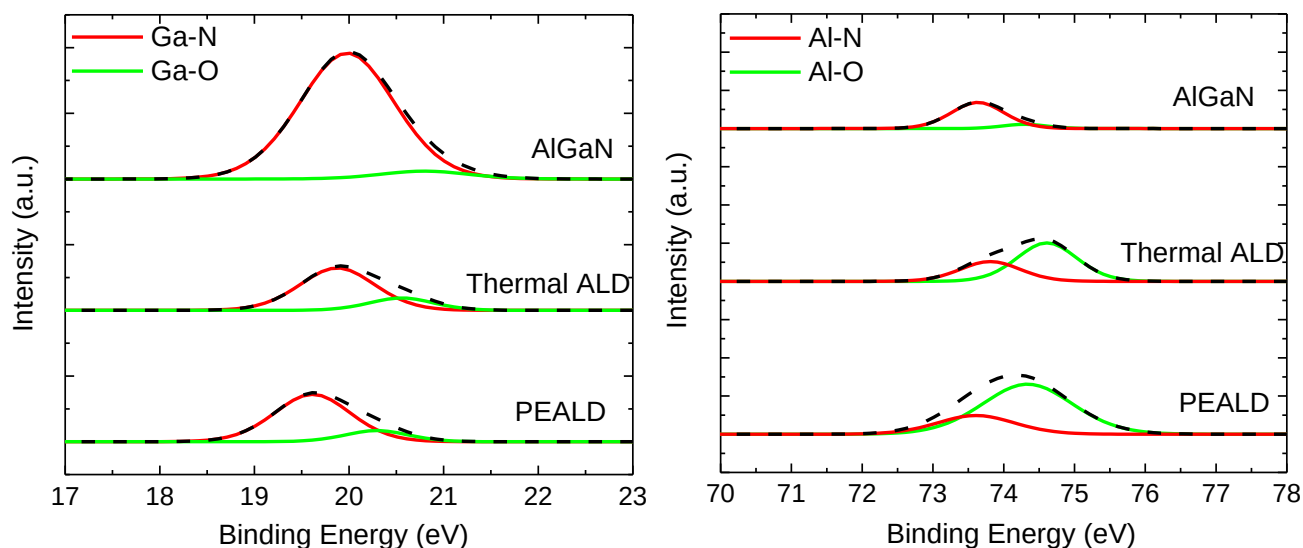


Figure 2-7 XPS (a) Ga 3d and (b) Al 2p core-level spectra of AlGaN, thermal ALD Al_2O_3 thin film on AlGaN and PEALD Al_2O_3 thin film on AlGaN.

Figure 2-7 shows Ga 3d and Al 2p core-level spectra for AlGaN, PEALD Al_2O_3 thin film on AlGaN and thermal ALD Al_2O_3 thin film on AlGaN. The detail thickness of films and the binding energy are given in table 2-4 below. It can be seen that Ga 3d peak positions shift towards smaller binding energy for thermal ALD and PEALD Al_2O_3 thin films. These shifts might be attributed to dipole formation at $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface that change the AlGaN surface potential.

It should also be noted that Ga-O to Ga-N bond ratio increases from 0.057 for AlGaN to 0.196 for PEALD film and 0.25 for thermal ALD film. The rising ratio implies that GaO_x forms at interface during both ALD Al_2O_3 growth. The lower GaO_x composition in PEALD grown sample suggests that plasma process has a better control to the surface oxide formation.

Table 2-4 Thickness, binding energy and Ga-O/Ga-N ratio of AlGaIn, thermal ALD Al₂O₃ thin film on AlGaIn and PEALD Al₂O₃ thin film on AlGaIn.

		Binding Energy (eV)				
		Ga 3d		Al 2p		
Sample	Al ₂ O ₃ thickness(nm)	Ga-N	Ga-O	Al-O	Al-N	GaOx/GaN
AlGaN	0	20.02	20.84	74.33	73.67	0.057
PEALD	3.90	19.69	20.37	74.41	73.68	0.196
Thermal	3.75	19.87	20.55	74.61	73.81	0.25

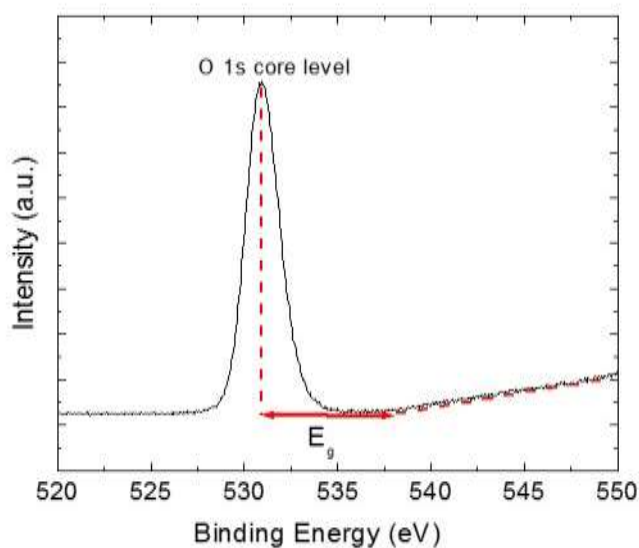


Figure 2-8 XPS O1s energy loss spectrum of 50 nm PEALD Al₂O₃ thin film on AlGaIn.

The bandgap of the Al₂O₃ film can be estimated using O 1s energy loss spectrum. Figure 2-8 shows a spectrum for the 50 nm PEALD Al₂O₃ film. The separation of energy between O 1s peak and

plasmon loss onset represents the minimum energy for an electron to reach conduction band and result in plasmonic oscillation, and is approximately the energy bandgap. Here, the bandgap for the PEALD Al_2O_3 film is measured as 7.0 eV. Table 2-5 shows a comparison of the bandgap for both thermal ALD and PEALD Al_2O_3 films as-deposited and after 1000°C annealing. The increase of Al_2O_3 bandgap after annealing is due to that Al_2O_3 thin films change from amorphous to polycrystalline at high annealing temperatures.

Table 2-5 Band gap of 50 nm thermal ALD Al_2O_3 thin films and PEALD Al_2O_3 thin films with and without annealing.

Sample	Bandgap (eV)
Thermal ALD	6.7
Thermal ALD + Annealing	7.0
PEALD	7.0
PEALD + Annealing	7.3

The refractive index measurement also gave us an Al_2O_3 film density of ~ 1.5 in thermal ALD, much lower than the normal ALD Al_2O_3 density (1.6 - 1.65). This might be due to the existence of excessive CH_3 ligands from $\text{Al}(\text{CH}_3)_3$ precursor, and they are not fully dissociated during the thermal based deposition. The light atoms from the ligands such as carbon and hydrogen lead to a low Al_2O_3 film density. Since the density of TMA precursor is about 1/5 of the Al_2O_3 density, the impurity concentration can be estimated around 10% - 12% assuming refractive index is linearly proportional to film density, since we have observed an 8% - 10% reduction of refractive index.

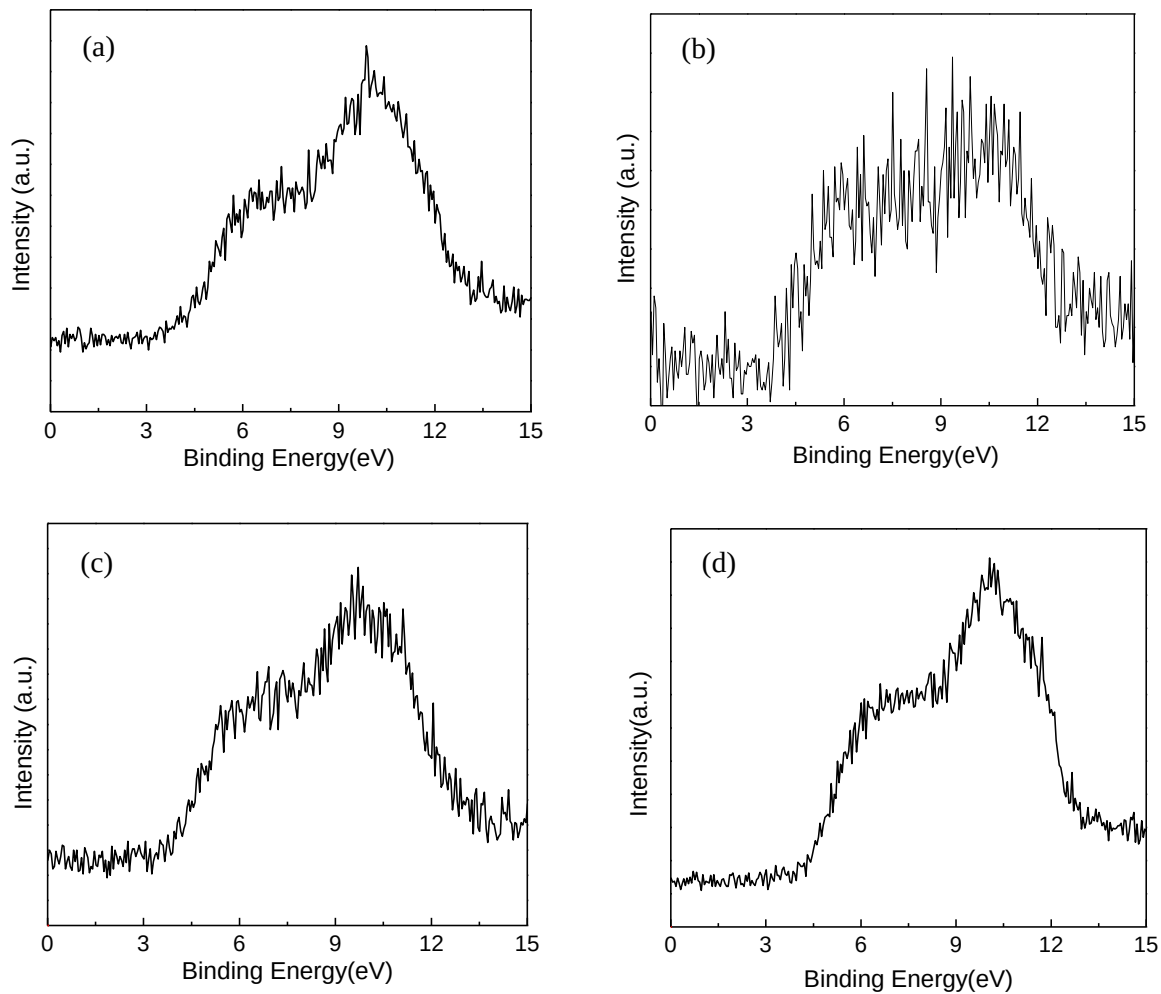


Figure 2-9 Valence band spectra of 50 nm (a) PEALD Al_2O_3 thin film after annealing, (b) PEALD Al_2O_3 thin film as-deposited, (c) thermal ALD Al_2O_3 thin film after annealing and (d) thermal ALD Al_2O_3 thin film as-deposited.

Valence band spectra of both thermal ALD and PEALD Al_2O_3 films with and without post annealing are depicted in figure 2-9. The valence band maximum (VBM) of each sample is extrapolated by crossing the leading edge of the spectrum over the baseline.

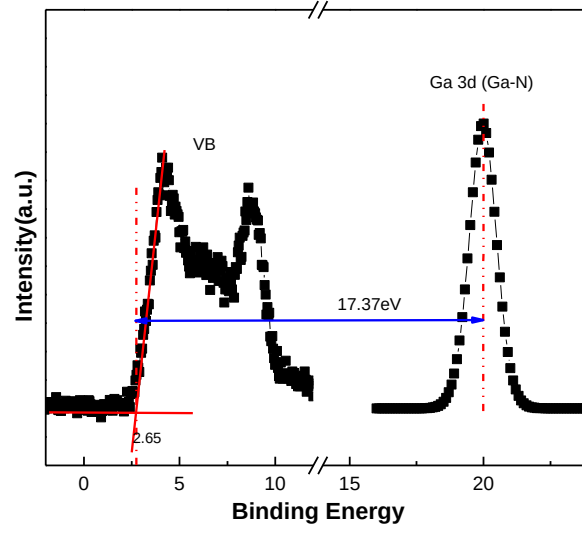


Figure 2-10 Ga 3d core-level and valence band spectra of AlGaN.

To calculate the valence band offset (VBO), we have

$$VBO = [E_{CL}^{Al_2O_3}(b) - E_V^{Al_2O_3}(b)] - [E_{CL}^{AlGaN}(b) - E_V^{AlGaN}(b)] - [E_{CL}^{Al_2O_3}(i) - E_{CL}^{AlGaN}(i)]$$

The letter E indicates the binding energy. The subscript CL and V stand for core-level and VBM, respectively. The letter b stands for the bulk Al_2O_3 and AlGaN signal while i for the interface signal. The binding energy difference between bulk AlGaN core-level and VBM is presented in figure 2-10. By substituting all the numbers into the equation above, we can obtain the valence band offset (ΔE_v) for Al_2O_3 films. Since we have measured the dielectric bandgap, the conduction band offset can also be calculated below:

$$\Delta E_c = E_g(Al_2O_3) - E_g(AlGaN) - \Delta E_v$$

where the bandgap of $Al_{0.23}Ga_{0.77}N$ is [4]:

$$E_g(\text{Al}_x\text{Ga}_{1-x}\text{N}) = 3.42 \text{ eV} + x \cdot 2.86 \text{ eV} - x(1 - x) \cdot 1.0 \text{ eV}$$

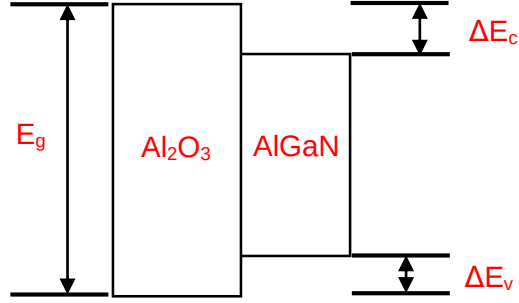


Figure 2-11 Schematic band alignment of $\text{Al}_2\text{O}_3/\text{AlGaN}$.

Figure 2-11 shows a schematic band alignment of $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface and band offset. The number of ΔE_v and ΔE_c are summarized in table 2-6 for the as-deposited and annealing samples. The valence band offsets of the Al_2O_3 films after annealing are in agreement with reported studies.

Table 2-6 Summary for valence band offset and conduction band offset of thermal ALD and PEALD Al_2O_3 thin film samples with and without annealing.

Sample	ΔE_v (eV)	ΔE_c (eV)
Thermal ALD	1.2	1.6
Thermal ALD + Annealing	0.8	2.3
PEALD	1.0	2.1
PEALD + Annealing	0.7	2.7

2.2.2.3 Crystal structure

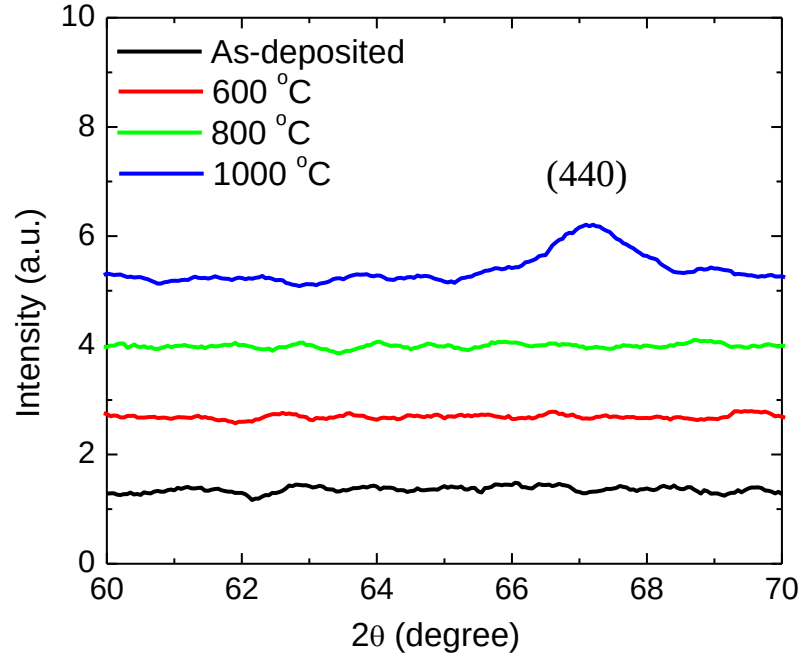


Figure 2-12 Grazing incidence X-ray diffraction of 50 nm Al_2O_3 thin films grown in one chamber but with different post annealing temperatures.

To understand the crystal structure of Al_2O_3 thin films, we deposited 50 nm Al_2O_3 films using PEALD on p-type silicon substrate. The deposition was followed by 5 minutes rapid thermal annealing in nitrogen atmosphere with various temperature conditions from 600°C to 1000°C. The crystal structure and crystallization behavior of as-deposited and annealed Al_2O_3 thin films were investigated using grazing incidence X-ray diffraction.

The scans were conducted from low angle to high angle (10° to 80°). The intensity curves do not show any peaks along the scanning range for samples without annealing or annealed at 600°C and 800°C, which might suggest that Al_2O_3 thin films under these conditions are amorphous. However,

the sample annealed at 1000°C shows a peak at two theta of 67° in figure 2-12. The appearance of this peak may indicate the crystallinity has changed for Al₂O₃ thin films at high temperatures. The Al₂O₃ thin film probably transforms from amorphous to polycrystalline at a temperature between 800°C and 1000°C. Our result is also in agreement with other reported ALD Al₂O₃ studies [5], [6]. It is suggested that the Al₂O₃ thin film has a crystallization temperature around 900°C and the film structure changes from amorphous to γ -Al₂O₃.

2.3 Fabrication

2.3.1 GaN process

Many efforts have been spent on solving GaN process issues since nitride based III-V material and process technology is significantly different from traditional silicon and gallium arsenide technology. In general, a successful process requires a good uniformity, reproducibility and reliability. Before realizing a stable process flow, some of special requirements have to be satisfied for high performance GaN FETs. The following points are particularly important in GaN process [7]:

- Surface cleaning, pre-treatment and post annealing to remove native oxide and reduce interface defect states
- Good device isolation to avoid device crosstalk
- Low resistance contacts for high performance transistors
- Good dielectric materials to achieve low leakage current

2.3.2 Process flow for MISH devices

Some of the issues mentioned above were investigated when we start to build our own GaN process flow in UCLA nanolab. Problems including pre-treatment and post annealing will be addressed in following paragraphs. Before we discuss these processes, the entire process flow of our GaN MISH device is presented.

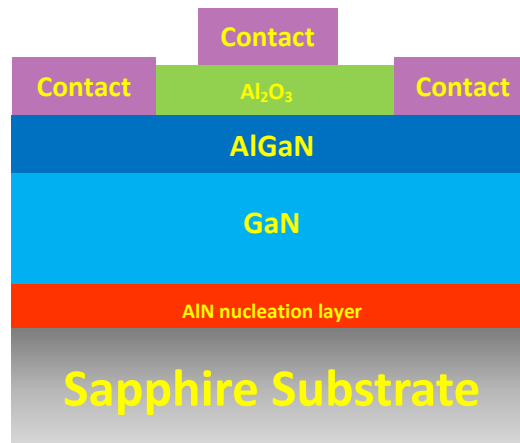


Figure 2-13 Schematic cross section of metal/Al₂O₃/AlGaN/GaN MISH structure.

Figure 2-13 shows an MISH test device structure. The detail steps are listed below.

- Surface cleaning
- Ohmic contacts formation
- Rapid thermal annealing
- Pre-deposition treatment
- Dielectric deposition
- Post-deposition annealing
- Gate contacts formation

A short description of each steps is summarized here.

An AlGaIn/GaN bare substrate was first rinsed by acetone and IPA to remove organic species. The sample was then dipped into HF solution for 5 minutes and HCl solution for 2 minutes to remove native oxide and metal contaminants, and followed by DI water rinse.

After surface cleaning, the sample was patterned and ohmic contacts were deposited using e-beam evaporator in nanolab. Ring pattern Ti/Al/Ni/Au metal stacks were evaporated on sample surface. The thickness of this four layers was 20nm/120nm/40nm/50nm. Ti/Al metal stack was also fabricated and compared to the Ti/Al/Ni/Au contact.

To obtain ohmic contacts, rapid thermal annealing was performed at 830 °C for 1 minute in nitrogen atmosphere.

A plasma surface treatment was carried out prior to the ALD process. We applied plasma N₂ and NH₃ on AlGaIn surface to improve Al₂O₃/AlGaIn interfacial properties. ALD Al₂O₃ film was then grown on the sample using standard procedure shown previously, and it was followed by a post annealing in different ambient with varied temperature. The annealing impact on devices will be shown in detail in next chapter.

The final step was the Ni/Au gate contact formation. A 40nm/50nm metal contact was deposited using e-beam evaporator as well.

All the steps above were finished in UCLA nanolab.

2.3.3 Pre-deposition treatment

Since the dielectric/semiconductor interface quality is crucial to transistor performance, special processes and treatments have been applied before or after dielectric deposition to reduce defect states and improve device behavior. From the experience in traditional silicon industry, we learn that surface plasma treatments prior to dielectric deposition may significantly affect number of interface states and fixed charges at the interface. Depending on the type of plasma treatment, the process may remove native oxide, form an interlayer that assists following deposition or modify surface states to achieve a desirable band alignment [8], [9].

In our work, we incorporated two types of surface pre-treatments that may be favorable to $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfacial behavior. The plasma species we chose here were ammonia and nitrogen. A brief introduction of these plasmas and their background in semiconductor applications are given below.

NH_3 plasma treatment has been employed in silicon industry because of its ability to form nitridation layer. This nitridation layer allows the following growth of silicon nitride or silicon oxynitride. This method was also introduced in GaN based HEMT devices as a pre-treatment step prior to SiN passivation. It was reported that the treatment effectively reduced gate lag and current collapse, and improved AlGaIn/GaN HEMT reliability [10].

Nitrogen plasma is an alternative source to the nitridation layer formation. In addition, different usage of N_2 plasma has been widely reported on GaN based electronic devices. It was not only performed to remove surface residue contaminants such as carbon and oxides, but also to reduce gate leakage and mitigate device I-V dispersion [11], [12], [13], [14].

In addition, oxygen plasma surface pre-treatment was another method that intensively applied on sample cleaning and oxidation layer growth. Studies on AlGaN or GaN O_2 plasma surface treatments show a lower surface impurity concentration but an increased oxygen content. The high power O_2 plasma may assist to form a surface oxidation layer, and this layer aims to reduce gate leakage current and RF collapse. It was also suggested that oxygen treatment is beneficial to ohmic contact formation on the n-type GaN surface. In our case, however, the plasma oxygen treatment favors the growth of GaOx surface oxide layer. This layer creates more dangling bonds and increases the density of interface states at Al_2O_3 /AlGaN interface [15], [16], [17].

The plasma NH_3 and N_2 pre-deposition surface treatment were performed before ALD Al_2O_3 film growth. Various power and time were applied to the treatments. The process temperature was set at $300^\circ C$ and chamber pressure was 300 mTorr.

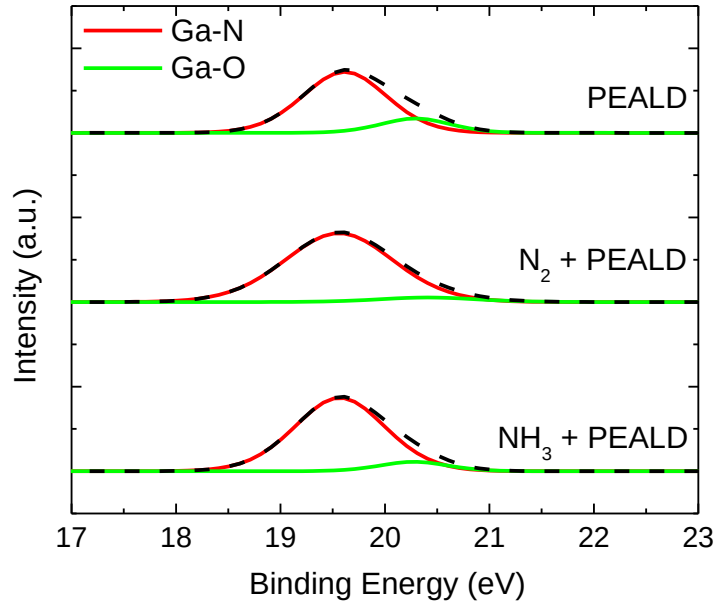


Figure 2-14 XPS Ga 3d core-level spectra of PEALD Al_2O_3 thin films on AlGaN with plasma NH_3 , N_2 and without surface plasma treatment.

Figure 2-14 shows the XPS results of the plasma treated samples. These samples were subject to 5 minutes and 50W N₂ and NH₃ treatments, and followed by a thin PEALD Al₂O₃ film deposition. One sample with only PEALD growth was also measured as comparison. It can be seen that the Ga-O peak intensity in both N₂ and NH₃ treated samples is lower than the non-treated sample. Table 2-7 summarizes the binding energy and Ga-O/Ga-N ratio of each sample. We can clearly observe that GaO_x/GaN ratio reduces when the plasma treatment is performed before deposition. The N₂ treatment is more effective since the ratio is nearly identical to the one measured with bare AlGaIn surface. The XPS data suggests that nitrogen based plasma treatments lead to a good suppression of GaO_x layer which is detrimental to Al₂O₃/AlGaIn interfacial properties. The plasma N₂ and NH₃ serve as nitridation sources and form thin nitridation layers on the AlGaIn surface, and the nitrided film prevents GaO_x growth at the initial of the ALD process.

Table 2-7 Binding energy and Ga-O/Ga-N ratio of AlGaIn, PEALD Al₂O₃ thin films on AlGaIn with and without surface plasma treatment.

	Binding Energy (eV)				
	Ga 3d		Al 2p		
Sample	Ga-N	Ga-O	Al-O	Al-N	GaO _x /GaN
AlGaN	20.02	20.84	74.33	73.67	0.057
PEALD	19.69	20.37	74.41	73.68	0.196
NH ₃	19.57	20.28	74.33	73.5	0.096
N ₂	19.62	20.47	74.29	73.52	0.059

2.3.4 Post-deposition annealing

The post ALD annealing of Al_2O_3 films is also considered as a critical step to improve film quality and interfacial properties. As suggested above, the crystal structure change of the Al_2O_3 film is subject to the post annealing temperature. Different annealing temperatures and gaseous species were investigated to acquire the best film quality and device performance.

The post annealing temperature study was conducted in N_2 ambient. It was reported that the annealing process can effectively reduce dielectric/semiconductor interface state density. We performed our annealing temperature lower than the Al_2O_3 phase transition point, since the polycrystalline dielectric film results in high leakage current. From previous section, we have already found that the phase transition for amorphous Al_2O_3 films to polycrystalline films occurs around 900°C . Therefore, the annealing temperatures were varied from 400°C to 700°C in our investigation to avoid this phase transformation [18].

Nitrous oxide (N_2O) plasma treatment is another widely used technique in silicon industry to form oxynitride films and improve interfacial properties. The incorporation of nitrogen in this annealing step can both increase dielectric constant and lead to a more robust oxide resistive to impurity diffusion. It was also found that a higher breakdown field and a lower interface state density were achieved after exposing Si/SiO_2 films to a N_2O plasma [19]. The N_2O surface pre-treatment on GaN surface was also investigated on GaN MIS diodes and a better dielectric/semiconductor interface was observed [20]. In our experiment, we performed a low temperature plasma N_2O annealing to observe if the dielectric transport behavior was improved.

2.4 References

- [1] R. F. Davis, A. M. Roskowski, E. A. Preble, J. S. Speck, B. Heying, J. A. Freitas, Jr., E. R. Glaser, and W. E. Carlos, "Gallium nitride materials - Progress, status, and potential roadblocks," *Proc. IEEE*, vol. 90, pp. 993-1005, 2002.
- [2] S. George, "Atomic layer deposition: an overview," *Chem. Rev.* vol. 110, pp. 111-131, 2010.
- [3] T. L. Duan, J. S. Pan, D. S. Ang, "Interfacial chemistry and valence band offset between GaN and Al₂O₃ studied by X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 102, no. 20, pp. 201604, 2013.
- [4] F. Yun, M. A. Reshchikov, L. He, T. King, H. Morkoç, S. W. Novak and L. Wei, "Energy band bowing parameter in Al_xGa_{1-x}N alloys," *J. Appl. Phys.*, vol. 92, pp. 4837-4839, 2002.
- [5] S. Jakschik, U. Schroeder, T. Hecht, M. Gutsche, H. Seidl and J. W. Bartha, "Crystallization behavior of thin ALD-Al₂O₃ films," *Thin Solid Films*, vol. 425, no. 1, pp. 216-220, 2003.
- [6] C. M. Tanner, Y. C. Perng, C. Frewin, S. E. Saddow and J. P. Chang, "Electrical performance of Al₂O₃ gate dielectric films deposited by atomic layer deposition on 4H-SiC," *Appl. Phys. Lett.*, vol. 91, no. 20, pp. 203510, 2007.
- [7] R. Quay, "Gallium Nitride Electronics," vol. 96, Springer, 2008.
- [8] F. H. P. M. Habraken and A. E. T. Kuiper, "Silicon nitride and oxynitride films," *Materials Science and Engineering: R: Reports*, vol. 12, no. 3, pp. 123-175, 1994.
- [9] Y. Cai, Y. Zhou, K. J. Chen and K. M. Lau, "High-performance enhancement-mode AlGa_N/Ga_N HEMTs using fluoride-based plasma treatment." *IEEE Electron Devices Lett.*, vol. 26, no. 7, pp. 435-437, 2005.
- [10] S. Shimoda, I. Shimizu and M. Migitaka, "Chemical vapor deposition of a silicon nitride layer with an excellent interface by NH₃ plasma treatment," *Appl. Phys. Lett.*, vol. 52, no. 13, pp. 1068-1070, 1988.
- [11] Q. Feng, Y. Hao, and Y. Z. Yue, "The reduction of gate leakage of AlGa_N/Ga_N metal-insulator-semiconductor high electron mobility transistors by N₂ plasma pretreatment," *Semicond. Sci. Technol.*, vol. 24, no. 2, pp. 025030, 2009.
- [12] M. F. Romero, A. Jiménez, J. Miguel-Sánchez, A. F. Brana, F. González-Posada, R. Cuervo and E. Munoz, "Effects of Plasma Pretreatment on the Si₃N₄ Passivation of AlGa_N/Ga_N HEMT," *IEEE Electron Devices Lett.*, vol. 29, no. 3, pp. 209-211, 2008.
- [13] T. Hashizume, S. Ootomo, S. Oyama, M. Konishi and H. Hasegawa, "Chemistry and electrical properties of surfaces of GaN and GaN/AlGa_N heterostructures," *J. Vac. Sci. Technol., B*, vol. 19, no. 4, pp. 1675-1681, 2001.

- [14] J. H. Kim, H. G. Choi, M. W. Ha, H. J. Song, C. H. Roh, J. H. Lee and C. K. Hahn, "Effects of nitride-based plasma pretreatment prior to SiNx passivation in AlGaIn/GaN high-electron-mobility transistors on silicon substrates," *Jpn. J. Appl. Phys.*, vol. 49, no. 4S, pp. 04DF05, 2010.
- [15] F. González-Posada, J. A. Bardwell, S. Moisa, S. Haffouz, H. Tang, A. F. Braña and E. Muñoz, "Surface cleaning and preparation in AlGaIn/GaN-based HEMT processing as assessed by X-ray photoelectron spectroscopy," *Appl. Surf. Sci.*, vol. 253, no. 14, pp. 6185-6190, 2007.
- [16] D. S. Lee, J. W. Chung, H. Wang, X. Gao, S. Guo, P. Fay and T. Palacios, "245-GHz InAlN/GaN HEMTs with oxygen plasma treatment," *IEEE Electron Devices Lett.*, vol. 32, no. 6, pp. 755-757, 2011.
- [17] J. Yan, M. J. Kappers, Z. H. Barber and C. J. Humphreys, "Effects of oxygen plasma treatments on the formation of ohmic contacts to GaN," *Appl. Surf. Sci.*, vol. 234, no. 1, pp. 328-332, 2004.
- [18] Y. Q. Wu, T. Shen, P. D. Ye and G. D. Wilk, "Photo-assisted capacitance-voltage characterization of high-quality atomic-layer-deposited Al₂O₃/GaN metal-oxide-semiconductor structures," *Appl. Phys. Lett.*, vol. 90, no. 14, pp. 143504-143504, 2007.
- [19] P. C. Chen, K. Y. Hsu, H. L. Hwang and J. Y. Lin, "Fundamental electrical properties of fluorinated and N₂O plasma-annealed ultrathin silicon oxides grown by microwave plasma afterglow oxidation at low temperatures," *J. Appl. Phys.*, vol. 76, no. 9, pp. 5508-5514, 1994.
- [20] Y. Hori, C. Mizue and T. Hashizume, "Interface state characterization of ALD-Al₂O₃/GaN and ALD-Al₂O₃/AlGaIn/GaN structures," *Phys. Status Solidi C*, vol. 9, no. 6, pp. 1356-1360, 2012.

Chapter 3 Defect state characterization

3.1 Background

Since metal-insulator-semiconductor transistors were invented, the dielectric/semiconductor interfacial property has always been the first issue to concern in terms of device performance and reliability. Traps and defect states at the dielectric/semiconductor interface not only affect an effective gate control to the conduction channel by shifting electrostatic potential, but also degrade device parameters such as current and transconductance. In addition, trapped holes and electrons may interact with carriers and damage interface or even bulk insulator by breaking local bonds. The dangling bonds create new traps and trap more holes and electrons. The entire process brings reliability problems in long term transistor operations.

Fortunately, our nature creates a nearly perfect silicon-silicon dioxide interface for us. The low state density at Si/SiO₂ interface allows the invention of silicon base MOSFETs, which enable tremendous advancement and breakthrough in modern electronic industry in the past half century. In the meanwhile, various theories, techniques and tools have been developed to characterize silicon based devices and Si/SiO₂ interface. These methods are mature and now being applied to other semiconductor material and device systems. In our work, we take the advantage and modify these characterization techniques to fit our own application.

Different from Si/SiO₂ interface, interfaces between dielectric and III-V based semiconductors have been facing serious issues due to lack of reliable native oxide and the binary characteristic of the materials themselves. The gallium arsenide (GaAs) society has been struggling with these problems for thirty years, and now same situation occurs in nitride based semiconductors. Usually, the density of defect states at a dielectric/III-V interface is around $10^{12}/\text{cm}^2\text{eV}$ to $10^{13}/\text{cm}^2\text{eV}$, two

to three magnitudes higher than the number at Si/SiO₂ interface. In GaN MISH system, the dielectric/AlGaN interface plays an important role on realization of MIS-HEMT. In the following section, we characterized Al₂O₃/AlGaN interface and investigated the impact on Al₂O₃/AlGaN interface state density due to different processes and treatments.

3.2 Characterization setups

The capacitance voltage (C-V) technique is the most popular method for interface states characterization. This technique allows a fast test and facilitates the fabrication process for the test device since it can be performed on a simple diode structure. The MISH structure we introduced in chapter two was designed for the C-V characterization. Besides the interface state density, C-V curves can provide other information such as carrier density profiles and dielectric constant. A detail theory and interpretation of C-V curves in MISH system is explained in next section.

Agilent 4284A LCR meter and Boonton 72B capacitance meter were both used in our C-V characterization. The sweeping rate was set at 100 mV/s. The test frequency was varied from 100 Hz to 1MHz. Multi-frequency C-V was used to extract interface state densities. Samples were tested on MMR probe station.

3.3 Capacitance-voltage characterization

3.3.1 Theory and interpretation

Because there exist $\text{Al}_2\text{O}_3/\text{AlGaN}$ and AlGaN/GaN two interfaces in the MISH diode, the C-V curves are significantly different from conventional C-V curves in silicon MOS caps. Figure 3-1 shows a general voltage sweep of the MISH diode from negative bias to positive bias. It can be noticed that there are three stages presenting in this curve. At the beginning of the sweep, almost no capacitance can be measured. At this stage 1, the 2DEG is depleted below the threshold voltage. As the gate voltage swept above the threshold condition, the 2DEG starts to accumulate at AlGaN/GaN interface. Then we obtain a constant capacitance which equals to the capacitance of the AlGaN layer in series with the Al_2O_3 layer. The capacitance curve keeps flat at stage 2 until the sweep reaches a high positive gate bias at which electrons at AlGaN/GaN interface partially transfer to $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface. The slope during this transition looks less steep than the one from stage 1 to stage 2, which indicates a higher density of states at $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface. At stage 3, electrons accumulate at $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface and the capacitance value corresponds to the capacitance of the Al_2O_3 layer.

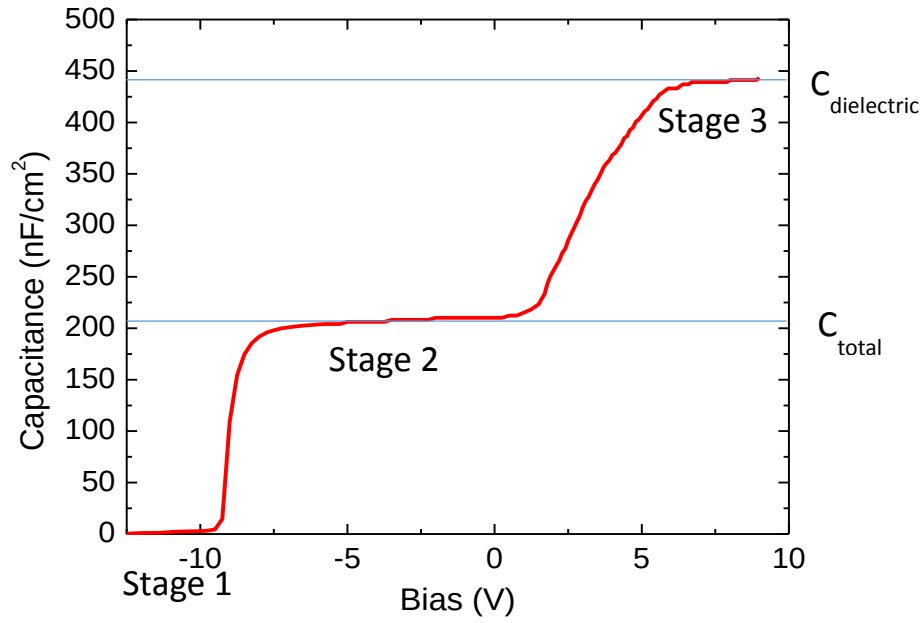


Figure 3-1 A typical capacitance-voltage sweep curve of MISH diodes.
There are three stages along the sweeping voltage.

3.3.2 Dielectric constant

This simple curve also provides us other information of the materials and capacitors. From figure 3-2, the dielectric constant of the Al_2O_3 film and AlGaIn film can be calculated using the following equations:

Al_2O_3 dielectric constant is:

$$\epsilon_r = \frac{C_{\text{dielectric}} \cdot t}{\epsilon_0}$$

where t is the film thickness, and $C_{\text{dielectric}}$ is the dielectric capacitance per unit area and can be read from the C-V curve in stage 3.

Then according to the equation of parallel capacitor:

$$C_{total} = \frac{C_{AlGaN} \cdot C_{dielectric}}{C_{AlGaN} + C_{dielectric}}$$

where the total capacitance C_{total} is shown in stage 2

The capacitance of AlGaN is

$$C_{AlGaN} = \frac{C_{total} \cdot C_{dielectric}}{C_{dielectric} - C_{total}}$$

AlGaN dielectric constant can be calculated by:

$$\epsilon_{rAlGaN} = \frac{C_{AlGaN} \cdot t_{AlGaN}}{\epsilon_0}$$

3.3.3 Carrier profile

We also need the C-V profile to study electrons confinement at AlGaN/GaN heterointerface. The distribution of electrons can be extracted from C-V curve at stage 2.

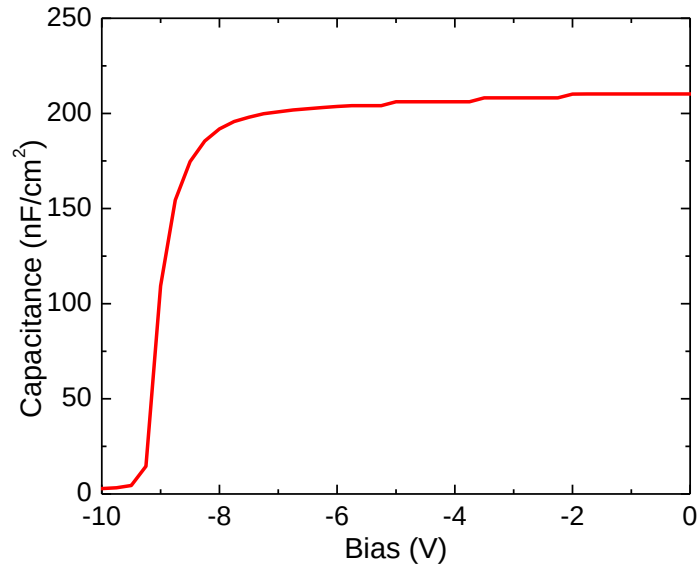


Figure 3-2 C-V curve of MISH diodes at negative bias.

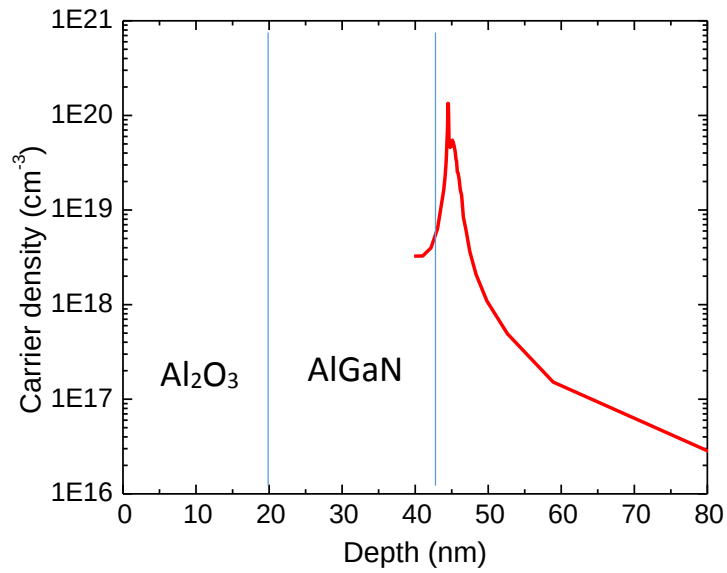


Figure 3-3 Carrier density profile of MISH diodes along the vertical direction.

The depth is the distance from the deposited Al_2O_3 surface.

By applying the equation:

$$N = \frac{C^3}{q\epsilon_r\epsilon_0} \cdot \frac{dV}{dC}$$

We can acquire the number of carrier concentration. And the depth can be calculated by

$$x = \frac{\epsilon_r\epsilon_0}{C}$$

By plotting the carrier concentration as a function of depth, we can obtain figure 3-3. This figure shows a good confinement of 2DEG within ~5 nm near the heterointerface.

If we want to know the sheet carrier density, we can integrate the carrier concentration along z direction by:

$$n_s = \int_0^{\infty} N(x)dx$$

This technique is very simple and useful to determine sheet carrier density at the interface [1]. Comparing the calculated value with sheet density value obtained from Hall effect measurement, we found them in a good consistency.

Table 3-1 Comparison of 2DEG density measured from Hall system and calculated from C-V curve.

Dielectric	Hall (cm ⁻²)	C-V (cm ⁻²)
Al ₂ O ₃	1.06×10 ¹³	1.07×10 ¹³

3.4 C-V characterization of interface states density

One of the most important application for C-V measurements is to extract the interface state density information. We first start with a single measurement. Figure 3-4 shows a typical C-V curve of Al₂O₃/AlGa_N/Ga_N MISH capacitors in which the Al₂O₃ film is grown by PEALD. The gate bias was swept from -4 to 4V at 10 KHz. The 2DEG is first depleted as the capacitance is close to zero. At $V_g = -3V$, electrons start to accumulate at AlGa_N/Ga_N 2DEG channel, and the capacitance increases until reaching a constant value equal to the capacitance of the dielectric layer in series with the AlGa_N layer. As the sweeping voltage increases to 2V, the capacitance increases again, as electrons gradually transfer to dielectric/AlGa_N interface. We can divide interface states at Al₂O₃/AlGa_N into three categories: fixed charges, slow traps and fast traps. Fixed charges are located in deep energy states. They shift 2DEG threshold voltage. Fast traps can follow the C-V sweep. Their energy levels are much closer to conduction band. Slow traps stay in between the fixed charges and fast traps. They cannot follow AC signal but can respond to DC signal in the C-V. By applying different C-V techniques, we can distinguish these three types of interface states [2], [3].

The fixed charge at Al₂O₃/AlGa_N interface shifts the threshold voltage of 2DEG accumulation. The equation is shown below,

$$n = \frac{C_{Al_2O_3}}{q\Delta E} (V_{th} - V_{th(ideal)})$$

where

$$V_{th(ideal)} = \frac{qn_{Hall}}{C_{total}}$$

The fixed charge density is calculated by the difference between the real V_{th} and the ideal V_{th} , which can be calculated from the measured 2DEG density at AlGaIn/GaN interface. We substitute the sheet charge density measured in Hall measurement and the capacitance in accumulation stage in figure 3-4, and obtained a $V_{th(ideal)} \sim -6V$. The real V_{th} is defined as the voltage at the capacitance equal to 90% of total capacitance can be read from the C-V curve. Here we choose ΔE as the energy range that cannot respond to either AC or DC C-V signal, which is from the valence band to the lowest energy level in slow traps. The energy level will be discussed below in multi-frequency measurements. Therefore, fixed charge density can be estimated $\sim 7 \times 10^{12}/cm^2 eV$.

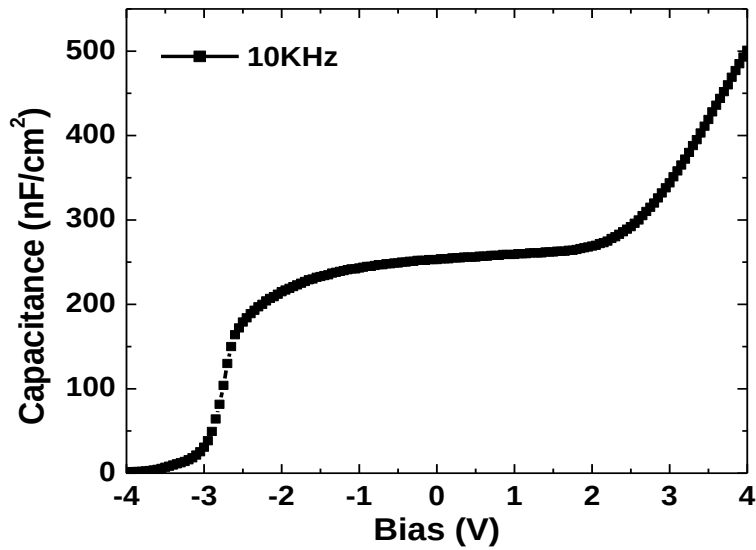


Figure 3-4 C-V characteristic of MISH diodes at 10 KHz.

The C-V hysteresis measurement was used to study slow trap densities. As stated before, electrons at these states cannot follow AC signal but can follow DC bias voltage change. In figure 3-5, a forward sweep from -4 V to 4 V was performed and followed by a reverse sweep back to -4 V.

The entire C-V curve is shifted after a reverse sweep. The interface state density can be calculated from equation

$$D_{it} = \frac{C_{Al_2O_3} \Delta V}{q \Delta E}$$

where

$$\Delta E = kT \ln\left(\frac{f_1}{f_2}\right)$$

and the corresponding signal period is between DC sweep rate and the entire sweep time, from 0.1s to 100s. The detail calculation of ΔE is given in next section. And the slow trap density is found around $2.2 \times 10^{13}/\text{cm}^2\text{eV}$ at the band range from $E_c - 0.6\text{eV}$ to $E_c - 0.42\text{eV}$.

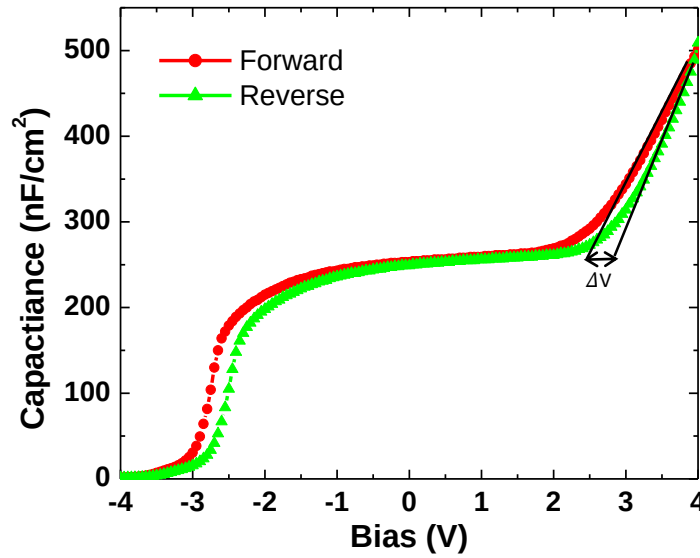


Figure 3-5 C-V hysteresis characteristic of the MISH diode swept from -4V to 4V, and back to -4V at 10KHz. The voltage difference is also extracted to calculate the deep level interface state density.

3.5 Multi-frequency C-V for interface states

The multi-frequency C-V characterization was carried to investigate fast traps located near the conduction band. C-V curves with three different frequencies (1KHz, 10KHz and 100KHz) are plotted in Figure 3-6. A frequency dispersion is observed at positive voltage since traps with a certain emission constant can only respond to a slow test signal. We may use Shockley Read Hall

model to explain this behavior. The emission constant τ can be expressed by $\tau = \frac{1}{\sigma v_{th} N_t} = \frac{1}{\sigma v_{th} N_c} \exp(\frac{E_t}{kT})$, assuming E_t is the energy difference from the defect state to the conduction band.

The emission constant has to be smaller than the test signal so that electrons at traps can follow the small signal and therefore can contribute to capacitance increase at positive bias.

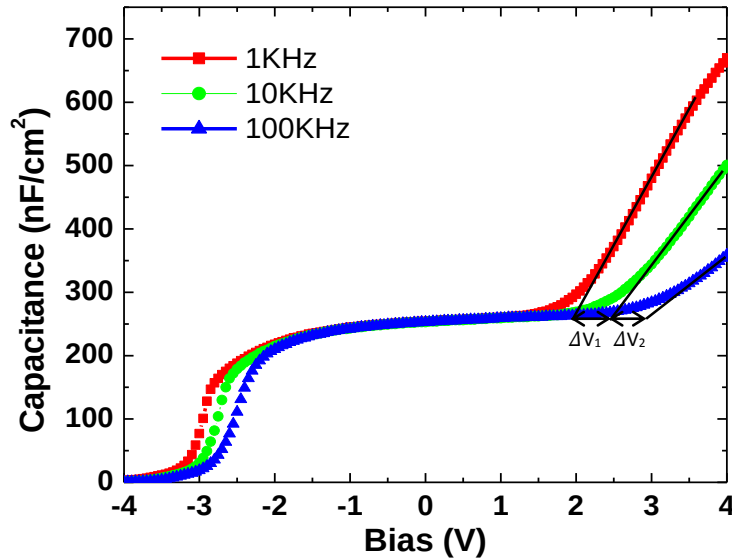


Figure 3-6 Multi-frequency C-V characteristic of the MISH capacitor with forward sweep from -4V to 4V at 1KHz, 10KHz and 100KHz. The solid lines are plotted to extract the onset voltage for the charge transfer process.

In figure 3-6, low frequency C-V and high frequency C-V correspond to high and low test signals, since $f \sim \frac{1}{\tau}$. Relating them to τ expression, we can find $f \sim \exp\left(-\frac{E_t}{kT}\right)$. It means that traps in deep states with larger activation energy (larger E_t) can only follow low frequency while not high frequency. In figure 3-7, E_t difference at two measurement frequency can be written as:

$$\Delta E = kT \ln\left(\frac{f_1}{f_2}\right)$$

and the trap density can be obtained by:

$$D_{it} = \frac{C_{Al_2O_3} \Delta V}{q \Delta E}$$

where ΔV is the difference between voltages at the onset of capacitance increase and can be read from figure 3-6. It corresponds to the voltage at which electrons at traps start to communicate with the conduction band. Then an average trap density of $4.6 \times 10^{13}/\text{cm}^2\text{eV}$ can be acquired within the energy level from $E_c - 0.3\text{eV}$ to $E_c - 0.18\text{eV}$.

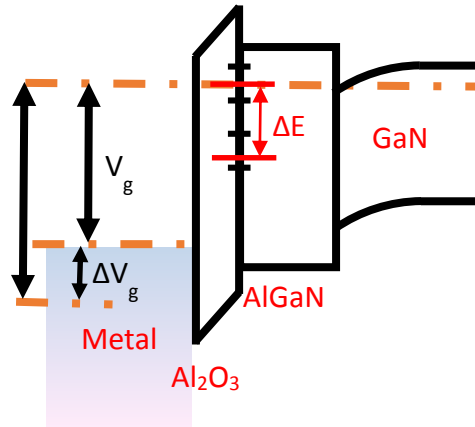


Figure 3-7 Schematic band diagram of the $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ MISH capacitor that illustrates ΔE and ΔV at different C-V test frequencies.

Table 3-2 summarizes the density of three types of defects at Al₂O₃/AlGaN interface. As the defect energy level approaches to midgap, the density of the defect reduces.

Table 3-2 Al₂O₃/AlGaN interface defect densities in the PEALD MISH diode.

Defect type	Defect density (cm ⁻² eV ⁻¹)
Fixed charge	7×10^{12}
Slow trap	2.2×10^{13}
Fast trap	4.6×10^{13}

3.6 Effects of thermal ALD and PEALD Al₂O₃ thin films

Multiple ALD growth techniques have been developed to deposit Al₂O₃ films. Among them, two of the most frequently used methods are thermal ALD and plasma enhanced ALD. Both of them involve TMA as aluminum precursor, but the oxidizing agent are different. Thermal ALD uses H₂O vapor while PEALD uses plasma O₂. We have already compared their film qualities from the material perspective. When we fabricate our device structures with these films, it is also necessary to investigate their electrical properties and understand the difference of interfacial properties resulting from these dielectrics.

Some reports have already studied the influences from different technique grown films on silicon MOS capacitors [4]. The films were grown by O₃, H₂O and O₂ oxidants and all the samples were annealed at three different temperature conditions. The C-V curves of the three films show obvious discrepancy, indicating the enormous difference in interface state densities. The annealing treatments after three types of growth techniques also had different impacts on interfacial properties. In this section we discuss influences of thermal ALD and PEALD growth techniques

on $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISH C-V curves and $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states, and in following sections we focus on various effects of pre-treatments and post annealing treatments on MISH devices.

Two samples with similar $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISH structure and processes were fabricated in this study except that Al_2O_3 films were deposited by thermal ALD and PEALD, respectively. These samples went through a same testing procedure and C-V measurements were performed on them.

Figure 3-8 shows C-V curves of these two ALD grown samples at 10KHz frequency. From this graph a clear discrepancy of these two curves can be observed. The 2DEG threshold voltage of the thermal ALD sample is much more negative. Also the capacitance at stage 2 of the thermal ALD sample is slightly lower than the one in the PEALD sample. In addition, even though the measurements were performed at same frequency, the C-V curve for the thermal ALD sample is less steep at the transition from stage 2 to stage 3 and the capacitance is much lower. The sweep for the thermal ALD sample has to stop at 3.5V since the sample shows the early breakdown behavior at less than 4V.

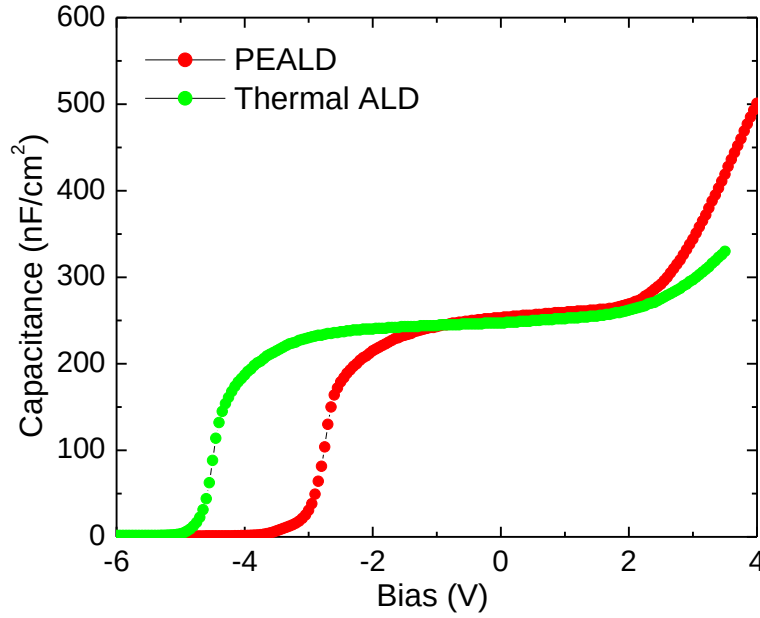


Figure 3-8 C-V profiles of MISH diodes with thermal ALD Al₂O₃ thin film and PEALD Al₂O₃ thin film.

Figure 3-9 (a) shows a close look of the C-V curves from stage 1 to stage 2 and figure 3-9 (b) shows the C-V from stage 2 to stage 3. According to previous analysis and equation, the fixed charge densities of these two films have a significant difference. Still using equations below:

$$n = \frac{C_{Al_2O_3}}{q\Delta E} (V_{th} - V_{th(ideal)})$$

where

$$V_{th(ideal)} = \frac{qn_{Hall}}{C_{Al_2O_3//AlGaIn}}$$

Then we can obtain the fixed charge density at thermal $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. Notice that the negative fixed charge in the PEALD sample is larger than the one in the thermal ALD sample with same Al_2O_3 film thickness. Since the Al_2O_3 film itself exhibits negative interfacial fixed charges and positive bulk fixed charges as its intrinsic property, the larger density of fixed charges in the PEALD sample indicates the denser and better quality film with low positive fixed charges. The explanation can probably be that the use of thermal energy in thermal ALD does not fully activate the oxidant so that the precursor is not completely reacted, and therefore unreacted precursor may still exist in the thermal ALD film. On the other hand, PEALD provides plasma O_2 with enough energy to thoroughly oxidized TMA precursor, and a purer Al_2O_3 film is obtained. The number of fixed charges also plays a critical role on determining the threshold voltage of the device. The negative fixed charge results in a positive shift of the threshold voltage. The PEALD sample enables a threshold voltage that closer to the positive, and that might be beneficial to the development of the enhancement mode transistor that currently is still a big challenge.

At stage 2, dielectric constant of the Al_2O_3 film can be calculated through the capacitance. The lower K value of the thermal ALD Al_2O_3 film also confirms the less dense film compared to the PEALD film.

From the previous interpretation of the C-V curve, we can estimate the interface state density through the slope and voltage difference at the transition from stage 2 to 3. The steeper curve for the PEALD sample indicates a better interface and a lower density. Since we have obtained the fast trap density for PEALD grown samples from previous calculation, the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ fast trap density for thermal ALD samples can be also calculated by the same equation using multi-frequency C-V:

$$\Delta E = kT \ln\left(\frac{f_1}{f_2}\right)$$

$$D_{it} = \frac{C_{Al_2O_3} \Delta V}{q \Delta E}$$

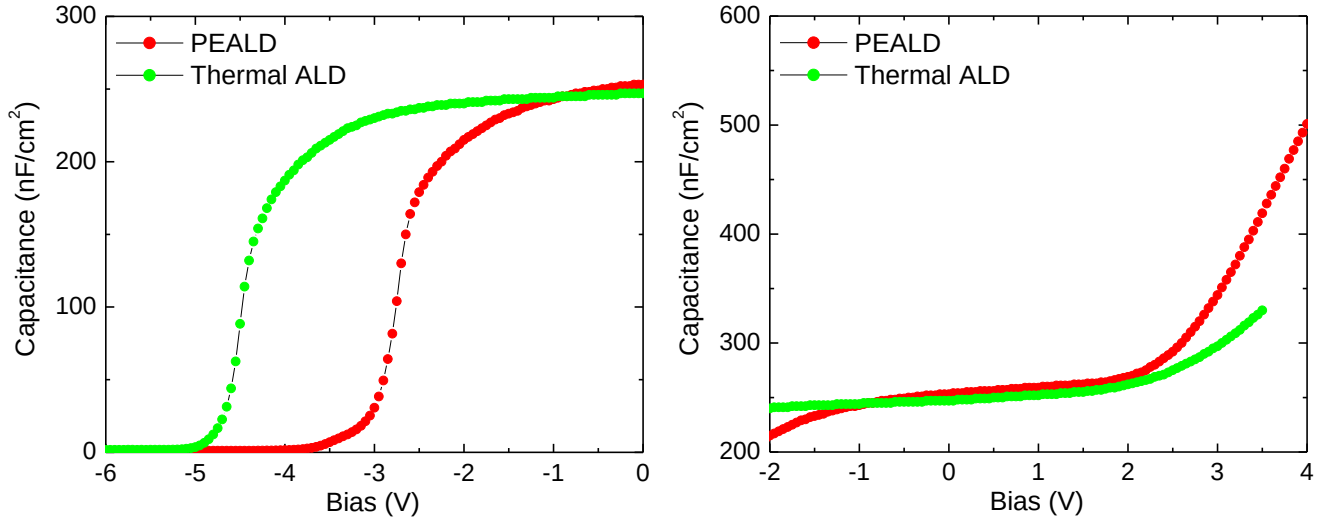


Figure 3-9 C-V profile of (a) 2DEG depletion to accumulation region and (b) 2DEG transfer from AlGaN/GaN to Al₂O₃/AlGaN interface region.

We further carried out a C-V hysteresis measurement for the thermal ALD sample. Using the same calculation as shown in previous section, we can get the slow trap density. Combining all three types of defects, table 3-3 summarizes a comparison of the interface state density for the thermal ALD and PEALD Al₂O₃/AlGaN/GaN MISH structures. From this table, we can conclude that the PEALD sample has less traps but more fixed charges than the thermal ALD sample. Since normal transistor operation is mainly affected by the number interface states and traps, the PEALD Al₂O₃/AlGaN/GaN structure might offer a better device performance and reliability.

Table 3-3 Comparison of Al₂O₃/AlGaN interface defect densities in thermal ALD and PEALD MISH diodes.

Defect type	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)
	PEALD	Thermal ALD
Fixed charge	7×10^{12}	4.1×10^{12}
Slow trap	2.2×10^{13}	3.6×10^{13}
Fast trap	4.6×10^{13}	6.8×10^{13}

Another interesting point can be raised if we plot the capacitance in a logarithm scale versus the voltage bias in figure 3-10. Notice that the thermal ALD curve has a larger capacitance tail at stage 1 that corresponds to the off channel and 2DEG depletion. This is an indication that more electrons and leakage exist in this region for the thermal ALD sample. In terms of the device performance, we can probably translate this phenomenon into a larger subthreshold leakage and worse off-state behavior in thermal ALD grown transistors.

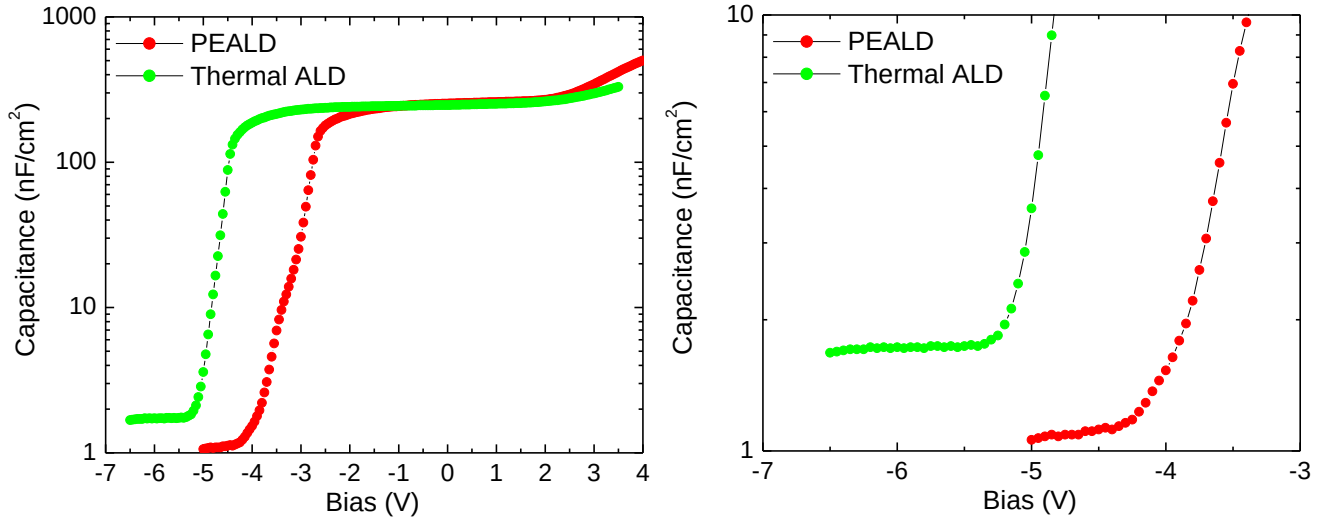


Figure 3-10 Logarithm scale C-V profiles of two types of MISH diodes (a) along the entire voltage sweep range and (b) at stage 1.

3.7 Effects of pre-deposition surface treatments

It is believed that the surface treatment prior to dielectric deposition might have a positive effect on dielectric/semiconductor interfacial properties. The plasma technology has been extensively utilized in semiconductor industry. The implementation of the plasma process into surface treatment results from its various functions. First, energetic plasma species either chemically react with surface contaminants or physically break impurity bonds so that organic and other impurity contents reduce due to their dissociation with surface. The plasma may also react with surface atoms and form a thin interfacial layer. This layer may change the surface functional group and therefore benefit subsequent growth. Either usage can provide a cleaner surface and improve interfacial properties [5]. In our research, several plasma surface treatment methods were

investigated and improvements of $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface were observed. Figure 3-11 compares the C-V profiles of three types of MISH diodes with plasma N_2 , plasma NH_3 treatment and without treatment. The sample under N_2 treatment has the steepest slope at the transition region. The NH_3 treatment sample is also slightly better than the one without surface treatment. The detail analysis is given below.

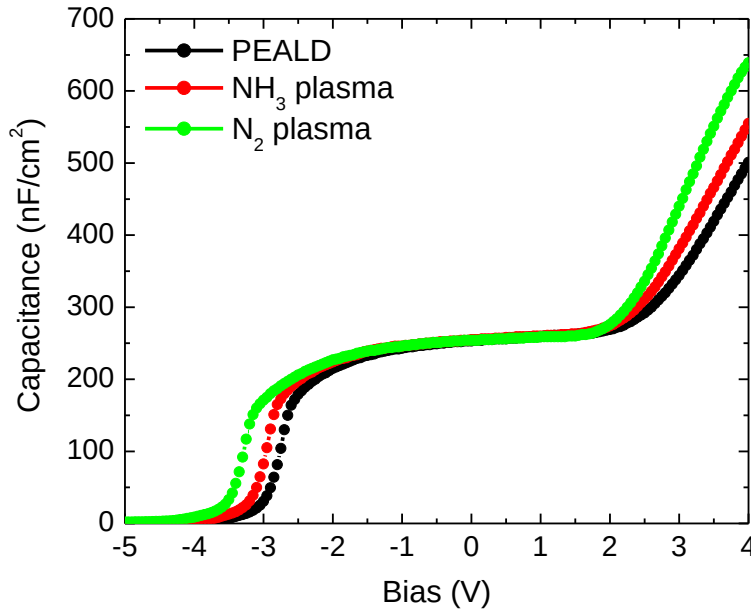


Figure 3-11 C-V profiles comparison of MISH diodes with NH_3 pre-deposition treatment, N_2 pre-deposition treatment and without treatment.

3.7.1 Plasma N_2

The MISH diode was fabricated using standard process, except that a 10 minutes plasma nitrogen treatment was applied to AlGaIn surface prior to Al_2O_3 deposition. C-V techniques described above were performed on samples with and without treatments to compare the treatment effects.

Table 3-4 shows the defect state densities with 50W, 100W plasma N₂ treatment and without any treatment.

Table 3-4 Comparison of Al₂O₃/AlGaIn interface defect densities in MISH diodes with different N₂ plasma power.

Defect type	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)
	Non-treatment	50W	100W
Fixed charge	7×10^{12}	4.5×10^{12}	5.6×10^{12}
Slow trap	2.2×10^{13}	5.2×10^{12}	9.1×10^{12}
Fast trap	4.6×10^{13}	8.6×10^{12}	1.6×10^{13}

From the table above it can be summarized that the diodes with 50W and 100W plasma N₂ surface treatments both have better interfacial properties than the one without treatment. The explanation for these results can be described as following: The plasma nitrogen radicals can react with surface impurities such as native oxides and carbon so the number of defects can be reduced. In addition, by replacing these impurities on the surface, nitrogen atoms can be bonding with underneath gallium atoms, and therefore form a surface nitridation layer on AlGaIn. The nitridation layer can prevent Ga-O bonds formation during the ALD growth. The XPS characterization in last chapter also suggests less Ga-O bonds existing after surface treatment. The reduction of Ga-O bonds minimizes the interface state density and improves the Al₂O₃/AlGaIn interfacial properties.

Comparing with the 50W plasma treatment sample, the 100W plasma sample has a higher interface state density. The possible reason for the higher trap density can be due to stronger ion

bombardments at high power that lead to the damage of surface stoichiometry. Energetic nitrogen ions break Ga-N and Al-N bonds and create traps at AlGaN surface.

3.7.2 Plasma NH₃

The effects of plasma NH₃ treatment was also investigated. Similar processes were applied to MISH diodes fabrication and a 10 minutes NH₃ treatment was employed before ALD. Table 3-5 compares the interface state densities with different treatment power.

The NH₃ plasma treatment has similar effects as the N₂ plasma treatment. As other studies also suggested, the nitrogen based plasma treatments are able to recover N-vacancy related defects. NH₃ may bring particular benefits because the hydrogen inside can passivate not only surface dangling bonds but bulk defects in GaN as well [6]. In our study, the effectiveness of the NH₃ plasma treatment is not as good as the N₂ treatment, which confirms our XPS study on GaO_x/GaN ratio. Other report shows that NH₃ is not sufficient to remove native oxides on GaN by nature [7].

Table 3-5 Comparison of Al₂O₃/AlGaN interface defect densities in MISH diodes with different NH₃ plasma power.

Defect type	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)
	Non-treatment	50W	100W
Fixed charge	7×10 ¹²	6.4×10 ¹²	6.2×10 ¹²
Slow trap	2.2×10 ¹³	9.7×10 ¹²	1.1×10 ¹³
Fast trap	4.6×10 ¹³	2×10 ¹³	1.9×10 ¹³

3.8 Effects of post-deposition annealing

We have studied and characterized the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface and the post annealing effects on interface states to better understand the relative importance of these issues. The Al_2O_3 layer was deposited by atomic layer deposition in Savannah thermal ALD system. Trimethylaluminum and water vapor were used as the Al and O sources for the Al_2O_3 films. The samples then underwent post deposition annealing at 400 °C, 500 °C and 600 °C for 5 minute in nitrogen atmosphere, respectively. Non-annealed $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ structure was also fabricated for comparison.

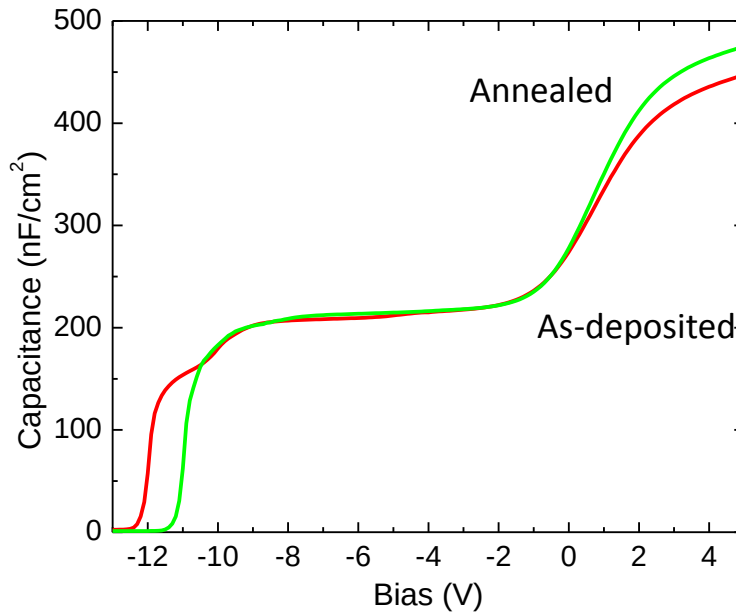


Figure 3-12 C-V profiles comparison of MISH diodes with and without post-deposition annealing.

C-V curves of non-annealed sample and annealed sample are compared. The threshold voltage of the annealed sample shifts toward the positive side, which shows a reduction of positive fixed charges. The positive fixed charge here represents the net fixed charge in both bulk Al_2O_3 film and

at $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. The bulk Al_2O_3 fixed charge was found carrying positive charges [8]. In this ALD system, the number of the positive fixed charges in bulk films exceeds the negative charges at the interface so that the net fixed charge density is positive. We can also find the elimination of ledges at the 2DEG onset. This probably indicates the local defect reduction by the annealing and the recovery of dangling bonds. The higher capacitance at positive voltage shows more electrons accumulated at $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface due to less trapped electrons at interface states.

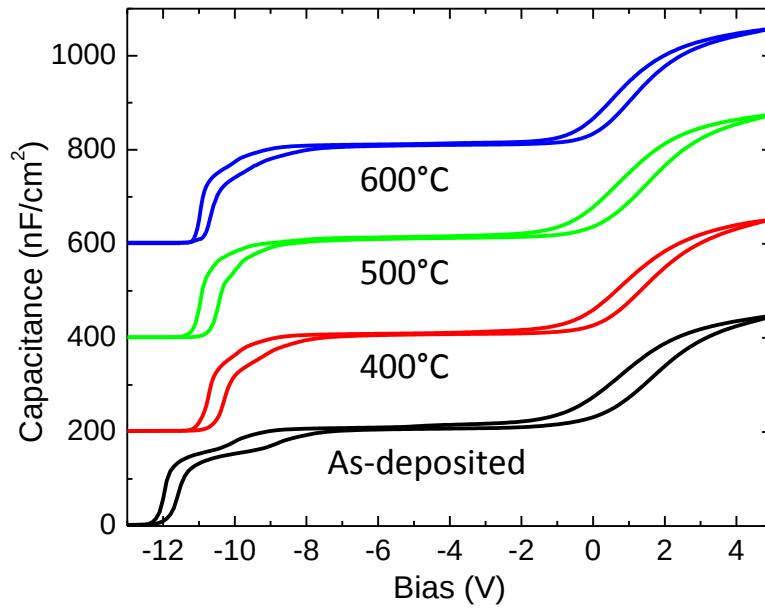


Figure 3-13 Forward and backward C-V sweep of MISH diodes with 400°C, 500°C, 600°C 5 minutes post-deposition annealing and without post-deposition annealing.

C-V hysteresis curves (shown in figure 3-13) and multiple frequency C-V profile (not shown here) also suggest that the trap densities of annealed samples are much lower than non-annealed samples. The calculated defect densities of samples with different annealing conditions is listed in table 3-

6. It is approximately shown that the 600 °C 5 minutes annealed sample has the lowest defect density.

Table 3-6 Comparison of Al₂O₃/AlGaIn interface defect densities in MISH diodes with different post annealing temperature.

Defect type	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)	Defect density (cm ⁻² eV ⁻¹)
	As-deposited	400°C	500°C	600°C
Fixed charge	4.2×10 ¹²	3.2×10 ¹²	3.4×10 ¹²	3.4×10 ¹²
Slow trap	4.9×10 ¹³	3.5×10 ¹³	3.8×10 ¹³	2.7×10 ¹³
Fast trap	1×10 ¹⁴	7.3×10 ¹³	7.2×10 ¹³	5.3×10 ¹³

3.9 References

- [1] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy and J. Hilsenbeck, “Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaIn/GaN heterostructures,” J. Appl. Phys., vol. 85, no. 6, pp. 3222-3233, 1999.
- [2] J. Wu; X. Lu; S. Ye; J. Park; D. C. Streit, “Electrical characterization and reliability analysis of Al₂O₃/AlGaIn/GaN MISH structure,” Proc. Int. Rel. Phys. Symp., pp.CD.6.1-CD.6.5, 2014.
- [3] Y. Hori, Z. Yatabe and T. Hashizume, “Characterization of interface states in Al₂O₃/AlGaIn/GaN structures for improved performance of high-electron-mobility transistors,” J. Appl. Phys., vol. 114, pp. 244503, 2013.
- [4] D. Suh, W. S. Liang, “Electrical properties of atomic layer deposited Al₂O₃ with anneal temperature for surface passivation,” Thin Solid Films, Vol. 539, pp. 309-316, 2013.
- [5] S. Yang, Z. Tang, K. Y. Wong, Y. S. Lin, C. Liu, Y. Lu and K. J. Chen, “High-Quality Interface in Al₂O₃/GaN/AlGaIn/GaN MIS Structures With In Situ Pre-Gate Plasma Nitridation,” IEEE Electron Device Lett., vol. 34, no. 12, pp. 1497-1499, 2013.
- [6] A. Hierro, S. A. Ringel, M. Hansen, J. S. Speck, U. K. Mishra, and S. P. DenBaars, “Hydrogen passivation of deep levels in n-GaN,” Appl. Phys. Lett., vol. 77, no. 10, pp. 1499–1501, 2000.

- [7] L.C. Grabow, J.J. Uhlrich, T.F. Kuech and M. Mavrikakis, "Effectiveness of in situ NH_3 annealing treatments for the removal of oxygen from GaN surfaces," *Surf. Sci.*, vol. 603, no. 2, pp. 387-399, 2009.
- [8] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle and P. C. McIntyre, "Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate insulators on chemically treated InGaAs substrates," *Appl. Phys. Lett.*, vol. 96, no. 15, pp. 152908, 2010.

Chapter 4 Dielectric conduction and reliability

One of the most important reason for introducing dielectric layer into GaN heterostructure is to suppress gate leakage current during device operation. The dielectric material should have good insulating properties so that electrons in the channel cannot transport to gate terminal. Therefore, it is necessary to study carrier transport properties for our Al_2O_3 films. In this chapter, current voltage (I-V) tests were carried out on the MISH diodes and the temperature dependence of I-V curves were analyzed.

4.1 Dielectric conduction mechanisms

Dielectric conduction properties have been well studied in silicon industry due to the need of thinner dielectric films and the development of high K dielectric materials in both logic and memory application. In table 4-1, several common current transport mechanisms are summarized [1]. It should be noticed that most of these processes involve the temperature and voltage variables.

Table 4-1 Dielectric conduction mechanisms

Process	Expression	Voltage & temperature dependence
Tunneling	$J \propto \mathcal{E}_i^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\mathcal{E}_i}\right]$	$\propto V^2 \exp\left(\frac{-b}{V}\right)$
Thermionic emission	$J = A^{**}T^2 \exp\left[\frac{-q(\phi_B - \sqrt{q\mathcal{E}_i/4\pi\epsilon_i})}{kT}\right]$	$\propto T^2 \exp\left[\frac{q}{kT}(a\sqrt{V} - \phi_B)\right]$
Frenkel-Poole emission	$J \propto \mathcal{E}_i \exp\left[\frac{-q(\phi_B - \sqrt{q\mathcal{E}_i/\pi\epsilon_i})}{kT}\right]$	$\propto V \exp\left[\frac{q}{kT}(2a\sqrt{V} - \phi_B)\right]$
Ohmic	$J \propto \mathcal{E}_i \exp\left(\frac{-\Delta E_{ac}}{kT}\right)$	$\propto V \exp\left(\frac{-c}{T}\right)$
Ionic conduction	$J \propto \frac{\mathcal{E}_i}{T} \exp\left(\frac{-\Delta E_{ai}}{kT}\right)$	$\propto \frac{V}{T} \exp\left(\frac{-d'}{T}\right)$
Space-charge-limited	$J = \frac{9\epsilon_i\mu V^2}{8d^3}$	$\propto V^2$

A^{**} = effective Richardson constant. ϕ_B = barrier height. $\mathcal{E}_i$ = electric field in insulator. ϵ_i = insulator permittivity. m^* = effective mass. d = insulator thickness. ΔE_{ac} = activation energy of electrons. ΔE_{ai} = activation energy of ions. $V \approx \mathcal{E}_i d$. $a \equiv \sqrt{q/4\pi\epsilon_i}$. b , c , and d' are constants.

As dielectric thickness reduces, quantum mechanical tunneling becomes more and more significant. This quantum process involves the penetration of electron wave through dielectric potential barrier and shows a strong field dependence. The tunneling behavior can be separated into three categories: direct tunneling, Fowler-Nordheim tunneling and trap assisted tunneling.

Direct tunneling occurs in thin dielectric films (usually less than 5 nm). This type of tunneling does not require a high electric field. The tunneling current can increase exponentially when dielectric thickness decreases. As oxide thickness scales down, high K dielectric materials have to be developed to prevent excessive gate current leakage which affects the circuit operation. The expression of direct tunneling current is:

$$J \propto E_{ox}^2 \exp\left[-\frac{4\sqrt{2m_{ox}^*}(q\phi_B)^{\frac{3}{2}}\left(1 - \left(1 - \frac{V_{ox}}{\phi_B}\right)^{\frac{3}{2}}\right)}{3q\hbar E_{ox}}\right]$$

where E_{ox} is the oxide electric field, m_{ox} is the oxide average electron mass, Φ_B is the potential barrier height between metal and dielectric conduction band, q is electron charge and $\hbar$ is Planck constant divided by 2π .

Fowler-Nordheim tunneling is a special type of direct tunneling as electrons only tunnel through the top triangular potential barrier of the dielectric film. This type of tunneling usually occurs in thicker dielectric film and requires a high enough electric field in the dielectric. The Wentzel-Kramers-Brillouin (WKB) approximation is often involved during the tunneling current calculation. The equation is listed as below:

$$J \propto E_{ox}^2 \exp\left[-\frac{4\sqrt{2m_{ox}^*}(q\phi_B)^{\frac{3}{2}}}{3q\hbar E_{ox}}\right]$$

Trap assisted tunneling is another tunneling process that electrons tunnel to semiconductor through assistance of trap states which result from pre-existing traps in the dielectric or bulk traps induced by electrical stress during device operation. This tunneling can happen at very low electrical field and the tunneling current will increase as more traps are created due to the stress. The equation for trap assisted tunneling is:

$$J \propto \exp\left[-\frac{4\sqrt{2m_{ox}^*}(q\phi_t)^{\frac{3}{2}}}{3q\hbar E_{ox}}\right]$$

Thermionic emission and Frenkel-Poole emission are two important transport mechanisms in dielectrics besides tunneling processes. Thermionic emission involves electrons jumping over the dielectric potential barrier and usually occurs at high temperature because of the need of enough

thermal energy. Frenkel-Poole emission, however, is strongly dependent of both temperature and electric field. This process requires thermal excitation of trapped electrons to dielectric conduction band.

Figure 4-1 describes four types of tunneling processes.

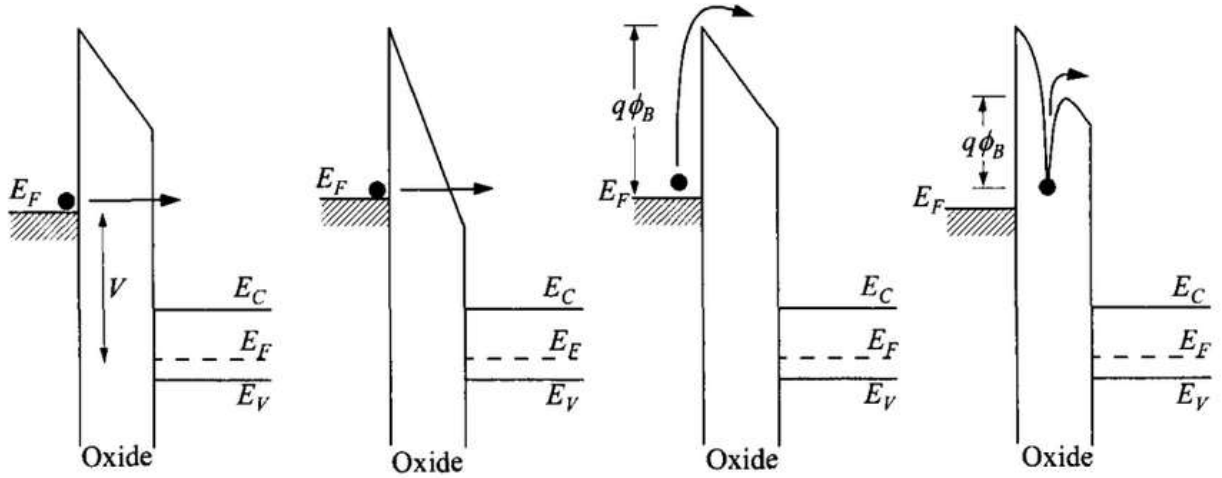


Figure 4-1 Schematic band diagram illustrating conduction mechanisms of (a) direct tunneling, (b) F-N tunneling, (c) thermionic emission and (d) F-P emission.

4.2 Gate conduction current of thermal ALD and PEALD Al_2O_3 thin films

MISH diodes with thermal ALD and PEALD grown Al_2O_3 films of 12 nm thickness were fabricated and characterized by I-V measurement. Schottky structure diodes without Al_2O_3 films were also fabricated and tested as comparison.

Figure 4-2 shows negative to positive I-V sweep on three diodes with thermal ALD, PEALD and without ALD process. We observe a significant reduction of gate leakage current in both thermal ALD and PEALD MISH structures compared to the schottky structure. It indicates that Al_2O_3 films can effectively suppress leakage current at a high voltage bias. Besides, PEALD Al_2O_3 film shows

better insulating property than thermal ALD Al_2O_3 film, since plasma process reacts with precursor more completely and provides a denser and better quality film [2].

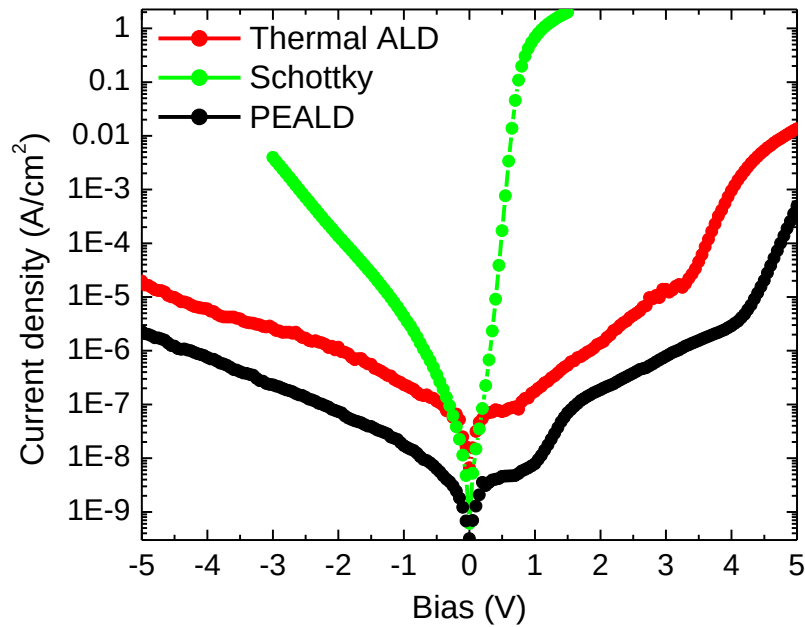


Figure 4-2 J-V characteristic of schottky diode and MISH diodes using thermal ALD and PEALD Al_2O_3 growth.

4.3 Effects of post deposition treatment

MISH diodes fabricated by PEALD Al_2O_3 film with 5 minutes 500°C N_2 post deposition annealing were studied by I-V measurement and compared to diodes without any post treatment.

It is shown that the device after N_2 annealing has a slightly increased leakage current. This could possibly be explained by decrease of Al_2O_3 film thickness after annealing. Reduction of tunneling distance may exponentially enhance tunneling current.

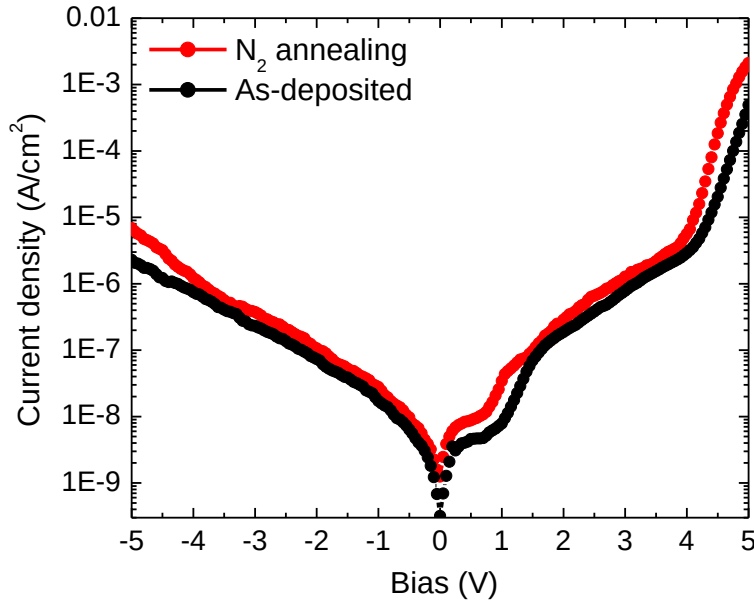


Figure 4-3 J-V characteristic of PEALD MISH diodes with and without N₂ post deposition annealing.

4.4 Temperature dependent I-V characterization

Gate current transport properties were investigated by I-V measurement from room temperature to 200°C. The result is shown in figure 4-4. There is a clear temperature dependence for current density starting from gate voltage $\sim 0.7V$. After $V_g = 2.4V$, current densities measured at different temperatures begin to converge and become less temperature dependent.

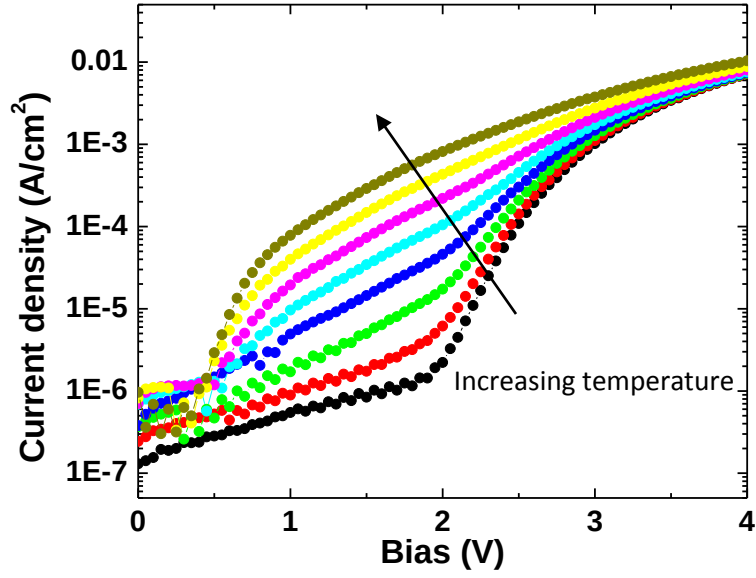


Figure 4-4 Forward J-V characteristics of MISH diodes from room temperature (25°C) to 200°C with a step temperature increase of 25°C.

To understand the actual gate current transport mechanism at different bias and temperature, we plot J/E vs $1000/T$ with different bias conditions in figure 4-5. We can observe three straight curves at low to medium voltage (1.2V-2V) regime, which can be fitted into Frenkel-Poole hopping model [3]:

$$J \propto E_{ox} \exp\left[-\frac{q}{kT}(\Phi_t - \sqrt{\frac{qE_{ox}}{\pi\epsilon_{ox}}})\right]$$

where $\Phi_t = 0.905\text{V}$ is extracted as a trap level in the oxide and $\epsilon_{rox} = 8.29$ is Al_2O_3 dielectric constant.

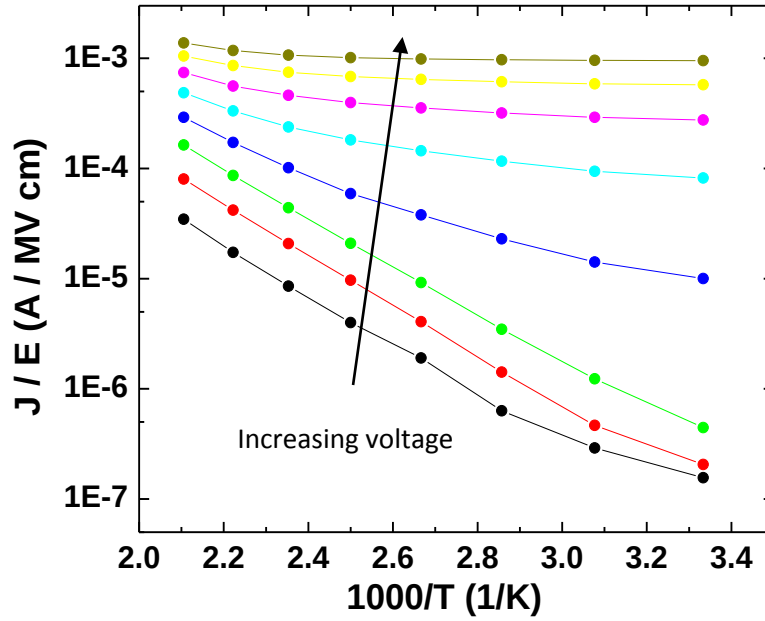


Figure 4-5 Temperature dependence of current at various voltages from 1.2V to 4V with a step voltage increase of 0.4V. The data follow F-P fits at low bias and show tunneling like behavior at high bias.

In medium to high voltage bias range, J/E vs $1/T$ curves deviate from straight lines, and eventually become flat at low temperature when the bias is above 3.2V. It indicates that another transport mechanism dominates in this range [4]. Since the current density no longer depends on temperature, it is likely that tunneling mechanism may take place in this high oxide field region.

Trap assisted tunneling (TAT) and Fowler-Nordheim tunneling (FNT) are two possible tunneling mechanisms [5] since the oxide field is relatively high and the oxide thickness is not too thin.

According to tunneling equations,

$$J \propto \exp\left[-\frac{4\sqrt{2m_{ox}^*}(q\phi_t)^{\frac{3}{2}}}{3q\hbar E_{ox}}\right]$$

and

$$J \propto E_{ox}^2 \exp\left[-\frac{4\sqrt{2m_{ox}^*}(q\phi_B)^{\frac{3}{2}}}{3q\hbar E_{ox}}\right]$$

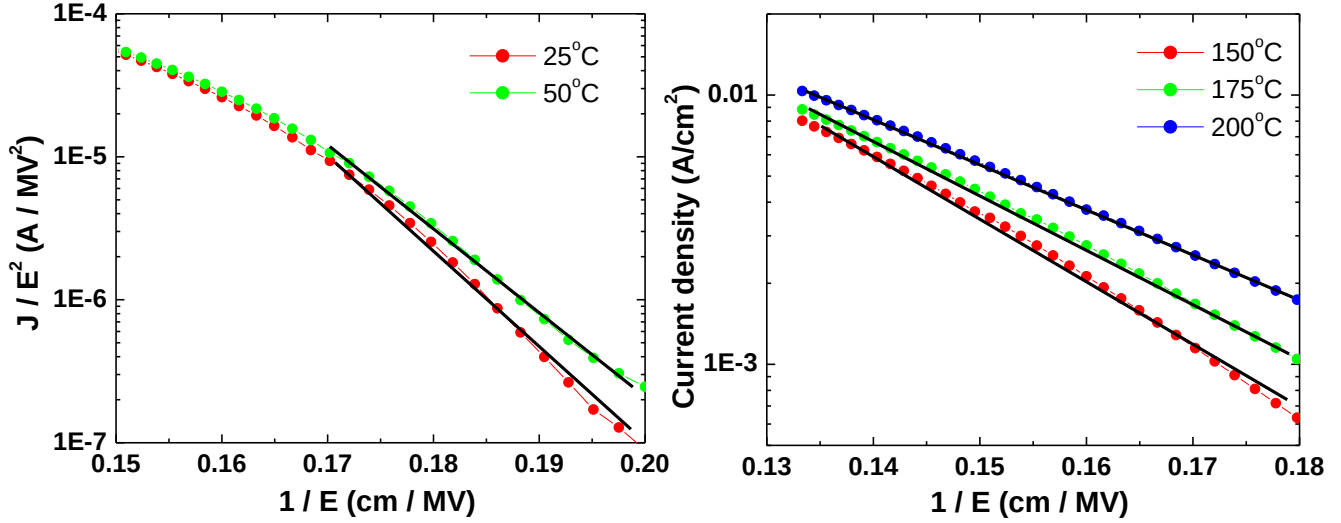


Figure 4-6 (a) Fowler Nordheim and (b) trap assisted tunneling plot of MISH diode at low and high temperature.

At low measurement temperatures (25°C and 50°C), we can fit our data with Fowler-Nordheim plot (J/E^2 vs $1/E$), assuming m_{ox}^* is an averaged electron tunneling mass $\sim 0.23m_0$ [6]. In the F-N plot, the dielectric barrier height Φ_B is extracted as ~ 2.6 - 2.9 eV, which is in agreement with our XPS data on $Al_2O_3/AlGaN$ barrier height. At high temperatures, however, the F-N fitting is no longer valid since the extracted barrier height is substantially lower than previous value. At high temperatures, we can fit our curves with TAT plot (J vs $1/E$), and trap states of ~ 1.1 - 1.2 eV can be extracted in our measurement temperature range. Therefore, we suggest that TAT may be dominant tunneling mechanism at high temperatures.

4.5 Dielectric reliability

Reliability of dielectric materials has become a more and more important issue as transistor dimensions and dielectric thickness scale down. When a gate voltage is applied to the dielectric, damage may happen in the dielectric and eventually an accumulative degradation leads to a dielectric breakdown [7]. The entire breakdown process can be separated to several stages. An early wearout is usually a long term event if the applied voltage is not high enough. In this stage, degradation increases slowly by trap generation and structural damage in the dielectric. If degradation induced defects are able to form a current conduction path along the dielectric, the current density suddenly increases by several order magnitude and short term breakdowns are triggered by local heating in the dielectric. The local temperature then reaches to dielectric melting point and permanent physical damage occurs in the dielectric.

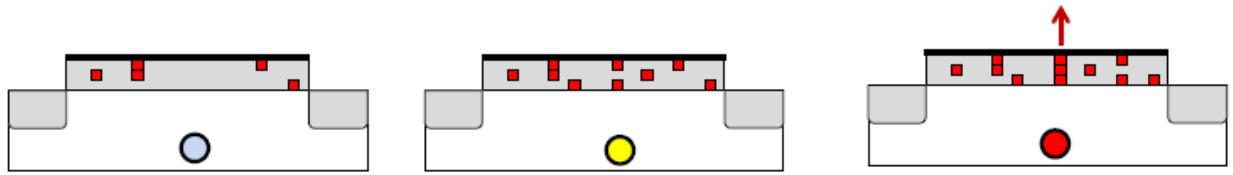


Figure 4-7 Dielectric breakdown processes after long term gate stress.

Dielectric reliability of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISH diode is essentially of great importance in GaN based high power transistors since devices might be operated in very critical conditions that need high voltage and high current levels. Unfortunately reliability studies of this system are very few up to now [8]. In our work, we absorbed several well developed reliability theories and evaluation methods from on Si/SiO_2 and $\text{Si}/\text{high K}$ systems and implemented them to our MISH structures.

4.6 Reliability test

4.6.1 Stress test

Stress test is the most common dielectric reliability test. Usually a constant current or a constant voltage stress is applied to the sample and the voltage or current shift is recorded as a function of time. The density of traps generated by stress can be calculated by $Q = C \cdot \Delta V$ in the constant current stress test.

In this work, the constant-current stress test was used to study Al_2O_3 film reliability. We performed gate current stress tests at three different levels and observed gate voltage shifts under stress. Figure 4-8 illustrates V_g variation as a function of time in these stress conditions. At low stress level, the V_g remains unchanged after an initial trap filling process that results from electrons falling into traps at the interface and the bulk oxide. This small voltage shift indicates a good V_{th} stability in this MIS structure. When the stress is increased to a high current density that corresponds to a high oxide field, the gate voltage begins to drop and voltage signal becomes noisy. This could probably be explained by a hole trapping process in the oxide film. These holes may come from impact ionization due to heavily injected electrons under high oxide field. And trapped holes increase the oxide electric field near the oxide/semiconductor interface. According to the equation for tunneling, an increased electric field will result in a higher tunneling current. In the case of constant-current test, the gate voltage should decrease to keep the current unchanged. At high stress levels, defect and trap generation becomes so severe that significant voltage drops are observed.

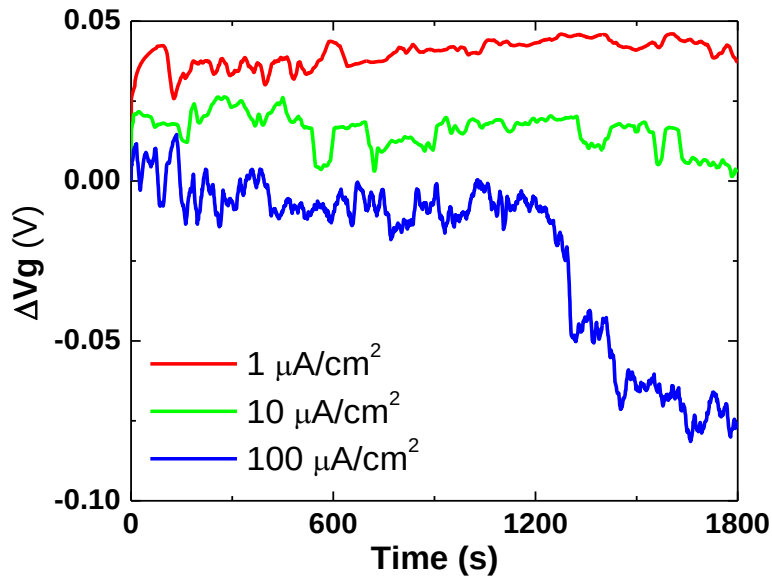


Figure 4-8 Gate voltage shifts at different constant-current stress levels.

4.6.2 Dielectric breakdown field distribution

The dielectric breakdown field is a good indicator of the dielectric material quality [9]. For a given dielectric, the breakdown field depends on traps, defects and the density of the material. Less pre-existing defects and denser films usually have higher breakdown fields. But even for films on the same sample with same process condition, breakdown fields may vary from one diode to another. It is necessary to investigate statistics of breakdown fields within a certain number of sample size. In addition, the degree of statistical variation of measured fields is also a good reflection of dielectric reliability. The less variation indicates the better deposition process.

Our study compared the breakdown field distribution for Al_2O_3 films with PEALD and thermal ALD growth in MISH diodes. N_2 and plasma N_2O post annealing effects on PEALD film

breakdown fields were also investigated. Post treatment process conditions were 5 minutes 500°C for N₂ post deposition annealing and 20 minutes 500°C for plasma N₂O post annealing, respectively.

Thermal ALD Al₂O₃ films have lowest breakdown fields among all samples. The calculation gives an average breakdown field of 7.4 MV/cm. This result is in agreement with our previous suggestion that thermal ALD Al₂O₃ films do not exhibit good insulating properties. PEALD Al₂O₃ films, however, show an average breakdown field of 8.6 MV/cm. In addition, more than 75% of test samples fall into the breakdown field range of 8-9 MV/cm. The small variation of samples indicates the reliable deposition process.

The N₂ annealing treatment on PEALD Al₂O₃ films does not significantly change the dielectric breakdown field. An average number of 8.2 MV/cm is slight below the average field of samples without annealing. The increase of leakage current could be a factor that contributes to the reduction of the mean breakdown field. On the other hand, plasma N₂O annealed samples exhibit supreme insulating properties with an average breakdown field of 8.9 MV/cm. The plasma N₂O annealing allows both oxygen and nitrogen incorporation into Al₂O₃ film. Incorporated nitrogen atoms harden the dielectric film and improve the film resistance to dielectric breakdown.

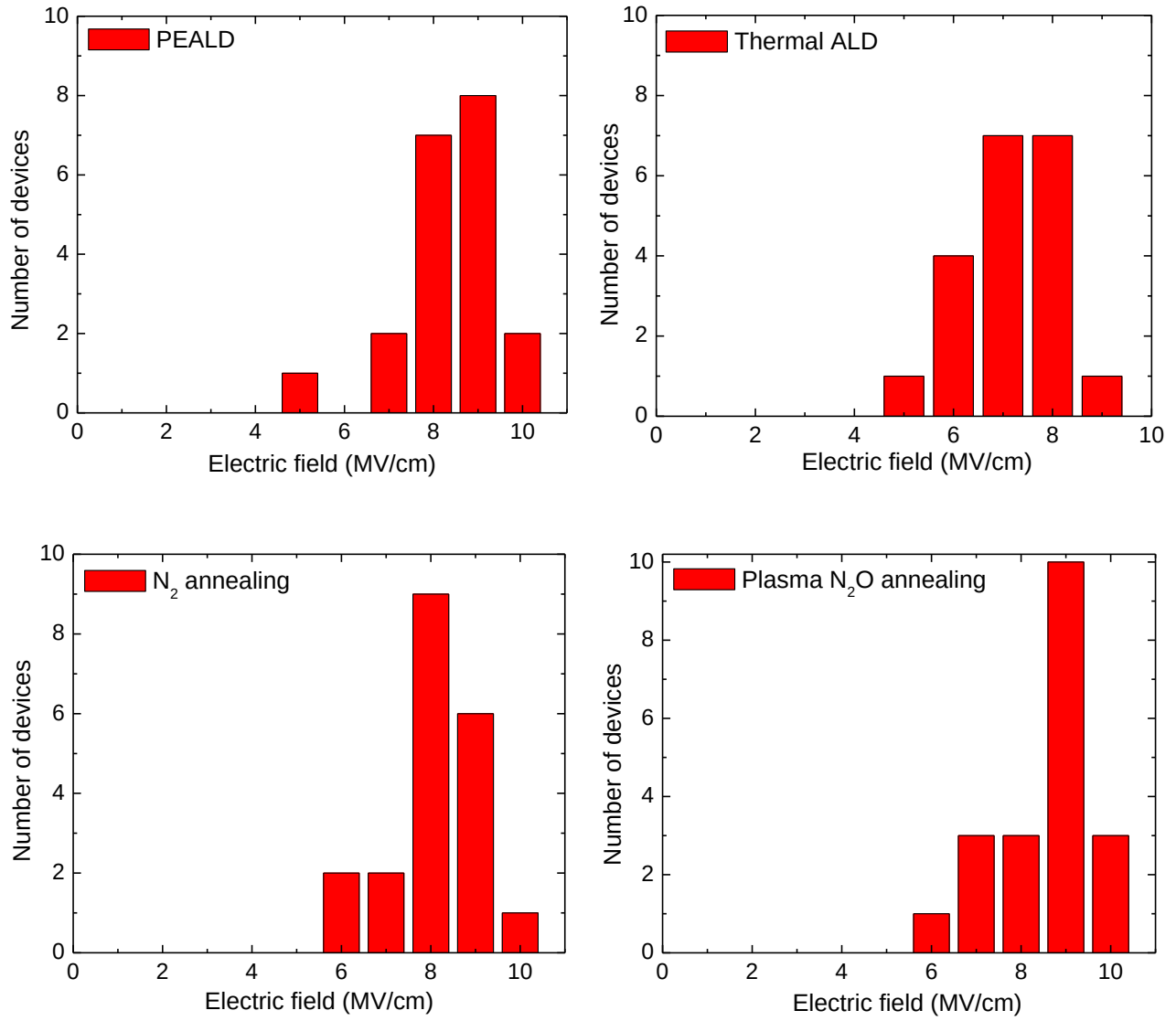


Figure 4-9 Dielectric breakdown field distribution of MISH diodes with (a) PEALD Al_2O_3 films, (b) thermal ALD Al_2O_3 films, (c) PEALD Al_2O_3 films after N_2 post deposition annealing and (d) PEALD Al_2O_3 films after plasma N_2O post deposition annealing.

4.6.3 TDDB test

One of major concerns of dielectric thin film reliability in long term is time dependent dielectric breakdown. An empirical model was first introduced with the observation of logarithm time to failure versus electric field relation. Two theories were then developed to explain this model. One theory focused on the dipolar interaction with electric field (E-Model) while the other one was based on Fowler-Nordheim tunneling (1/E-Model). Both of them were found fit experimental results very well.

The E-Model can be expressed by the following equation:

$$\ln t \propto \frac{Q_1}{K_b T} - \gamma E_{ox}$$

where Q_1 stands for the activation energy required for breaking a bond and γ stands for a field acceleration factor.

The 1/E-Model can be expressed by the following equation:

$$\ln t \propto \frac{Q_2}{K_b T} - G \frac{1}{E_{ox}}$$

where Q_2 stands for the activation energy related to current induced hole injection and capture and G also stands for the field acceleration factor.

We employed this TDDB test in our work in order to study Al_2O_3 dielectric lifetime and reliability. The test was performed on $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MISH capacitors with three constant gate voltage stress (3.4V, 3.7V and 4.0V) and 10 devices at each voltage condition. The result is plotted through Weibull distribution in figure 4-10. A Weibull slope of 2.87 is extracted by fitting $\ln(-\ln(1-F))$ vs t_{BD} (time to breakdown) curves. The inset figure shows a lifetime plot of this structure. The time

to 63% breakdown plot shows a field dependence of $1/E$, which also indicates that the current-driven breakdown process is dominated by tunneling conduction. This result is also in agreement with the conclusion of tunneling transport mechanism in the previous analysis.

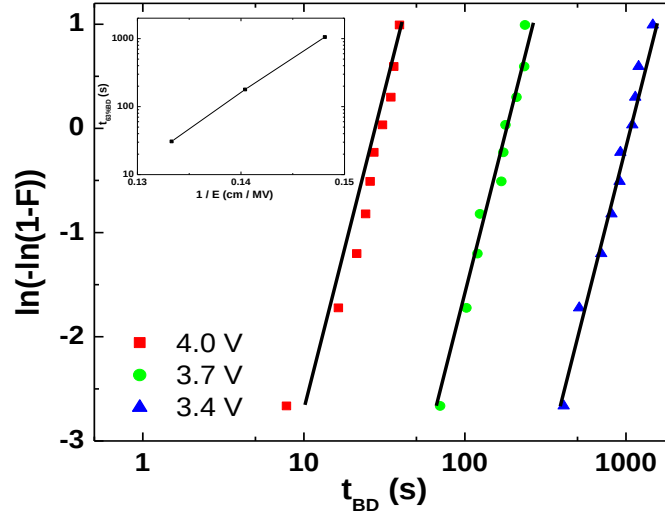


Figure 4-10 Weibull distribution in three TDDB tests at 3.4V, 3.7V and 4V gate voltage. A Weibull slope of 2.87 is extracted from the plot. Inset plot shows a field dependence of 63% time to breakdown.

4.7 References

- [1] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed., New Jersey: Wiley-Interscience, 2007, p. 227.
- [2] K. B. Jinesh, J. L. Van Hemmen, M. C. M. Van De Sanden, F. Roozeboom, J. H. Klootwijk, W. F. A. Besling and W. M. M. Kessels, "Dielectric properties of thermal and plasma-assisted atomic layer deposited Al_2O_3 thin films," J. Electrochem. Soc., vol. 158, no. 2, pp. G21-G26, 2011.
- [3] R. Ludeke, M. T. Cuberes and E. Cartier, "Local transport and trapping issues in Al_2O_3 gate oxide structures," Appl. Phys. Lett., vol. 76, no. 20, pp. 2886-2888, 2000.

- [4] M. Specht, M. Städele, S. Jakschik and U. Schröder, "Transport mechanisms in atomic-layer-deposited Al₂O₃ dielectrics," *Appl. Phys. Lett.*, vol. 84, pp. 3076-3078, 2004.
- [5] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung and H. Zhou, "Temperature dependent forward gate current transport in atomic-layer-deposited Al₂O₃/AlGaIn/GaN metal-insulator-semiconductor high electron mobility transistor," *Appl. Phys. Lett.*, vol. 98, pp.163501, 2011.
- [6] M. D. Groner, J. W. Elam, F. H. Fabreguette and S. M. George, "Electrical characterization of thin Al₂O₃ films grown by atomic layer deposition on silicon and various metal substrates," *Thin Solid Films*, Vol 413, pp 186-197, 2002.
- [7] R. Degraeve, B. Kaczer and G. Groeseneken, "Degradation and breakdown in thin oxide layers: mechanisms, models and reliability prediction," *Microelectronics Reliability*, Vol. 39, pp. 1445-1460, 1999.
- [8] T. L. Wu, D. Marcon, M. B. Zahid, M. Van Hove, S. Decoutere and G. Groeseneken, "Comprehensive investigation of on-state stress on D-mode AlGaIn/GaN MIS-HEMTs," *Proc. Int. Rel. Phys. Symp.*, pp. 3C.5.1-3C.5.7, 2013.
- [9] B. Gaffey, L. J. Guido, X. W. Wang, and T. P. Ma, "High-quality oxide/nitride/oxide gate insulator for GaN MIS structures", *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp.458 - 464, 2001.

Chapter 5 Summary and future work

Our research helps us understand the properties of nitride based materials and devices. Although the entire picture of achieving required interfaces and dielectrics has yet to be realized, part of the issues and problems has been revealed and solved in this work.

5.1 Materials and fabrication

Thermal ALD and PEALD Al_2O_3 thin films were successfully deposited on MBE grown AlGaIn/GaN heterostructure epitaxial layers. Both Al_2O_3 thin films exhibit better surface morphology. The thin film crystal structure changes from amorphous to polycrystalline after annealing under 1000°C for 5 minutes. The XPS study reveals the band offset of $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. The fabrication of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS diodes was also achieved using Ti/Al/Ni/Au stack as ohmic contact while Ni/Au as gate contact. The pre-deposition treatment shows a lower oxygen concentration at interface after ALD growth. The future work could be emphasizing on developing better dielectric materials. ALD growth and surface treatment conditions can also be optimized to pursue an even lower density of interface states.

5.2 Interface

Interface state characterization by C-V test were widely used in our work. C-V profiles provide us plenty of information on dielectric material properties and dielectric/semiconductor interfacial properties. The profound C-V technique and its derivative tools enrich our knowledge and understanding on electrical performance. Traps with different energy levels were differentiated by

C-V hysteresis curves and multi-frequency C-V. Effects of deposition methods on defect densities were studied. It suggests that PEALD provides better film quality with lower defect densities than thermal ALD. The use of NH_3 and N_2 pre-deposition surface plasma treatment and post-deposition annealing also improves the interfacial behavior. In the future, more work should be focused on deep level states characterization by photo assisted C-V or DLOS. The employment of light source enables the characterization of mid-gap defect states. Since the interfacial property depends on the intrinsic compatibility of the dielectric and semiconductor material, seeking another GaN matched dielectric other than Al_2O_3 might be an alternative solution to achieve a lower interface state density. AlN makes itself almost perfect candidate for AlGaIn/GaN gate dielectric material due to its nitride based nature and small lattice mismatch with GaN. However, the high quality and high conformity film deposition needs to be realized first.

5.3 Dielectric

Al_2O_3 dielectric thin film leakage current and conduction mechanisms were investigated. PEALD Al_2O_3 thin films exhibit better leakage current suppression compared to thermal ALD films. The result of temperature dependent I-V characterization suggests us that Poole-Frenkel emission dominates in dielectric current transport at medium electric fields, while at high electric fields, Fowler-Nordheim tunneling and trap-assisted tunneling dominate at low temperatures and high temperatures, respectively. In terms of dielectric reliability, we employed stress test, dielectric breakdown field distribution statistics and TDDB test on Al_2O_3 thin films. It shows that PEALD Al_2O_3 films have a larger average dielectric breakdown field than thermal ALD films, while the plasma N_2O post deposition annealing can improve the average breakdown field. TDDB test

results can be fit with $1/E$ field dependent model and a Weibull slope of 2.87 is extracted on PEALD Al_2O_3 thin films.

5.4 Summary

To summarize, this work focused $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISH structure design, fabrication and characterization. We successfully designed our processes, deposited Al_2O_3 thin films on $\text{AlGaIn}/\text{GaIn}$ epitaxial layers by thermal ALD and PEALD techniques and fabricated $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MISH diodes. Several electrical characterization methods were modified and performed to evaluate dielectric/semiconductor interfacial properties, dielectric conduction mechanisms and reliability. By applying pre-deposition surface treatment and post-deposition annealing, we were able to significantly improve the interface and dielectric material with a reduction in the interface state density and gate leakage current. These achievements might offer a better device performance and reliability in MIS-HEMTs, and enable the further progress and development of nitride based power electronics.