UNIVERSITY OF CALIFORNIA,
IRVINE

The Art of Voltage Boosting

Part I: Boosting Switched Capacitor Converter

Part II: Hybrid Boosting Converters

DISSERTATION

submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Bin Wu

Dissertation Committee:
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ACKNOWLEDGMENTS

I'm writing this acknowledgement on Morning, Aril 10, 2016, Irvine, California, which is a cloudy morning. At this moment, recalling my four and half years' study in UC Irvine, all up and downs in my research and final achievements upon graduation, I cannot suppress my excitement to express my deepest gratitude to my dear advisor, Keyue Smedely, who offer me the chance to pursuit my PhD's degree in US and led me to the true way of becoming a scientist. Without her cultivation, both in personality and research methodology, my giant progress cannot be possible. It's her who changed my life and shed me the bright light into the future. There will never be enough words to express my acknowledgement to this.

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Publications

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[1] **B. Wu**, S. Li, K. Ma Smedley, and S. Singer, "A Family of Two-Switch Boosting Switched-Capacitor Converters," IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5413–5424, Oct. 2015.(IF:6.008)

[2] **B. Wu**, S. Li, Y. Liu, and K. Ma Smedley, "A New Hybrid Boosting Converter for Renewable Energy Applications," IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1203–1215, Feb. 2016. (IF:6.008)

[3] **B. Wu**, S. Li, K. M. Smedley, and S. Singer, "Analysis of High-Power Switched-Capacitor Converter Regulation Based on Charge-Balance Transient-Calculation Method," IEEE Trans. Power Electron., vol. 31, no. 5, pp. 3482–3494, May 2016. (IF:6.008)

[4] **Wu, B.**; Naderi, R, Smedley, K. "A Modified Buck-Boost DMPPT Tracker with Improved Tracking Accuracy" submitted to IET power electronics (Accepted) (IF:1.683)

[5] **Wu, B**.; Li, S.; Smedley, K. "A new Single-switch Isolated Hybrid Boosting Converter with Bipolar Voltage Multiplier" submitted to IEEE Transactions on Industrial Electronics (Accepted) (IF:6.498)

[6] **Wu, B.**; Smedley, K. and S. Singer, "Comparative Analysis of Steady-State Models for Switched Capacitor Converter" submitted to IEEE Transactions on Power Electronics (Accepted) (IF:6.008)

Conference Papers:

[7] **B. Wu** and K. Smedley, "A new Isolated Hybrid Boosting Converter," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 28–34

[8] **B. Wu**, S. Keyue, and S. Sigmond, "A new 3X interleaved bidirectional switched capacitor converter," in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, 2014, pp. 1433–1439.

[9] **B. Wu**, S. Li, and S. Keyue, "A new hybrid boosting converter," in 2014 IEEE Energy Conversion Congress and Exposition (ECCE), 2014, pp. 3349–3354.

[10] **B. Wu** and S. Keyue, "A current control MPPT method in high power solar energy conversion system," in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, 2014, no. 1, pp. 3021–3025.

[11] **B. Wu**, S. Keyue, and S. Sigmond, "A Unified Switched Capacitor Converter," in Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2014, pp. 1433–1439.

[12] Singer S, Beck Y, **Bin Wu**, et al. Suitability of capacitive converters to photovoltaic systems[C]//Electrical and Electronics Engineers in Israel (IEEEI), 2014 IEEE 28th Convention of. IEEE, 2014: 1-5.

[13] S. Li, **B. Wu**, K. Smedley, and S. Sigmond, "Analysis and Design of a 1-kW 3X Interleaved Switched-Capacitor DC-DC Converter," in Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, 2014, pp. 1692–1698.

Patents:

[14] **Bin Wu**, Keyue Smedley, Sigmond Singer, Two-switch switched-capacitor converters, Issued number: US20150263612 A1, Issued date: 2015.9.17

[15] **Wu, B.**; Smedley, K. "A family of hibird boosting converters"(Pending)

ABSTRACT OF THE DISSETTATION

The Art of Voltage Boosting

Part I: Boosting Switched Capacitor Converter

Part II: Hybrid Boosting Converters

By

Bin Wu

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine 2016

Professor Keyue M. Smedley, Chair

Voltage boosting is required in many energy conversion applications, ranging from front-end solar energy system to Medium-Voltage DC (MVDC)-grid system, and from headlamp ballast of automobile to fuel cell powered system. This dissertation is dedicated to the development of voltage boosting technology. New circuits were found both in switched capacitor converters and inductor-based power converters.

Part I

Switched Capacitor Converter (SCC) is a special branch of power electronics converters which is composed of capacitors and switches without the participation of inductors/transformers. It potentially has lower electromagnetic interference (EMI), lighter weight, lower cost, higher energy density, and the promise for full integration.

In this part, a family of "Two-switch Boosting Switched-capacitor Converters (TBSC)" is introduced, which distinguishes itself from the prior arts by its symmetrical interleaved operation, reduced output ripple, low yet even voltage stress on components, and systematic expandability. Along with the topologies, a modeling technique based on charge-balance transient-calculation is formulated, which provokes the converter regulation method through duty cycle and frequency adjustment. The design guideline for high efficient TBSC is provided and regulation under high power condition is explored.

In addition, an enhanced accurate modeling technique considering the output capacitor effect is developed for simple two-phase SC converters.

Part II

Built upon the momentum of the "Two-switch Boosting Switched-capacitor Converters (TBSC)" circuit structure, another family of Hybrid Boosting Converters (HBC) is developed, featuring wide regulation range, symmetrical configuration, low component voltage stress, small output voltage ripple, and expandable structure. It integrates the inductive switching cores of various functionalities and control strategies with Bipolar Voltage Multiplier (BVM), resulting in the new breed of hybrid converters: Hybrid Boosting Converters (HBC). The proposed HBC family includes the basic HBC, symmetrical HBC, Isolated HBC, and tapped inductor HBC, all of which are analyzed in details and design considerations are provided.

In addition, the 3D DC-DC converter concept for high power application, inverter configuration and DC micro-grid based on HBC converters are developed.

The proposed HBCs are applicable in many areas such HID lamp driver, X-ray system, ion pumps, front-end photovoltaic energy system, and energy storage systems.

Chapter 1 Introduction

1.1 Objective

In the past, most DC-DC converters were for step-down applications since most consumer electronic products draw energy from Power Grid, whose voltage level is much higher than the load DC voltage. A typical grid interfaced power electronics system is comprised of a front-end stage as a voltage rectifier and a second stage as a step-down DC-DC converter. The first stage performs the function of rectifying the AC voltage to a relatively high DC voltage, either actively or passively, while the second stage converts the high DC voltage to a much lower DC voltage. Step-down DC-DC topologies such as fly-back, LLC, push-pull converter for second stage were extensively investigated both in academia and industry, aiming at higher efficiency, lower cost, increased power density and improved reliability.

In contrast, voltage boosting technologies, which are also an important subset of DC-DC power electronics conversion technology, were less developed due to fewer applications found decades ago. In recent years, power electronics technology has been experiencing a booming development, with applications ranging from mili-watt energy scavenger to tens of megawatt wind power system. Voltage step-up technology is playing an increasingly important role in modern power electronics industry. The Uninterruptible Power Supply (UPS) system, serving as the back-up power system for critical load such as factories and hospitals, demands high step-up converter to boost the 48V telecom power supply voltage to 380V for inverter application[1]. The two-stage PV system requires a

front-end stage to be high-gain DC-DC converter to step up voltage from 20~40V to 400V, due to low terminal voltage of single solar panel. The offshore wind farm with an internal Medium Voltage DC (MVDC) grid calls for a high power high gain DC-DC converter to interface between the rectifier output at 1~6kV with MVDC bus at 30~60kV[2]. The automobile HID headlamp driver requires a DC voltage about 100V which should be boosted from the 12V battery voltage. Moreover, the state of art voltage booting technology has also been found widely used in X ray power supply system, modern electrical vehicle system, and fuel cell powered systems, where different specific requirements may be required, such as isolated or non-isolated, regulated or non-regulated, low gain or ultra-high gain, single-direction or bidirectional.

The objective of this dissertation is to explore voltage boosting technologies. Switched capacitor converter known as a network composed of only capacitors and switches has the advantages of easy integration, high power density, low EMI and lower cost. While for inductor-based converters, as it employ the magnetic components such as inductor, transformer or tapped-inductor, has an apparent advantage of easiness in voltage regulation. This dissertation focuses on voltage boosting technology both in switched capacitor and inductor based converter fields. New topologies were discovered together with modeling techniques and control methods.

1.2 Background

Voltage boosting technology in the power electronics field can be regarded as an input source connected with a collection of voltage boosting elements, resulting in an increased output voltage. Apart from the active switch, other adopted components include diode,

capacitor, inductor, tapped inductor and transformer. A concept description graph of voltage boosting technology can be presented shown as Figure 1.1. According to the figure, when the component network doesn't involve magnetic components, it can be defined as boosting switched capacitor converter. Otherwise it is an inductor based boosting converter.

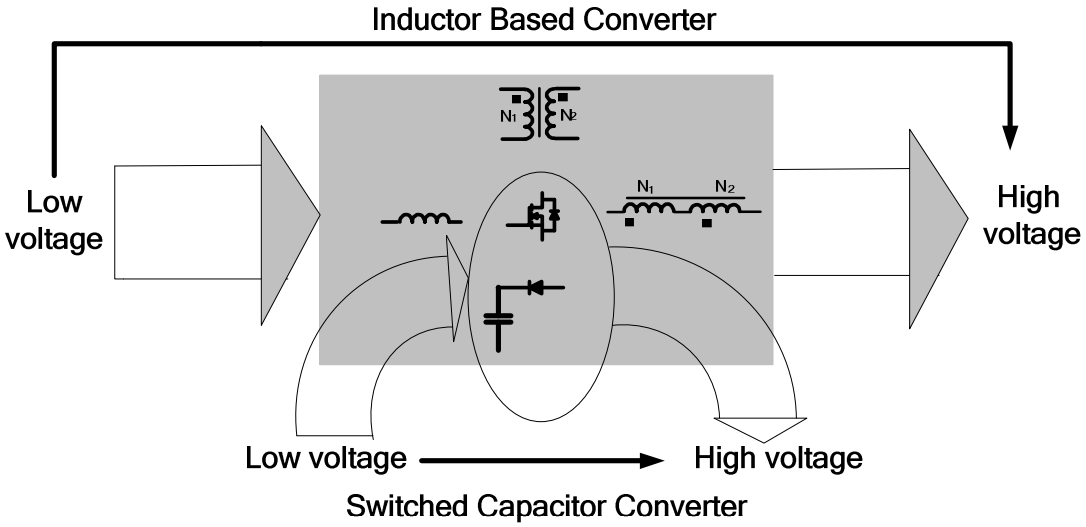
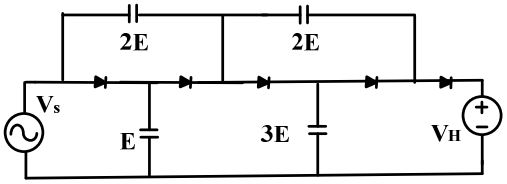
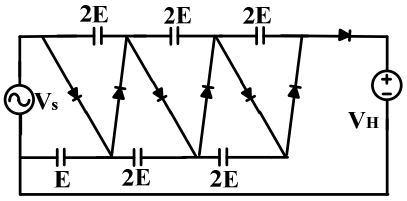


Figure 1.1 Voltage Boosting Technology

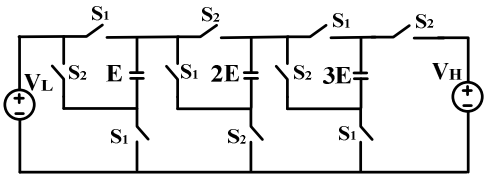
A comprehensive review of voltage boosting technology in switched capacitor converter and inductor based converter are provided in following two subsections.



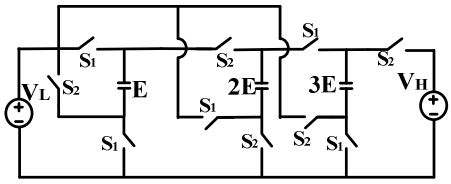
(a) Dickson multiplier



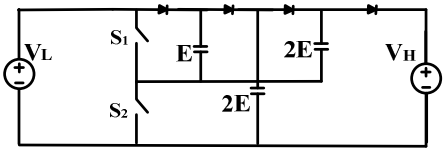
(b) Cockcroft Walton multiplier



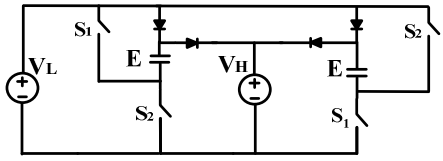
(c) Fibonacci SC(Makowski charg pump)



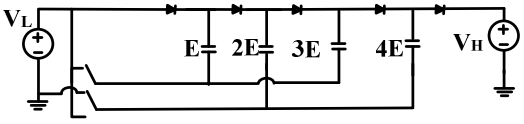
(d) MMCCC



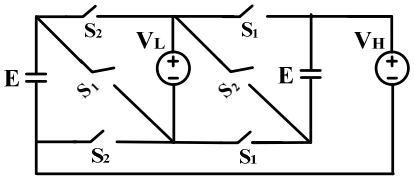
(e)Voltage lift (Luo)converter



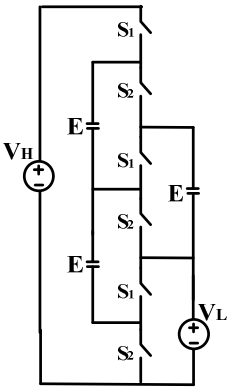
(f)Interleaved Parallel-Series SC Converter



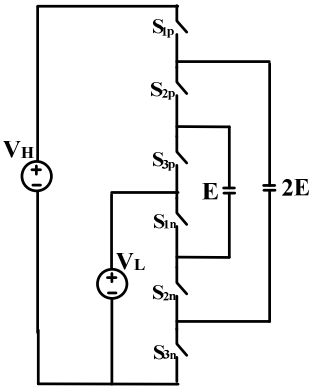
(g)Dickson charge pump



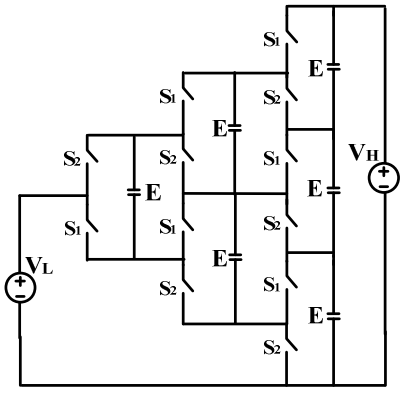
(h)DC-DC voltage doubler based on half-cell



(i) Ladder Converter



(j)Flying-capacitor SC converter



(k)Generalized multilevel SC converter

Figure 1.2 Switched Capacitor Boosting Technology

1.2.1 Switched capacitor voltage boosting technology

In the past, many step-up switched capacitor converters have been reported. Typical topologies are listed in Figure 1.2 and discussed in this section. The DC low voltage side has input source of V_L whose amplitude is "E". In the low voltage side is AC input, low annotated as V_s, it's amplitude is also assumed "E". Therefore, all the associated capacitors voltage stress can be clearly identified by "E" or multiples of "E" in Figure 1.2. The voltage at high voltage side is annotated as V_H. Moreover, the switches S_1 and S_2 are usually operating under duty cycle of 0.5 in complimentary manner. In regulation case, the switch controlling charging state can operate under Pulse Width Modulation (PWM) mode. Each converter is briefly introduced as below:

(1) Dickson Multiplier

Voltage multiplier was initially created to rectify and boost the alternating voltage to a high DC voltage, which has been used in X-ray tube power supplies[3]–[5]. The famous Dickon Multiplier is shown as Figure 1.2(a)[6]. The disadvantage of this multiplier is its uneven voltage stress of flying capacitors. Hence, this multiplier is not widely used.

(2) Cockcroft Walton multiplier

In contrast, the Cockcroft Walton multiplier has evenly distributed voltage across the flying capacitors, thus the component stress is low. This voltage multiplier has been widely used in very high gain applications, as shown in Figure 1.2(b). Isolated version and variations based on this multiplier has been comprehensively investigated[7], [8]. Small signal model is derived in [9]. However, due to its non-interleaving nature, large flying capacitors are needed to suppress the output voltage ripple.

(3) Fibonacci SC converter

Fibonacci switched capacitor converter is known as the topology that has the maximum attainable gain for a given number of capacitors[10], shown as Figure 1.2(c). It is a good candidate to increase the voltage gain with minimized die area. But it is demonstrated that the equivalent output resistance increases rapidly as the gain increases[11].

(4) MMCCC

The Multilevel Modular Capacitor Clamped DC-DC Converter (MMCCC) is a two phase modular switched capacitor converter[12], shown as Figure 1.2(d). It is expect to improve the conversion efficiency due to current flow path is optimized. But the high switch count and the increased capacitor stresses with increment of conversion ratio can post challenges on components selection, size, and cost[13].

(5) Voltage-lift Converter

The voltage lift technology has many variations[14]–[18], one of which is switched capacitor converter. A 3-lift circuit is shown as Figure 1.2(e). It has some similarities with the principle of Dickson charge pump but has less switches and smaller gain boosting capability. It can be a good candidate when tradeoff between switch number and voltage gain is required. But it also suffers from unbalanced capacitor stress issue and large output voltage ripple.

(6) The interleaved Parallel-Series SC converter

Figure 1.2(f) gives an interleaved Parallel-Series voltage doubler topology[19]. Other step-up topologies with different gain but similar configurations are investigated in [20]–[23]. The similarity of these converters is that the paralleling phase is controlled to regulate the output voltage, which determines the charging time of flying capacitors. Moreover,

interleaved branch is adopted to minimize the output filter capacitor and input current ripple. An apparent disadvantage of these topologies is the significant components count adopted to achieve a moderate gain.

(7) Dickson Charge Pump

Dickson Charge Pump is a well know charge pump and is being used in many voltage step up applications[24], shown as Figure 1.2(g). Compare with Fibonacci SC converter, it shows better performance in high gain situation, as equivalent output impedance is comparatively lower[11]. However, similar to voltage lift SC converter, it suffers from uneven capacitor stress and large output ripple.

(8) DC-DC voltage doubler based on half-cell

The DC-DC voltage doubler based on half-cell shown in Figure 1.2(h) is proposed in [25]. It introduces the interleaving operation to achieve smaller output ripple and input current stress. But the structure is not easy to expand while maintaining symmetrical configuration and the switch count is still large to achieve a given voltage gain.

(9) Ladder converter

Ladder converter shown as Figure 1.2(i) is well known for its capability of elevating an input voltage like a ladder. All flying capacitors and switches are equally stressed and the control is easy with two simple complementary control signals. The structure is flexible for expansion. But due to asymmetrical configuration, the component current stress is still large as well as output ripple.

(10)Flying Capacitor SC converter

The flying capacitor SC converter is employed in the electrical vehicle systems [26].A four-level dc-dc flying capacitor SC converter is shown as Figure 1.2(j). It apparently has a

reduced the flying capacitor number compared with other topologies in Figure 1.2 having same voltage gain. But it has an increased the component stress and calls for larger flying capacitor and filter capacitor to handle the voltage ripples. Moreover, the control complexity is increased because more operational stages found during a switching period.

(11) SC converter based on generalized multi-level converter

The SC converter shown in Figure 1.2(k) is also adopted in (42/14V) automotive system in [27]. The voltage conversion principle is straightforward with only two simple complementary control signals. The components stress is also balanced and minimized. But the large component count may prevent it from wide applications.

A summarizing table of listed topologies is provided as Table 1.1.

Table 1.1 Comparison of switched capacitor boosting topologies

Figure 1.2	Gain(V_H)	Flying Capacitors	Switch/ Diode	Comment Voltage Stress	Output Voltage Ripples
(a)	5E	4	5	large/uneven	Large
(b)	7E	6	7	Low/even	Large
(c)	5E	3	10	large/uneven	Large
(d)	4E	3	10	large/uneven	Large
(e)	3E	3	6	large/uneven	Large
(f)	2E	2	8	Low/even	Small
(g)	5E	4	9	large/uneven	Large
(h)	2E	2	6	Low/even	Small
(i)	3E	3	6	Low/even	Large
(j)	3E	2	6	large/uneven	Large
(k)	3E	6	12	Low/even	Small

It is not easy to pick a best topology among the listed topologies. Rather, it's more meaningful for designers to understand tradeoffs for specific applications. Different topologies may have some merits in certain aspects but suffer from problems in other

perspectives. The comparison table shown in 1.1 gives a general guideline for the trade-off considerations.

Part I of this dissertation is dedicated to provide some switched capacitor step-up solutions with small active switch count, low and even component stress, and small output voltage ripple, which is essential to reduce the cost and improve power density of SC converter.

1.2.2 Inductor based voltage boosting technology

On the contrary of switched capacitor converter, the inductor based voltage boosting topology has at least one magnetic component participating in the voltage conversion process. The magnetic components can serve as an energy storage element or transformer for mere voltage level escalation. Most inductor-based voltage-boosting topologies can be illustrated as some combinations in Figure 1.3. It should be noted that in some places, if a transformer is designed to store energy in its magnetizing inductance while release it in other operational stages, it is called “coupled inductor or tapped inductor”, regardless weather it provides isolation or not. Nevertheless, in this dissertation, to clarify topology based on configurations, transformer is defined based on whether it provides the galvanic isolation or not. If it doesn't provide galvanic isolation for the converter, it is defined as tapped inductor. Otherwise, it is defined as transformer.

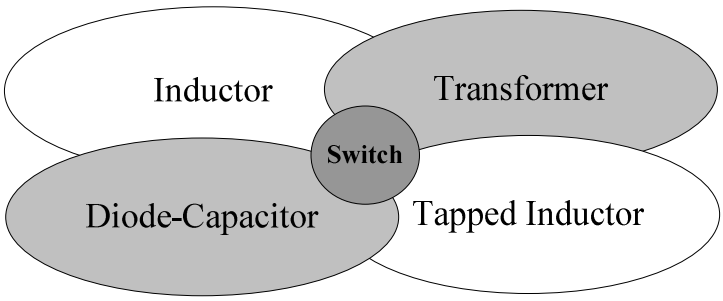


Figure 1.3 Inductor based voltage gain boosting elements

Figure 1.3 shows that the switch is the central element of a voltage boosting converter; a combination with four other major voltage boosting elements yields countless new topologies. Reviewing all the topologies is a tedious work. Therefore, they are briefly discussed based on the combination categories as below:

(1) Switch+Inductor

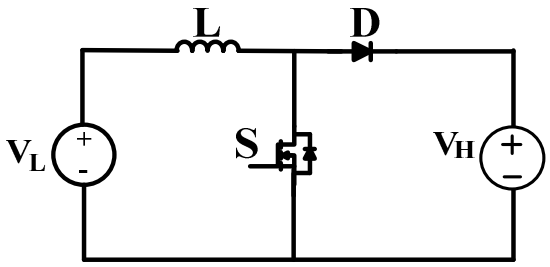


Figure 1.4 Switch+Inductor topology

The basic inductor based voltage boosting topology is the traditional boost converter, shown as Figure 1.4. It consists only switch and inductor elements because the diode and output capacitor serve as rectifier and filter instead of implementing voltage lift functionality. The boost converter is well suited to step up voltage less than four times as it has very low efficiency at a higher gain, in which case the extreme duty cycle has to be used and serious diode reverse recovery loss occurs. Moreover, the gain drops when duty

cycle becomes closer to one due to parasitic parameters of the circuit. Therefore, in order to further increase the voltage gain while maintain high efficiency, new topologies must be created.

(2) Switch+Transformer

A simple way to increase voltage level is using the principle of magnetic coupling. Figure 1.5 shows a conventional fly-back topology. It was commonly used in step-down DC-DC applications previously with step-down transformer. However, it also can be used to step up voltage when more turns at secondary side is used compared with primary side. Therefore, it is considered as voltage boosting technology with combination of switch and transformer. However, the issue associated with this approach is that when the voltage gain is increased, the primary side current will increase accordingly, leading to increased loss of leakage energy and aggregated voltage spike problem.

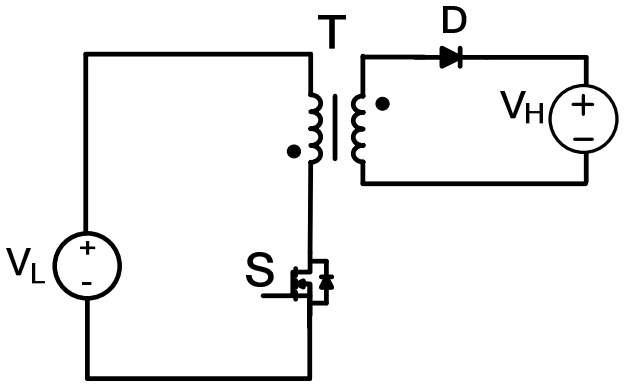


Figure 1.5 Switch+ Transformer topology

A new topology based on this combination was proposed in [28], which took use of the third winding of transformer and the primary-parallel secondary-series structure,

substantially extended the voltage gain. There are many merits created by this structure but the major concern is the challenges posted by production of three-winding transformers.

(3) Switch+Tapped-inductor

Another voltage gain boosting element is tapped inductor. The tapped boost converter is a well-known converter which employs the tapped inductor to extend the gain of boost converter, shown as Figure 1.6. Detail analysis of this converter is given in [29]. The problem with this topology is similar to the fly-back converter. The leakage energy loss may limit the conversion efficiency when the gain increases.

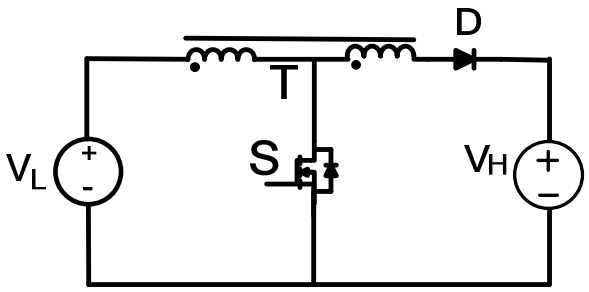


Figure 1.6 Switch+Tapped-inductor topology

(4) Switch+Inductor+Diode-Capacitor

Diode-capacitor structure is also a gain enhancement solution which can avoid dealing with issues cause by magnetic coupling method. A typical topology is shown in Figure 1.7, proposed in [30]. The diode-capacitor structures basically serve as voltage duplicators which are able to effectively enhance the voltage gain while maintaining high efficiency. But the capacitor number with high voltage ratings can increase the cost and volume of converter. Moreover, the output voltage ripple needs to be mitigated to reduce output filter size.

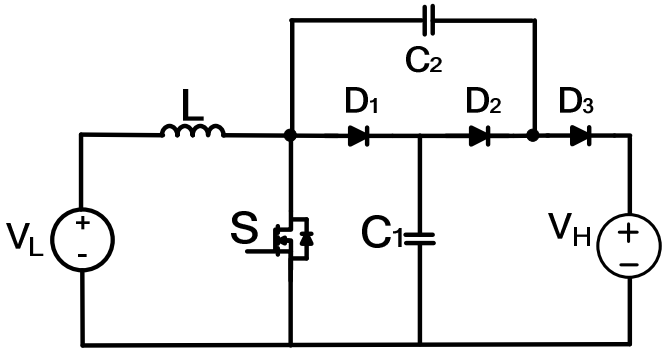


Figure 1.7 Switch+inductor+diode-capacitor topology

(5) Switch+Transformer+Diode-Capacitor

A typical topology that implements the idea of combining switch, transformer and diode-capacitor is given in Figure 1.8, reported in [31]. In such case, the desirable voltage gain can be achieved either by adjusting transformer turn ratio or diode-capacitor stage, leading to a more flexible gain design. But the leakage of transformer needs to be taken care of and the component stress is high.

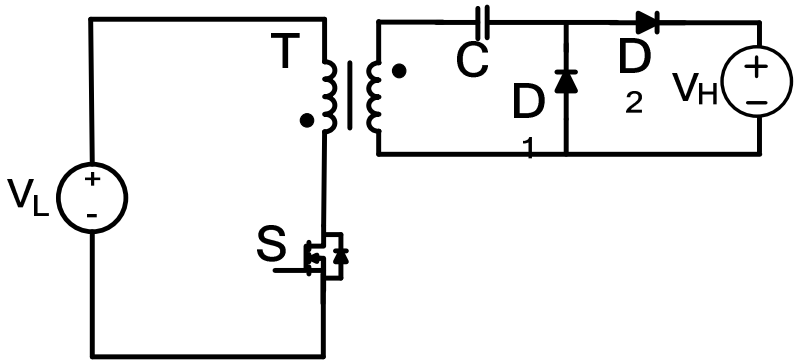


Figure 1.8 Switch+Transformer+Diode-capacitor topology

(6) Switch+Tapped-Inductor+Diode-Capacitor

A more advanced combination of two gain boosting elements is integrating tapped inductor with diode-capacitor stages, while handling leakage energy simultaneously. This

solution usually leads to more sophisticated operational process, but many topologies with high gain and high efficiency were created, at the price of increased components count. An example topology is show as Figure 1.9, proposed in [32]. The main reason for high efficiency achieved by these topologies is that it recycles the leakage energy of tapped inductor and creates soft-switching condition for the main switch. But due to more complicated circuit structure and increased component count, they are more suitable for low power applications. Moreover, large filter capacitors are normally required at the output.

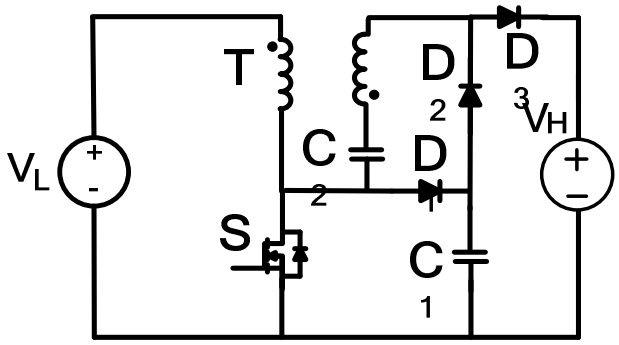


Figure 1.9 Switch+Tapped-inductor+Diode-capacitor topology

(7) Switch+Inductor+Transformer+Diode-Capacitor

With a further increased the complexity of combination (5), an extra inductor is added in some topologies, a sample circuit is given in Figure 1.10, developed in [33]. The benefit brought by the new inductor includes continuous input current and enhanced voltage gain boosted by the inductor. But due to the power processing path gets longer, the loss dissipated in circuit path may increase.

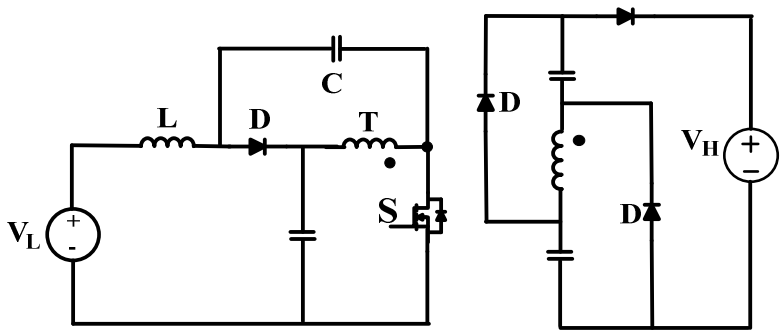


Figure 1.10 Switch+Inductor+Transformer+Diode-capacitor topology

(8) Switch+Inductor+Tapped-inductor+Diode-Capacitor

To amend the pulsating input current problem of the combination (6), an input inductor also can be incorporated in such circuits[34], shown as Figure 1.11. This combination has similar complexity level as the combination (7), which has employed three voltage boosting elements in the final circuit. The voltage gain was greatly enhanced. But compared to non-isolated structures, the efficiency has no superiority. Another topology implementing this combination was proposed in [35], where soft switching for main switch was created and more promising efficiency was derived. But complicate circuit design and increased component stress post the cost challenge for commercializing.

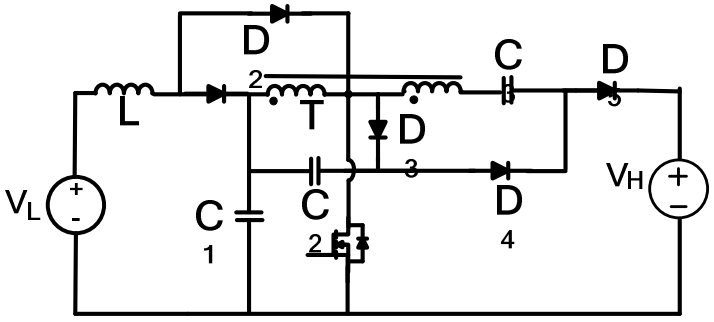


Figure 1.11 Switch+Inductor+Tapped-inductor+Diode-capacitor topology

In summary, the art of inductor-based boosting technology can be very sophisticated with numerous possibilities provided by the increase of participated boosting elements. It is a constant pursuit among the researchers to find circuit structures with minimum components, best efficiency, while achieving maximum gain. The challenges are discussed in above discussions. Many papers compared a proposed topology with some previous papers only in terms of voltage gain, but under different combination categories, which may not be appropriate. Such comparison may have disregarded the drawbacks brought by the high gain obtained, such as increased components count, component stress or deteriorated efficiency.

Therefore, a more proper comparison shall be performed within the same combination categories as referred to apple to apple comparison. For example, when the continuous input current or galvanic isolation is indispensable in some applications, such conditions should be default for all the converters in the comparison. The difference should be the cost, power density, and efficiency of two topologies with similar gain boosting capability, crossing combination categories. In this way, superior topology can be finally selected for specific applications.

Table 1.2 Combination of inductor based boosting topologies

Elements \ Combinations	1	2	3	4	5	6	7	8
A. Switch	★	★	★	★	★	★	★	★
B. Inductor	★			★			★	★
C. Transformer		★			★		★	
D. Tapped inductor			★			★		★
E. Diode-Capacitor				★	★	★	★	★
References	[36]	[28]	[29], [37]	[1], [15], [16], [30], [38]–[60]	[5], [31], [61]–[68]	[69]–[86]	[33], [87]–[96]	[34], [35], [97]–[105]

The combination categories are summarized in Table 1.2, with associated references given for further investigation.

In this dissertation, a family of inductor based converter, which is composed by a Bipolar Voltage Multiplier (BVM) and different inductive switching cores, is proposed. They can be classified to different categories in Table 1.2. Their superiority among the topologies in the same category is analyzed and demonstrated.

1.3 Outline of the thesis

This dissertation is composed of two parts. The first part reports the invention related to the voltage boosting switched capacitor topologies: the Two-switch Boosting Switched Capacitor Converter (TBSC). The second part reports the discoveries of new inductor-based converters: the Hybrid boosting Converters. Each part is presented with theoretical analysis and experimental demonstrations.

Part I:

The general introduction and development of switched capacitor converter is given in Chapter 2, with the topology, modeling and control technique reviewed respectively. The new development in this Part is outlined. In Chapter 3, the topology evolvement of TBSC family and its operation principal are introduced by case study of 2X TBSC and 3X TBSC. The new modeling method for TBSC is presented in Chapter 4. The performance investigation of TBSC and comparison with some previous topologies are carried out in Chapter 5. The simulation and experimental verification of proposed theory are provided in Chapter 6. The generalized Charge-balance Transient-Calculation (CT) modeling method

suitable for interleaved SC converter and enhance CT modeling method considering output capacitance are extensively studied in Chapter 7. They are both compared with many recently developed modeling methods.

Part II:

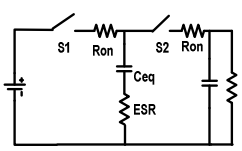
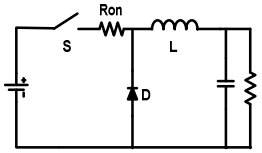
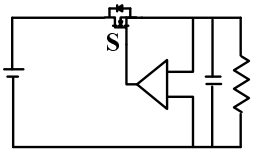
In part II, the introduction of hybrid converter is given in Chapter 9 and the new development in Part II is outlined. The topology development of Hybrid Boosting Converters (HBC) family is introduced in Chapter 10, which is inspired by TBSC family. The operational principles of each family member are briefly introduced. In Chapter 11, the based members of HBC family, basic HBC, is fully investigated. It is compared with other topologies in the same category defined by previous section. Experimental results are provided to verify the proposed theory. In Chapter 12, another member of HBC family, isolated HBC, is fully explored with a new design method of lossless snubber circuit proposed to cope with the leakage problem of transformer. The performance comparison with other work and experimental verification are provided. In Chapter 13, many potential new circuit configurations and applications are developed based proposed HBC converter. The simulation results are provided to verify the feasibility of these configurations.

Part I Two-switch Boosting Switched Capacitor Converter

Chapter 2 Introduction of Switched Capacitor Converter

Switched Capacitor Converter (SCC) is an important subset of power electronics converters, which is composed of capacitors and switches without the participation of inductors/transformers. It potentially has lower Electro Magnetic Interference (EMI), lighter weight, lower cost, higher energy density, and the promise for full integration[106], [107]. A comprehensive comparison of switched capacitor converter, inductor based converter, and Low Voltage Dropout (LDO) is summarized in Table 2.1.

Table 2.1 Comparison of SCC, inductor-based converter and LDO

Comparison	Switched capacitor converter	Inductor based converter	LDO
Concept topology			
EMI emission	Low	High	Very low
Cost	Low	High	Very low
Volume	small	large	Very small
Weight	light	heavy	light
Integration	full	partial	full
input current	impulsive	peak limited	continues
regulation	poor	good	poor
Power density	high	medium or low	high
efficiency	Suffer intrinsic loss	good	Suffer resistive loss
Gain flexibility	Step up/step down	Step up/step down	Step down
Dynamic	Fast	Medium	Slow

According to Table 2.1, the unique merits that switched capacitor converter can bring to future portable devices is small size, high power density, flexible gain choice and fast

response equipped by appropriate control scheme. Due to these unique characteristics, it becomes increasingly important to investigate the topology, modeling and control of switched capacitor converters.

In this chapter, the general development of switched capacitor converter in past decades is briefly reviewed in section 2.1. The previous research outcomes focused on topology, modeling, and control of switched capacitor converter are briefly discussed. The new development and contributions in this part are outlined in section 2.2.

2.1 Development of switched capacitor converter

2.1.1 Topology

Before 1990s, switched capacitor converter was primary in the form of voltage multiplier where diodes were usually driven by sinusoidal source[3]. After 1990s, switch mode Switched Capacitor Converter (SCC) attracted more attentions from power electronics community. A number of new topologies based on two-branch interleaving operation were proposed and verified with discrete semiconductor components prototype in power electronics labs[19], [20], [23], [108]–[110]. They were basically based on the idea of parallel-series configuration. Most of these topologies relied on controlling the time of charging phase to regulate the output voltage. These converters showed high power density and small output ripple. In the meantime, the CMOS level circuit design on simple switched capacitor converter began at the end of 1990s[111], [112]. In 1999, the simple switched capacitor product LM2660 with voltage doubling and inverting functions was released by National Semiconductor. In 2002, regulated SC converter with wide input

voltage range Max5008 was created by Maxim. In 2006, improved version of voltage inverting and doubling SC converter TL7660 was announced by TI. All these commercialized SC converters were focused on low power, simple topology by utilizing off-chip surface mounted capacitors. Compare with inductor-based converter, significant improvement was achieved in converter size by getting rid of inductor. Thereafter, researchers intended to integrate increased number of switches to formulate more complicate switched capacitor converters, such as charge pump[113] and structure variable SC converters[114].

In recent years, along with the advance of semiconductor industry, full integration of capacitors have become more realistic, which triggered a new round of enthusiasm to pursuit full integrated SC converter with further reduced convert size and improved power density. Many industrial and academic research institutions such as IBM, Intel, TI and UC Berkeley have built chip level full integrated SC converters in laboratory using different capacitor integration technologies [115]–[121]. Normally, structure variable scheme was adopted for SC converter to increase regulation range. Moreover, great efforts have been reported to optimize the design[122] and improve power density[123] of full integrated switched capacitor converter.

On the other hand, the application of switched capacitor converters on high power field was found in automobile system in 2000s, where topology using multilevel DC-DC structure were adopted[27], [124]. Article [125] reported a unregulated 1kW SC DC-DC converter for 42V automobile system with peak efficiency of 98%. In order to mitigate pulsating current and reduce capacitor size, resonant inductor was introduced to turn the SCC to Resonant Switched Capacitor Converter(RSCC) [126]. Some merits in efficiency

improvement under high power condition were confirmed. Article [127] uses the stray inductance in circuit to operate the resonant switched capacitor converter at 55kw. Article [128] and [2] proposed a new resonant SCC based on utilization of stray inductance or air core inductor, in which case careful selection of switching frequency is necessary. The regulation of high power switched capacitor becomes a challenge due to possible high component stress. Recently, some more switched capacitor topologies for DC-AC, AC-DC and AC-AC conversion have been reported[45], [128]–[131].

2.1.2 Modeling

Modeling technique of switched capacitor converter is essential to understand the performance of SCC. In 1990s, the traditional state-space averaging method was adapted to model the switched capacitor converter for steady state model analysis [19], [132], [133]. This model is general for inductor based power converter modeling and it found its way for switching capacitor converter modeling with satisfactory results under high frequency and large flying capacitance condition. Modified state-space averaging method was introduced to address the nonlinear property of switched capacitor but does not provide the frequency regulation characteristic either [134], [135]. In recent years, many new modeling techniques were developed to study the physical insights of switched capacitor converter from different aspects [136]–[153]. A widely referred equivalent circuit for steady state model of SC converter is showed in Figure 2.1. Instead of deriving the steady state conversion ratio of a switched capacitor converter directly, calculation of equivalent output impedance R_e was explored.

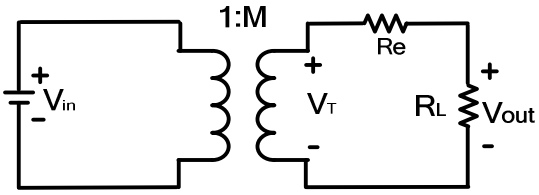


Figure 2.1 Equivalent circuit of SCC for steady state model

Based on the equivalent circuit, V_T is defined as target voltage, which is determined by the topology of switched capacitor converter. Regulation of equivalent transformer turn ratio M typically requires a large number of switches and capacitors to reconfigure circuit topology [114], [120], [154], [155]. Once M is fixed, lower equivalent R_e leads to higher conversion efficiency. Consequently, to derive an elegant expression of R_e becomes objective of many researchers for steady state modeling.

Previously, most expressions of R_e were derived based on analysis of a simplified SC block [136]–[146], as shown in Figure 2.2. Firm input and output voltage were usually assumed in the charging or discharging loops. The intermediate capacitor C serves as a storage element which delivers charge and energy by manipulation of switches S_1 and S_2. More sophisticated converters were considered composition of multiple building blocks equivalent to this basic structure [137]. Typically, the output filter capacitor effect was neglected, which raises the difficulty for output voltage ripple control.

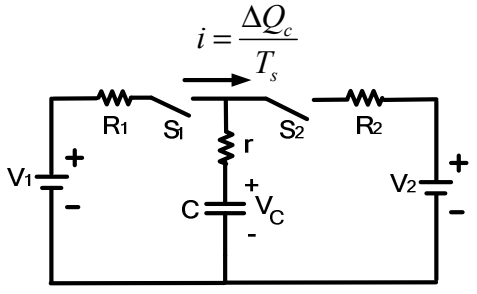


Figure 2.2 Simple SC blocks for steady state model analysis.

The recently developed steady state modeling techniques are reviewed as follows:

(1) Average current base method

In [136], [137], an average current based steady state model was proposed based in Figure 2.2. It assumes the intermediate capacitor voltage varied from V_{c1} to V_{c2} during discharging state. According to charge balance, the average current passing from V_1 to V_2 was found and denoted as i. The equivalent resistance between V_1 and V_2 was expressed as:

$$R_{eq} = \frac{V_1 - V_2}{i} = \frac{1}{fC} \frac{e^{(\frac{D_1 T}{\tau_1} + \frac{D_2 T}{\tau_2})} - 1}{(e^{\frac{D_1 T}{\tau_1}} - 1)(e^{\frac{D_2 T}{\tau_2}} - 1)} \quad \textbf{(2.1)}$$

where D_1 and D_2 are duty cycle of charging and discharging state, τ_1 and τ_2 are time constant of charging and discharging loops.

Equation (2.1) provides a unified form of the output impedance showing overall impact from circuit parameters on steady state of the unity gain SC converter, including the switching frequency, duty cycle, resistive elements and flying capacitance. But the method is based on the assumption of firm input voltage V_1 and output voltage V_2 sources. It is general but may not be accurate when limited output filter capacitance is considered.

(2) Average-current-base conduction loss method

Another general method based on average-current conduction loss calculation was proposed in [142]–[144]. This method divided a switching period into switching phases according to the operational modes. For each phase, equivalent RC sub-circuits were found

and power loss caused by each sub-circuit was calculated to match with a corresponding equivalent output resistor R_{ei}. Then the total output impedance can be accumulated as:

$$R_e = \sum_{i=1}^{m} k_i^2 \frac{1}{2 f_s C_i} \frac{1+e^{-\beta_i}}{1-e^{-\beta_i}} \tag{2.2}$$

where $\beta_i = T_i / R_i C_i$. T_i is the operation time of the sub-circuit, R_i is the total resistance alone the circuit loop and C_i is the total capacitance. The coefficient k_i was introduced to set $I_{Cav_i} = k_i I_{out}$, which is the average capacitor current of corresponding phase.

This method can be used for either dual-phase SC converters or multi-phase SC converters. It also takes into account the frequency effect on the steady state and includes overall circuit parameters effects. But as it employs the average current for conduction loss calculation, it suffers from inaccuracy issue for converters with large capacitor ripple. This method is suitable for SC converter without coupling loops since the RC sub-circuits are difficult to derive for some complex SC converters such as the ladder converter. Complex coupling loops in this dissertation refer that two circuit loops share a common element while each loop contains individual charging and discharging elements (source or capacitor) in the same switching state.

(3) Fast Switching Limit and Slow Switching Limit method

Paper [156] found that by comparing sub-circuit time constant τ_i with the switching period T_s, three different regions can be distinguished: low frequency, high frequency and intermediate region. Different analysis approaches can be applied to derive the corresponding equivalent output impedances according to frequency ranges. A general

form for low frequency limit $\tau_i << T_s$ was provided in the paper but equations for other regions were not given. In [146], a specific step down SC converter was investigated and the expressions for low frequency limit and high frequency limit were both calculated. In the intermediate frequency region, an empirical approximation equation employing corner frequency and low frequency limit was provided. Paper [157] proposed an approach based on power loss analysis on switches to derived the general form of output impedance for fast switching limit. Thereafter the analytical approaches for output impedance during full switching frequency range were available.

However, more systematic analysis and elegant expressions were given in [140]. It synthesized previous works and generalized the results as Fast Switching Limit (FSL) and Slow Switching Limit (SSL). For SSL, the finite resistance of switches, and capacitor ESR were neglected. The output impedance was given as:

$$R_{SSL} = \sum_i \frac{(a_{c,i})^2}{C_i f_s} \tag{2.3}$$

Where $a_{c,i} = q_i / q_{out}$ corresponds to the i^{th} entry of the charge multiplier vector a_c. C_i is the i^{th} flying capacitor and f_s is the switching frequency.

For FSL, the output impedance was expressed as:

$$R_{FSL} = 2\sum_i R_i (a_{r,i})^2 \tag{2.4}$$

Where R_i is "on resistance" of the i^{th} switch. In this derivation, other resistive elements along circuit paths were neglected and the switching duty cycle was assumed to be 50%.

The method neglects the resistive loss under low switching limit case and merely considers switch conduction loss under fast switching limit case, causing the modeling process to be simpler and easier to implement even for complex SC converters. Since this method treats the capacitors and switches as independent elements instead of searching RC sub-circuits, it can be applied to model the SC converter with coupled charging loops such as ladder converter. In [138], some further work based on [140] was explored to amend the model. ESR of capacitor during FSL calculation was included and the output impedance at intermediate range between LSL and FSL was reworked by employing a new empirical equation using Minkowski distance form:

$$R_e = \sqrt[i]{R_{FSL}^i + R_{SSL}^i} \tag{2.5}$$

where i was proven to be more precise when adopting the value of 2.54514. This result corrected the equation given in [146][111] and [158], where i was assumed to be 2. However, as the result was obtained empirically by postulation and verification, the extensive accuracy over the entire frequency range was still undemonstrated.

(4) Voltage Gap Calculation method

Another modeling approach based on voltage gap calculation was proposed in [139] recently. It was also based on the basic SC block as Figure 2.2.The voltage gap between the input voltages and maximum flying capacitor voltage as well as the gap between minimum flying capacitor voltage and output capacitor were calculated. Based on the gap expressions derived, the equivalent impedance between V_1 and V_2 in Figure 2.2 can be expressed as:

$$R_{eq} = \frac{V_1 - V_2}{i} = \frac{1}{Cf_s}\left(1 + \frac{e^{-\frac{T_{cr}}{R_{cr}C}}}{1 - e^{-\frac{T_{cr}}{R_{cr}C}}} + \frac{e^{-\frac{T_{dr}}{R_{dr}C}}}{1 - e^{-\frac{T_{dr}}{R_{dr}C}}}\right) \quad \textbf{(2.6)}$$

This modeling method was developed for multi-input SC converters, regardless of resonant or non-resonant case. A brief comparison of surveyed steady state molding methods is given in Table 2.2.

Table 2.2 Comparison of surveyed steady state modeling methods for SC converter

Steady state modeling method	Pros	Cons	Suitable Applications
Average Current based method(AC) [136], [137]	Straightforward, for simple dual-phase SCC	Not generalized, infinite output capacitor assumed	Simple dual-phase SC converter
Average-Current-based Conduction Loss method(ACCL)[142]	Generalized, Continuous frequency range addressed	Inaccurate under Large capacitor ripple	Dual-phase and multi-phase SC converter with simple RC loops
FSL and SSL method(FSL-SSL) [140].	Generalized, easy implementation for complex SCC	Inaccurate in moderate switching frequency region	Complex SC converter with very high or low switching frequency
Voltage-Gap modeling method(VG) [139]	Easy implementation for multi-input SCC	Not generalized, infinite output capacitor assumed	Single or Multi-input SC converters

According to Table 2.2, most of the modeling methods listed have their application limitations and may become inaccurate under certain operation conditions. Moreover, no modeling method addresses the output filter capacitor effect on steady state behavior of SC converter.

2.1.3 Control Technique

Control technique is critical for power electronics converters since voltage regulation is indispensable for most power supplies. In order to solve the poor regulation issue of

switched capacitor converter, some researchers employed two stages converter and leave the regulation task to one dedicated stage while leaving the switched capacitor stage unregulated [2], [159]. But this dissertation will focus on the regulation issue of switched capacitor converter itself, which is consider as an challenge of this type of converter. Some previous proposed controlling techniques are reviewed as follows:

(1) Linear PWM control

PWM control is the most popular control technique in low power switched capacitor applications with discrete components. When the state space averaging modeling method was applied to switch capacitor converter in 1990s, small signal model considering duty cycle as control variable was derived. It became nature to use linear PWM control though modulation of duty cycle, based on linearization at designed operating point. However, the nonlinearity of switched capacitor was not considered, which may lead to deteriorated dynamic response and stability issue. A one-zero two-pole compensator design for close loop was investigated in [160]. Many interleaved buck type and boost type SC converters were reported using linear PWM control method [20], [109], [161].

(2) None-Linear PWM control

To address the nonlinearity of switched capacitor converter, variable structure sliding mode control was proposed in [147] and [162]. It was based on the sliding mode control theory, where a sliding function should be chosen and the sliding coefficient should be determined. This control method improved the dynamic response but may increase the complexity of control system design.

(3) Quasi-Switch current source control

The idea of controlling input switch as current source to mitigate pulsating input current issue and regulate output voltage had appeared in [132], [163]–[165].It controls gate voltage of the switch thus the switch behaves like a controllable current source. Due to reduced di/dt, the EMI problem is further mitigated with smooth input current obtained, which is beneficial to input source. However, this control method relies on accurate control of gate voltage, which is sensitive to system notice. Moreover, to guarantee the current source behavior of switch, significant amount of voltage drop on switch is required, leading to constrained system efficiency.

(4) Frequency control

In CMOS level SC converter, frequency modulation, ranging from several MHz to several hundreds of MHz, was more commonly used [111], [121]. It reflects the fact that switching frequency has fundamental impact on voltage gain of SC converter. The problem with switching frequency regulation is its narrow regulation range due to constrained frequency range. In addition, the variable voltage ripple and component stress caused by variable frequency may pose challenges in component design and circuit cost.

(5) Pulse dropping switching scheme

A pulse dropping switching technique(PDT) was proposed in [148]. The switching pattern was generated by comparing a triangular wave and rectangular wave with different frequency and amplitude. Therefore, pulsed driving signal with different density regions can be generated, leading to controllable output impedance of switched capacitor converter. The equivalent output resistance was demonstrated to have wide control range which enhances the regulation range of SC converter. But the control response may not be fast due to fixed pulse duty cycle.

(6) Other control methods

In order to improve the performance of controls system, some other more complicated control techniques were reported. The outer PWM loop for coarse control and FM inner loop for fine control was proposed in [166]. The pulse density and width modulation(PDWM) was reported in [167] to reduce output ripple. A voltage-reference-free pulse-density-modulation(VRF-FDM) method was presented in [168]. Overall, these methods are typically complicate.

2.2 Development in Part I of this dissertation

Based on comprehensive review and investigation of switched capacitor converter, contributions on step-up topology, modeling and control are made respectively in this dissertation as following:

A. A family of switched capacitor voltage boosting topologies

In article[169], a Two-Switch Boosting Switched-capacitor Converter (TBSC) family has been proposed. It has following figures:

(1) Symmetrical structure with automatic interleaving, leading to small output ripple

(2) Only two active switches, leading to simpler control and smaller converter size

(3) Feasible of pulse width modulation and frequency modulation for output voltage

(4) Low voltage stress of all components.

(5) Flexible gain extension for different applications

B. CT and enhanced CT modeling method

The Charge-balance Transient-Calculation (CT) modeling technique is fully investigated which is suitable for interleaves SC converters. It is applied to TBSC

converter and comprehensive voltage gain formula is derived. Moreover, the concerns in high power regulation design can be addressed by peak current stress estimation using this modeling method. Its accuracy in steady stage analysis is verified. The CT modeling result reveals the two dimensional regulation property of switched capacitor converters: duty cycle and frequency. Moreover, it's suitable for high power application analysis due to its accuracy in circuit stress analysis. The theories are demonstrated by experimental results.

In addition, enhance CT modeling method suitable for simple due-phase SC converter considering output capacitor converter effect is also investigated in this part. The results can provide accurate voltage gain estimation with different output capacitor. The output ripple optimization becomes possible for most commercialized switched capacitor products due to their simple due-phase structure.

Chapter 3 Topology Development of TBSC and Operational Principle

In chapter 1, a number of voltage boosting switched capacitor converters have been reviewed. In this chapter, the “Two-switch Boosting Switched Capacitor Converter” family is proposed, which is inspired by the traditional ladder converter. By moving the input source of ladder converter to the middle and keeping only two active switches, the TBSC topologies bring a number of new features: (1) Small output ripple, (2) Reduced input current ripple, (3) Reduced cost, and (4) Simpler driver design, while it maintains the advantages of (1) Low component stress and (2) Easy extension. The topology derivation of proposed TBSC family is described in section 3.1. The operational principle with proposed control signal pattern is illustrated in section 3.2, where case studies of 2X TBSC and 3X TBSC are illustrated. Bidirectional and step-down topology variation is briefly discussed in section 3.3.

3.1 TBSC family Derivation

The proposed TBSC family contains n members, where n=1, 2, 3 ... The first member is the 1X TBSC as shown in Figure 3.1(a). It is merely a two-switch 3-terminal network with terminal 0, 1, and 1'. Nevertheless, it is the core to build the entire TBSC family. For all TBSC members, terminal 1-1' is defined as the low side, while terminal n-n', high side.

In order to obtain the second member in the TBSC family, a pair of n=2 gain-extension networks, the top one with terminals 0, 1,and 2 and the bottom one with terminals 0', 1',

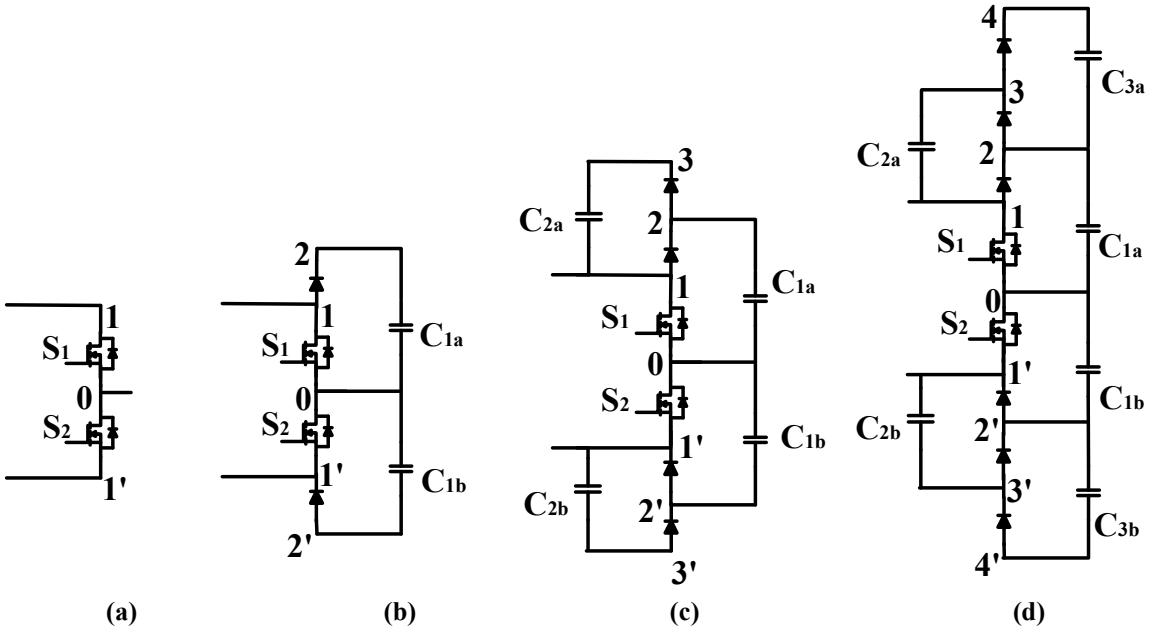


Figure 3.1 The proposed TBSC family

(a)1X TBSC (b) 2X TBSC (c) 3X TBSC (d) 4X TBSC

and 2' as shown in Figure 3.2 are added to the 1X TBSC as shown in Figure 3.1(a). By connecting the matching terminals of the gain-extension network and the 1X TBSC, the 2X TBSC is derived as shown in Figure 3.1(b). The voltage at the high side of the 2X TBSC configurations is double of that of the low side under the case of no load and idea components (ideal condition), by operating the two switches S_1 and S_2 in an interleaved manner.

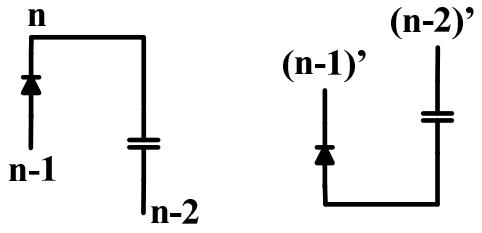
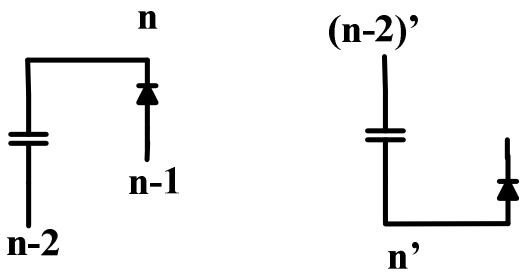


Figure 3.2 Gain-extension network (n=2, 4, 6…) (a) Top (b) Bottom

Further by adding a pair of n=3 gain-extension networks as shown in Figure 3.3 to the 2X TBSC in a similar fashion, the 3X TBSC can be derived as shown in Figure 3.1(c). The new configuration triples the low-side voltage by operating the two active switches S_1 and S_2 in an interleaved manner under ideal condition.



(a) (b)

Figure 3.3 Gain extension network (n=3, 5, 7…) (a) Top (b) Bottom

To synthesize the 4X TBSC topology, a pair of n =4 gain-extension networks in Figure 3.2 are added to the 3X TBSC topology in a similar fashion. Thus a new member with 4X gain is derived as shown in Figure 3.1(d).

This process can continue infinitely to obtain a TBSC with an ideal gain of arbitrary positive digital number n, by applying gain-extension network. In general, in order to obtain nX TBSC, a pair of 3-terminal gain-extension networks, the top one with terminals n-2, n-1, and n and the bottom one with terminals (n-2)', (n-1)', and n', as shown in Figure 3.2 or Figure 3.3, are added to the (n-1)X TBSC. By connecting the matching terminals of the gain-extension network to the (n-1)X TBSC, the nX TBSC configuration is derived. The voltage at the high side is n times of the low-side voltage (applied to terminal 1 and 1') by operating the two active switches S_1 and S_2 in an interleaved manner under ideal condition. Due to the symmetrical interleaved configuration of the circuit, the output

voltage ripple is reduced. Additionally, all components voltage rating is set by low side voltage.

3.2 Operational principle of TBSC

In order to illustrate the operating principle of TBSC family, the examples of 2X TBSC, 3X TBSC and nX TBSC are briefly discussed in this section.

3.2.1 2X TBSC

A simple voltage doubler as second member of TBSC family is shown in Figure 3.4, with source and load connected. Note that output filter capacitor is not necessary due to serial connection of C_{1a} and C_{1b}. The switch S_1 and S_2 will be controlled by interleaved PWM signal described by two top waveforms in Figure 3.5. The "Dead-time" which indicates the time period when both switches are off is controlled intentionally to modulate the output voltage. Therefore, four operation states will be observed during a period shown in Figure 3.6.

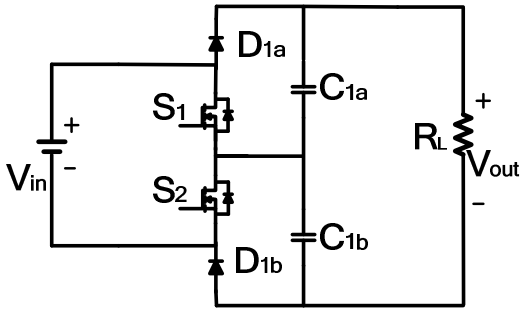


Figure 3.4 Topology of 2X TBSC

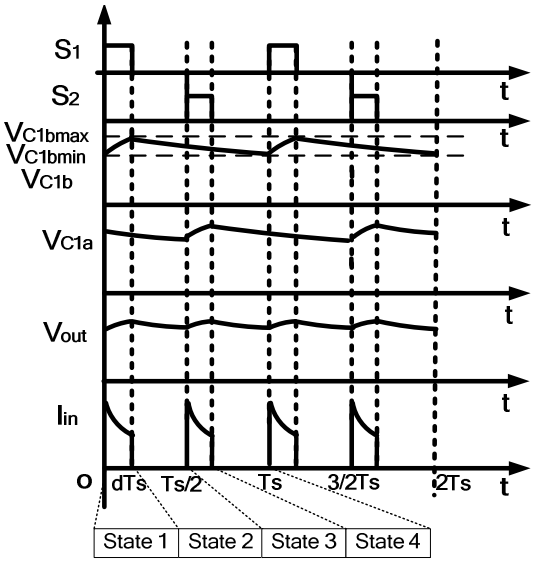


Figure 3.5 Driving signals and key waveforms of 2X TBSC

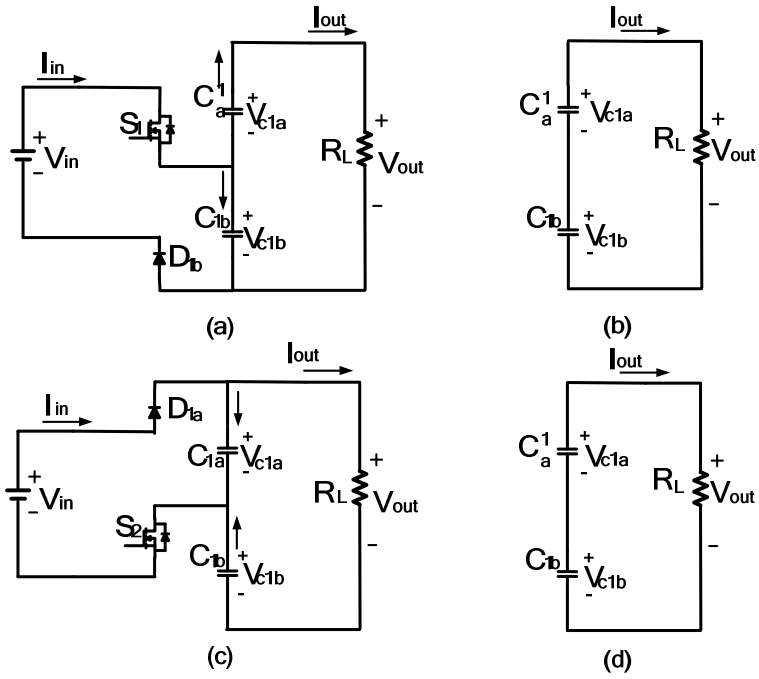


Figure 3.6 Operation states of 2X TBSC

(a) State 1[0, dTs]. (b) State 2[dTs, Ts/2] (c) State 3[Ts/2, (d+1/2)Ts].(d) State 4[(d+1/2)Ts, Ts].

Each operational state is briefly introduced as below:

1) State 1[0,dT_s]:

Switch S_1 is turned on during [0, dTs] while the duty cycle d is in the range of [0, 0.5]. When S_1 is on, the energy from input source will partially charge C_{1a} though D_{1a} and partially provide the load current directly, as shown in Figure 3.6(a).

2) State 2[dT_s, $T_s/2$]:

When S_1 and S_2 are both off, it comes to state 2 shown as Figure 3.6(b). Both diodes D_{1a} and D_{2a} become reverse biased and only capacitor C_{1a} and C_{2b} are connected in series to charge the load. Input current becomes zero at this state.

3) State 3[Ts/2,dTs+Ts/2]:

At this state, switch S_2 is on while S_1 is kept off, shown as Figure 3.6(c).The energy from input source will be partially delivered to load and partially used to charge capacitor C_{1a}.

4) State 4[dTs+Ts/2,Ts]

This state repeats the state 2.

By interleaved operation of S_1 and S_2, the input current ripple has the frequency twice of the switching frequency. Moreover, the voltage ripple of C_{1a} and C_{1b} are automatically interleaved. Therefore, the output voltage ripple is smaller due the ripple cancellation of capacitors C_{1a} and C_{1b}. Circuit key waveforms are shown as Figure 3.5.

3.2.2 3X TBSC

The 3X TBSC converters, shown as Figure 3.7, is a little more complicated compared with 2X TBSC. It contains coupled switched-capacitor loops, which will introduce

difficulty in modeling process. Its coupled loops which include source-capacitor pair and capacitor-capacitor pair achieve charge redistribution at the same time by sharing one or more common elements in circuit path.

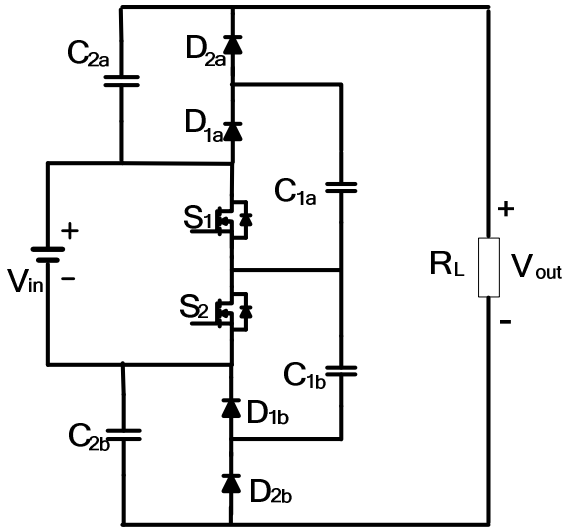


Figure 3.7. Topology of 3X TBSC

The 3X TBSC converter has following unique properties: First, it can serve as a voltage trippler under ideal condition. In real case, where components loss exist and load is non-zero, a duty ratio closer to 0.5 can achieve higher gain and higher conversion efficiency. Secondly, the input source is cascading with two flying capacitors C_{2a} and C_{2b} to build up the output voltage. These two flying capacitors C_{2a} and C_{2b} exhibit interleaved voltage ripples which are supposed to alleviate each other. Therefore, the output voltage ripple of proposed topology is expected to be small, yielding a smaller output filter capacitor or even skipped. Thirdly, the input source will keep delivering current to load even both switches are turned off, shown in Figure 3.9(b) and (d). This property, however, is different from 2X TBSC. It means for the whole period, the power source will release

energy without termination. The circuit driving signals and key waveforms are shown in Figure 3.8. Detailed operational states and waveforms are explained as following:

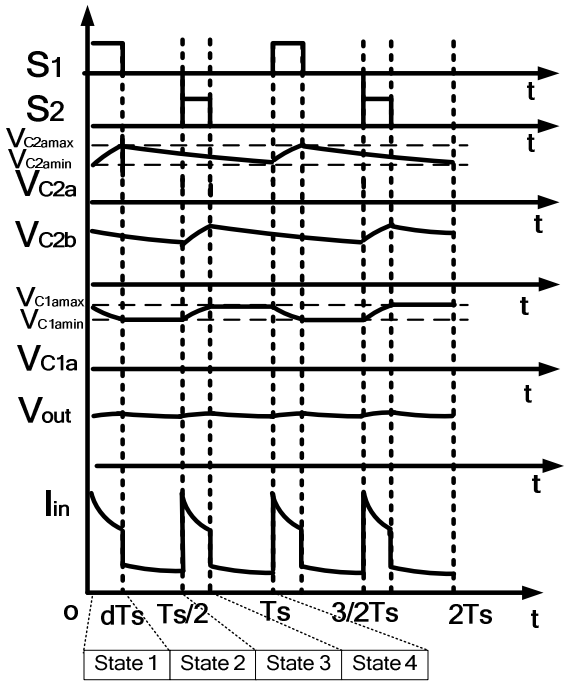


Figure 3.8 Driving signals and key waveforms of 3X TBSC

1) State 1[0,dTs]

When S_1 is on, as shown in Figure 3.9(a), the input source will charge the flying capacitor C_{1b}. At the meantime, it cascades with C_{2a} and C_{2b} to build up the output voltage. The flying capacitor C_{2a} is charged by C_{1a} though D_{2a} at the same state and C_{1a} is also delivering power to load.

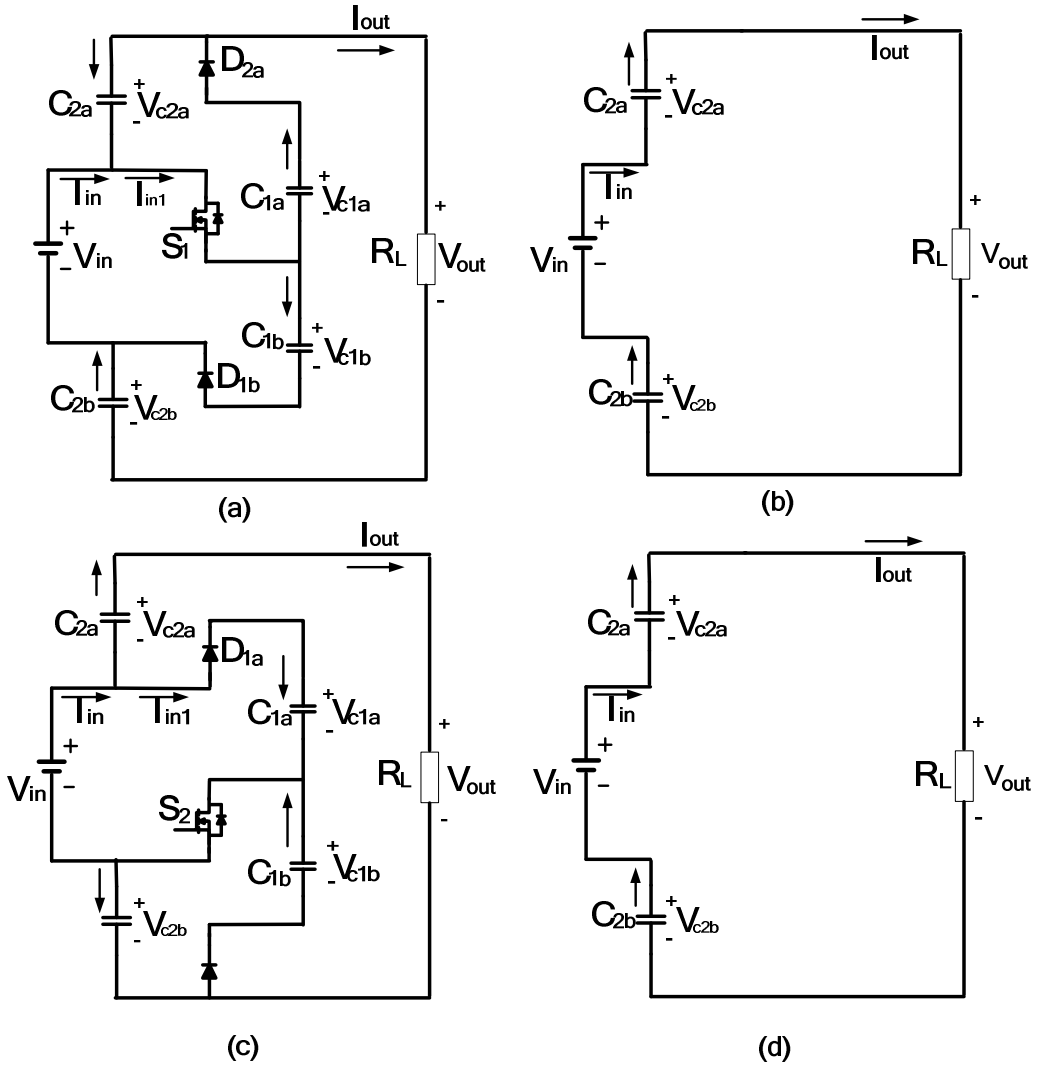


Figure 3.9 Operation states of 3X TBSC

(a) State 1[0, dTs]. (b) State 2[dTs, Ts/2] (c) State 3[Ts/2, (d+1/2)Ts].(d) State 4[(d+1/2)Ts, Ts].

2) State 2[dTs,Ts/2]

When both switches are off, the input source will be connected with C_{2a} and C_{2b} in series and power the load together. Thus input current I_{in} equals to the load current at this state, shown as Figure 3.9(b).

3) State 3[Ts/2,dTs+Ts/2]

In Figure 3.9(c), when S_2 is turned on while S_1 is off, the input source starts to charge C_{1a} which has released its energy in state 1. Thus C_{1a} can keep charge balance in one switching period. At the meantime, the input source is cascading with C_{2a} and C_{2b} to power the load. C_{2b} is charged by C_{1b}.

4) State 4[dTs+Ts/2,Ts]

This state repeats state 2.

The introduction of duty cycle to control the charging phase is only effective under the none-ideality and loaded condition. For ideal condition, which means all semiconductors components and capacitors are considered ideal, the 3X TBSC can reach its ideal gain of three, regardless of duty cycle variation.

3.2.3 High-order TBSC

In fact, the control signals for the entire TBSC family can be the same, which is simple and easy for implementation by utilizing traditional bridge-based driving circuit. It is convenient to draw control power from input source according to the circuit configuration.

For higher order TBSC converters, the operational principle is similar while higher voltage boosting capability can be achieved. Based on the ideal voltage gain of high-order TBSC, the TBSC can be classified as even-order TBSC or odd order TBSC, as shown in Figure 3.10.

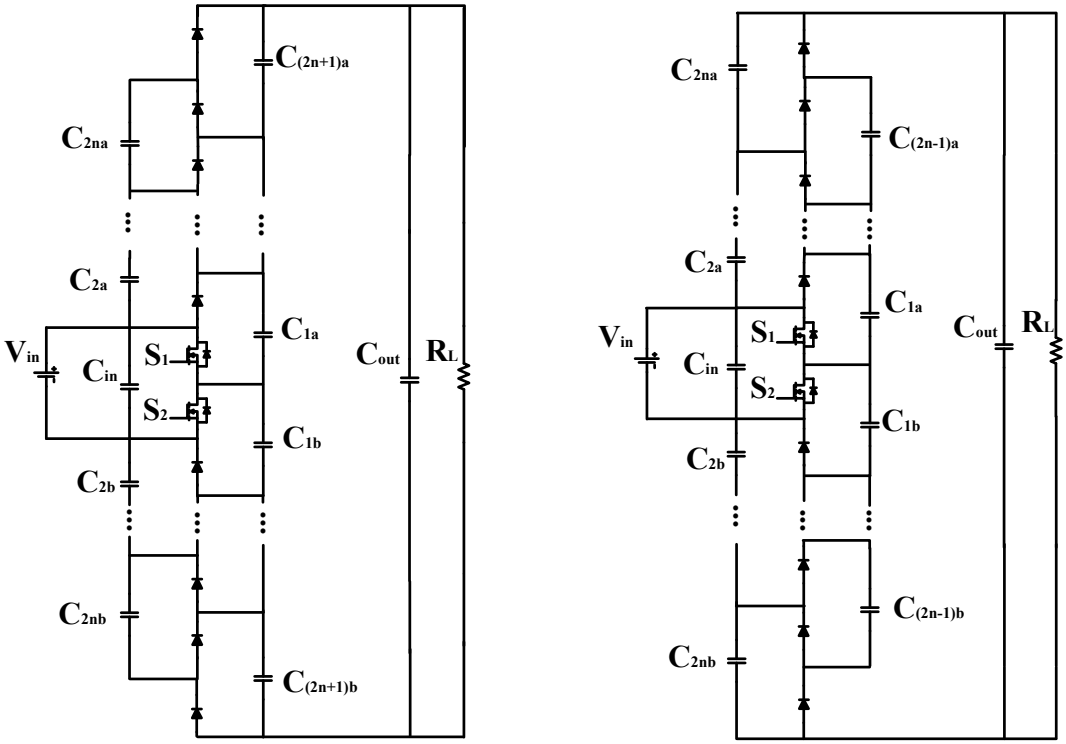
The ideal voltage gain for even-order TBSC can be expressed as:

$$Gain = 2n(n = 1, 2, 3...) \quad \textbf{(3.1)}$$

The ideal voltage gain for odd-order TBSC can be expressed as:

$$Gain = 2n + 1(n = 1, 2, 3...) \quad \textbf{(3.2)}$$

The major difference between even order and odd order TBSC is whether the input source participates in building up the output voltage or not.



(a) (b)

Figure 3.10. Topology of high-order TBSC (a) Even-order (b) Odd-order

3.3 Extensions for bi-direction and step-down conversion

3.3.1 Bidirectional TBSC

The nX TBSC topology can be modified to realize bidirectional power flow by replacing all the diodes with switches. For example, the nX TBSC has its bidirectional version as shown in Figure 3.11. Either of the voltage sources V_L and V_H can be used as the input source.

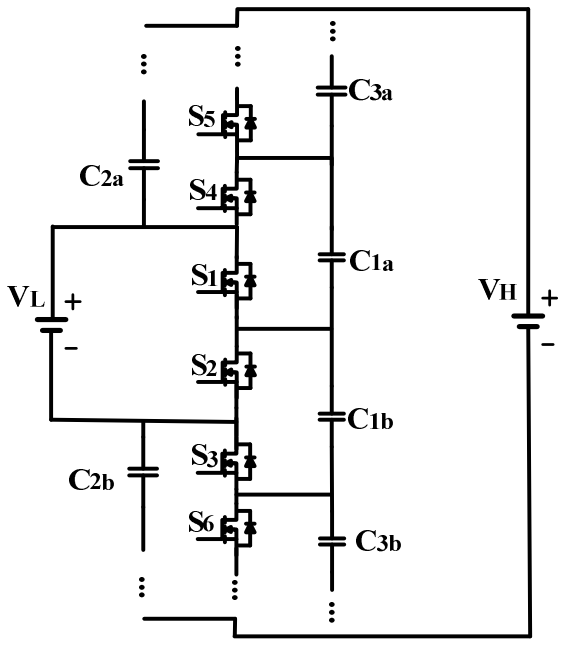


Figure 3.11 Extensions of TBSC for Bi-directional application

If a voltage source is connected at low side and load is connected at high side, only S_1 and S_2 are required to be trigged to deliver power from source to load. If the source is connected at high side and load at low side, S_3, S_5… and S_4, S_6… should be triggered separately by the interleaved PWM signal to deliver power from high side to low side. However, if both sides are connected with voltage sources, the group of S_1, S_3, S_5,… and

the group of S_2, S_4, S_6,… should be triggered by interleaved PWM signals respectively. The duty cycle and frequency can be used to control the direction of charging current.

3.3.2 Buck-mode (Step down) TBSC

To derive the buck version of nX TBSC, the diodes in nX TBSC topology are replaced by switches while the switches by diodes. The power source is connected at high side and the load is connected at low side. The result is shown in Figure 3.12. Generally, in a Buck-mode nX TBSC, the switches with odd number as subscript are triggered by the pulses labeled S_1, while the ones with even number as subscript, by the pulses labeled S_2 as shown in the two top curves in Figure 3.8.

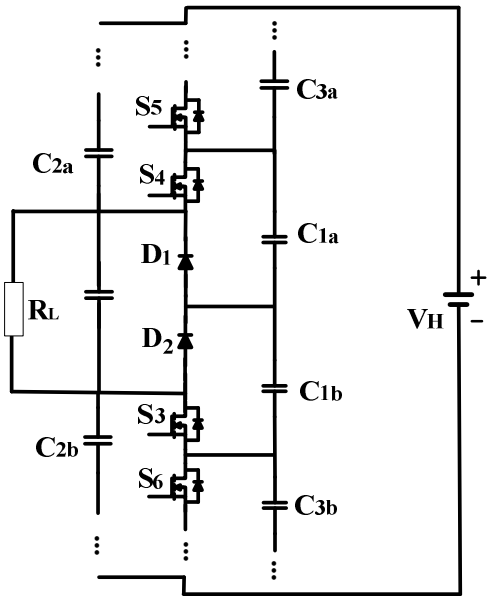


Figure 3.12 Extensions of TBSC for Step-down application

3.4 Summary

In this chapter, the topology development and extensions of TBSC family are discussed. The operational principle is illustrated by designed interleaved PWM driving signals. Based on simple control and selection of converter stages, different voltage gain can be achieved to meet different application requirements. Moreover, the power bidirectional and voltage step-down are possible based on simple modification of circuit components. The in-depth investigation of circuit model and verification of circuit performance will be discussed in the following chapters.

Chapter 4 Modeling of TBSC

Modeling of switched capacitor is essential to gain full understanding of switched capacitor converter. In this Chapter, a Charge-balance Transient-Calculation (CT) modeling technique is developed to analyze the steady state behavior of TBSC. The voltage gains of 2X TBSC and 3X TBSC are derived respectively in section 4.1 and 4.2. The model result not only predicts the impact of circuit parameters such as load resistor, input voltage, and duty cycle, but also reveals the effect of flying capacitance and switching frequency on the output voltage, which was not identified by traditional methods.

In order to provide design guidelines for high power switched capacitor design, CT modeling results are used to analyze the circuit current stress of 3X TBSC in section 4.3. In section 4.4, the small signal model of 3X TBSC is derived using traditional approach to facilitate regulation issue analysis.

4.1 Modeling of 2X TBSC

In this section, the modeling process using CT method for 2X TBSC is investigated. The operational states in Figure 3.6 are simplified to their equivalent circuits, shown as Figure 4.1. Some assumptions are made during calculation as follows:

(1) The load current I_{out} is assumed to be constant which equals to V_{out}/I_{out}. The reason to model the load as a current source is based on two unique properties of the proposed structure. First, there is no high voltage rating output capacitor. Thus, only a resistor is

connected to output, which consumes nearly a constant current from flying capacitors. Second, the symmetrical structure and interleaved PWM control make the converter operate with small output voltage ripple condition.

(2) The flying capacitors are assumed to have the same capacitance C. As film capacitors are adopted, a small equivalent serial resistance (ESR) r is assumed for each capacitor. Also, S_1 and S_2 have the same "on-resistance" R_{on}. Diodes are modeled as voltage source V_d in series with a resistor r_d.

(3) Some simplifications are made based on: $r_d << R_L$, $R_{on} << R_L$, $V_d << V_{in}$, $r << R_{on}$.

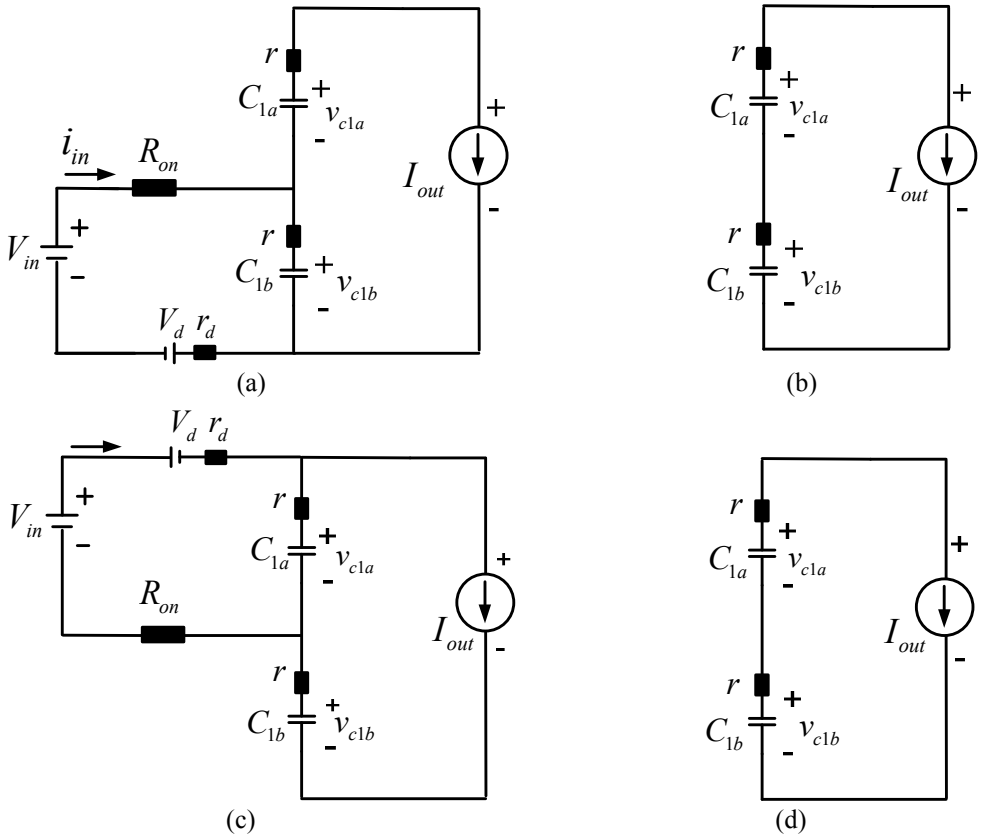


Figure 4.1 Equivalent circuits of different states for 2X SC converter

(a) State 1[0, dTs]. (b)State 2[dTs,Ts/2] (c) State 3[Ts/2,(d+1/2)Ts].(d) State 4[(d+1/2)Ts, Ts].

In Figure 4.1(a), this is the only state that capacitor C_{1b} is charged. Therefore, the voltage of C_{1b} will rise from its minimum value V_{c1bmin} to peak value V_{c1bmax} during [0, dTs], as depicted by voltage waveform V_{c1b} in Figure 3.5. By applying the KVL on circuit state 1 shown as Figure 4.1(a), the following equation can be obtained:

$$V_{in} = (I_{out} + C\frac{dV_{c1b}(t)}{dt})(R_{on} + r_d) + rC\frac{dV_{c1b}(t)}{dt} + V_{c1b} + V_d \quad \textbf{(4.1)}$$

According to the boundary condition $V_{c1b}(0) = V_{c1bmin}$, the following result can be derived:

$$V_{c1b\max} = V_{c1b}(dT_s) = (V_{c1b\min} - V_m)e^{-\frac{dT_s}{(r+R_{on}+r_d)C}} + V_m \quad \textbf{(4.2)}$$

where $V_m = V_{in} - V_d - I_{out}(R_{on} + r_d)$.

Due to the automatic interleaved configuration, C_{1a} and C_{1b} have interleaved voltage ripple with same amplitude. As a result, the output voltage can be approximated as following:

$$V_{out} = V_{c1b\max} + V_{c1b\min} \quad \textbf{(4.3)}$$

During time interval [dTs, Ts], C_{1b} is discharging with current I_{out}, causing its voltage dropping from V_{c1bmax} to V_{c1bmin}. Based on charge balance principal, the following equation can be obtained:

$$C(V_{c1b\max} - V_{c1b\min}) = I_{out}(1-d)T_s \tag{4.4}$$

According to (4.2), (4.3), (4.4) and note that $\mathrm{I_{out}} = \frac{\mathrm{V_{out}}}{\mathrm{R_L}}$, the voltage gain of 2X TBSC can be derived. Typically, as $\mathrm{r_d}, \mathrm{R_{on}} \ll \mathrm{R_L}, \mathrm{V_d} \ll \mathrm{V_{in}}$, the simplified voltage gain equation is derived as following:

$$\frac{V_{out}}{V_{in}} = \frac{2R_L C(1-e^{-\frac{dT_s}{RC}})}{(1-d)T_s + R_L C + [(1-d)T_s - R_L \mathrm{C}]\mathrm{e}^{-\frac{dT_s}{RC}}} \tag{4.5}$$

where $R = R_{on} + r_d + r$.

According to the equation (4.5), if $\mathrm{R_L} = \infty$, the voltage gain of 2X TBSC will reach its ideal condition value:

$$\lim_{R_L \to +\infty} \frac{V_{out}}{V_{in}} = 2 \tag{4.6}$$

It indicates the converter can reach its idea gain under no load condition when voltage drop of diodes is neglected.

4.2 Modeling of 3X TBSC

The similar modeling method of 2X TBSC converter can be applied to 3X TBSC converter. The equivalent circuit of operation states in Figure 3.9 is given as Figure 4.2. However, the 3X TBSC converter has coupling loops which can affect each other and increase the difficulty to derive voltage gain formula. For instance, in Figure 4.2(a), C_{2a} and C_{1b} are charged at the same time within loop 1 and loop 2 respectively, which share a

common switch S_1. Solving the differential equations in time domain will make the problem complicated. A way to simplify calculation is loop decoupling technique.

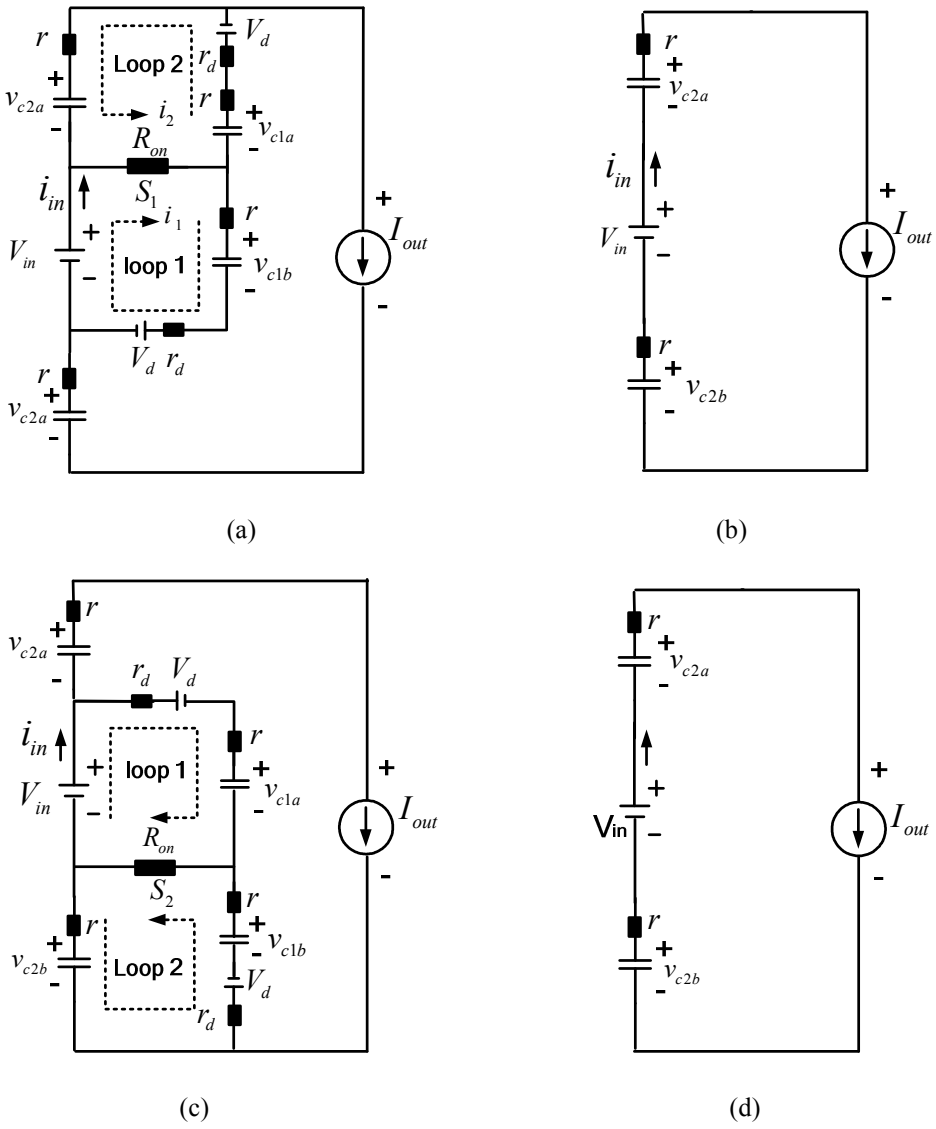


Figure 4.2 Equivalent circuits in different modes for 3X TBSC converter

(a) State 1[0, dTs]. (b)State 2[dTs,Ts/2] (c) State 3[Ts/2,(d+1/2)Ts].(d) State 4[(d+1/2)Ts, Ts].

4.2.1 Complex coupling Loop

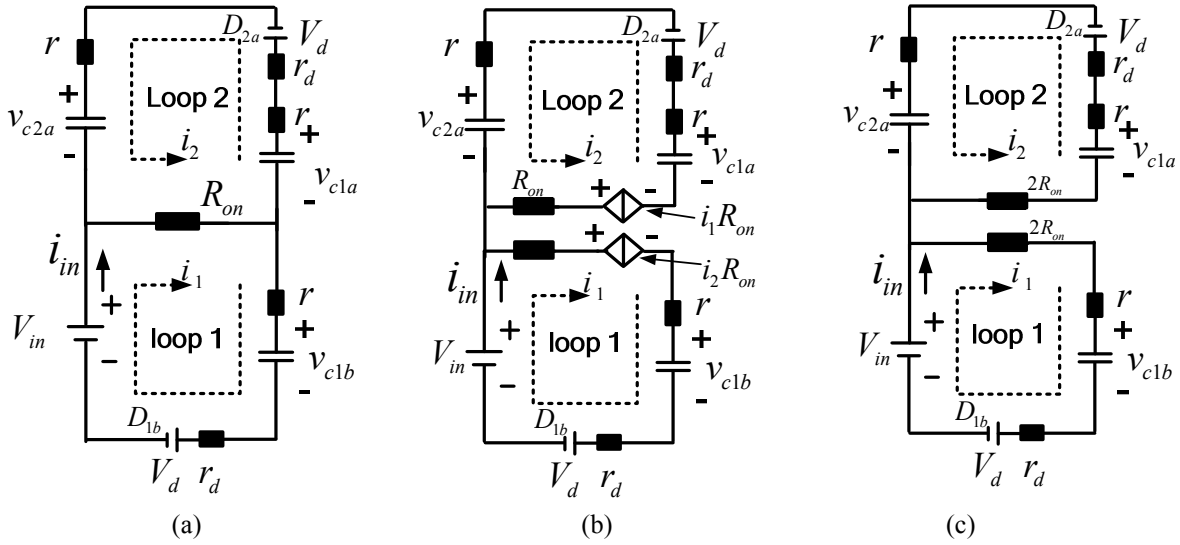


Figure 4.3 Loop decoupling procedure

Figure 4.3 shows the loop decoupling procedure of two coupled loops shown in Figure 4.2(a). The loop 2 has a loop current i_2 equal to the current flowing though diode D_{2a} and i_1 is the current flow through D_{1b}. The loop current i_1 will cause extra voltage drop i_1R_{on} along loop 2, thus a current controlled voltage source is installed in decoupled loop 2 as shown in Figure 4.3(b).

Due to the charge balance of flying capacitors, the average current of D_{2a} and D_{1b} is equal to load current. Since conducting periods of both diodes are the same, i_1 can be approximated the same as i_2. Thus the current controlled voltage source can be further replaced by resistor R_{on}. The final decoupled loops are shown as Figure 4.3(c).

With the decoupled loops, the circuit transient calculation equations can be derived much easier.

4.2.2 Accurate Steady State Model Derivation of 3X TBSC

In Figure 4.2(c), loop 1 and loop 2 can be decoupled similarly as Figure 4.3 due to symmetry. C_{1a} is charged from V_{c1amin} to V_{c1amax} through loop 1. Solving the differential equation based on its decoupled loop 1, the following equation is derived:

$$V_{c1a\max} = V_{in} + e^{-\frac{dT_s}{R_1 C}}(V_{c1a\min} - V_{in} + V_d) - V_d \tag{4.7}$$

where $R_1 = 2R_{on} + r_d + r$.

Assume C_{2a} is charged from C_{2amin} to C_{2amax} in Figure 4.2(a) by loop 2. Solving the differential equation based on decoupled loop 2 as shown on top of Figure 4.3(c), the following equation can be derived:

$$V_{c2a\max} = \frac{V_{c1a\max} + V_{c2a\min} - V_d - \frac{I_{out}R_2}{2} - \frac{I_{out}dT_s}{C}}{2} - \frac{V_{c1a\max} - V_{c2a\min} - V_d - \frac{R_2 I_{out}}{2}}{2} e^{-\frac{2dT_s}{CR_2}} \tag{4.8}$$

where $R_2 = 2R_{on} + r_d + 2r$.

As all the charge delivered to load will be first stored in C_{1a} during each switching period, the following equation can be derived based on the charge balance principal:

$$(V_{c1a\max} - V_{c1a\min})C = I_{out}T_s \tag{4.9}$$

The voltage of C_{2a} drops from V_{2amax} to V_{2amin} during state 2, 3 and 4, thus the following equation is derived:

$$(V_{c2a\max} - V_{c2a\min})C = I_{out}(1-d)T_s \tag{4.10}$$

At the meantime, V_{c2b} has the same voltage ripple as V_{c2a} with interleaving configuration. Thus, the output voltage can be approximated as following:

$$V_{out} = V_{c2a\max} + V_{c2a\min} + V_{in} \tag{4.11}$$

In this dissertation, film capacitors are adopted. ESR is small compared with R_{on}. In order to simplify the final voltage gain formula, the following approximation for general loop resistance is made:

$$R_1 \approx R_2 = R \tag{4.12}$$

Based on equations (4.7) ~ (4.12) and with regard to the condition $V_d \ll V_{in}, I_{out} = \frac{V_{out}}{R_L}$, the final voltage gain equation can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{3CR_L(1-e^{-\frac{2dT_s}{RC}})}{-(CR_L + dT_s - 3\mathrm{T}_s + \mathrm{RC})e^{-\frac{2dT_s}{RC}} + 2T_s e^{-\frac{dT_s}{RC}} + RC + CR_L - dT_s + 3\mathrm{T}_s} \tag{4.13}$$

According to equation (4.13), switching period T_s and duty cycle d can be both used to regulate the voltage gain. Besides, loop resistance R, flying capacitance C, and load R_L, all take part in determining the final voltage gain, which is critical to achieve high system efficiency. A general impact of circuit parameters on voltage gain can be described as Figure 4.4 when other parameters are determined.

Unlike the boost converter, the TBSC can work under no load condition. When $\mathrm{R_L} = \infty$, the following result can be derived:

$$\lim_{R_L \to +\infty} \frac{V_{out}}{V_{in}} = \frac{3CR_L(1-e^{-\frac{2dT_s}{RC}})}{CR_L(1-e^{-\frac{2dT_s}{RC}})} = 3 \tag{4.14}$$

In order to explore regulation issue, the voltage conversion ratio of equation (4.13) is plotted in three dimensions as function of duty cycle and frequency, shown as Figure 4.5. Other circuit parameters are fixed in Table 4.1.

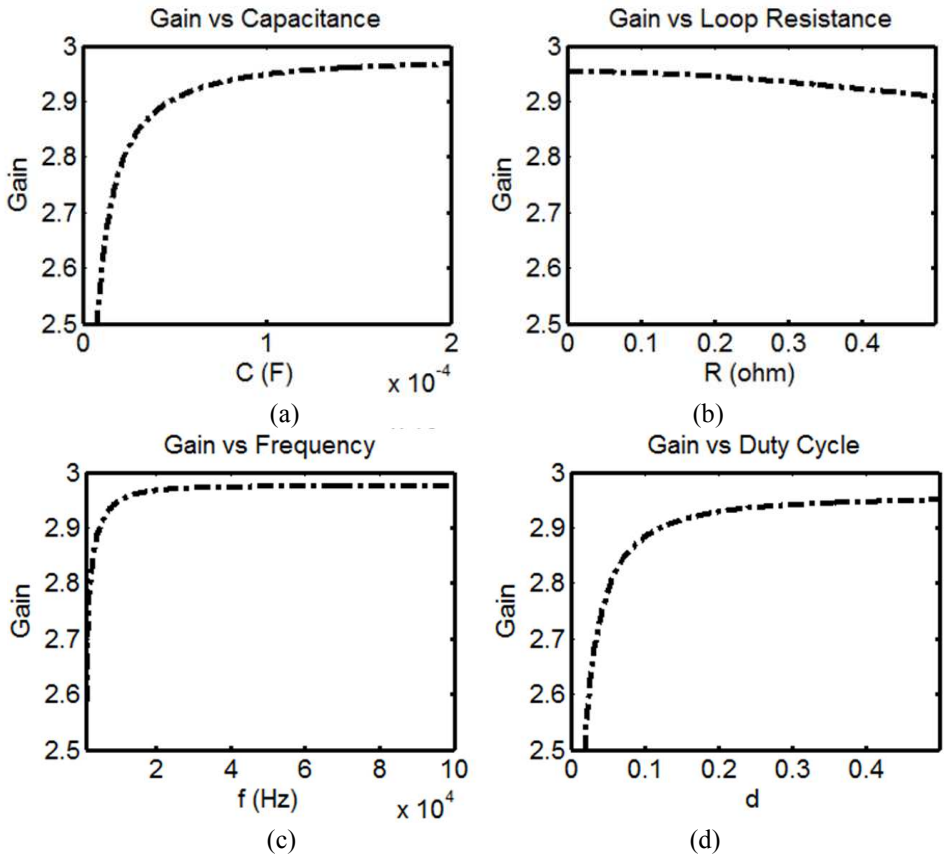


Figure 4.4 General impact of circuit parameters impact on voltage gain of 3X TBSC

(a) Flying Capacitor Impact (b) Loop resistance impact (c) Frequency impact (d) Duty Cycle impact

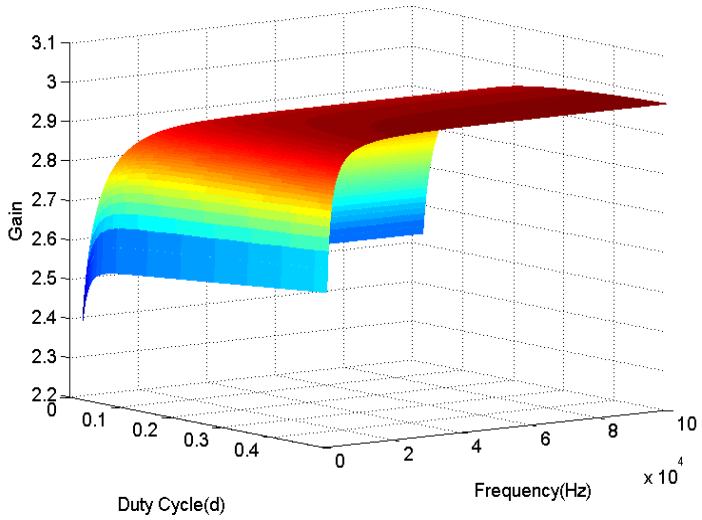


Figure 4.5 3X TBSC voltage gain as function of frequency and duty cycle

Table 4.1 Circuit Parameters of 1kW 3X TBSC

Circuit parameters	Value
R_L	160Ω
V_{in}	100V
r	10m Ω
R_{on}	70m Ω
V_d	0.78V
C	100uF

At the meantime, the following useful voltage boundaries of flying capacitors can be derived based on equations (4.7) ~ (4.12):

$$V_{c1a\max} = \frac{-C(-1+a)(R+R_L)(V_d - V_{in}) + ((1+d+2b-3a+da)V_d - (d+b-3a+da)V_{in})T_s}{C(-1+a)(R+R_L) - (-3+d-2b-3a+da)T_s} \quad \textbf{(4.15)}$$

$$V_{c1a\min} = \frac{-C(-1+a)(R+R_L)(V_d - V_{in}) + ((-3+d+2b+a+da)V_d - (-3+b+d+da)V_{in})T_s}{C(-1+a)(R+R_L) - (-3+d-2b-3a+da)T_s} \quad \textbf{(4.16)}$$

$$V_{c2a\min} = \frac{-C(-1+a)(R_L V_d + RV_{in}/2 - R_L V_{in}) + (2(1-d)(a-1)V_d - (d+b+3a-2ad)V_{in})T_s}{C(-1+a)(R+R_L) - (-3+d-2b-3a+da)T_s} \quad \textbf{(4.17)}$$

where $a = e^{\frac{2dT_s}{RC}}$, $b = e^{\frac{dT_s}{RC}}$.

4.2.3 Peak Current Analysis of 3X TBSC

The CT modeling result not only reveals the characteristic of duty cycle and frequency regulation property of switched capacitor converter, it is also suitable to analyze the circuit stress for high power design due to it transient calculation property.

Due to the coupled loop effect, to derive the expression of peak current is difficult based on calculation through precise differential equations within the circuit. Moreover, when switch S_1 is turned on as shown in Figure 4.2(b), there is a slight delay between the conduction of D_{2a} and D_{1b}, shown as Δt in Figure 4.5. The reason is the voltage difference between two flying capacitors C_{1a} and C_{2a} is larger than that of V_{in} and C_{1b}, which causes a rush current in loop 2, leading to the voltage drop on R_{on} high enough to block D_{1b}. When the rush current deceases, voltage drop on R_{on} decreases gradually and D_{1b} starts to conduct together with D_{2a}. Therefore, the charging current of C_{1b} exhibits a soft rising edge, described as positive part of I_{c1a} in Figure 4.6.

The two coupled loops in Figure 4.3(c) are defined as one charging loop (loop 1) where C_{1b} is charged and one discharging loop (loop 2) where C_{1a} is discharged. The current waveforms of two coupled loops can be described by the positive part and negative part of current I_{c1a} in Figure 4.6 for the sake of symmetry.

In discharging loop, the peak current can be estimated by equation (4.18), since this peak current occurs before its coupled loop starts conducting:

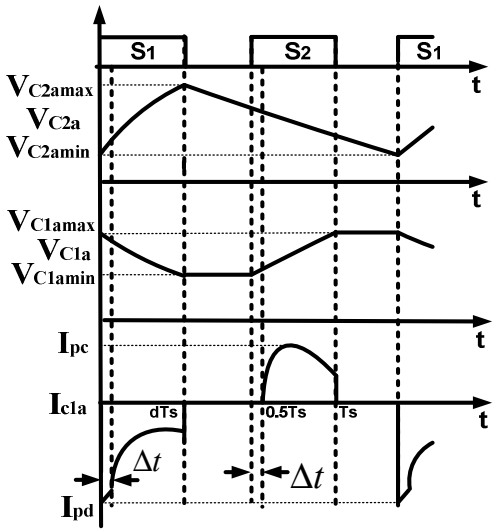


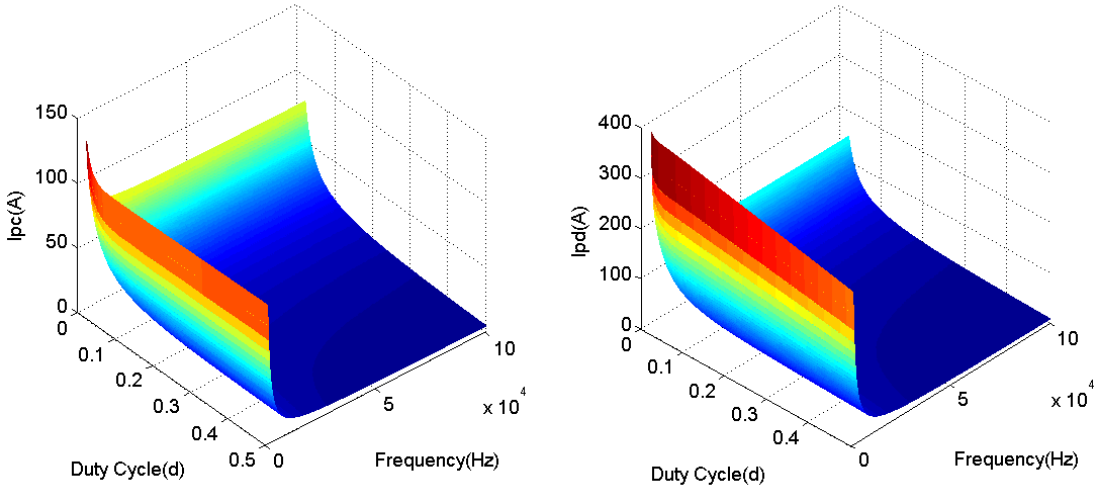
Figure 4.6 Transient voltages of capacitor C_{1a}, C_{2a} and transient current of C_{1a}.

$$I_{pd} = \frac{V_{c1a\max} - V_{c2a\min} - V_d}{R_{on} + r} \tag{4.18}$$

For the charging loop, which can be presented as loop 1 in Figure (a), the peak current occurs when both loops are conducted. Therefore, the equivalent loop resistance is used for peak current estimation:

$$I_{pc} = \frac{V_{in} - V_{c1a\min} - V_d}{R} \tag{4.19}$$

In order to examine the duty cycle and frequency effect on peak currents of charging and discharging loops, equations (4.18) and (4.19) are plotted as function of duty cycle and frequency in Figure 4.7. The other circuit parameters are adopted as Table 4.1. According to the figure, sufficient large switching frequency is preferred to suppress peak current stress both in charging and discharging loops, especially for high power design.



(a) (b)

Figure 4.7 Peak current as function of frequency and duty cycle

(a) Charging loop I_{pc} (b) Discharging loop I_{pd}

4.2.4 Small Signal Model of 3X TBSC

Although the voltage gain shows dependency on both switching frequency and duty cycle, the frequency regulation is still unrealistic due to large current stress when the frequency is low. In higher frequency range, the duty cycle regulation capability is more prominent than frequency regulation, according to Figure 4.5. Therefore the duty cycle regulation is adopted for the closed loop design with a sufficient high switching frequency.

The averaged state-space equations of 3X TBSC converter can be written as:

$$\begin{aligned} \dot{x} &= A_{av}x + B_{av}u \\ x &= [v_{c1a}, v_{c2a}, v_{c1b,}, v_{c2b}]^T \\ u &= v_{in} \end{aligned} \tag{4.20}$$

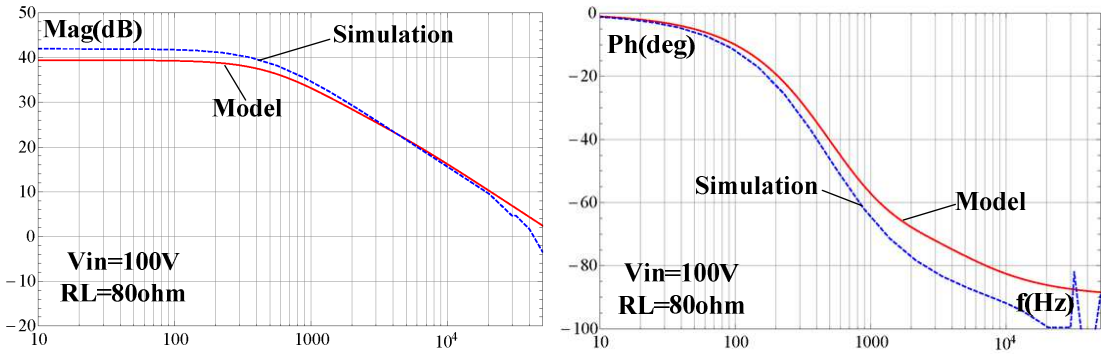
where:

$$A_{av}=\begin{bmatrix} -\frac{2d}{C(r+2R_{on})} & \frac{d}{C(r+2R_{on})} & 0 & 0 \\ \frac{d}{C(r+2R_{on})} & \frac{-dR_L-r-2R_{on}}{C(r+2R_{on})} & 0 & 0 \\ 0 & 0 & \frac{-2d}{C(r+2R_{on})} & \frac{d}{C(r+2R_{on})} \\ 0 & -\frac{1}{CR_L} & \frac{d}{C(r+2R_{on})} & \frac{-r-dR_L-2R_{on}}{R_L\,C(r+2R_{on})} \end{bmatrix},\quad B_{av}=\begin{bmatrix} \frac{d}{C(r+2R_{on})} \\ -\frac{1}{CR_L} \\ \frac{d}{C(r+2R_{on})} \\ -\frac{1}{CR_L} \end{bmatrix}$$

By using standard perturbation, the small signal model can be derived. The final analytical expression is not presented due to its tedious expression. However, the numerical transfer functions under d=0.17, R_L=80 Ω and other parameters given as default in Table 4.1 can be derived as follows:

$$G(s)=\frac{416378\times(1.18332\times10^{12}+4.9333910^{8}s+41975.3s^{2}+s^{3})}{(5.26285\times10^{15}+3.67329\times10^{12}s+7.85742\times10^{8}s^{2}+50620.4s^{3}+s^{4})} \qquad \textbf{(4.21)}$$

It is compared with simulation result derived from PSIM in Figure 4.8. The small deviation between model prediction and simulation result is expected with regarding to loop decoupling approximation during small signal model derivation process.



(a) (b)

Figure 4.8. Comparison between model (solid, red) and PSIM simulation (dashed, blue)

(a)Magnitude (b) Phase

It can be seen the small signal mode of 3X TBSC is similar to a first order system which can achieve comprehensive stability. Due to constrain of switching frequency in high power condition, a simple PI controller is needed to restrict system bandwidth and reduce steady state error. The PI parameters are selected using the MATLAB SISO tool by setting the close loop bandwidth at 1 kHz and placing the zero of compensator at the position of low frequency pole of circuit open loop system, therefore we get:

$$C_c = 0.005+100/\mathrm{s} \tag{4.22}$$

After compensation, the loop gain bandwidth is shrined from around 50 kHz to 1 kHz, as shown in Figure 4.9. In experimental condition, 40 kHz switching frequency is adopted which is 40 times of circuit bandwidth.

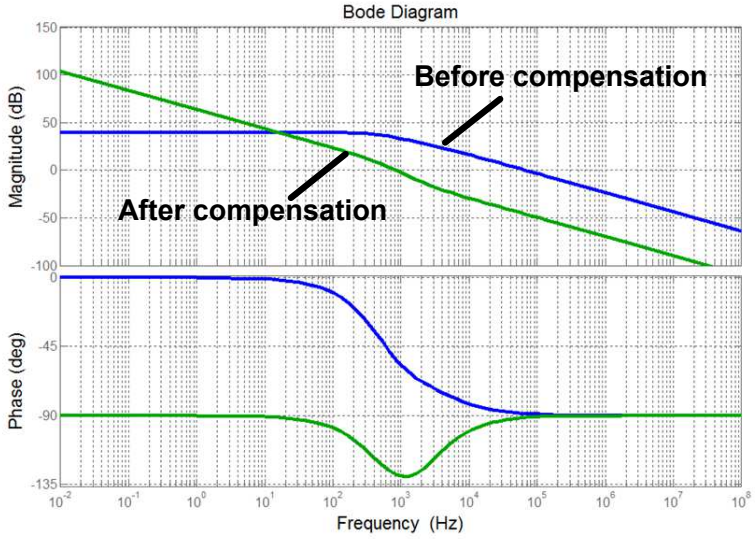


Figure 4.9 T. Loop gain Bode plot comparison before and after compensation

4.3 Summary

In this chapter, a Charge-balance Transient-calculation modeling method is explored to model the TBSC converters. Based on the modeling results, comprehensive circuit parameters impacts on converter voltage gain are clarified. Frequency and duty cycle regulation possibilities are confirmed.

For high power design, the CT modeling method is used to analyze the current peaks in charging and discharging loops, which can provide more guidelines in component selection. Based on the peak current model, it's challenging to use frequency regulation for high power application due to current stress concerns.

To demonstrate some moderate regulation capability under high power condition, the small signal model for 3X TBSC is derived to facilitate duty cycle regulation when sufficient large switching frenemy is chosen. The simulation and experimental verifications will be provided in Chapter 6.

Chapter 5 Performance Analysis of TBSC

In this chapter, the TBSC topology performance is evaluated in the aspects of component count, components stress and output ripple. Brief comparison with selected previous topologies is carried out to support the claimed advantages. The advantages of proposed TBSC family include (1) Voltage boosting with only two active switches, (2) Natural interleaving achieved with all associated benefits such as low input current ripple, small output voltage ripple, (3) All circuit components require low voltage rating, and (4) Flexible gain extension.

5.1 Comparison with Previous Step-up SC Converters

5.1.1 Component Count

Compared with interleaved SC converter with same voltage boosting capability, the proposed TBSC family has obvious advantage of low component count, low cost and higher power density due to its reduced driving circuits. The component count comparison for TBSC topologies with some previous topologies is given in Table 5.1. The numbers of flying capacitor, active switch and diode for topologies with different voltage gains are listed. According to the table, the proposed topologies have greatly minimized the number of semiconductor components while maintaining interleaving benefits and voltage gain. Thus the cost can be reduced and volume shrunk.

Table 5.1 Components Number Comparison

Topology	Gain under ideal condition	Flying capacitors	Switches	Diodes
Proposed 2X TBSC	2	2	2	2
Proposed 3X TBSC	3	4	2	4
Proposed nX TBSC	n	2(n-1)	2	2(n-1)
Paper[19]	2	2	4	4
Paper[20]	3	4	8	6
Paper[23]	4	8	14	8

5.1.2 Component Stress

Assuming the input voltage at low side is V_{in} and the load current is I_{out}, the components Voltage Stress (VS) and Current Stress (CS) of topologies listed in Table 5.1 is given in Table 5.2.

Table 5.2 Components Stress Comparison

Topology	Gain under ideal condition	Flying capacitors VS	Switches VS	Switches CS(rms)	Diodes VS	Diodes CS(rms)
Proposed 2X TBSC	2	V_{in}	V_{in}	$\frac{I_{out}}{\sqrt{d}}$	V_{in}	$\frac{I_{out}}{\sqrt{d}}$
Proposed 3X TBSC	3	V_{in}	V_{in}	$\frac{2I_{out}}{\sqrt{d}}$	V_{in}	$\frac{I_{out}}{\sqrt{d}}$
Proposed nX TBSC	n	V_{in}	V_{in}	$\frac{(n-1)I_{out}}{\sqrt{d}}$	V_{in}	$\frac{I_{out}}{\sqrt{d}}$
Paper[19]	2	V_{in}	V_{in}	$\frac{0.5I_{out}}{\sqrt{d}}$	V_{in}	$\frac{0.5I_{out}}{\sqrt{d}}$
Paper[20]	3	V_{in}	V_{in}	$\frac{0.5I_{out}}{\sqrt{d}}$	V_{in}	$\frac{0.5I_{out}}{\sqrt{d}}$
Paper[23]	4	V_{in}	V_{in}	$\frac{0.5I_{out}}{\sqrt{d}}$	V_{in}	$\frac{0.5I_{out}}{\sqrt{d}}$

During calculation, average current during switch conducting period is used to calculate RMS current instead of using instantaneous current.

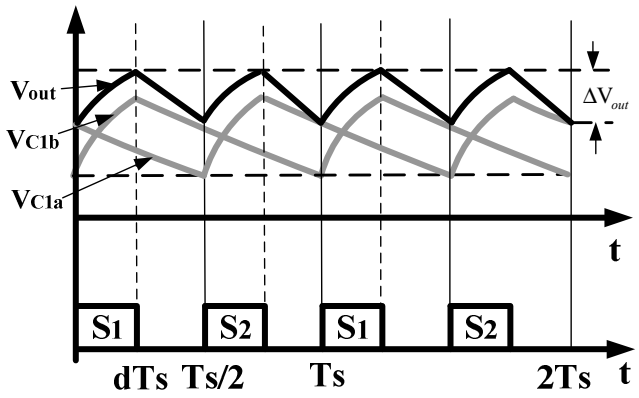
Based on the comparison outlined in Table 5.1 and Table 5.2, the low component count and high power density advantages of TBSC can be identified. Taking the proposed 3X TBSC as an example, it has the same number of capacitors and voltage gain as the converter proposed in paper [20]. However, it has only 6 semiconductor components (switches & diodes) compared with 14 in paper [20]. Although the component current stress of proposed converter is a little higher based on Table 5.2, a smaller converter size still can be expected because the voltage stress is the same and simpler control circuit is required for 3X TBSC.

5.2 Output voltage ripple analysis of TBSC

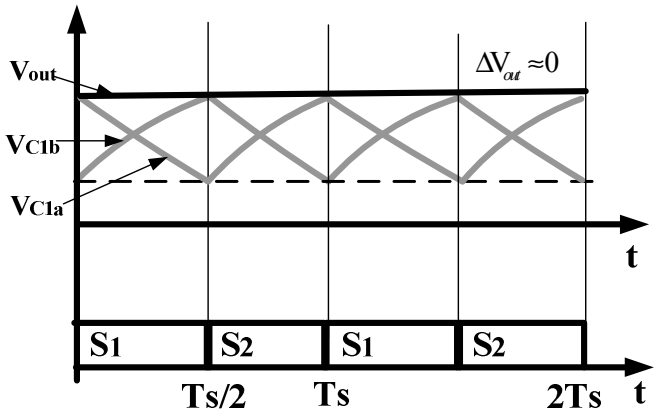
Another benefit of proposed structure is its interleaving characteristic by adopted control signal pattern. Taking 3X TBSC as example, the relationship of output voltage ripple and the ripple of Capacitor C_{1a} and C_{1b} is described as Figure 5.1.

Base on the equivalent circuit shown in Figure 4.1, the quantitative expression of output voltage ripple can be given as follows:

$$\Delta V_{out} = \frac{I_{out}(1-d)T_s + I_{out}(\frac{1}{2}-d)T_s}{C} - \frac{I_{out}\frac{1}{2}T_s}{C} = \frac{(1-2d)T_s}{C} \qquad \textbf{(5.1)}$$



(a)



(b)

Figure 5.1 Relationship of ΔV_{c1a}, ΔV_{c1b} ΔV_{out}

(a) d=0.25. (b) d=0.5.

When the duty cycle d is less than 0.5, as shown in Figure 5.1(a), partial ripple cancelation between C_{1a} and C_{1b} is achieved. However, when the duty cycle reaches its maximum value of 0.5, as shown in Figure 5.1(b), full cancelation can be obtained, leading to nearly zero output voltage ripple.

5.3 Summary

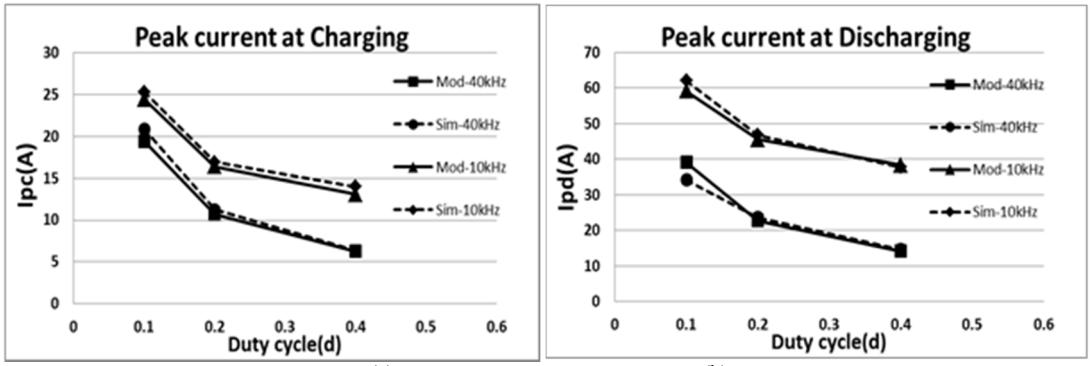
In this chapter, the topology performance of TBSC is briefly investigated by comparison with previous work and quantitatively calculations. The claimed benefits in the topology perspective are confirmed. Further experimental verification will be given in Chapter 6.

Chapter 6 Simulation and Experimental Results of 3X TBSC

The CT modeling result for 3X TBSC and peak current formula were derived in Chapter 4. Circuit performance of 3X TBSC was discussed in Chapter 5. In this chapter, a 1kW 3X TBSC prototype is presented. Extensive simulation and experimental results are provided to verify the theories proposed in above two chapters.

6.1 Simulation verification of CT model and peak current analysis

In order to verify the accuracy of CT method and peak current stress model, the simulation results were compared with the model calculation, with various operation conditions of switching frequency and duty cycle. The results are presented in Table 6.1 and Figure 6.1. The simulation parameters are chosen as default in Table 4.1.



(a) (b)

Figure 6.1 Comparison of peak current model with simulation

(a) Peak current comparison at charging phase (b) Peak current comparison at discharging phase

Table 6.1 Verification of Steady State Model

f(Hz)	d	**Vc1amax (V) (model)**	Vc1amax (V) (sim)	error	**Vc1amin (V) (model)**	Vc1amin (V) (sim)	error	**Vc2amin (V) (model)**	Vc2amin (V) (sim)	error
40k	0.1	**96.7552**	96.79	-0.036%	**96.3082**	96.34	-0.033%	**92.8449**	92.81	0.038%
40k	0.2	**98.0695**	98.09	-0.021%	**97.6143**	97.64	-0.026%	**95.4692**	95.4	0.073%
40k	0.4	**98.7354**	98.76	-0.025%	**98.2762**	98.3	-0.024%	**96.8199**	96.79	0.031%
10k	0.1	**97.3388**	97.51	-0.176%	**95.556**	95.73	-0.182%	**91.8252**	91.71	0.126%
10k	0.2	**98.5718**	98.68	-0.110%	**96.7608**	96.87	-0.113%	**94.1528**	94.12	0.035%
10k	0.4	**99.0839**	99.09	-0.006%	**97.2616**	97.26	0.002%	**95.2374**	95.25	-0.013%
1k	0.1	**99.20**	99.16	0.040%	**83.5066**	83.4	0.128%	**68.4849**	68.4	0.124%
1k	0.2	**99.22**	99.16	0.061%	**83.4411**	83.24	0.242%	**69.9196**	69.7	0.315%
1k	0.4	**99.22**	99.16	0.061%	**83.2716**	82.89	0.460%	**72.8029**	72.4	0.556%

According to Table 6.1, The CT modeling method is confirmed by close agreement between the simulation result and model prediction for boundary voltages of C_{1a} and C_{2a}. Based on Figure 6.1, the peak current model is verified which can provide more design guidelines for engineers in semiconductor components selection for high power switched capacitor converter design.

6.2 Experimental verification

To confirm the feasibility of proposed TBSC topologies, a 1kW 3X TBSC prototype is built as an example design, as shown in Figure 6.2. The components are chosen as Table 6.2.

AVR micro-controller Tiny 24 from Atmel corporation is used to generate the two channel interleaved PWM signals to control the active switches.

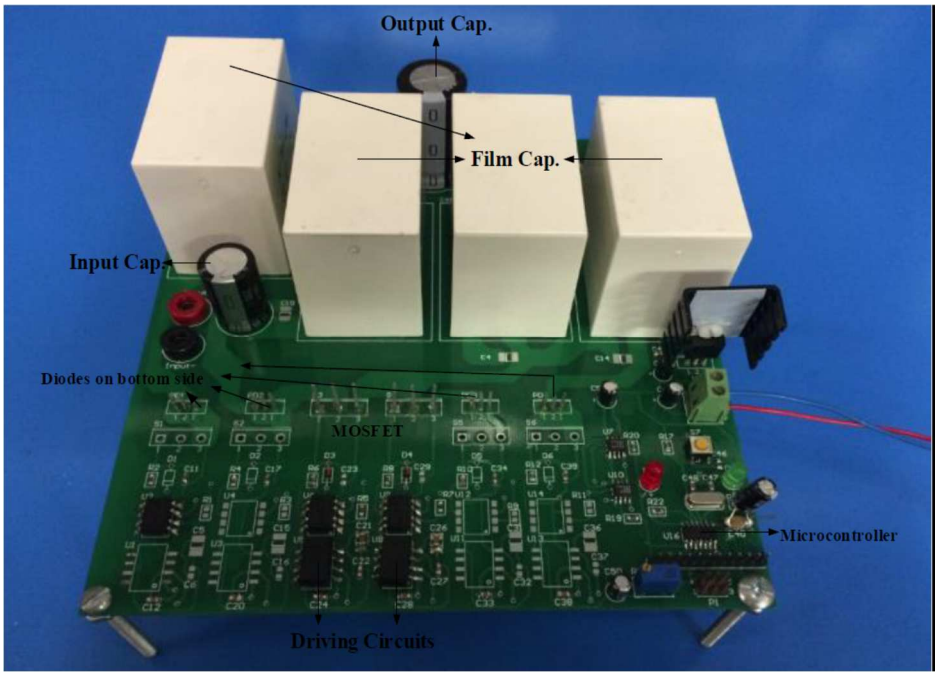


Figure 6.2 Experimental prototype of 1kW 3X TBS

Table 6.2 Parameters of the 3X TBSC Prototypes

Component	Model	Number	Parameter
MOSFETs	FQA40N25	2	Ron=70mΩ
Diodes	STTH2002C	4	Vd=0.78V, rd$\approx$ 10mΩ
Flying Capacitors	Film capacitor(C2AE)	4	100uF（$\pm$5%）, ESR=2.6mΩ (10kHz,70°C)

6.2.1 Duty cycle and frequency modulation verification

In order to investigate the modulation possibilities of 3X TBSC converter, the input voltage is fixed at 40V to make sure input current spike will not exceed component current rating with various switching frequency operation conditions. The modulation capabilities

of duty cycle and frequency on voltage gain of 3X TBSC are tested. The tested conditions are given as Table 6.3.

Table 6.3 Parameter control for modulation testing

Switching Frequency fs (Hz)	Duty cycle d	Load(Ω)	Vin(V)
1k	0.025, 0.05;0.1, 0.45		
4k	0.025, 0.05; 0.1,0.45	160	40
10k	0.025,0.05; 0.1,0.45		

Some typical waveforms of V_{gs}, V_{in}, V_{out} and I_{in} are given in Figure 6.3 under various frequency and duty cycle conditions. The experimental modulation curves based on duty cycle modulation and frequency modulation are compared with model prediction respectively in Figure 6.4 and Figure 6.5. Generally good agreement can be found between model prediction and experimental results, which further demonstrates the CT modeling method.

In Figure 6.4, it demonstrates that when the duty cycle increases, the output voltage goes up correspondingly. The modulation effect is stronger under low duty cycle condition. When the duty cycle is smaller, the voltage gain is farther departing away from the idea gain of three. In Figure 6.4(b), a larger error between model and experiential result appears. It is because the comparison is made under higher switching frequency condition, in which case circuit parasitic parameters start to take more effect on real voltage gain. However, the duty cycle modulation capability is clearly confirmed by experiment.

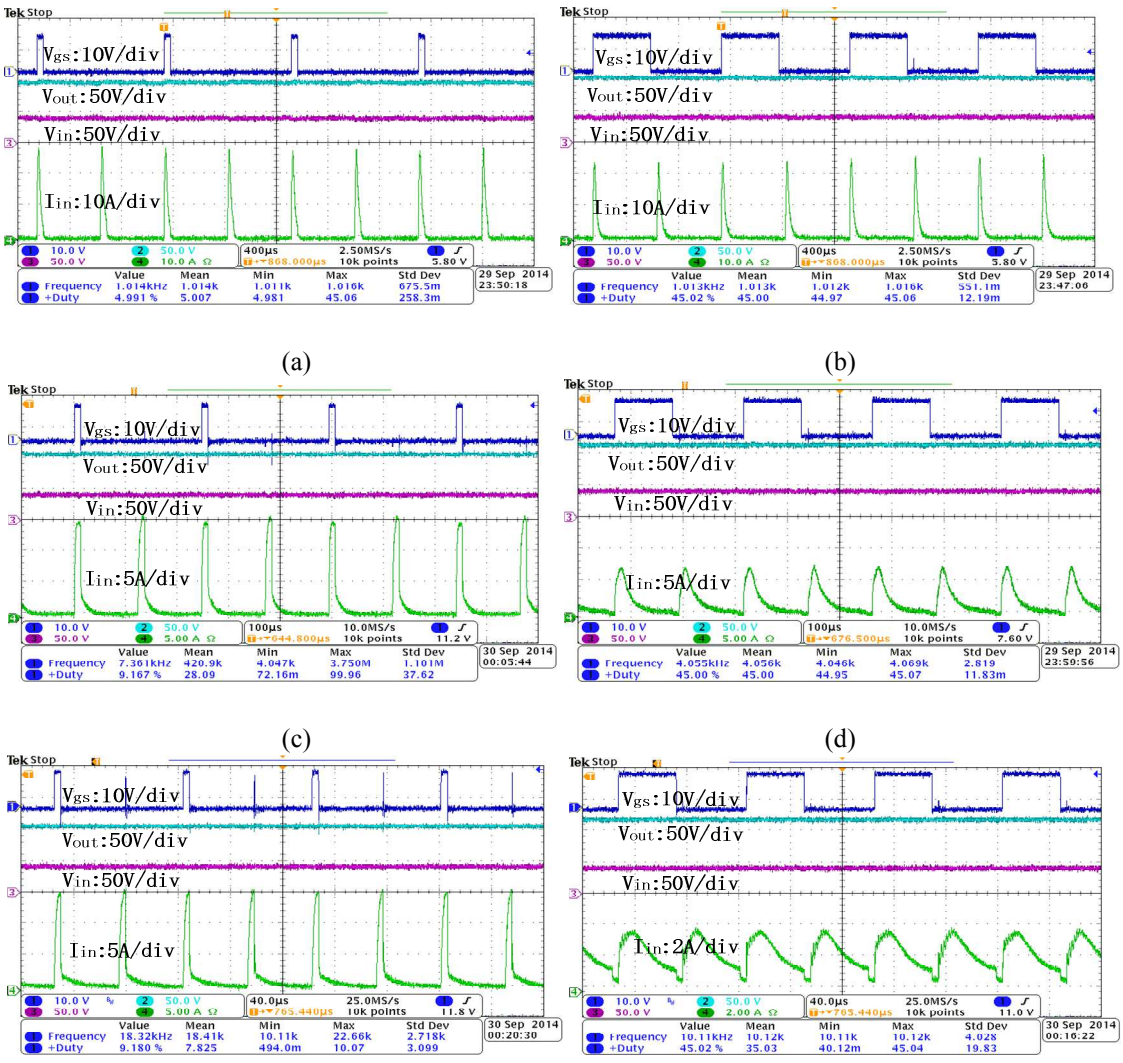


Figure 6.3 Waveforms of V_{gs1}, V_{in}, V_{out} and I_{in}

(a) fs=1kHz, d=0.05 (b) fs=1kHz, d=0.45 (c) fs=4kHz, d=0.05 (d) fs=4kHz, d=0.45

(e) fs=10kHz, d=0.05 (f) fs=10kHz, d=0.45

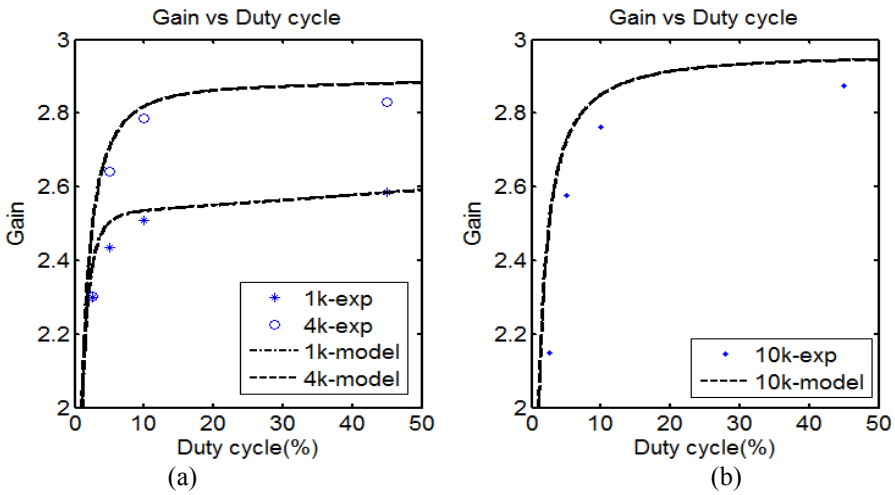


Figure 6.4 Comparison of duty cycle modulation between experiment and model

(a) 1kHz, 4kHz (b) 10kHz

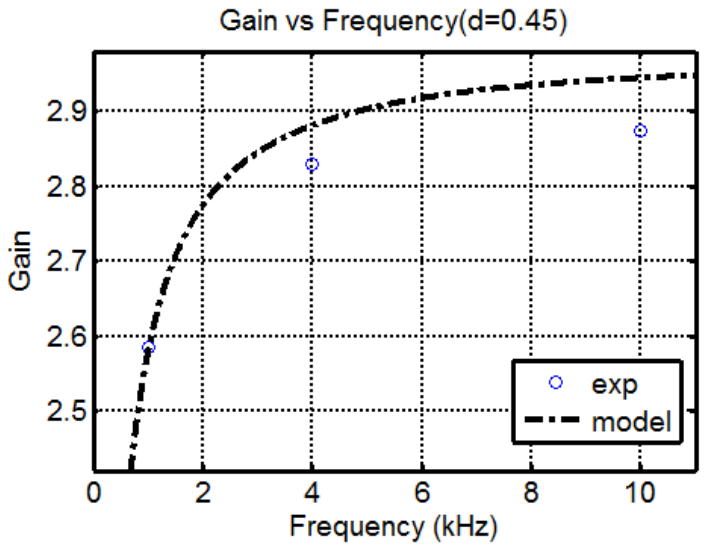


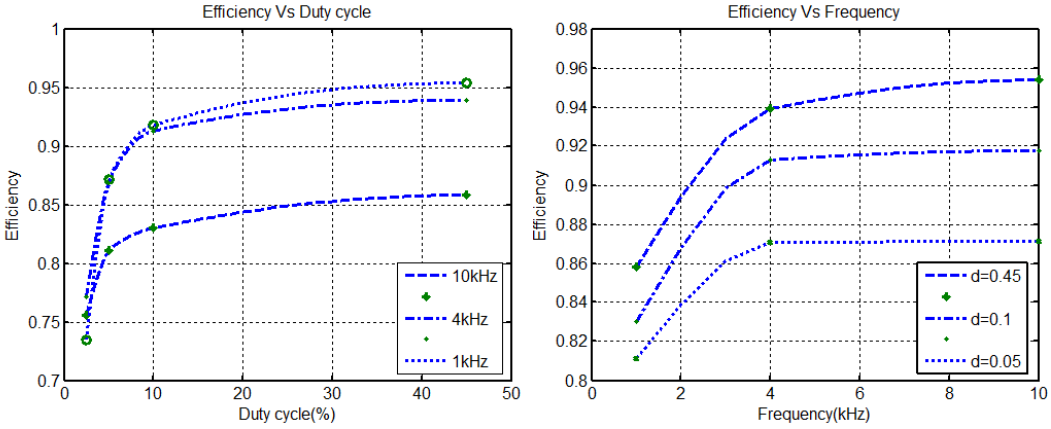
Figure 6.5 Comparison of frequency modulation between experiment and model

In frequency modulation testing case shown as Figure 6.5, the duty cycle is fixed at 0.45. The reason to choose large duty cycle for frequency modulation test is that under low duty cycle condition, increasing frequency will cause the "turn on" time extremely small, which can introduce high testing error due to parasitic parameters.

In the testing condition, the frequency is adjusted from about 1 kHz to 10 kHz. The load is fixed at 160ohm. Figure 6.5 shows when the frequency increases, both model and experimental results show higher voltage gain. Thus, the frequency modulation capability is verified.

6.2.2 Efficiency testing and high efficiency design consideration

Efficiency under various frequency and duty cycle conditions is also tested with V_{in}=40V. The curves of efficiency verse frequency and duty cycle are shown in Figure 6.6(a) and (b).



(a) (b)

Figure 6.6 Relationship between duty cycle and frequency under fixed load

(a)Efficiency vs ducy cycle (b) Efficiency vs frequency

Figure 6.6(a) shows that when the other parameters are fixed, higher duty cycle leads to higher efficiency, which is similar to the voltage gain curve. Figure 6.6(b) shows the efficiency will also increase by increasing the switching frequency. But the curve becomes almost flat when the frequency reaches certain point. It demonstrates that the switching frequency does not have to be very high to reach a good efficiency. The low efficiency

under low duty cycle and low frequency can be explained by some physical phenomena shown in Figure 6.3.

Under low duty cycle condition, the switching loss contributes more in lower efficiency compared with high duty cycle condition. For example, Figure 6.3(a) shows the case when duty cycle is 0.05 while switching frequency is at 1kHz. The input current has been chopped when it hasn't reach zero, which means significant conduction loss will be resulted. But under higher duty cycle condition, such as d=0.45 in Figure 6.3(b), the "turn off" current has been greatly reduced, thus less switching loss occurs.

Under low frequency condition, the conduction loss contributes more for lower efficiency compared with high frequency case. Comparing Figure 6.3(b) and (f), where 1kHz and 10kHz switching frequency are adopted respectively with same duty cycle, it can be found that under 1kHz condition, the input current ripple is much higher. Therefore, much higher conduction loss will occur, leading to lower efficiency.

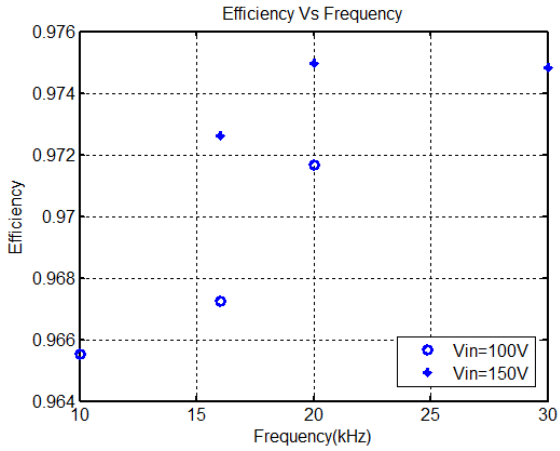


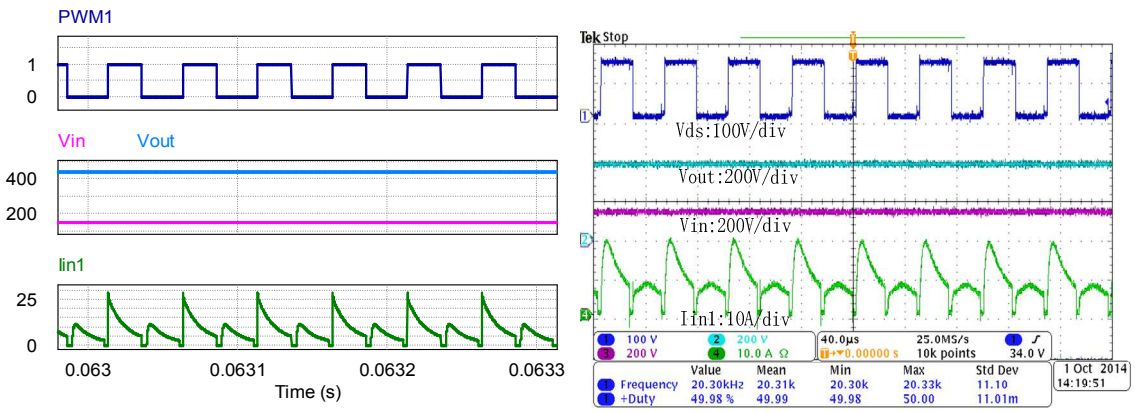
Figure 6.7Effeiciency V.S. Frequency under input voltage of 100V and 150V

According to above analysis, high efficiency can be achieved under maximum duty cycle and sufficiently high frequency condition.

Under high power testing condition, when the input voltage increases, the frequency should increase to avoid the input current spike exceeding an acceptable level. Therefore, two groups of switching frequencies: 10 kHz, 16 kHz, 20 kHz and 16 kHz, 20 kHz, 30 kHz are used for two input voltage testing conditions: 100V and 150V. The tested efficiency points are plotted as dots in Figure 6.7. The maximum efficiency of 97.5% is achieved under 150V input voltage and 20 kHz switching frequency condition.

6.2.3 Soft rising input current

Under the maximum efficiency condition, the circuit key waveforms by simulation and experiment are presented in Figure 6.8. Note that there is a half switching cycle of I_{in1} with soft rising current, which is corresponding to the state in Figure 3.9(c). In this stage, the input current I_{in} equals to I_{in1} plus the load current which is considered constant. Therefore, the input current is considered to have soft rising edge characteristic. During the other half cycle that I_{in1} shows sharp rising input current, as shown in Figure 3.9(a), the input current I_{in} equals to the current of C_{1b} plus load current, which also exhibits soft rising property due to symmetry. Therefore, soft rising input current can be demonstrated. Although some stray inductance may exist in experimental case, the soft rising current still can be clearly identified in simulation case where no stray inductance is involved, as shown in Figure 6.8(a). The soft rising input current property of 3X TBSC makes it more suitable for high power applications.



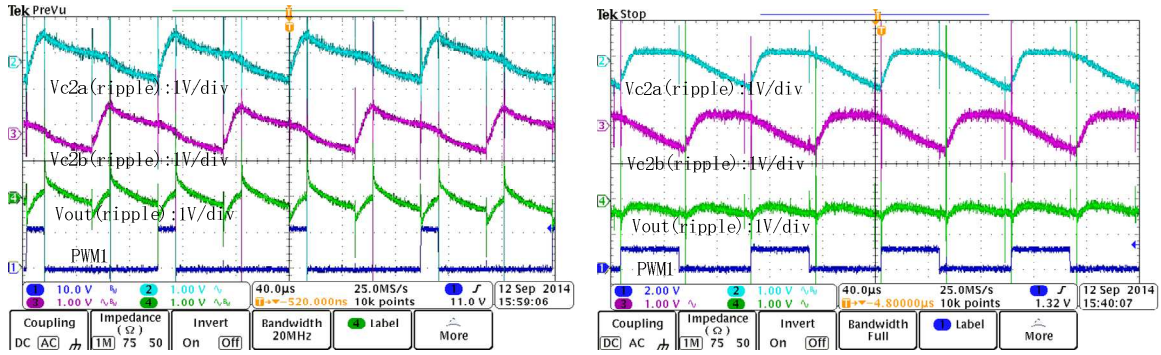
(a) (b)

Figure 6.8 Waveforms of V_{gs1}, V_{in}, V_{out} and I_{in1} under fs=20kHz, d=0.45.

(a) Simulation result (b) Experimental result

6.2.4 Ripple cancelation

As stated previously, the TBSC family has small output voltage ripples. This is due to its natural interleaving operation, which makes the flying capacitors C_{Xa} and C_{Xb} exhibit interleaved voltage ripples. During 3X TBSC experiment, the ripple of C_{2a}, C_{2b} and output voltage under duty cycle of 0.25 and 0.45 are given in Figure 6.9(a) and (b). It can be seen when the duty cycle is small, the output ripple is not fully cancelled but is still smaller compared with the ripple of each flying capacitor. When the duty cycle is controlled at 0.45, the ripple cancellation effect is much more significant. Nearly zero output voltage ripples is achieved. At the meantime, the ripple of flying capacitors also demonstrates that the load can be approximated as current source due to its linear voltage decreasing phenomenon, as shown in Figure 6.9(b).

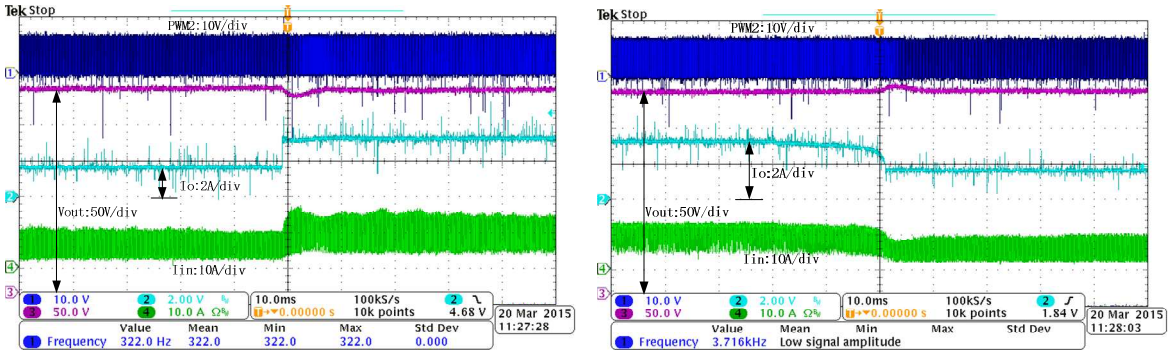


(a) (b)

Figure 6.9 Experimental result of ripple cancelation (a)d=0.25 (b)d=0.45

6.2.5 Close loop operation under load step condition

According to the designed PI controller in Chapter 5, the converter can operate under closed loop condition. The input is fixed at 100V while the output voltage is regulated at 280V. 40kHz switching frequency is adopted. The output power is switched between 1000W and 500W while the output voltage can be maintained constant after small disturbance during load transient. The testing results are shown in Figure 6.10. It can be seen the input current exhibits limited peak current under different load conditions.



(a) (b)

Figure 6.10 Load step with V_{in}=100V, V_{out}=280V

(a) Load step from 160Ω to 80Ω (b) Load step from 80Ω to 160Ω

6.2.6 Summary

In this chapter, extensive simulation and experimental results are provided to verify the theories presented in previous chapters. The accuracy of CT model is verified by simulation and experiment. The peak current model is confirmed by simulation. The high efficiency design for high power 3X TBSC is achieved by adopting maximum duty cycle with sufficient high switching frequency. If certain regulation capability is required, it's preferable to use duty cycle regulation by choosing high frequency, which is supposed to suppress current ripple. In addition, the soft rising input current of 3X TBSC and low output voltage ripple are both demonstrated by experimental results, which confirm the suitability of applying 3X TBSC to high power applications.

Chapter 7 Accurate Modeling Technique of Switched Capacitor Converter

In this chapter, the modeling technique adopted to model the TBSC converter known as Charge-Balance Transient-Calculation (CT) Modeling Method[170] is further investigated in section 7.1. Standardized modeling procedure is presented based on simple interleaved voltage doubler topology. Comparison with several reviewed modeling methods in chapter 2 is carried out in term of equivalent output impedance. The accuracy of CT method is confirmed.

In section 7.2, an enhanced CT modeling method is developed by including output capacitance effect on circuit steady state model. It's more accurate when moderate output capacitor is adopted with noticeable output ripple. In addition, the modeling procedure is extended to non-interleaved dual-phase switched capacitor converters. Its accuracy is verified by simulation and experimental results.

7.1 Charge-Balance Transient-Calculation (CT) Modeling Method

In order to investigate the accuracy issue and constrains of CT modeling method and generalize it to other interleaved SC converters, a simple topology shown in Figure 7.1 is adopted as an example topology for model evaluation and comparison.

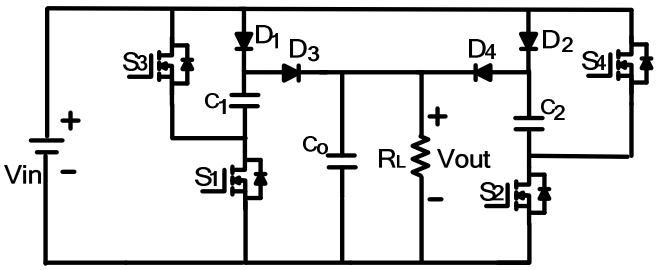


Figure 7.1 A voltage doubler topology proposed in [19]

7.1.1 State Space Average (SSA) Modeling

The State-Space Averaging(SSA) method[171] was developed for traditional inductor-based PWM converters. It is a general method for switching converter modeling. This method was applied to the voltage doubler circuit in Figure 7.1 in paper [19]. According to the SSA method, the voltage gain formula of topology in Figure 7.1 can be calculated as follows:

$$\frac{V_o}{V_{in}-V_d}=\frac{2}{1+(1+\frac{1}{2d})\frac{r+R_{on}}{R_L}} \tag{7.1}$$

where V_d is the voltage drop of all diodes, r is ESR of flying capacitor C_1 and C_2, R_{on} is the "on resistance" of all switches. Equation (7.1) demonstrates that the voltage gain can be regulated by controlling parameter d. At the meantime, the gain curve will be affected by loop resistance $r + R_{on}$ and the load R_L.

The original SSA method is well-suited for conventional inductor-based PWM converter, which has already become an industrialized standard modeling method. This method is applicable also for switching capacitor converters and it yields a general solution. With the special arrangement of switching converters, there is still opportunity to

improve the accuracy for the entire switching frequency range of SC converter. For example, the gain equation of (7.1) is unable to explain the frequency regulation which has been reported in SCC[123], [172]. Moreover, the impact of flying capacitor C_1 and C_2 is not observed. It is critical to establish comprehensive understanding of switching capacitor converter including the frequency regulation and flying capacitor effects on the voltage gain.

7.1.2 Charge-balance Transient-Calculation Modeling

Alternatively, the voltage gain of circuit in Figure 7.1 can be derived based on Charge-balance Transient-Calculation modeling method. The original idea of this method can be found in paper [21], [147], [173] for different purpose. Paper [173] focused on deriving the expression of "on time" in order to achieve adaptive control. Paper [21], [147] didn't adopt the linear discharging approximation for flying capacitors during discharging phase which makes the resulted equation complex. Article [170] synthesizes the previous work and generalized the modeling method as CT modeling technique for interleaved SC converters. At the meantime, it pursuits more physical insights of the regulation issue through duty cycle and frequency for switched capacitor converters. Its accuracy is compared with other recently develop modeling methods.

The operation modes of topology in Figure 7.1 are illustrated as Figure 7.2. Some assumptions are made for calculation simplification: (1)All switches have identical on resistance R_{on}. (2)Flying capacitors C_1 and C_2 have the same capacitance C and Equivalent Series Resistance (ESR) r. (3)All diodes have the same voltage drop $V_{d.}$ (4)The output current is assumed constant at flying capacitor discharging phase.

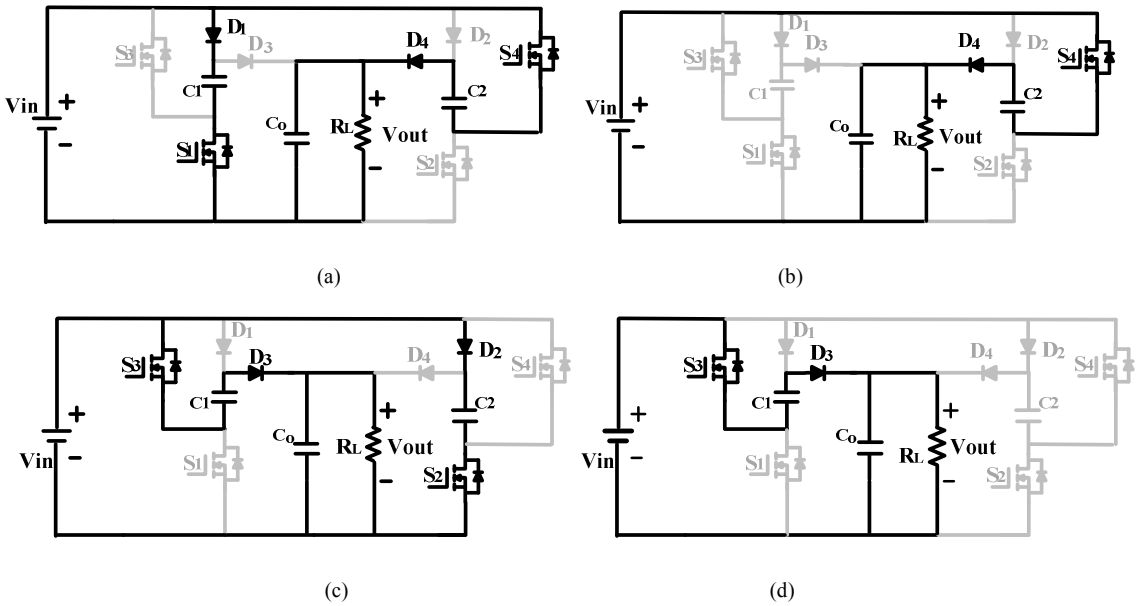


Figure 7.2 Operation modes of voltage doubler topology proposed in [19]

(a) State1 [0, dT_s]. (b) State2 [dT_s, $\frac{T_s}{2}$]. (c) State3 [$\frac{T_s}{2}$, $dT_s+\frac{T_s}{2}$]. (d) State4 [$dT_s+\frac{T_s}{2}$, T_s].

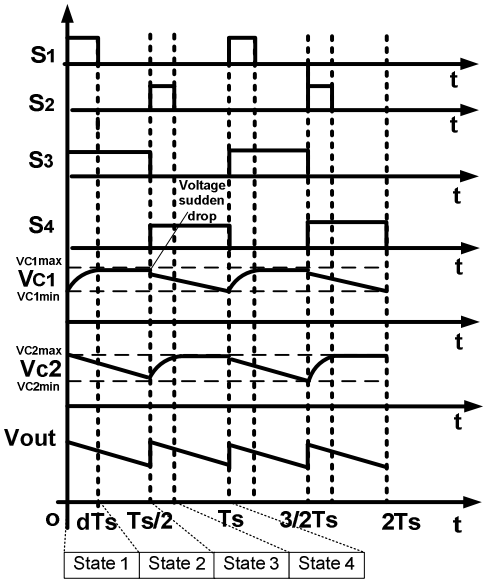


Figure 7.3 Transient waveforms based on CT modeling method

The steps of deriving SC converter voltage ratio are given as following:

1) Transient calculation

The only charging time for C_1 in one switching cycle is [0, dT_s], shown in Figure 7.2(a). The voltage of C_1 rises from V_{c1min} to V_{c1max}, as shown in Figure 7.3. By solving the differential equation based on the charging loop of C_1, it can be derived that:

$$V_{c1\max} = (V_{c1\min} - V_{in} + V_d)\,\mathrm{e}^{-\frac{dT_s}{(r+R_{on})C}} + V_{in} - V_d \tag{7.2}$$

2) Averaging output voltage

Due to the symmetrical configuration, flying capacitors C_1 and C_2 exhibit similar charging and discharging operation modes and the voltage of V_{c1} and V_{c2} have the same maximum and minimum value. The waveform of output voltage is depicted at the bottom of Figure 7.3. Thus the average output voltage can be presented as:

$$V_{out} = V_{in} - V_d - \frac{V_{out}}{R_L}\left(R_{on} + r\right) + \frac{V_{c1\min} + V_{c1\max}}{2} \tag{7.3}$$

3) Charge balance principle

The discharging period of C_1 are shown as Figure 7.2(c) and (d) in one switching cycle. The voltage of C_1 decreases from V_{c1max} to V_{c1min}. The discharging current is assumed constant and is equal to load current. According to charge balance principle, the following equation is got:

$$C_1(V_{c1\max} - V_{c1\min}) = \frac{V_{out}T_s}{2R_L} \tag{7.4}$$

According to equations (7.2)~(7.3), the voltage ratio between input and output is derived as following:

$$\frac{V_{out}}{V_{in}-V_d}=\frac{8CR_L(e^{-\frac{dT_s}{RC}}-1)}{4CR_Le^{-\frac{dT_s}{RC}}+4CRe^{-\frac{dT_s}{RC}}-T_se^{-\frac{dT_s}{RC}}-4CR_L-4CR-T_s} \tag{7.5}$$

where R = R_{on} + r.

7.1.3 Comparison of SSA Model and CT Model

In order to examine the differences between the aforementioned two modeling methods, equation (7.5) is rearranged as:

$$\frac{V_{out}}{V_{in}-V_d}=\frac{2R_L}{R_L+R+\frac{T_s}{4C}\frac{1}{\tanh(\frac{dT_s}{2RC})}} \tag{7.6}$$

Meanwhile, the formula (7.1) based on the traditional SSA modeling method is rearranged as:

$$\frac{V_o}{V_{in}-V_d}=\frac{2R_L}{R_L+R+\frac{1}{2d}R} \tag{7.7}$$

where R = R_{on} + r.

Under the condition of dTs<<2RC, $\coth(\frac{dT_s}{2RC})\approx\frac{dT_s}{2RC}$. The equation (7.6) approaches (7.7). It indicates that under small switching period and large flying capacitor condition, the CT model result is the same as the SSA modeling result. Note that CT model contains two more parameters in the gain equation: the switching period T_s and flying capacitance C. Therefore, it can easily illustrate the mechanism of frequency regulation and reveal the

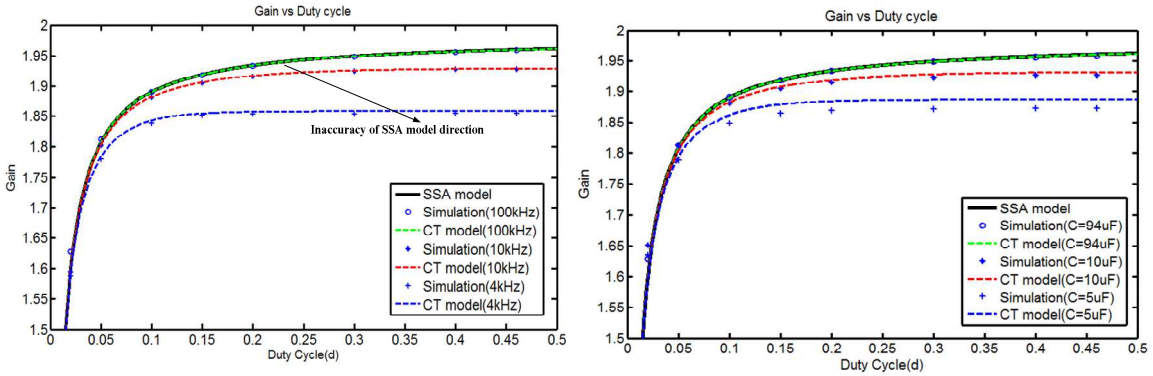
flying capacitor impact on voltage gain, which is not mentioned in the traditional SSA modeling method.

A gain comparison between SSA model and CT model is given as Figure 7.4, where the simulation result is presented as a series of dots. The circuit and control parameters in Table 7.1 are adopted for model calculation and simulation.

Table 7.1 Circuit and Control parameters for model comparison

Figure 7.4	V_{in}(V)	d	f_s(Hz)	R_{on}(Ω)	r(Ω)	C_1 (uF)	C_o(uF)	R_L(Ω)
(a)	5	0~0.5	4k, 10k, 100k	0.077	0.02	94	1	10
(b)	5	0~0.5	100k	0.077	0.02	5 10 94	1	10

For the SSA model, only loop resistance (R_{on}, r), duty cycle and load are involved in the final voltage gain equation. Therefore, only one black and thick regulation curve is plotted in Figure 7.4(a) and (b), regardless of frequency and flying capacitor variation of the circuit. It overlaps with the CT mode and the simulation result under 100kH switching frequency and 100uF flying capacitor condition.



(a) (b)

Figure 7.4. Duty cycle regulation curves with different control parameters

(a) Frequency effect (b) Flying capacitor effect

Nevertheless, the simulation results in Figure 7.4(a) show that when the frequency is decreased, the regulation curve tends to move "downward", which agrees well with the prediction of the CT method.

While in Figure 7.4(b), when the capacitance of flying capacitor is reduced, the lower voltage gain is also observed in simulation. The CT modeling result again agrees pretty well with this trend except a slight deviation under the condition of 5uF flying capacitance. This is because when C=5uF and Co=1u, there will be an obvious "voltage sudden drop" between C_1 and C_o when S_3 is turned on before the voltage of C_1 starts to decrease constantly. However, the model assumes the voltage of C_1 starts to decrease immediately at a constant rate when S_3 is turned on.

Therefore, in order to guarantee the accuracy of CT model, the condition of $C>>C_o$ is required, which leads the "voltage sudden drop" to be negligible. According to the comparison, the traditional SSA method is demonstrated to be too coarse to describe the voltage conversion ratio under the conditions of low switching frequency and small flying capacitance.

7.1.4 Model evaluation based equivalent output impedance

In order to further evaluate the CT modeling method, the output impedance based on more reviewed modeling methods in Chapter 2 is explored. According to a comprehensive SC equivalent circuit model in Figure 7.5 , the steady state equivalent circuit of Figure 7.1 can be interpreted as m=1 and n=2. The output impedance R_e using CT modeling can be derived as follows by inspection of equation (7.6):

$$R_e = R + \frac{T_s}{4C}\coth(\frac{dT_s}{2RC}) \tag{7.8}$$

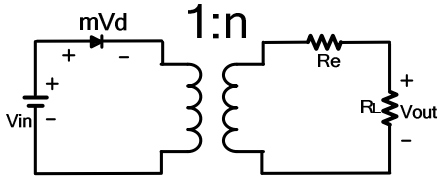


Figure 7.5 Model of an idealized SCC

Similarly, based on the gain equation (7.7) obtained by SSA method, the correspondingly output impedance can be found as:

$$R_e = R + \frac{R}{2d} \tag{7.9}$$

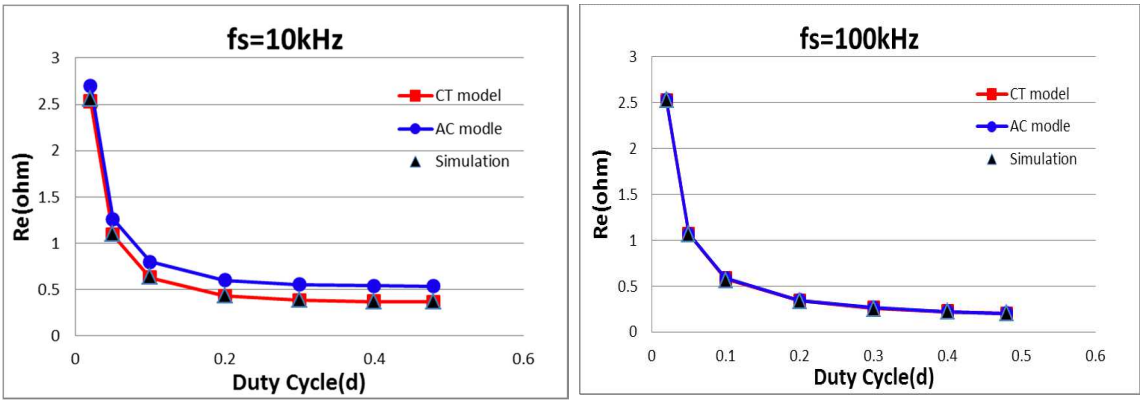
where R = R_{on} + r.

Besides steady state model, two modeling methods proposed in paper [142] and [140] recently are also applied to the converter in Figure 7.1 and the corresponding output impedances are derived in Table 7.2.

Table 7.2 Comparison of output impedance based on different Molding method

	Modeling methods	Equivalent Output impedance
(a)	State Space Averaging(SSA) Model[19]	$R + \frac{R}{2d}$
(b)	Charge balance-Transient Calculation(CT) Model	$R + \frac{T_s}{4C}\coth(\frac{dT_s}{2RC})$
(c)	Average-current based Conduction loss(AC) Model[142]	$\frac{T_s}{4C}\coth(\frac{dT_s}{2RC}) + \frac{T_s}{4C}\coth(\frac{T_s}{4RC})$
(d)	Slow and Fast Switching Limit (S-FSL) Model[140]	SSL Impedance: $\frac{T_s}{2C}$ FSL Impedance: $2R_{on}$

Based on comparison, it can be concluded different modeling methods have different merits and limitations. The SSA method focuses on duty cycle regulation. This model is general and simple, while its accurate is best under small “on time” and large flying capacitance condition. The AC method reflects the duty cycle and frequency effects on the output impedance, but due to the loss estimation through average current, the accuracy under low switching frequency is impaired. However, under high frequency condition, the output impedance based on this method becomes the same as CT method, as the second item of output impedance in Table 7.2(c) will evolve to R. The output impedance comparison between AC and CT methods is given in Figure 7.6 under switching frequency at 10k and 100 kHz, in contrast with simulation results. The other circuit parameters are set the same as Table 7.1(a) for simulation and model calculation. It shows CT model has a better agreement with simulation results under switching frequency of 10 kHz.



(a) (b)

Figure 7.6 Comparison of CT model and AC model with simulation results

(a) fs=10kHz (b)fs=100kHz

For S-FSL method, it emphasizes the impedance under very low frequency and very high frequency conditions. It is based on the energy conservation principle and neglects the duty cycle regulation effect. Moreover, the fast switching limit (FSL) doesn't consider the conduction loss of ESR of flying capacitors.

In view of above discussion, the CT modeling method provides more accurate prediction of circuit behavior under continuous variation of duty cycle and frequency conditions.

7.2 Enhanced CT Modeling Method

Since most previous steady state modeling methods neglect the output capacitor effect, including the CT method in previous section, their accuracy is compromised when output capacitor value is taken into account. In [174], an enhanced CT method that considering output capacitor effect is introduced aiming for more convenient circuit design and optimization.

The enhanced CT modeling method can be applied to simple dual-phase SC converters without coupling loops. In this dissertation, simple dual-phase SC converter is defined as three types of SC topologies based on different configurations during charging and discharging phase, as shown in Figure 7.7. The equivalent charging capacitance and discharging capacitance are expressed as C_{ch} and C_{dis} respectively. Type I dual-phase SCC in Figure 7.7(a) refers to all the SC converters whose charging phase can be modeled as an charging loop composed of input source, equivalent loop resistance R_{ch} and equivalent loop capacitance C_{ch}, while the discharging phase can be modeled as an discharging loop composed of equivalent discharging capacitance C_{dis}, loop resistance R_{dis} and load. Many

topologies such as unity gain SC converter, step down SC converter in [110] fall into this category. In contrast, for type II dual-phase SC converter shown as Figure 7.7(b), the input source becomes part of discharging loop, such as voltage tripler in [20]. For type III dual-phase SC converter as shown in Figure 7.7(c), the load will take part in the charging phase.

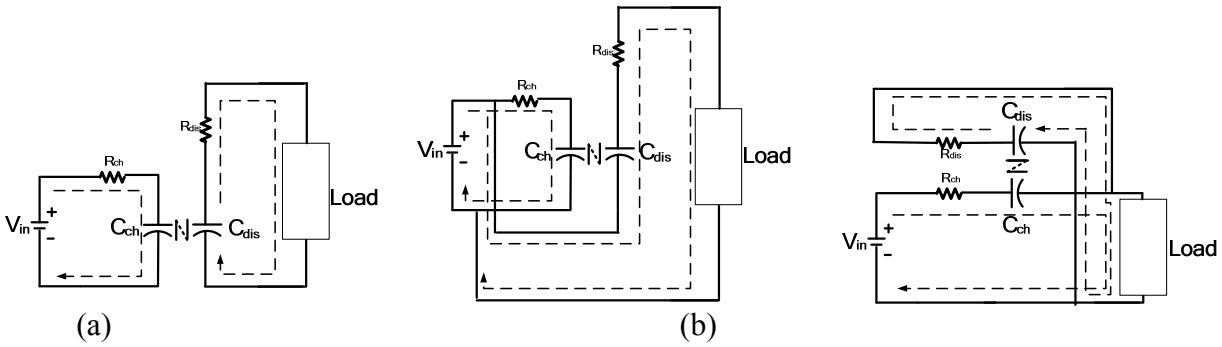


Figure 7.7 Simple dual-phase SC converter

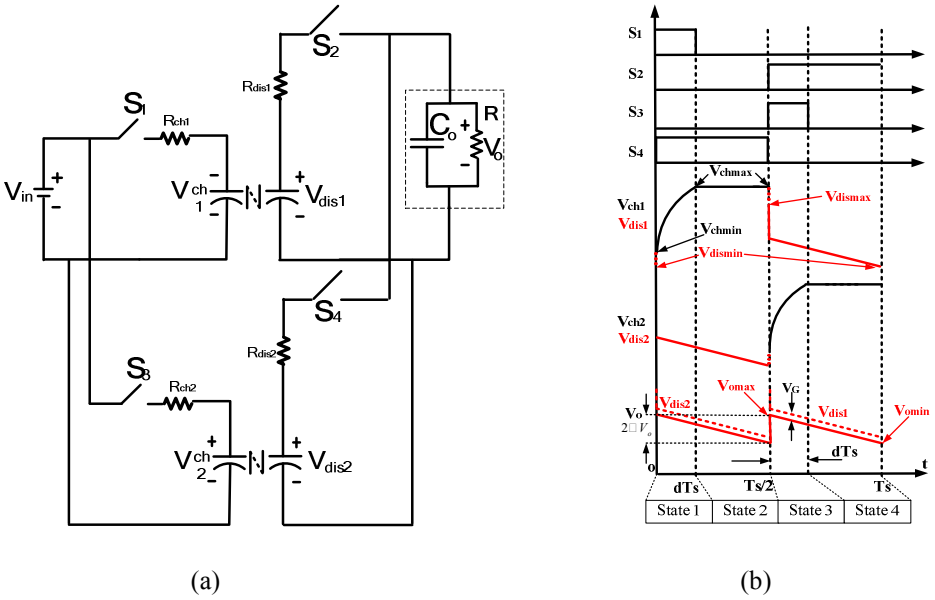
(a) Type I. (b) Type II. (c) Type III.

The modeling procedures for interleaved and non-interleaved configuration are investigated in section 7.2.1 and 7.2.2 respectively.

7.2.1 Modeling of Interleaved simple dual-phase SC converter

Interleaved SC converters were demonstrated to be effective to reduce the input current ripple, output voltage ripple and increase the regulation range [20], [175]. The duty cycle modulation is usually introduced to control the time of charging phase in order to regulate output voltage. At discharging phase, each circuit branch is supposed to power the load for a half switching cycle. Consequently, the output voltage could be maintained even under very small or no output filter capacitor condition. Interleaved type I dual-phase SC

converter is presented as Figure 7.8(a) and the key operational waveforms are presented in Figure 7.8(b), with consideration of output capacitor effect. Based on the switch control signals, four operational states are derived as shown in Figure 7.9.



(a) (b)

Figure 7.8 Interleaved type I dual-phase SC converter(a)Topology (b) Waveforms

To simplify calculation, the following assumptions are made: (1) The interleaved two branches have identical circuit elements: $C_{ch1} = C_{ch2} = C_{ch}$, $R_{ch1} = R_{ch2} = R_{ch}$, $R_{dis1} = R_{dis2} = R_{dis}$. The voltage of equivalent charging capacitor C_{ch1} is assumed rising from V_{chmin} to V_{chmax} at charging phase during time interval [0, dT_s]. (2) The voltage of equivalent discharging capacitor C_{dis1} is assumed decreasing from V_{dismax} to V_{dismin} during discharging phase within the time interval [$T_s/2$, T_s]. (3)At the begin of discharging phase, charge redistribution between C_{dis} and C_o is considered completed in very short time compared with a switching period, described as Figure 7.10(a) . Therefore, its time duration is neglected during calculation. After charge redistribution, C_{dis} and C_o are approximated to

discharge linearly due to large RC constant compared with switching period, as shown as Figure 7.10(b).

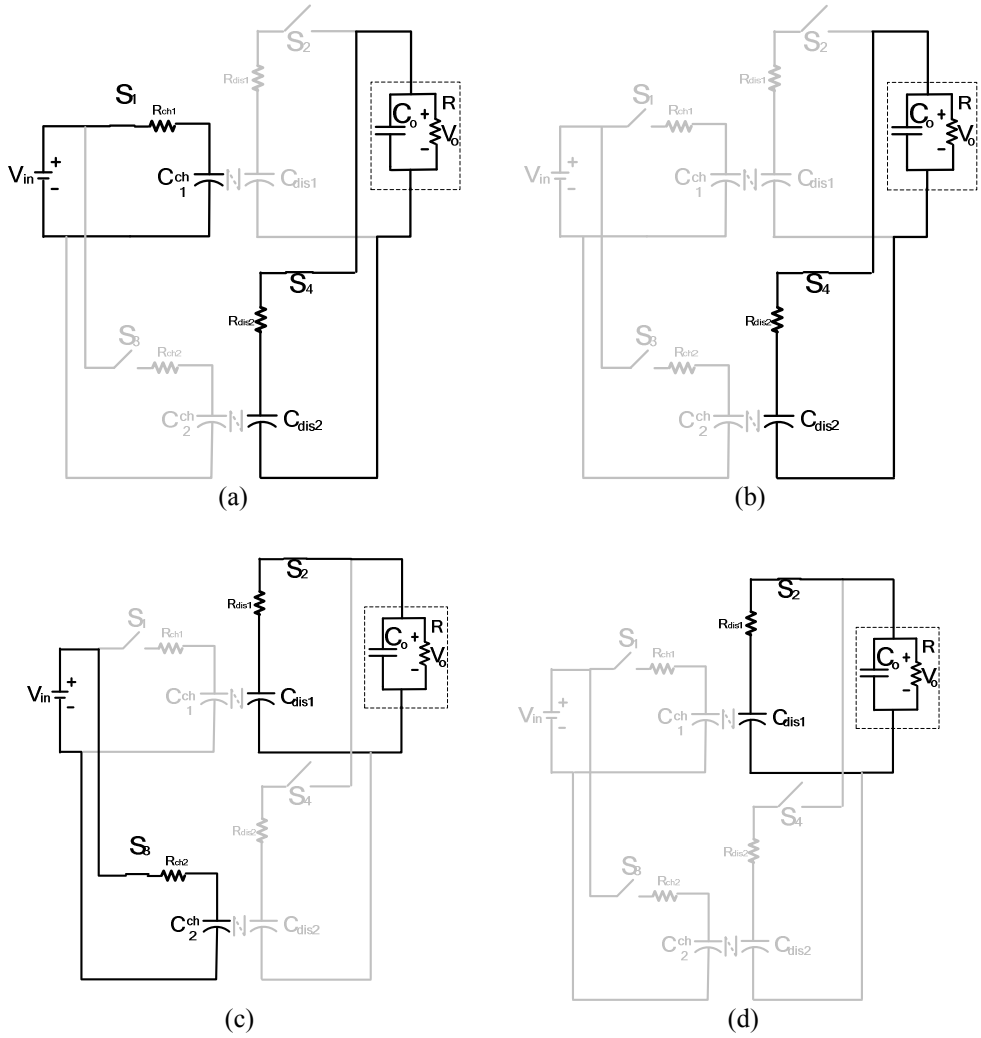
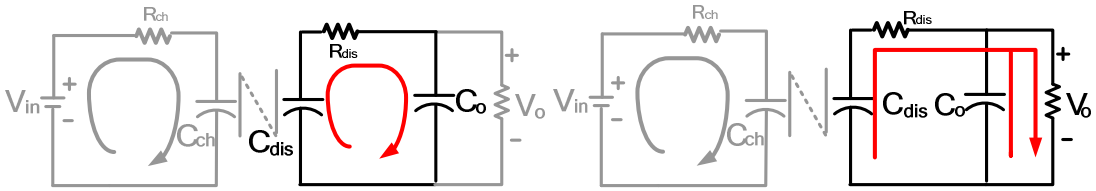


Figure 7.9 Operational states of Interleaved type I dual-phase SC converter.

(a) State 1[0,dT_s](b)State 2[dT_s,0.5T_s] (c)[0.5T_s, 0.5T_s +dT_s] (d) [0.5T_s +dT_s,T_s].



(a)

(b)

Figure 7.10 Circuit states of type I dual-phase SC converter at discharging phase

(a) Charge Redistribution. (b) Linear Discharging.

The proposed modeling process can be illustrated as following:

1) Transient calculation

During the time interval [0, dT_s] as shown in Figure 7.9(a), the following equation can be derived based on transient calculation:

$$V_{ch\max} = V_{in} - (V_{in} - V_{ch\min})e^{-\frac{dT_s}{R_{ch}C_{ch}}} \tag{7.10}$$

2) Output voltage averaging

According to the output voltage waveform described in bottom of Figure 7.8(b), the output voltage can be expressed as:

$$\overline{V_o} = \frac{V_{o\max} + V_{o\min}}{2} \tag{7.11}$$

3) Charge balance calculation

At the moment of $0.5T_s$, charge redistribution effect between C_{dis} and C_o results in the following equation:

$$C_{dis}V_{dis\max} + C_oV_{o\min} = C_{dis}(V_{o\max} + V_G) + C_oV_{o\max} \tag{7.12}$$

where V_G is the voltage gap between voltage of equivalent discharging capacitor and output voltage, depicted in Figure 7.8(b).

At discharging period right after charge redistribution, the following relationship can be derived based the assumption of linear discharging for C_{dis} and C_o:

$$V_G = \frac{C_{dis}}{C_o + C_{dis}} \frac{\overline{V_o}}{R_L} R_{dis} \tag{7.13}$$

$$V_{o\max} - V_{o\min} = \frac{1}{C_o + C_{dis}} \frac{\overline{V_o}}{R_L} 0.5T_s \tag{7.14}$$

At the end of discharging phase, the following relationship is obtained:

$$V_{dis\min} - V_G = V_{o\min} \tag{7.15}$$

4) Energy Conservation Calculation

For dual-phase SC converter, the energy stored in equivalent charging capacitor C_{ch} at the end of charging phase is equal to the energy stored in the equivalent discharge capacitor C_{dis} at the beginning of discharging phase. Therefore, at the time $0.5T_s$, it can be derived that:

$$\frac{1}{2} C_{ch} V_{ch\max}^2 = \frac{1}{2} C_{dis} V_{dis\max}^2 \tag{7.16}$$

Analogously, the following equation can be obtained:

$$\frac{1}{2} C_{ch} V_{ch\min}^2 = \frac{1}{2} C_{dis} V_{dis\min}^2 \tag{7.17}$$

Based on (7.10)-(7.17), there are eight variables ($V_{ch\max}$, $V_{ch\min}$, $V_{o\max}$, $V_{o\min}$, $V_{dis\max}$, $V_{dis\min}$, V_{out}, V_G) with eight equations. By employing Mathematica software tool, the voltage gain of type I dual-phase SC converter is calculated as follows:

$$\frac{\overline{V_o}}{V_{in}} = \frac{\sqrt{C_{ch}/C_{dis}}\,R_L}{\frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + \frac{C_oT_s}{4C_{dis}(C_{dis}+C_o)} + \frac{C_{dis}}{C_{dis}+C_o}R_{dis} + R_L} \tag{7.18}$$

For this type of converter, when load resistor R_L goes to infinity, the ideal gain M is derived as:

$$M = \frac{\overline{V_o}}{V_{in}}|_{R_L\to\infty} = \sqrt{C_{ch}/C_{dis}} \tag{7.19}$$

If the value of output capacitor output capacitor goes to zero, equation (15) evolves to:

$$\frac{\overline{V_o}}{V_{in}}|_{C_o\to 0} = \frac{\sqrt{C_{ch}/C_{dis}}\,R_L}{\frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + R_{dis} + R_L} \tag{7.20}$$

This equation exactly matches the result derived in paper [173], in which case more specific conditions $T_s = 2nT_{on} = 2nT_s d$ were assumed using adaptive control.

Based on (15), the general equivalent output impedance can be derived as below:

$$R_{e\_\text{int}} = \frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + \frac{C_oT_s}{4C_{dis}(C_{dis}+C_o)} + \frac{C_{dis}}{C_{dis}+C_o}R_{dis} \tag{7.21}$$

Based on (11), the ratio of output ripple with respect to output voltage is expressed as:

$$\delta = \frac{\Delta V_o}{\overline{V_o}} = \frac{1}{4}\frac{1}{C_o + C_{dis}}\frac{1}{R_L}T_s \tag{7.22}$$

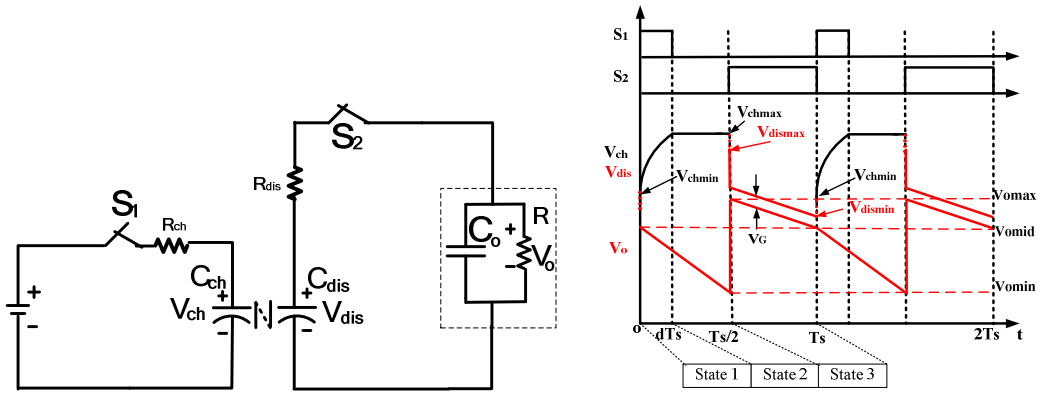
If the output ripple limitation $\delta < m$ is given, the minimum output capacitor C_o can be decided as follows:

$$C_o > \frac{T_s}{4mR_L} - C_{dis} \tag{7.23}$$

7.2.2 Modeling of Non-interleaved simple dual-phase SC converter

Although interleaved SC converter has the benefits of reducing the size of output filter capacitor, reduced input current ripple and enhanced regulation range, it is also recognized that inclusion of the extra circuit branch increases the cost and circuit size. Thus in applications with strict volume and cost requirement, non-interleaved dual-phase SC converters should also be considered. Since the output capacitor is an optimization object during circuit design, steady state model with consideration of output filter capacitor effect is useful in some practical design conditions.

A non-interleaved type I dual-phase SC converter is given in Figure 7.11(a). The similar modeling technique discussed in previous section is extended to model this converter. The key circuit waveforms are presented as Figure 7.11(b). Three operational modes can be identified in one switching period, as shown in Figure 7.12.



(a) (b)

Figure 7.11 Interleaved type I single-phase SC converter (a) Topology (b) Waveform

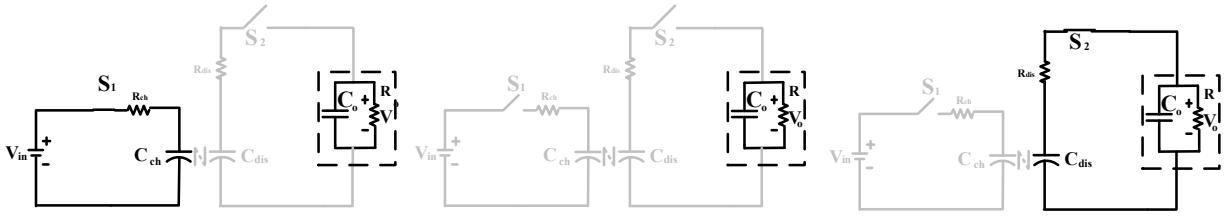


Figure 7.12 Operational states of None-interleaved type I dual-phase SC converter

(a) State 1[0,dT_s](b)State 2[dT_s,$0.5T_s$] (c)[$0.5T_s$, $0.5T_s$ +dT_s] (d) [$0.5T_s$ +dT_s,T_s]

The circuit assumptions are made the same as previous section. The application of proposed modeling technique is illustrated as follows:

1) Transient calculation

In state 1 [0, dT_s], the following equation can be derived based on transient calculation:

$$V_{ch\max} = V_{in} - (V_{in} - V_{ch\min})e^{-\frac{dT_s}{R_{ch}C_{ch}}} \tag{7.24}$$

2) Output voltage averaging

According to the output waveform given in Figure 7.11(b), the average output voltage can be expressed as:

$$\overline{V_o} = \frac{V_{o\max} + V_{o\min} + 2V_{omid}}{4} \tag{7.25}$$

3) Charge balance calculation

During C_o discharging period [0, $0.5T_s$], when S_2 is turned off, the following equation can be derived based on linear discharging assumption of C_o:

$$V_{omid} - V_{o\min} = \frac{1}{C_o}\frac{\overline{V_o}}{R_L}0.5T_s \tag{7.26}$$

At the time $0.5T_s$, charge redistribution between C_{dis} and C_o gives the following equation:

$$C_{dis}V_{dis\max} + C_oV_{o\min} = C_{dis}(V_{o\max} + V_G) + C_oV_{o\max} \tag{7.27}$$

During discharging period of $[0.5T_s, T_s]$ as shown in Figure 7.12(c), C_{dis} and C_o are discharged simultaneously. The following equations can be derived based on the assumption of linear discharging of C_{dis} and C_o:

$$V_G = \frac{C_{dis}}{C_o + C_{dis}}\frac{\overline{V_o}}{R_L}R_{dis} \tag{7.28}$$

$$V_{o\max} - V_{omid} = \frac{1}{C_o + C_{dis}}\frac{\overline{V_o}}{R_L}0.5T_s \tag{7.29}$$

At the moment of T_s, the following relationship is derived:

$$V_{dis\min} - V_G = V_{omid} \tag{7.30}$$

4) Energy Conservation during phase transition

Similar to interleaving case, according to energy conservation during phase transition moment, it can be derived that:

$$\frac{1}{2}C_{ch}V_{ch\max}^2 = \frac{1}{2}C_{dis}V_{dis\max}^2 \tag{7.31}$$

Analogously, the following equation can be obtained:

$$\frac{1}{2}C_{ch}V_{ch\min}^2 = \frac{1}{2}C_{dis}V_{dis\min}^2 \tag{7.32}$$

According to (7.24) - (7.32), the voltage gain of type I single-branch SC converter can be derived as:

$$\frac{\overline{V_o}}{V_{in}} = \frac{\sqrt{C_{ch}/C_{dis}}R_L}{\frac{T_s}{2C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + \frac{(2C_o + C_{dis})^2 T_s}{8C_{dis}C_o(C_{dis}+C_o)} + \frac{C_{dis}}{C_{dis}+C_o}R_{dis} + R_L} \tag{7.33}$$

The general output impedance for single-branch type 1 SC converter is thus derived as:

$$R_{e\_\sin} = \frac{T_s}{2C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + \frac{(2C_o + C_{dis})^2 T_s}{8C_{dis}C_o(C_{dis}+C_o)} + \frac{C_{dis}}{C_{dis}+C_o}R_{ch} \tag{7.34}$$

According to (7.26) and (7.29), the ratio of output ripple with respect to output voltage can be expressed as:

$$\delta = \frac{\Delta V_o}{\overline{V_o}} = \frac{1}{4}(\frac{1}{C_o + C_{dis}} + \frac{1}{C_o})\frac{T_s}{R_L} \tag{7.35}$$

In this case, if the output ripple limitation $\delta < m$ is set, the minimum output capacitor C_o can be decided by following equation:

$$C_o > \frac{2 - kC_{dis} + \sqrt{(kC_{dis}-2)^2 + 4kC_{dis}}}{2k} \tag{7.36}$$

where $k = \frac{4mR_L}{T_s}$.

7.2.3 Comparative analysis of interleaved and non-interleaved SC converter

According to equivalent output impedance derived for interleaved and single-branch dual-phase SC converter in (18) and (29), it can be concluded that the choice of output capacitance influences the circuit steady state behavior.

When the output capacitor goes to zero, it can be found that:

$$R_{e\_\text{int}}|_{C_o=0} = \frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + R_{dis} \tag{7.37}$$

$$R_{e\_\text{sin}}|_{C_o=0} = \infty \tag{7.38}$$

Above two equations reveal the physical insight that single-branch SC converter cannot operate without output capacitor. While theoretically, the interleaved SC converter have finite output impedance even if the output filter capacitor is absent. In practice, output capacitor is still preferred for both cases.

When the output capacitance is approaching infinity, it can be found that:

$$R_{e\_\text{int}}|_{C_o=+\infty} = \frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + \frac{T_s}{4C_{dis}} \tag{7.39}$$

$$R_{e\_\text{sin}}|_{C_o=+\infty} = \frac{T_s}{2C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}}) + \frac{T_s}{2C_{dis}} \tag{7.40}$$

It demonstrates that when the output becomes a firm voltage with infinite filter capacitor, the equivalent output impedance of interleaved structure is half of single-branch case. This is the reason why interleave can increase regulation range.

The proposed modeling method can be easily applied to type II or type III dual-phase SC converter in Figure 7.7, based on the modeling procedure illustrated for type I dual-

phase SC converter. The modeling results for all simple dual-phase SC converters are given in Table 7.3 for reference.

Table 7.3 Proposed modeling Method for modeling Simple dual-phase SC converter

Simple dual-phase SC converter	Configuration	Steady State Gain	Ideal Gain(M)
Type I	Interleaved	$\frac{\sqrt{C_{ch}/C_{dis}}\,R_L}{\frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_1C_{ch}})+\frac{C_oT_s}{4C_{dis}(C_{dis}+C_o)}+\frac{C_{dis}}{C_{dis}+C_o}R_{dis}+R_L}$	$\sqrt{C_{ch}/C_{dis}}$
	Single-branch	$\frac{\sqrt{C_{ch}/C_{dis}}\,R_L}{\frac{T_s}{2C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}})+\frac{(2C_o+C_{dis})^2T_s}{8C_{dis}C_o(C_{dis}+C_o)}+\frac{C_{dis}}{C_{dis}+C_o}R_{dis}+R_L}$	$\sqrt{C_{ch}/C_{dis}}$
Type II	Interleaved	$\frac{(\sqrt{C_{ch}/C_{dis}}+1)R_L}{\frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}})+\frac{C_oT_s}{4C_{dis}(C_{dis}+C_o)}+\frac{C_{dis}}{C_{dis}+C_o}R_{dis}+R_L}$	$\sqrt{C_{ch}/C_{dis}}+1$
	Single-branch	$\frac{(\sqrt{C_{ch}/C_{dis}}+1)R_L}{\frac{T_s}{2C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}})+\frac{(2C_o+C_{dis})^2T_s}{8C_{dis}C_o(C_{dis}+C_o)}+\frac{C_{dis}}{C_{dis}+C_o}R_{dis}+R_L}$	$\sqrt{C_{ch}/C_{dis}}+1$
Type III	Interleaved	$\frac{\frac{\sqrt{C_{ch}}}{\sqrt{C_{ch}}+\sqrt{C_{dis}}}R_L}{\frac{\sqrt{C_{dis}}}{\sqrt{C_{ch}}+\sqrt{C_{dis}}}[\frac{T_s}{4C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}})+\frac{C_oT_s}{4C_{dis}(C_{dis}+C_o)}+\frac{C_{dis}}{C_{dis}+C_o}R_{dis}]+R_L}$	$\frac{\sqrt{C_{ch}}}{\sqrt{C_{ch}}+\sqrt{C_{dis}}}$
	Single-branch	$\frac{\frac{\sqrt{C_{ch}}}{\sqrt{C_{ch}}+\sqrt{C_{dis}}}R_L}{\frac{\sqrt{C_{dis}}}{\sqrt{C_{ch}}+\sqrt{C_{dis}}}[\frac{T_s}{2C_{dis}}\coth(\frac{dT_s}{2R_{ch}C_{ch}})+\frac{(2C_o+C_{dis})^2T_s}{8C_{dis}C_o(C_{dis}+C_o)}+\frac{C_{dis}}{C_{dis}+C_o}R_{dis}]+R_L}$	$\frac{\sqrt{C_{ch}}}{\sqrt{C_{ch}}+\sqrt{C_{dis}}}$

7.2.4 Model comparison for Unity Gain SC Converter

In order to compare the enhanced CT modeling method with CT modeling method in previous section and other surveyed modeling methods in Table 2.2, case study for unity gain SC converter is conducted for simplification purpose in this section, with both interleaving and non-interleaving structures considered, shown in Figure 7.13(a) and (b).

The purpose is to find out the discrepancies among different steady state models and investigate the accuracy issue. The switching diagram of S_1~S4 in Figure 7.13(a) is provided as top waveforms in Figure 7.8(b) while switching diagram of S_1~S_2 in Figure 7.13(b) is presented as top waveforms in Figure 7.11(b).

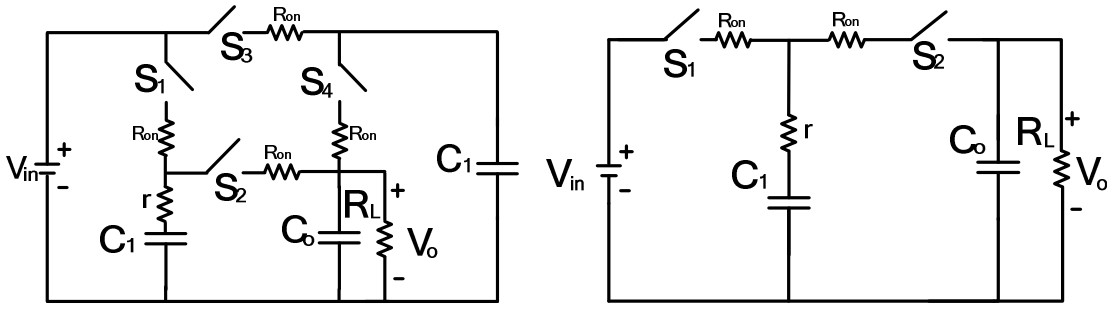


Figure 7.13 Unity gain SC Converter

(a) Interleaving Condition. (b) Single-branch condition.

The modeling results for equivalent output impedance based on different modeling methods are derived and compared in Table 7.4. Note that $R_{ch}=R_{dis}=R_{on}+r=R$ is assured for both interleaved and non-interleaved conditions.

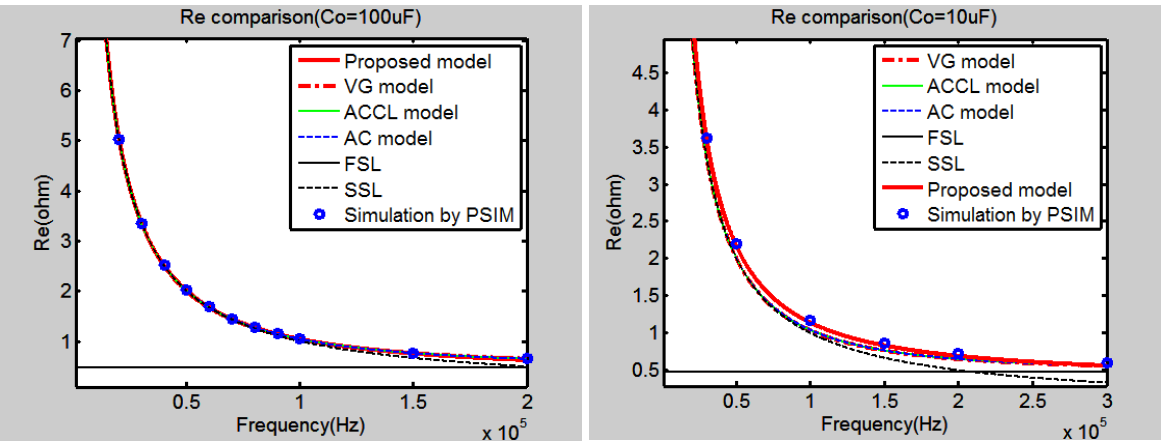
Table 7.4 Comparison of Output impedance calculation for unity gain SC converter

Steady state modeling method	Interleaving Condition	Single-branch Condition
Average Current based method(AC) [136], [137]	$\frac{T}{2C}\frac{e^{\frac{d+0.5}{RC_1}T_s}-1}{(e^{\frac{dT_s}{RC_1}}-1)(e^{\frac{0.5T_s}{RC_1}}-1)}$	$\frac{T}{C}\frac{e^{\frac{d+0.5}{RC_1}T_s}-1}{(e^{\frac{dT_s}{RC_1}}-1)(e^{\frac{0.5T_s}{RC_1}}-1)}$
Average-Current-based Conduction Loss method(ACCL)[142]	$\frac{T_s}{4C_1}\coth(\frac{dT_s}{2RC_1})+\frac{T_s}{4C_1}\coth(\frac{0.5T_s}{2RC_1})$	$\frac{T_s}{2C_1}\coth(\frac{dT_s}{2RC_1})+\frac{T_s}{2C_1}\coth(\frac{0.5T_s}{2RC_1})$
FSL and SSL method(FSL-SSL) [140].	$R_{FSL}=\frac{R}{2d}+R\ ,R_{SSL}=\frac{T_s}{2C_1}$	$R_{FSL}=\frac{R}{d}+2R\ ,R_{SSL}=\frac{T_s}{C_1}$
Voltage-Gap modeling method(VG) [139]	$\frac{T}{2C_1}\frac{1-e^{-\frac{d+0.5}{RC_1}T_s}}{(1-e^{-\frac{dT_s}{RC_1}})(1-e^{-\frac{0.5T_s}{RC_1}})}$	$\frac{T}{C_1}\frac{1-e^{-\frac{d+0.5}{RC_1}T_s}}{(1-e^{-\frac{dT_s}{RC_1}})(1-e^{-\frac{0.5T_s}{RC_1}})}$
CT Modeling method	$\frac{T_s}{4C_1}\coth(\frac{dT_s}{2RC_1})+R$	/
Enhanced CT modeling method	$\frac{T_s}{4C_1}\coth(\frac{dT_s}{2RC_1})+\frac{C_oT_s}{4C(C_1+C_o)}+\frac{C_1R}{C_1+C_o}$	$\frac{T_s}{2C_1}\coth(\frac{dT_s}{2RC_1})+\frac{(2C_o+C_1)^2T_s}{8C_1C_o(C_1+C_o)}+\frac{C_1R}{C_1+C_o}$

In order to compare the results in detail, the output impedances for single-branch condition are plotted as function of switching frequency, as shown Figure 7.14. The simulation results are also given in blue circles for contrast. The flying capacitor C_1 is fixed at 10uF, while the output capacitor of 10uF and 100uF are investigated respectively and plotted in Figure 7.14(a) and (b).

Table 7.5 Parameter list for model comparison

Component	Value
S_1 and S_2	R_{on} =80mohm
d	0.3
C_1	10uF, ESR=10mohm
C_o	10uF, 100uF



(a) (b)

Figure 7.14 Output impedance comparison for single-branch unity gain SC converter

(a) Co = 100uF. (b) Co = 10uF.

The circuit and control parameters for model calculation and simulation are summarized in Table 7.5. In simulation case, the input is set as 10V and load resistor fixed at 10 ohm for equivalent output impedance acquisition, with other parameters kept the same as model calculation. ESR of output capacitor is not considered in model calculation and simulation here.

According to Figure 7.14(a), all the modeling methods show great match with simulation result at the frequency range under 200 kHz except FSL and SSL, where large output capacitor (C_o = 100uF) is adopted. This is not surprising because large output capacitor can achieve approximately firm DC output voltage, which is assumed based on most surveyed modeling methods. Only under very low and very high frequency condition, FSL and SSL model shows good accuracy

However, according to Figure 7.14(b), it shows the enhanced CT model exhibits better match with simulation results when output capacitor of 10uF is adopted. This is because

the assumption of firm output voltage become relaxed when decreased output capacitance and noticeable output ripple appear. Therefore, the better accuracy of CT model with small output capacitor condition is verified. This modeling method is useful for output capacitor optimization with specific output ripple requirement.

7.2.5 Accuracy constraint analysis of enhanced CT modeling method

1) Switching frequency constrain

With deep investigation of proposed modeling method, the accuracy of the model can be achieved within some constrained conditions. This is due to the assumptions that charge redistribution period should be relatively small compared with half switching cycle. The accuracy condition can be found as following:

The charge redistribution time can be approximated as RC time constant of charge redistribution loop in Figure 7.10(a):

$$T_{QR} \approx R_{dis}(C_{dis} + C_o) \tag{7.41}$$

Therefore, the accuracy condition of proposed modeling method can be approximated as:

$$\frac{T_s}{2} > T_{QR} \tag{7.42}$$

It can be further expressed as:

$$f_s < \frac{1}{2R_{dis}(C_{dis} + C_o)} \tag{7.43}$$

where f_s is the switching frequency, T_s is switching period.

When the switching frequency is too high and beyond the limitation, the accuracy of proposed model can be impaired. Under this case, the FSL model can be adopted for steady state analysis.

2) ESR of output capacitor analysis

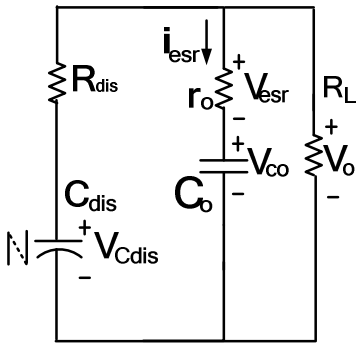


Figure 7.15 Discharging phase with consideration of ESR of Co.

During a switching period, the average voltage drop on the ESR of output capacitor C_o can be expressed as:

$$\overline{V_{esr}} = \frac{1}{T_s}\int_0^{T_s} r_o i_{esr}(t)dt = \frac{r_o}{T_s}\int_0^{T_s} i_{esr}(t)dt = 0 \qquad \textbf{(7.44)}$$

Therefore, based on proposed transient calculation, the output voltage V_o is the same as the voltage drop on capacitor C_o. As a result, the charge redistribution phase in Figure 7.10(a) has a new equivalent discharging resistor:

$$R'_{dis} = R_{dis} + r_o \qquad \textbf{(7.45)}$$

The formula of V_G at linear discharging phase shown as can be modified as:

$$V_G^{'} = V_G \frac{R_{dis}^{'}}{R_{dis}} - \frac{V_o}{R_L} r_o \tag{7.46}$$

As V_G is usually very small and sometime even negligible, the only impact of ESR becomes the slight increase of the equivalent discharging resistance R_{dis}. The model is still accurate only when new $R_{dis}^{'}$ satisfy condition (7.43).

7.2.6 Simulation and experimental verification

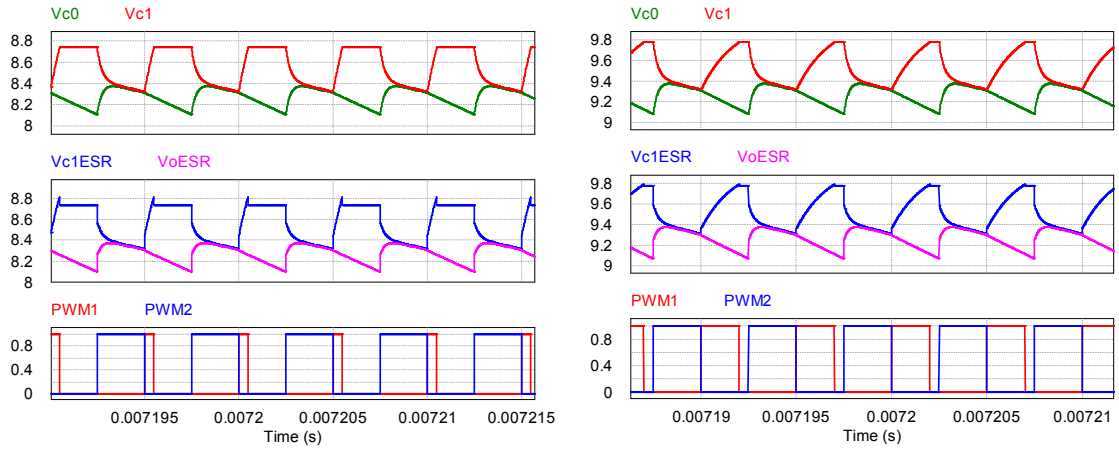
In order to verify the accuracy of enhanced CT modeling technique for simple dual-phase SC converter, experiments for single-branch unity-gain SC converter are conducted. A simple unity gain SC converter prototype using topology Figure 7.13(b) is built based on discrete components. The circuit parameters and adopted components are listed in Table 7.6.

Table 7.6 Circuit parameters of unity gain SC converter

Components	Value	Parameter	Value
C_o	Film capacitor:10uF ESR:12mohm	V_{in}	10V
C_1	Film capacitor:10uF ESR:12mohm	R_L	$10\,\Omega$
S_1	FDPF 20N50T $R_{ds(on)}$:230 $m\Omega$	d	[0,0.5]
S_2	IRF3710 $R_{ds(on)}$:23 $m\Omega$	f_s	100kHz

The simulation waveforms with same circuit parameters are provided in Figure 7.16 under duty cycle of 0.1 and 0.4 conditions. V_{c1ESR} indicates voltage drop on ESR of C_1 is included while V_{oESR} includes ESR voltage drop of Co, which are the real measured voltage during experiments. According to the simulation results, the ESR of C_1 can cause

voltage drop when charging period is finished. The ESR of Co can cause output voltage boost during charge redistribution phase. But it doesn't change the average output voltage.

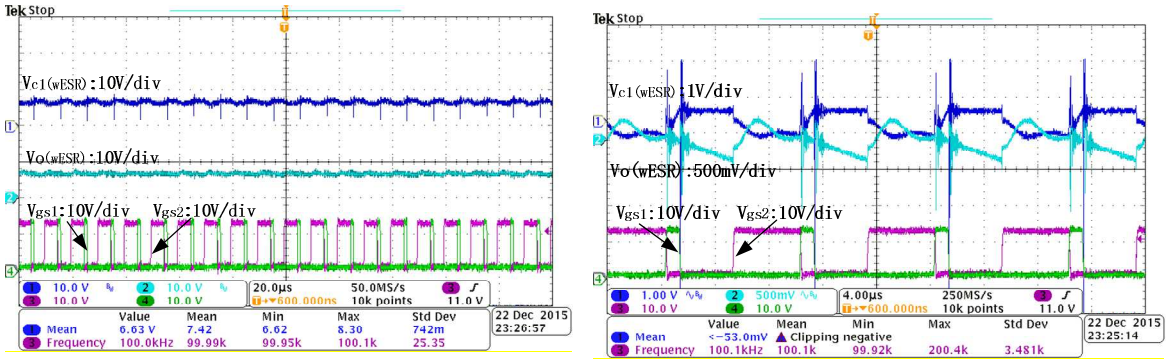


(a) (b)

Figure 7.16 Voltage Waveforms of Capacitor C_1, C_o and Control signals

(a)d=0.1 (b) d=0.4

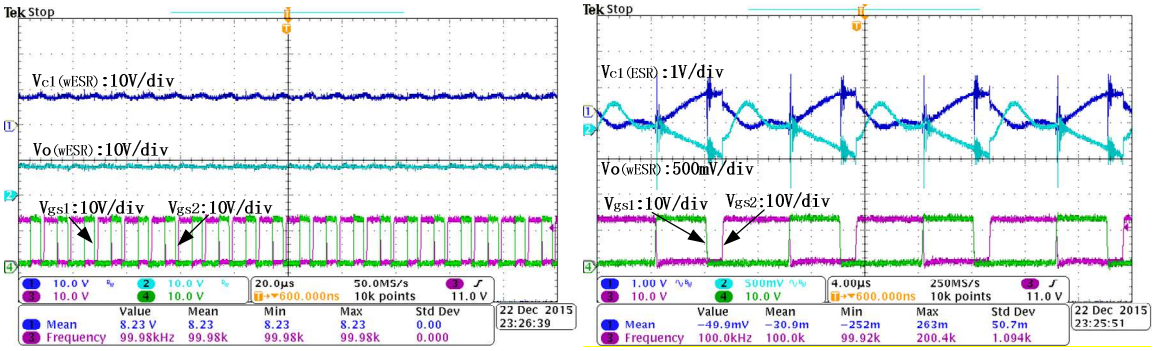
The experimental results are presented in Figure 7.17 and Figure 7.18. In Figure 7.17(a), the voltages of C_1, C_o and driving signals are presented. The ripples of C_1 and C_o are zoomed in for detail exhibition in Figure 7.17(b). About 5%-10% output voltage ripple is existed in experiment to show more clearly of the model details. Another reason by using limited switching frequency is due to discrete components used in prototype can bring considerable stray inductor interference under extremely high switching frequency condition, which can deteriorate the accuracy in experimental case. Therefore, 100kH is adopted finally for experimental verification. In chip level SC converters, the output ripple can be further optimized based on proposed model with higher frequency design.



(a) (b)

Figure 7.17 Voltage Waveforms of Capacitor C_1, C_o ,V_{gs1}, V_{gs2} at d=0.1

(a)Zoomed out (b) Zoomed in (AC coupling for DC voltage)



(a) (b)

Figure 7.18 Voltage Waveforms of Capacitor C_1, C_o ,V_{gs1}, V_{gs2} at d=0.4

(a)Zoomed out (b) Zoomed in (AC coupling for DC voltage)

The output voltage as function of duty cycle based on proposed model, simulation and experiment are compared in Figure 7.19. According to Figure 7.19, the simulation results match almost exactly with the proposed model, while the experimental results also show good agreement with model prediction. The slight difference is caused by the parasitic parameters' effect particularly the stray inductance. Generally, the accuracy of enhance CT model is demonstrated.

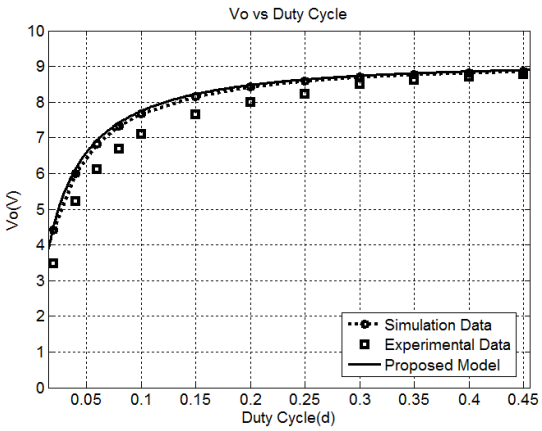


Figure 7.19 Model, simulation and experiment comparison at V_{in}=10V, f_s=100kHz

7.3 Summary

In this chapter, an accurate modeling technique for switched capacitor converter is comprehensively investigated. The CT modeling method which is suitable for interleaved SC converter is compared with state space averaging method and some other reviewed modeling methods. Better accuracy in predicting circuit steady state behavior is demonstrated. However, when comparatively large output capacitor is used, the accuracy of CT modeling method may be compromised.

Therefore, the enhanced CT modeling method is proposed to include the output capacitor effect on voltage gain by considering charge redistribution phase. This method is suitable for interleaved and non-interleaved simple dual-phase SC converter with moderate output capacitor condition, by providing guidelines for output capacitor optimization design.

A comprehensive guideline for application of different steady state modeling techniques of SC converter can be concluded as Figure 7.20. This figure shows when output capacitor is large enough, the AC, ACCL, and VG modeling method are accurate for the entire

switching frequency, while SSL is accurate under low frequency condition, and FSL under high frequency condition. The CT model is especially accurate under interleaving condition with small output capacitor, though it may have some sufficient accuracy under larger output capacitor condition. For Enhance CT model method, it is accurate under moderate output capacitor condition. Its accuracy on frequency range can vary depending on adopted output capacitor. The SSA model is accurate under high frequency range with all output capacitor conditions.

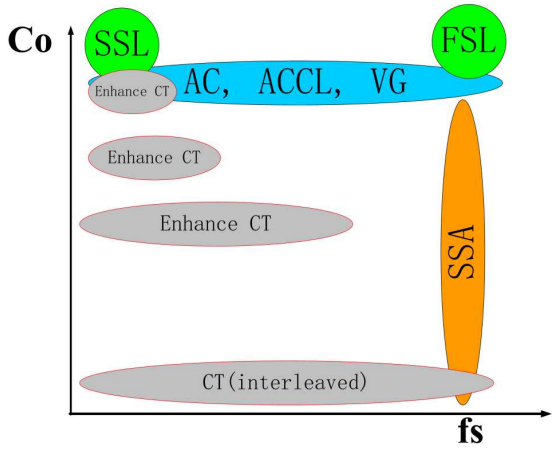


Figure 7.20 Application guideline for steady state model of SC converter

Part II Hybrid Boosting Converters (HBC)

Chapter 8 Introduction of hybrid converters

In part I, the merits of switched capacitor converter such as high efficiency, high power density, low component voltage stress, and gain enhancement were confirmed. However, in wide voltage regulation application area, the switched capacitor converter still suffers from the drawbacks of low system efficiency and week regulation capability. In this part, the technology combining switched capacitor converter with traditional inductive PWM converter is investigated as hybrid converter and new topologies for voltage boosting applications are generated. Regulation capability is greatly strengthened while many benefits of switched capacitor converter are maintained.

8.1 Definition of hybrid converters

In a broad view, "Hybrid Converters" in power electronics filed can be defined as topology combination of any two or more distinctive types of power electronics converters. In the past, some researchers have shrunk the definition of hybrid converter to be the converter that only hydrides the structures of switched capacitor and switched inductor. In [176], the traditional boost converter was basically combined with a voltage multiplier, leading to named hybrid converter. In [38], several switched capacitor or switched inductor structures were developed and combined with classic PWM converters. The resulted converters were also called hybrid converters. In [60], a new hybrid boost three level DC-DC converter was defined by synthesizing two boost three-level dc-dc converter, where switched capacitor and switched inductor structures both existed.

In this dissertation, a clearer and more comprehensive definition for hybrid converter is given: a power electronics converter that implements the topology combination of switched capacitor converter and inductive PWM converter. The switched capacitor converter, regarded as a special subset of power electronics converters, has a number of specific features without participation of inductive elements. On the other hand, inductive PWM converter is referred to all PWM converters that employ one or more magnetic elements such inductor, tapped inductor or transformer for energy conversion without switched capacitor structure. Therefore, the concept of hybrid converter can be interpreted as Figure 8.1. Topology variations based on Figure 8.1 can classified as combination 4~8 listed in Table 1.2 in Chapter 1. More extensive topologies review and comparison with proposed topology will be given in Chapter 10 and Chapter 11 based on each combination category.

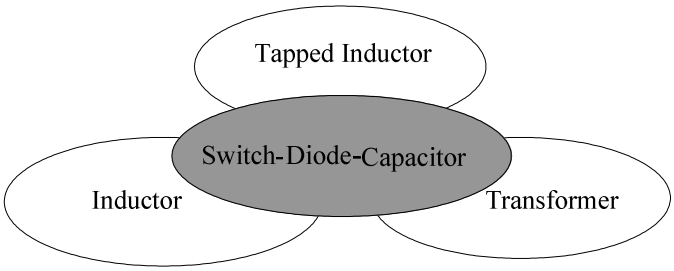


Figure 8.1 Concept of Hybrid Converter

8.2 Merits of hybrid converters

Since hybrid converter is a combination of switched capacitor converter and inductive PWM converter, its benefits may be a collective advantages of both types of converters, as shown in Figure 8.2.

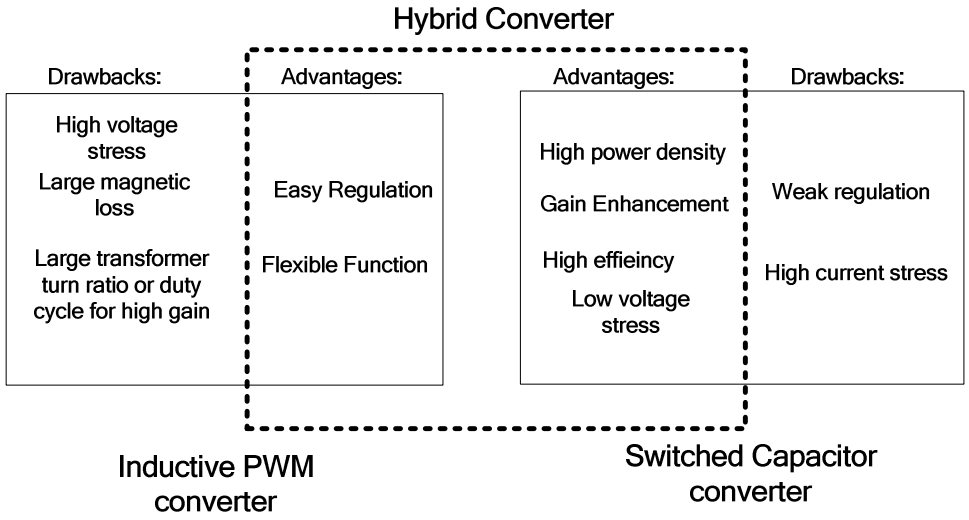


Figure 8.2 Merits of Hybrid Converter

According to the Figure 8.2, the major drawbacks of inductive PWM converter and switched capacitor converter can be avoided by proper design of hybrid converter structure. For instance, the current stress issue of switched capacitor structure can be totally eliminated by inserting a second winding of tapped inductor such as hybrid topology in Fig 1.9 of Chapter 1. High component voltage stress problem of inductive PWM converter can be entirely avoided by employing some special switched capacitor structure, such as the DC-DC multilevel boost converter developed in [55]. However, it's also possible some drawbacks of each type of converter are not fully eliminated in order to pursuit some other

more critical performance. Consequently, a trade-off design for hybrid converters may be required in practice.

8.3 Development in Part II of this dissertation

In this part, a family of hybrid boosting converters is developed, inspired by the TBSC topology in Part I. The topologies will be detailed. Each HBC converter is comprised of a bipolar voltage multiplier and an inductive switching core. Different inductive switching cores are developed with a variety of functionalities. The bipolar voltage multiplier is regarded as switched capacitor technology while the inductive switching cores maintain the benefits of traditional inductive PWM converters. With this combination, many desirable features are derived for the generated converters.

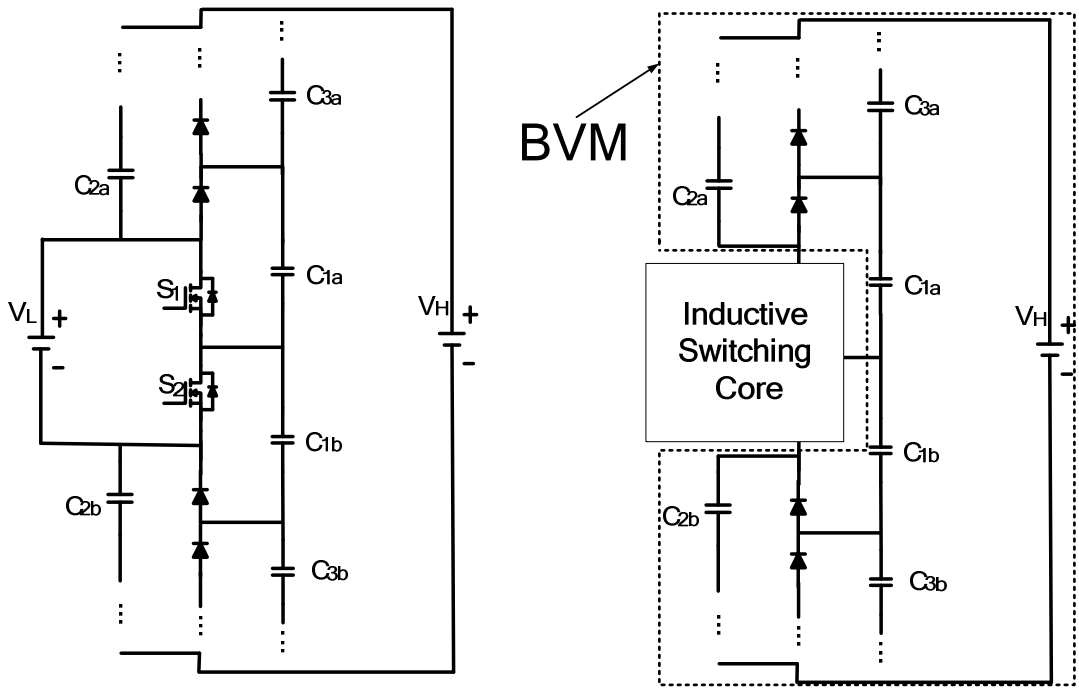
The development of HBC family and operational principle of each converter are briefly discussed in Chapter 9. The detail analysis and design of basic HBC is investigated in Chapter 10 with experimental verification. Its superiority compared with previous topologies in the same category is demonstrated. The isolated HBC is fully explored in Chapter 11. Due to the leakage problem of isolation transformer, a new design of a lossless snubber is proposed and investigated to improve the circuit efficiency. Simulation and experimental results are provided to verify the proposed theory. In chapter 12, many innovative circuit structures regarded as extensions of HBC are presented and discussed, most of which are verified by simulation results. The topology system with the center of HBC converters is basically established, with a number of potential applications envisioned. The future work of Part I and Part II are summarized in Chapter 13.

Chapter 9 Topology Development of HBC and Operational Principle

In this chapter, a new hybrid converter family, Hybrid Boosting Converters (HBC) is developed. The topology evolvement and derivation of different HBC are introduced in section 9.1. Four primary HBC family members, basic HBC, isolated HBC, tapped HBC and symmetrical HBC are analyzed individually from section 9.2 to section 9.5. Their basic operational principle and conversion ratio are investigated under Continuous Conduction Mode (CCM) condition based on simple topologies in each section.

9.1 Derivation of HBC family

In Part I, the Two-switch Boosting Switched-capacitor Converter (TBSC) was developed as Figure 9.1(a) with sufficient analysis. There are one input source and two active switches at the middle of circuit structure. In spired by TBSC, another family of hybrid converter is found, by replacing the input source and two switches with an inductive switching core block, as shown in Figure 9.1(b). With the aid of inductive switching core, the switched capacitor converter is turned to hybrid converter, resulting in a variety of new features and benefits. The circuit structure of HBC is investigated by two parts respectively: inductive switching core and Bipolar Voltage Multiplier (BVM) within dashed line of Figure 9.1(b).



(a) (b)

Figure 9.1 Topology development from TBSC to HBC

9.1.1 Inductive Switching Core (ISC) Development

The Inductive Switching Core (ISC) is a three terminal network that is composed of an electric energy source, one or more magnetic components (inductor, tapped-inductor, or transformer, etc.), and one or more switches. It pumps electrical charge to the BVM for voltage boosting purpose due to the "on" and "off" operation of the active switches.

Some examples of the ISC are given in Figure 9.2, including but not limited to Inductor-Switch(LS) core, Inductor-double switch(LSS) core, Transformer-Switch-Diode(TSD) core and Tapped inductor-Switch(TLS) core, shown as Figure 9.2(a)~(d). Their output terminals A, O and B should be connected to the input terminals A', O', B' of a bipolar voltage multiplier, thus a HBC topology can be generated.

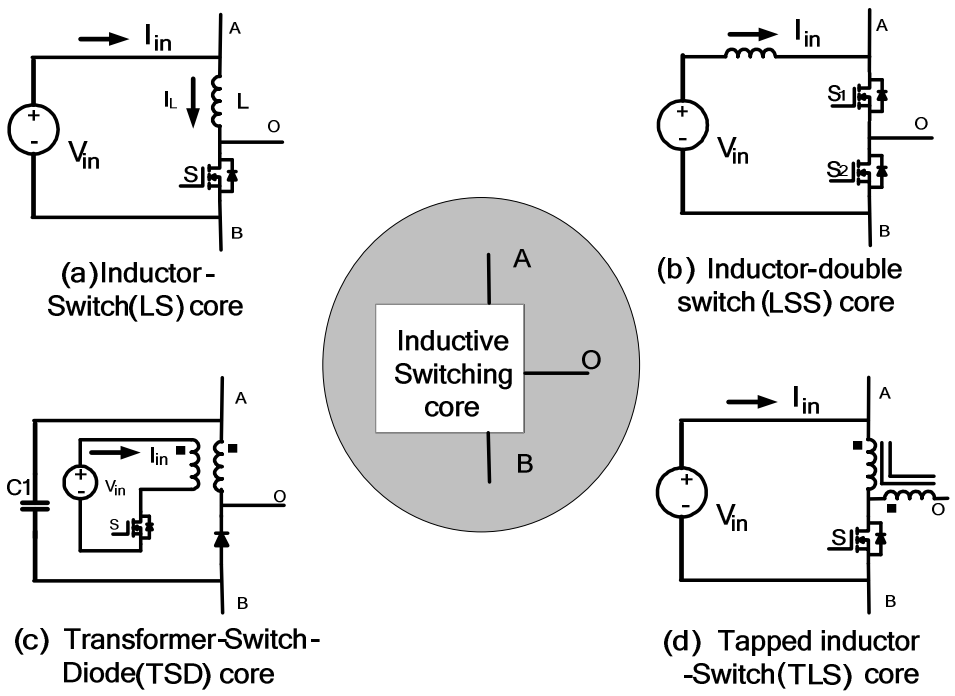


Figure 9.2 Inductive switching cores: LS, LSS, TSD, and TLS

The different inductive switching cores equipped with BVM can achieve different functionalities. Based on the inductive switching cores in Figure 9.2, four typical HBC family members are generated: Basic HBC, Symmetrical HBC, Isolated HBC and Tapped HBC.

The LS core which only contains an inductor and a switch evolves to the Basic HBC. It operates like cascading outputs of two boost converters, who are sharing the same inductor and switch. It is suitable for handling low power with moderate voltage gain. The Symmetrical HBC with ISS core is useful when input current needs to be continuous. The Isolated HBC with TRS core can be used when galvanic isolation is necessary. Tapped HBC with TAS core is suitable for super high gain applications. A brief comparison of the inductive switching cores is summarized in Table 9.1.

Table 9.1 Comparison of inductive switching cores

Inductive switching cores	Generated Converter	Pros	Cons
Inductor-Switch(IS) core	Basic HBC	Simplest	Pulsating input current
Inductor-Double Switch(ISS) core	Symmetrical HBC	Continuous input current	Two active switches, narrower duty cycle range
Transformer-Switch(TRS) core	Isolated HBC	Isolation	leakage problem
Tapped inductor-Switch(TAS) core	Tapped HBC	High gain	Leakage problem

9.1.2 Bipolar Voltage Multiplier Analysis

A BVM shown in dashed line of Figure 9.1(b) is comprised of two symmetrical branches: the positive branch and the negative branch. The input of a BVM has three terminals, A', B' and O', which should be connected with the three matching terminals of the inductive switching core A, B and O respectively. According to the diode number of one branch, the BVM can be classified into odd-order BMV and even-order BMV.

The even-order BVM contains capacitors C_{ia}(i=1,3,…,2n), diodes D_{ia}(i=1,2,…,2n) at positive branch and C_{ib}(i=1,3,…,2n), D_{ib}(i=1,3,…,2n) at negative branch, as shown in Figure 9.3(a),(b). The odd-order BVM contains C_{ia}(i=1,3,…,2n+1), D_{ia}(i=2,4,…,2n+1) at positive branch and C_{ib}(i=2,4,…,2n+1), D_{ib}(i=2,4,…,2n+1) at negative branch, as shown in Figure 9.3(c),(d).

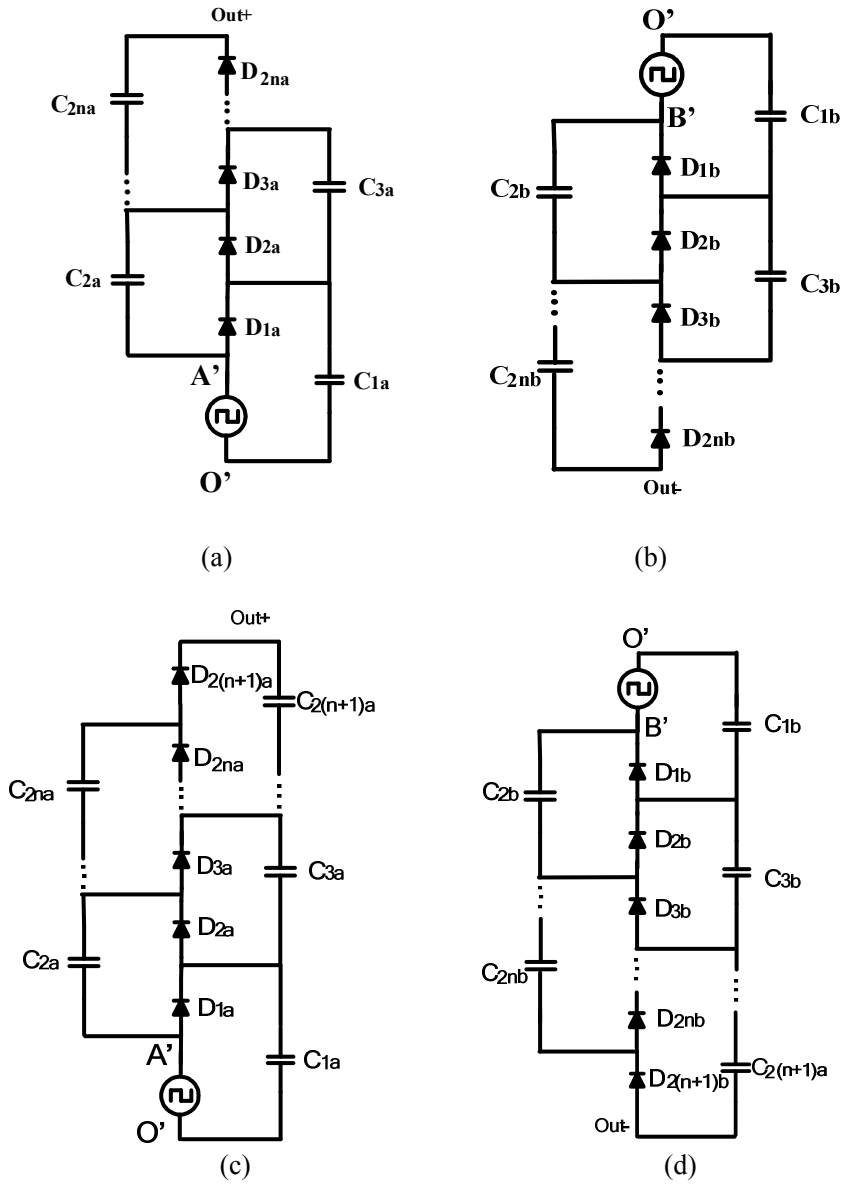


Figure 9.3 The positive branch and negative branch of BVM

(a) Positive branch of even-order BVM (b) Negative branch of even-order BVM

(c) Positive branch of odd-order BVM (d) Negative branch of odd-order BVM

In order to illustrate the operational principle of each HBC, the second-order bipolar voltage multiplier shown in Figure 9.4(a) is selected to connect with IS, TSD, TAS cores respectively. The ISS core which is only suitable for odd-order BVM is connected to a

third-order BVM shown in Figure 9.4(b), leading to a third-order Symmetrical HBC. All the formulated topologies are investigated with their voltage gains derived under CCM condition in following sections.

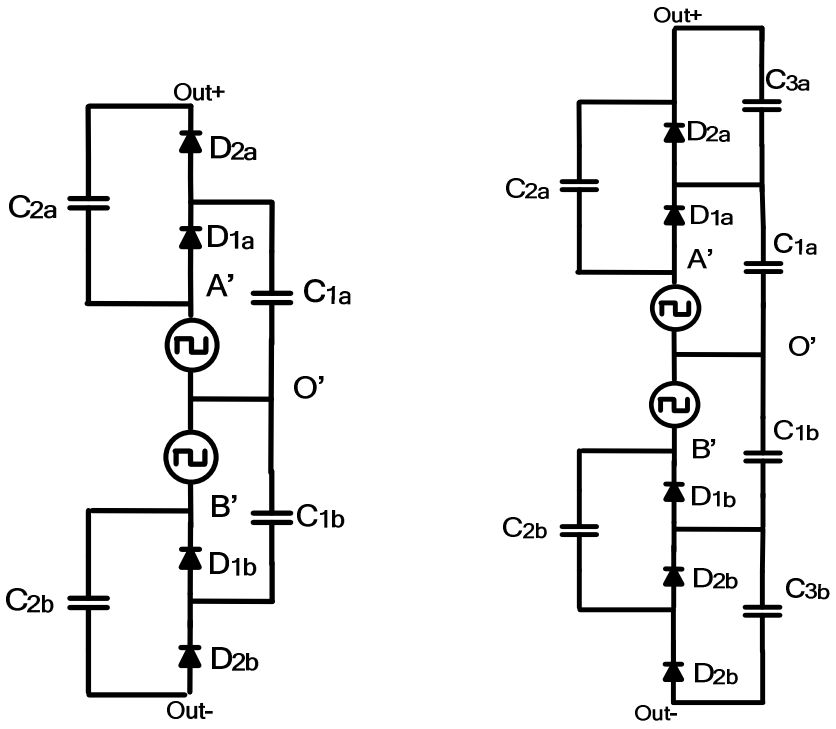


Figure 9.4 Example BVMs (a) second-order BVM (b) third-order BVM

9.2 Basic HBC

A Basic HBC is developed by combining the basic boost converter with the even/odd-order BVMs. It acquires the benefits of wide regulation capability from conventional boost converter and high gain boosting capability form BVM structure. The resulted basic HBC topology is featuring in simple control, easy regulation, low component stress and high efficiency. A second-order Basic HBC is shown in Figure 9.5.

The control circuit is as simple as the traditional boost converter. The Pulse Width Modulation (PWM) control strategy is adopted for regulation of basic HBC converter. Key circuit waveforms are described as in Figure 9.6.

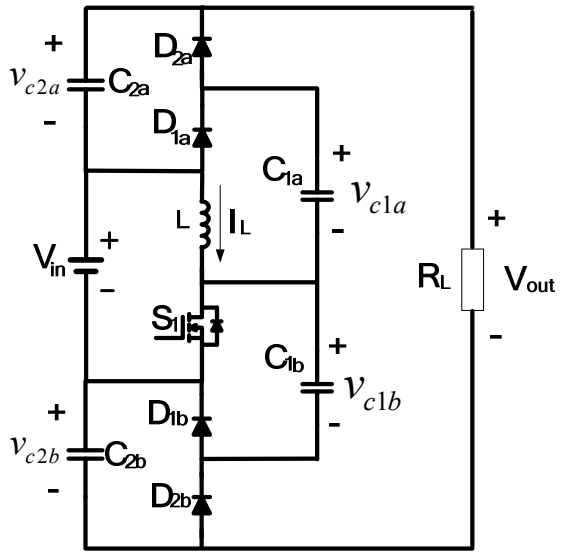


Figure 9.5 Second-order Basic HBC

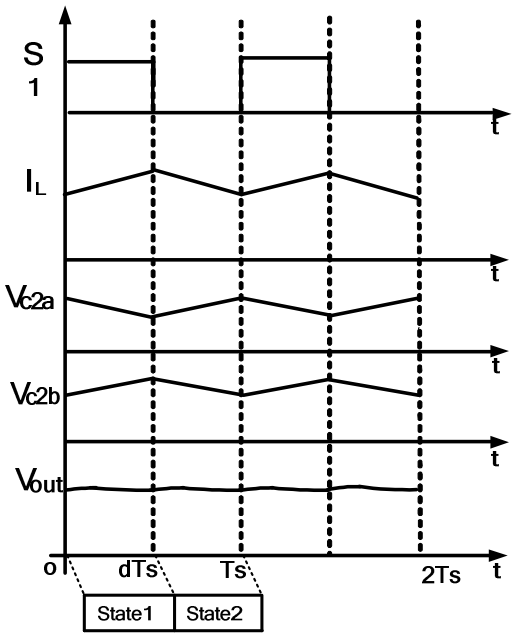


Figure 9.6 Key circuit waveforms of second-order basic HBC

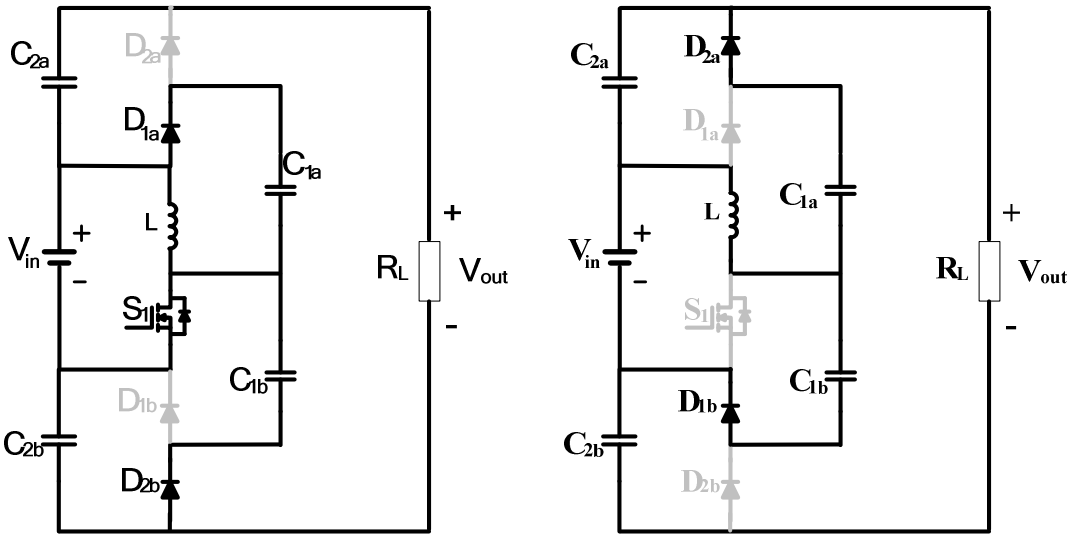


Figure 9.7 CCM operation modes of second-order Basic HBC

(a) State 1[0~dTs] (b) State 2[dTs~Ts]

Continuous Conduction Mode (CCM) indicates the inductor current I_L doesn't drop to zero for the whole switching period. When the second-order basic HBC is operating in CCM mode, only two operation states are derived, as shown in Figure 9.7.

1) State 1[0~dTs]

When switch S_1 is turned on, the converter is working in state 1 shown in Figure 9.7(a). The input source at low voltage side is magnetizing the inductor L. Moreover, it is charging capacitor C_{1a} by turning on diode D_{1a}. At the same time, capacitor C_{2b} is being charged by C_{1b} by turning on diode D_{2b} automatically. Therefore, the switch S_1 has to withstand current from inductor L and current of two coupled switched capacitor loops at the same time. At this state, the output voltage equals to the sum of input voltage and the voltage of C_{2a}, C_{2b}.

2) State 2[dTs~Ts]

When switch S_1 is turned off, the converter comes to state 2, shown in Figure 9.7(b). In this state, the circuit loop that contains V_{in}, L, C_{1b}, and D_{1b} is working as a boost converter at "off" state with the output of V_{c1b}. Meanwhile, the loop that contains C_{1a}, D_{2a}, C_{2a} and L is also working as another boost converter at "off" state, with the input voltage V_{c1a} and output voltage V_{c2a}. Thus, both boost circuits are sharing the same inductor L. At this state, the output voltage again equals to sum of input voltage and the voltage of C_{2a}, C_{2b}, same as state 1.

Therefore, it can be concluded the proposed structure brings following merits: (1) Realizing boosting capability of two boost converters while using only one set of inductor and switch (2) Employing flying capacitors C_{2a} and C_{2b} for dual functions of energy storage and ripple filtering.

Based on the waveforms shown in Figure 9.6 under CCM condition, the voltage ripples of capacitor C_{2a} and C_{2b} show opposite variation trend. Since the output voltage is built by cascading of C_{2a} and C_{2b}, the output voltage ripple is expected to be greatly suppressed compared with single boost converter.

Assuming all the components are ideal and the flying capacitors are large enough, the voltage of flying capacitor can be considered constant in steady state analysis. Based on inductor-second balance principle, the voltage gain of second-order basic HBC can be obtained as:

$$\frac{V_{out}}{V_{in}} = \frac{3-d}{1-d} \tag{9.1}$$

where d is the duty cycle of driving signal.

More details of converter performance, design and application of basic HBC will be investigated in Chapter 10.

9.3 Symmetrical HBC

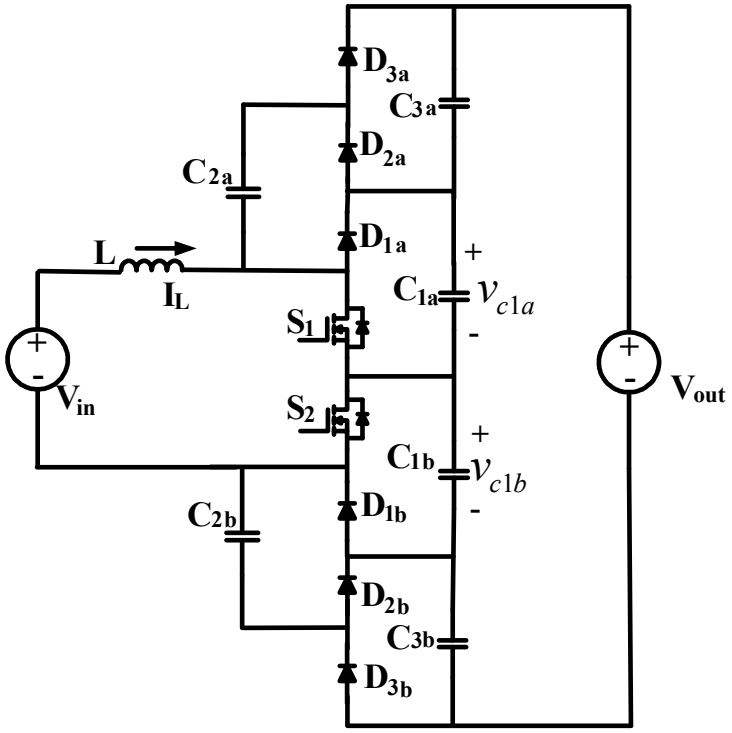


Figure 9.8 Third-order symmetrical HBC

The symmetrical HBC can be obtained by incorporating the LSS inductive switching core shown as Figure 9.2(b) with the odd-order BVM. When the third order BVM in Figure 9.4(b) is used, the derived third-order symmetrical HBC is shown as in Figure 9.8. With one more switch, the symmetrical HBC overcomes the drawback of pulsating input current of basic HBC. It has continuous input current and perfect interleaving structure, yielding equal and balanced voltages for all flying capacitors. The output voltage ripple is minimized with ripple cancelation between top flying capacitors and bottom flying

capacitors. The current ripple of inductor is also smaller compared with basic HBC due to the doubled equivalent switching frequency applied to the input inductor, allowing reduced inductance to be used.

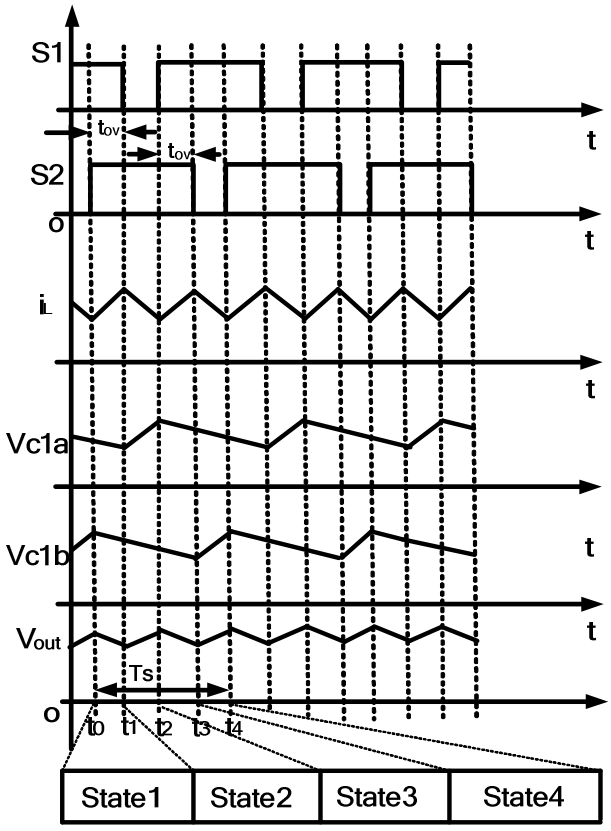


Figure 9.9 Overlaping interleaved PWM signal

The symmetrical HBC can be controlled by two interleaved and overlapping PWM signals, shown as S_1 and S_2 in Figure 9.9. Consequently, four operational states during each switching period are generated, shown as Figure 9.10, based on time sequence annotated. The other key circuit waveforms are also provided.

The overlapping duty cycle d_{ov} is defined by following equation:

$$d_{ov} = \frac{t_{ov}}{T_s / 2} \tag{9.2}$$

where t_{ov} is the overlapping time of two interleaved PWM signal. T_s is the switching period of each PWM signal.

Assuming the duty cycle of each PWM signal is d, the relationship between d and d_{ov} is given as:

$$d_{ov} = 2d - 1,\ 0.5 < d < 1 \tag{9.3}$$

The operational states can be briefly explained as following:

3) State 1[t0~t1]

At this state, switch S_1 and S_2 are both turned on. Inductor L is charged by input DC source V_{in}. At the same time, capcitor C_{1a} is charging capacitor C_{2a} and C_{1b} is charging C_{2b} through switched capacitor loops. Capacitor C_{1a}, C_{1b}, C_{3a} and C_{3b} are connected in serise to build up the output voltage and power the load together. At this state:

$$L\frac{di_L}{dt} = V_{in} \tag{9.4}$$

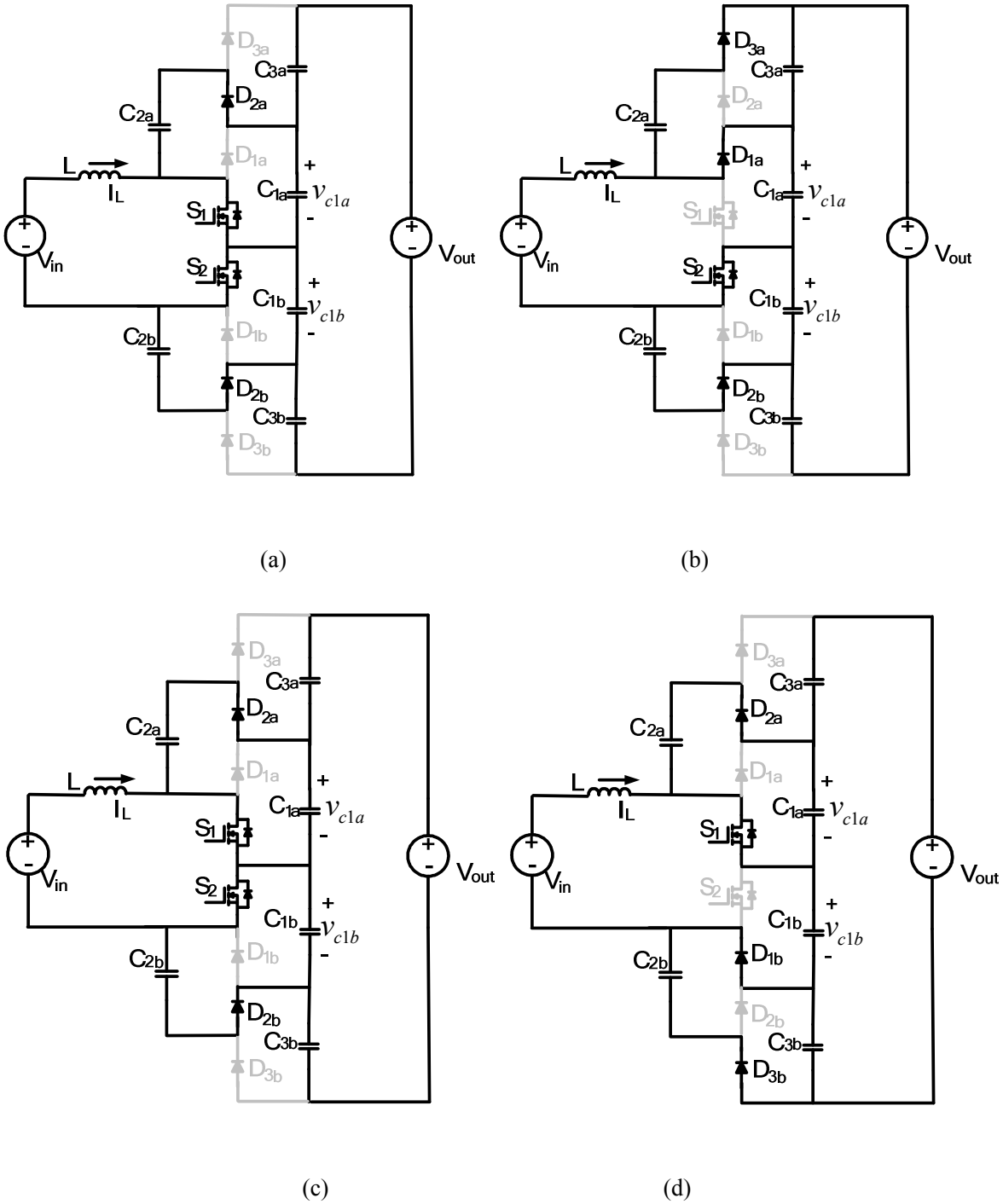


Figure 9.10 Operation states of third-order symmetrical HBC

(a) State 1[t0~ t1] (b) State 2[t1~ t2] (a) State 3[t2~ t3] (b) State 4[t3~ t4]

4) State 2[t1~t2]

At time t_1, switch S_1 is turned off while S_2 is kept on. Thus, the inductor energy is released to capacitor C_{1a}. At this state:

$$L\frac{di_L}{dt} = V_{in} - V_{c1a} \tag{9.5}$$

Meanwhile, capcitor C_{2a} is charging capacitor C_{3a} and deliveing power to load at same time. Capacitor C_{1b} continuously charging capacitor C_{2b}.

5) State 3[t2~t3]

At this state, switch S_1 is turned on again without turing off S_2. The configuration becomes exactely the same as state 1. Therefore:

$$L\frac{di_L}{dt} = V_{in} \tag{9.6}$$

6) State 4[t3~t4]

At this state, switch S_2 is turned off while S_1 is kept on. The inductor L starts to charge capacitor C_{1b}. Thus

$$L\frac{di_L}{dt} = V_{in} - V_{c1b} \tag{9.7}$$

At the same time, capacitor C_{1a} is charging C_{2a} . C_{2b} is discharging and C_{3b} is being charged.

Neglecting the voltage loss at voltage mulplier stages, according to voltage-second balance principle of input inductor, the voltage of C_{3a}, C_{1a}, C_{1b} and C_{3b} can be demonstrated to be equal to $V_{in}/(1-d_{ov})$. Therefore, the voltage gain of third-order symmetircal HBC is derived as follows:

$$\frac{V_{out}}{V_{in}} = \frac{4}{1-d_{ov}} \tag{9.8}$$

9.4 Isolated HBC

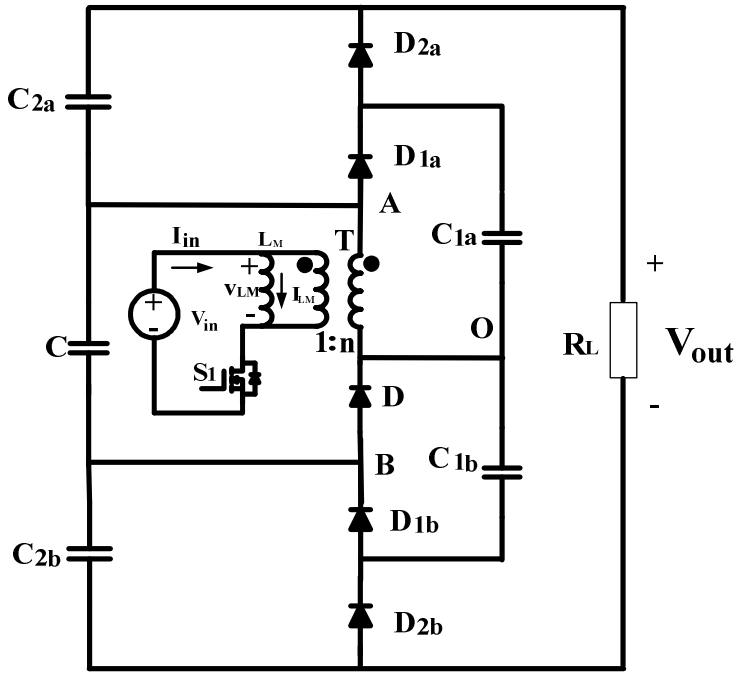


Figure 9.11 Second-order Isolated HBC

In order to derive the isolated version of HBC, a transformer with primary side connected to a voltage source and secondary side substituting Basic HBC inductor is inserted to the Basic HBC topology in Figure 9.5. The transformer has turn ration of n. The voltage source of Basic HBC is replaced by a capacitor C and the switch by a diode D. The obtained second-order Isolated HBC is shown in Figure 9.11.

With minimum components increase from second-order Basic HBC, the new isolated HBC topology can not only realize the galvanic isolation between source and load, but also eliminate the auxiliary magnetic resetting circuit due to its fly-forward operation

characteristics. In other words, when the switch S_1 is turned off, the stored magnetizing energy can find another circuit path at secondary side to be released while booting the voltage at the same time. This topology can be used in low power, high gain, isolation required applications with regulation capability.

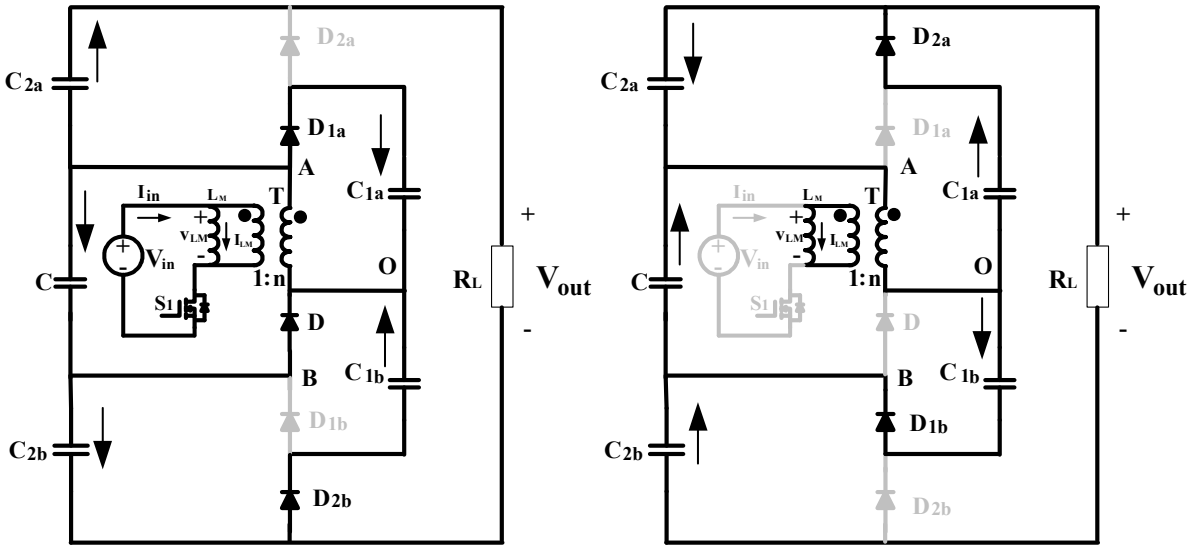


Figure 9.12 CCM operation states of second-order Isolated HBC

(a) State 1[0,dTs] (b) State 2 [dTs, Ts]

By applying same driving signal as basic HBC, the second-order Isolated HBC in CCM condition exhibits two modes shown in Figure 9.12. They are briefly discussed as follows:

1) State 1[0~dTs]

When switch S_1 conducts, the input voltage source V_{in} is applied on primary side of transformer T. The magnetizing current I_{LM} is increasing with slop of V_{in}/L_M. The secondary side with induced voltage of nV_{in} is charging capacitor C and C_{1a} at same time.

Capacitor C_{1b} is releasing its energy through secondary winding of transformer to charge C_{2b}, as shown in Figure 9.12(a).

2) State 2[dTs~Ts]

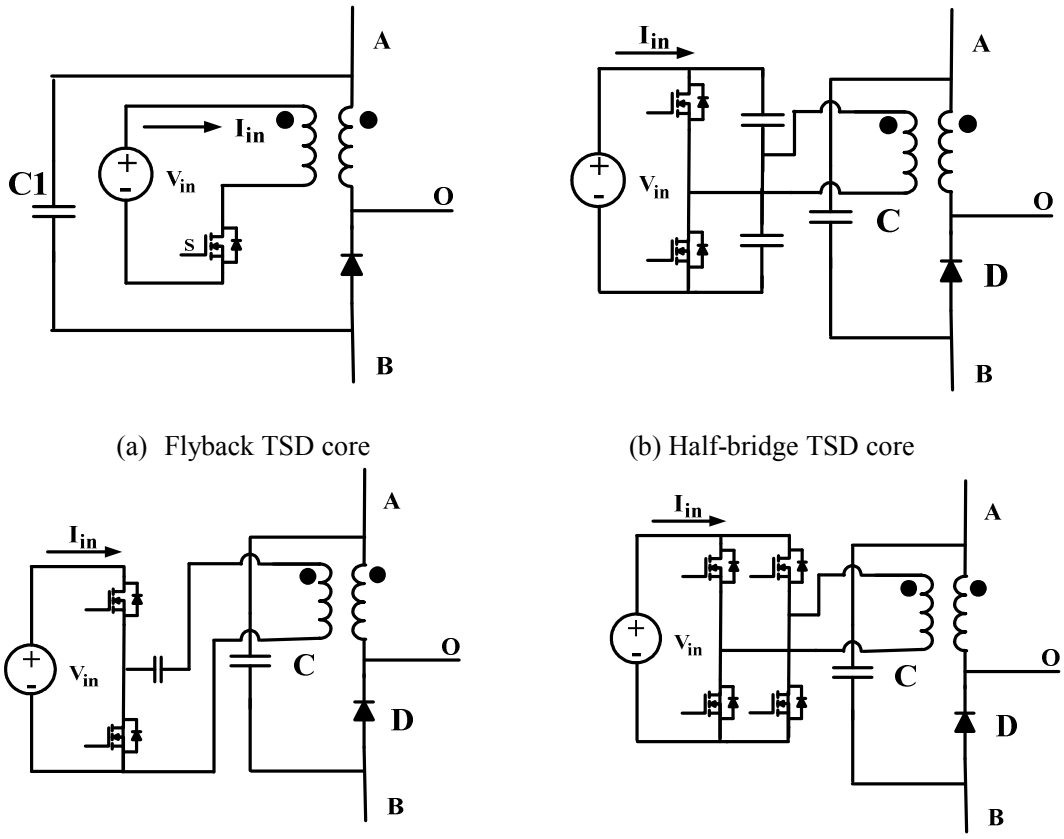
In Figure 9.12(b), as switch S_1 is off, the equivalent circuit model of transformer indicates that the magnetizing current is forced to flow into the primary side of the idea transformer, as no other current flow path can be found. According to the ampere-turn balance principle, a current of I_{LM}/n is induced at secondary winding of ideal transformer and flow into the dotted terminal. Therefore, the secondary winding will turn on D_{2a}, D_{1b} while D, D_{1a}, D_{1b} becomes revised biased. Thus, capacitors C_{1b} and C_{2a} are storing energy while capacitors C and C_{1a} are releasing energy. The power flow is indicated by arrows in Figure 9.12(b).

Based on voltage-second balance of magnitizing inductance, it can be found the voltage gain of third-order Isolated HBC in CCM mode is as follows:

$$\frac{V_{out}}{V_{in}} = n\frac{3-d}{1-d} \tag{9.9}$$

where d is the duty cycle of driving signal for S_1.

According to the magnetizing circuit configuration at primary side, four typical TSD cores are given as Figure 9.13(a)~(d): Fly-back TSD core, Half-bridge TSD, Resonant TSD core and full-bridge TSD core. By combining with BVM structure, different isolated high gain converters are expected.



(a) Flyback TSD core

(b) Half-bridge TSD core

(c) Resonant TSD core

(d) Full-bridge TSD core

Figure 9.13 Different configurations of TSD cores for Isolated HBC

9.5 Tapped HBC

If the inductor in Figure 9.5 is replaced by a tapped inductor with second winding connected between drain terminal of MOSFET S_1 and common point of C_{1a} and C_{1b}, the new topology Tapped HBC is created, as shown in Figure 9.14. Based on the proposed configuration, at least three major benefits are abstained:

First, reduced pulsating input current component will be achieved due to the current limitation function of second winding of tapped inductor. Therefore, the input filter can be reduced.

Second, pulsating current in voltage multiplier stage which exists in basic HBC is eliminated as well, which is beneficial in reducing component current stress and improve efficiency.

Last and most important, the voltage gain of the converter is greatly enhanced.

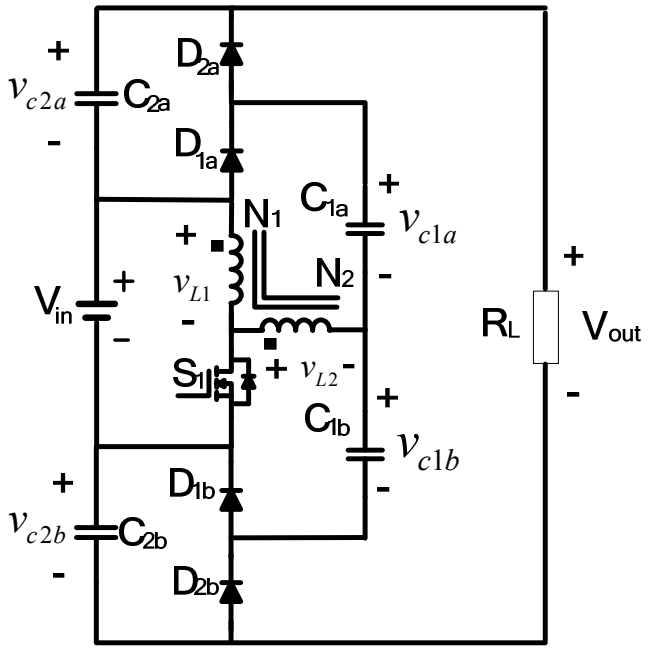


Figure 9.14 Second-order Tapped HBC

By employing the same driving signal of basic HBC and isolated HBC, the CCM operation states of proposed second-order Tapped HBC are derived in Figure 9.15(a) and (b). In order to simplify analysis, all flying capacitors are assumed to be big enough to sustain constant voltage in steady state. The leakage of tapped inductor is ignored and all the switches and diodes are considered ideal. The winding turn ratio of tapped inductor is assumed to be N_2/N_1. The magnetizing inductance at charging state and discharging state is regarded differently based on the associated turns.

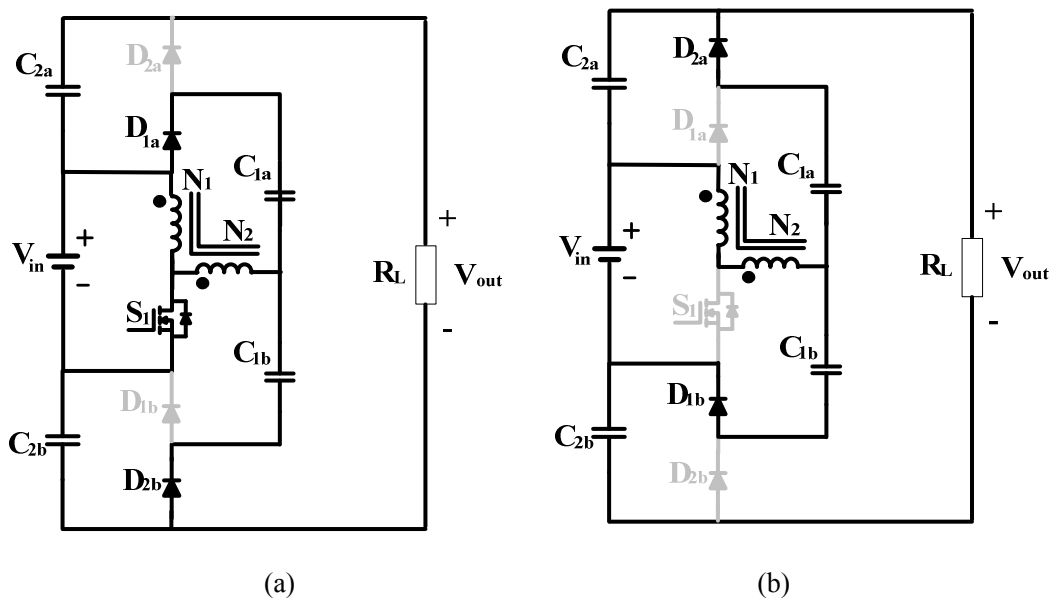


Figure 9.15 CCM operational states of second-order Tapped HBC

(a) State 1[0,dTs] (b) State 2 [dTs, Ts]

The operational stages are analyzed as follows:

1) State 1[0~dTs]

In Figure 9.15(a), the switch S_1 is turned on. The voltage source V_{in} is applied on primary winding of tapped inductor. Assuming the voltage drop on primary winding and secondary winding is V_{L1} and V_{L2} respectively. The voltage generated at secondary winding can be expressed:

$$V_{L2} = \frac{N_2 V_{in}}{N_1} \tag{9.10}$$

At the same time, the following equations can be obtained:

$$V_{c1a} = V_{in} + V_{L2} \tag{9.11}$$

$$V_{c2b} = V_{c1b} + V_{L2} \tag{9.12}$$

Substituting (9.10) to (9.11), the following equation can be obtained:

$$V_{c1a} = (1 + \frac{N_2}{N_1})V_{in} \tag{9.13}$$

During time interval [0~dTs], the increment of magnetizing current Δi_{LM1} shown in Figure 9.16 can be expressed as following:

$$\Delta i_{LM1} = \frac{V_{in}}{L_{m1}} dT_s \tag{9.14}$$

where L_{m1} is the magnetizing inductance during state 1, associated with primary turn number N_1 of tapped inductor.

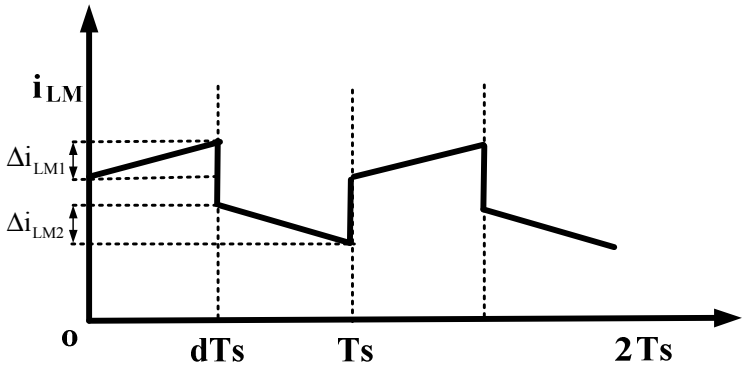


Figure 9.16 Magnetizing current with different mac

2) State 2[dTs~Ts]

When switch S_1 is turned off, the equivalent magnetizing inductance is switched to L_{m2}, associated with to total turn number of primary winding and secondary winding. As the

relationship between L_{m1} and L_{m2} is determined by the turn ratio based on definition of inductance, the following relationship is obtained:

$$\frac{L_{m2}}{L_{m1}} = (\frac{N_2 + N_1}{N_1})^2 \tag{9.15}$$

Therefore, the decrease of magnetizing current Δi_{LM2} at this state shown in Figure 9.16(b) can be expressed as follows:

$$\Delta i_{LM2} = \frac{V_{c1b} - V_{in}}{L_{m2}}(1-d)T_s \tag{9.16}$$

At the same time, the following equations can be obtained:

$$\mathrm{V_{c2a}} + V_{in} = V_{c1a} + V_{c1b} \tag{9.17}$$

From t=0_ to t=0+, and dTs- to dTs+, the energy stored in the magnetic element cannot lose suddenly. Therefore:

$$\frac{1}{2} L_{m2} {i_{Lm}}^2 (T_s-) = \frac{1}{2} L_{m1} {i_{Lm}}^2 (0+) \tag{9.18}$$

$$\frac{1}{2} L_{m1} {i_{Lm}}^2 (dT_s-) = \frac{1}{2} L_{m2} {i_{Lm}}^2 (dT_s+) \tag{9.19}$$

Based on**(9.15)**, **(9.18)** and **(9.19)**, the following relationship is derived:

$$\frac{\Delta i_{LM1}}{\Delta i_{LM2}} = \frac{i_{LM}(dT_s-) - i_{LM}(0+)}{i_{LM}(dT_s+) - i_{LM}(T_s-)} = \sqrt{\frac{L_{m2}}{L_{m1}}} = \frac{N_1 + N_2}{N_1} \tag{9.20}$$

According to (9.14), **(9.15)**, **(9.16)**, **(9.20)**, the following result can be obtained:

$$V_{c1b} = V_{in} \frac{\frac{N_2}{N_1} d + 1}{1 - d} \tag{9.21}$$

Substitute (9.10), **(9.21)** to (9.12), yielding

$$V_{c2b} = V_L \frac{\frac{N_2}{N_1} + 1}{1 - d} \tag{9.22}$$

Substitute (9.10),(9.11),**(9.21)** to **(9.17)**, yielding

$$V_{c2a} = V_L \frac{\frac{N_2}{N_1} + 1}{1 - d} \tag{9.23}$$

The output voltage can be expressed as:

$$V_{out} = V_{in} + V_{c2a} + V_{c2b} \tag{9.24}$$

Based on equation **(9.22)**, **(9.23)** and **(9.24)**, the voltage gain can be obtained as following:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{2}{1 - d} \frac{N_2 + N_1}{N_1} \tag{9.25}$$

9.6 Summary

In this chapter, the topology development of HBC family is illustrated. The two major topology construction parts, inductive switching core and bipolar voltage multiplier are investigated respectively. The four typical HBC family members: Basic HBC, Symmetrical HBC, isolated HBC and Tapped HBC are analyzed. Their operational principle under CCM condition is illustrated and the associated voltage conversion ratio is derived. Different merits based topologies of different HBC members are obtained.

Chapter 10 Analysis and Design of Basic HBC for Renewable Energy Applications

In Chapter 9, the HBC family was proposed and the basic operation principle of HBC family members was given. In this chapter, the general basic HBC converter is fully investigated for renewable energy applications. Since the basic HBC falls into the category of "Switch+Inductor+Diode-Capacitor" classified in Chapter 1, a brief review of topologies within this category is presented in section 10.1 for comparison purpose. The general high-order basic HBC topology is analyzed in section 10.2 with multiple voltage multiplier stages. Steady state analysis under CCM and DCM modes are discussed in section 10.3. Circuit performance is investigated in section 10.4. Simulation and experimental verifications are provided in section 10.5.

10.1 A review of topology category of "Switch+Inductor+Diode-capacitor"

In the past, many gain extension methods of boost converter by adding only diodes and capacitors were investigated. A collective of topologies that use single switch and single inductor in circuit configuration for voltage boosting is sampled in Figure 10.1. While the proposed second order Basic HBC is given in Figure 10.1(h) for comparison purpose.

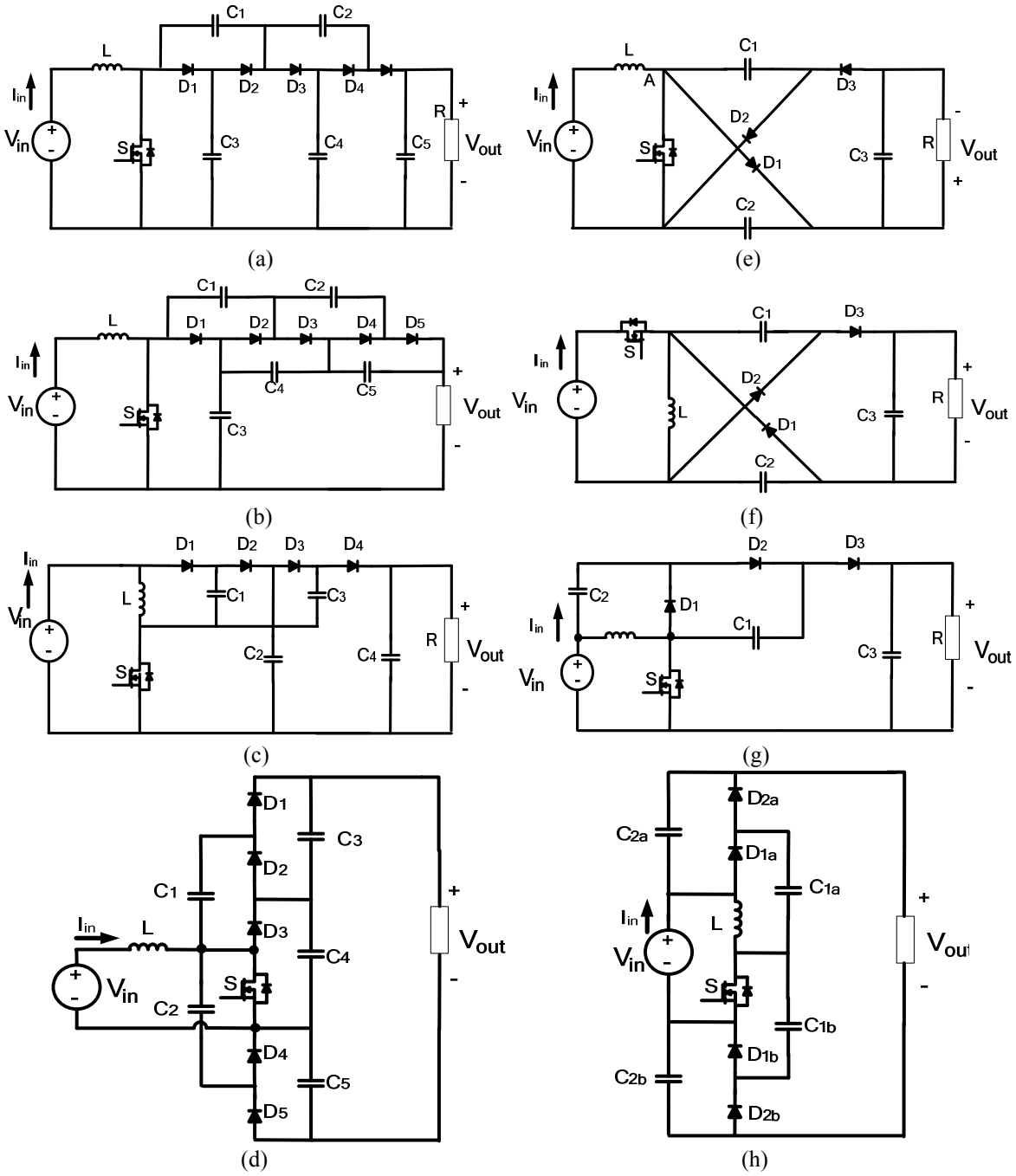


Figure 10.1 High-gain DC-DC converters with single-switch and single-inductor

(a) Boost+Dickson multiplier[30] , (b)Boost+Cockcroft- Walton multiplier[30], (c)Super-lift with elementary circuit [177], (d)Central source multilevel boost converter[55], (e)Cuk derived[45], (f)Zeta derived[45], (g) Modified voltage lifter[59], and (h) Proposed second-order HBC

The method of combining boost converter with the traditional Dickson multiplier and Cockcroft-Walton multiplier to generate new topologies was proposed in [30], leading to topologies shown in Figure 10.1(a) and (b). Air core inductor or stray inductor was used within voltage multiplier unit to reduce current pulsation in[178]. An elementary circuit employing the super lift technique was proposed in [177] and extended to higher gain applications such as Figure 10.1 (c). Its counterpart of negative output topology and double outputs topology were proposed and discussed in [14] and [17]. The concept of multilevel boost converters was investigated in [55] and the topology of Figure 10.1 (d) was given as central source connection converter. Besides, two switched capacitor cells were proposed in[45] and numerous topologies were derived by applying them to the basic PWM DC-DC converters . Typical topologies are shown as Figure 10.1 (e) and (f). A modified voltage-lift cell was proposed in [59] and the topology of Figure 10.1 (g) was produced.

All these topologies successfully enhanced the conversion ratio of traditional boost converter despite some remaining issues such as pulsating input current, high components stress and high output ripple, depending on their unique configurations. Recently, some other more complex structures achieved higher gain were also reported [42], [46], [60], [74], [96], [179],but they adopted at least two inductors or switches, which may complicate the circuit design and increase cost.

In this chapter, the proposed second-order HBC shown as Figure 10.1(h) is emphasized. Compared with the converter in Figure 10.1(d), the second-order HBC has smaller output ripple and higher components utilization rate with respect to conversion ratio. Compared with other topologies in Figure 10.1, second-order basic HBC decreases the size of the

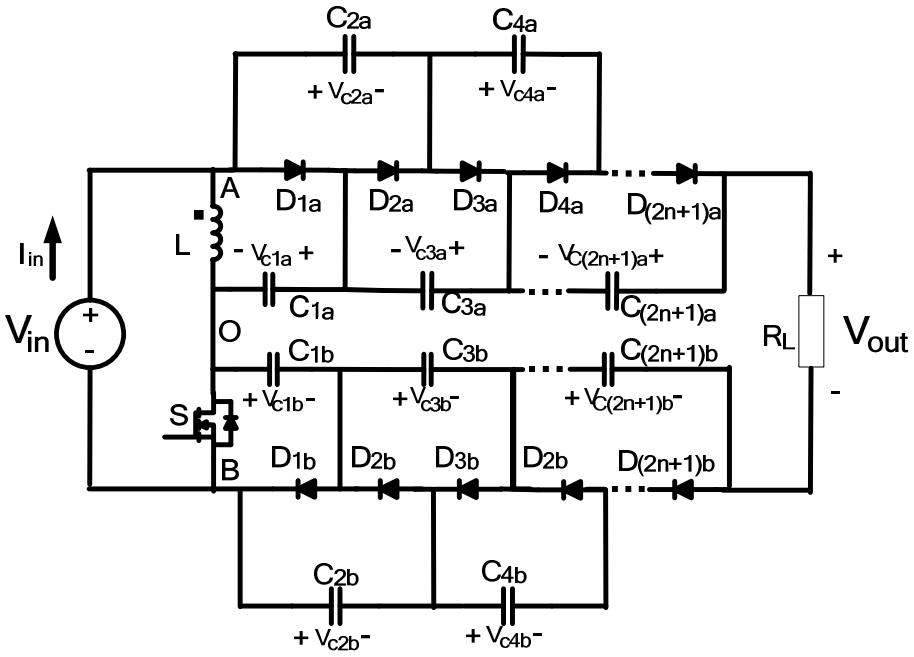
high voltage rating output filter capacitor and exhibits the nature interleaving operation characteristics.

Some Interleaving technologies for the enhanced boost converter were reported in literature aimed at increasing power level and reducing filter size [37], [180], but these methods were normally based on circuit branch expansion which requires more switches and inductors. The proposed second-order HBC has achieved some of the interleaving benefits with single switch and single inductor while maintaining high voltage gain.

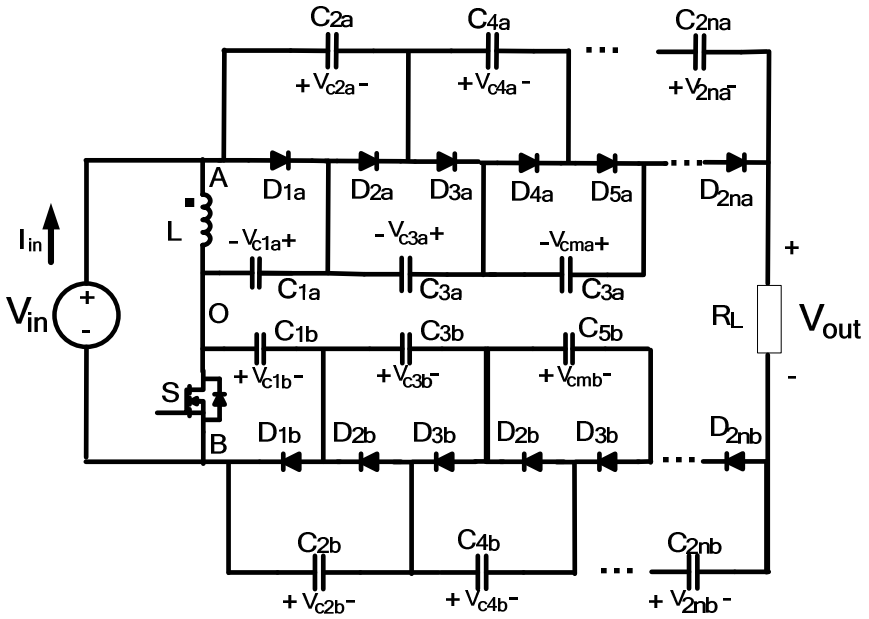
10.2 General HBC topology and its operational principle

The proposed HBC is shown in Figure 10.2. There are two versions of HBC, odd-order HBC and even-order HBC as shown in Figure (a) and (b). The even-order topology integrates the input source as part of the output voltage, leading to a higher components utilization rate with respect to the same voltage gain. Both share similar other characteristics and circuit analysis method. Therefore, the even-order topology is highlighted in this chapter.

In a basic HBC topology, the inductor, switch and input source serve as an “inductive switching core”, shown as Figure 10.3. It can generate two “complimentary” PWM voltage waveforms at port AO and port OB. Although the two voltage waveforms have their individual high voltage level and low voltage level, the gaps between two levels are identical, which is an important characteristic of inductive switching core to drive the BVM structure given in Figure 9.3.



(a)



(b)

Figure 10.2 Proposed General HBC topology (a) Odd-order HBC (b) Even-order HBC

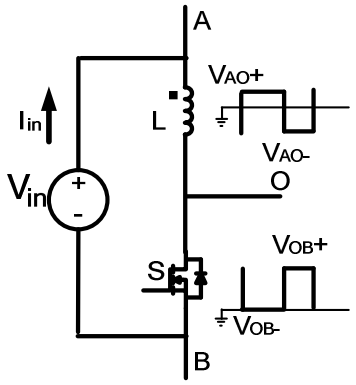


Figure 10.3 LS inductive switching core

10.2.1 Analysis of general BVM

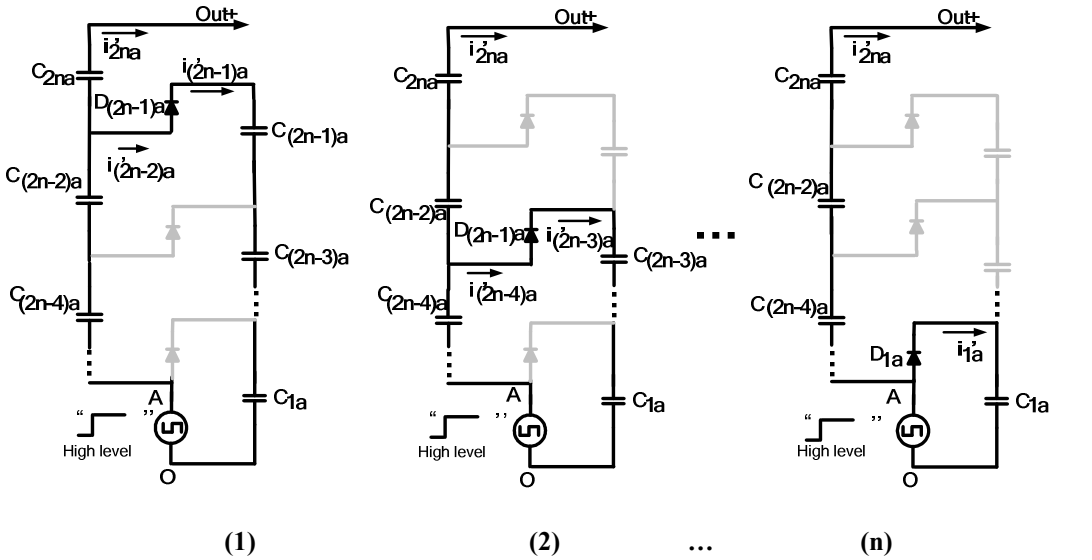
By defining the high voltage level at port AO as $V_{OA}+$, the low voltage level as $V_{OA}-$, and the duty cycle of high voltage level as d, the operational states of the even-order positive branch in Figure 9.3(a) can be derived as Figure 10.4. They are illustrated as follows:

1) State 1 [0, dTs]:

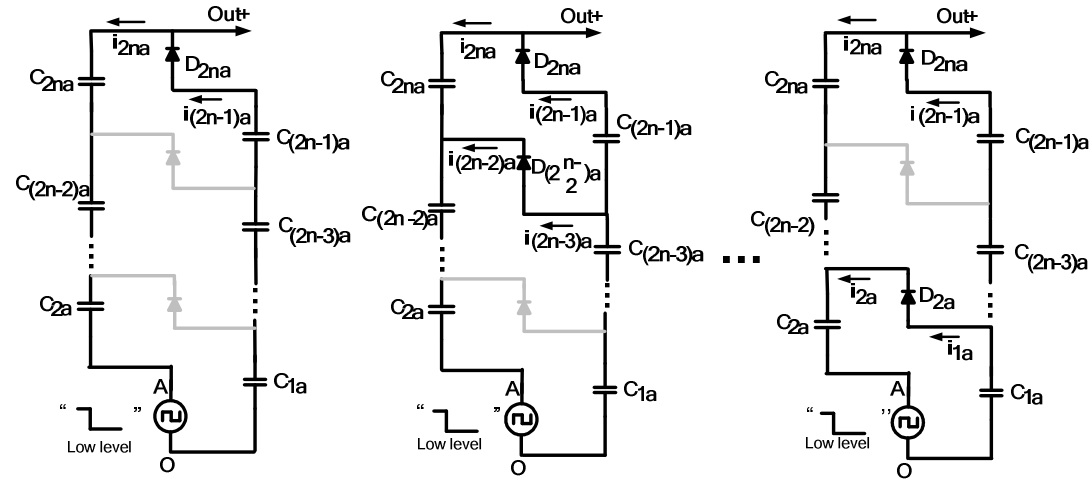
When the voltage at port AO is at high level, diodes D_{ia} (i=2n-1, 2n-3...3, 1) will be conducted consecutively. Each diode becomes reversely biased before the next diode with lower number fully conducts. The n sub-states are resulted as shown in Figure 10.4(a). Capacitor C_{ia} (i=2, 4...2n) are discharging during this time interval. Assuming the flying capacitors are large enough to maintain constant voltage and gets fully charged at steady state, while the diodes voltage drop are neglected, the follow relationship can be derived:

$$V_{c1a} = V_{AO+} \tag{10.1}$$

$$V_{cia} = V_{c(i+1)a} (i = 2,4,6,...,2n-2) \tag{10.2}$$



(a)State 1[0,dTs]



(b)State 2[dTs,Ts]

Figure 10.4 Operation States of even-order BVM positive branch

(a)State 1[0, dTs] (b)State 2[dTs,Ts]

2) State 2[dTs, Ts]:

When the voltage at port AO is at low level, diode D_{2na} is conducted first, shown as Figure 10.4(b). Then the diodes D_{ia} (i=2, 4,... 2n-2) will be turned on one after another from high number to low. Each diode will be turned on when the previous one becomes blocked. Only diode D_{2na} is conducted for the entire time interval of [0, dTs], since capacitor $C_{(2n-1)a}$ has to partially supply the load current during the whole time period of state 2. Although not all the diodes are conducted and blocked at the same time, the flying capacitors still have the following relationship by the end of state 2:

$$V_{c2a} = V_{cla} - V_{AO-} \tag{10.3}$$

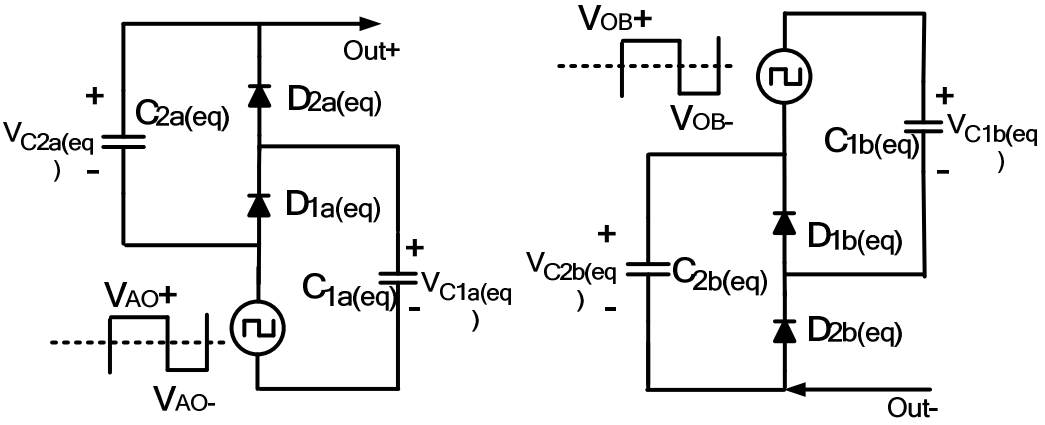
$$V_{cia} = V_{c(i+1)a} (i = 3,5,7,...,2n-1) \tag{10.4}$$

According to the charge balance principle, the total charge flowing into positive terminals of capacitors C_{ia} (i=2,4,...2n) should be equal to that coming out of them in a switching period at steady state, therefore, according to Figure 10.4:

$$\sum_{i=1}^{n} \int_{0}^{dT_S} i'_{2ia} dt = \sum_{i=1}^{n} \int_{dT_S}^{T_S} i_{2ia} dt \tag{10.5}$$

Thus the capacitor group $C_{ia}(i = 2,4,...2n)$ can be replaced by an equivalent capacitor $C_{2a(eq)}$. The diode group $D_{ia}(i = 2,4,...2n)$, which provides the charging path for $C_{2a(eq)}$ is equivalent to a single diode $D_{2a(eq)}$. Similarly, the capacitor group $C_{ia}(i = 1,3,...2n\text{-}1)$ can be replaced by an equivalent capacitor $C_{1a(eq)}$ and diode group $D_{ia}(i = 1,3,...2n\text{-}1)$ substituted by $D_{1a(eq)}$. Consequently, the equivalent circuit of even-order positive multiplier branch in

Figure 9.3(a) is given as Figure 10.5(a). By analogously analysis, the equivalent circuit of negative even-order multiplier branch in Figure 9.3(b) is shown in Figure 10.5(b).



(a) (b)

Figure 10.5 Equivalent circuit of even-order BVM

(a) Positive branch of even-order BVM (b) Negative branch of even-order BVM

According to equations (10.1)~(10.4), the voltage of equivalent capacitors $C_{1a(eq)}$, $C_{2a(eq)}$ can be expressed as follows:

$$V_{c2a(eq)} = n(V_{AO+} - V_{AO-}) \tag{10.6}$$

$$V_{c1a(eq)} = (n-1)(V_{AO+} - V_{AO-}) + V_{AO+} \tag{10.7}$$

For the negative branch shown in Figure 10.5(b), following results can be obtained based on similar analysis:

$$V_{c2b(eq)} = n(V_{OB+} - V_{OB-}) \tag{10.8}$$

$$V_{c1b(eq)} = (n-1)(V_{OB+} - V_{OB-}) + V_{OB+} \tag{10.9}$$

where V_{OB+} is the high voltage level at input OB and V_{OB-} is the low voltage level.

In order to derived the equivalent capacitance equation of $C_{2a(eq)}$ and $C_{1a(eq)}$, a voltage ripple based calculation method is proposed. Some assumptions are made to facilitate calculation: (1) Capacitors C_{ia} (i=1, 2, 3,...2n) have the same capacitance C (2) The peak to peak voltage ripple of each flying capacitor can be expressed as ΔV_{cia} (i=1, 2, 3...2n) while the ripple of equivalent capacitor $C_{2a(eq)}$ is assumed as ΔV.

Therefore, the following relationship can be approximated:

$$\Delta V = \Delta V_{c2a} + \Delta V_{c4a} + ...\Delta V_{c2na} \tag{10.10}$$

In Figure 10.4, assuming that the average current of $i'_{ia}(i = 1,2,...2n)$ during [0, dTs] is $\overline{i'_{ia(on)}}(i = 1,2,...2n)$ and the average current of $i_{ia}(i = 1,2,...2k)$ during [dTs, Ts] is $\overline{i_{ia(off)}}(i = 1,2,...2n)$, according to charge balance of capacitors C_{ia} (i=2, 4...2n), it can be derived that:

$$\overline{i'_{ia(on)}}dT_S = \overline{i_{ia(off)}}d'T_S(i = 2,4,...2n) \tag{10.11}$$

According to Figure 10.4(a), it can be derived that:

$$\overline{i'_{ia(on)}} = \overline{i'_{(i+1)\ a(on)}}(i = 2,4,...2n-2) \tag{10.12}$$

According to Figure 10.4(b), it can be derived that:

$$\overline{i_{ia(off)}} = \overline{i_{(i+1)\ a(off)}}(i = 1,3,...2n-3) \tag{10.13}$$

Based on the equations (10.11)~(10.13), the following relationship can be obtained:

$$\overline{i_{2a(off)}} = \overline{i_{4a(off)}} = ...\overline{i_{(2n-4)a(off)}} = \overline{i_{(2n-2)a(off)}} = \overline{i_{(2n-1)a(off)}} \tag{10.14}$$

Based on charge balance of capacitor C_{2na}, it can be derived that:

$$\overline{i_{2(n-1)a(off)}}d^{'}T_S = I_{out}T_S \tag{10.15}$$

$$\overline{i_{2na(off)}}d^{'}T_S = \overline{i'_{2na(on)}}dT_S = I_{out}dT_S \tag{10.16}$$

where $I_{out} = \frac{V_{out}}{R_L}$.

According to KCL in Figure 10.4(b), voltage ripple of capacitors C_{ia} (i=2, 4...2n) can be obtained as:

$$\begin{cases} C\Delta V_{c2a} = (\overline{i_{2na(off)}} + \overline{i_{2n-2a(off)}} + ...\overline{i_{4a(off)}} + \overline{i_{2a(off)}})d^{'}T_S \\ C\Delta V_{c4a} = (\overline{i_{2na(off)}} + \overline{i_{(2n-2)a(off)}} + ...\overline{i_{4a(off)}})d^{'}T_S \\ \quad .... \\ C\Delta V_{c2na} = \overline{i_{2na(off)}}d^{'}T_S \end{cases} \tag{10.17}$$

Where $d^{'} = 1 - d$.

Based on the equations from (10.14) to (10.16), the equation group (10.17) can be reduced to the following expression:

$$\begin{cases} C\Delta V_{c2a} = (n - 1 + d)I_{out}T_S \\ C\Delta V_{c4a} = (n - 2 + d)I_{out}T_S \\ \quad .... \\ C\Delta V_{c2ka} = (0 + d)I_{out}T_S \end{cases} \tag{10.18}$$

Substituting equation (10.18) to (10.10), the following equation is derived:

$$C\Delta V = (\frac{n(n-1)}{2} + nd)I_{out}T_S \tag{10.19}$$

Based on Figure 10.5(a), following equation can be easily derived based on discharging stage of equivalent capacitor $C_{2a(eq)}$:

$$C_{2a(eq)}\Delta V = I_{out}dT_S \tag{10.20}$$

By comparing equations (10.19) and (10.20), the equivalent capacitor $C_{2a(eq)}$ can be expressed:

$$C_{2a(eq)} = \frac{2d}{n(n-1+2d)}C \tag{10.21}$$

Similarly, in order to derive the equivalent capacitor of $C_{1a(eq)}$, the following equation can be derived:

$$\begin{cases} C\Delta V_{c1a} = nI_{out}T_S \\ C\Delta V_{c3a} = (n-1)I_{out}T_S \\ \quad .... \\ C\Delta V_{c2(n-1)a} = I_{out}T_S \end{cases} \tag{10.22}$$

At the meantime, the following equation exists:

$$C_{1a(eq)}\Delta V' = I_{out}T_S \tag{10.23}$$

where $\Delta V^{'} = \Delta V_{c1a} + \Delta V_{c3a} + ...\Delta V_{c(2n-1)a}$

According to (10.22) and (10.23) , the expression of $C_{1a\,(eq)}$ is obtained:

$$C_{1a(eq)} = \frac{2}{(n+1)n}C \tag{10.24}$$

Due to the symmetry, the equivalent capacitance $C_{1b(eq)}$ and $C_{2b(eq)}$ is given as following:

$$C_{1b(eq)} = \frac{2}{(n+1)n} C \tag{10.25}$$

$$C_{2b(eq)} = \frac{2d'}{n(n-1+2d')} C \tag{10.26}$$

The derivation of voltage and equivalent value of the equivalent flying capacitors can facilitate the output voltage calculation and ripple estimation for general BVM.

10.2.2 Steady state analysis of general basic HBC

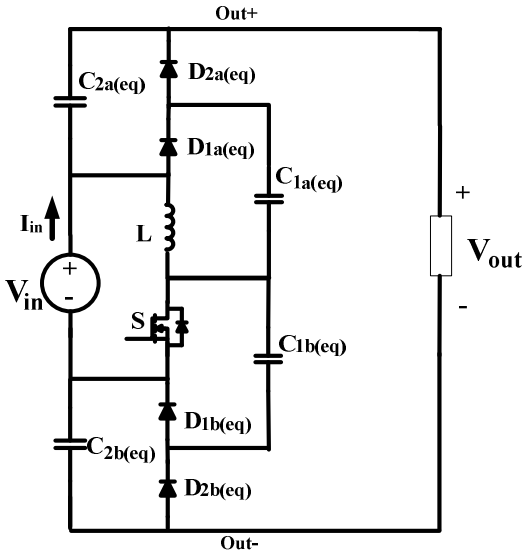


Figure 10.6 Equivalent circuit of general even-order Basic HBC

Based on the simplification method discussed in previous section, the general even-order Basic HBC in Figure 10.2(b) can be simplified to an equivalent Basic HBC circuit shown as Figure 10.6. It's similar to the second-order Basic HBC. The two "boost" like sub-circuits are intertwined through the operation of the active switch S. The total output voltage of HBC is the sum of the output voltage of two boost sub-circuits plus the input

voltage. Based on the inductor current waveform, the converter can operate under CCM or DCM conditions. The key waveforms under CCM and DCM operational conditions are presented in Figure 10.7(a) and (b). Three possible circuit states are given in Figure 10.8. The voltage at the two ports of inductive switching core AO and OB in each mode is calculated and annotated in Figure 10.7.

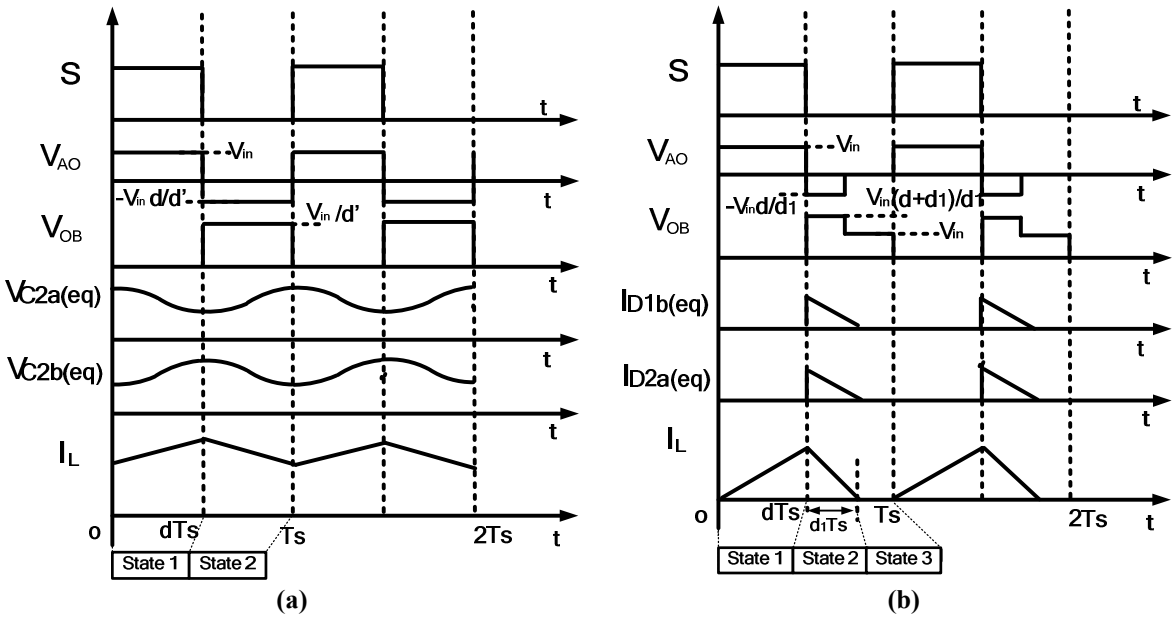


Figure 10.7 Key waveforms of even-order HBC

(a) CCM (b) DCM

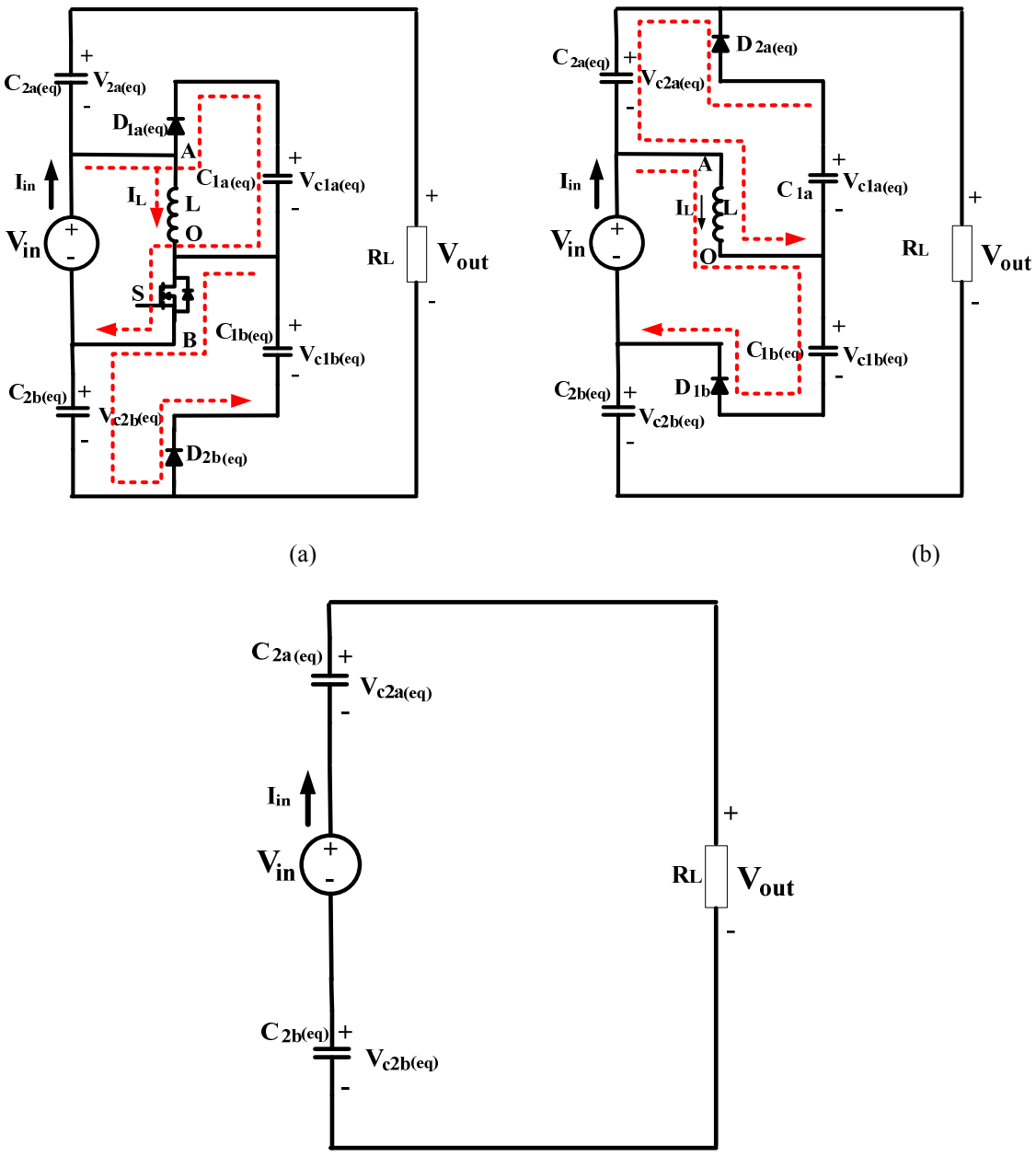


Figure 10.8 Three operation states of Basic even-order HBC

(a) State 1[0,dT_s]. (b)State 2[dT_s, $(d + d_1)T_s$]. (c)State 3[$(d+ d_1)T_s$, T_s]

1) Voltage gain derivation in CCM mode

Under CCM condition, $d_1 = 1 - d = d'$. Only state 1 and state 2 in Figure 10.8(a) and (b) occurs. During State 1[0, dTs], switch S is turned on and diodes $D_{1a(eq)}$, $D_{2b(eq)}$ conduct while diodes $D_{2a(eq)}$ and $D_{1b(eq)}$ are reversely biased. The following equations can be derived:

$$V_{AO+} = V_{in} \tag{10.27}$$

$$V_{OB-} = 0 \tag{10.28}$$

During State 2 as described in Figure 10.8(b), when S is turned off, the inductor current will free wheel through diodes $D_{2a(eq)}$ and $D_{1b(eq)}$. The inductor is shared by the two charging boost loops. During this time interval, voltage generated at AO and OB is expressed as following based on inductor balance principle:

$$V_{AO-} = -V_{in}\frac{d}{d'} \tag{10.29}$$

$$V_{OB+} = \frac{V_{in}}{d'} \tag{10.30}$$

Based on equations (10.6) and (10.8), the equivalent voltage of $C_{2a(eq)}$ and $C_{2b(eq)}$ is obtained as:

$$V_{c2a(eq)} = n(V_{AO+} - V_{AO-}) = n\frac{V_{in}}{d'} \tag{10.31}$$

$$V_{c2b(eq)} = n(V_{OB+} - V_{OB-}) = n\frac{V_{in}}{d'} \tag{10.32}$$

Therefore, the voltage gains of general 2n-order HBC shown in Figure 10.6 is derived as following:

$$\frac{V_{out}}{V_{in}} = 1 + 2n\frac{1}{d'} \tag{10.33}$$

2) Voltage gain derivation in DCM mode

Under DCM operation mode, the waveforms of voltage at input V_{AO}, V_{OB} are shown in Figure 10.7(b). The duration of state 2 becomes [dTs, $(d+d_1)$Ts]. The third state in Figure 10.8(c) appeals. In state 1, the voltage of port AO and OB is the same as CCM condition.

However, in state 2, the port voltage of inductive switching core should be modified to following equations:

$$V_{AO-} = -V_{in}\frac{d}{d_1} \tag{10.34}$$

$$V_{OB+} = \frac{(d + d_1)V_{in}}{d_1} \tag{10.35}$$

At state 3, the switch S is kept off, the inductor current has dropped to zero and all the diodes are blocked. During this time interval, voltage generated at port AO and OB can be expressed as:

$$V_{AO-} = 0 \tag{10.36}$$

$$V_{OB+} = V_{in} \tag{10.37}$$

Since the voltages used in equations (10.6) and (10.8) are the peak values. Thus, the voltage derived at state 3 is not used for calculation. Based on state 1 and state 2, the gain of DCM condition can be expressed as:

$$V_{out} = V_{in} + n(V_{OA+} - V_{OA-}) + n(V_{OB+} - V_{OB-}) = V_{in} + 2nV_{in}\frac{d + d_1}{d_1} \quad \textbf{(10.38)}$$

In Figure 10.7(b), the inductor current can be expressed as follows during state 2:

$$I_L = I_{D2a(eq)} + I_{D1b(eq)} \quad \textbf{(10.39)}$$

According to charge balance principle of the circuit:

$$\overline{I_{D2a(eq)}} = \overline{I_{D1b(eq)}} = I_{out} \quad \textbf{(10.40)}$$

where $\overline{I_{D2a(eq)}}$ and $\overline{I_{D1b(eq)}}$ are the average current in the whole switching period.

As current waveforms of $I_{D2a(eq)}$ and $I_{D2a(eq)}$ both exhibit triangle profiles, they should have proximately same peak value, which shall inductor peak current equally. Therefore:

$$I_{D2a(eq)p-p} = I_{D1b(eq)p-p} = \frac{1}{2}\frac{V_{in}}{L}dT_S \quad \textbf{(10.41)}$$

Since the average current of $I_{D2a(eq)}$ in a switching period is I_{out}, thus:

$$\frac{1}{2}d_1T_S\frac{1}{2}\frac{V_{in}}{L}dT_S\frac{1}{T_S} = I_{out} \quad \textbf{(10.42)}$$

This can be simplified to:

$$d_1 = \frac{4I_{out}L}{V_{in}T_S d} \quad \textbf{(10.43)}$$

Substituting equation (10.43) to equation (10.38), the following equation can be derived:

$$V_{out} = V_{in} + 2n(V_{in} + \frac{V_{in}^2 d^2 T_S}{4 I_{out} L}) \tag{10.44}$$

Solving the equation (10.44) gives the voltage gain in DCM mode:

$$\frac{V_{out}}{V_{in}} = \frac{2n+1+\sqrt{(2n+1)^2 + n\frac{2d^2 T_S R_L}{L}}}{2} \tag{10.45}$$

3) BRM mode analysis

In order to derive boundary condition for CCM and DCM mode, the average power balance between input and output is used:

$$V_{in}(\overline{I_L} + \overline{I_{D1a(eq)}}) = V_{out} I_{out} \tag{10.46}$$

Where $\overline{I_{D1a(eq)}} = I_{out} = \frac{V_{out}}{R_L}$

Thus, the average current of I_L under CCM condition is:

$$\overline{I_L} = \frac{2n}{d'}\frac{V_{out}}{R_L} \tag{10.47}$$

The current ripple of inductor is:

$$\Delta i_L = \frac{V_{in}}{2L} d T_S \tag{10.48}$$

Therefore, circuit condition for CCM condition is:

$$\frac{2n}{d'}\frac{V_{out}}{R_L} > \frac{V_{in}}{2L} d T_S \tag{10.49}$$

The criteria can be described as:

$$\frac{2L}{R_L T_S} > \frac{dd^{'2}}{2n(d^{'} + 2n)} = K_{crit}(d) \tag{10.50}$$

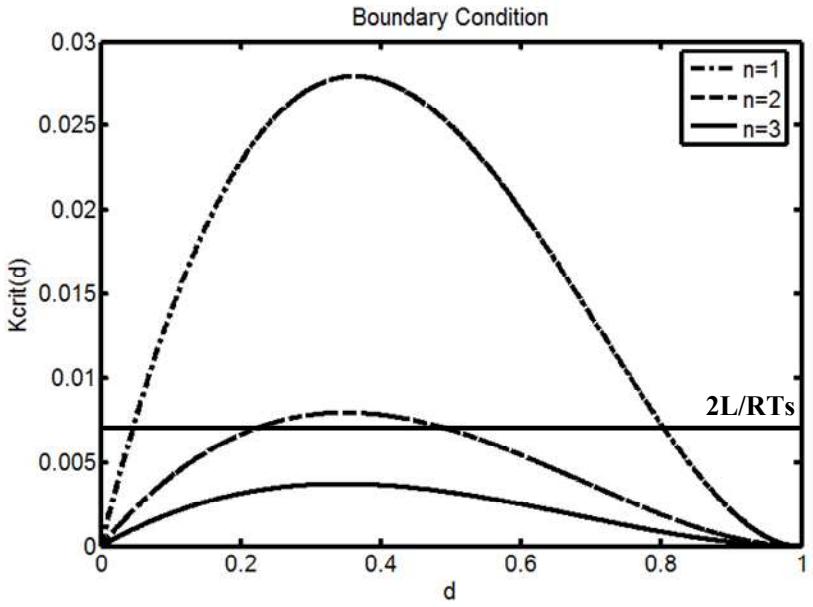


Figure 10.9 $K_{crit}(d)$ **with variation of n**

The curves of $K_{crit}(d)$ with n=1, 2, 3 are shown in Figure 10.11. It can be seen that when the voltage multiplier stage increases, it's easier to achieve CCM when other parameters are fixed.

10.3 Converter Performance Analysis

10.3.1 Component stress analysis

Detailed analysis of components stress for the converter provides solid reference for components selection and optimization. The components stress under CCM mode is estimated in this section.

1) Diodes and Switch

According to the charge balance principle of flying capacitors, all the diodes $D_{ia}(i=1,2,3...2n)$ and $D_{ib}(i=1,2,3...2n)$ have the same average current I_{out} during one switching period. The average current during conduction state is used to calculate I_{rms} here. The current of switch S during "on" state is composed of current from inductor, charging current of C_{1a} and discharging current of C_{1b}.

The average inductor current can be calculated as:

$$I_L = \overline{I_{in}} - \overline{I_{D1a}} = \frac{V_{out} I_{out}}{V_{in}} - I_{out} = 2n\frac{I_{out}}{d'} \tag{10.51}$$

According to the analysis in Figure 10.4(a), the average changing current of C_{1a} during switch "on" state can be found as:

$$\overline{I_{c1a(on)}} = n\frac{I_{out}}{d} \tag{10.52}$$

Similarly, the average current of C_{1b} during switch "on" state can be found as:

$$\overline{I_{c1b(on)}} = -n\frac{I_{out}}{d} \tag{10.53}$$

Based (10.51)~(10.53), the average current of switch S during "on" state can be derived:

$$\overline{I_{s(on)}} = 2n\frac{I_{out}}{d} + 2n\frac{I_{out}}{d'} = 2n\frac{I_{out}}{dd'} \tag{10.54}$$

The current waveforms of diodes and switch are shown in Figure 10.10. Their current stress and voltage stress are calculated in Table 10.1.

Table 10.1.

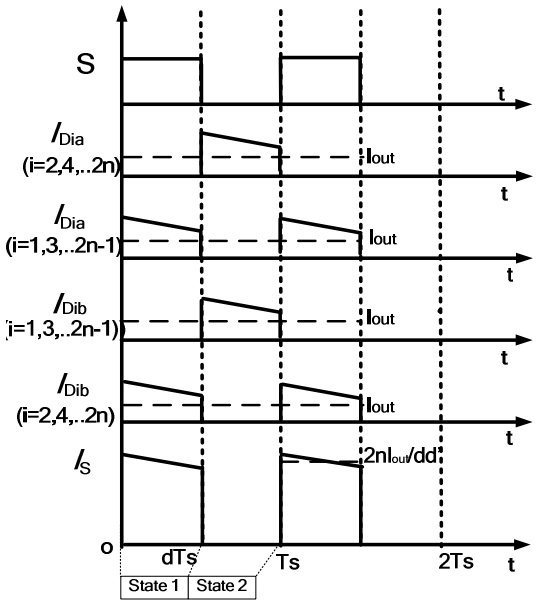


Figure 10.10 Current waveforms of Diodes and Switch

2) Capacitors

According to the analysis of bipolar voltage multiplier in Figure 10.4, the flying capacitors that are closer to inductive switching core have a larger charging and discharging current, which exhibits larger voltage ripple. Their average charging and discharging current can be used to estimate the RMS current, which is useful to evaluate power loss of each capacitor. The expressions of RMS current for each capacitor in a 2n-order HBC are also given in Table 10.1.

Table 10.1 Components Stress

Components	$V_{\max}$	I_{ave}	I_{rms}
S	$\frac{V_{in}}{d'}$	$\frac{2kI_{out}}{d'}$	$2n\frac{I_{out}}{\sqrt{d}d'}$
$D_{ia}(i=1,3...2n-1)$ $D_{ib}(i=2,4...2n)$	$\frac{V_{in}}{d'}$	I_{out}	$\frac{I_{out}}{\sqrt{d}}$
$D_{ia}(i=2,4...2n)$ $D_{ib}(i=1,3...2n-1)$	$\frac{V_{in}}{d'}$	I_{out}	$\frac{I_{out}}{\sqrt{d'}}$
C_{1a}	V_{in}	0	$nI_{out}\sqrt{\frac{1}{dd'}}$
$C_{ia}(i=3,5...2n-1)$	$\frac{V_{in}}{d'}$	0	$(n-\frac{i-1}{2})I_{out}\sqrt{\frac{1}{dd'}}$
$C_{ib}(i=1,3...2n-1)$	$\frac{V_{in}}{d'}$	0	$(n-\frac{i-1}{2})I_{out}\sqrt{\frac{1}{dd'}}$
$C_{ia}(i=2,4...2n)$	$\frac{V_{in}}{d'}$	0	$((n-\frac{i}{2})\frac{I_{out}}{d}+I_{out})\sqrt{\frac{d}{d'}}$
$C_{ib}(i=2,4...2n)$	$\frac{V_{in}}{d'}$	0	$((n-\frac{i}{2})\frac{I_{out}}{d'}+I_{out})\sqrt{\frac{d}{d'}}$

10.3.2 Voltage ripple analysis

The output voltage ripple is determined by the ripple of equivalent capacitor $C_{2a(eq)}$ and $C_{2b(eq)}$ .Assuming the input source has a constant voltage. As the equivalent capacitance of

$C_{2a(eq)}$ and $C_{2b(eq)}$ are given as equation (10.21) and (10.26), the voltage ripple of $C_{2a(eq)}$ and $C_{2b(eq)}$ can be presented as following:

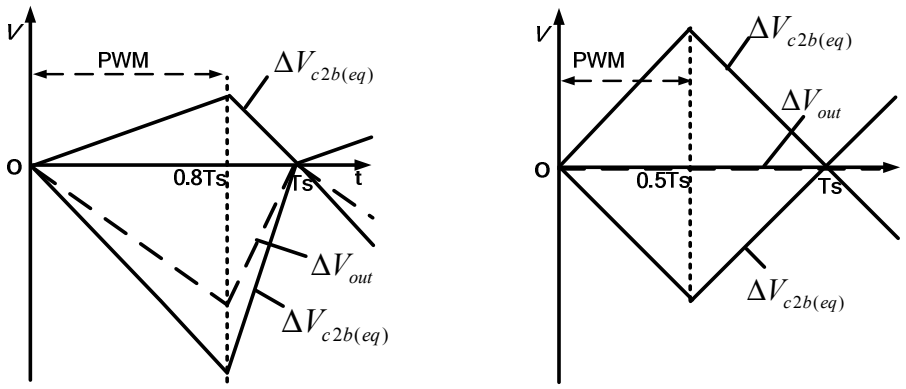
$$\Delta V_{c2a(eq)} = \frac{I_{out}T_S}{2C} n(n-1+2d) \tag{10.55}$$

$$\Delta V_{c2b(eq)} = \frac{I_{out}T_S}{2C} n(n-1+2d') \tag{10.56}$$

The final output ripple can presented as following:

$$\Delta V_{out} = |\Delta V_{c2a(eq)} - \Delta V_{c2b(eq)}| = \frac{I_{out}T_S}{C} n|2d-1| \tag{10.57}$$

According to the equation (10.57), when the duty cycle d is 0.5, the theoretical output voltage ripple is zero. The ripple examples of d=0.8 and 0.5 are compared in Figure 10.11(a) and (b). It can be concluded the interleaving operation has led to ripple cancellation of the capacitors $C_{2a(eq)}$ and $C_{2b(eq)}$.



(a) (b)

Figure 10.11 Voltage ripple cancellation with different duty cycle

(a)d=0.8 (b) d=0.5

10.3.3 Comparison of Basic HBC with previous converters

In order to distinguish the proposed Basic HBC converter, a comparison is carried out between the second-order Basic HBC converter and several previous published converters with single inductor and single switches shown in Table 10.1.

Table 10.1(a)~(h). All capacitors are assumed to have the same value C for easier comparison. Component voltage stress and output voltage ripple are normalized as shown in Table 10.2. The voltage gain, component count, as well as normalized switch stress and normalized output ripple are all listed for each topology.

The absolute voltage gain curves for all topologies presented in Figure 10.1 are plotted in Figure 10.12. The proposed second-order basic HBC has good gain boosting capability but not highest. However, it's difficult to judge the performance of each configuration merely based on the level of its gain curve, especially with consideration of different components count for different topologies. Most of the topologies can extend their gain by adding more stags with a larger number of capacitors and diodes. Therefore, more details should be taken into consideration to evaluate topologies, such as total normalized capacitor voltage rating and normalized output voltage ripple.

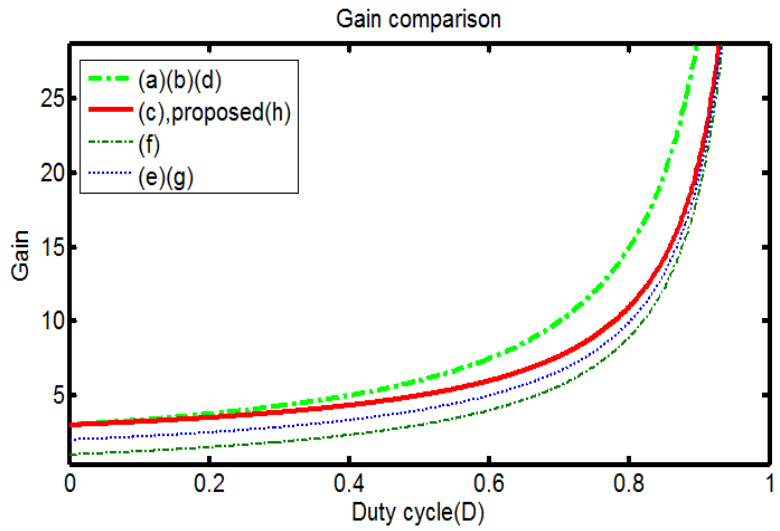


Figure 10.12 Comparison of voltage gain

Table 10.2 Comparison of proposed second-order HBC with other converters

Figure 10.1	Converters	Voltage gain	Diodes	Capacitors	$M_{\text{s\_stress\_norm}} = V_{s\_stress} / V_{out}$	$M_{\text{ripple\_norm}} = \Delta V_{out} / \frac{V_{out} T_s}{R_L C}$
(a)	Boost+Dickson Multiplier[30]	$\frac{3}{1-d}$	5	5	1/3	d
(b)	Boost+Cockcroft Walton Multiplier[30]	$\frac{3}{1-d}$	5	5	1/3	$3+3d$
(c)	Super-lift Converter[177]	$\frac{3-d}{1-d}$	4	4	1/(3-d)	d
(d)	Multilevel Boost Converter[55]	$\frac{3}{1-d}$	5	5	1/3	$3d$
(e)	Cuk-derived Converter[45]	$-\frac{2}{1-d}$	3	3	1/2	$1-d$
(f)	Zeta-derived Converter[45]	$\frac{1+d}{1-d}$	3	3	1/(1+d)	$1-d$
(g)	Modified voltage Lift Converter[59]	$\frac{2}{1-d}$	3	3	1/2	d
(h)	Proposed HBC	$\frac{3-d}{1-d}$	4	4	1/(3-d)	$\lvert 2d-1 \rvert$

For the high gain DC-DC converters with single switch and inductor, a critical aspect to realize high power density and low cost is to decrease the size of capacitors. Diodes usually have comparably much smaller volume, whose effect to the power density is neglected in this comparison. The voltage rating and value are the primary factors that affect the size of each capacitor. In order to compare the density of each topology with same gain, the normalized voltage stresses of capacitors for each topology are calculated in Table 10.3. The normalized voltage stresses are defined as the actual voltage stress divided by the output voltage V_{out}. The total normalized capacitor voltage stress is the sum of all capacitor voltage ratings, which has taken into account the capacitor number and voltage ratings. This parameter can be used to evaluate the volume of high gain DC-DC converters with single switch and inductor.

Table 10.3 Comparison of Normalized Capacitor Voltage Stress for Converters

Figure 10.1	C1 (V_{c1}/V_{out})	C2 (V_{c2}/V_{out})	C3 (V_{c3}/V_{out})	C4 (V_{c4}/V_{out})	C5 (V_{c5}/V_{out})	Total normalized capacitor voltage stress
(a)	1/3	1/3	1/3	2/3	1	8/3
(b)	1/3	1/3	1/3	1/3	1/3	5/3
(c)	(1-d)/(3-d)	(2-d)/(3-d)	(2-d)/(3-d)	1	0	(8-4d)/(3-d)
(d)	1/3	1/3	1/3	1/3	1/3	5/3
(e)	1/2	1/2	1	0	0	2
(f)	d/(1+d)	d/(1+d)	1	0	0	(1+3d)/(1+d)
(g)	d/2	1/2	1	0	0	(3+d)/2
(h)	(1-d)/(3-d)	1/(3-d)	1/(3-d)	1/(3-d)	0	(4-d)/(3-d)

Note: C1~C4 are representing C1a, C1b, C2a, C2b for Figure 10.1 (h)

The total normalized capacitor voltage stresses of all topologies are sketched in Figure 10.13, with variation of duty cycle. Compared with other listed topologies, the proposed second-order HBC has lowest total normalized capacitor voltage stress in a wide range of duty cycle. This result shows the superiority of proposed Basic HBC for high power density design.

In addition to the normalized capacitor voltage stress comparison, the normalized output ripple given in Table 10.2 is also compared as Figure 10.14. Among all the converters considered, the proposed Basic HBC structure (h) has the lowest ripple in the duty cycle range of [1/3, 2/3]. When duty cycle ranges are higher than 2/3, only converter (e) and (f) shows smaller ripple theoretically. However, under this condition, converter (e) and (f) exhibits much larger total normalized capacitor voltage stress and weaker gain boosting capability, as shown in Figure 10.13 and Figure 10.12 .

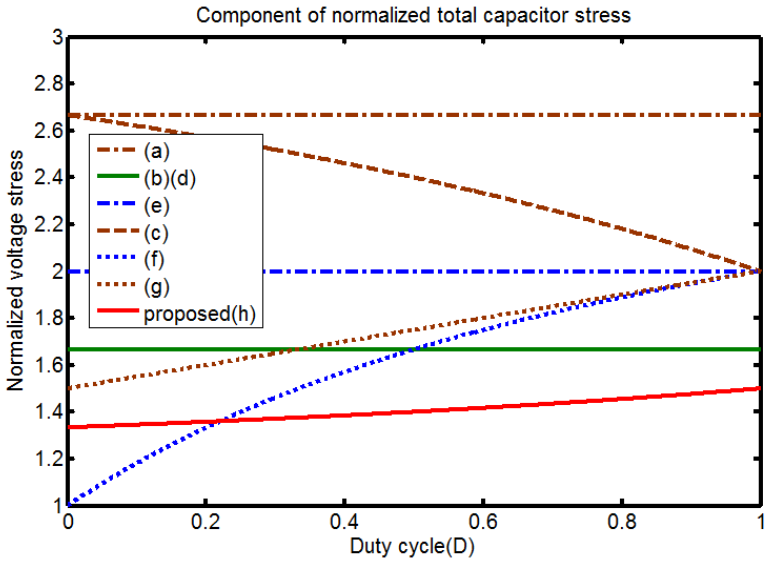


Figure 10.13 Comparison of total normalized capacitor voltage stress

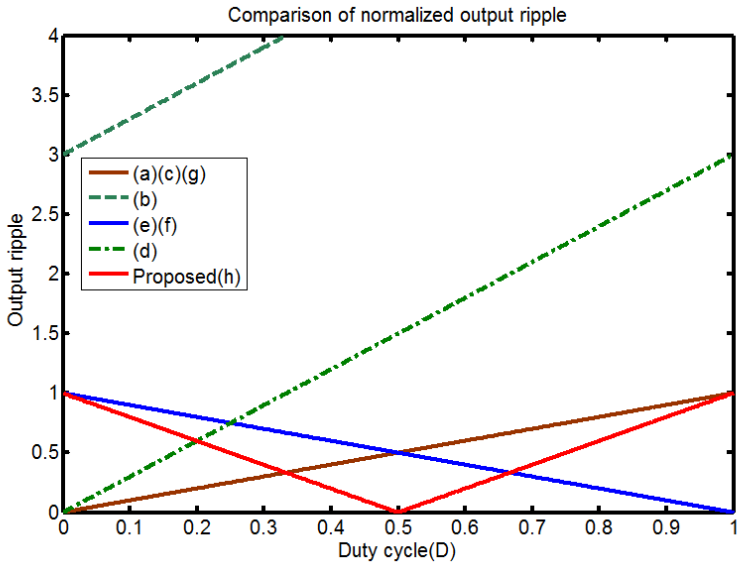


Figure 10.14 Comparison of normalized output ripple

It should be pointed out that although the proposed Basic HBC has the advantages in high power density and low cost design, it also has the intrinsic issue of uncommon ground between source and load, which may limit its applications in areas where common ground are required. Besides, due to direct connection between the input and output, the audio susceptibility may be an issue, calling for an input filter and fast control loop.

10.4 Simulation and Experimental Verification

In order to verify the feasibility of proposed converter and it performance, simulation and experimental results of a second-order HBC converter in Figure 10.1(h) are provided in this section.

A prototype of 200W 35V to 380V second-order HBC was built. The specifications of the prototype are listed in Table 10.4.

Table 10.4 Parameter Selected for prototype design

Name	Denomination	Value
MOSEFT	S	250V/40A,29 $m\Omega$ (IRFP4330)
Inductor	L	500 μH
Diode	D_{1a} D_{2a} D_{1b} D_{2b}	200V/20A,VF=0.78V(STH2002C)
Capacitor	C_{1a} C_{2a} C_{1b} C_{2b}	250V/100uF, electrolytic capacitor
Switching Frequency	fs	40kHZ
Load	R_L	722 Ω

A concern of the proposed converter is its input current spike due to the embedded switched-capacitor stage. However, a proper choice of switching frequency can mitigate this problem. The simulation results in Figure 10.15 shows this spike can be suppressed by increasing the frequency due to the reduced voltage difference between flying capacitors or capacitor and source. When the effect of some stray inductance is taken into consideration, the spike of input current will be further suppressed in the real application.

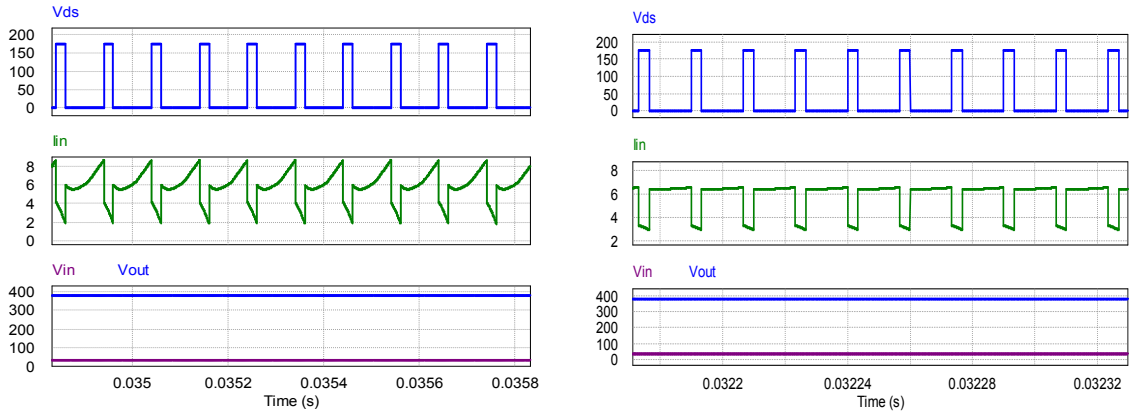
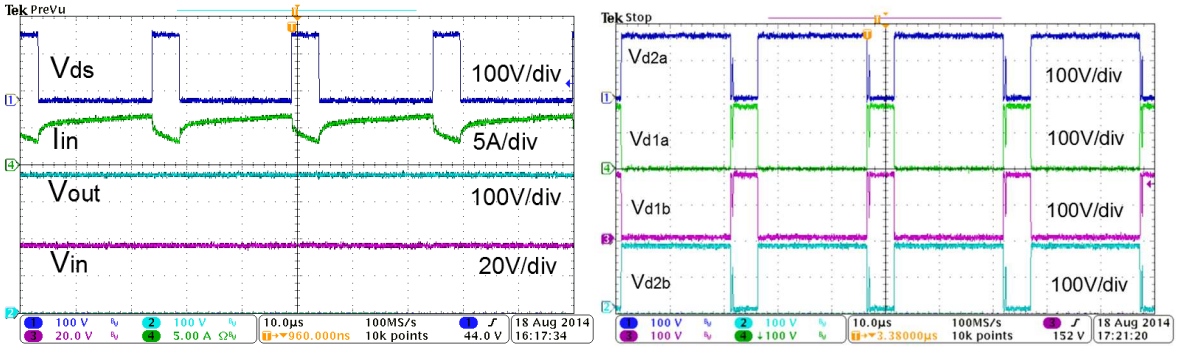


Figure 10.15 Simulation waveforms of V_{ds} , I_{in} , V_{out} , V_{in}

(a)10kHz (b)60kHz

The experimental waveforms of drain-source voltage input current, input voltage and output voltage are given in Figure 10.16(a). It can be seen only small overshoot at voltage V_{ds} because of the buffering function of capacitors C_{1a} and C_{1b} . The input current is pulsating without reaching zero and no rush current is observed due to the operation frequency is chosen properly. The output voltage is boosted to 380V and kept stable without high voltage rating filter capacitor. In Figure 10.16(b), the voltage waveforms of four diodes are presented, which is relatively low compared with output voltage.



(a) (b)

Figure 10.16 Experimental waveforms

(a)V_{ds} , I_{in} , V_{out} , V_{in} (b)Diodes voltage: V_{d2a} , V_{d1a} , V_{d1b} , V_{d2b}

In Figure 10.17, the output voltage ripple is compared with the voltage ripple of flying capacitors C_{2a} and C_{2b} under different duty cycle conditions, while the output voltage manually maintained at 200V to guarantee constant load current. According to the discussion in section 10.3.2, full ripple cancellation can be achieved under d=0.5 condition. It is observed in Figure 10.17(a) that the output ripple is almost zero when duty cycle is 0.5. When duty cycle is above 0.5, increasing duty cycle leads to increased output ripple,

as indicated in Figure (b), (c), (d). The interleaved voltage ripple of C_{2a} and C_{2b} shows the benefit of potential small output ripple design for proposed basic HBC topology.

Under the light load condition, the HBC may enter DCM operational mode easily. The experimental result of BRM and DCM conditions are given as Figure 10.18. Waveforms of V_{out}, V_{in}, I_L and V_{ds} are presented.

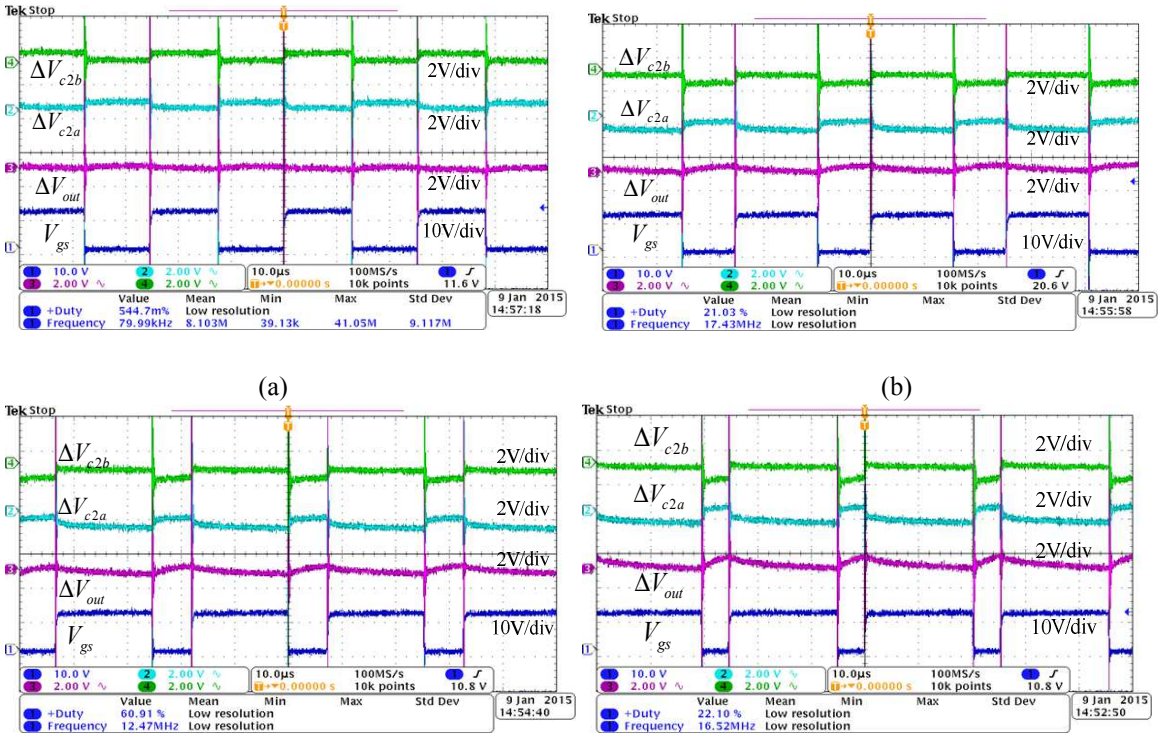
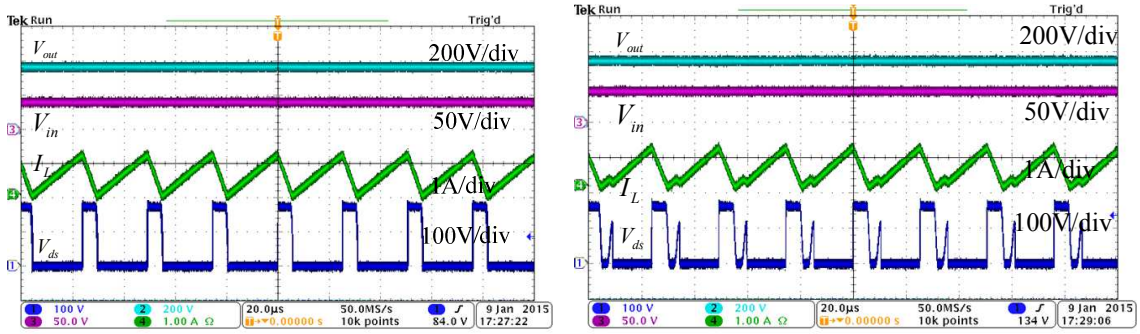


Figure 10.17 Experimental waveforms of voltage ripples: V_{c2a}, V_{c2b} ,V_{out} , V_{gs}

(a) D=0.5 (b)D=0.6 (c) D=0.7 (d)D=0.8



(a) (b)

Figure 10.18 Experimental waveforms of V_{out}, V_{in}, I_L and V_{ds}

(a) BRM condition (b) DCM condition

The efficiency curve of the prototype is tested and shown in Figure 10.19, with the load variating from 40W to 250W. A peak efficiency of 95.44% is achieved.

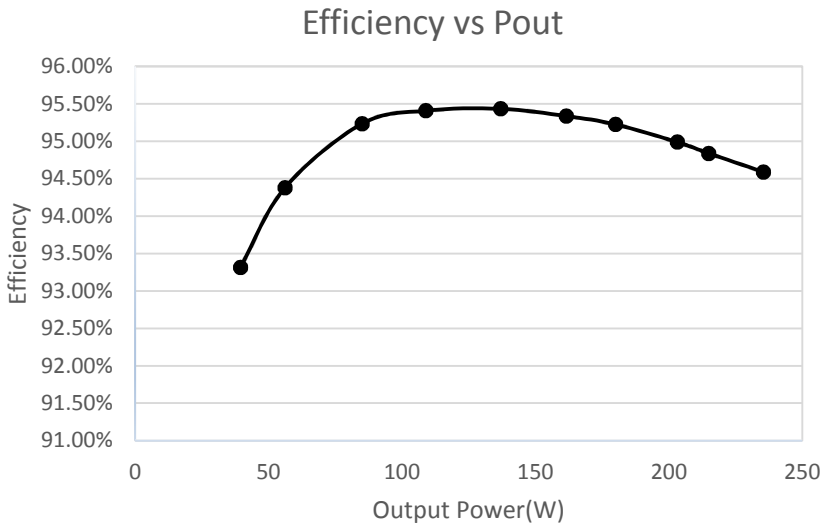


Figure 10.19 Efficiency curve with load variation (Vin=35V,Vout=380V)

10.5 Summary

The general Basic HBC composed of LS inductive switching core and Bipolar Voltage Multiplier was fully investigated in this Chapter. It acquires a collective advantages of the gain boosting capability from voltage multiplier and voltage regulation capability from boost converter, featuring in nature interleaved operation, wide regulation range, low component stresses, small output ripple, flexible gain extension, and high efficiency. Compared with other high gain boosting technologies such as tapped inductor, multi-inductor/switch method or transformer based method, the Basic HBC has reduced the complexity which is suitable for mass production. Compared with other single switch and single inductor high gain DC-DC converters, it has a better component utilization rate, smaller output ripple and lower component stress. The simulation and experimental results have demonstrated the proposed theories. The Basic HBC is suitable for many high gain DC-DC required applications such as the front-end PV system, fuel cell powered system, etc.

Chapter 11 A new Design of lossless Snubber for high efficiency Isolated HBC

Galvanic Isolation is critical in some high gain DC-DC applications for safety purpose. Therefore, another HBC member, Isolated Hybrid Boosting Converter, featuring low component stress, simple control, high efficiency, high power density and flexible gain extension is fully investigated in this Chapter.

A brief review of topology category "Switch+Transformer+Diode-capacitor" defined in Chapter 1 is given in section 11.1. In section 11.2, the operational principle of Isolated HBC with lossless snubber is profoundly analyzed with mathematical calculations. The new design method of energy regenerative snubber which helps providing soft switching condition, suppressing voltage spike and recycling leakage energy is illustrated in section 11.3. The simulation and experimental verification are given in section 11.4.

11.1 A review of topology category of "Switch+Transformer+Didoe-capacitor"

Recently, a number of energy sources such as solar panel, fuel cell, exhibit low terminal voltage, which call for high-gain step-up converter to interface with inverter for grid connection[181]. In these cases, electrical isolation may be also required. Instead of using costly and bulky low frequency isolation transformer at grid side, researchers is making efforts to find high frequency isolation solutions at the step-up DC-DC stage to shrink

system volume, improve efficiency, and reduce cost[28], [31], [33], [61]–[63], [65]–[68], [88]–[90], [93]–[95], [182]–[187].

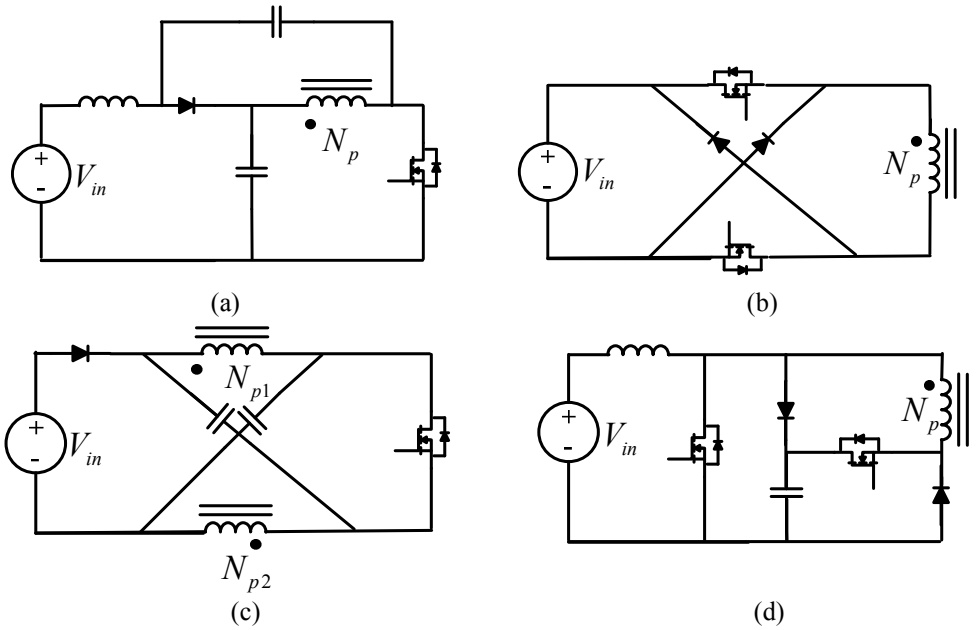


Figure 11.1 Primary side configurations for high-gain isolated DC-DC converters

(a)Z source based structure I [33] (b)Double switch with clamping diodes structure[63] (c)Z source based structure II [61] (d)Boost with lossless clamp structure[86]

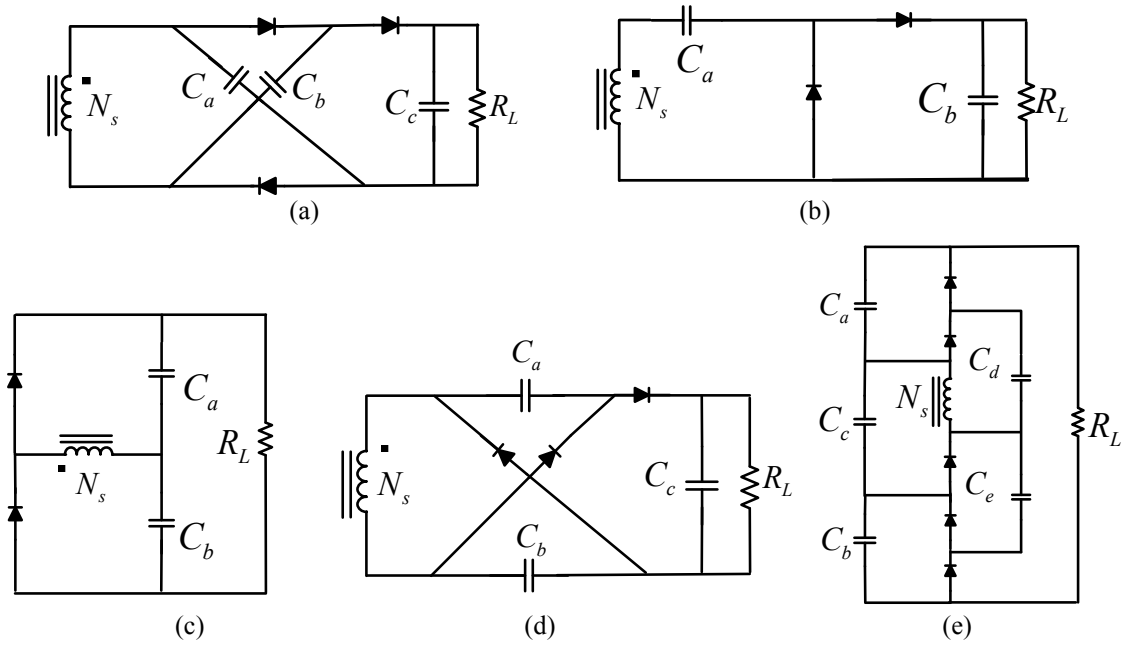


Figure 11.2 Secondary side configurations for high-gain isolated DC-DC converters

(a)Inverse voltage multiplier[63] (b)Voltage lift[31] (c)Voltage doubler[65]
(d) Voltage multiplier[62] (e)Bipolar Voltage Multiplier

Some typical isolated low power and high-gain oriented topologies for primary side and secondary side are summarized in Figure 11.1 and Figure 11.2 respectively. The topologies presented in Figure 11.2(a) and (d) are similar with the only difference of transformer polarity. But it can impact the conversion ratio formula. The combination of topologies in Figure 11.1 and Figure 11.2 may lead to new topologies. For instance, Figure 11.1 (a), (b), (c) were combined with Figure 11.2(d) and the formulated topologies were investigated in paper [33], [63] and [61], respectively. Combining the conventional fly-back structure at the primary side with topologies shown in Figure 11.2(b),(d),(c) at secondary side leads to different isolated high-gain DC-DC converters, which were reported in [31], [62], [65]. However, only comparing the voltage gain of those derived converters becomes unfair due to different conversion ratio is usually associated with the component number, stress, cost, and circuit efficiency. Therefore, the compassion based on total normalized capacitor voltage stress discussed in Chapter 9 is adopted in this Chapter.

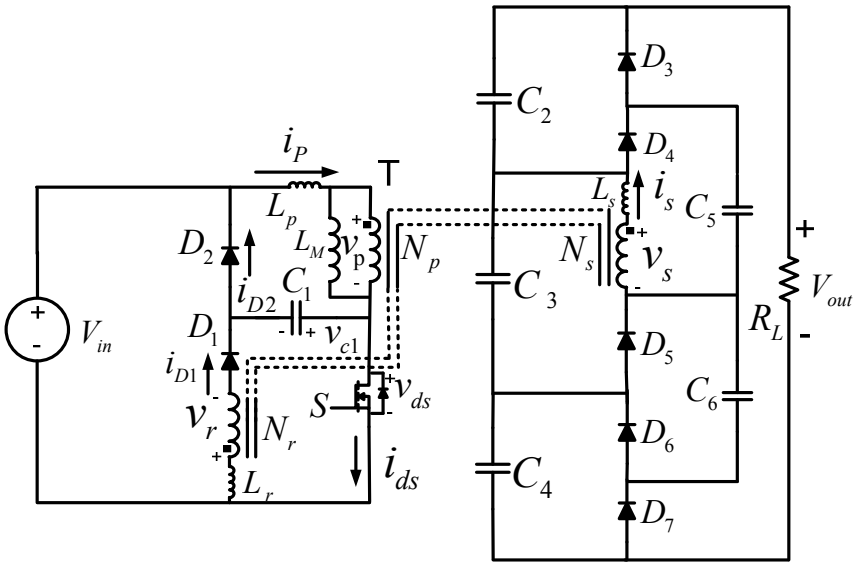


Figure 11.3 Isolated HBC with energy regenerative snubber

11.2 Operational Principal of Isolated HBC with Lossless Snubber

The proposed Isolated HBC with an energy regenerative snubber is shown as Figure 11.3. The original energy regenerative snubber using discrete inductor at primary side was first proposed in [188] and further studied in [62], [189]–[191], as shown in Figure 11.4(a). It provides zero voltage "turn-off" condition by a resonant tank composed of L and C_1. In order to save space and magnetic core of inductor, a configuration utilizing the tertiary winding of transformer to substitute discrete inductor was proposed in [192] show as Figure 11.4(b). This tertiary winding configuration is defined as "resistant" winding in this paper as it resists the voltage polarity change of capacitor C_1 at switch "turn-on" transient. It can recycle energy from capacitor C_1. According to papers[193]–[195], the reported efficiency is still low as capacitor C_1 does change its voltage polarity and zero voltage turn-off condition was not granted. In order to assist the voltage polarity change of C_1, the snubber with "assistant" tertiary winding configuration shown as Figure 11.4(c) was

proposed in [184] and the capacitor C_1 could successfully change voltage polarity until reaching negative input voltage, in which case the zero voltage "turn-off" condition can be created. The only problem with this configuration is the tertiary winding will release energy during "turn-on" transient, which may cause increased circulation energy. In this paper, the snubber with "resistant" tertiary winding in Figure 11.4(b) is adopted, with added zero voltage "turn-off" condition by proper design and utilization of resonant tank comprised of tertiary winding leakage inductance and capacitor C_1.

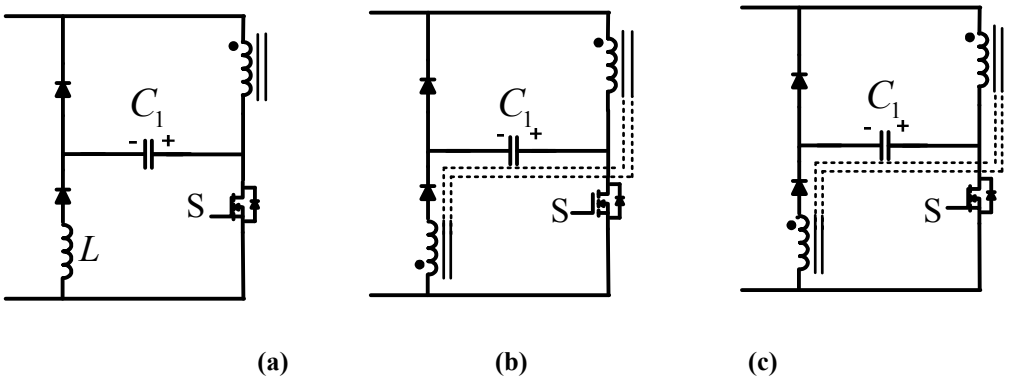


Figure 11.4 Energy regenerative snubber configurations

(a)Snubber with discrete inductor (b) Snubber with resistant tertiary winding

(c) Snubber with assistant tertiary winding

11.2.1 CCM operation of Isolated HBC

Under Current Conduction Mode (CCM) condition, the key waveforms of the circuit in Figure 11.3 are sketched in Figure 11.5. The circuit states under CCM condition are illustrated from Figure 11.6(a) to (h). They are analyzed as follows:

1) State 1[t0, t1]:

This state is corresponding to the circuit in Figure 11.6(a). At time t_0, the switch S is turned on. At this moment, a positive voltage v_s at dotted terminal of secondary winding is induced which tends to turn on D_4 and D_5. However, the secondary winding current hasn't dropped to zero in previous state due to leakage inductance in CCM condition. Thereby, the leakage of secondary winding will keep the diodes D_3 and D_6 conducted for a short period. This state ends when D_4, D_5 and D_7 turned on.

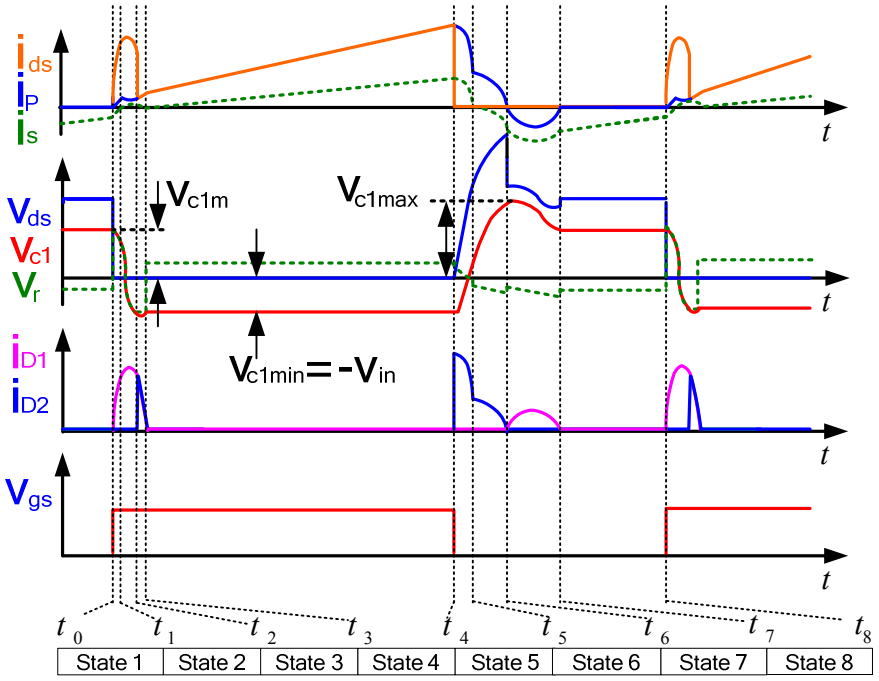


Figure 11.5 Key waveforms under CCM operation condition

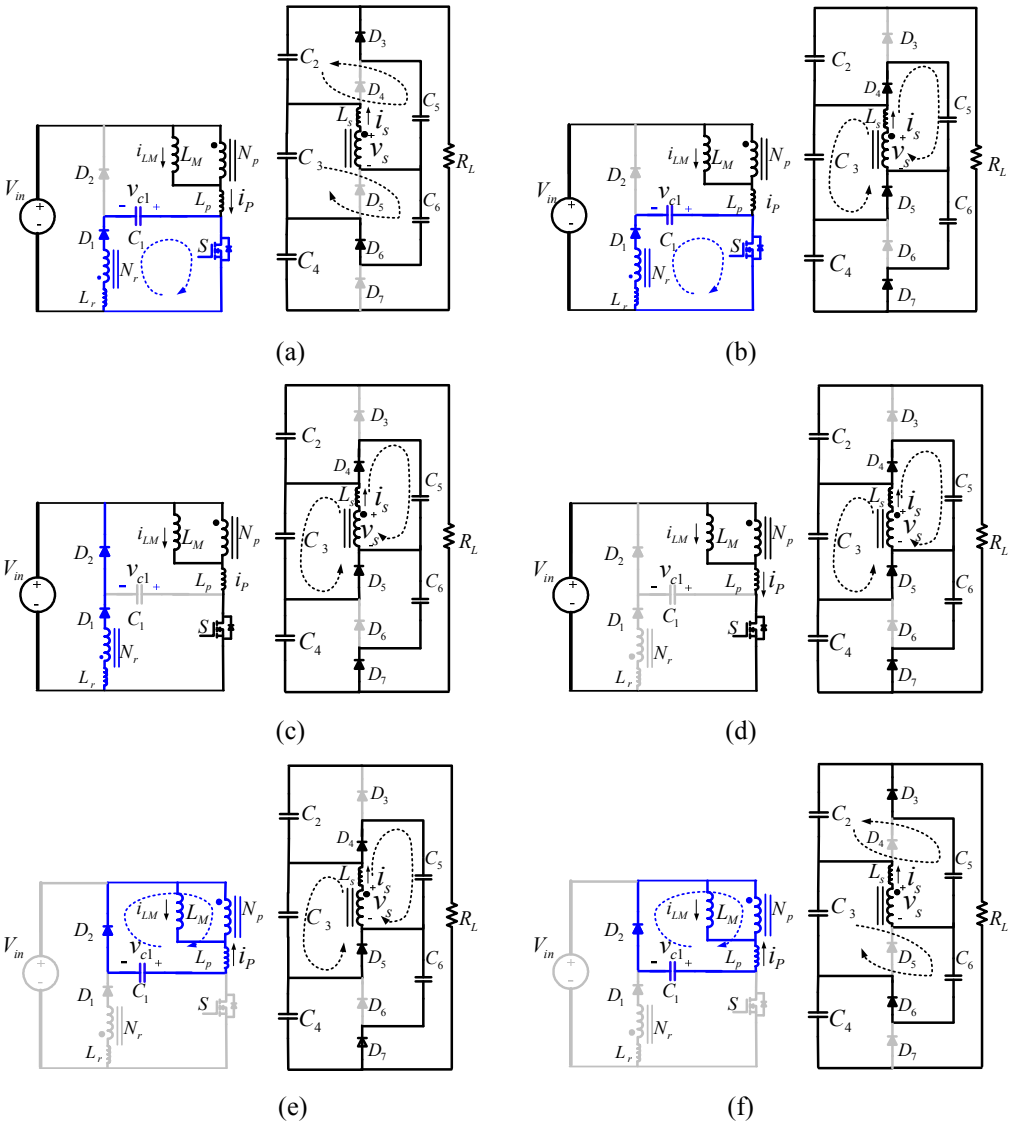
2) State 2[t1, t2]:

Since time t_1, the diodes D_4, D_5 and D_7 are turned on and the secondary winding of transformer starts to charge C_3 and C_5. The load is powered by the cascading structure of C_2, C_3 and C_4. At primary side, the equivalent circuit of resonant tank is shown as Figure

11.7. Since duration of state 1 is short, its resonance effect is neglected to simplify calculation. Therefore, based on initial condition: $V_{c1}(t_1)=V_{c1m}$, $i_{c1}(t_1)=0$, the voltage of capacitor C_1 can be expressed as:

$$V_{c1}(t)=\frac{N_r}{N_p}V_{in}+(V_{c1m}-\frac{N_r}{N_p}V_{in})\cos(w_2(t-t_1)) \tag{11.1}$$

Where $t\in[t_1,t_2]$, $w_2=1/\sqrt{L_{r\_eq}C_1}$, V_{c1m} is capacitor voltage at switch turn-on moment, described in Figure 11.5.



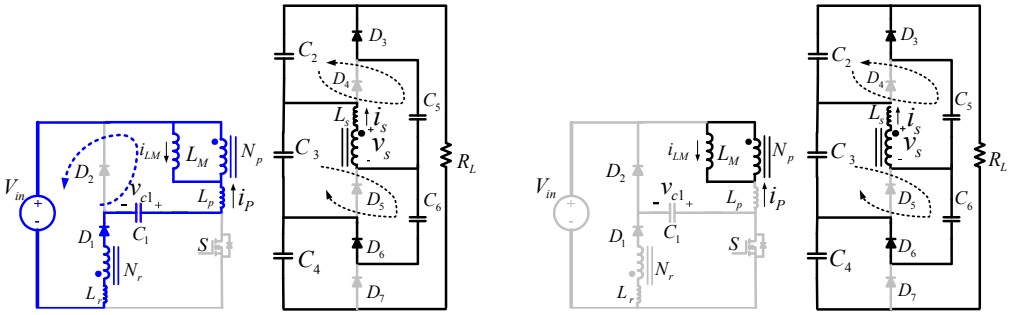


Figure 11.6 Operational states under CCM condition (a) State 1~ (h) State 8

According to equivalent circuit within dashed line of Figure 11.7, the equivalent resonant inductor L_{r_eq} can be expressed as:

$$L_{r\_eq} = L_r + (\frac{N_r}{N_s})^2 L_s \,//\, (\frac{N_r}{N_p})^2 L_p \tag{11.2}$$

where L_p, L_s and L_r are real leakage inductance of primary, secondary and tertiary winding of transformer individually.

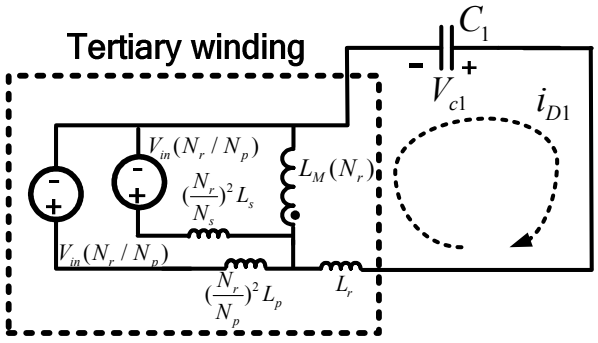


Figure 11.7 Equivalent circuit of resonant tank of State 2

3) State 3[t2, t3]:

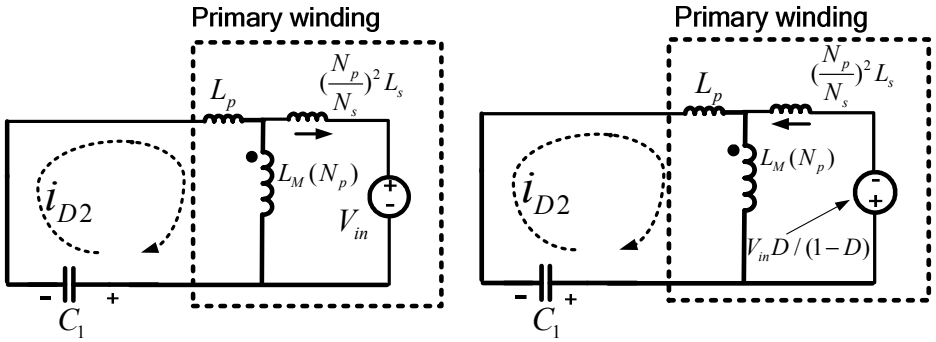
State 3 occurs when the capacitor C_1 reverses its voltage until less than $-V_{in}$ by resonance, as shown in Figure 11.6(c). The requirement is the minimum of (1) is smaller than $-V_{in}$, which can be described as:

$$(2\frac{N_r}{N_p}+1)V_{in} < V_{c1m} \tag{11.3}$$

However, when the voltage of C_1 reaches $-V_{in}$, it will be clamped to $-V_{in}$ due to conduction of D_2. Therefore, in this state, the energy stored in L_{r_eq} will be sent back to the input source and the output. The currents passing through D_1 and D_2 are the same and they decrease linearly. In the real case, a negative peak voltage, smaller than $-V_{IN}$, may appear on resonant capacitor C_1, which is due to the stray inductance along capacitor terminals and circuit path. This state ends when the current passing through D_1 and D_2 drops to zero.

4) State 4[t3, t4]:

At this state, D_1 and D_2 are both turned off. The voltage of C_1 is kept constant at $-V_{in}$. D_4, D_5 and D_7 are conducting and the input source partially sends energy to secondary side and partially magnetizes the transformer. In the real case, voltage of C_1 may show a small slope, which is because the voltage drop on $R_{ds(on)}$ of main switch increases when the magnetizing current increases.



(a) (b)

Figure 11.8 Equivalent circuit of resonant tank

(a) State 5 (b) State 6

5) State 5[t4, t5]:

As shown in Figure 11.6(e), this state starts when switch S is turned off. As the voltage of C_1 was kept close to $-V_{in}$ from the previous state, the switch voltage V_{ds} increases from zero gradually. The leakage energy at the primary side is recycled to capacitor C_1. At secondary side, the leakage current takes time to decrease to zero. Therefore, the diode D_4, D_5 and D_7 are still conducting during this state. The equivalent resonant tank at primary side is given as Figure 11.8(a). As the tertiary winding is an open circuit, its real leakage doesn't participate in resonance.

Based on $V_{c1}(t_4) = -V_{in}$, $i_{c1}(t_4) = i_{M\_peak} + i_{s\_\max} {}^{N_s}\!/_{N_p}$, the voltage of capacitor C_1 during this state can be expressed as:

$$V_{c1}(t) = -V_{in} + \sqrt{\frac{L_{p\_eq}}{C_1}}(i_{M\_peak} + \frac{N_s}{N_p} i_{s\_\max}) \sin(w_5(t - t_4)) \quad \textbf{(11.4)}$$

where $t \in [t_4, t_5]$, $w_5 = {}^{1}\!/_{\sqrt{L_{p\_eq} C_1}}$. i_{M_peak} is the peak magnetizing current which is assumed constant during resonance period and i_{s_max} is the maximum current of secondary winding. According to Figure 11.8(a), the equivalent resonant inductor L_{p_eq} can be expressed as:

$$L_{p\_eq} = L_p + (\frac{N_p}{N_s})^2 L_s \quad \textbf{(11.5)}$$

The voltage of C_1 at the end of this state can be calculated as (6):

$$V_{c1}(t_5) = -V_{in} + \sqrt{\frac{L_{p\_eq}}{C_1}} \sqrt{(\frac{N_s}{N_p} i_{s\_\max})^2 + 2\frac{N_s}{N_p} i_{s\_\max} i_{M\_peak}} \quad \textbf{(11.6)}$$

6) State 6[t5, t6]:

If $V_{c1}(t_5)>V_{in}D/(1-D)$, diodes D_3, D_6 conduct immediately after diodes D_4, D_5 and D_7 become blocked. The equivalent resonant tank circuit switches from Figure 11.8(a) to Figure 11.8(b). In this case, the initial conditions of resonance are derived based on(11.6) and $i_{c1}(t_5) = i_{M\_peak}$, the voltage of capacitor C_1 therefore can be derived as:

$$V_{c1}(t) = \frac{D}{D'} V_{in}(1-\cos(w_6(t-t_5))) + V_{c1}(t_5)\cos(w_6(t-t_5)) + i_{M\_peak}\sqrt{\frac{L_{p\_eq}}{C_1}}\sin(w_6(t-t_5)) \quad \textbf{(11.7)}$$

where $t \in [t_5, t_6]$, $w_6 = 1/\sqrt{L_{p\_eq}C_1}$, $D' = 1-D$. This state ends when the voltage of C_1 reaches to its maximum value V_{c1max}.

However, if $V_{c1}(t_5)<V_{in}D/(1-D)$, which means the voltage accumulated in capacitor C_1 in state 5 is not enough to turn the resonant tank from Figure 11.8(a) to Fig.8(b), another intermediate state shown as Figure 11.9 will appears between state 5 and 6. In this intermediate state, the magnetizing current only charges the capacitor C_1 until it reaches $V_{in}D/D'$. Then the diodes D_3, D_6 conducts and the equivalent resonant circuit turns to Figure 11.8(b). In this case, the $V_{c1}(t_5)$ in (11.7) should be replaced by a constant voltage $V_{in}\,D/D'$.

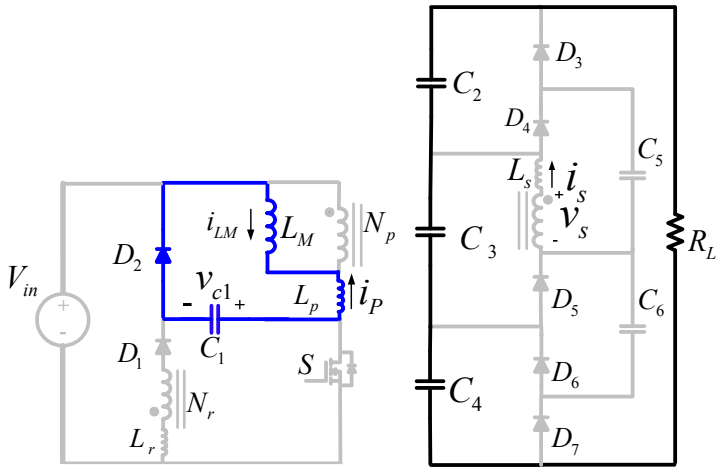


Figure 11.9 Intermediate state before state 6 under $V_{c1}(t_5)<V_{in}D/(1-D)$ condition.

7) State 7[t6, t7]:

According to (11.7), the peak value of V_{c1} is obtained as:

$$V_{c1\_\max} = \frac{D}{D'}V_{in} + \sqrt{(V_{c1}(t_5) - \frac{D}{D'}V_{in})^2 + (i_{M\_peak}\sqrt{\frac{L_{p\_eq}}{C_1}})^2} \tag{11.8}$$

This maximum voltage of C_1 should be high enough to make state 7 occur. By inspection of Figure 11.6(g), the requirement of V_{c1max} is obtained:

$$V_{c1\_\max} > V_{in} + V_{in}\frac{D}{D'}(1-\frac{N_r}{N_p}) = KV_{in} \tag{11.9}$$

where $K = (1+{}^{D}\!/_{D'}(1-{}^{N_r}\!/_{N_p}))$.The new resonant tank equivalent circuit is described in Figure 11.10. The voltage of capacitor C_1 starts to fall from its peak value at this state.

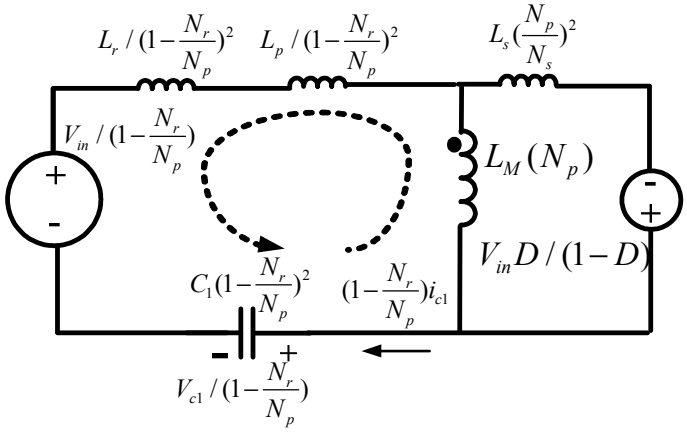


Figure 11.10 Equivalent circuit of resonant tank at state 7

Based on the initial condition $V_{c1}(t_6) = V_{c1\max}$, $i_{c1}(t_6) = 0$, the voltage V_{c1} can be expressed as:

$$V_{c1}(t) = KV_{in} + (V_{c1\max} - KV_{in})\cos w_7(t - t_6) \quad \textbf{(11.10)}$$

where $t \in [t_6, t_7]$. According to Figure 11.10, the resonant angular frequency can be expressed as:

$$w_7 = \frac{1}{\sqrt{(\frac{N_p}{N_s}(1-\frac{N_r}{N_p})^2 L_s + L_p + L_r)C_1}} \quad \textbf{(11.11)}$$

This state can advance to state 8 if minimum voltage of (11.10) is kept higher than $V_{in}D/D'$ to block D_2, which is desirable to avoid over oscillation. Therefore, the following equation should be satisfied:

$$2V_{in} + \frac{D}{D'}(1-\frac{2N_r}{N_p})V_{in} > V_{1\max} \quad \textbf{(11.12)}$$

Note that the voltage V_{c1m} employed in state 1 equals to the voltage at the end of this state. Therefore, it can be expressed as minimum of (11.10):

$$V_{c1m} = 2(1+\frac{D}{D'}(1-\frac{N_r}{N_p}))V_{in} - V_{c1\max} \quad \textbf{(11.13)}$$

8) State 8[t7, t8]:

This state starts with both diodes D_1 and D_2 blocked. The stored energy in magnetizing inductance is released to the secondary side. The capacitors C_3, C_5, C_4 are discharged while C_2 and C_6 are getting charged. The magnetizing current drops to its initial value at t_0 by the end of this state.

11.2.2 DCM operation of Isolated HBC

If the magnetizing current drops to zero at state 8, the converter will experience DCM operation condition. A new state described as Figure 11.11 will appear with all diodes turned off. At this state, the magnetizing current is maintained at zero and capacitor C_2, C_3 and C_4 are all discharged in cascade to power the load.

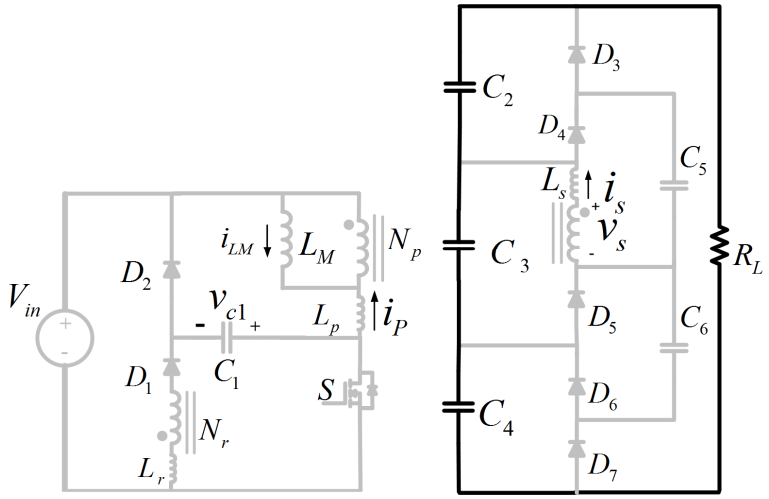


Figure 11.11 Final state under DCM condition

At the meantime, the state in Figure 11.6(a) disappears due to no secondary winding current exist at "turn on" transient. The operation states under DCM can be described from Figure 11.6(b) to Figure 11.6(h) and a final state in Figure 11.11 .

11.3 Circuit Design Analysis

Based on the steady state analysis of CCM, the duty cycle D and turn ratio between secondary winding and primary winding can be determined. In this section, magnetizing inductance, the tertiary winding of transformer and resonant components design will be investigated and the circuit performance will be analyzed under CCM condition.

1) Fly-back-Forward Transformer Design Consideration

In the proposed topology, the transformer operates in "fly-back-forward" mode. At the switch "on" period, the input source partially stores energy in magnetizing inductor and partially sends energy directly to output, which is "forward" mode. While during the switch "off" period, the stored energy at magnetizing inductance will be released to the output, with magnetic resetting automatically achieved, which is called "fly-back" mode.

The ideal waveforms of magnetizing current and secondary winding current are shown as Figure 11.12. By inspecting current flow of secondary winding in Figure 11.6, it can be found the current flow out of dotted terminal comprises the current passing through diode D_4 and the current going toward the common point of C_3 and C_5, while the current going into doted terminal only comes from the common point of C_3 and C_5. As the average current of D_4 equals to output current, it can be derived that:

$$D\overline{I_{s(on)}} + D'\overline{I_{s(off)}} = I_{out} \tag{11.14}$$

Due to transformer turn ratio, it can be obtained that:

$$\overline{I_{s(off)}} = -{I_M N_p}/{N_s} \tag{11.15}$$

In addition, the energy conversation between input and output results in:

$$V_{in}(I_M + \frac{N_s}{N_p}\overline{I_{s(on)}})D = V_{out}I_{out} \tag{11.16}$$

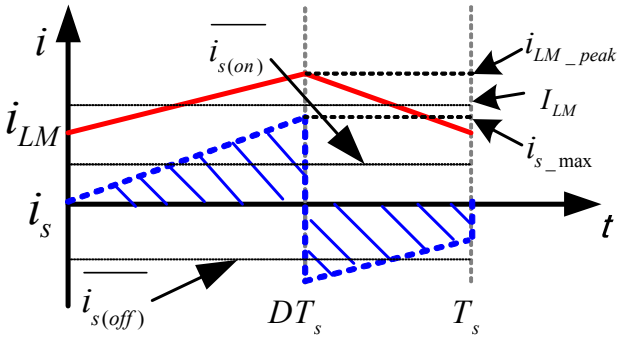


Figure 11.12 Ideal waveforms of magnetizing current and secondary winding current

To increase calculation accuracy, the leakage voltage drop is taken into account here. The converter voltage gain under CCM condition can be modified as:

$$V_{out} = \frac{N_s}{N_p}\frac{3-D}{1-D}V_{in}k \tag{11.17}$$

where $k = {}^{L_{p\_eq}}\!/_{(L_{p\_eq}+L_M)}$.

Furthermore, according to Figure 11.12, the peak current of secondary side can be written as:

$$i_{s\_max} = 2\overline{I_{s(on)}} \tag{11.18}$$

Based on (11.14)~(11.18), the following results are obtained, which are useful for snubber circuit design:

$$I_M = \frac{N_s}{N_p}(\frac{3-D}{1-D}k-1)\frac{V_{out}}{R_L} \tag{11.19}$$

$$i_{M\_peak} = \frac{N_s}{N_p}(\frac{3-D}{1-D}k-1)\frac{V_{out}}{R_L} + \frac{V_{in}}{2L_M}DT_s \tag{11.20}$$

$$i_{s\_\max} = 2I_{s(on)} = 2(1+\frac{3-D}{D}k)\frac{V_{out}}{R_L} \tag{11.21}$$

In addition, the magnetizing inductance guarantee CCM condition can be presented as follows:

$$L_M > \frac{D(1-D)^2}{4(3-D)}(\frac{N_p}{N_s})^2 T_s R_L \tag{11.22}$$

Therefore, the turns of primary winding N_p can be determined. Since the transformer needs to store energy, some air gap should be added.

2) Regenerative Snubber Design Consideration

According to the voltage analytical equations derived in section 11.2.1, the desirable waveform of capacitor C_1 can be described in Figure 11.13 as black solid line. The peak voltage of capacitor C_1 should satisfy the following requirements based on (11.9) and (11.12) to restrict the resonation between t_6 and t_7 to avoid over oscillation indicated as red dashed line in Figure 11.13:

$$(\frac{1}{D'} - \frac{D}{D'}\frac{N_r}{N_p})V_{in} < V_{1\max} < (\frac{1+D'}{D'} - \frac{2}{D'}\frac{DN_r}{N_p})V_{in} \tag{11.23}$$

On the other hand, in order to guarantee $V_{c1\min}$ to reach $-V_{in}$, the following requirement should be satisfied based on (11.3) and (11.13):

$$V_{1\max} < (\frac{1+D}{D'} - \frac{2}{D'}\frac{N_r}{N_p})V_{in} \tag{11.24}$$

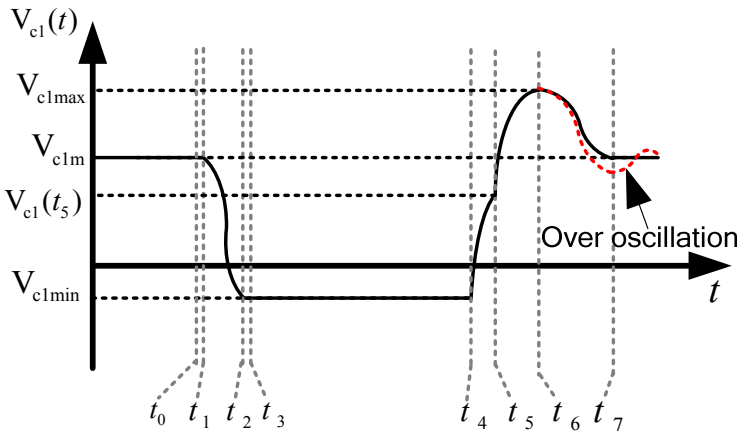


Figure 11.13 Desirable waveform of resonant capacitor C_1.

Apparently, there are two upper boundaries and one lower boundary for V_{1max} to achieve desirable voltage waveform. Thus, the choice of tertiary winding turn number can be derived to ensure the region between boundaries:

$$N_r < \min\{\frac{D'}{D}N_p, \frac{D}{2-D}N_p\} \tag{11.25}$$

According to analysis in section 11.2.1 state 6, the maximum voltage of C_1 can be expressed as:

$$V_{c1\max} = \begin{cases} \frac{D}{D'}V_{in} + \sqrt{(\sqrt{\frac{L_{p\_eq}}{C_1}}\sqrt{(\frac{N_s}{N_p}i_{s\_\max})^2 + 2\frac{N_s}{N_p}i_{s\_\max}i_{M\_peak}} - \frac{1}{D'}V_{in})^2 + (i_{M\_peak}\sqrt{\frac{L_{p\_eq}}{C_1}})^2} & C_1 < C_{1m} \\ \frac{D}{D'}V_{in} + i_{M\_peak}\sqrt{\frac{L_{p\_eq}}{C_1}} & C_1 > C_{1m} \end{cases} \tag{11.26}$$

where:

$$C_{1m} = \frac{L_{p\_eq} D'^2}{V_{in}^2} [(\frac{N_s}{N_p} i_{s\_max})^2 + 2\frac{N_s}{N_p} i_{s\_max} i_{M\_peak}] \quad \textbf{(11.27)}$$

Therefore, V_{c1max} is dependent on the C_1 and L_{p_eq} when other steady state circuit parameters are determined. Based on the above analysis, the snubber circuit design process can be concluded as following steps:

(1) Choose a proper tertiary winding turns of N_r by (11.25).

(2) Make a transformer according to L_M, N_p, N_r and N_s based on simplified steady state analysis. Create intentional leakage at tertiary winding. Test the leakage L_{p_eq} and calculate other steady state parameters D, i_{s_max}, i_{M_peak} based on equations obtained.

(3) Plot the piecewise function (11.26) as function of C_1 and all boundaries of V_{c1max}.

(4) Select a C_1 within boundaries, thus desirable voltage waveform of C_1 will be achieved.

The major advantage of this design method is it's not necessary to quantitatively control the leakage inductance at primary side, which is difficult in practice. For some leakage of tertiary winding wanted, it can be intentionally obtained by choosing special bobbin structure or adding air core inductor.

A design example is shown in Figure 11.14. The adopted parameters are listed in Table 11.1. As shown in Figure 11.14, the black line represents the top equation of (11.26) while the red line presents the bottom equation of (11.26). There is an intersection between two lines where the capacitance of C_1 is chosen as C_{1m}. Finally, formula (11.26) is determined as solid line in Figure 11.14.

To verify the formula (11.26) simulation points are provided as small circles and good agreement is found between model prediction and simulation results.

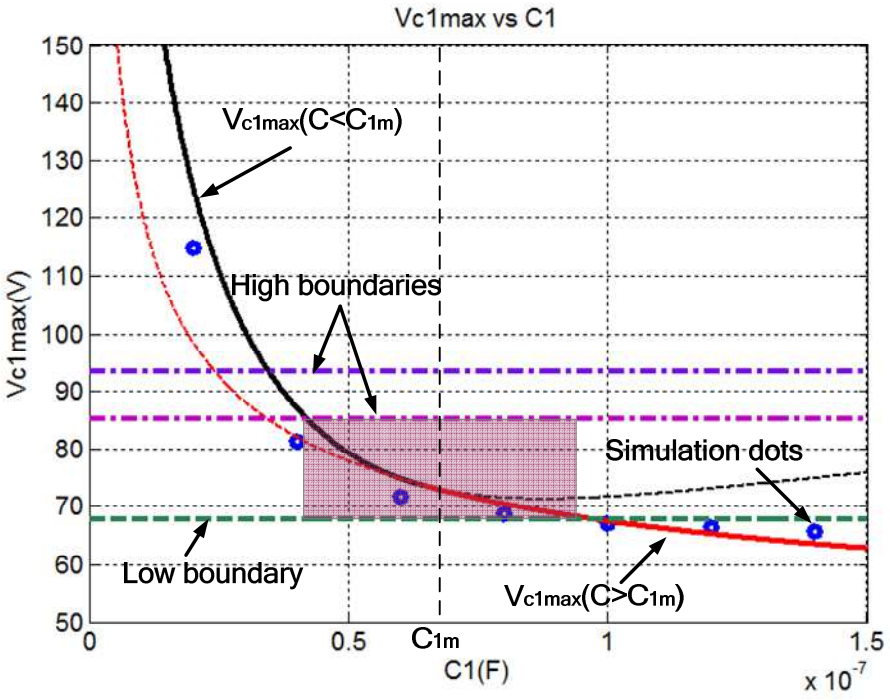


Figure 11.14 Design of resonant capacitor C_1

Table 11.1 Parameters of example Design

Parameters	Value	Parameters	Value
V_{in}	35V	R_L	800ohm
V_{out}	400V	Turns of Transformer	Np=9,Ns=19,Nr=2
fs	50kHz	Lp_eq	1.692uH
D	0.547	L_M	200uH

Obviously, there is a region for selection of C_1 to achieve ZVS and suppress voltage oscillation when magnetizing inductance L_M and tertiary wind turn N_r are determined, shown as shaded area in Figure 11.14. At the meantime, the input voltage takes effect on the curve of (38) and the boundaries. In order to maintain soft switching and desirable

resonant behavior in a range of input voltage, the design procedure should be implemented with up limit and lower limit of input voltage respectively. The derived overlap region of C_1 can be used to determine the value of C_1.

The shaded area shows the desirable area for choosing resonant capacitor C_1. The typical choice of C_1 can be slightly smaller than C_{1m}. After C_1 is determined, the equivalent leakage inductance of tertiary winding determined in formula (11.2) has to meet following criteria:

$$\pi\sqrt{L_{r\_eq}C_1} < DT_s \tag{11.28}$$

Components stress analysis for the snubber circuit design guideline is summarized in Table 11.2

Table 11.2 Component Design of Snubber Circuit

Components	Voltage Stress	Peak Current
D_1	$V_{in} + V_{in}\frac{N_r}{N_p}$	$\sqrt{\frac{C_1}{L_{r\_eq}}}(V_{c1m} - \frac{N_r}{N_p}V_{in})$
D_2	$V_{in} + V_{c1\max}$	$i_{M\_peak} + \frac{N_s}{N_p}i_{s\_\max}$
C_1	$V_{c1\max}$	/

11.4 Experimental Verification

In order to verify the proposed topology, a 200W prototype which boosts voltage from 35V to 400V is built with switching frequency of 50 kHz. The adopted circuit components are summarized in Table 11.3. Measurement setup is show in Figure 11.15.

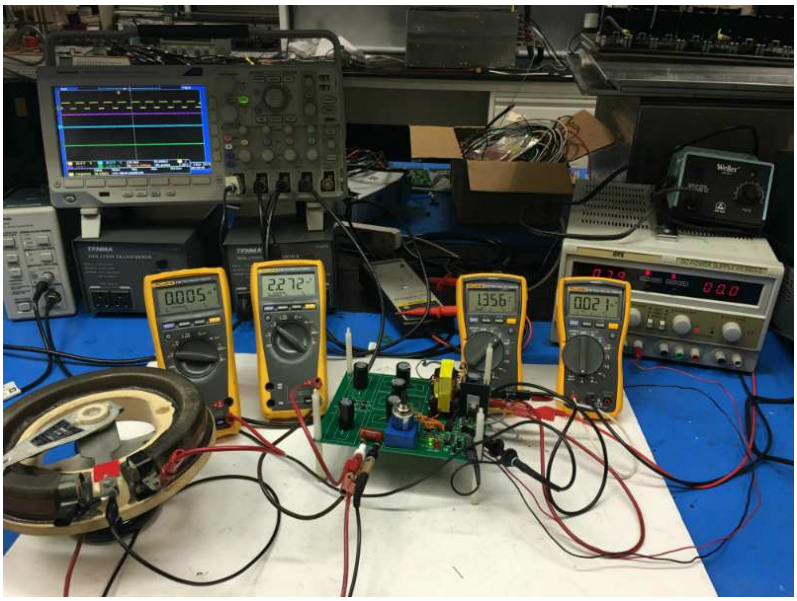


Figure 11.15 Prototype with measurement set-up

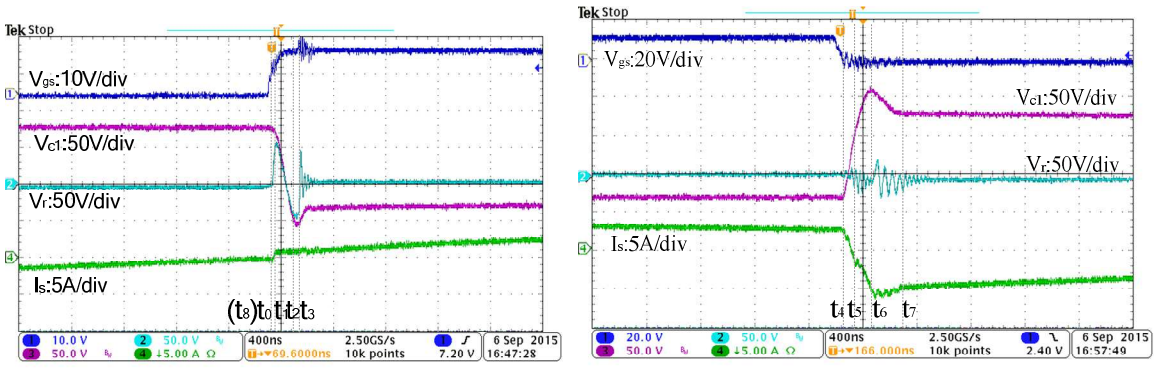
Table 11.3 Circuit Components list

Device	Model	Value
Switch	IRFP4332PbF	250V/120A, R(on)=29mohm
D1~ D2	VSB3200	200V/3A
D3-D7	SJPX-H3	300V/2A
C1	Film Capacitor	20nF/400V
C2-C6	Electrolytic capacitor	100uF/250V
Transformer	EER 35L (Magnetics)	Np: Ns: Nr=15:30:2 LM=55uH,Lp_eq=0.921uH

The experimental results are given from Figure 11.16 to Figure 11.19:

Figure 11.16 shows the waveforms of the driving signal, voltage of resonant capacitor, voltage of transformer tertiary winding and current of transformer secondary winding. The "turn-on" and "turn-off" transients are displayed in subfigures (a) and (b) respectively. The timing of different resonant states from t0-t8 is identified which validates the principle analysis.

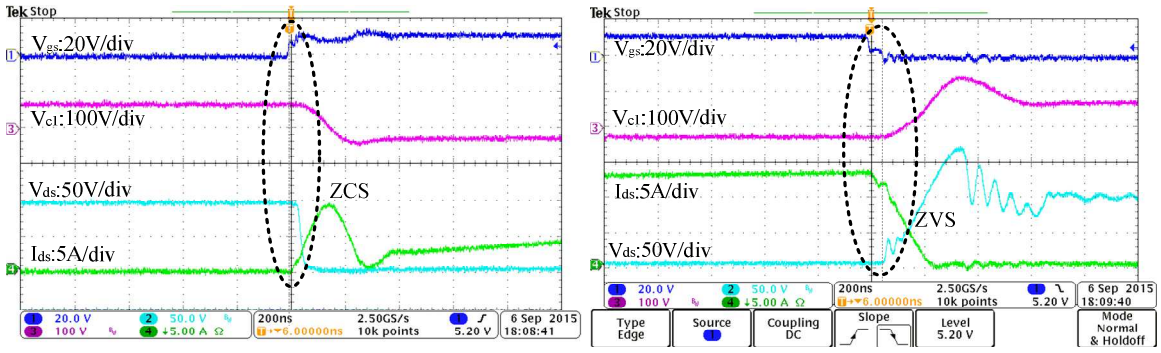
Figure 11.17 shows the soft switching condition created. Figure 11.17(a) shows zero current switching. When the switch is turned on, the switch current waveform comprises the resonance current from snubber circuit and the current from primary winding, both of which initiate from zero. In Figure 11.17(b), when the switch is turned off, the resonant capacitor voltage which was clamped at $-V_{in}$ creates the zero voltage "turn off" condition. By proper design, the snubber can also be used for higher power applications and realize soft switching with wide input voltage range.



(a) (b)

Figure 11.16 Circuit Resonation states validation waveforms: V_{gs}, V_{c1}, V_r, V_s

(a) Turn on transient (b) Turn off transient



(a) (b)

Figure 11.17 Soft Switching waveforms from top to bottom V_{gs}, V_{c1}, V_{ds}, I_{ds}

(a) Zero current "turn on" (b) Zero voltage "turn off"

Figure 11.18 shows the steady state waveforms of V_{c1}, I_{d1}, V_{out} and V_{in} with input voltage under 30V and 40V conditions. The desirable waveform of C_1 is achieved in both cases.

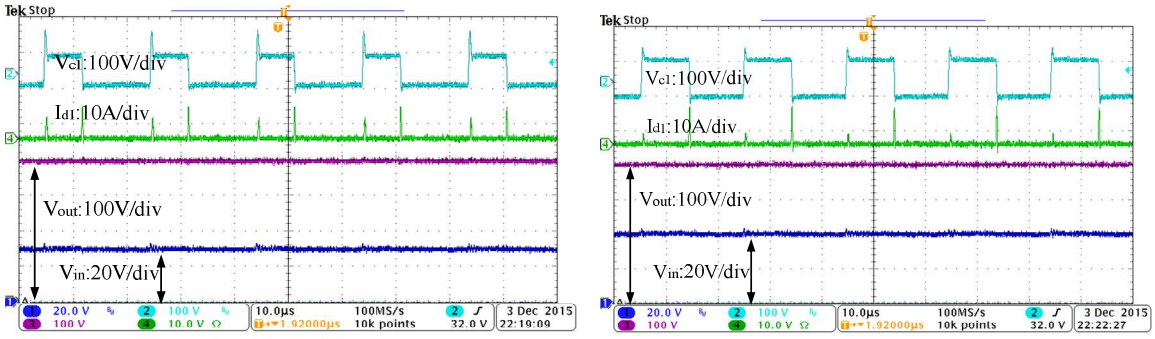


Figure 11.18 Steady state waveforms from top to bottom V_{c1}, I_{d1}, V_{out}, V_{in}

(a) V_{in}=30V, V_{out}=400V (b) V_{in}=40V,V_{out}=400V

The circuit efficiency curve with input voltage at 35V and output at 400V is tested under various load condition and sketched in Figure 11.19. At the rated power, efficiency

of 91.2% is achieved and over 90% efficiency is obtained for a wide power range. The peak efficiency can reach nearly 94%.

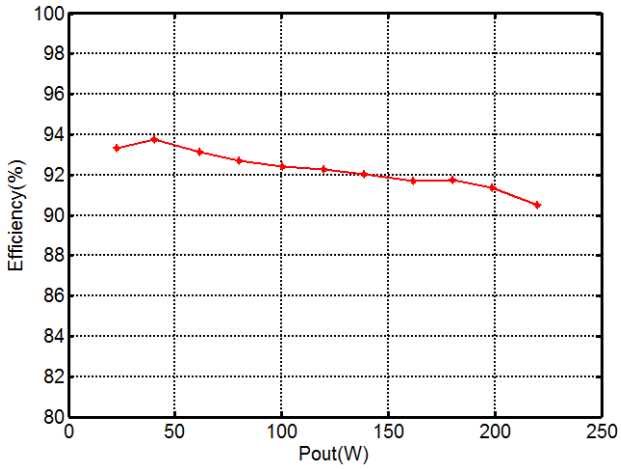


Figure 11.19 Efficiency curve under fixed gain Vin=35V, Vout=400V

11.5 Summary

This Chapter provides a comprehensive investigation of the Isolated HBC equipped with an energy generative snubber circuit. As a member of HBC family, it has the collective features of: (1) High-gain boosting capability (2) Low component stress (3) Low output ripple (4) No-magnetic resetting circuit (5) High power density (6) Flexible extension. At the primary side, the fly-back type topology is used to save components and an energy regenerative snubber that takes advantage of the tertiary winding leakage inductance is explored. The newly designed snubber circuit can realize soft-switching for main switch with a range of input voltage. At the meantime, only a few turns of tertiary winding is used. Good efficiency is obtained for the second-order isolated HBC.

Chapter 12 Extension Circuits based on HBC

In this chapter, a variety of circuit extensions based on the proposed HBC family are introduced and briefly analyzed. The circuit paralleling technology of HBC is introduced in section 0. The single-source paralleling configuration aiming at flexible power expansion and multi-source paralleling configuration for multi-source connection are both discussed. The inverter configurations based on HBC are investigated in section 12.2. The micro-inverter and multi-level converter hybridizing with HBC are introduced alone with benefits addressed. A system level application of HBC is proposed in section 12.3, where new multi-bus DC micro-grid system is created. A hybrid system with renewable energy, storage, AC and DC loads, and different DC buses is explored

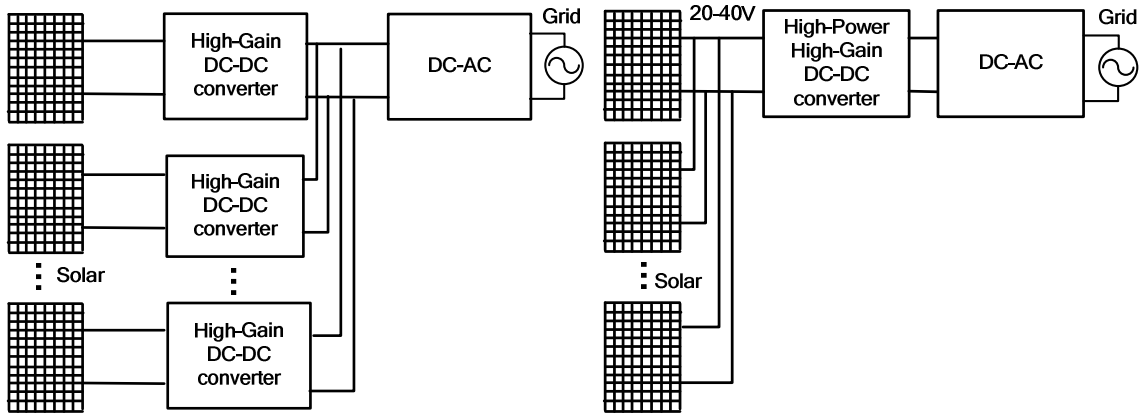
12.1 Paralleling technology of HBC

12.1.1 Single-source paralleling technology (3D DC-DC converter)

In order to overcome the partial shading issue in panel level, a dedicated DC-DC converter may be required to connect with each solar panel for MPPT racking. Two-stage solar conversion system is usually adopted as shown in Figure 12.1(a). However, the cost of such system is significant with increased number of power electronics devices.

In practice, the maximum power point voltage of solar panel is mostly dependent on temperature instead of solar illumination. Therefore, the partial shading of solar panel doesn't significantly change its maximum power point voltage even though solar power

fluctuates fiercely. To reduce the cost and volume, the system shown in Figure 12.1(2) can be adopted, in which case all solar panels are in parallel while one high power and high gain DC-DC converter is employed to track their common maximum power point. In this case, when some solar panels get shaded, their maximum power still can be adequately extracted.



(a) (b)

Figure 12.1 Two-stage solar system

(a) Low power high-gain DC-DC (b) High power high-gain DC-DC

In order to obtain the high power and high gain DC-DC converter, a 3D-DC converter concept is proposed for power expansion of proposed HBC in Chapter 9. To distinguish this concept with conventional circuit paralleling technology with multiple branches, the definition of 3D DC-DC converter includes the following meanings:

(1) The converter is composed of flexible "plug and play" paralleling branches of the same sub-circuits.

(2) All the branches share the input source and output filter capacitors

(3) The input source and obtained output voltage shares a common charge flow path as "z" axis while the paralleling branches are expanded in "x-y" dimension.

Based on this definition, some members of the HBC family can be extended to 3D DC-DC converters. The general circuit configuration is described as Figure 12.2.

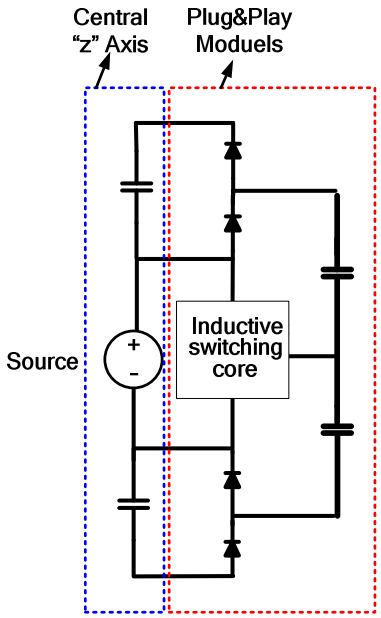


Figure 12.2 3D DC-DC extension of HBC

It can be seen that only the even-order BVM equipped with inductive switching cores can be extended to 3D DC-DC converter due to equipment of (3). Therefore, the Symmetrical HBC doesn't have 3D version since only odd-order BVM can be used. The Isolated HBC cannot realize a common charge path for input and output voltage in a common axis, thus it cannot be extended to 3D converter either. Consequently, only even-order Basic HBC and Tapped HBC has 3D version. A summarization table is given as Table 12.1.

Table 12.1 3D DC-DC converter extension options

Topology	3D extension	
	Even-order	Odd-order
Basic HBC	Yes	No
Symmetrical HBC	No	No
Isolated HBC	No	No
Tapped HBC	Yes	No

The proposed 3D HBC converters have the following advantages:

(1) All the "plug and play branches" the input and output filter, which is beneficial to improve power density.

(2) Input and output filter can be greatly reduced when more branches are added by interleaving control of "plug and play" branches.

(3) The common charge flow path for input and output creates the direct energy transferring path form input to output, enabling the more efficient energy conversion.

(4) The input voltage participates as part of output voltage, bringing the merit for gain enhancement.

The extended 3D $2n^{th}$-order Basic HBC and $2n^{th}$-order Tapped HBC are investigated as following:

1) 3D $2n^{th}$-order Basic HBC

As is shown in Figure 12.3, the 3D $2n^{th}$-order Basic HBC contains a common axis with power source in the center and N symmetrical branches. The voltage gain in CCM condition is given as follows:

$$\frac{V_{out}}{V_{in}} = \frac{1-D+2n}{1-D} \tag{12.1}$$

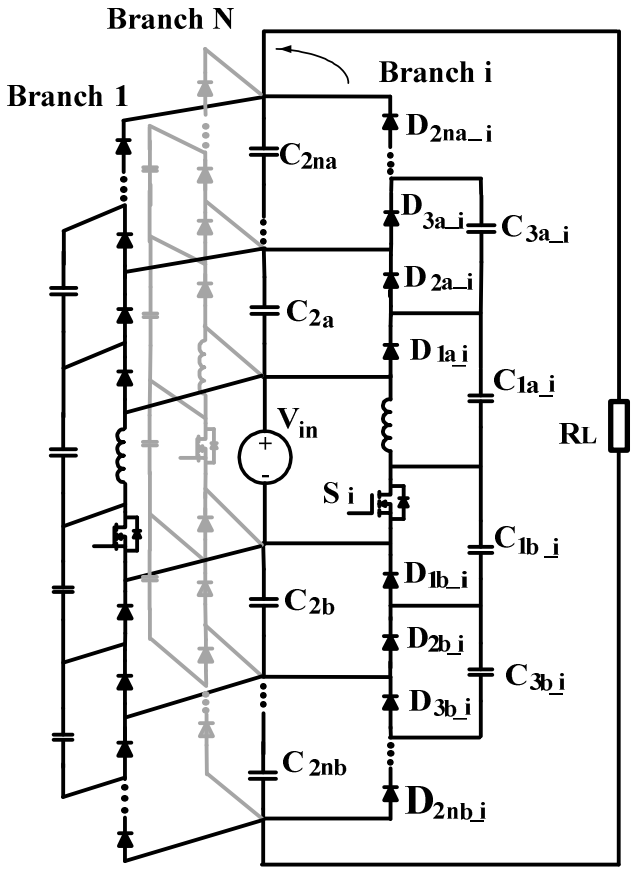


Figure 12.3 3D 2nth-order Basic HBC

The common axis and "plug and play" branches are shown as Figure 12.4(a) and (b). All the "Plug and Play" branches share the resources on common axis. Theoretically, unlimited number of "plug and play" branches can be added to common axis to achieve extremely high power application, which makes the proposed structure attractive for high power application.

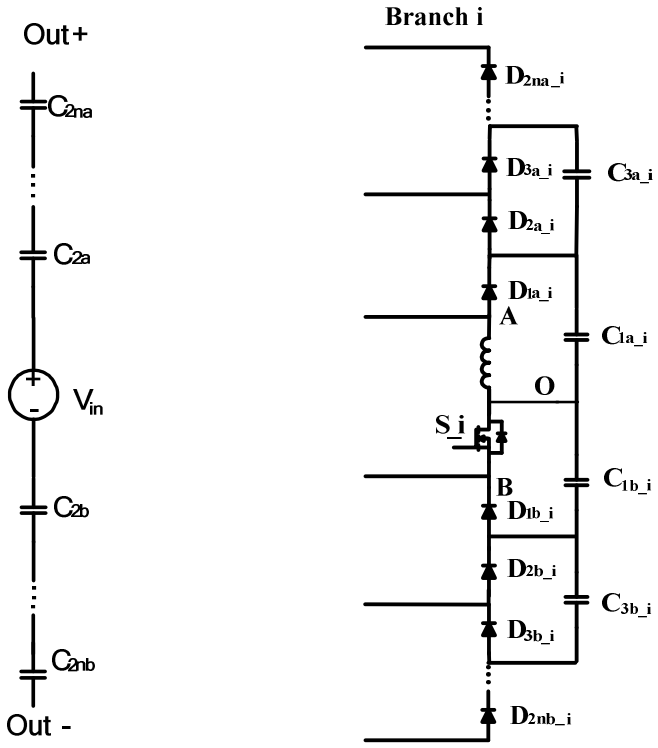


Figure 12.4 3D Basic HBC

(a)Common axis (b) "Plug and play" branch

As there are N "Plug and play" branches in parallel and operating at interleaved manner, the voltage ripples of capacitors on the common axis will be much smaller compared with the ripple of capacitors at "Plug and Play" branches. Thus the high voltage rating output capacitor is not necessary. With the increase of system power, more branches are "Plugged" to the common axis, leading to an even smaller output ripple. The control signal for switch S_i (i=1, 2, 3…N) is given as Figure 12.5. The phase shift of two consecutive driving signals should be $\frac{2p}{N}$.

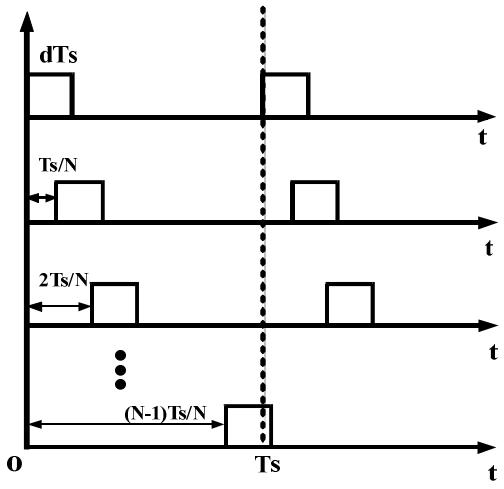


Figure 12.5 Control signal for the 3D Basic HBC

The components count of a $2n^{th}$-order N-branch 3D Basic HBC is given in Table 12.2.

Table 12.2 Component count of $2n^{th}$-order N-branch 3D Basic HBC

Component	Common Axis	Each Plug and Play branch	Total
Magnetic components	0	1	N
Capacitors	2n	2n	2n(N+1)
Switches	0	1	N
Diodes	0	4n	4nN

2) 3D $2n^{th}$-order Tapped HBC

If N branches of the $2n^{th}$-order Tapped HBC are connected in parallel and controlled by interleaved PWM control signals the same as Figure 12.5, a high power high gain 3D Tapped HBC is derived, as shown in Figure 12.6.

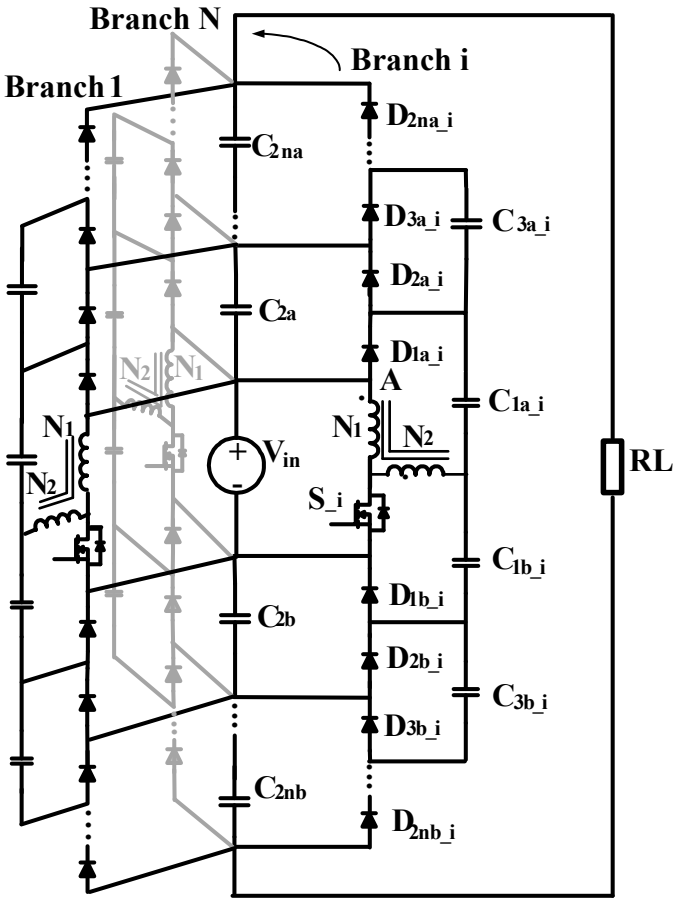


Figure 12.6 3D 2nth-order Tapped HBC

Similar to the 3D Basic HBC, the proposed topology is extremely flexible in expanding to different power levels by plugging in or deleting "Plug and Play" branches. The output voltage ripple is expected to be small due to interleaving operation.

The voltage gain of a 3D 2nth order Tapped-inductor HBC with a tapped inductor whose turn ratio is N_2/N_1 has following voltage conversion ratio:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{(1 + {N_2}/{N_1})2n}{1 - D} \tag{12.2}$$

According to the gain equation, there are three variables n, N_2/N_1 and D for circuit voltage gain control. However, higher order BVM requires larger number of components while larger turn ratio N_2/N_1 leads to higher leakage inductance. At the meantime, extreme duty cycle D may increase loss caused by diodes recovery. Therefore, a trade-off design is required in high gain DC-DC applications with appropriate selection of BVM order, turn-ratio of transformer and duty cycle at steady state. The relationship of voltage gain with n and N_2/N_1 is plotted in Figure 12.7, under three typical duty cycle conditions. Accord to the figure, the proposed 3D Taped HBC has promising potential to build high power and super high gain DC-DC converter.

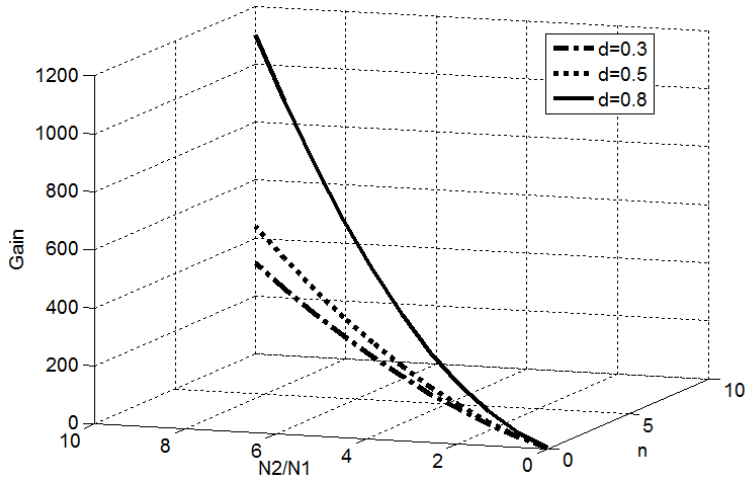


Figure 12.7 Voltage gain of 2nth-order Tapped-inductor HBC

12.1.2 Multi-source paralleling technology

If an odd-order BVM is chosen for HBC, the output paralleling brings the benefit of multi-source input, as shown in Figure 12.2. For each “Plug and Play” modules, an independent input source can be integrated, facilitating the power integration of sources with different voltage levels.

The flying capacitors on the “central axis” are shared by all “plug and play” branches. When one branch is supposed to plug into the central axis, the rest of the system will not be affected before the inductive switching core start working. The diodes of new HBC branch will prevent the power flow from central axis to the new branch. After it is plugged in, the inductive switching core can be activated, leading to energy injection from new source to the central axis capacitor for load consumption.

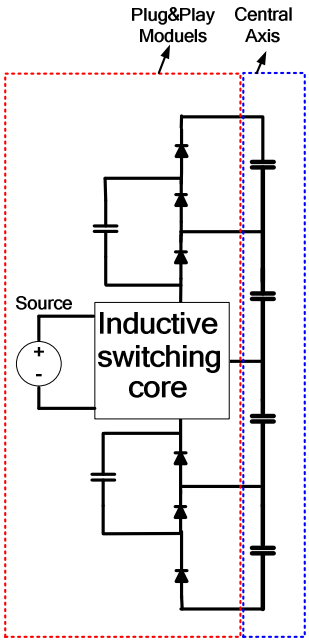


Figure 12.8 Multi-source paralleling of HBC

The Multi-source paralleling technology can be used in solar generation system as well, shown in Figure 12.9. The Symmetrical HBC is used as example for "plug and play" branch. In this configuration, each branch can implement the MPPT tracking independently.

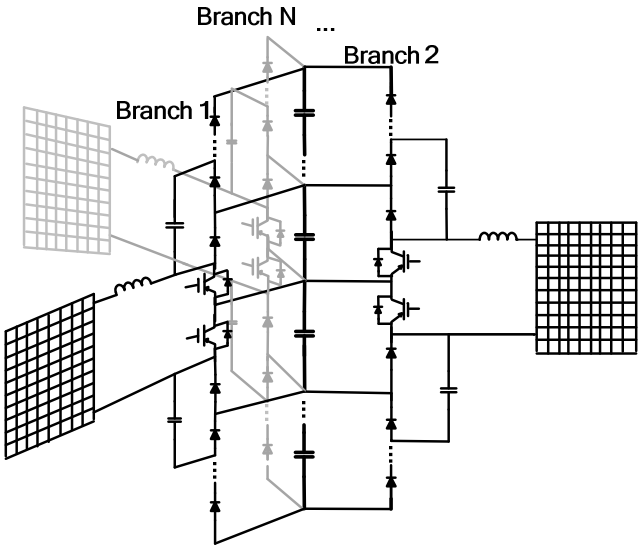


Figure 12.9 Multi-source paralleling solar system with Symmetrical HBC

Furthermore, the storage element can be integrated by small modifications of its corresponding HBC branch, to create hybrid energy generation and storage system, as shown in Figure 12.10(a) and (b). In Figure 12.10(a), the third-order Symmetrical HBC is used and full bidirectional modification is made in branch 2 by replacing all the diodes to switches. In this case, the fully power bidirectional function can be achieved from output DC bus to the battery at the cost of more switches. In Figure 12.10(b), only two diodes are replaced by switches in branch 2 to achieve partial power bidirectional of Symmetrical HBC branch. Under such condition, the battery still can be charged by solar panel through two central flying capacitors, which is a usual scenario that surplus solar energy is

generated and storage is required. When illumination intensity decreases, the battery can discharge through the modified Symmetrical HBC branch to support the high DC bus voltage.

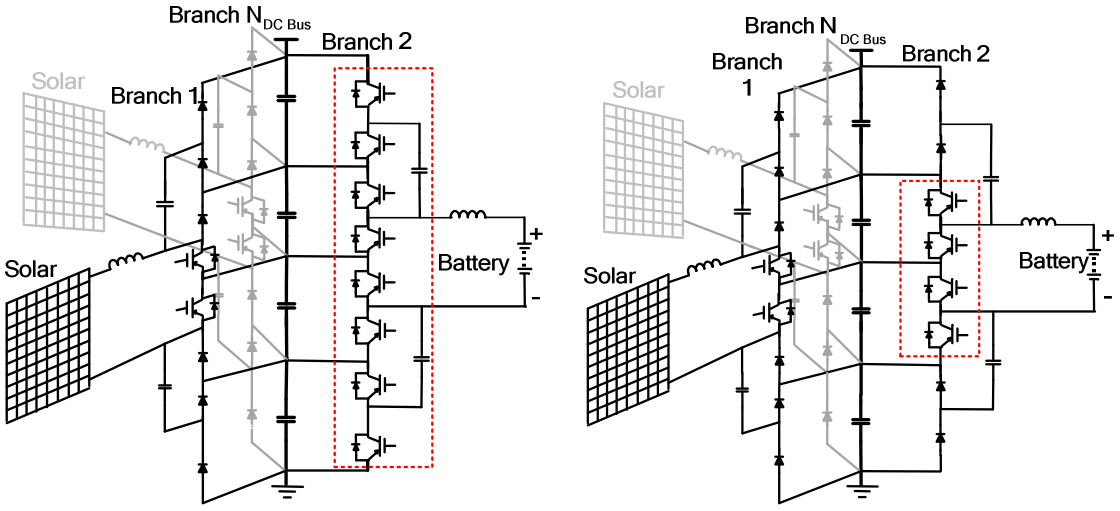


Figure 12.10 Multi-source paralleling system with storage

(a) Fully power bidirectional for battery (b) Partial power bidirectional for battery

12.2 Inverter based on HBC

The HBC family has unique circuit structure, which make it convenient to connect/hybrid with inverter stage, arising the potential of grid connection and motor drive applications.

12.2.1 Micro-inverter

Due to the bipolar configuration of HBC converters, a convenient extension to half-bridge micro-inverter by making use of gain boosting capability of HBC is given in Figure

12.11. The central source grounding configuration and central flying capacitor grounding configuration are shown as Figure 12.11(a) and (b). The central source grounding connection can be applied to entire HBC family, leading to different extended micro-inverters. The grounding point is intentionally created by connecting a pair of capacitors in cascade with the positive and negative terminals of energy source. The central flying capacitor grounding configuration can be only used in Symmetrical HBC due to complete balanced voltage of capacitor C_{ia} and C_{ib}(i=1,3,5…2n+1).

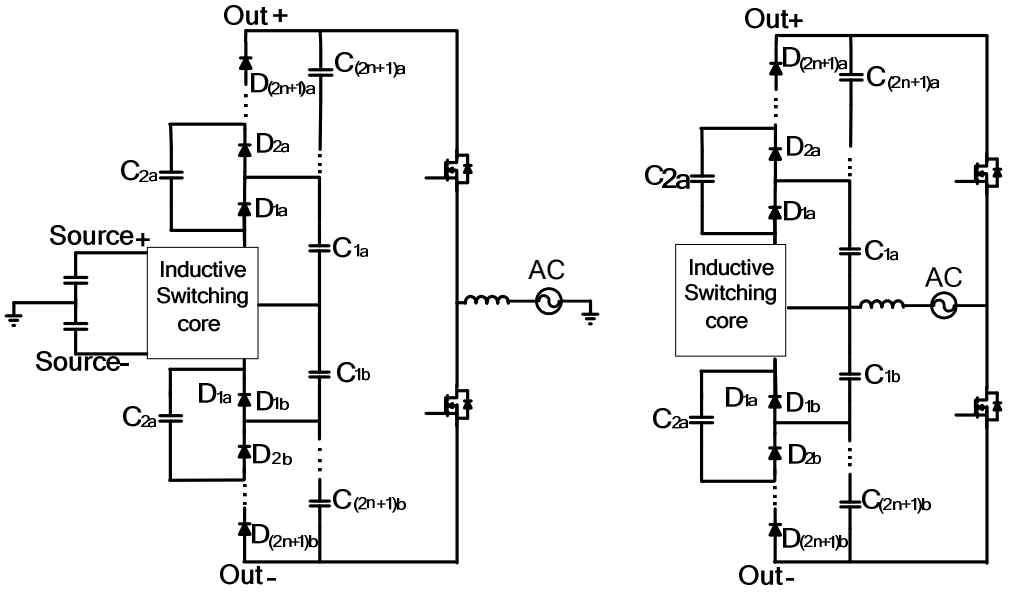


Figure 12.11 Half-bridge micro-inverter based on HBC

(a)Central source grounding (b) Central flying capacitor grounding

An example topology of Figure 12.11(a) is second-order Tapped HBC micro-inverter, given as Figure 12.12. The key waveforms are shown in Figure 12.13. Even though significant fluctuation of voltage of V_{c2a} and V_{c1a} occurs, the small ripple of DC bus voltage V_{dc} is obtained due to ripple cancelation.

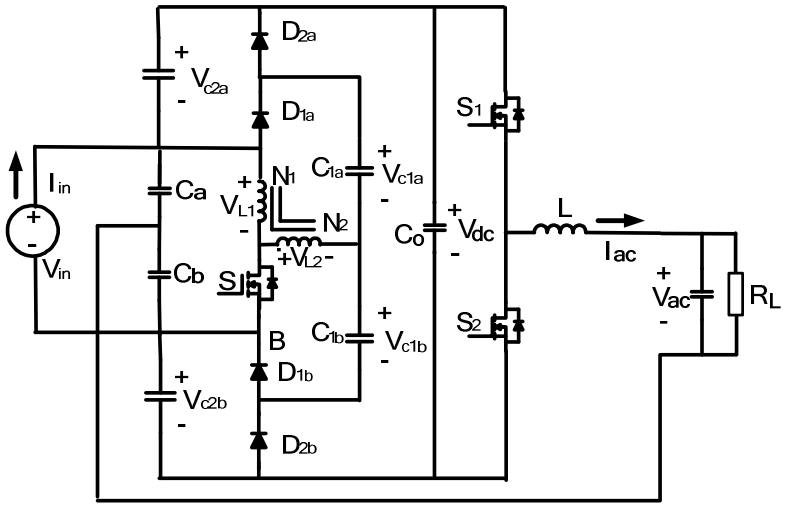


Figure 12.12 Second-order Tapped HBC micro-inverter

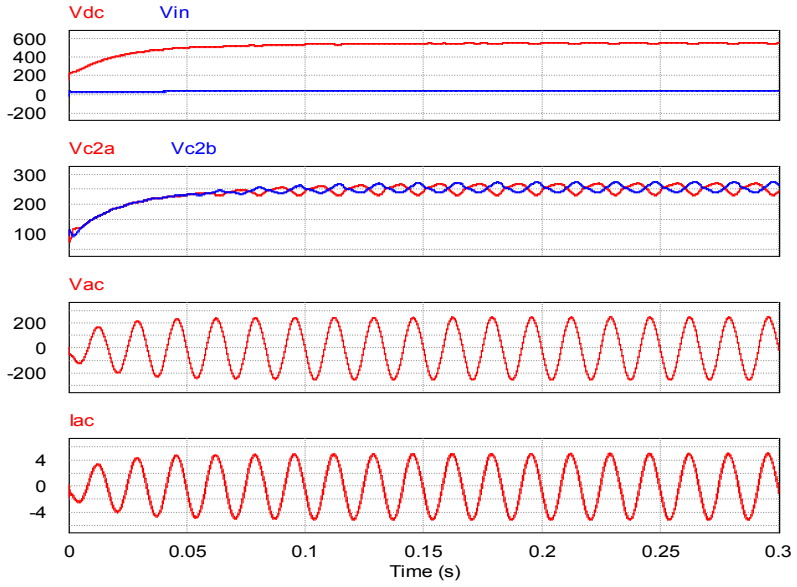


Figure 12.13 Simulation waveforms of Second-order Tapped HBC micro-inverter

For topology configuration of Figure 12.11(b), the representative topology third-order Symmetrical HBC micro-inverter is given as Figure 12.14. Simple Half-bridge is used while the middle point of flying capacitors is adopted as neutral point. The key simulation waveforms are shown in Figure 12.15.

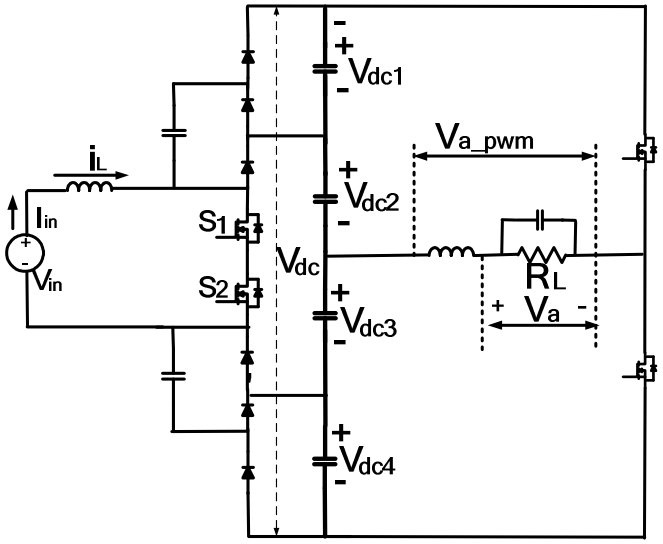


Figure 12.14 Second-order half-bridge symmetrical HBC micro-inverter

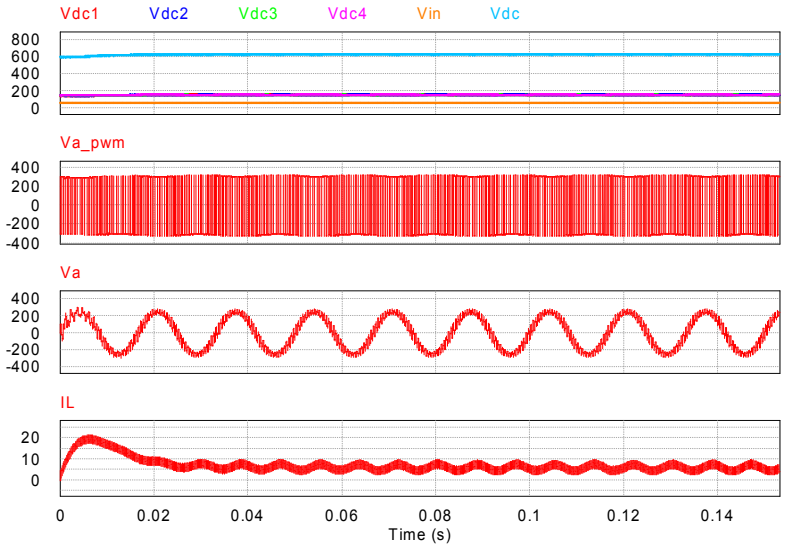


Figure 12.15 Simulation waveforms of third-order Symmetrical HBC micro-inverter

12.2.2 Multilevel Inverter

The HBC has potential to be hybrid with multilevel inverter for high voltage and high power application. For instance, one major drawback of traditional five-level diode clamp multi-level inverter is its balancing problem of four cascaded DC capacitors. However, buy making use the auto-balance flying capacitor (C_{1a}, C_{3a}, C_{1b}, C_{3b}) of third-order Symmetrical HBC, the voltage balancing issue can be solved automatically without using and voltage sensor or associated control circuit, as shown in Figure 12.16. Moreover, the low DC source input is allowed for high level AC voltage generation.

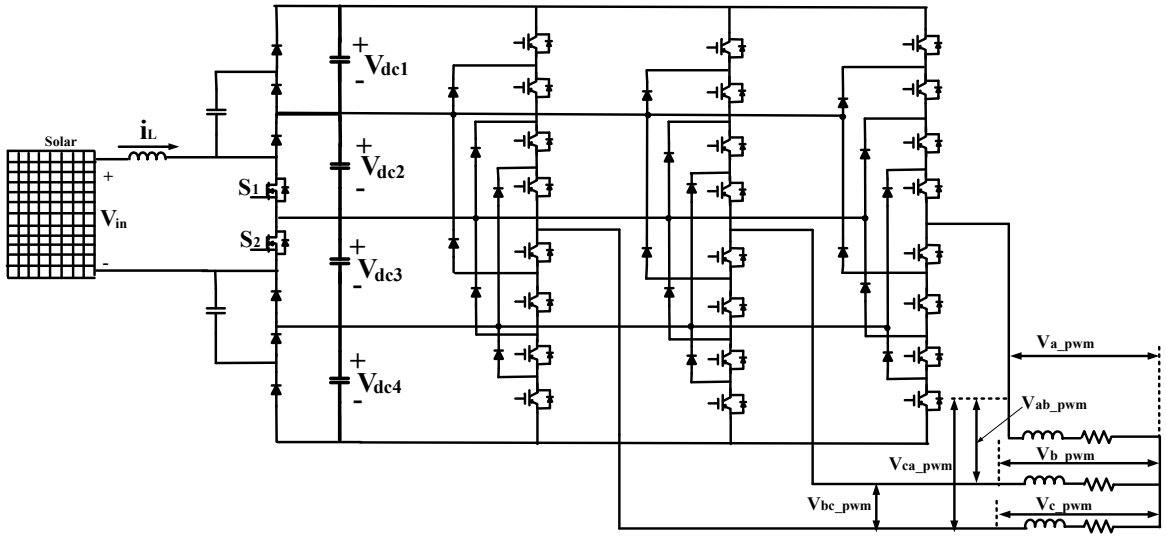


Figure 12.16 Third-order Symmetrical HBC Multilevel inverter

The feasibility demonstration simulation results in given in Figure 12.17, where circuit key waveforms are provide. In this simulation case, input voltage of 60V is used and 600V DC bus is generated for DC-AC conversion. Four cascaded flying capacitor voltages are balanced with approximately 150V for each.

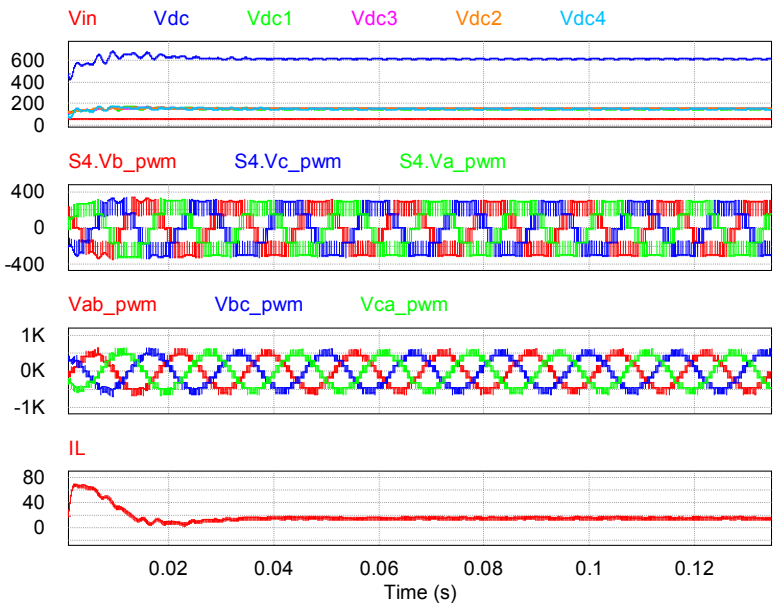


Figure 12.17 Simulation waveforms of third-order Symmetrical HBC Multilevel inverter

12.3 Multi-bus DC micro-grid based on HBC

The Symmetrical HBC(possible other HBCs) can be used to construct a DC micro-grid system by using Multi-source configuration, which is able to incorporate a variety of energy sources, storages and different load systems, shown as Figure 12.18. The "plug in" modules have several variations, such as step-up branch, bidirectional branch, partial bidirectional branch, DC-AC branch, etc., discussed in previous sections. For DC-AC branch, the traditional half bridge, diode clamped multilevel topology or three-phase inverter topology can consider as a plug-in modules to feed different AC load demands or for grid connecting purpose.

Another advantage of the configuration is it provides different DC voltage levels to meet different DC load requirements. Four levels of DC bus are available as shown in Figure 12.8. Each level of DC voltage is supposed to be able to supply power to DC loads.

At the meantime, the capacitors at the center axis can be replaced by battery modules when the DC bus voltage is allowed to fluctuate in an acceptable range, which can enhance the system energy storage capability, improve efficiency, and provide more reliable power to the AC or DC loads.

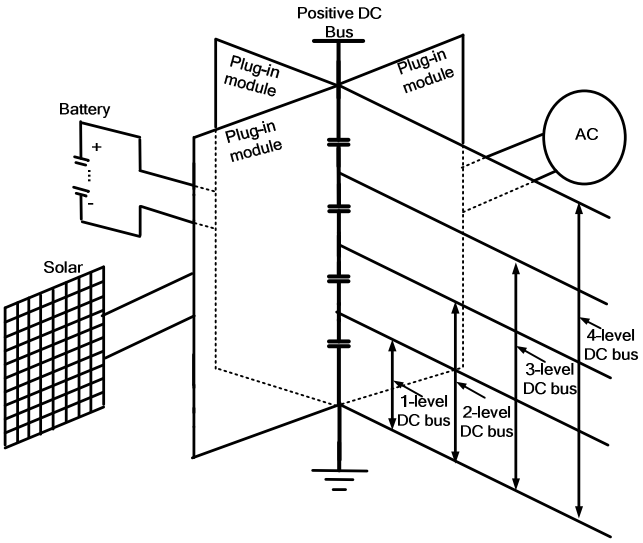
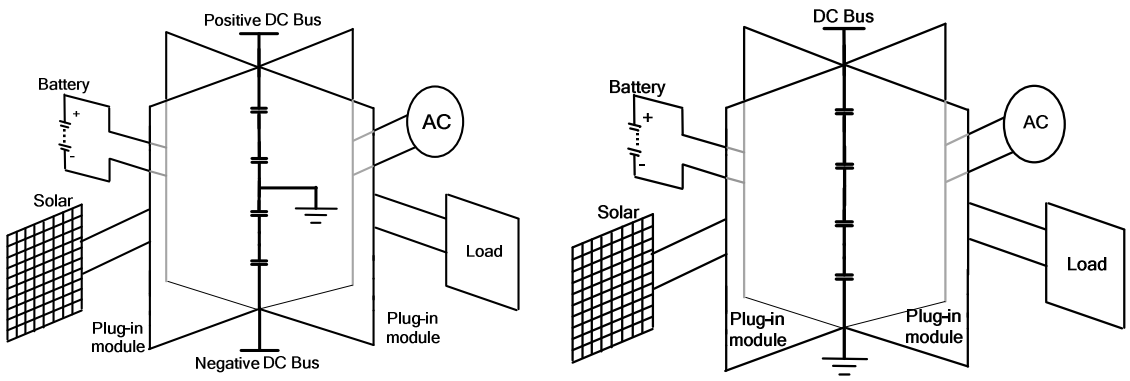


Figure 12.18 Multi-bus DC micro-grid system

Furthermore, the DC bus may be grounded from middle or the negative terminal, as shown in Figure 12.19. Different grounding strategies provide convenience to inverter design depending on practical requirements and safety concerns.



(a) (b)

Figure 12.19 Grounding solutions for Multi-bus DC micro-grid system

(a)Middle grounding (b) Negative terminal grounding

12.4 Summary

A few extensions circuit based on HBC and their applications are discussed yet not fully investigated in this chapter. It shows a promising future of applying the proposed HBC topologies to renewable energy application field.

The 3D DC-DC structure provided a high efficiency, flexible power expansion and low cost solution for high power high gain DC-DC application filed. The multi-source paralleling configuration of HBC facilitates the integration of independent energy sources and storage elements.

The inverter-based HBC configuration naturally hybridizes the HBC with some exited inverter topologies, which extends the HBC to be able to provide power to feed AC load or connect to grid.

Finally, the modular design of step-up, bidirectional, partial directional HBC branches and DC-AC branches creates a system level solution for renewable energy generation,

storage, and distribution system, named “multi-bus DC micro grid”. It is characterized by: (1) Modular branches for DC-DC and DC-AC integration (2) Variable DC-DC branches for energy resources or storage elements connection (3) Variable DC-AC branches for different AC loads and grid connection purpose. (4)Multi-level DC bus provided for different DC loads consumption.

Chapter 13 Conclusions and future work

With the advancement of industry, the applications of power electronics technology have experienced a swift growth in nearly every field associated with electrical power conversion. The innovations of power electronics are badly in need to satisfy the new demands and adapt to some extreme application situations.

In the future smart energy conversion systems, the voltage boosting technology will play critical rules. The requirement of voltage step up can range from chip level power management system to ultra-high power renewable energy conversion system. High gain and high efficiency step-up power converters with flexible power expansion, optional gain boosting capabilities, selectable isolation or power flow direction control will be pursuit constantly in academia and industry .

This dissertation comprehensively reviewed the voltage boosting technologies in the field of switched capacitor converter and inductor-based converters. Collective contributions are made in both areas.

Part I Boosting Switched Capacitor Converter

In switched capacitor converter field, a Two-switched Boosting Capacitor Converter family is synthesized with modeling technique developed. The following features of TBSC family are demonstrated:

(1)Symmetrical structure with automatic interleaving, leading to small output ripple

(2)Only two active switches, leading to simpler control and smaller converter size

(3)Feasible of pulse width modulation and frequency modulation for output voltage

(4) Low voltage stress of all components.

(5) Flexible gain extension for different applications

Besides, comprehensive Charge-balance Transient-calculation (CT) modeling method and enhance CT modeling method are developed for accurate modeling and circuit stress analysis of switched capacitor converters with application constrains discussed. It has enriched the modeling technologies of switched capacitor converter fields, facilitated the high efficiency design of switched capacitor converter system.

The CT modeling technique has following features:

(1) Accurate

(2) Reveals the regulation property of switched capacitor converter by duty cycle and switching frequency

(3) Suitable for circuit stress analysis especially for high power design

(4) Suitable for interleaved SC converter modeling

Based on CT modeling method, the enhanced CT modeling technique has been developed and following new features are included:

(1) Output capacitor effect considered

(2) Suitable for both Interleaved and non-interleaved simple dual-phase SC converter

Based on the modeling methods, some new control technologies with fast response can be investigated to achieve accurate control. It will be the future research work of this part. Figure 3.1 has summarized the developed circuit and modeling system in part I and the future work based the established knowledge.

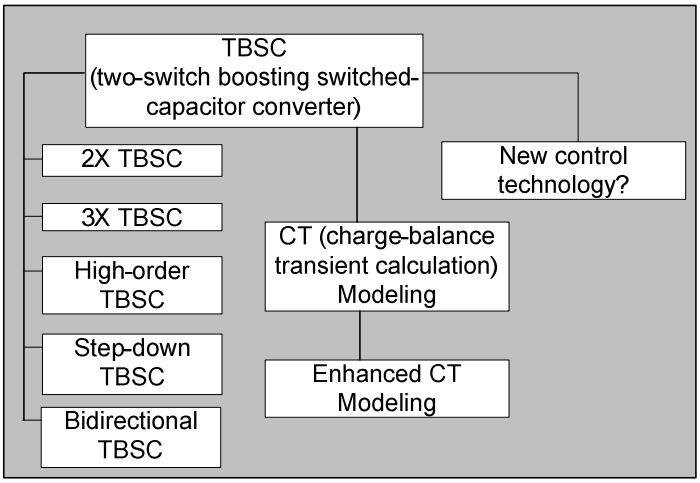


Figure 13.1 Developed and future work of Part I

Part I Hybrid Boosting Converter

As most important content of inductor based boosting technology, hybrid converter is investigated and a new topology system Hybrid Boosting Converters (HBC) is built in Part II. Within HBC family, four typical members Basic HBC, Isolated HBC, Symmetrical HBC and Tapped HBC are discovered. The common advantages of HBC family members can be summarized as:

(1) Partial symmetrical structure with duty cycle modulation, leading to reduced output ripple

(2) Potential for High power density design

(3) Simple regulation strategy

(4) Low voltage stress of all components

(5) Easy gain extension

While for each HBC family member, unique features should be considered according to application requirement. The Basic HBC has high efficiency and low cost properties. The

isolated HBC provides galvanic isolation and achieves fly-back-forward operation for isolation transformer. The Tapped HBC can realize greatly enhanced voltage gain by simple modification from Basic HBC. The Symmetrical HBC can operate with continues input current. They are supposed to satisfy different gain boosting applications.

Build upon the HBC family, a number of the extension circuits are developed. The single source paralleling technology based on HBC (3D DC-DC) provides an extremely flexible power expansion solution for high gain DC-DC converter with low cost. The multi-source paralleling technology presents a possibility of integrating independent voltage sources and storage elements through modular “plug and play” branches. The inverter extension based on HBC has found a “smooth” way to connect the HBC DC energy system to connect with the power grid or feed AC loads.

Finally, an investigation of Multi-bus DC micro-grid will be the future work of this part, which is tagged at a multi-function, flexible extension, and high efficiency micro power system. The circuit system developed in part II can future work can be concluded as in **Error! Reference source not found.**.

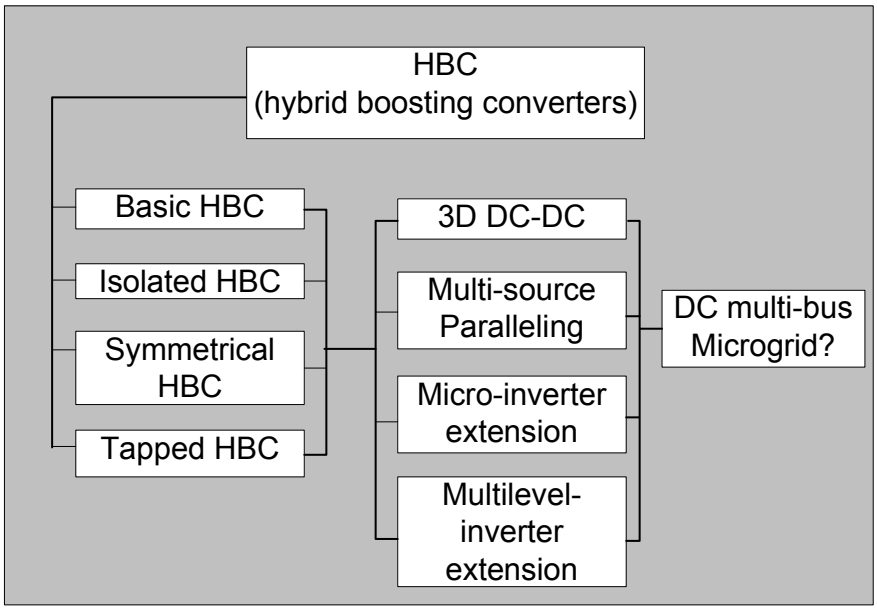


Figure 13.2 Developed and future work of Part II

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