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High-Efficiency and High-Power CMOS Power Amplifiers for Millimeter-Wave Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Amir Agah

Committee in charge:

Professor Lawrence Larson, Chair
Professor James Buckwalter, Co-Chair
Professor Peter Asbeck
Professor Andrew Kummel
Professor Brian Keating

2013

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The dissertation of Amir Agah is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California, San Diego

2013

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Chapter 2, in part, is a reprint of the material as it appears in "An 11% PAE, 15.8-dBm Two-Stage 90-GHz Stacked-FET Power Amplifier in 45-nm SOI CMOS," *IEEE Microwave Theory and Techniques* July 2013, and "A 45GHz Doherty Power Amplifier with 23% PAE and 18dBm Output Power, in 45nm SOI CMOS," *IEEE Radio Frequency Integrated Circuit Symposium,* July. The authors are Amir Agah, Jefy Jayamon, Hayg Dabag, Bassel Hanafi, Peter Asbeck, James Buckwalter and

Lawrence Larson. The authors are .author of this dissertation is the primary author and investigator of both papers.

Chapter 3, in part, has material submitted for publication in "A 42 to 47-GHz, 8-bit I/Q Digital-to-RF Converter with 21-dBm Psat and 16% PAE in 45-nm SOI CMOS," *IEEE Radio Frequency Integrated Circuit Symposium*. The authors are A.Agah, W. Wang, P. Asbeck, J. Buckwalter and L. Larson. The dissertation author is the primary author and investigator of this paper.

Chapter 4, in part, is a reprint of the material as it appears in "Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45-nm SOI CMOS *IEEE Journal of Solid-State Circuits*, October, 20013. The authors are Amir Agah, Hayg Dabag, Bassel Hanafi, Peter Asbeck, James Buckwalter and Lawrence Larson. The dissertation author is the primary author and investigator of this paper.

Chapter 5, in part, is a reprint of material as it appears in "Multi-Drive Stacked FET Power Amplifiers at 90 GHz in 45-nm SOI CMOS," submitted to *IEEE Journal of Solid-State Circuits*. The authors are Amir Agah, Jefy Jayamon, Peter Asbeck, James Buckwalter and Lawrence Larson. The dissertation author is the primary author and investigator of this paper.

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A.Agah, H. Dabag, B. Hanafi, P. Asbeck, J. Buckwalter, L. Larson, " Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45-nm SOI CMOS," *IEEE Journal of Solid-state Circuits*, vol. 48, no, 10, pp. 1-13, Oct. 2013.

A.Agah, W. Wang, P. Asbeck, L. Larson, J. Buckwalter, "A 42 to 47-GHz, 8-bit I/Q Digital-to-RF Converter with 21-dBm Psat and 16% PAE in 45-nm SOI CMOS" *IEEE RFIC*, pp. 249-252, June 2013.

A.Agah, H. Dabag, J. Buckwalter, "High-speed, High-Efficiency Millimeter-wave Transmitters at 45 GHz in CMOS" *IEEE IMS*, pp. 1-3, June2013.

A.Agah, J. Jayamon, P. Asbeck, J. Buckwalter, L. Larson, "An 11% PAE, 15.8-dBm Two-Stage 90-GHz Stacked-FET Power Amplifier in 45-nm SOI CMOS," *IEEE IMS*, pp. 1-3, June 2013.

A.Agah, H. Dabag, B. Hanafi, P. Asbeck, J. Buckwalter, L. Larson, "A 34% PAE, 18.6dBm 42-45GHz Stacked Power Amplifier in 45nm SOI CMOS," *IEEE RFIC*, pp. 57-60, June 2012.

A.Agah, H. Dabag, B. Hanafi, P. Asbeck, L. Larson, J. Buckwalter, "A 45GHz Doherty Power Amplifier with 23% PAE and 18dBm Output Power, in 45nm SOI CMOS," *IEEE IMS*, pp. 1-3, June 2012.

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H. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. Buckwalter, P. Asbeck "Analysis and design of stacked-FET millimeter-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, no.99, pp. 1543-1556, April 2013.

ABSTRACT OF THE DISSERTATION

High-Efficiency and High-Power CMOS Power Amplifiers for Millimeter-Wave Applications

by

Amir Agah

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor Lawrence Larson, Chair

Professor James Buckwalter, Co-Chair

This research focuses on the analysis and design of stacked-FET power amplifiers for millimeter-wave applications. We analyze the loss mechanisms in the stacked-FET PA circuit to develop the fundamental bounds on PAE and output power. Two-stack power amplifiers are designed and implemented at 45 and 90GHz achieving 19 and 15.8dbm output power with 34% and 11% PAE, respectively. The

gate resistance of the stacked-FET PA is demonstrated to be a dominant source of loss at high frequency. To overcome this limitation, a multi-drive stacked-FET approach is proposed to improve the output power and efficiency. An analysis of conventional and multi-drive stacked-FET PAs demonstrates the performance improvement. A multi-drive three-stack PA is implemented in 45-nm SOI CMOS for 90GHz operation occupying 0.23 mm^2. This PA achieves 19dBm saturated output power at a *PAE* of 14% and 12dB gain at 90 GHz using a 3.4-V power supply.

To achieve high output power and high efficiency with high data rates using QAM modulation, this research proposes a new stacked-FET transmitter in 45-nm SOI CMOS at 45 GHz, which shares a common DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high voltage swing without exceeding the breakdown voltage of the transistors in the stack. The circuit approach proposed here provides high RF output power at high efficiency along with a high-resolution DAC control to transmit complex modulation schemes. The use of high-resolution DACs enables the use of digital predistortion (DPD) to improve the error vector magnitude (EVM). The proposed architecture demonstrates 21.3 dBm saturated output power at a peak PAE of 16% into a 50 Ohms load impedance at 45 GHz, generating a 1.25-Gbps QPSK at an EVM of 5.5% using digital predistortion.

Considering that modern communication systems employ modulation techniques that exhibit high peak-to-average power ratios (PAPRs), demand for amplifiers with high efficiency over a wide power range is increasing. The traditional Doherty power amplifier is one of the circuits that satisfy this demand by providing

peak efficiency at 6-dB back off as well as peak power. In this work, the designed stacked-FET power amplifiers are utilized to make a Doherty power amplifier and a modified Doherty PA is proposed that addresses the limitations of the traditional design. The results demonstrate 4% improved back-off PAE as well as 1.5dB higher gain in comparison to the designed traditional Doherty PAs.

I

Introduction

I.A. Motivation for High-Power CMOS Millimeter-Wave Power Amplifiers

The demand for high data rate communication systems is growing rapidly and the millimeter-wave spectrum, with a broad frequency range available for high-capacity wireless communication, is drawing increasing attention. In particular, Q-band (30 to 50GHz) is relevant for satellite communication and automotive radar, while W-band (75 to 110GHz) applications include point-to-point communication as well as imaging and radar applications. Considering the long distance nature of these applications and due to high atmospheric losses at these frequency bands, power amplifiers with high output power are required for link budget, making the power amplifier's design one of the major challenges in the design of the mm-wave transceiver.

Although the cutoff frequency (f_t) of modern scaled CMOS technologies allows mm-wave operation, CMOS has never been a favorable choice for power amplifier design due to low drain-gate and drain-source breakdown voltages and poor passive element

quality factor. Traditionally, high-power high-efficiency PAs for mm-wave application were mainly fabricated using compound semiconductors such as GaAs, SiGe, InP and GAN, because these processes offer both high output power and high efficiency. Recent advances in wide bandgap GaN devices and materials have made high-power solid-state power amplifiers a real possibility at these frequencies and single-chip GaN based MMICs have been reported operating at frequencies up to 90 GHz with an output power level of typically 1.5W [1]. By using power combining techniques, W-band amplifiers with output power levels of up to 5W have been reported [2]. While these results are impressive, these technologies are both costly and, in many cases, low-yield with unacceptable performance variations, both within a given wafer and wafer-to-wafer.

However, future applications and broader commercialization are motivating researchers to develop circuit techniques, using the lower cost technologies such as CMOS, which can also offer the advantage of integration density on a single chip. And recent publications in the field [3][4], achieving 28dBm and 20dBm saturated output power at 43 and 79 GHz respectively, are showing that for the first time, CMOS is becoming a realistic alternative to III-V high-speed and high-power technologies in some applications.

I.B The Need for Efficiency Enhancement Techniques in Power Amplifiers

Power amplifiers are critical in the design of portable battery-operated communication systems, dominating the power consumption in the transmit mode.

For ideal Class-A and Class-B operation (assuming the knee voltage is zero), the drain efficiency is given by [5]

$$DE_A = \frac{1}{2}\frac{P_{RF}}{P_{RF,max}} \tag{1.1}$$

$$DE_B = \frac{\pi}{4}\sqrt{\frac{P_{RF}}{P_{RF,max}}} \tag{1.2}$$

As shown in equation (1.1) and (1.2), the efficiency of the class-A PA is proportional to the output power, while the efficiency of the class-B PA is proportional to the square root of the output power. And in both cases, the peak efficiency is achieved at peak output power. Therefore, a constant envelope modulation scheme was often employed to maximize the efficiency of the PA. However, modern communication systems employ modulation techniques that exhibit high peak-to-average power ratios (PAPRs) such as 64 and 128 QAM to achieve high data rates and high spectral efficiency. The PA linearity requirement for these modulation schemes is also high to avoid distortion of the signal, making the PA design even more challenging. Traditionally, linear PAs are implemented by backing off the Class-A or Class-AB PA, so that their average output power is well below the amplifier saturated power. Unfortunately, this decreases the average efficiency, since the PA is now operating in the low-efficiency region most of the time.

Many techniques have been proposed to improve the efficiency of the power amplifiers at backed-off output powers. One potential solution is the outphasing system [6][7].The outphasing system is based on the fact that the waveform $X(t)$ of a

carrier wave at radian frequency of ω_0 with arbitrary amplitude and phase modulation can be expressed as

$$X(t) = Re(\gamma(t)\exp(j\omega_0 t)) = S_1(t) + S_2(t) \tag{1.3}$$

where $\gamma(t)$ is a complex phasor waveform that captures the baseband modulation and S_1(t) and S_2(t) are

$$S_1(t) = X_m \sin\big(\omega_0 t + \angle\gamma(t) + \varphi(t)\big) \tag{1.4}$$

$$S_2(t) = X_m \sin\big(\omega_0 t + \angle\gamma(t) - \varphi(t)\big) \tag{1.5}$$

where X_m is the maximum of $|X(t)|$ and $0<\varphi(t)<\pi/2$ is called the outphasing angle.

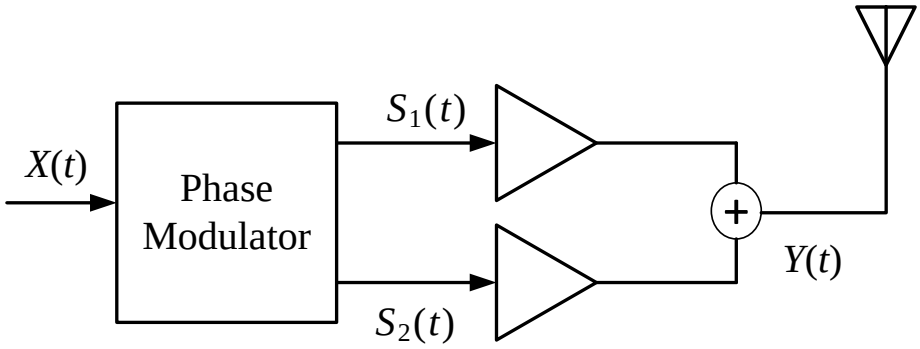


Figure 1.1. Block diagram of an outphasing transmitter

The block diagram of an outphasing system is shown in Figure 1.1, where an input signal containing both amplitude and phase modulation is divided into two constant-envelope phase-modulated signals [8]. An amplified version of the original signal is achieved by varying the phases of these two signals and summing the amplified branch signals with a passive power combiner. The maximum envelope is obtained when the branches are in-phase, while the minimum envelope is obtained when the branches are antiphase. The advantage of this technique is that highly

efficient nonlinear PAs can be used to amplify the two constant envelope signals, increasing the overall efficiency without degrading linearity. Nonetheless, the efficiency of an outphasing PA at back-off output levels is limited by the power dissipation in the switch-mode output stage and the constant driver power consumption. A conventional outphasing PA is also limited in its output power range, since a zero output power requires the two outphasing paths to cancel each other perfectly due to the variation and mismatch of scaled CMOS processes and other non-idealities[7].

In 1935, Chireix proposed a combining technique to improve the outphasing system efficiency in the back-off power using load-pulling effect [6]. However, the proposed reactively compensated combiner is not suitable for some switching PAs such as Class-E amplifiers, which require a load impedance with a specific phase to achieve high efficiency [7-8].

The other solution, which has received great interest in high efficiency PA research, is power amplifiers with dynamically changing supply voltage, such as envelope elimination and restoration (EER) and envelope tracking (ET) amplifiers [9]. Figure 1.2 shows the block diagram of typical EER and ET PA systems. The envelope amplifier provides a dynamically changing supply to the RF PA to keep its efficiency higher in the back-off region, as depicted in Figure 1.3.

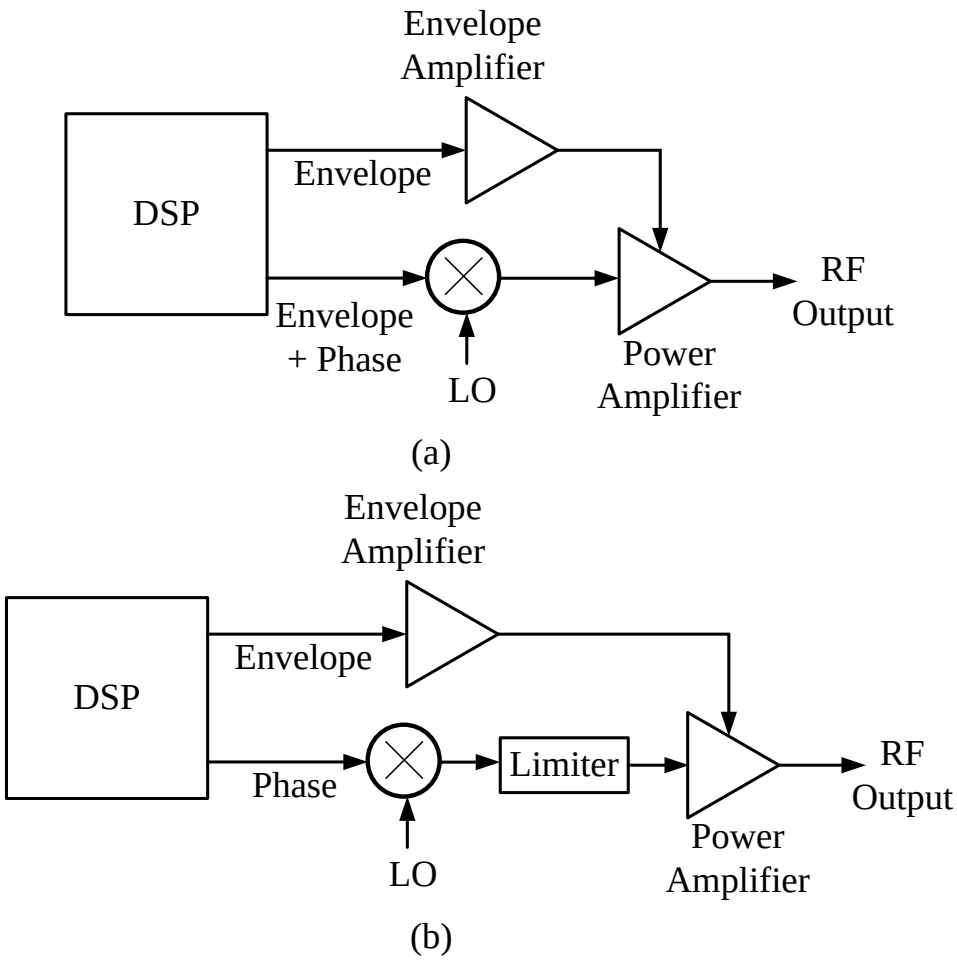


Figure 1.2. Block diagram of (a) ET and (b) EER system.

Although the envelope tracking technique has gained momentum as an effective efficiency enhancement technique for handset applications, its implementation still faces challenges. The efficiency of these systems is determined by the product of the envelope amplifier efficiency and the RF transistor drain efficiency. So it is equally important for the envelope amplifier to be highly efficient. Also, the envelope amplifier bandwidth should be larger than the envelope signal bandwidth, which makes the design challenging for wideband modulations. At the same time, the envelope amplifier provides all of the power amplifier current, which

puts a constraint on its size and usually requires external components. Using switching envelope amplifiers improves their efficiency. However, the switching noise is another impairment that can limit the transmitter performance.

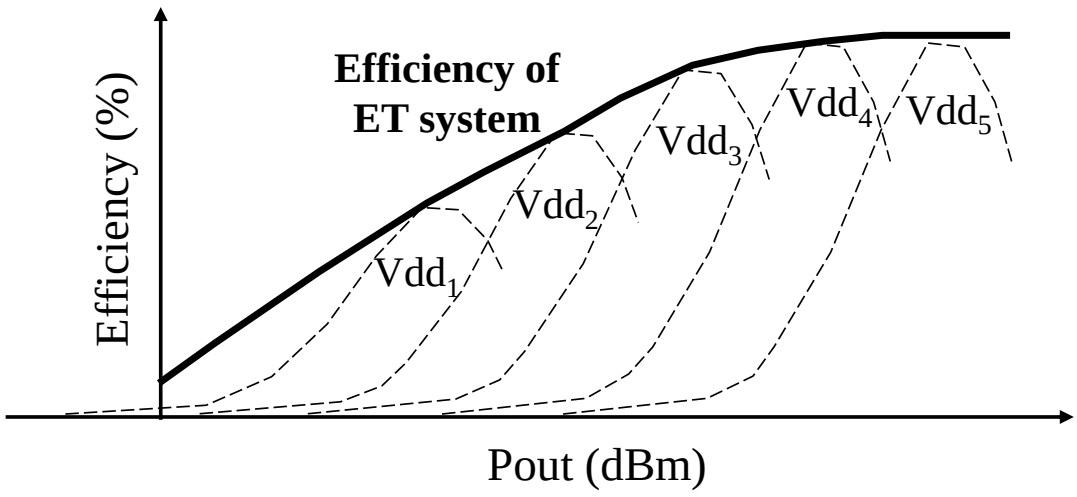


Figure 1.3. Efficiency as a function of output power for envelope tracking system.

In fact, an EER system is a polar transmitter in which the signal is decomposed into a constant-envelope RF phase-modulated signal and an envelope component. Several papers have demonstrated the suitability of such architectures for CMOS implementation [10-11], and polar transmitters that take advantage of the digital signal processing to ease the generation of phase and amplitude signals have been successfully implemented [12-13]. However, implementation of the amplitude modulation has typically limited the signal bandwidth of polar architectures to the vicinity of 1 MHz.

The Doherty power amplifier is another circuit that satisfies the demand for high efficiency at back off by providing peak efficiency at 6-dB back off as well as peak power. A conventional Doherty amplifier consists of two power amplifiers – a main amplifier and an auxiliary (peaking) amplifier – interconnected with two quarter-wavelength transmission lines as shown in Figure 1.4. The main amplifier is designed to be *on* at all input power levels, while the auxiliary amplifier is only *on* at high input power levels. This is achieved by biasing the auxiliary amplifier in class C and biasing the main amplifier in class A.

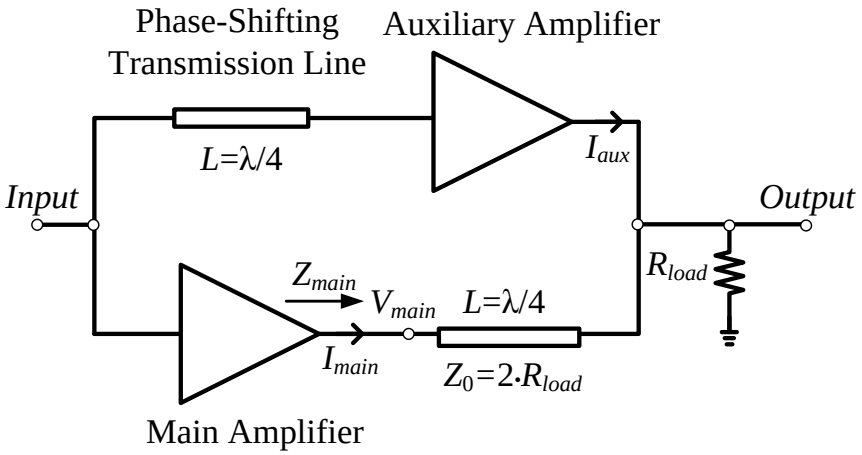


Figure1.4. Block diagram of Doherty Power amplifier.

The characteristic impedance of the transmission line at the output of the main amplifier is twice the load impedance and the current of the main amplifier and R_{load} are designed so that when $I_{main}=I_{main\text{-}max}/2$, Vmain reaches its maximum. Since the voltage swing is maximized, the efficiency of the main amplifier peaks as well.

Increasing the input power further increases I_{main} above $I_{main\text{-}max}/2$, and the auxiliary amplifier turns on, lowering the impedance seen at the output of the main amplifier.

Assuming infinite output impedance for the main and auxiliary amplifiers, the voltage at the output of the main amplifier is [14-15]

$$V_{main-HP} = \frac{{Z_0}^2}{R_{load}} \cdot I_{main} - jZ_0 I_{aux} \,. \tag{1.6}$$

Considering that $Z_0=2R_{load}$, if the output current of the auxiliary amplifier is set to

$$I_{aux} = -j2\left(I_{main} - \frac{I_{main-max}}{2}\right) \tag{1.7}$$

and substituted into (1.6), then V_{main} becomes independent of I_{main} and remains at its peak value. As a result, the efficiency of the main amplifier also remains at its peak even when $I_{main}>I_{main\text{-}max}/2$. However, the efficiency of the auxiliary amplifier is not at its maximum until it reaches its peak output power, at which point, the overall efficiency peaks. Figure 1.5 shows the simulated ideal drain efficiency of the Doherty PA as a function of the normalized output power, assuming zero knee voltage for the transistors and lossless transmission lines. Figure 1.4 also includes the simulated efficiency of the Doherty PA for different classes of operation for the main and auxiliary amplifier [16].

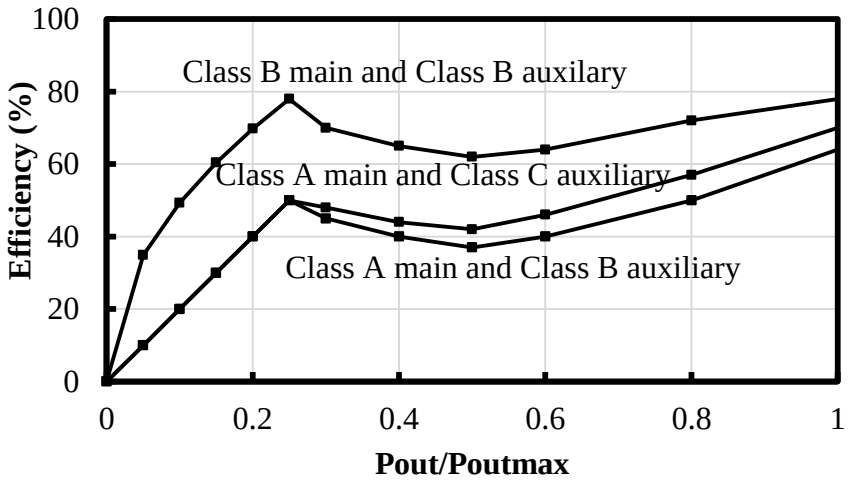


Figure1.5. Ideal drain efficiency of the conventional Doherty PA with different biasing for the main and auxiliary amplifier. Drain current conduction angle is 110° for class-C operation.

I.C. Previous Work on CMOS Millimeter-Wave Power Amplifiers

As mentioned in Section I.A, CMOS technologies have traditionally not been favorable for millimeter-wave PA applications, despite the high cutoff frequencies of modern scaled CMOS devices. The main drawback of CMOS FETs for PA applications is the low breakdown voltage. Considering the limited voltage swing of FETs, high output power can only be achieved if very wide FETs with low load impedances are used. However, the parasitic capacitances introduced by the layout of the FETs increases almost linearly with the width of the device, resulting in high losses and instability problems. Furthermore, the required impedance-matching networks required are high Q, lowering the efficiency and obtainable bandwidth.

Previous work on CMOS power amplifier design with large output powers at the millimeter-wave regime has been mainly focused on power combining techniques,

using Wilkinson combiners and transformer-based combiners. However, the low quality factor of passive components fabricated on silicon processes introduces high losses in the power distribution and combining networks, lowering the gain and efficiency of the PA. Additionally, these networks require a relatively large circuit area, increasing the fabrication cost per chip.

At the same time, the output power from a single power amplifier generally falls as the frequency of operation increases, resulting in a larger number of PAs required for a given output power. Scaling the power distribution network for a large numbers of PAs results in diminishing returns, after which it becomes difficult to yield any further improvements in output power. Wilkinson power combiner is one of the most widely used power combiners in industry, which also provides isolation between combiners input by acquiring quarter wave-length transmission lines. Therefore Wilkinson power combiners are area hungry and use of quarter-wave length transmission lines increases the combining loss, especially if implemented on-chip. However, assuming that all combiner inputs have zero-degree phase difference, port isolation is no longer a major constraint and the requirement for exact quarter-wavelength segments in the Wilkinson combiner is removed and shorter lines can be used as long as they satisfy impedance transformation requirements. One of the best examples of this approach is presented in [4], which power combines 16 power amplifiers, achieving 28dBm output power at 45GHz. However the peak efficiency is only 10% and the PA occupies 5.55 mm^2.

Transformer-based power combining is the other common technique, which can increase impedance-transformation ratio by increasing the number of input ports,

resulting in a compact layout and low loss [3]. However, at millimeter-wave frequencies, the behavior of a transformer departs far from that of a lumped element, limiting the combiner's efficiency because of additional phase delays. Examples in [3] and [17] are among the best examples of using this technique, achieving 19.3 and 20 dBm saturated output power at 79 and 60 GHz respectively.

An alternative to passive power combining is the FET-stacking circuit technique [18-19], which solves two significant problems. First, FETs can be stacked to support higher supply voltages and a higher RF voltage swing at the output. In principle, with N transistors in the stack, the overall structure can tolerate $N \times BV_{ds}$, where BV_{ds} is the drain-source breakdown voltage of a single FET. Second, the stacked-FET approach also increases the loadline impedance for each additional FET, allowing lower loss impedance matching at the output.

Figures 1.6 and 1.7 show the efficiency versus output power of recently published silicon Q-band and W-band power amplifiers, including the PAs implemented in this work. These graphs also compare CMOS PAs with BiCMOS PAs, indicating that CMOS is becoming a realistic competitor for BiCMOS technology in millimeter-wave PA designs. This graph shows that this work achieves the highest PAE among all the 45GHz silicon PAs and the highest output power and efficiency between all the published silicon PAs above 80GHz.

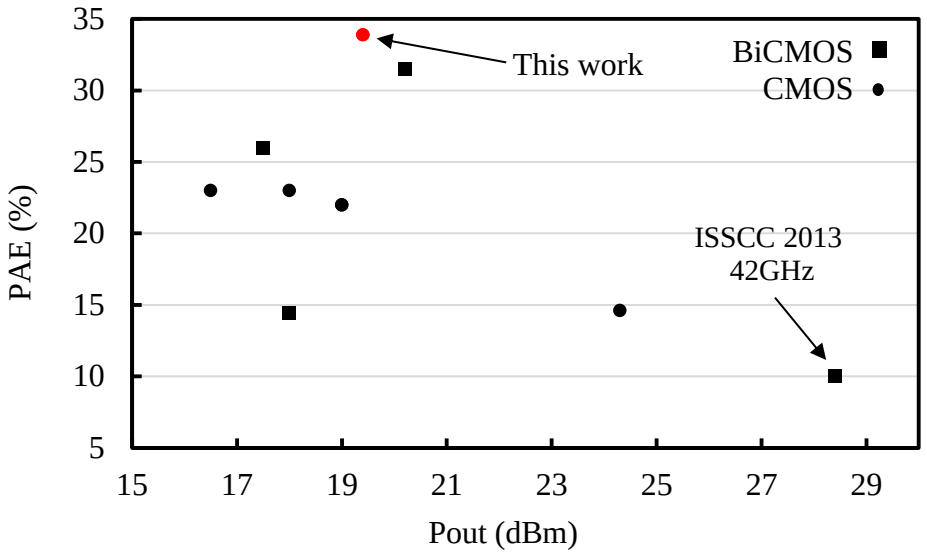


Figure 1.6. PAE versus output power of recently published Q-band PAs.

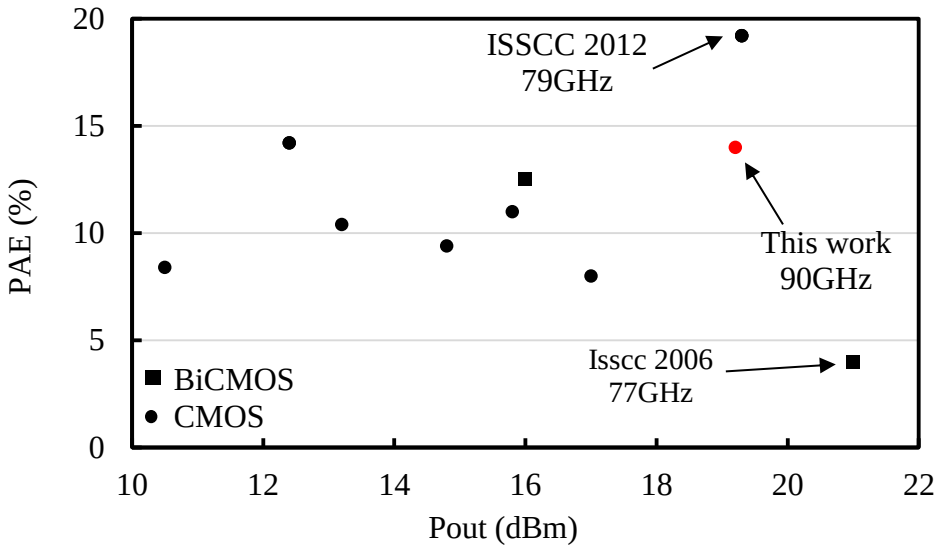


Figure 1.7. PAE versus output power of recently published W-band PAs.

I.C. Dissertation Organization

In Chapter II, stacked-FET power amplifiers are introduced and analyzed to develop the fundamental bounds on PAE and output power over frequency. Using the

results of the analysis, two-stack PAs are implemented and designed at 45 and 90GHz in 45-nm SOI CMOS technology.

In chapter III, the stacked-FET technique is utilized to design a 45GHz I/Q modulator with high efficiency and high output power. The experimental results are presented and compared with previous work.

In Chapter IV, the working principles of the traditional Doherty power amplifier are presented and two 45GHz Doherty PAs are implemented, using grounded coplanar waveguides and slow-wave coplanar waveguides in 45-nm SOI CMOS. An active phase-shift Doherty PA is then proposed, analyzed and implemented, reducing the chip area and improving the gain and efficiency in comparison to the traditional designs.

Chapter V proposes the multi-drive stacked-FET PA along with its analysis, addressing the limitations of the stacked-FET technique at millimeter-wave frequencies. The multi-drive three-stack PA is implemented in 45-nm SOI CMOS, achieving more than 19dbm saturated output power with 14% PAE at 90GHz.

II

Stacked-FET Power Amplifiers for Millimeter-Wave Applications

II.A. Introduction

The demand for higher data rate communication systems is growing rapidly and the millimeter-wave spectrum offers a broad frequency range for high-capacity wireless communication. One of the major challenges for mm-wave transceiver design is the power amplifier. Traditionally, high power, high efficiency PAs for mm-wave application were mainly fabricated using compound semiconductors such as GaAs, SiGe and InP. However, future applications are motivating the use of lower cost technologies like CMOS, which can also offer the advantage of integration density on a single chip. Although the cutoff frequency (f_t) of modern scaled CMOS technologies allows mm-wave operation, CMOS has never been a favorable choice

for power amplifier design due to low drain-gate and drain-source breakdown voltages, and poor passive element quality factor.

One potential solution to achieve a higher output power is to combine the output power of several PAs. This technique increases the output power, but efficiency is compromised due to the loss of the power combiner and power distribution network [17],[3],[4].

FET-stacking is an alternative technique that allows higher power without causing breakdown of FETs [23-24].

This chapter presents the analysis of the stacked-FET power amplifiers, demonstrating how all the elements in the stack should be selected to optimize the performance of the stacked-FET PA.

Using this analysis, a two-stack PA for 45GHz operation in 45-nm SOI CMOS is designed and measured, achieving an output saturated power of greater than 18.6dBm with 34% peak PAE from a 2.7V supply.

Although the designed two-stack PA demonstrates a promising output power level and efficiency, the gain of the single stage PA is only 8 dB at 45 GHz. Therefore, this work studies methods to optimize a two-stage amplifier design with high gain and minimal impact on efficiency. A multi-stage stacked-FET PA is designed, fabricated and measured at 45 GHz using 45nm SOI CMOS. The same approach is also utilized to design a two-stage PA at 90GHz and it is demonstrated that by modifying the inter-stage matching, this two-stage design achieves wide bandwidth.

II.B. Analysis of Stacked FET PAs

Nanometer scale CMOS FETs traditionally suffer from low breakdown voltage. To overcome this limitation, a FET-stacking technique is utilized to achieve high output voltages without sacrificing reliability. By using the stacking technique, the power supply voltage can be $N \times BV_{DS}$, where N is the number of stacked FETs and BV_{DS} is the drain-source breakdown voltage of a single device.

Figure 2.1 shows the schematic of a stacked-FET amplifier and Figure 2.2 shows the simulated drain and gate voltages of the FETs in a two-stack FET PA of Figure 2.3. As shown in Figure 2.2, the d.c. voltage is equally distributed between the FETs, allowing operation with a power supply of 2.5 V.

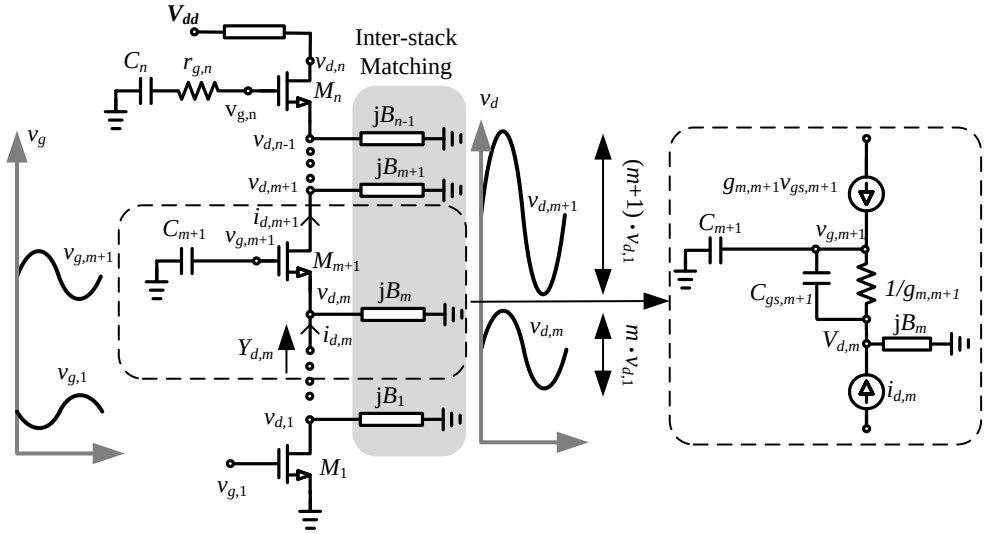


Figure 2.1 . Schematic of the main amplifier using a stacked-FET technique.

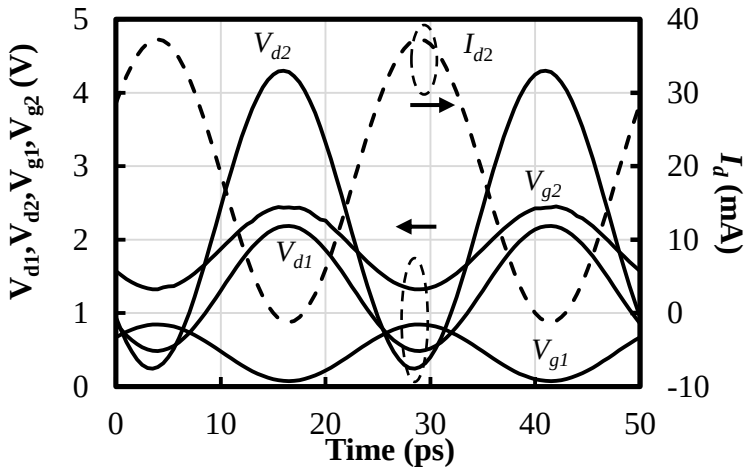


Figure 2.2. Simulated 45-GHz waveforms of a two-stack amplifier.

For reliable operation of the FETs in the stacked architecture, the peak RF voltage swing seen over V_{dg} and V_{ds} of each device should be kept below a certain breakdown voltage as well. Preliminary reliability measurements in [23] and [24] shows that this voltage is approximately 2.5 V peak for V_{dg} and V_{ds}. To address this problem, the RF swing should be distributed equally between the FETs in the stack as shown in Figure 2.2. Hot carrier injection is the major cause of degradation of FETs in power amplifiers [25]. In traditional analog circuits with constant bias current, the degradation has been found to be a quasi-static phenomenon, i.e. the total amount of degradation can be predicted by integrating voltage and current waveforms. However, in power amplifier as shown in Figure 2.2, the current through the FETs is almost zero, when V_{ds} reaches its maximum value. This low current is shown to reduce the probability of hot carrier injection significantly [26].

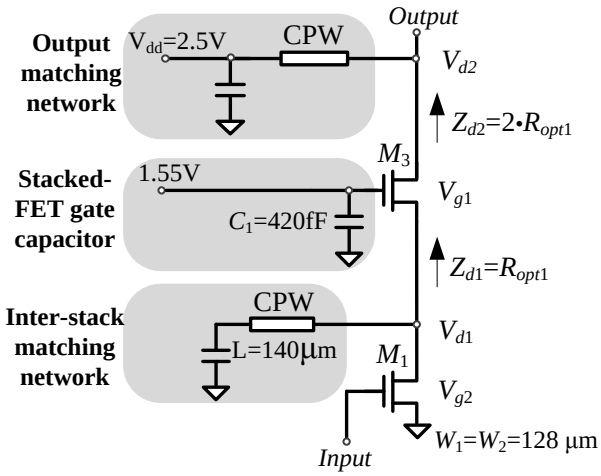


Figure 2.3. Schematic of the main amplifier using a stacked-FET technique.

In stacked-FET power amplifiers, the RF voltage swing should be equally distributed among all the FETs such that $|V_{ds,1}|=|V_{ds,2}|= \cdots =|V_{ds,n}|$. The maximum output voltage swing and therefore the maximum output power for a stacked-FET PA is achieved if all the drain-source voltages are in phase i.e.

$$V_{d,m+1} \cong \frac{m+1}{m} \cdot V_m \,, \tag{2.1}$$

where V_{d_i} is the RF swing at the drain of the i^{th} FET in the stack.

A high V_{dg} is the other cause of breakdown. The gate of FETs in the stack are not RF grounded, allowing a limited gate voltage swing, preventing the breakdown of the stacked FET by lowering the V_{dg} and V_{gs} as shown in Figure 2.2.

Assuming that the relationship between $V_{d,m}$ and $V_{d,m+1}$ is determined by (2.1), the admittance at the drain of M_{m} is

$$Y_{d,m}(s) \cong \left(sC_{gs,m+1} + g_{m,m+1}\right)\left(\frac{C_{m+1} - \frac{1}{m}C_{dg,m+1}}{C_{m+1} + C_{gs,m+1} + C_{dg,m+1}}\right). \tag{2.2}$$

Using the small-signal model of the stacked-FET PA shown in Figure 2.1 and assuming that the imaginary part of this admittance is resonated with the inter-stack matching network i.e.

$$B_m(\omega) = \omega C_{gs,m+1}\left(\frac{C_{m+1} - \frac{1}{m}C_{dg,m+1}}{C_{m+1} + C_{gs,m+1} + C_{dg,m+1}}\right), \tag{2.3}$$

the relationship between the drain currents of M_m and M_{m+1} becomes

$$I_{m+1} = I_m\,, \tag{2.4}$$

ensuring that all the drain voltages of the FETs in the stack are in phase.

However without the inter-stack matching network, the relationship between the drain currents of M_m and M_{m+1} is

$$I_{m+1} \cong \frac{1}{1 + j\frac{\omega}{\omega_t}} I_m\,, \tag{2.5}$$

where ω_t is the unity current gain frequency of the FET. Equation (2.5) shows the importance of inter-stack matching network in the stacked-FET PA, especially, when the frequency of operation is close to the f_t of the device.

According to [5] the optimum load conductance for a PA, resulting in the best efficiency and output power is $G_{opt} = i_{sw}/v_{sw}$, where i_{sw} and v_{sw} are the maximum ac current amplitude and peak voltage at the output of the PA. Assuming (2.1), the

optimum admittance required at the m^{th} stage of the stacked-FET PA is real and equal to

$$G_{opt,m} = \frac{i_{sw}}{v_{sw}} = \frac{i_{sw-FET}\prod_{k=2}^{m}|\alpha_k|}{m v_{sw-FET}} = \frac{\prod_{k=2}^{m}|\alpha_k|}{m} G_{opt-FET}. \quad (2.6)$$

where $G_{opt\text{-}FET}$, $i_{sw\text{-}FET}$ and $v_{sw\text{-}FET}$ are the optimum load conductance, maximum FET ac current and ac voltage and α_m is the current gain between two consecutive FETs in the stack defined as

$$\alpha_m = \frac{i_{d,m}}{i_{d,m-1}}. \quad (2.7)$$

Assuming that inter-stack matching is selected according to (2.3), α_m=1 and (2.6) becomes

$$G_{opt,m} = \frac{i_{sw}}{v_{sw}} = \frac{1}{m} G_{opt-FET}. \quad (2.8)$$

Using (2.8) and (2.2), the required capacitance at gate of each FET in the stack is

$$C_{m+1} \approx \left(\frac{g_{m,m+1}}{G_{opt,m}} - 1\right)^{-1} \left(C_{gs,m+1} + C_{dg,m+1}\right) \quad (2.9)$$

Assuming that gate capacitance (C_m) at each stage of the stacked-FET PA is optimized using (2.9) and $B_m(\omega)$ is optimized according to (2.3), the drain efficiency (*DE*), output power (P_{out}), and power-added efficiency (*PAE*) of the *n*-stack PA with identical devices in the stack are

$$DE_{n-stack} \cong DE_{FET} \quad (2.10)$$

$$P_{out,n-stack} = n\, P_{out,FET} \quad (2.11)$$

$$PAE_{n-stack} = \frac{n\, P_{out,FET} - P_{in}}{n P_{DC-FET}} = DE_{FET}\left(1 - \frac{1}{nG_{FET}}\right) \cong DE_{FET} \quad (2.12)$$

where $P_{out,FET,}$ $DE_{FET,}$ $P_{DC\text{-}FET}$ and G_{FET} are the output power, drain efficiency, power consumption, and gain of a single common-source FET. Equations (2.10-12) show that the output power of a stacked-FET PA increases linearly with the number of FETs in the stack, without any efficiency penalty. However, this analysis doesn't take into account gate resistance of the FETs and low quality factor of the passives elements in the stacked-FET PA. Effect of these non-idealities on the performance of the stacked-FET PA will be discussed in details in Chapter III.

II.C. Technology and Device Modeling

The IBM 45nm SOI CMOS is the process used in this work. In this process, the transistor body is partially depleted and contained inside a 225nm thick buried oxide layer, isolating the transistor from the 13.5Ω-cm (low resistivity) silicon bulk and reducing the source-drain junction capacitor. The 11 metal layers above the silicon substrate are made of copper except the top 2.2μm aluminum LB layer. Figure 2.4 shows the metal stack in 45nm SOI CMOS.

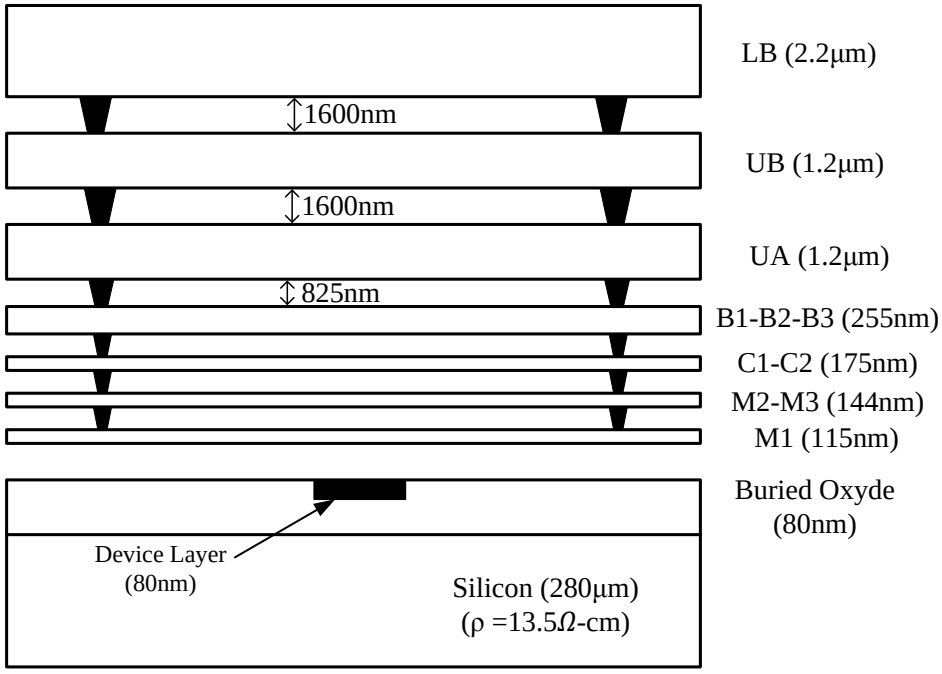


Figure 2.4. 45nm SOI CMOS metal stack-up.

To characterize the metals used in the process, a ground shielded coplanar waveguide (CPW) is implemented using LB as the signal line and B_3 and B_2 for the ground plane. The width of the signal line is 8μm with 8μm spacing to the side ground planes creating a 50Ω transmission line. Figures 2.5 and 2.6 show the measured and simulated amplitude and phase of the implemented 800μm long 50Ω CPW, demonstrating a good agreement between the simulation and measurement.

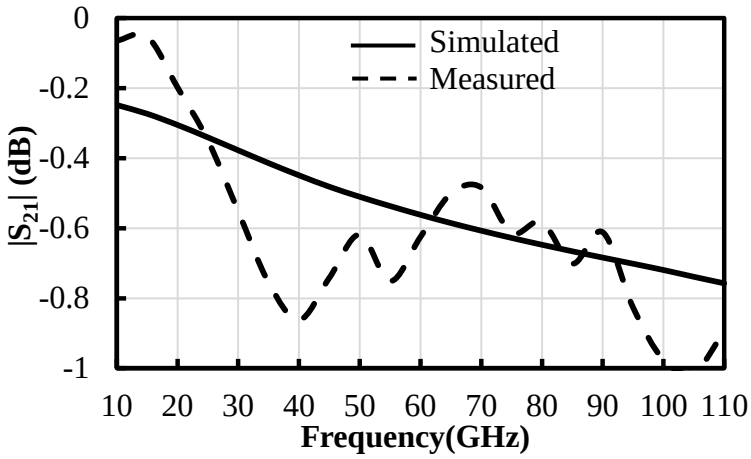


Figure 2.5. Simulated and measured amplitude of S_{21} for an 800μm 50Ω CPW.

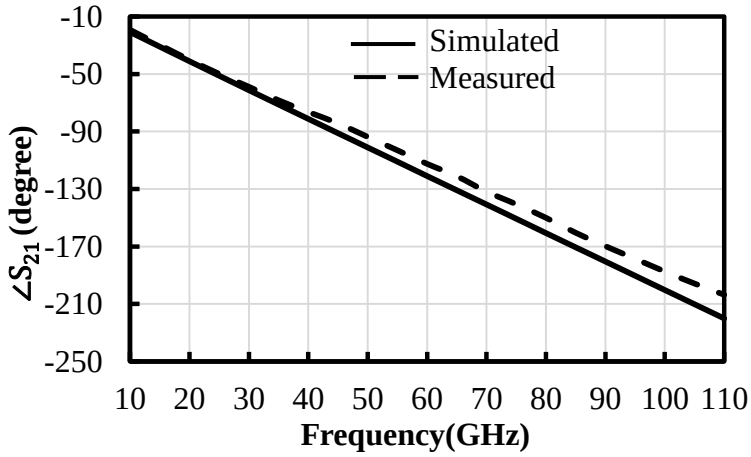
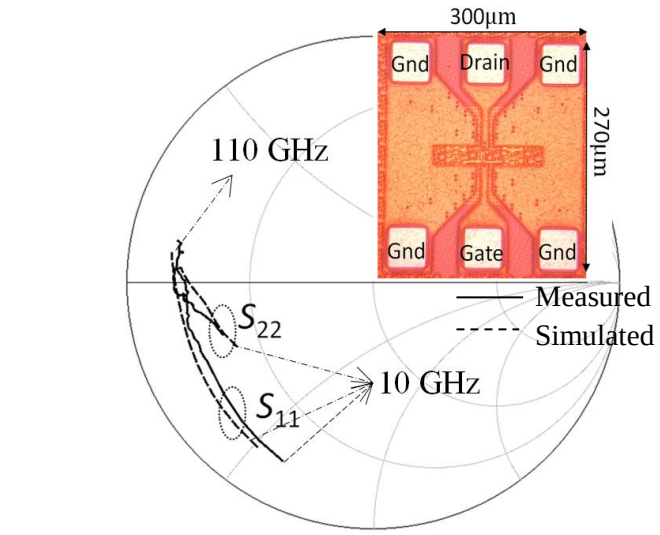


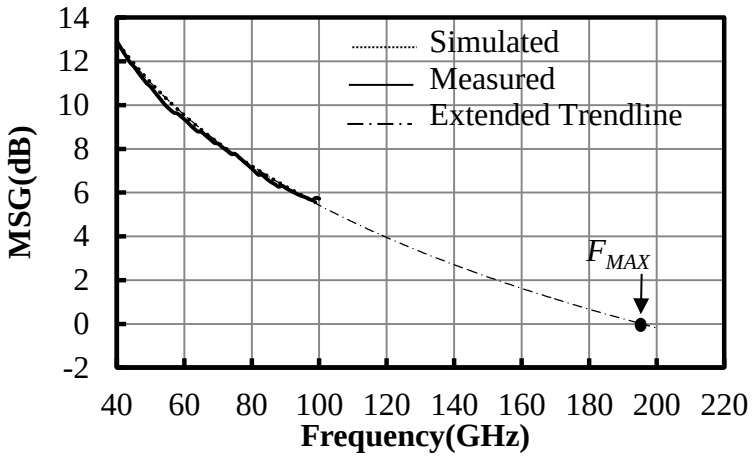
Figure 2.6. Simulated and measured phase of S_{21} for an 800μm 50Ω CPW.

A 256μm×40nm FET test structure is used to characterize the device, and the measured S_{11}, S_{22} and maximum stable gain (*MSG*) are plotted in Figure 2.6 along with a photomicrograph. The *MSG* curve has been extrapolated showing an f_{MAX} of 190 GHz for this device, which is more than 100GHz bellow the simulated f_{MAX} of a native device due to parasitic resistance and capacitances of the vias and other interconnects up to the top metal. To match the simulation with the measurement

results, the inductances of these interconnects in the FET layout are modeled using Sonnet™ and have been added to the gate, drain and source of the RC extracted view. Simulations are plotted in Figure 2.7 to show the agreement of the models with the measurements.



(a)



(b)

Figure 2.7. Simulated and measured, (a) S11, S22 from 10 to 110GHz (b) MSG of a 256µm NFET.

II.D. Design of stacked-FET PAs

In this Section, the design process for 45 and 90GHz stacked-FET power amplifiers in 45nm SOI CMOS are explained.

II.D.I. 45GHz Two-Stack FET PA

The schematic of the 45GHz two-stack power amplifier is shown in Figure 2.8.

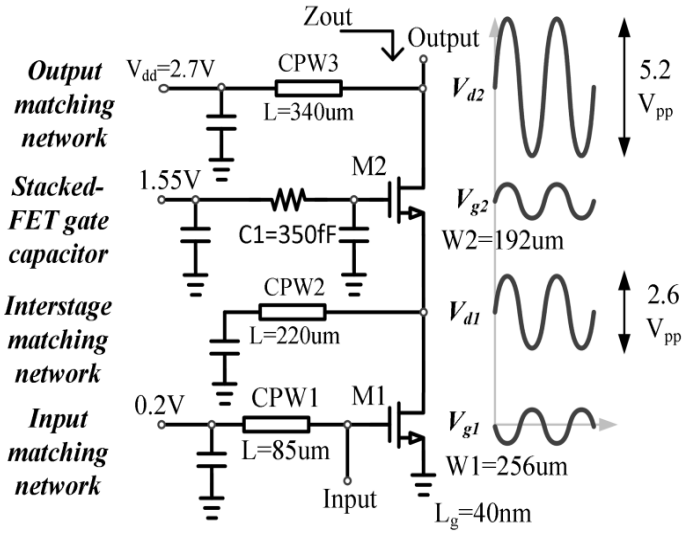


Figure 2.8. Schematic of the two-stack power amplifier.

Figure2.9 shows the load-line simulation for a FET with W=256μm and L=40nm. Considering Figure2.5 and Equation (2.8), the optimum load of the two-stack PA with W_1= 256μm and Vdd=2.5V is 50Ω, eliminating the need for impedance matching network at the output of the PA. As shown in Figure2.8, the output matching network only consists of a shunt transmission line for susceptance cancellation, which also

provides a path for Vdd. The width of this transmission line is 30μm which provides a low resistance path for Vdd to avoid any IR drop.

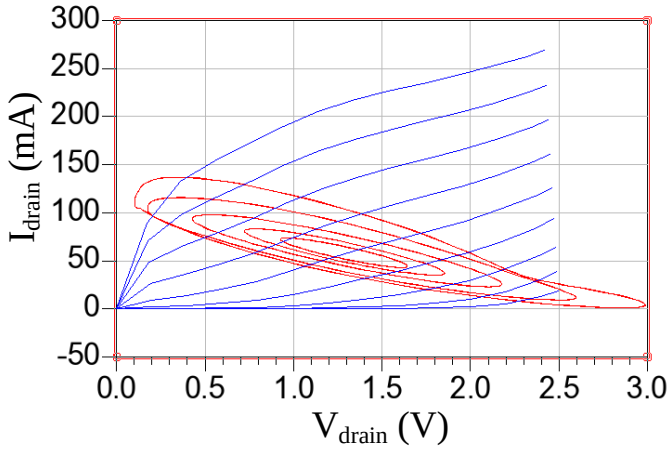


Figure 2.9. Load line simulation for a FET with W=256μm and L=40nm.

The inter-stack matching network is designed according to (2.3), resonating with the imaginary part of Y_{d1}. Simulation indicates that the use of inter-stack matching network increases the PAE by approximately 6%.

The capacitance at the gate of M2 is designed according to (2.9) and W_2=192μm, providing a 25Ω impedance at the drain of M1.

Considering the finite gate swing of the stacked FET, and the fact that the total capacitance to ground at the drain of M1 and M2 are tuned out using CPW2 and CPW3 at the operating frequency, the output impedance of the stacked amplifier is:

$$Z_{out} \cong r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2} \frac{C_1}{C_1 + C_{gs2}} . \qquad (2.13)$$

This differs from the Zout of the traditional cascode by the presence of the $C_1/(C_1+C_{gs2})$ factor. Equation (2.13) illustrates that the output impedance and therefore

voltage gain $g_{m1}(Z_{out} \parallel R_{load})$ of the stacked-FET is lower than that of the traditional cascode. This is a compromise that is necessary in order to prevent FET breakdown, while achieving high output powers.

II.D.II. 45GHz Two-Stage PA

In mm-wave PAs, the ratio of the f_t of the device to the RF carrier frequency is low so the power gain of a single stage is low. We wish to investigate preamplifier circuit design that increases the overall PA gain. To achieve the best gain and efficiency, interstage matching networks must provide the optimal load between stages. However, losses in the interstage matching networks reduce the overall gain and efficiency.

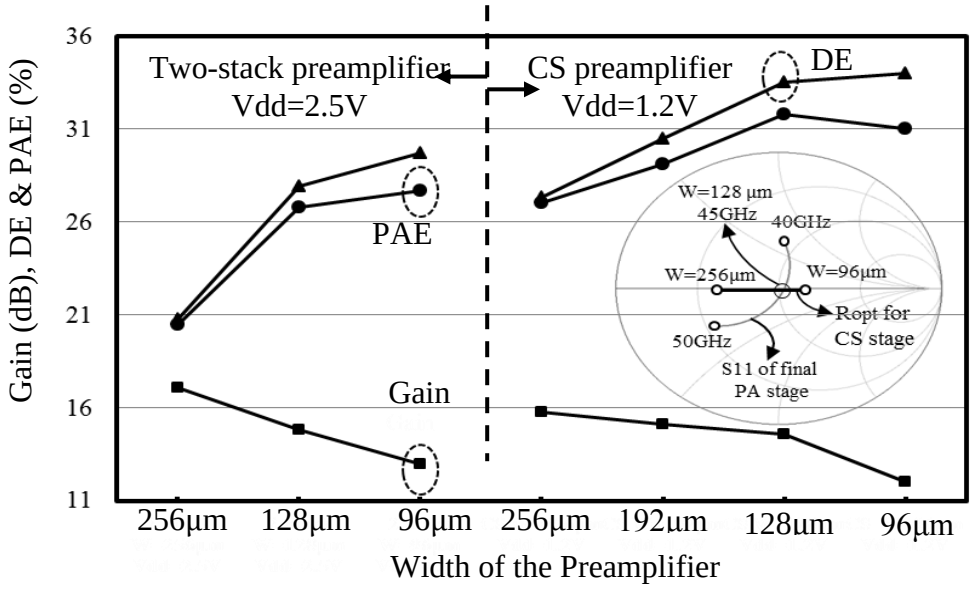


Figure 2.10. Simulated DE, PAE and gain of the two-stage PA for different pre-amplifier circuits, S11 of the final PA stage with optimum load for different FET geometries of CS preamplifier.

The number of stages and size of each transistor in the final stacked FET PA is chosen to provide 19dBm output power and a loadline impedance close to 50 Ω to avoid high-Q output matching networks. From Section II.C.I, a two-stack PA with W_2=256 μm and Vdd=2.6 V is selected to be the final stage in this work.

To determine the pre-amplifier circuit architecture, which most efficiently increases the gain of the two-stack final stage, different FET geometries of 2-stack PAs with 2.5 V power supply and CS amplifiers with 1.2 V supply are investigated and results are shown in Figure 2.10. Smaller FETs are not included in this study since they cannot provide enough power to compress the final stage or the gain is not sufficient. This simulation shows that a CS PA with W=128μm and 1.2-V power supply is the best choice for the highest PAE.

The conclusion reached in Figure 2.10 can also be explained with theory. Since the output stage has 8 dB power gain and 19dBm saturated output power, the pre-amplifier should only deliver 11 dBm output power. The two stack PAs with W_2>128 μm are not efficient to use at 11dBm output power. On the other hand, the smaller geometries of the two-stack preamplifier require a high Q impedance transformation network, which is lossy and the additional gain become negligible. However, a CS PA with W=128 μm and 1.2-V power supply delivers enough power to compress the final stage and as shown in Figure 2.6 its optimum load is identical to the input impedance of the final stage with use of a shunt transmission line, which results in the minimum loss in the interstage network and best overall PAE. The schematic of the designed two-stage PA is shown in Figure 2.11.

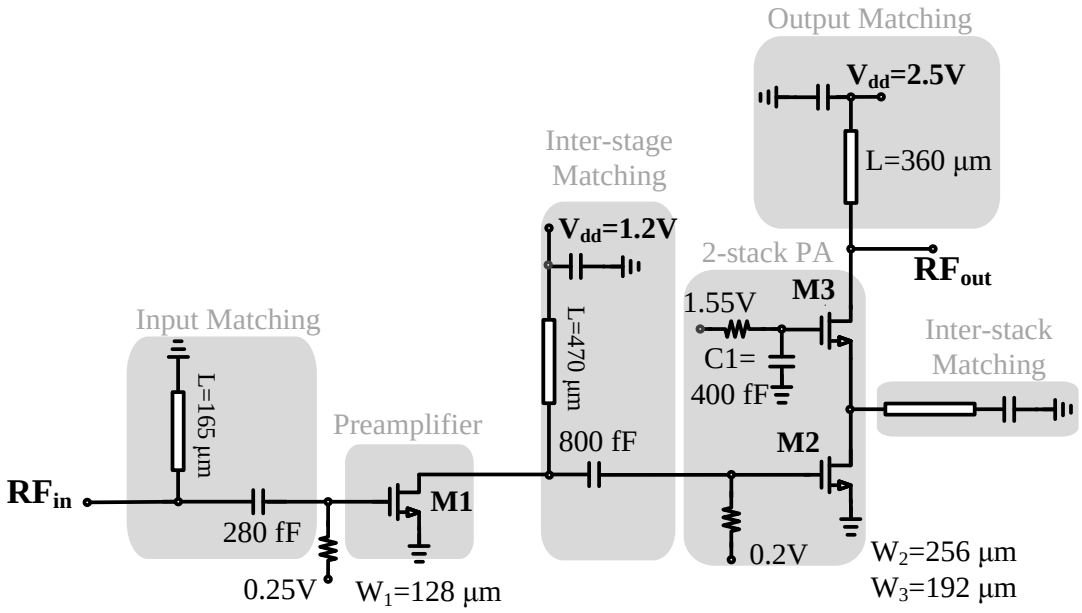


Figure 2.11. Schematic of the two-stage power amplifier.

II.D.III. 90GHz Two-Stack FET PA

In 45-nm SOI CMOS, the f_t of the MOS devices is approximately 200 GHz. To compensate for the modest available gain at the operating frequency (90 GHz), multiple amplifier stages are required to reach gain greater than 10 dB.

To achieve the highest possible efficiency, each amplifier is loaded with the optimal impedance, which is $R_{opt}=V_{sw}/I_{sw}$. The driver stage should deliver enough power to saturate the following stage and the power consumption of the preamplifiers is significantly lower than the final stage.

Figure 2.12 shows the schematic of the two-stage amplifier. The final stage is a two-stack PA with W_2=256μm and 2.8V power supply and the preamplifier is a common-source amplifier with W_1=128μm and 1.4V supply. Measurements indicate

that at the peak PAE point, the driver consumes approximately 110mW of DC power, while the final stage consumes 160mW.

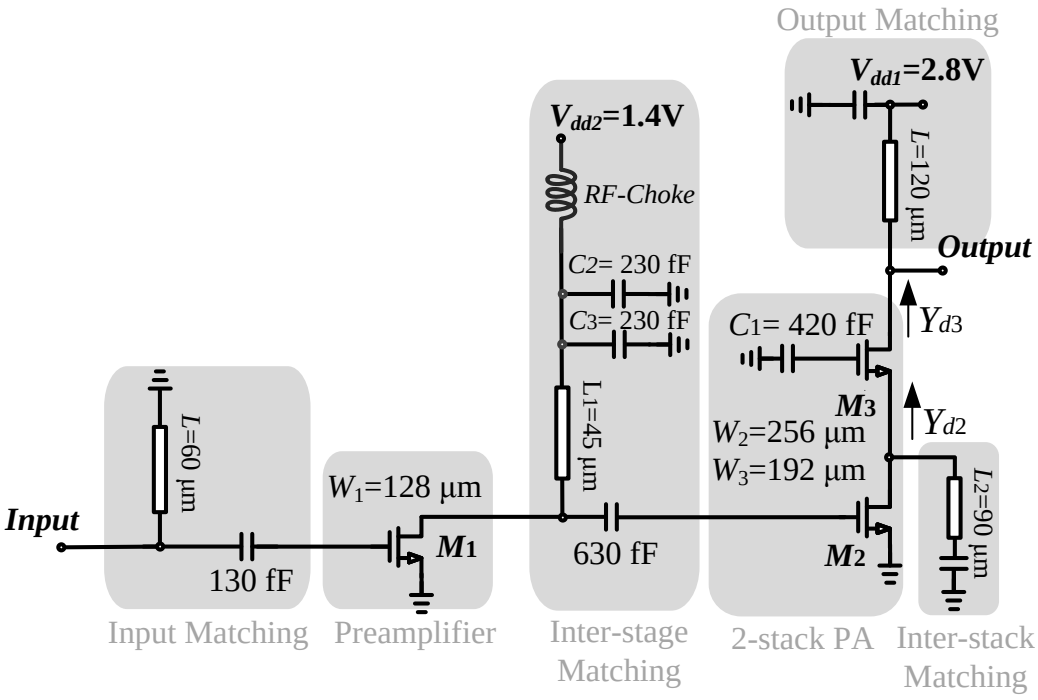


Figure 2.12. Schematic of the two-stack power amplifier.

Simulations and previous work on mm-wave FET-stacking techniques shows that the saturated output power of the stacked-FET PA is not a strong function of frequency, and the 3-dB gain bandwidth of the stacked-FET PAs is smaller than the 3-dB saturated output power bandwidth. Therefore, two strategies can be used to design a multi-stage PA as shown in Figs. 2.13 (a) and (b). Figure 2.13 (a) is the case, where matching networks of both the driver and the final stage amplifiers are designed to have peak S_{21} at the same frequency, resulting in the highest gain and efficiency for the cascaded architecture. This is the design, which is implemented in this work. In

Figure 2.13 (b), the peaks of each amplifier are slightly shifted to achieve the widest bandwidth, at the expense of gain and efficiency.

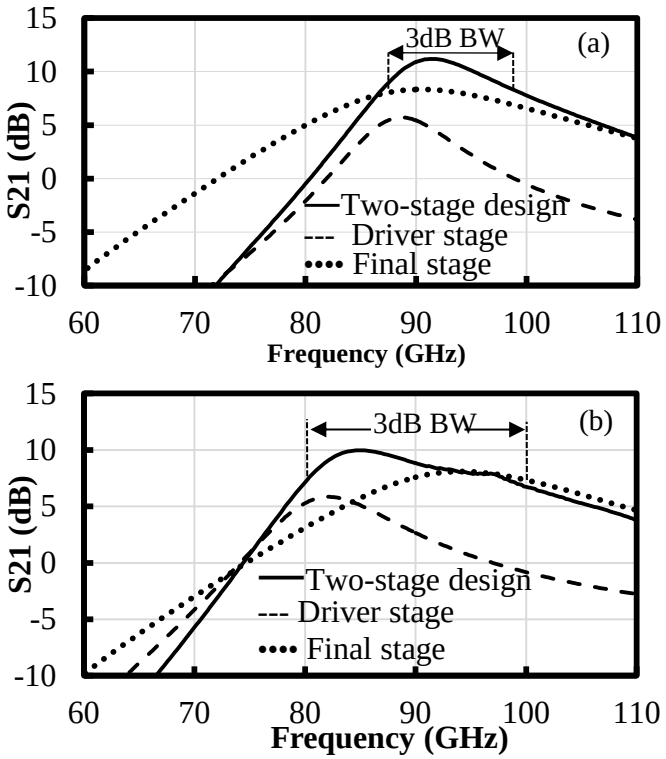


Figure 2.13. Simulated S21 of (a) the high gain configuration, (b) the wide band configuration.

The inter-stage matching network between the CS amplifier and the final stage is shown in Figure 2.12. If C_2 is eliminated from the inter-stage matching network, the peak gain of the preamplifier shifts to lower frequency resulting in the wideband response of the cascaded PA similar to the response shown in Figure 2.13 (b). In the measurements, responses of the both wideband and narrowband PAs are measured by

removing C_2 from the inter-stage matching network of the tuned PA shown in Figure 2.12.

II.E. Measurements and Comparison

In this Section, the measurement results for the three power amplifiers explained in Section II.D are presented and compared with the previous work.

II.E.I. 45GHz Two-Stack PA

Figure 2.14 is a chip photomicrograph of the two-stack PA fabricated in a 45nm SOI CMOS process. The area of the PA is 0.3mm^2 including the pads.

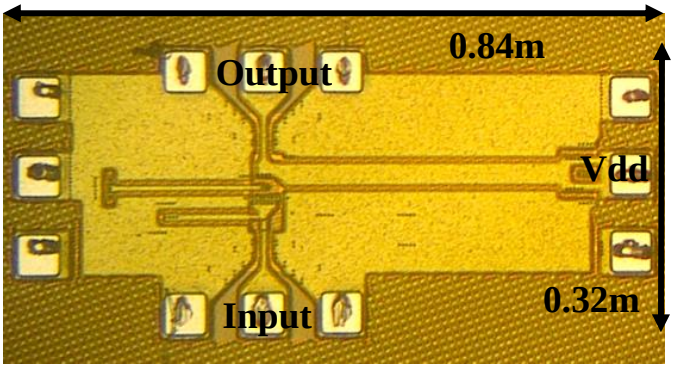


Figure 2.14. Photomicrograph of two-stack PA.

The simulated and measured S-parameters are compared in Figure 2.15. The agreement is good over a wide frequency range. As shown in Figure 2.15, the measured S_{21} and S_{11} are tuned to 42GHz instead of 45GHz. This difference can be explained by parasitic inductances in the device layout, which are not taken into account in the simulations. This measurement shows a peak S_{21} of more than 8dB, when biased in class AB mode. This measurement is further confirmed with the large-signal measurement since this PA achieves the best gain, PAE and Pout at 42.5GHz.

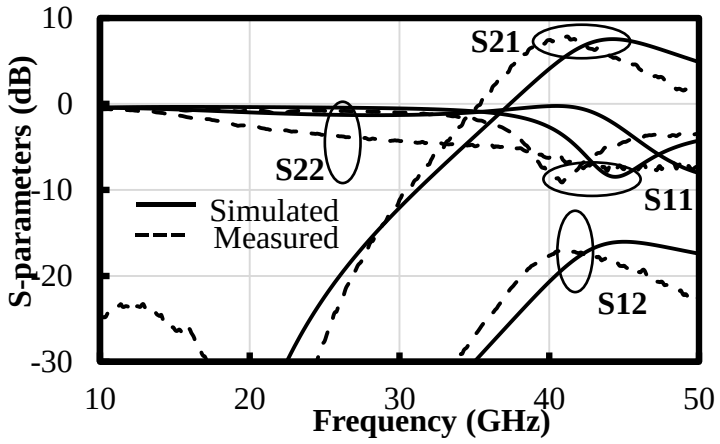


Figure 2.15. Measured and simulated S-parameters of the power amplifier biased in class AB mode.

Figure 2.16 plots the measured PAE, P_{out} and gain as a function of input power at 42.5GHz. The gain plot indicates that the PA is biased in class-AB operation with a peak gain of 9.5dB. This choice of biasing leads to a 1dB gain expansion before entering gain compression and results in the best PAE, while keeping the PA linear and maintaining high P_{sat}. The PA achieves 34.4% peak PAE at 18.2dBm output power and P_{sat} of 18.6dBm with P_{-1dB} of 17.5dBm measured at 42.5GHz. The DC power consumption is 178mW from a 2.7V supply. No degradation was observed during laboratory testing of the amplifier.

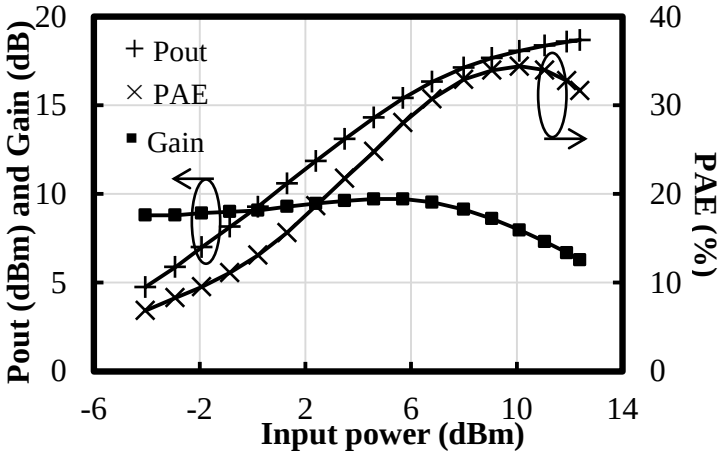


Figure 2.16. Measured output power, gain and PAE as a function of input power at 42.5GHz biased in class AB mode.

Figure 2.17 plots the measured peak PAE and P_{sat} of the PA from 41GHz to 45GHz. The PAE remains higher than 30% and P_{sat} remains higher than 17.5dBm from 42GHz to 45GHz.

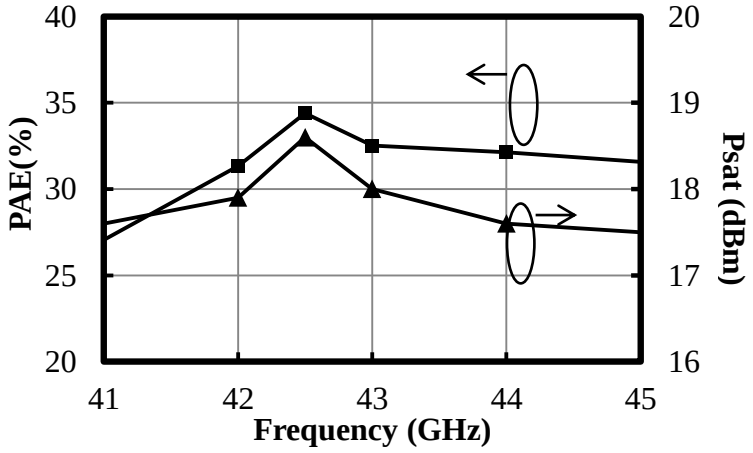


Figure 2.17. Measured peak PAE and Psat as a function of frequency.

To verify the uniformity and consistency of the results, four different chips were measured with two different measurement setups; large signal calibration was

separately conducted for each chip to de-embed the cable and probe losses. Figure 2.18 shows the measured PAE as a function of output power of these chips measured at 42.5GHz. The peak PAE and P_{sat} varies between 32% and 34% and 19.4dBm and 18.6dBm, respectively. These small variations demonstrate that the measurements are repeatable and consistent across multiple devices.

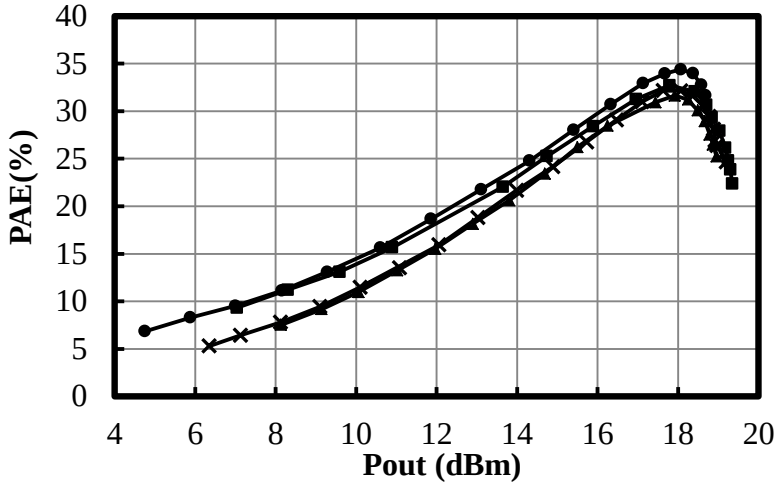


Figure 2.18. Measured PAE as a function of output power for four chips.

Table 2.1 summarizes the measured performance and compares the results with recently published PAs. Comparable silicon CMOS PAs [7-9] operate in the 60GHz band, and have Psat between 9.9dBm and 17dBm and PAE ranging between 8% and 14%. Reference [19] is a three-stack FET PA, which is also implemented in 45nm SOI CMOS with P_{sat} of 19dBm. This PA can only achieve 22% peak PAE and 7.4dB gain. Reference [17] is a BiCMOS PA, which has P_{sat} of 20dBm and PAE of 20%. The peak PAE in this work is 34%.

Table 2.1. Comparison to previous work.

Technology	**45nm SOI CMOS**	45nm SOI CMOS	130nm BiCMOS	65nm SOI CMOS	90nm CMOS	65nm CMOS	GaAs PHEMT
References	**This Work**	[19]	[17]	[27]	[28]	[29]	[30]
Freq (GHz)	**45**	45	60	60	60	65	40
Supply (V)	**2.7**	4	1.8	1.8	1.2	1	6
Psat (dBm)	**18.6-19.4**	19	20.5	14.5	12.5	17.9	27
Peak PAE (%)	**32-33.9**	22	19.4	25.7	19.3	11.7	26.6
Gain (dB)	**9.5**	7.4	20.5	16	15	19.2	16
Area (mm^2)	**0.3**	0.25	0.72	0.57	0.15	0.825	3.48

II.E.II. 45GHz Two-Stage PA

Figure 2.19 is a chip photomicrograph of the two-stage 45GHz PA fabricated in a 45-nm SOI CMOS process. The area of the PA is 0.37 mm^2 including the pads. The simulated and measured S-parameters are compared in Figure 2.20. The small-signal gain peaks at 15.5 dB at 43 GHz.

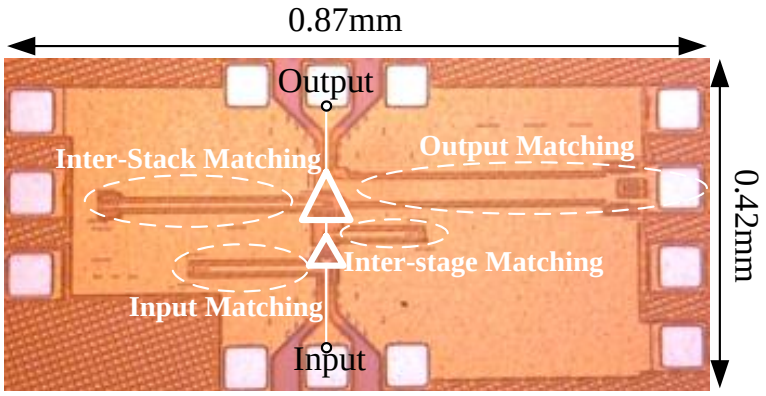


Figure 2.19. Photomicrograph of two-stack PA.

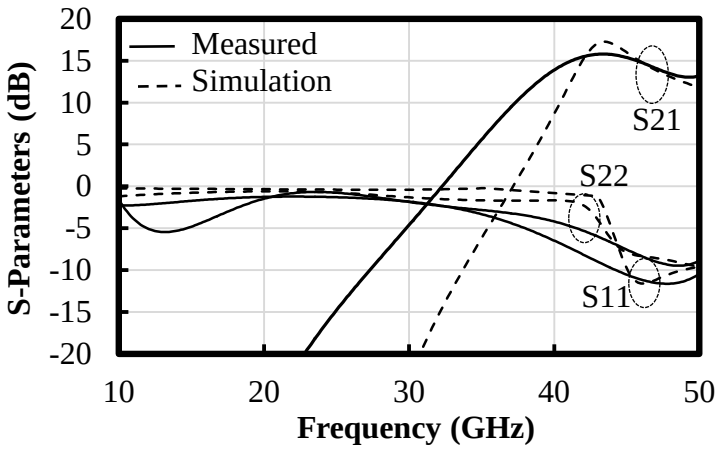


Figure 2.20. Measured and simulated S-parameters of the power amplifier biased in class AB mode.

Figure 2.21 plots the measured and simulated PAE, DE and gain as a function of output power at 44 GHz. The peak PAE is 31% and the peak power is 18 dBm.

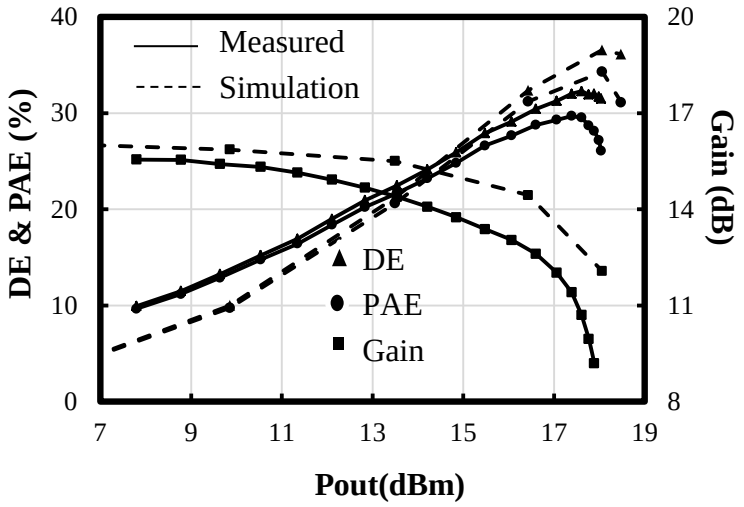


Figure 2.21. Measured and simulated DE and PAE as a function of output power at 44 GHz.

Figure 2.22 shows the peak PAE and Psat as a function of frequency. The implemented PA shows more than 21% peak PAE and 17.5dBm saturated output power from 41 to 47 GHz. This graph confirms the S-parameter measurements, which also indicated the maximum gain at 44GHz.

This PA has been measured at 1dB compression point for 2 hours and no degradation has been observed during this measurement.

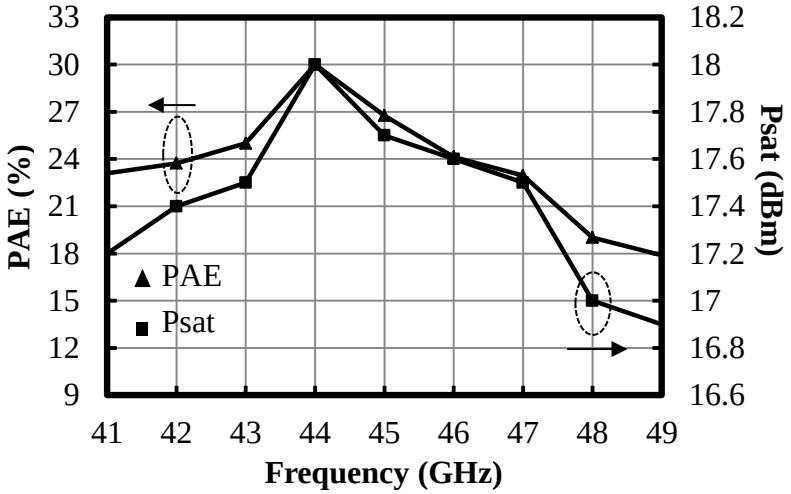


Figure 2.22. Measured peak PAE and Psat as a function of frequency.

Figure2.23 shows the effect of increasing power supply of the CS amplifier from 1.1 V to 1.4 V on the power gain as a function of output power at 44 GHz. This measurement indicates that the CS amplifier with 1.2 V power supply is delivering enough power to the two-stack PA to saturate its output power.

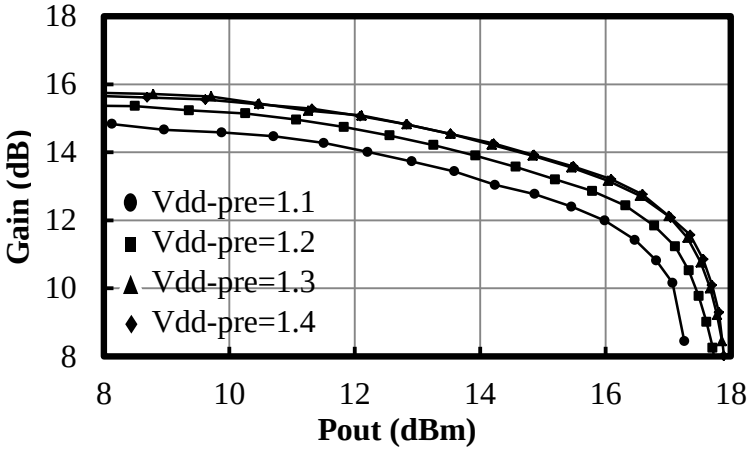


Figure 2.23. Effect of increasing the power supply voltage of the preamplifier on gain as a function of output power.

This two-stage PA has 7dB higher gain than the single-stage two-stack PA designed in Section II.D.I at the expense of 2% lower PAE. The lower Psat of this PA is due to the choice of lower Vdd for more reliable operation.

II.E.III. 90GHz Two-Stack PA

Figure 2.24 is a chip photomicrograph of the two-stage 90GHz PA fabricated in a 45-nm SOI CMOS process. The area of the PA is 0.37 mm^2 including the pads. The measured S-parameters of the narrowband and wideband PAs are shown in Figure 2.25. This measurement indicates that the peak gain of the wideband PA is reduced to 9 dB, lower than 10.2 dB peak gain of the tuned PA achieved at 89 GHz.

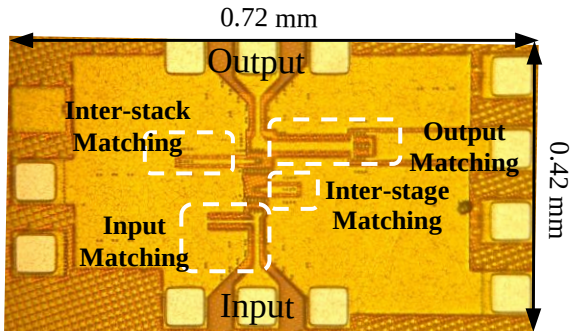


Figure 2.24. Photomicrograph of two-stage PA.

Figure 2.26 plots the measured PAE, DE and gain as a function of output power at 89 GHz for the narrowband PA. The peak PAE is 11% and the saturated output power is 15.8 dBm. No degradation was observed during the laboratory testing of this amplifier.

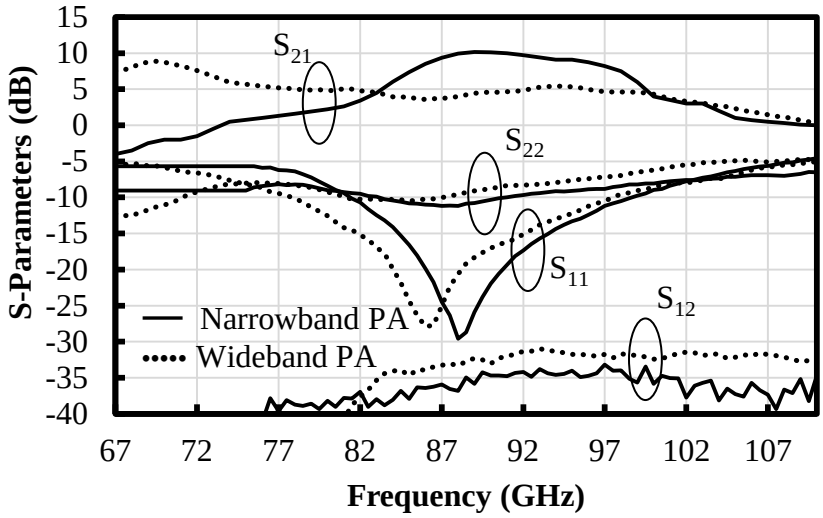


Figure 2.25. Measured S-parameters of the narrowband and wideband power amplifiers.

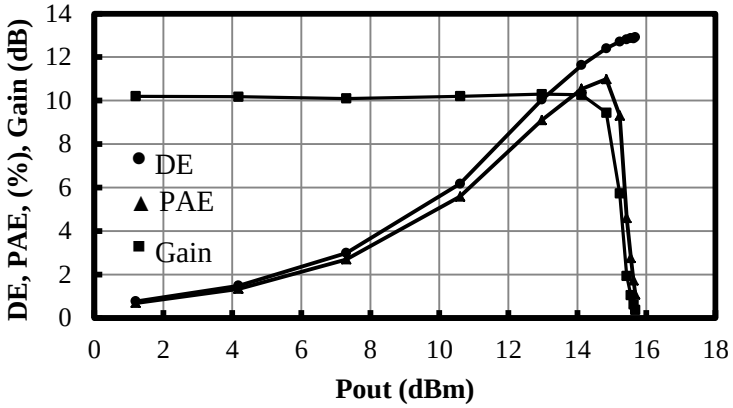


Figure 2.26. Measured DE and PAE as a function of output power at 89 GHz of narrowband (Figure 2.13(a)) amplifier.

Figure 2.27 shows the measured peak PAE and Psat as a function of frequency for the narrowband PA. This PA shows more than 8% peak PAE and 14 dBm saturated output power from 86 to 94 GHz.

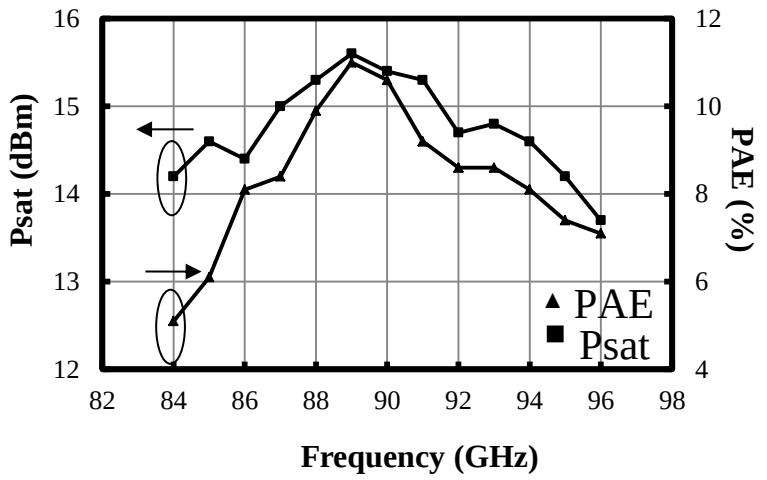


Figure 2.27. Measured peak PAE and Psat of narrowband (Figure 2.13(a)) amplifier.

The measured peak output power and PAE of the wideband PA are shown in Figure 2.28 as a function of frequency. These measurements indicate that the wideband PA achieves more than 14 dBm saturated output power over a 26 GHz bandwidth.

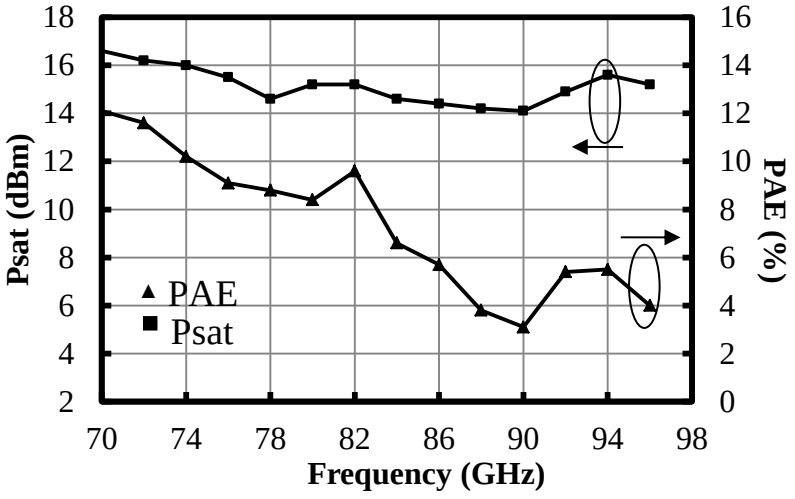


Figure 2.28. Measured peak PAE, Psat and gain of wideband (Figure 2.13(b)) amplifier.

Table 2.2 is a comparison of the previous CMOS work at W-band frequency regime. This work achieves 15.8 dBm saturated output power at 90 GHz, which is one of the highest among the PAs operating above 80 GHz. This design only occupies 0.05 mm^2 excluding the pads. This demonstrates the clear advantage of the FET stacking technique. This design also demonstrates 11% PAE, which is the highest of the CMOS PAs operating at its frequency of operation.

Table 2.2. Comparison to previous work.

Ref.	**This Work**	[3]	[31]	[32]	[33]
Technology	**45nm SOI CMOS**	65nm CMOS	65nm CMOS	65nm CMOS	45nm SOI CMOS
Frequency [GHz]	**86-94**	79	101-107	79-106	80
Psat [dBm]	**15.8**	19.3	14.8	14.8	12.4
PAE [%]	**11**	19.2	9.4	8.7	14.2
Gain [dB]	**10.2**	24.2	14.1	12	11
Area*[mm^2]	**0.05**	0.855	0.106	<0.28	0.18

*Area excluding the pads

II.F. Conclusion

The stacked-FET PA is analyzed and the optimum value of circuit parameters for the best efficiency is calculated and it is shown that the use of inter-stack matching network is more important for operating frequency closer to the f_t of the device.

A 45GHz two-stack PA is demonstrated in 45nm SOI CMOS technology. A stacking technique avoids the breakdown of the FETs, while allowing a power supply of 2.7V. A shunt inter-stage matching network is used, and is shown to improve PAE

by more than 6%. This PA occupies 0.3mm^2 and it achieves saturated output power ranging from 18.6 to 19.4dBm with 32-34% peak PAE at 42.5GHz. The amplifier has a peak gain of 9.6dB and it achieves more than 30% PAE from 42 to 45GHz.

To improve the gain of the designed PA, a 45-GHz two-stage PA is also demonstrated in 45-nm SOI CMOS technology. The first stage is a common-source amplifier operating from a 1.2-V supply and the second stage is a two-stack amplifier with a 2.5V supply. This combination provides high gain and high output power with high efficiency. This PA occupies 0.35 mm^2 and it achieves more than 18.1dBm saturated output power with 30% peak PAE at 44 GHz. The amplifier has a peak gain of 16 dB and it achieves more than 21% PAE from 41 to 47GHz.

A 90GHz two-stage PA is also demonstrated in 45nm SOI CMOS technology. The first stage is a common-source amplifier operating from a 1.4V supply and the second stage is a two-stack amplifier with a 2.8V supply. This PA occupies 0.05 mm^2 excluding the pads and it achieves 15.8dBm saturated output power with 11% peak PAE at 89 GHz. The amplifier has a peak gain of 10.3 dB and it achieves more than 8% PAE from 86 to 94GHz. These results, for the first time indicates that CMOS technology is becoming a realistic alternative for III-V technologies in some of the high-power millimeter-wave application.

Chapter 2, in part, is a reprint of the material as it appears in "An 11% PAE, 15.8-dBm Two-Stage 90-GHz Stacked-FET Power Amplifier in 45-nm SOI CMOS," *IEEE Microwave Theory and Techniques* July 2013, and "A 45GHz Doherty Power Amplifier with 23% PAE and 18dBm Output Power, in 45nm SOI CMOS," *IEEE Radio Frequency Integrated Circuit Symposium,* July. The authors are Amir Agah,

Jefy Jayamon, Hayg Dabag, Bassel Hanafi, Peter Asbeck, James Buckwalter and Lawrence Larson. The authors are .author of this dissertation is the primary author and investigator of both papers.

III

Design and Analysis of Multi-Drive Stacked-FET Power Amplifiers

III.A. Introduction

Highly-scaled silicon processes have expanded the application of CMOS to millimeter-wave bands. However, the low breakdown voltage of highly-scaled FETs continues to plague the realization of high-power, high-frequency power amplifiers.

To overcome the power limitations at high frequencies relative to the f_t /f_{MAX} of the device, power combining techniques have been developed to combine the power from multiple stages. However, the low quality factor of passive components fabricated on silicon processes introduces high losses in the power distribution and combining networks. Additionally, these networks require a relatively large circuit area [23-25]. The output power from a single power amplifier (PA) generally falls as the frequency of operation increases, resulting in a larger number of PAs required for a given output power. Scaling the power distribution network for a large numbers of

PAs results in diminishing returns, after which it becomes difficult to yield any further improvements in output power.

An alternative to passive power combining is the FET-stacking circuit technique [35-39],[23-24],[18-19], which solves two significant problems. First, FETs can be stacked to support higher supply voltages and a higher RF voltage swing at the output. Millimeter-wave stacked-FET PAs have demonstrated record efficiency and output power, two-stack [23], three stack [36] and differential three-stack PAs [37] achieved 18.6 dBm, 21 dBm, and 23 dBm output power with 34%, 27% and 25% PAE respectively at 45 GHz. Second, the stacked-FET approach also increases the loadline impedance for each additional FET, allowing lower loss impedance matching at the output.

The fundamentals of stacked-FET PA design have been discussed in detail in the previous chapter. In this chapter, we analyze the loss mechanisms in the stacked-FET PA circuit to develop the fundamental bounds on PAE and output power. The gate resistance of the stacked-FET PA is demonstrated to be a dominant source of loss at high frequency.

III.B. Analysis and Limitations of Stacked FET Power Amplifiers

Nanometer scale CMOS FETs traditionally suffer from low breakdown voltage. To overcome this limitation, a FET-stacking technique, as shown in Figure 3.1, is often utilized to achieve high output voltages without sacrificing reliability [35-39]. For reliable operation of the FETs in the stacked architecture, the peak V_{dg}

and V_{ds} of each device should be kept below a certain breakdown voltage and should be equal for each device for reliable operation, i.e.

$$|V_{ds,1}| = |V_{ds,2}| = \cdots = |V_{ds,n}| \tag{3.1}$$

where n is the number of FETs in the stack. The maximum reliable drain-to-source voltage BV_{ds}, is determined by the drain-source breakdown voltage [40]. Preliminary reliability measurements indicates that this voltage is approximately 2.5V for both V_{ds} and V_{dg} for a device with 45-nm length [36],[23],[24].

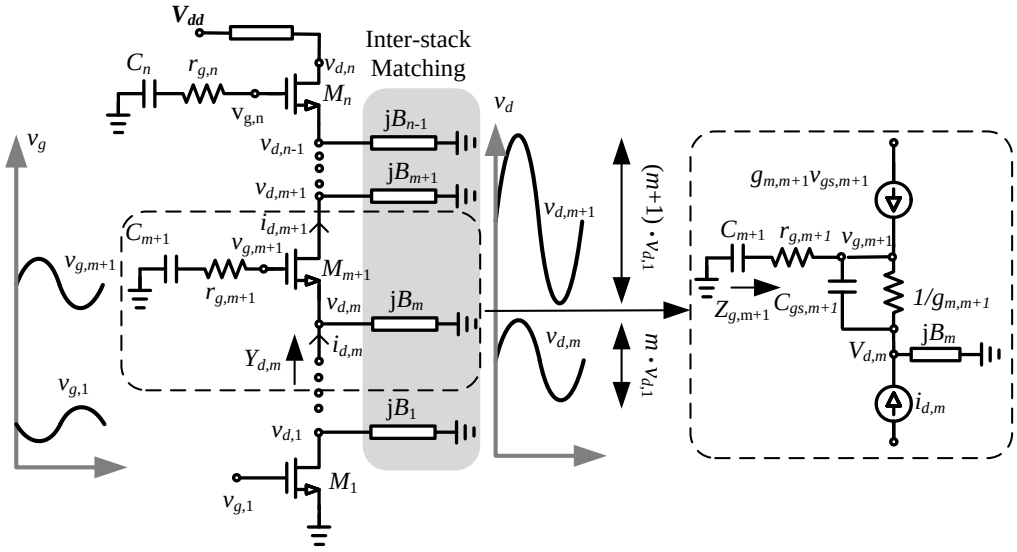


Figure 3.1. Schematic of an n-stack PA.

According to [5] the optimum load conductance for a PA, resulting in the best efficiency and output power is $G_{opt}= i_{sw}/v_{sw}$, where i_{sw} and v_{sw} are the maximum ac current amplitude and peak voltage at the output of the PA. Assuming that the voltage swing is distributed equally among all the FETs in the stack according to (3.1), the optimum admittance required at the m^{th} stage of the stacked-FET PA is real and equal to

$$G_{opt,m} = \frac{i_{sw}}{v_{sw}} = \frac{i_{sw-FET}\prod_{k=2}^{m}|\alpha_k|}{m v_{sw-FET}} = \frac{\prod_{k=2}^{m}|\alpha_k|}{m} G_{opt-FET}. \quad (3.2)$$

where $G_{opt\text{-}FET}$, $i_{sw\text{-}FET}$ and $v_{sw\text{-}FET}$ are the optimum load conductance, maximum FET ac current and ac voltage and α_m is the current gain between two consecutive FETs in the stack defined as

$$\alpha_m = \frac{i_{d,m}}{i_{d,m-1}}. \quad (3.3)$$

In previous work on stacked-FET PAs, the effect of gate resistance and limited quality factor of the passive components has not been considered [36], but these effects may be more important at high frequencies by reducing the current gain.

Ignoring the C_{dg} and r_{ds} of the FETs, it can be shown from Figure3.1 that

$$\alpha_{m+1} = \frac{j\omega C_{p,m+1}\omega_{t,m+1}}{-\omega^2 C_{p,m+1} - \omega B_m(\omega) + j\omega C_{p,m+1}\left(\omega_{t,m+1} - \omega B_m(\omega) r_{g,m+1}\right)}, \quad (3.4)$$

where $B_m(\omega)$ is the susceptance of the inter-stack matching network in Figure 3.1 [36-37],[31], ω_t is the unity current gain frequency of the FET, and $C_{p,m}$ is the series combination of the gate-source ($C_{gs,m}$) and external gate capacitance (C_m), i. e.

$$C_{p,m} = \frac{C_m C_{gs,m}}{C_m + C_{gs,m}}. \quad (3.5)$$

Therefore, the magnitude and the phase of the current gain is

$$|\alpha_{m+1}| = \frac{1}{\sqrt{\left(1 - \frac{\omega}{\omega_{t,m+1}} B_m(\omega) r_{g,m+1}\right)^2 + \left(\frac{\omega}{\omega_{t,m+1}}\right)^2 \left(1 + \frac{B_m(\omega)}{\omega C_{p,m+1}}\right)^2}} \quad (3.6)$$

$$\angle(\alpha_{m+1}) = tan^{-1}\left(\frac{1 + \frac{B_m(\omega)}{\omega C_{p,m+1}}}{\frac{\omega_{t,m+1}}{\omega} - B_m(\omega) r_{g,m+1}}\right). \quad (3.7)$$

Using the small-signal model in Figure 3.1, it can be shown that the admittance at the drain of transistor M_m , looking toward the source of M_{m+1}, is $Y_{d,m}=G_{d,m}+jB_{d,m}$, where $G_{d,m}$ and $B_{d,m}$ are

$$G_{d,m} = \frac{C_{p,m+1}^2 r_{g,m+1}^2 \omega^2 + C_{p,m+1} r_{g,m+1} \omega_{t,m+1}}{r_{g,m+1}\left(1 + C_{p,m+1}^2 r_{g,m+1}^2 \omega^2\right)} \tag{3.8}$$

$$B_{d,m} = \frac{r_{g,m+1}\omega C_{p,m+1} - \omega\omega_{t,m+1} C_{p,m+1}^2 r_{g,m+1}^2}{r_{g,m+1}\left(1 + C_{p,m+1}^2 r_{g,m+1}^2 \omega^2\right)} + B_m(\omega). \tag{3.9}$$

From (3.2), the highest efficiency and output power is achieved, when

$$Y_{d,m}(\omega) = G_{opt,m} \ . \tag{3.10}$$

In a stacked-FET PA, (10) can be satisfied only if

$$B_{d,m}(\omega) = 0 \quad . \tag{3.11}$$

In the case of r_g=0, (3.11) can be achieved if $B_m(\omega)$= -$\omega C_{p,m+1}$ and therefore, using (3.6) and (3.7) $|\alpha_{m+1}|$=1 and $\angle\alpha_m$ = 0 . Considering (3.11) and $\angle\alpha_m$ = 0, when r_g=0, the current through the FETs is minimum and almost zero, when V_{ds} reaches its maximum value, minimizing hot-carrier injection, which is a major cause of performance degradation in power amplifiers [25-26]. Furthermore, when r_g=0, $G_{d,m}=g_{m,m+1}(C_{m+1}/(C_{gs,m+1}+C_{m+1})=G_{opt\text{-}m}$, which is in agreement with previous stacked-FET PA analysis [35][37].

When r_g is not zero, (3.11) can only be satisfied if

$$B_m(\omega) = -\frac{r_{g,m+1}\omega C_{p,m+1} - \omega\omega_{t,m+1} C_{p,m+1}^2 r_{g,m+1}^2}{r_{g,m+1}\left(1 + C_{p,m+1}^2 r_{g,m+1}^2 \omega^2\right)}. \tag{3.12}$$

Ignoring the C_{dg} of the FET, we define a quality factor of the gate network to be

$$Q_m = \frac{1}{r_{g,m}\omega C_{p,m}}. \tag{3.13}$$

From (3.12), (3.6) and (3.7) and assuming that $Q_{m+1} >> 1$ and $f \approx f_T$ it can be shown that

$|\alpha_{m+1}| \cong$

$$\frac{g_{m,m+1}\left(C_{m+1} + C_{gs,m+1}\right)}{g_{m,m+1}\left(C_{m+1} + C_{gs,m+1}\right) + r_{g,m+1}\omega^2 C_{m+1} C_{gs,m+1}^2} = \frac{Q_{m+1}}{Q_{m+1} + \frac{\omega}{\omega_{t,m+1}}} \tag{3.14}$$

$$\angle(\alpha_{m+1}) \cong 0. \tag{3.15}$$

Figure 3.2 plots $|\alpha_{m+1}|$ as a function of Q_{m+1} at 20, 60 and 100GHz for a device with unity current gain frequency of approximately 190GHz. It is apparent in these plots that the current gain is reduced substantially at high frequency, limiting the number of devices that can be stacked and the output power.

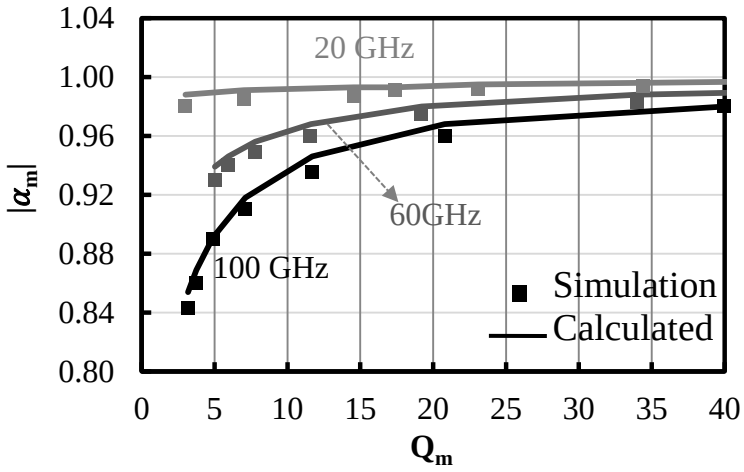


Figure 3.2. Simulated and calculated $|\alpha|$ as a function of Q_i at 20, 60 and 100GHz.

Using (3.14), along with (3.9) and (3.2), the required C_{m+1} at each stage of the stacked-FET PA to satisfy (3.1) is

$$(C_{m+1})^{-1} \approx \frac{\omega_{t,m+1} + \sqrt{{\omega_{t,m+1}}^2 + 4\omega^2 r_{g,m+1} G_{opt,m}\left(1 - r_{g,m+1} G_{opt,m}\right)}}{2G_{opt,m}} - \left(C_{gs,m+1}\right)^{-1} \quad (3.16)$$

If r_g=0, $C_{m+1} = (g_{m,m+1}/G_{opt,m} - 1)^{-1}\ C_{gs,m+1}$, which is consistent with previous stacked-FET PA analysis [35],[37]. Using (3.16), $|\alpha_m|$ in (3.14) can also be rewritten as

$$|\alpha_{m+1}| \cong \frac{1 + \sqrt{1 + 4\left(\frac{\omega}{\omega_{t,m+1}}\right)^2 r_{g,m+1} G_{opt,m}\left(1 - r_{g,m+1} G_{opt,m}\right)}}{1 + \sqrt{1 + 4\left(\frac{\omega}{\omega_{t,m+1}}\right)^2 r_{g,m+1} G_{opt,m}\left(1 - r_{g,m+1} G_{opt,m}\right)} + 2G_{opt,m}\left(\frac{\omega}{\omega_{t,m+1}}\right)^2 r_{g,m+1}} \quad (3.17)$$

Assuming that gate capacitance (C_m) at each stage of the stacked-FET PA is optimized using (3.16) and $B_m(\omega)$ is optimized according to (3.12), the drain efficiency (*DE*), output power (P_{out}), and power-added efficiency (*PAE*) of the *n*-stack PA with identical devices in the stack are

$$DE_{n-stack} \cong DE_{FET} \prod_{m=2}^{n} |\alpha_m| \quad (3.18)$$

$$P_{out,n-stack} = n\, P_{out,FET} \prod_{m=2}^{n} |\alpha_m| \quad (3.19)$$

$$PAE_{n-stack} = \frac{n\,P_{out,FET}\prod_2^n|\alpha_m| - P_{in}}{nP_{DC-FET}} = DE_{FET}\left(\prod_2^n|\alpha_m| - \frac{1}{nG_{FET}}\right) \cong DE_{FET} \quad (3.20)$$

where $P_{out,FET,}$ $DE_{FET,}$ $P_{DC\text{-}FET}$ and G_{FET} are the output power, drain efficiency, power consumption, and gain of a single common-source FET. Figures 3.3, 3.4, and 3.5 show the calculated normalized *DE*, *Pout* and *PAE* of an *n*-stack PA for a 256μm×40nm device at 20, 60 and 100GHz, showing a good agreement between circuit simulation and calculated results. These graphs indicate that stacking more FETs at low frequency increases the output power linearly without any efficiency reduction. But as the frequency increases, the marginal increase in output power from adding FETs decreases, resulting in decreasing efficiency, demonstrating a fundamental limitation of the stacking technique.

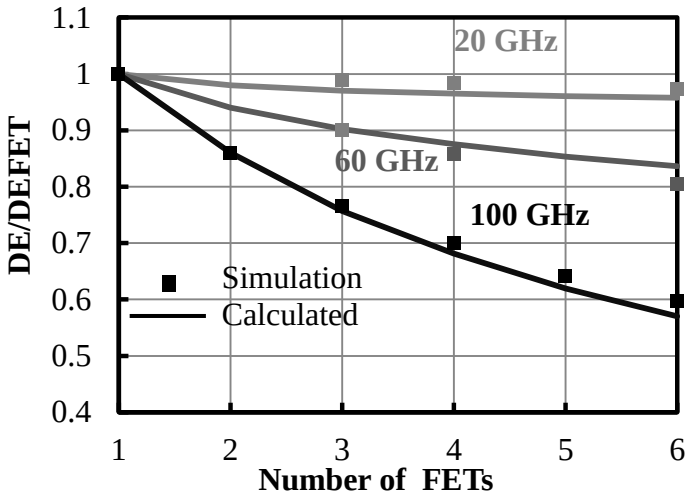


Figure 3.3. Normalized *DE* of stacked-FET PA at different frequencies as a function of number of FETs with W=256μm.

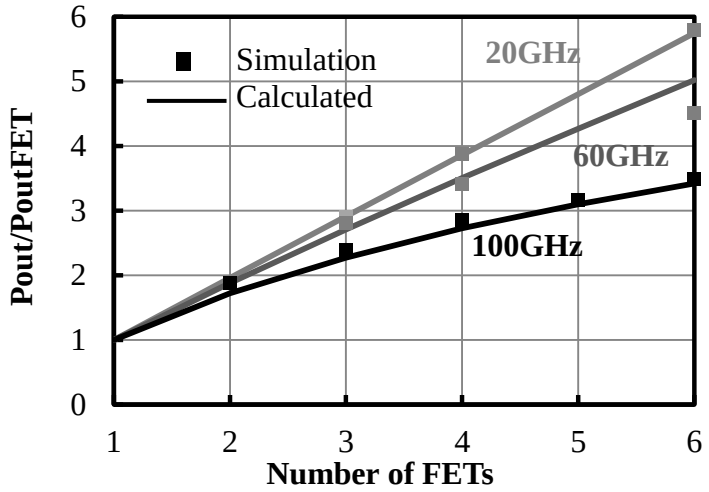


Figure 3.4. Normalized Pout of stacked-FET at different frequencies as a function of number of FETs with W=256μm.

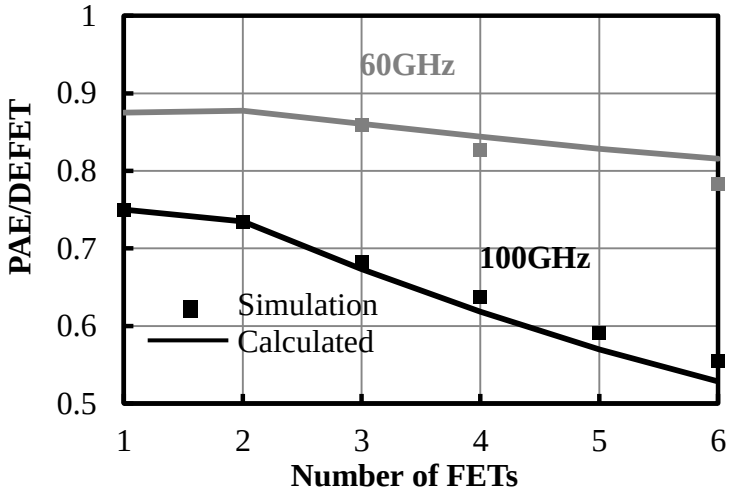


Figure 3.5. Normalized PAE of stacked-FET PA at different frequencies as a function of number of FETs with W=256μm.

III.C. Analysis of Multi-Drive Stacked FET PA

Section III.B demonstrated that the output current in a stacked-FET PA decreases with increasing *n* at high frequency, resulting in lower efficiency and lower

output power improvement. To address this problem, a multi-drive stacked-FET PA is proposed, where the current lost in each stage of the stack is recovered by driving each gate separately. A schematic of the improved approach is shown in Figure 3.6.

To achieve the best performance in the new multi-drive stacked-FET PA, we assume that all the devices should deliver the same current, i.e.

$$i_{d,m+1} = \left|i_{d,m}\right| e^{j\varphi_{m+1}} \tag{3.21}$$

where φ_{m+1} is the phase difference between $i_{d,m}$ and $i_{d,m+1}$.

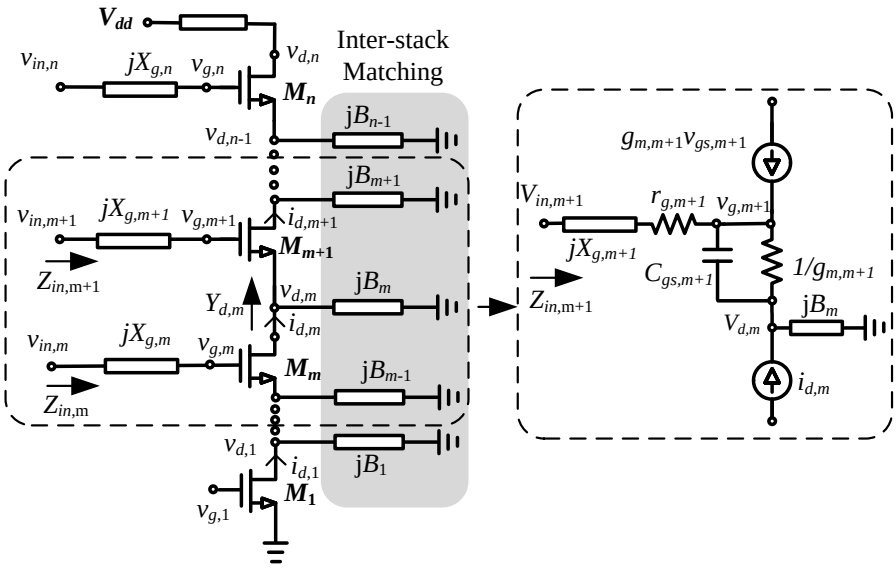


Figure 3.6. Schematic of multi-drive stacked-FET PA.

As explained in the previous section, the optimum load admittance at the m^{th} stage of the stacked-FET PA is equal to $G_{opt,m}$, as shown in (3.2). Assuming (3.21), $|\alpha|$ is unity in multi-drive stacked-FET PAs and (3.2) can be rewritten for multi-drive stacked-FET PA such that

$$G_{opt,m} = \frac{G_{opt,FET}}{m} \tag{3.22}$$

Ignoring the C_{dg} and r_{ds} of the FETs, the small-signal model of the m^{th} stage in the multi-drive stacked-FET PA is shown in Figure 3.6. Assuming (3.21) and (3.22), there are two possible solutions for φ_{m+1}.

$$\varphi_{m+1} = 0\,, \tag{3.23a}$$

$$\varphi_{m+1} = \sin^{-1}\left(\frac{-2\dfrac{\omega}{\omega_{t,m+1}}}{1+\left(\dfrac{\omega}{\omega_{t,m+1}}\right)^2}\right). \tag{3.23b}$$

If (3.23b) is selected, the real part of real part of the impedance seen at the gate input of each stage in the stack (Re[$Z_{in,m+1}$]) is

$$Real\left[Z_{in,m+1}\right] = r_{g,m+1} - \frac{2mR_{opt-FET}}{1+\left(\dfrac{\omega}{\omega_{t,m+1}}\right)^2}\,, \tag{3.24}$$

which is negative in most cases, resulting in potential instability. Therefore, the acceptable solution for φ_{m+1} is zero as shown in (3.23a). Therefore,

$$i_{d,m+1} = i_{d,m}. \tag{3.25}$$

Using the small-signal model of Figure 3.6 and considering that φ_{m+1}=0, the required inter-stack matching network is

$$B_m(\omega) = \frac{-\omega}{mR_{opt-FET}\omega_{t,m+1}}. \tag{3.26}$$

and the input impedance of each stage in the stack ($Z_{in,m+1}$) is

$$Z_{in,m+1} = r_{g,m+1} + jX_{g,m+1} + \frac{1}{sC_{gs,m+1}}\left(1 - mR_{opt-FET}g_{m,m+1}\right), \tag{3.27}$$

where $X_{g,m+1}$ is the reactance of the gate network. If $X_{g,m+1}$ is designed such that

$$jX_{g,m+1} = \frac{1}{sC_{gs,m+1}}\left(mR_{opt-FET}g_{m,m+1} - 1\right). \tag{3.28}$$

Then the input impedance of each FET in the stack becomes purely real and is equal to

$$Z_{in,m+1} = r_{g,m+1}\,, \tag{3.29}$$

which is independent of frequency and is identical for all the FETs in the stack, assuming identical devices.

From the small-signal model of Figure 3.6, the voltage required to drive the gate of the m+1th stage of the PA is

$$v_{in,m+1} = -i_{d,m}\frac{sC_{gs,m+1}r_{g,m+1}}{g_{m,m+1}}. \tag{3.30}$$

Considering (3.29) and (3.30), the required power to drive the gate of the m+1th FET in the multi-drive stacked-FET PA is

$$P_{in,m+1} = 0.5\left(\left|i_{d,m+1}\right|\frac{\omega}{\omega_{t,m+1}}\right)^2 r_{g,m+1}, \tag{3.31}$$

which is identical for all the FETs in the stack, assuming identical devices.

Now that the driving requirements have been determined for the gate driver, the power and efficiency of this approach can be examined. Assuming (3.25), (3.26) and (3.28), the drain efficiency (*DE*) and output power (P_{out}) of an *n*-stack multi-drive stacked-FET PA for a given bias current with identical devices is improved to

$$DE_{n-stack} = DE_{FET} \tag{3.32}$$

$$P_{out,n-MDSFET} = n\,P_{out,FET} \tag{3.33}$$

Figures 3.7 and 3.8 shows the calculated drain efficiency and output power of an *n*-stack multi-drive stacked-FET PA using (3.32) and (3.33) compared with simulation results using 256μm×40nm devices at 100 GHz. These figures also include

analysis and simulation results for the conventional stacked-FET PA. Unlike the traditional stacked-FET PA, the output power of the multi-drive stacked-FET PA increases linearly with the number of FETs in the stack, while the *DE* remains unchanged.

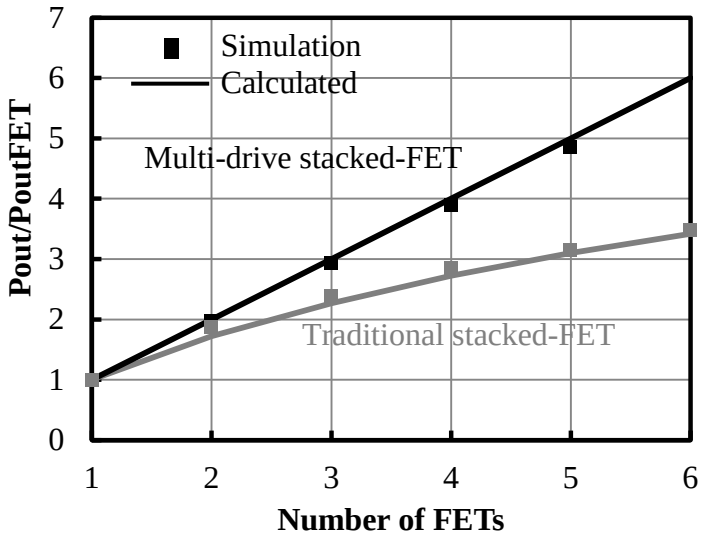


Figure 3.7. Calculated $Pout/Pout_{FET}$ for multi-drive stacked-FET PA and traditional stacked-FET PA at 100GHz with W=256μm.

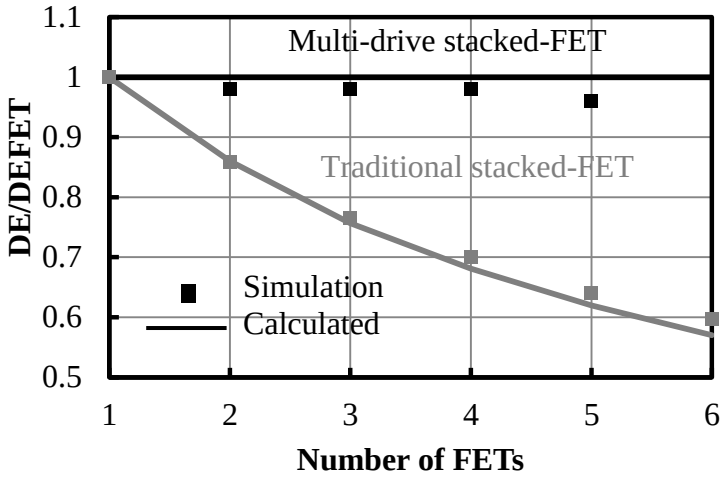


Figure 3.8. Calculated DE/DE_{FET} for multi-drive stacked-FET PA and traditional stacked-FET PA at 100GHz with W=256μm.

As shown in (3.31), the power required to drive each of the stages of the multi-drive stacked-FET PA is identical. Therefore, although the output power increases linearly with number of FETs in the stack as shown in (3.33), the input power also increases linearly, so the power gain of the multi-drive stacked-FET PA remains constant, unlike in conventional stacked-FET PAs. Figure 3.9 compares the simulated and calculated power gain of a multi-drive stacked-FET PA with a traditional stacked-FET PA using 256μm devices.

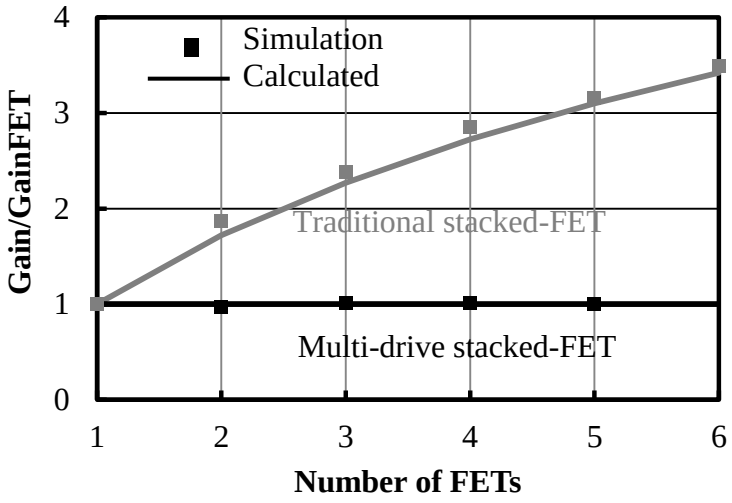


Figure 3.9. Calculated and simulated $Gain/Gain_{FET}$ for multi-drive stacked-FET PA and traditional stacked-FET PA at 100GHz with W=256μm.

Considering (3.33) (3.34) and (3.35), the PAE of a multi-drive stacked-FET PA is

$$PAE_{n-MD} = \frac{P_{out,n-MDSFET} - \left(\sum_{m=1}^{n} P_{in,m}\right)}{P_{DC}}$$

$$= \frac{n\,P_{out,FET} - P_{in,1}n}{nP_{DC-FET}} = DE_{FET}\left(1 - \frac{1}{G_{FET}}\right), \qquad (3.34)$$

indicating that the *PAE* of a multi-drive stacked-FET PA is ideally identical to the *PAE* of a single FET with the same dimensions and current. Figure 3.10 shows the simulated and calculated PAE/DE_{FET} of a multi-drive stacked-FET PA and conventional stacked-FET PA as a function of *n* at 100GHz, when G_{FET} is 6dB and W=256μm, indicating that the *PAE* of the multi-drive stacked-FET PA also remains unchanged by increasing the number stages of the stack.

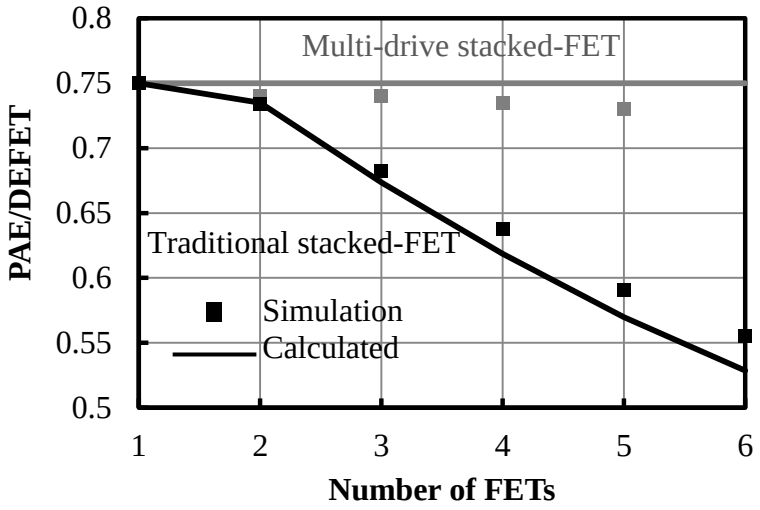


Figure 3.10. Calculated and simulated PAE/PAE_{FET} for multi-drive stacked-FET PA and traditional stacked-FET PA at 100GHz with W=256μm.

These results also imply that the power combining behavior of the multi-drive stacked-FET PA behaves like a traditional lossless power combined PA, showing the advantage of multi-drive approach over a traditional power combining technique, which may suffer from high losses of the passive elements in the power combiner.

III.D. Design of Multi-Drive Stacked FET PAs

As explained in Section II.C, a 256μm×40nm FET test structure is fabricated and used to characterize the device. Figure 3.11 shows the measured and simulated

$Q_{FET}=1/(r_{gate}C_{gs}\omega)$ of the 256μm×40nm FET and a simulated quality factor of a 208fF MIM capacitor ($Q_{c,m}=1/(r_{cap,m}C_m\omega)$, where $r_{cap,m}$ is the series parasitic resistance with the capacitor C_m). The factor $Q_m=1/((r_{gate}+r_{cap,m})\omega C_{p,m})$ introduced in Section III.B, can now be written in terms of Q_{FET} and $Q_{c,m}$, which can be measured. Using the small-signal model of the FET and ignoring the C_{dg}, Q_m is

$$Q_m = \frac{Q_{FET}Q_c(C_{gs}+C_m)}{Q_{FET}C_{gs}+Q_cC_m}. \tag{3.35}$$

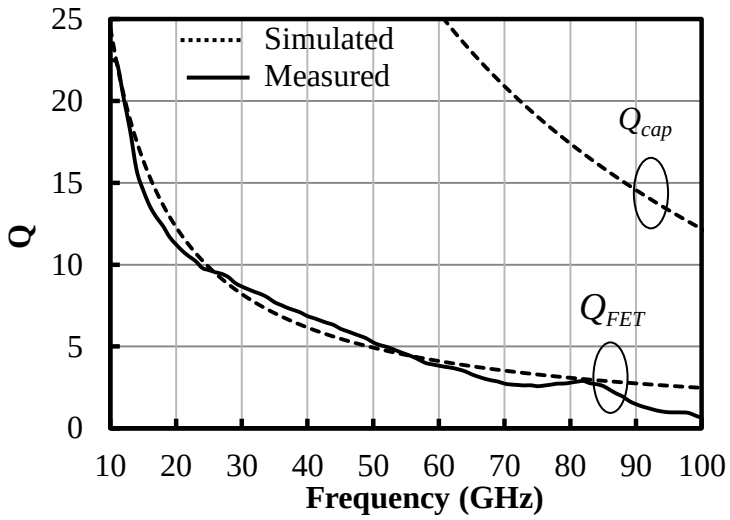


Figure 3.11. Simulated and measured Q of a 256μm NFET and a 208fF MIM capacitor.

Considering (3.35) and Figure 3.11, at lower stages of the stacked-FET PA, where C_m is comparable in size to C_{gs} and $Q_m \approx Q_{FET}$, there is approximately 20% loss in the current above 90GHz. However, at higher stages of the stack, where C_m is much smaller than C_{gs} and $Q_m \approx Q_c$, the current loss is negligible. Therefore, there is less need for the multi-drive approach for the devices at the top of the stack. In this work, the multi-drive approach is implemented with drive for only the first and the second FETs of the stacked-FET PA, while the third FET is not driven. Simulation shows

that driving the third gate increases the output power only by approximately 0.5dB, however it reduces the gain by 1.3dB. The schematic of the implemented multi-drive three-stack PA is shown in Figure 3.12.

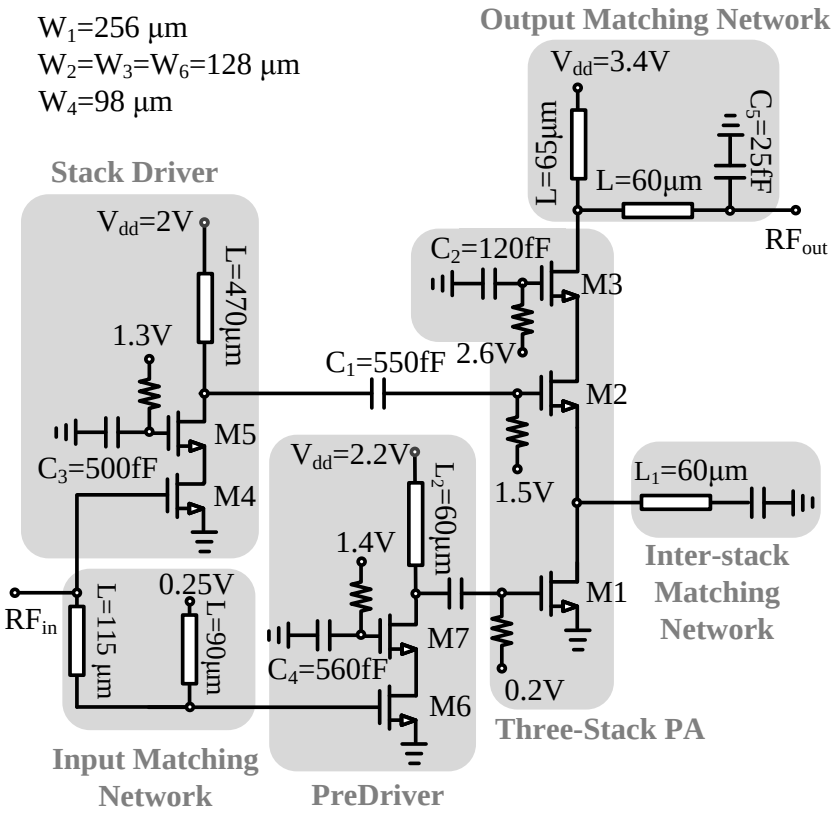


Figure 3.12. Schematic of 90GHz multi-drive stacked-FET PA.

The width of the bottom FET (*M*1) is designed to deliver more than 19dBm output power in a multi-drive three-stacked PA with 3.4V power supply. Considering (3.31), the gain of the multi-drive stacked-FET PA can be maximized by biasing the FETs at the optimum current density for the peak f_t. This can be achieved by increasing the over-drive voltage of *M*1, increasing the DC current. However, simulations show that increasing the gate-source voltage of *M*1 above 0.2V reduces

the peak PAE by pushing the PA toward class-A operation. Instead, the current density and therefore f_t of $M2$ and $M3$ can be increased by reducing their width in comparison to the bottom FET ($M1$), without any efficiency penalty. Simulation indicates that $W_2=W_3=W_1/2=128\mu m$ results in the best PAE.

In [4], the optimum load conductance for a three-stacked PA is 20mS, with width of 256µm, 128µm and 128µm for $M1$, $M2$ and $M3$ respectively, which is identical to the geometries of FETs used in this design. A comparison of (3.2) and (3.22) shows that the optimum load conductance for a multi-drive stacked-FET PA is larger than the conventional stacked-FET PA with identical FET geometries, since $|\alpha|=1$ for a multi-drive stacked-FET PA and $|\alpha|<1$ in the conventional stacked-FET PA. Therefore, the multi-drive three-stacked-FET PA requires an impedance transformation network at the output, which was not required in [4]. This network, shown in Figure 3.12, transforms 50Ω to 32Ω at 90GHz.

III.E. Measurements

The microphotograph of the multi-drive stacked-FET PA fabricated in 45nm SOI CMOS is shown in Figure 3.13 and occupies an area of $0.23mm^2$. For testing purposes, the device is nominally biased in class-A operation.

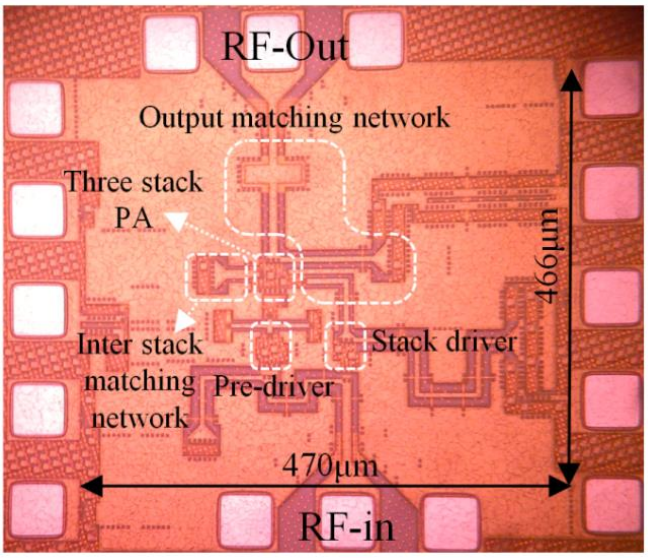


Figure 3.13. Photomicrograph of the multi-drive stacked-FET PA.

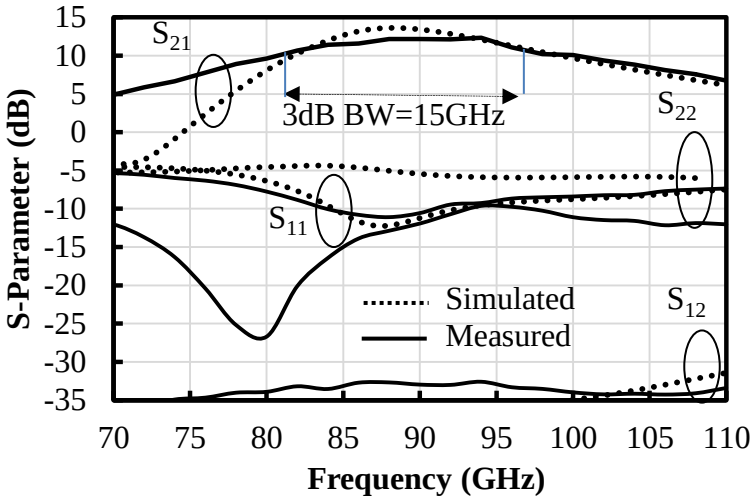


Figure 3.14. Simulated and measured S-parameters of the multi-drive stacked-FET PA.

Figure 3.14 shows the simulated and measured *S*-parameters of the multi-drive stacked-FET PA from 70 to 110 GHz. This PA has a 15GHz 3-dB bandwidth with a peak gain of 13dB achieved at 91GHz. Measurements and simulations indicate that the multi-drive stacked-FET PA is unconditionally stable from 0.001 to 100GHz.

The process of testing was also been conducted at lower frequencies and the measured and simulated S-parameters are plotted in Figure 3.15 showing that the multi-drive stacked FET PA has 10dB peak gain at 40GHz. Both measurement and simulation indicates that this low frequency gain remains unchanged even if the pre-driver is turned off. From this evidence, we concluded that the stacked-FET driver provides a gain mechanism at the lower band. Referring to the schematic of the multi-drive stacked-FET PA shown in Figure 3.12, the inter-stack matching behaves like a degeneration inductance for M2 and stack driver work as a pre-amplifier providing gain at 42 GHz.

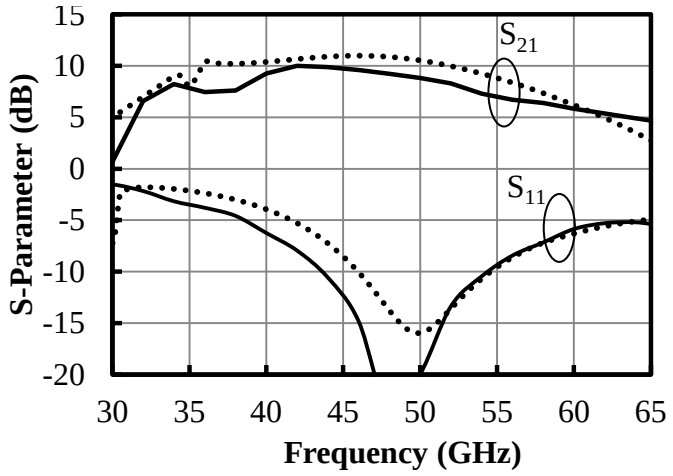


Figure 3.15. Simulated and measured S_{11} and S_{21} of the multi-drive stacked-FET PA from 30 to 65GHz

To examine the stability of the multi-drive stacked-FET PA, the measured and simulated stability factor (K) is plotted in Figure 3.16, showing that the multi-drive stacked-FET PA is unconditionally stable from 0.001 to 100GHz.

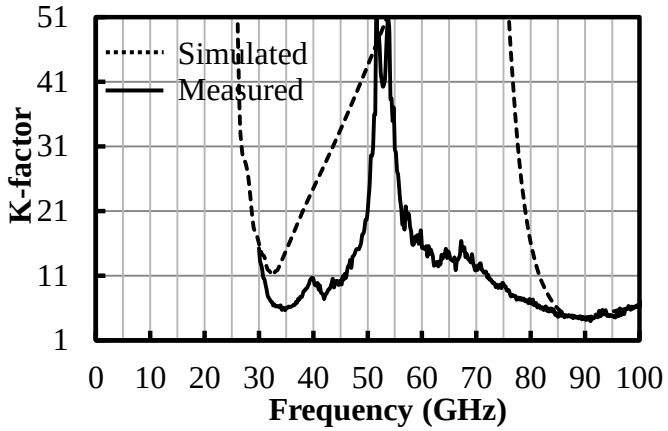


Figure 3.16. Simulated and measured K-factor of the multi-drive stacked-FET PA.

Figure 3.17 shows the simulation and measured *PAE* and gain of the multi-drive stacked-FET PA as a function of output power. This PA can achieve more than 19dBm output power with 14% peak PAE at 90GHz with a 3.4V power supply, which is the highest *Psat* and *PAE* reported above 90GHz for a CMOS PA. To insure the repeatability and consistency of the measurement, a second chip has also been measured and the results are also shown in Figure 3.17. Measurements show that the final stage of the multi-drive stacked-FET PA achieves *DE* of 38% at 90GHz, which is the highest among all previously reported PAs at this frequency range.

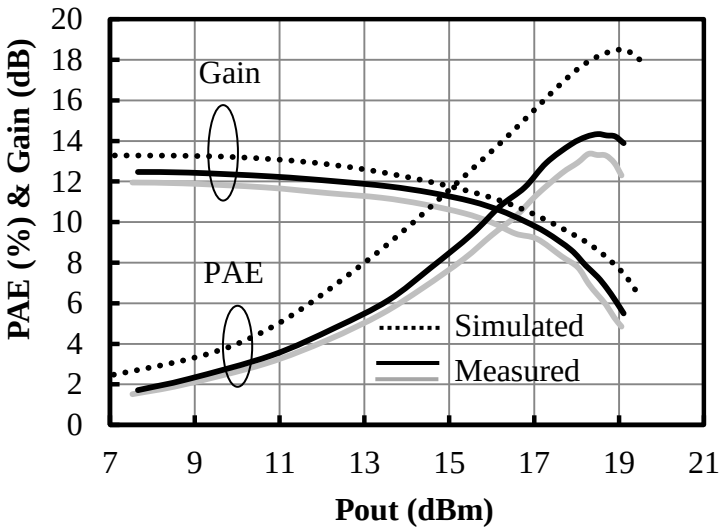


Figure 3.17. Simulated and measured gain and PAE of the multi-drive stacked-FET PA measured at 91GHz for two chips.

Figure 3.18 plots the output power of the multi-drive stacked-FET PA as a function of frequency. This shows that this PA has more than 18dBm saturated output power from 85 to 93GHz.

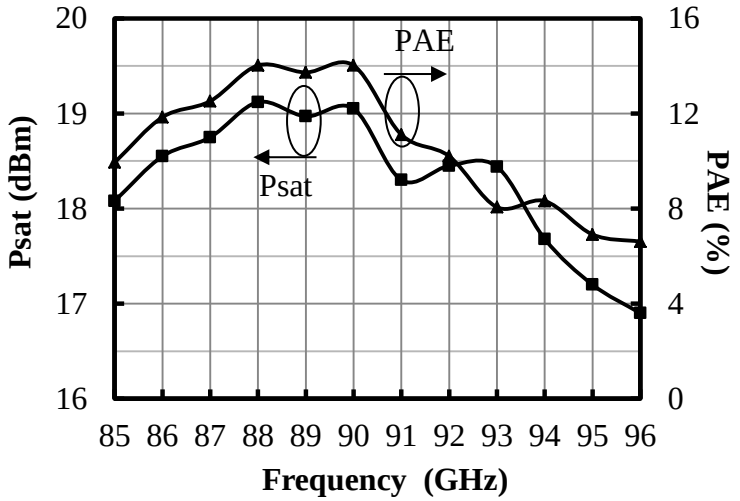


Figure 3.18. Measured PAE and Psat of the multi-drive stacked-FET PA from 85 to 96GHz.

Table 3.1 is a comparison of the measured multi-drive, three-stack PA performance with the conventional three-stack PA [35] and other published results in the same millimeter-wave frequency range. This work demonstrates 2dB more output power in comparison to the traditional three-stack PA at 90GHz while achieving 5% higher PAE. Reference [34] achieves comparable output power with 19% PAE. However these results are achieved at 80GHz using an 8-way power combining technique occupying roughly four times the area of the multi-drive stacked-FET PA presented here.

Table 3.1. Comparison to previous work.

Ref.	**This Work**	[35]	[39]	[3]	[31]	[32]	[33]
Technology	**45nm SOI CMOS**	45nm SOI CMOS	45nm SOI CMOS	65nm CMOS	65nm CMOS	65nm CMOS	45nm SOI CMOS
Design	**Multi-drive three-stack PA**	Three stack PA	Two stage two stack PA	CS. 8 way power combined	Diff. CS, Current combining	CS	Cascode
Frequency [GHz]	**91**	89	86-94	79-81	101-107	79-106	80
Psat [dBm]	**19.2**	17	15.8	19.3	14.8	14.8	12.4
PAE [%]	**14**	9	11	19.2	9.4	8.7	14.2
Gain [dB]	**12.4**	8	10.2	24.2	14.1	12	11
Area* [mm^2]	**0.228**	0.06	0.05	0.855	0.106	<0.28	0.18

*Area excluding the pads

III.F. Conclusion

It has been shown that the gate resistance limits the RF current swing in stacked-FET PAs and the proposed multi-drive stacked-FET PA minimizes this effect by injecting the lost current back to the stack at each stage. A multi-drive three-stack PA is implemented in 45-nm SOI CMOS for 90-GHz operation and achieves 19dBm saturated output power and 14% peak PAE from a 3.4 V power supply. These results are compared against prior work using the same technology and FET geometry and indicate 2dB higher output power and 4% higher PAE than conventional stacked-FET PAs at this frequency.

Chapter 3, in part, has material submitted for publication in "A 42 to 47-GHz, 8-bit I/Q Digital-to-RF Converter with 21-dBm Psat and 16% PAE in 45-nm SOI CMOS," *IEEE Radio Frequency Integrated Circuit Symposium*. The authors are A.Agah, W. Wang, P. Asbeck, J. Buckwalter and L. Larson. The dissertation author is the primary author and investigator of this paper.

IV

Design of Stacked-FET Millimeter-Wave I/Q Modulator

IV.A. Introduction

High-power, high-efficiency RF modulators are needed to keep pace with the growth in communication at millimeter-wave bands. Higher spectral efficiency motivates the application of complex QAM modulations rather than ASK or BPSK [38]. Traditionally, III-V technologies have been preferred for power amplification at millimeter-wave bands. However, CMOS technology lowers costs and allows for higher system integration. In this Chapter, an entire I/Q transmitter is integrated including DAC, mixers, and power amplifier stages. Highly-scaled CMOS suffers from low breakdown voltage and low Q of the passive circuit elements, which lowers reliability as well as amplifier efficiency and linearity. The work presented in Chapter

II at 45 GHz in 45-nm SOI CMOS has demonstrated a stacked-FET PA with 18.6-dBm Psat and 34% PAE and indicates that SOI CMOS is a feasible alternative to III-V technology for these applications [23],[19]. New architectures and approaches are required to enable CMOS-based mm-wave transmitters to have comparable efficiency and output power to III-V implementations.

To achieve high output power and high efficiency with the high peak-to-average power ratios of QAM modulation, in this chapter we propose a new stacked-FET transmitter in 45-nm SOI CMOS at 45 GHz shown in Figure 4.1, which shares a common DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high voltage swing without exceeding the breakdown voltage of the transistors in the stack. Whereas earlier work has demonstrated high supply voltages to generate high-power swings, these designs have supported low resolution and were only capable of providing ASK or BPSK signals [38][42]. The circuit approach proposed here provides high RF output power at high efficiency along with a high-resolution DAC control to transmit complex modulation schemes. The use of high-resolution DACs enables the use of digital predistortion (DPD) to improve the error vector magnitude (EVM) [38][42].

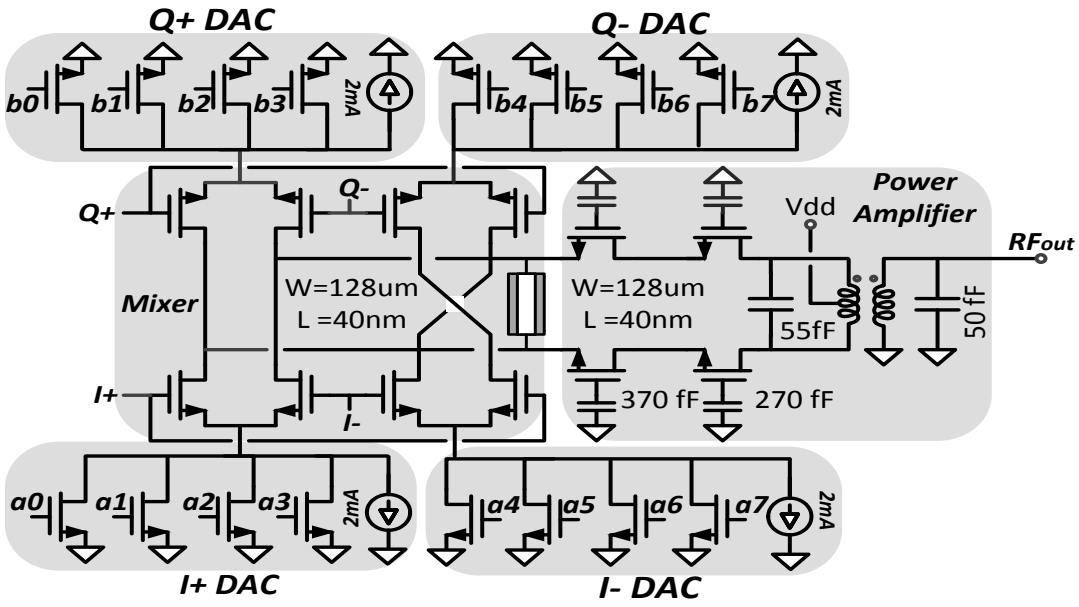


Figure 4.1. Schematic of the high power digital-to-RF converter implemented in 45-nm SOI CMOS process.

IV.B. Design of Stacked-FET Digital-to-RF Converter

The proposed digital-to-RF converter (DRFC) is based on a stacked-FET amplifier shown in Figure 4.1. High RF voltage swings are possible through stacking of transistors, without sacrificing the reliability. The stacked-FET structure is explained in detail in Chapter II.

As shown in Figure 4.1, the bottom (common-source) FET provides the DAC current. The second (common-gate) FET is part of the I/Q mixer. The mixer is implemented as a differential homodyne upconverter with four DACs. Finally, the two top (stacked) FETs form a current buffer that allows a high output voltage swing.

The gate biases of the FETs are selected so that the drain-source voltages of all the power devices are identical and below the breakdown voltage of the technology, which is approximately 1.3 V [23],[19]. The geometry of the FETs in the PA and their

gate capacitors are each designed to provide the optimal load for the previous stage as well as keeping the gate-drain voltage below the breakdown voltage [23],[19].

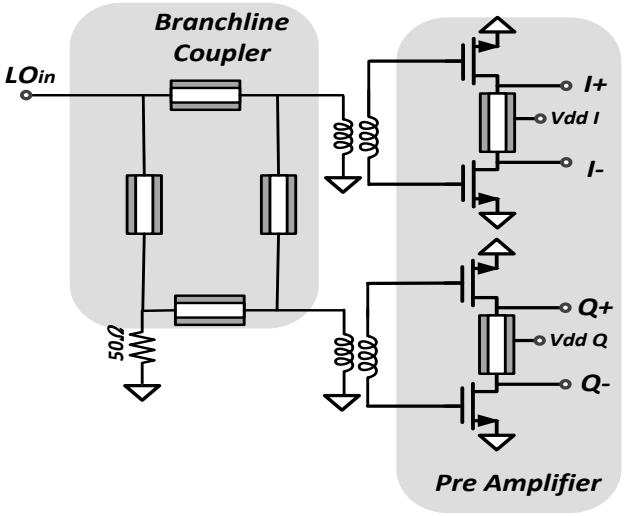


Figure 4.2. LO generation circuit for the digital-to-RF converter implemented in 45-nm SOI CMOS process.

A branchline coupler and two baluns are used to generate LOI+, LOI-, LOQ+ and LOQ- as shown in Figure 4.3. The generation of the quadrature signals from the input LO and the losses associated with this circuitry are included in the DRFC performance characterization. The simulated frequency response of the branchline coupler cascaded with the balun is shown in Figure 4.3. Two pseudo-differential common-source amplifiers amplify the ILO and QLO before applying them to the DRFC to improve the gain of the system and operate with 1.1 V supply to minimize the effect of their power consumption on the overall efficiency of the system. The biases and power supplies of these amplifiers are provided from separate pads to enable the correction of the phase and gain mismatches of the I and Q channels.

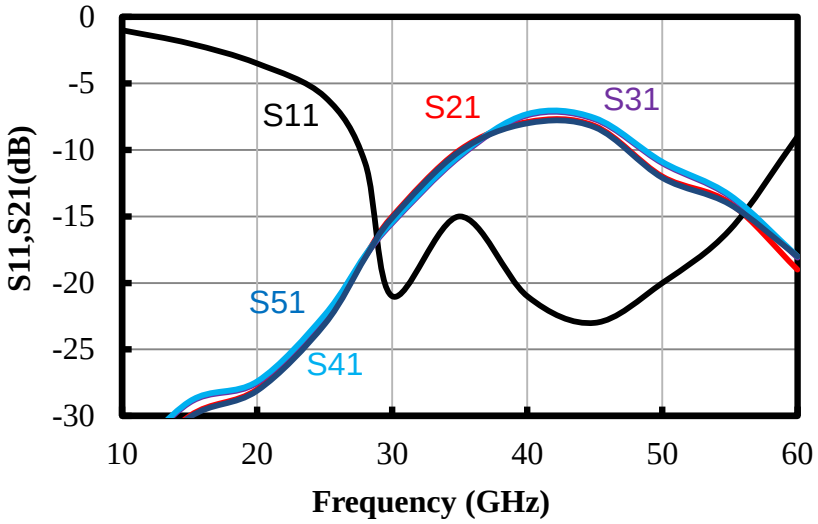


Figure 4.3. Simulated frequency response of the LO generation (excluding the amplifiers).

In traditional class-A, class-AB and class-B PAs, the RF output power is roughly proportional to the input power, and the efficiency of the PA biased in class-A and class-B is respectively proportional to the output power and the square root of the output power [5]. Therefore, the best efficiency achievable at 6 dB back-off output power is respectively one half and one quarter of the peak efficiency for the class-B and class-A PAs. This created a significant efficiency drop, when signals with high PAPR are used.

The proposed circuit can control the output power by changing the DAC code as well as the input LO power. Simulations indicate that the best efficiency at back-off is achieved by keeping the LO power at peak and changing the DAC code. Figure4.4 shows the simulated drain efficiency (DE) and the power gain of the transmitter for two DAC codes, while changing the LO power, where the power gain is defined as

$$\text{Gain} = \frac{P_{\text{out-RF}}}{P_{\text{in-LO}}}. \tag{4.1}$$

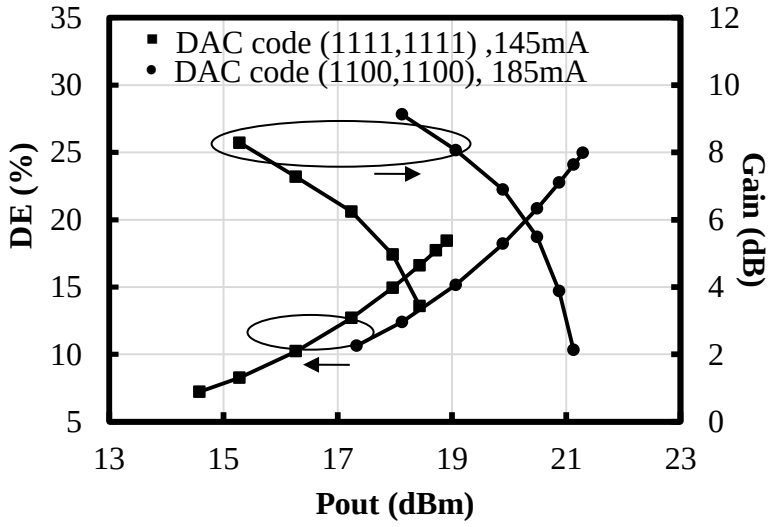


Figure 4.4. Simulated DE and gain of DRFC for two different DAC currents, while sweeping the LO power.

The DRFC is operated in class-B mode to achieve the highest efficiency. To operate in class-B, the I+ DAC – shown in Figure 4.1 - is turned off when the I- DAC is on, or vice versa. This maximizes the efficiency without degrading the output power. A 2 mA keep-alive current is utilized with each DAC to improve linearity and control the voltage swing across each FET, which might compromise reliability if the current drops to zero with a 4 V supply. A shunt 50Ω CPW is utilized for inter-stage matching [23] between the mixer and the PA shown in Figure 4.1. Simulations indicate that this inter-stack matching network improves the efficiency by approximately 3%. It is possible to use the inter-stack matching between the sources of the last FETs in the stack. However, simulations indicate an insignificant efficiency improvement that does not justify the required layout area and complexity.

To minimize pad area limitations, a serial-to-parallel converter demuxes high-speed input data. Current mode logic (CML) is used to maximize the speed of these blocks. Measurements indicate proper operation to 13.5 Gbps.

The output amplitude of the DRFC is constant for BPSK and QPSK constellations ignoring the transition periods between different points in constellation. However, to generate a 16-QAM signal, the output amplitude and phase change simultaneously. As shown in Figure 4.1, cascode transistors are avoided in the design for efficiency considerations. Varying current through the DAC transistors, the drain voltage of these devices are modulated, which results in current nonlinearity. These nonlinearities are not critical in BPSK or QPSK modulations, however in a QAM signal they cause high EVM even at low data rates. These errors can be corrected to some extent using digital predistortion; however the other solution would be to use cascode devices to provide better isolation, at an efficiency penalty of approximately 2%.

IV.C. Measurement Results and Comparison

The microphotograph of the DRFC is shown in Figure 4.5. The area of the circuit is 1.15mm^2 with a significant area overhead for the branchline coupler and baluns that generate differential quadrature signals from the input LO. The tested chip also contains a digital serial-to-parallel converter.

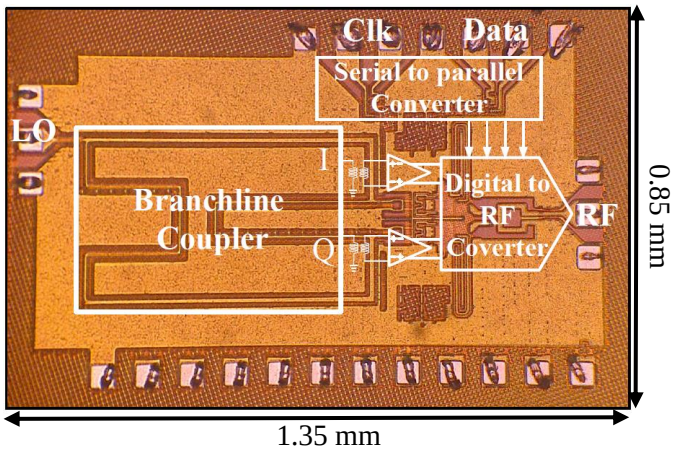


Figure 4.5. Photomicrograph of digital-to-RF converter.

As shown in Figure 4.1 and 4.2, three on-chip baluns are used in the design of the DRFC. Two of these baluns generate differential I and Q LO signals and an output balun converts differential signal to single-ended for the purpose of measurement and calibration. The loss of the output balun is calculated by measuring the S-parameters of two back-to-back baluns and each balun is found to have approximately 1.45 dB loss at 45-GHz. This loss is de-embedded from the power measurement.

Figure 4.6 shows the simulated and measured PAE, DE and gain as a function of output power, i.e. the LO power is varied, at the highest DAC current level, e.g. I+ = 1111, I- = 0000, Q+ = 1111 and Q- = 0000. The DRFC achieves a saturated output power of 21 dBm at 45 GHz with peak PAE of 16% and peak gain of 7.1dB. The peak drain efficiency is 24%

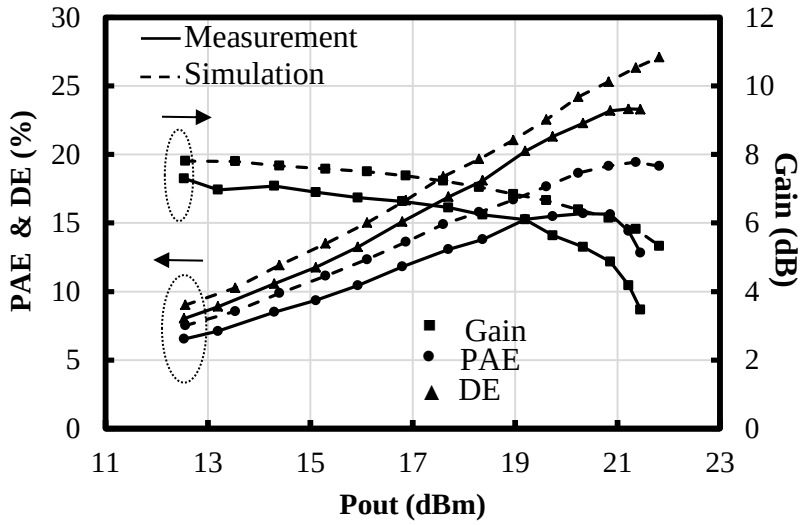


Figure 4.6. Measured and simulated gain, PAE and DE as a function of output power.

The maximum output power and maximum PAE of the DRFC are measured as a function of frequency in Figure 5. The circuit exhibits more than 18 dBm saturated output power from 42 to 47 GHz, while the PAE remains above 13% over the same range.

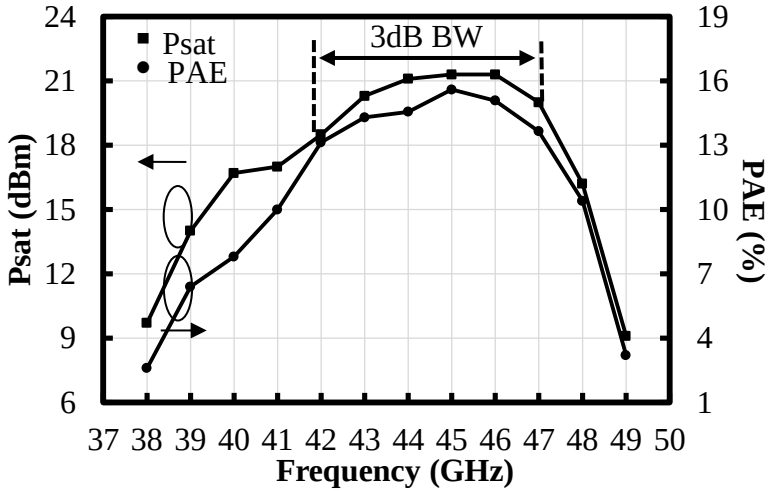


Figure 4.7. Measured peak PAE and saturated output power as a function of frequency.

To illustrate the ability of the DRFC to generate complex constellations such as 16-QAM, the output power is measured for various points of a QAM constellation. Figure 4.8 shows the measured drain efficiency as a function of output power at three digital I / Q pairs, demonstrating the ability of the DRFC in creating QAM signals.

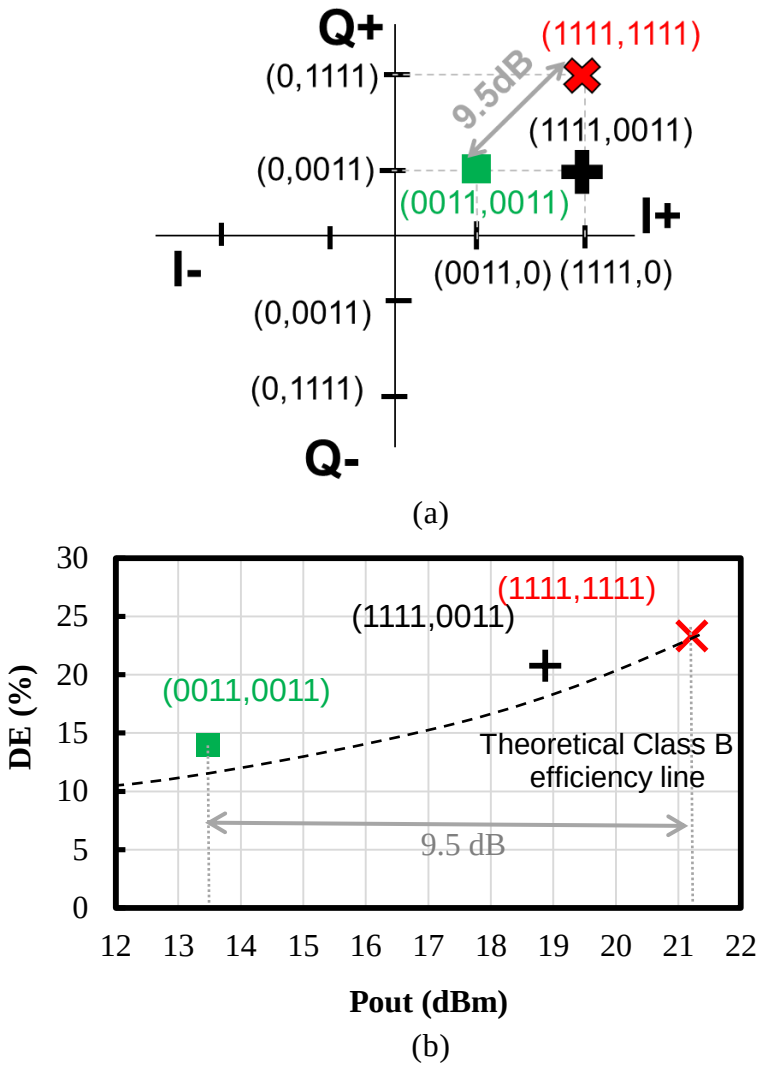


Figure 4.8. (a) Three points in the constellation (b) Measured DE as a function of output power for the consolation points shown in (a).

Figure 4.8 (b) also plots a theoretical class B efficiency line with the peak power and peak efficiency identical to the designed DRFC, demonstrating the efficiency advantage of the DRFC over the class-B PA at back-off powers.

The measurement indicates a 0.3 dB amplitude mismatch between I and Q channels. The error is corrected by increasing the power supply of the I preamplifier.

The error vector magnitude (EVM) is measured by downconverting the RF output from 45GHz to 3GHz and sampling the signal for digital demodulation. The measurement shows that the DRFC is capable of generating BPSK, QPSK and 16QAM signals with a 45GHz carrier at data rates in excess of 1 Gb/s. The uncalibrated measurement shows a BPSK signal to a maximum 735 Mbps and a QPSK signal at 1.2 Gbps at less than 4% and 7% EVM, respectively. According to [41], these EVM results correspond to BERs lower than 10-7 and 10-4 for BPSK and QPSK signals. A 16-QAM signal at 40 Mb/s showed an EVM of 9% and the data rate was limited by interfaces with the test equipment at this time. The EVM of the modulated signal as a function of the symbol rate is shown in Figure 4.9 for BPSK, QPSK and 16QAM modulations.

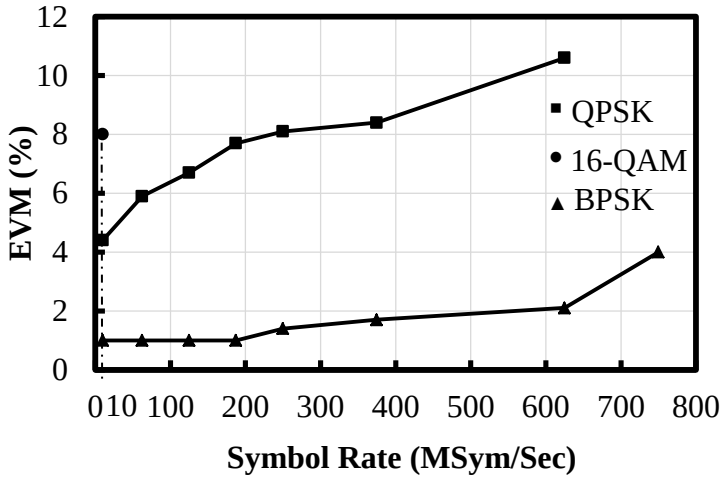


Figure 4.9. Measured EVM for BPSK, QPSK and 16QAM as a function of symbol rate.

The 4-bit DACs in the I and Q channels support the use of digital predistortion on low-order constellations. The use of predistortion improves the errors due to circuit mismatch. Figure 4.10 shows how the EVM of QPSK signal improves using predistortion at different symbol rates.

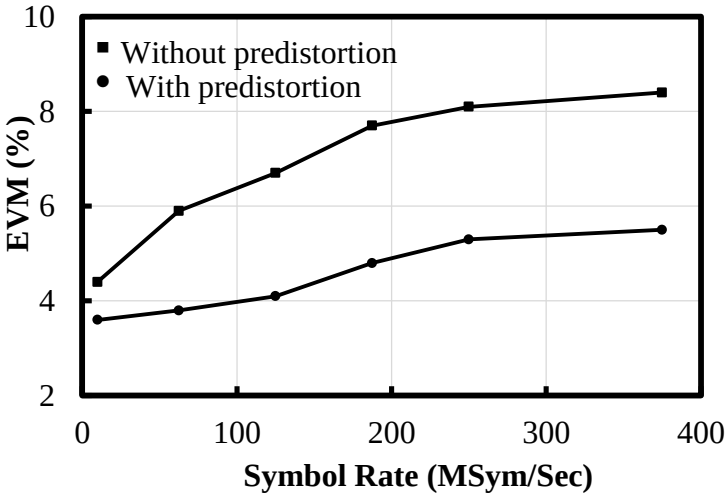


Figure 4.10. Measured EVM for QPSK with and without predistortion as a function of symbol rate.

Table 4.1 summarizes the measured performance and compares the results with recently published mm-wave modulators. This work demonstrates extremely high-power and efficiency, while generated higher-order complex modulation.

Table 4.1.
Comparison of millimeter-wave modulators

Technology	45nmCMOS SOI	120nm SiGe BiCMOS	45nm CMOS SOI
References	This Work	[43]	[42]
Freq (GHz)	42-48	40-45	40-50
Supply (V)	4	2.5	4.2-5.1
Modulation/Symbol Rate/EVM	BPSK/ 750Mbps/4% QPSK/ 1.25Gbps/5.5% 16QAM/ 40Mbps/8%	64QAM/ 48Mbps/2.1%	ASK/ 1.25Gbps/- BPSK/ 2.5Gbps/ -
Psat (dBm)	21.3	1	23.5-24.3
Peak PAE (%)	16	-	22-14.6
Area (mm2)	1.15	5	0.77

IV.D. Conclusion

A novel stacked FET digital-to-RF converter is implemented in 45-nm SOI CMOS, which shares DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high output power. The proposed architecture transmits at 1.25 Gbps for QPSK at 45GHz at an EVM of 5.5% using digital predistortion. . This transmitter exhibits a 21.3-dBm saturated output power, while achieving a peak PAE of 16%. The circuit occupies 0.3mm2 including pads, while the PAE and Psat remains above 13% and 18 dBm from 42 to 47 GHz.

Chapter 4, in part, is a reprint of the material as it appears in "Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45-nm SOI CMOS *IEEE Journal of Solid-State Circuits*, October, 20013. The authors are Amir Agah, Hayg Dabag, Bassel Hanafi, Peter Asbeck, James Buckwalter and Lawrence Larson. The dissertation author is the primary author and investigator of this paper.

V

Design and Analysis of Millimeter-wave Doherty Power Amplifiers

V.A. Introduction

With the growth in applications of the millimeter-wave spectrum for broadband terrestrial wireless communication, satellite radio and automotive radar, the need for fully integrated high-power, high-efficiency millimeter-wave power amplifiers (PAs) is growing. Traditionally, this field has been dominated by III-V and SiGe technology due to the high gain and high output power of these processes. However, the lower cost and higher integration level offered by CMOS technology has motivated research into CMOS mm-wave PA design. At the same time, the low breakdown voltage and poor passive element quality factor of silicon technology poses major challenges. Recent work in SOI CMOS, e.g., 14.5 dBm saturated output power and 25% PAE at 60 GHz with 65-nm SOI CMOS [27], 12.5 dBm Psat and 15% PAE at 80 GHz [33] and 18.6-dBm Psat and 34% PAE at 45 GHz with 45-nm SOI

CMOS [23], shows that SOI CMOS is becoming a realistic alternative to III-V and SiGe technology for these applications.

Most power amplifiers have high power-added efficiency (PAE) at peak power levels, but the efficiency drops as the input power decreases. However, modern communication systems employ modulation techniques that exhibit high peak-to-average power ratios (PAPRs) and demand for amplifiers with high efficiency over a wide power range is increasing. The traditional Doherty power amplifier is one of the circuits that satisfy this demand by providing peak efficiency at 6-dB back off as well as peak power.

The integration of a millimeter-wave transmitter for radar, guidance and high data rate satellite communication at 45 GHz has encouraged research in high efficiency PAs that operate with high-efficiency in back-off, and recent work has addressed the design of Doherty power amplifiers at 45 GHz [44]. In this chapter, a modified Doherty PA is presented that addresses the limitations of the traditional design. The results demonstrate improved back-off PAE as well as higher gain for a mm-wave Si CMOS PA. Block diagrams of the traditional Doherty PA is shown in Figure 5.1 (a).

In Section V.B, the challenges of designing a fully integrated Doherty PA for mm-wave applications are discussed and the active phase-shift Doherty PA is proposed, shown in Figure 5.1 (b). In Section V.C, the slow-wave CPW is discussed and compared to the traditional ground shielded CPW. In Section V.D, the design and implementation of a Doherty PA with ground-shielded CPW and slow-wave CPW are presented as well as the proposed active phase-shift Doherty PA. The circuit

measurements are reported in Section V.E along with a comparison to previous results.

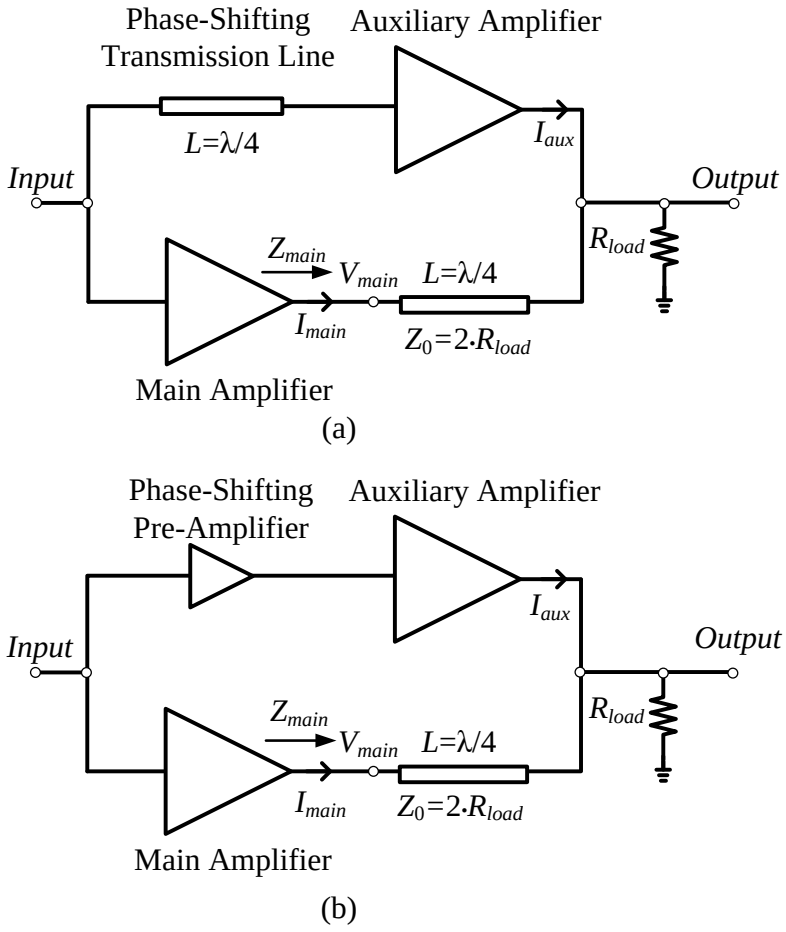


Figure 5.1. (a) Traditional Doherty amplifier (b) Proposed active phase-shift Doherty amplifier .

V.B. Fully Integrated Doherty Power Amplifier

V.B.I. Review of Conventional Doherty Amplifier Design

A conventional Doherty amplifier consists of two power amplifiers – a main amplifier and an auxiliary (peaking) amplifier – interconnected with two quarter-wavelength transmission lines as shown in Figure 5.1 (a) [5]. The main amplifier is designed to be *on* at all input power levels, while the auxiliary amplifier is only *on* at high input power levels. This is achieved by biasing the auxiliary amplifier in class C and biasing the main amplifier in class A.

The characteristic impedance of the transmission line at the output of the main amplifier is twice the load impedance. At low input power levels (LP), when the auxiliary amplifier is *off*, the impedance seen by the main amplifier is:

$$Z_{main-LP} = \frac{{Z_0}^2}{R_{load}} = 4 \cdot R_{load} \tag{5.1}$$

and as a result the voltage swing at the output of the main amplifier at low input power ($V_{main\text{-}LP}$) is

$$V_{main-LP} = \frac{{Z_0}^2}{R_{load}} \cdot I_{main} = 4 \cdot R_{load} \cdot I_{main} \tag{5.2}$$

where I_{main} is the current swing at the output of the main amplifier. The current of the main amplifier and R_{load} are designed so that when $I_{main}=I_{main\text{-}max}/2$, V_{main} reaches its maximum, which is

$$Max(V_{main-LP}) = 2 \cdot R_{load} \cdot I_{main-max} = Vdd_{main} \tag{5.3}$$

where Vdd_{main} is the power supply voltage of the main amplifier and $I_{main\text{-}max}$ is the maximum I_{main} . Since the voltage swing is maximized, the efficiency of the main amplifier peaks as well.

Increasing the input power further increases I_{main} above $I_{main\text{-}max}/2$, and the auxiliary amplifier turns *on*. Assuming infinite output impedance for the main and auxiliary amplifiers, the voltage at the output of the main amplifier is [14],[15]

$$V_{main-HP} = \frac{{Z_0}^2}{R_{load}} \cdot I_{main} - jZ_0 I_{aux} . \tag{5.4}$$

Considering that $Z_0=2R_{load}$, if the output current of the auxiliary amplifier is set to

$$I_{aux} = -j2\left(I_{main} - \frac{I_{main-max}}{2}\right) \tag{5.5}$$

and substituted into (5.4), then V_{main} becomes independent of I_{main} and remains at its peak value in (5.3). As a result, the efficiency of the main amplifier also remains at its peak even when $I_{main}>I_{main\text{-}max}/2$. However, the efficiency of the auxiliary amplifier is not at its maximum until it reaches its peak output power, at which point, the overall efficiency peaks. Figure 5.2 shows the simulated ideal drain efficiency of the Doherty PA as a function of the normalized output power, assuming zero knee voltage for the transistors and lossless transmission lines. Figure 5.2 also includes the simulated efficiency of the Doherty PA for different classes of operation for the main and auxiliary amplifier [16].

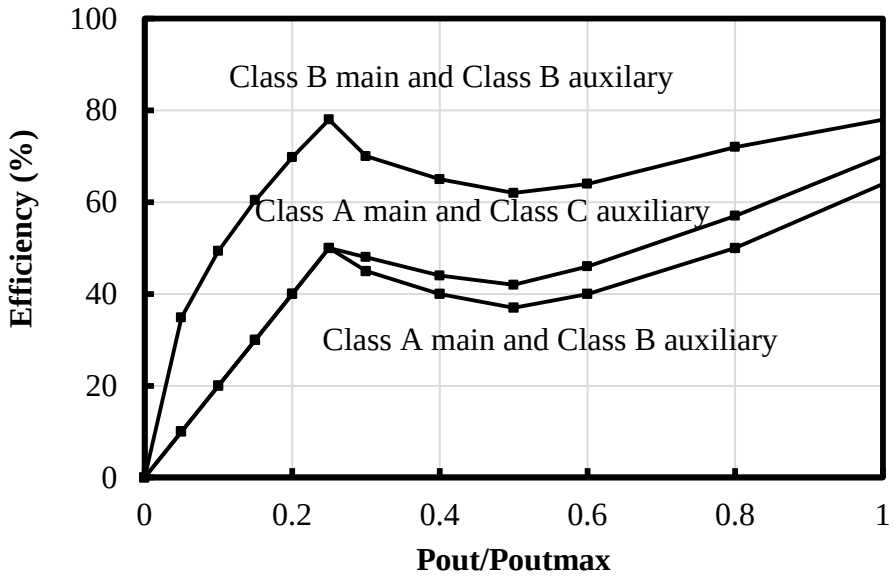


Figure 5.2. Ideal drain efficiency of the conventional Doherty PA with different biasing for the main and auxiliary amplifier. Drain current conduction angle is 110° for class-C operation.

In a conventional Doherty amplifier **Error! Reference source not found.**], the phase shift needed for (5.5) is achieved by utilizing a quarter-wavelength transmission line at the input of the auxiliary amplifier, and the auxiliary amplifier is designed to have twice the transconductance of the main amplifier **Error! Reference source not found.**].

V.B.II. Design of a fully-integrated mm-wave Doherty PA

The small size of the quarter wavelength transmission lines and the high f_t of the CMOS transistors allows fabrication of compact and fully integrated Doherty PAs at millimeter-wave frequencies. However, the low gain of the amplifiers at these bands is a challenge. The maximum current gain of a single-stage amplifier is limited

by ω_t/ω, where ω_t is the short-circuit current gain cutoff radian frequency. Assuming that $R_{load} \approx R_{source}$, it can be shown that

$$Power\ gain \leq \left(\frac{\omega_t}{\omega}\right)^2. \tag{5.6}$$

Considering 45 GHz as the operating frequency and f_t ≈200 GHz, a single-stage design provides roughly 14 dB power gain. With the high losses of the passive elements in a standard Si technology, achieving more than 7 or 8-dB gain from a single stage is difficult.

Since PAE=DE·(1-1/*G*), where *G* is the power gain and DE is the drain efficiency, reducing the gain by only 2 dB reduces the PAE by approximately 13%, when the PA has the initial gain of 6 dB. This PAE reduction is less than 1.5%, when the PA has 16 dB of gain. So even a small increase in the gain of a PA can have a significant effect on the PAE, when the initial gain is low.

Additionally, the low quality factor (*Q*) of the passive elements is a major obstacle. EM simulations show that a quarter-wavelength transmission line has approximately 0.7 dB loss at 45 GHz, which further reduces the gain. Figure 3 shows the effect of this transmission line loss on the efficiency of the Doherty PA at peak and 6-dB back-off power. The efficiency drops by 10% with a 1 dB transmission line loss at 6 dB back-off power.

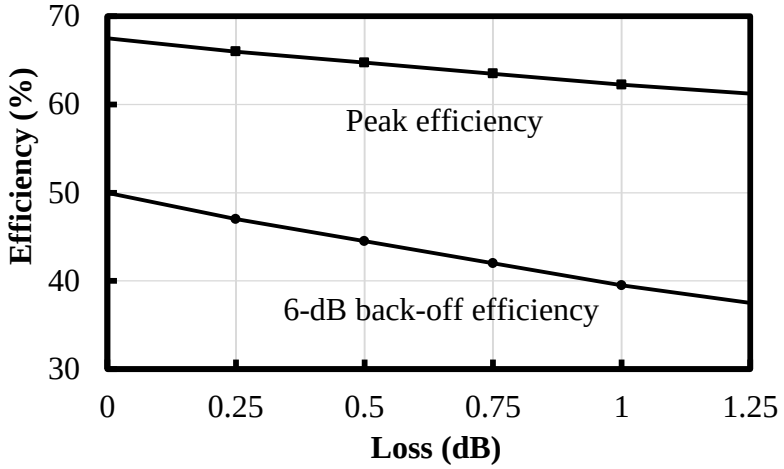


Figure 5.3. Simulated efficiency as a function of loss in the output transmission line of a Doherty PA with class A main and class C auxiliary amplifier.

To increase the gain, one can use a preamplifier to drive a Doherty PA or utilize two-stage amplifiers as the main and auxiliary PAs [45]. However both of these solutions have major efficiency penalties, especially at back-off power, since the driver amplifier is not operating at its peak efficiency in the back-off power region.

To address these problems, an active phase-shift Doherty amplifier is proposed, where the input quarter wave transmission line is replaced with a phase-shifting preamplifier as shown in Figure 5.1 (b). To reduce the output transmission line loss, a slow-wave coplanar waveguide (CPW) transmission line is investigated in Section IV [44]. The length of this transmission line is further reduced by incorporating the parasitic capacitance at the output of the main amplifier.

In a conventional Doherty PA, the auxiliary amplifier is *off* at low input power levels. In practice, the auxiliary amplifier gradually turns *on*, as the input power

increases and the load impedance of the main amplifier is modulated before it reaches its peak efficiency. For example, from (5.1), if the auxiliary amplifier turns *on* prematurely and delivers 10% of its peak current to the load, the impedance seen by the main amplifier reduces by 10%, resulting in a 10% reduction in efficiency.

One possible solution is to bias the auxiliary amplifier in deep class C but this will reduce its gain significantly. Adaptive biasing adjusts the gate d.c. bias of the auxiliary amplifier as a function of input power [16],[46-47] to keep the amplifier in deep class C at low input power and in class AB at high input power levels. As a result, the auxiliary amplifier is totally *off* at low input power and now has sufficient gain at high input power levels. An uneven power drive Doherty PA [48] is another solution to this problem, which is not employed here because of the low gain of the mm-wave amplifiers.

V.C. Active Phase-Shift Doherty Amplifier

As was mentioned in the previous Section, the single-stage gain of the mm-wave Doherty PA is low, which reduces the PAE. To increase the gain of the Doherty PA, without sacrificing back-off efficiency, and reduce the area of the PA, an active phase-shift Doherty amplifier is proposed that creates a 90° phase shift at the input of the auxiliary amplifier.

The circuit shown in Figure 5.4 illustrates the combination of the phase-shifting preamplifier and the auxiliary amplifier. When the circuit parameters of the phase-shifting preamplifier are correctly selected, the required 90° phase shift is generated between V_{g2} and V_{g1}. In a Doherty PA, the geometry of M_2 is selected

according to the required peak power capability of the auxiliary amplifier. Therefore, the geometry of driver (M_1) is set to a size that delivers enough power to saturate the auxiliary amplifier and to therefore achieve the best efficiency. In this case, W_{M1}=128μm and W_{M2}=256μm .

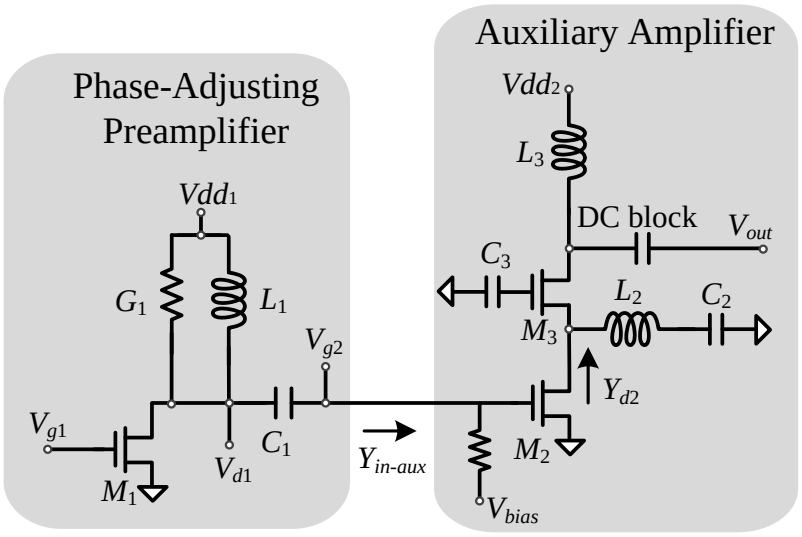


Figure 5.4. Phase-shifting preamplifier and auxiliary amplifier.

If C_{dg} of M_1 is neglected, the voltage gain from V_{g1} to V_{g2} (H_1) is

$$H_1(\omega) = \frac{V_{g2}}{V_{g1}} \cong -g_{m1}\left(\frac{s^2C_1L_1G_1 + sC_1 + Y_{in-aux}(s^2C_1L_1 + sL_1G_1 + 1)}{s^2C_1L_1}\right)^{-1}, \quad (5.7)$$

where

$$Y_{in-aux} = sC_{gs2} + sC_{dg2}\left(\frac{g_{m2} + Y_{d2}}{sC_{dg2} + Y_{d2}}\right). \quad (5.8)$$

Since the auxiliary amplifier is a stacked-FET PA and the total capacitance at the drain of M_2 is resonated with L_2 , which is explained in detail in Section III, the admittance seen at the drain of M_2 is

$$Y_{d2} = g_{m3}\left(\frac{C_2}{C_{gs3}+C_2}\right). \tag{5.9}$$

Assuming that Y_{d2} is small compared to ωC_{dg2} at millimeter-wave frequencies, (5.8) can be rewritten as

$$Y_{in-aux} \cong sC_{gs2} + g_{m2} + Y_{d2} \cong sC_{gs2} + G_{in-aux}, \tag{5.10}$$

where $G_{in\text{-}aux}=g_{m2}+Y_{d2}$. By substituting (5.10) into (5.7)

$$\frac{1}{H_1} \cong \frac{-s}{g_{m1}}\left(\left(\frac{s^2C_1L_1C_{gs2} + L_1G_1G_{in-aux} + C_{gs2} + C_1}{s^2C_1L_1}\right)\right)$$

$$-\frac{1}{g_{m1}}\left(\frac{s^2L_1\left(G_1\left(C_1+C_{gs2}\right)+C_1G_{in-aux}\right)+1}{s^2C_1L_1}\right) \tag{5.11}$$

Equation (5.11) shows that the preamplifier creates a 90° phase shift between V_{g2} and V_{g1} at frequency

$$\omega_O = \frac{1}{\sqrt{L_1C_1\left(\frac{G_1}{G_{in-aux}}\left(1+\frac{C_{gs2}}{C_1}\right)+1\right)}}. \tag{5.12}$$

C_1 and L_1 must be selected to establish the desired phase. Figure 5.5 plots the relation between C_1 and L_1 using (5.12) when f_o=45GHz and W_2=W_3=2W_1=256μm.

By substituting L_1 in (5.11) using (5.12),

$$|H_1(\omega_O)| = \frac{g_{m1}}{\omega_O C_1 + \frac{G_1 G_{in-aux}}{\omega_O C_1} + \frac{G_1}{G_{in-aux}}\left(\frac{\omega_O (C_{gs2} + C_1)^2}{C_1}\right)}. \quad (5.13)$$

Figure 5.5 shows the simulated and calculated $|H_1(\omega_o)|$ at 45GHz when W_2=W_3=2W_1=256µm. There is an optimum value for L_1 and C_1 that maximizes the gain, while achieving 90° phase shift. To determine the optimum value of C_1,

$$\frac{d|\,H_1(\omega_O)|}{dC_1} = 0. \quad (5.14)$$

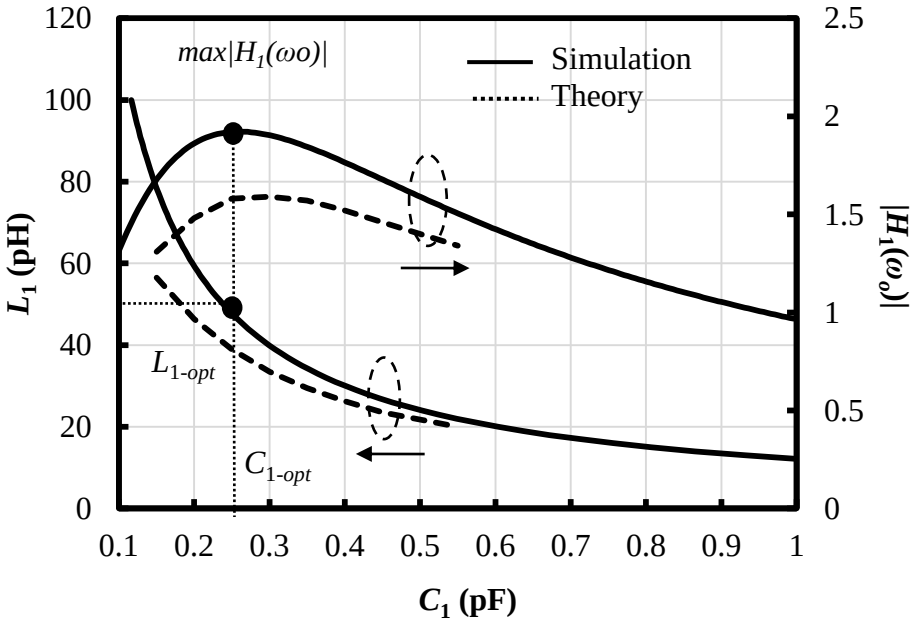


Figure 5.5. Analysis and circuit simulation of $|H_1|$ and L_1 vs. C_1 to achieve $\angle H_1$=90° at 45GHz, when W_2=W_3=2W_1=256µm, C_1=250fF and L_1=45nH

Solving (5.14) shows that the value of C_1 that achieves the highest gain is

$$C_{1,opt} = \left[\frac{G_{in-aux}G_1 + 2C_{gs2}\omega_O}{\omega_O{}^2(1+\frac{G_1}{G_{in-aux}})}\right]^{\frac{1}{2}} \tag{5.15}$$

and the value of L_1 that maximizes the gain ($L_{1\text{-}opt}$) is calculated from (12), and is shown graphically in Figure 5.5.

By using the extracted parameters from circuit simulation, when W_2=W_3=2W_1=256μm, C_1 = 250fF and L_1 = 45pH into (5.11), $|H_1|$ and $\angle H_1$ are plotted in Figure 5.6. This graph also shows the agreement between the circuit simulation and analytical results.

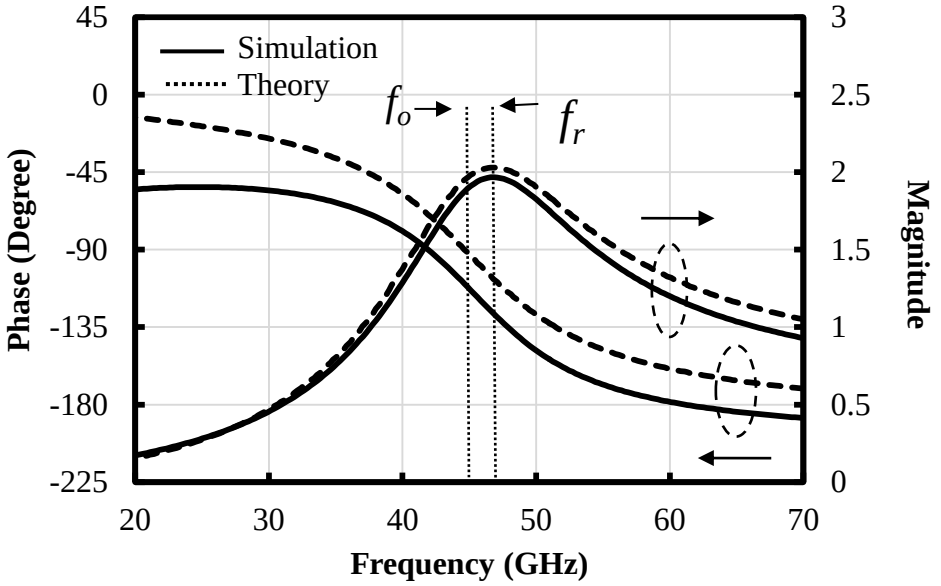


Figure 5.6. $|H_1|$ and $\angle H_1$ using (5.10) and circuit simulation, when W_2=W_3=2W_1=256μm, C_1=250fF and L_1=45nH.

As was mentioned in Section V.B.I, the auxiliary amplifier has twice the transconductance of the main amplifier as shown in Figure 5.6. The active phase-shift preamplifier increases the gain of the auxiliary amplifier, which assists in achieving this goal.

As shown in Figure 5.6, the frequency at which $\angle H_1$=-90° (f_o) is lower than the peak gain resonance frequency (f_r) where $|H_1|$ is maximum. The resonance ω_r occurs approximately at

$$\omega_r \cong \frac{1}{\sqrt{L_1\left(\frac{C_1 C_{gs2}}{C_1+C_{gs2}}\right)}}. \tag{5.16}$$

The result is that the phase-shifting preamplifier sacrifices less than one dB gain to achieve the required phase shift.

Simulations show that the transmission line length required for L_1 is much smaller than λ/4, and the use of the phase-shifting preamplifier reduces the overall area by approximately 20%.

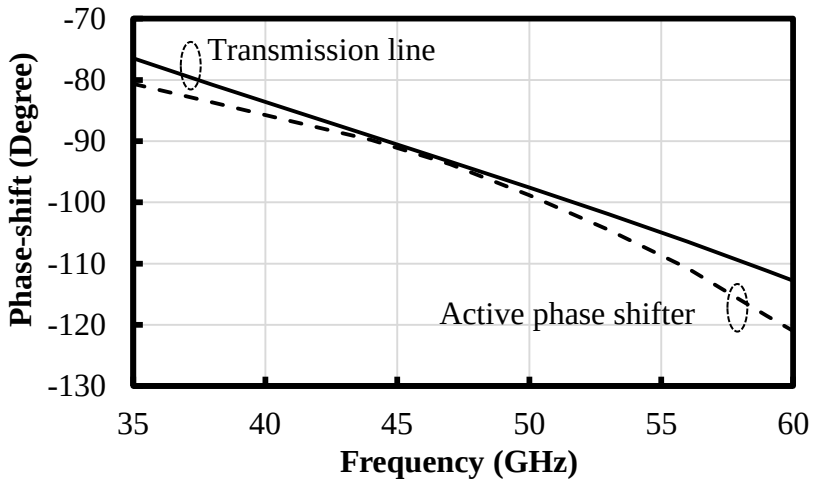


Figure 5.7. Phase shift as a function of frequency for a transmission line and the active phase-shift preamplifier.

Figure 5.7 plots the phase of H_1 as a function of frequency and compares it to the phase shift of a quarter-wavelength transmission line. This simulation shows that the phase-shifting amplifier can be utilized at the input of the auxiliary amplifier in the Doherty PA to create the required phase shift with little bandwidth penalty. In fact, this technique increases the gain of the auxiliary amplifier as shown in Figure 5.6. To take best advantage of this increased gain, the power consumption of the phase-shifting preamplifier should be minimized. Therefore, the preamplifier is implemented as a common-source amplifier with a 1.2 V power supply.

V.D. Slow-Wave Transmission Line Structure

Since a quarter-wave line is relatively long (λ/4=800 μm at 45 GHz), the overall die area of a traditional Doherty amplifier is determined by the size of the input and output networks. At the same time, the losses of these CPW transmission lines reduces the overall gain and efficiency. In order to improve the performance, a slow-wave CPW is investigated.

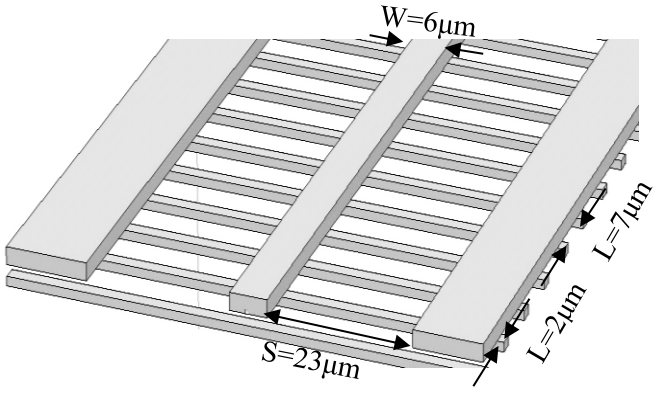


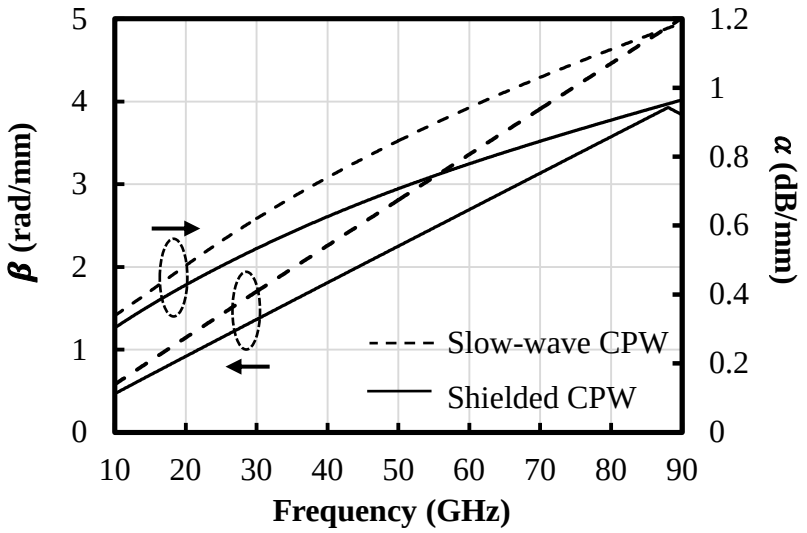
Figure 5.8. Slow-wave CPW structure with Z0≈50Ω.

Seki and Hasegawa proposed a slow-wave CPW for reducing the signal speed to create a more compact quarter-wave CPW transmission line [49]. This technique has recently been introduced in mm-wave PA design [51].

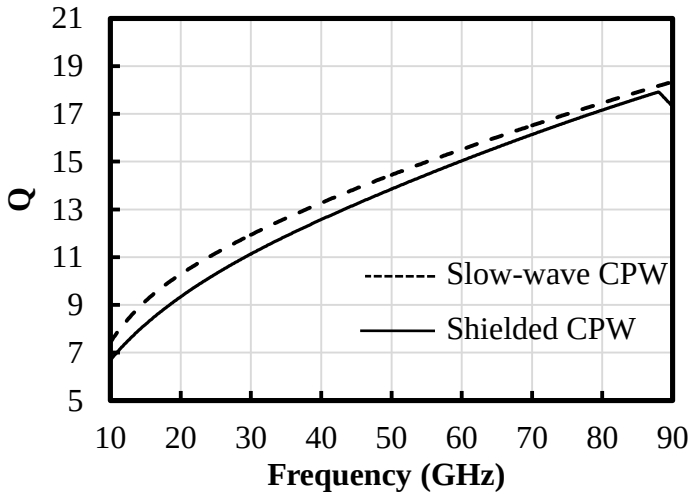
The design of a slow-wave CPW is shown in Figure 5.8 and consists of floating metal strips underneath the signal line and ground planes of a CPW. These metal strips are perpendicular to the signal line. Considering the symmetry of the S-CPW structure, the voltage of each floating metal stripe is 0 V with respect to the CPW line, therefore they can be considered as an effective shield between the CPW and the substrate, which minimizes the substrate loss. However, unlike the grounded substrate shield, these floating strips increase the distributed capacitance of the line without reducing the distributed inductance [51]. Since

$$v_p \propto \lambda \propto \frac{1}{\sqrt{L \cdot C}} \ , \tag{5.17}$$

where λ is the wavelength and v_p is the signal velocity. Therefore, the signal speed, impedance, and wavelength are reduced, resulting in more compact quarter wavelength transmission lines [51].



(a)



(b)

Figure 5.9. Simulated α, $\boldsymbol{\beta}$ and Q for a ground-shielded (800 μm) and slow-wave (620 μm) CPW. Z_0=50 Ω.

The simulated attenuation constant (α), phase constant (β) and quality factor (Q) of a λ/4 shielded 50 Ω CPW with L=800 μm and a slow-wave CPW with L=620 μm are compared in Figure 5.9 (a) and (b) using Sonnet™. The quarter-wave S-CPW

is 30% shorter than the grounded CPW and although it has higher loss per unit length, it has lower loss per unit wavelength and higher *Q* in comparison to the shielded CPW.

V.D. Design of Mm-wave Doherty PAs

In this section, the design of three Doherty PAs fabricated in 45-nm SOI CMOS will be reviewed. In Section V.D.I, two traditional Doherty PAs are designed using stacked amplifiers as main and auxiliary PAs. One amplifier uses slow-wave CPWs and the other employs ground-shielded CPWs as a comparison. As discussed in previous section, the length of the λ/4 slow-wave CPWs is 30% shorter than the shielded CPW, and since the length of transmission lines are the main factor in determining the overall area of the Doherty PA, using them reduces the total chip area by 20%.

In Section V.D.II the design of the third amplifier - the proposed active phase-shift Doherty PA is discussed.

V.E.I. Doherty Amplifiers Using Traditional and Slow-Wave Transmission Line Structures

The schematic of the designed Doherty power amplifiers are shown in Figure 5.10.

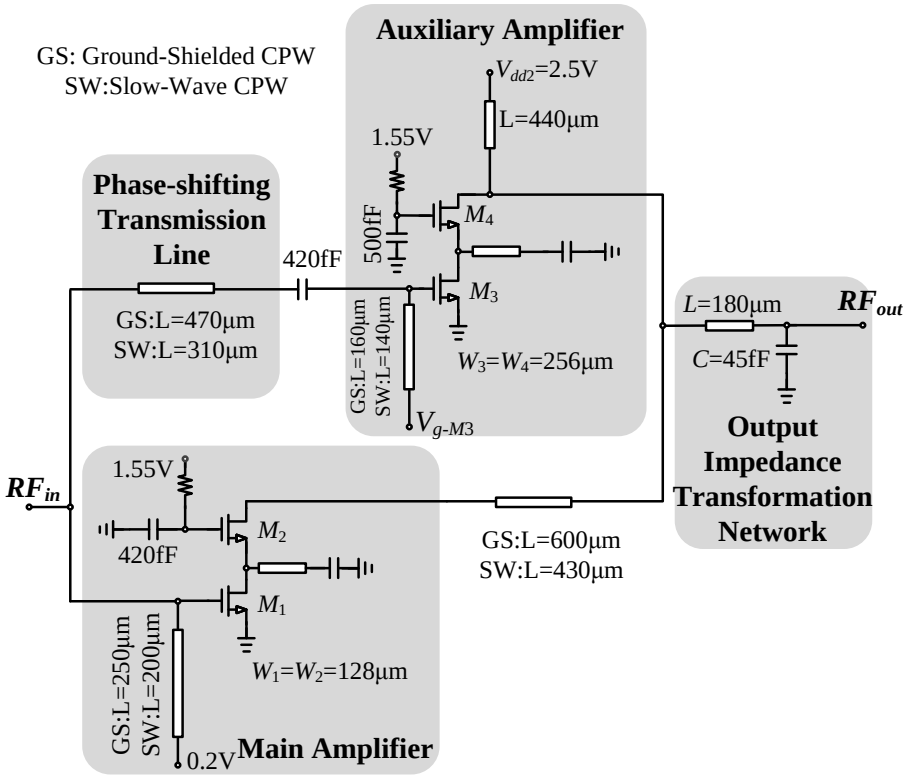


Figure 5.10. Schematic of the Doherty amplifiers with ground-shielded CPW and slow-wave CPW.

All the transmission lines in this work are implemented with 2.2 μm thick top metal layer to minimize resistive loss. As was mentioned in Section V.B.I, Z_0 should be $2 \cdot R_{load}$ in Doherty PA, where Z_0 is the characteristic impedance of the transmission line. Therefore, R_{load}=50 Ω requires Z_0=100 Ω. However, the maximum possible characteristic impedance on this metal layer is approximately 60 Ω, since the minimum width of the line is 4 μm. This motivates the need for an impedance transforming section at the output of the Doherty PA that transforms the 50 Ω load to a lower impedance - in this case 25 Ω. This impedance transformation is implemented using a shunt capacitor and a series transmission line as shown in Figure 5.10.

Since Z_0=50Ω and R_{load} is transformed to 25 Ω, this transmission line ideally provides a 100 Ω load for the main amplifier. However, the parasitic capacitance at the output of the main amplifier introduces an undesirable susceptance to this resistive load reducing the efficiency of the main amplifier. To provide a purely 100 Ω resistive load for the main amplifier, the length of this transmission line is reduced by 200 μm to 600 μm and the parasitic capacitance is included in the impedance transforming network. Figure 5.11 shows the network of the series 600-μm transmission line and the shunt parasitic capacitance at the output of the main amplifier transferring a 25 Ω load to 100 Ω. Using this technique, the loss of the transmission line is reduced by approximately 0.1 dB.

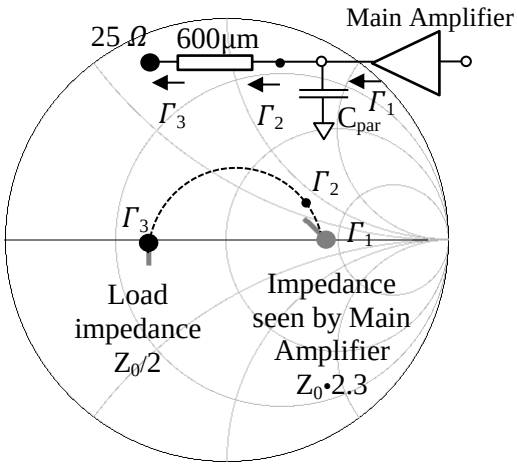


Figure 5.11. Impedance seen by main and auxiliary amplifiers at back-off power.

Simulation results at 42 GHz for the DE, PAE and gain of the Doherty PA with and without the slow-wave CPW are shown in Figure 5.12 and Figure 5.13. Both of these PAs achieve approximately 18-dBm saturated output power.

Comparison of these figures indicates that the Doherty PA with the slow-wave CPW achieves approximately 5% and 6% more DE and PAE at 6-dB back-off power when compared to the PA with ground shielded CPW, a significant improvement.

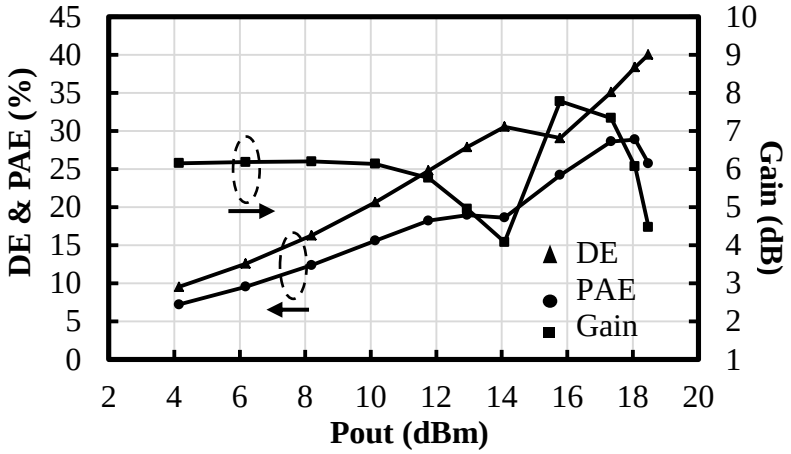


Figure 5.12. Simulated gain, DE and PAE of the Doherty PA with ground-shielded CPW as a function of output power.

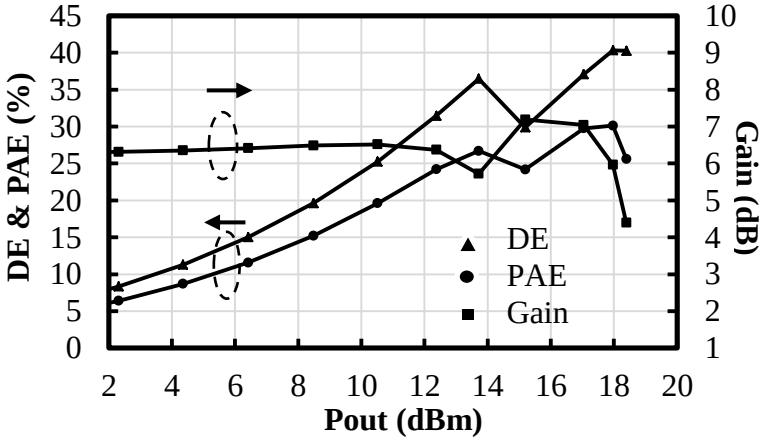


Figure 5.13. Simulated gain, DE and PAE of the Doherty PA with slow-wave CPW as a function of output power.

As was mentioned in Section V.B.II, the auxiliary amplifier should be totally *off* at back-off to achieve the best efficiency. One possible way to achieve this goal is

to bias the auxiliary amplifier in deep class C, which reduces the gain at high output power. To address the problem of the auxiliary amplifier turning on prematurely, adaptive biasing is evaluated. Adaptive biasing adjusts the bias of the auxiliary amplifier according to the input power as shown by the rule:

$$V_{g_{M3}} = \begin{cases} -0.2V & Pin < 8dBm \\ 0V & 8dBm < Pin < 10dBm \\ 0.2V & Pin > 10dBm \end{cases} \quad (5.18)$$

As a result of the adaptive biasing, the auxiliary amplifier is biased in deep class C at low input powers, therefore the back-off efficiency of the main amplifier is 7% higher than the case when the auxiliary amplifier is biased in class AB, as shown in Figure 5.14; at high input powers, the auxiliary amplifier is biased in class AB providing 2 dB higher gain than the case when it is biased in class C as shown in Figure 5.15.

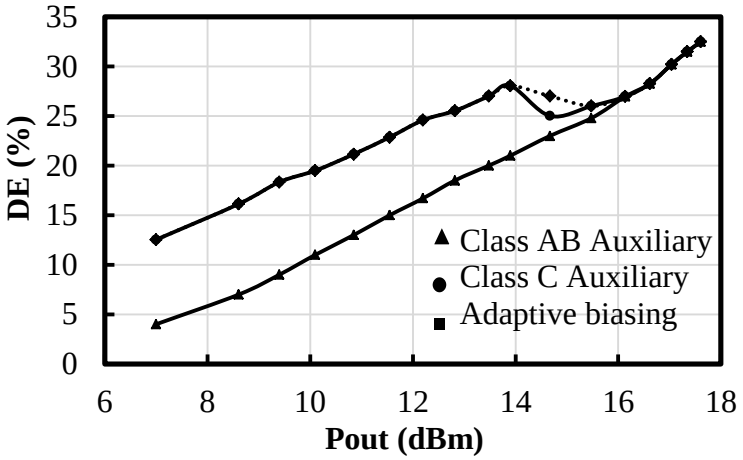


Figure 5.14. Simulation of the effect of adaptive biasing on DE of the circuit of Figure 5.10.

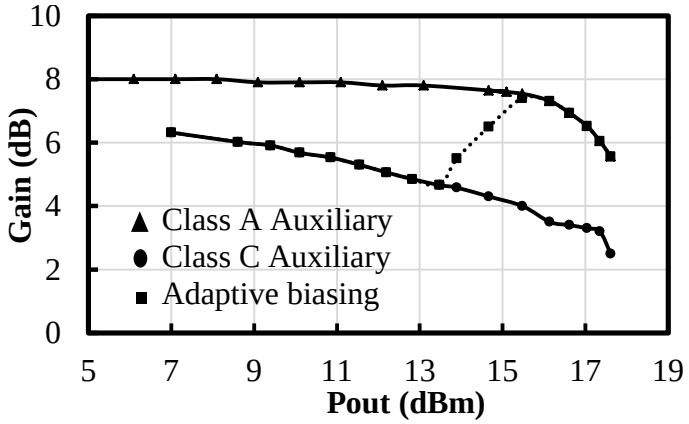


Figure 5.15. Simulation of the effect of adaptive biasing on gain of the circuit of Figure 5.10.

As explained in Section II-a, the transconductance of the auxiliary amplifier must be twice the transconductance of the main amplifier to achieve the best performance at peak output power. The bias voltages of the auxiliary amplifier shown in (5.23) are selected such that the transconductance criterion is met and efficiency is maximized. Simulation shows that changing V_{gM3} from 0.15V to 0.25V only changes the peak PAE by 2% indicating that the design is robust even if no calibration is done.

The other advantage of adaptive biasing is that the moment of switching *on* and *off* for the auxiliary amplifier is determined by the input power, making the system much less sensitive to threshold voltage variations. The drawback of using the adaptive biasing is complexity of the control and discontinuity in the gain characteristic of the PA shown in Figs. 5.12 and 5.13, which potentially degrades linearity. This will be investigated in future work.

V.E.II. Active Phase-Shift Doherty PA Design

The working principles of the active phase-shift Doherty have been introduced in Section V.C.

As was explained there, a preamplifier is utilized at the input of the auxiliary amplifier to increase the gain and provide the required phase-shift. Although this amplifier is *off* at low input power and has no effect on the back-off efficiency, its power consumption should be significantly lower than the DC power consumption of the auxiliary amplifier to avoid a significant degradation of the overall efficiency at high power. As is shown in Figure 5.16, the auxiliary amplifier is a two-stack PA with width of 256 μm and a 2.5 V power supply; therefore a CS amplifier with width of 128 μm and a 1.2 V power supply is utilized as a phase- shifting preamplifier.

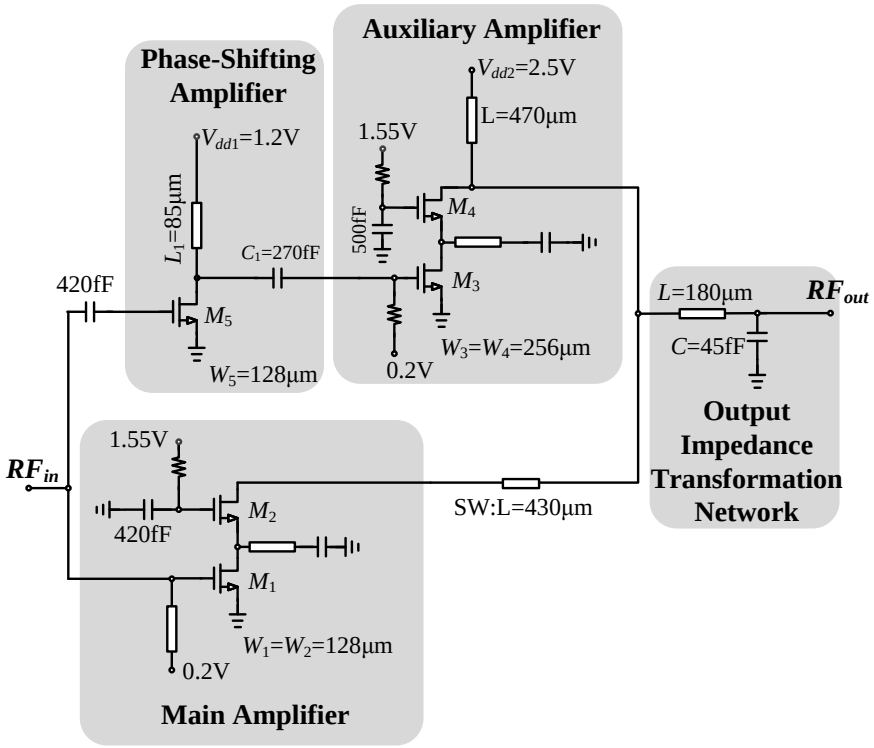


Figure 5.16. Schematic of the active phase-shift Doherty PA.

As discussed in Section V.D.I, adaptive biasing is utilized to maximize the efficiency and gain at back-off and peak power, respectively. However, adaptive biasing modifies the input capacitance of the auxiliary amplifier, changing the phase shift created by the phase-adjusting preamplifier according to (5.11). In this work, the pre-amplifier is tuned righto provide the correct phase-shift at peak power. Therefore the variation of C_{gs} due to dynamic biasing has no effect on peak efficiency and the phase shift error occurs only at low input powers. However, this will have a negligible effect on the overall efficiency at these power levels, since the output current of the auxiliary amplifier is significantly smaller than that of the main amplifier.

Simulations of the slow-wave Doherty show that the peak PAE occurs at 17.3 dBm P_{out} and d.c. power consumption of 165 mW, which corresponds to 33% DE. However, due to the higher gain of the active phase-shift Doherty, the peak PAE occurs at 18 dBm of P_{out} with a DE of 27%. This shows that the penalty of using the phase-shifting amplifier on the DE is approximately 5% at the peak PAE point.

Simulations confirms that the active phase-shift Doherty exhibits 1.2 dB higher gain at back-off than the traditional approach, which is attributed to the increased gain of the main amplifier due to the lower loss of the input network. Assuming identical DE of 32% at back-off power for both PAs, the 1.2 dB increase in the overall gain, translates into a PAE increase of roughly 3%.

Figure 5.17 shows the simulated gain, DE and PAE of the active phase-shift Doherty PA, which shows the gain increases by 1.5 dB at peak and back-off power and the PAE is also improved by 1% and 5% at peak and 6-dB back-off power

respectively. The total area of this PA is 20% smaller than the Doherty PA using the slow-wave CPW.

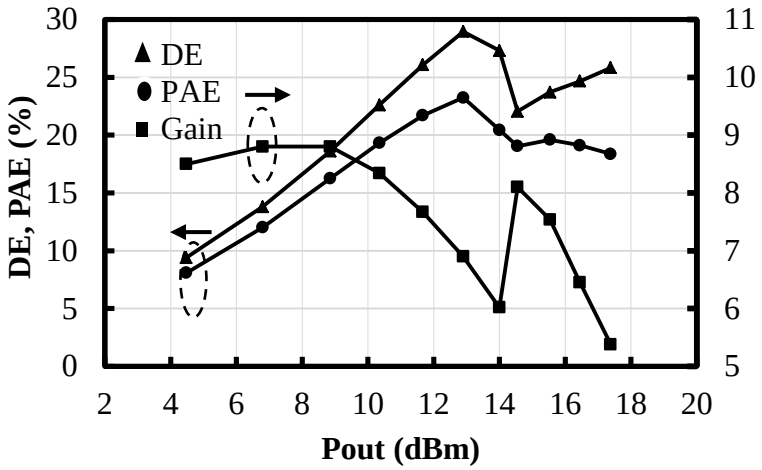


Figure 5.17. Simulated gain, DE and PAE of active phase-shift Doherty PA a as a function of output power.

V.F. Measurement Results and Comparison

The photomicrographs of the three Doherty PAs are shown in Figure 5.18. The active phase-shift Doherty PA, passive phase-shift Doherty PA with slow-wave CPW and the passive phase shift Doherty PA with ground shielded CPW occupies 0.45 mm^2, 0.64 mm^2 and 0.77 mm^2, which shows the advantage of the active phase-shift Doherty over the traditional Doherty design in terms of area.

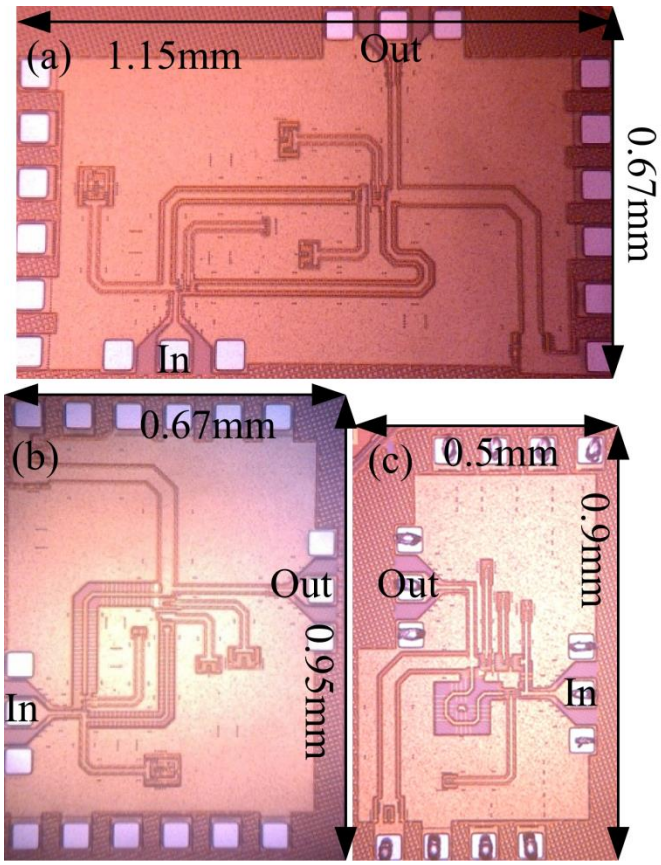


Figure 5.18. Photo micrograph of (a) Doherty PA with G-CPW (b) Doherty PA with S-CPW (c) active phase-shift Doherty.

All the results in this section are measured at 42 GHz for a 2.5 V supply. All the PAs have greater than 17.5 dBm saturated output power and there is a good agreement between simulation and measurement.

The measured and simulated gain, PAE, and drain efficiency of the passive phase-shift Doherty PA with ground-shielded CPWs are plotted in Figure 5.19 and Figure 5.20. It has 6-dB small-signal gain and it achieves 20% DE and 12% PAE at back-off. The low PAE at back-off is attributed to the drop in the gain of the PA. The DE and PAE of this PA at peak output power are 31% and 21% respectively.

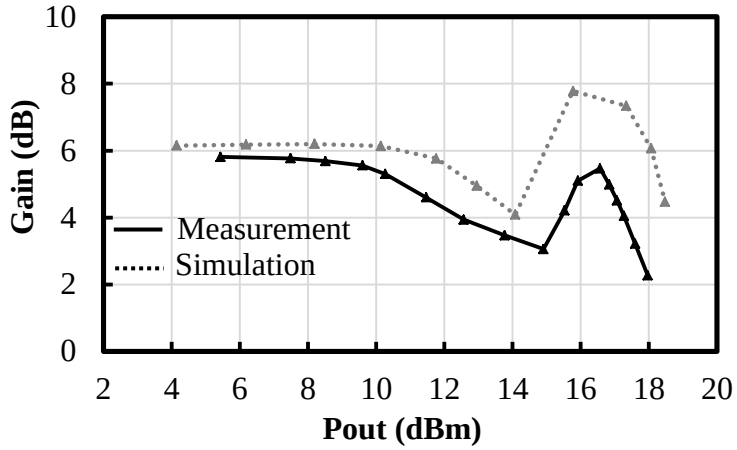


Figure 5.19. Gain as a function of output power of the Doherty PA with ground-shielded CPW.

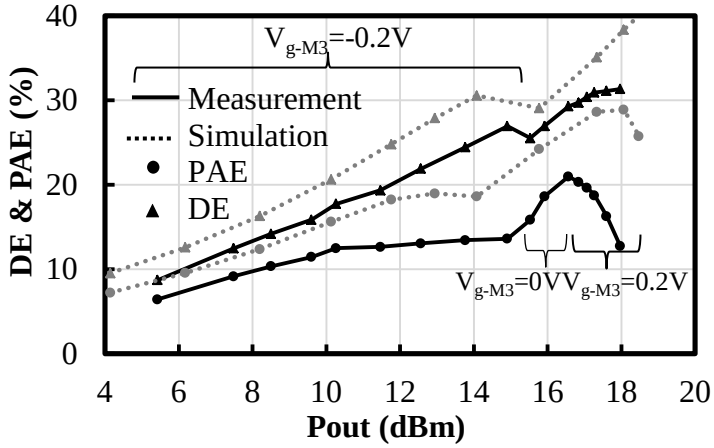


Figure 5.20. PAE and DE of the Doherty PA with ground-shielded CPW.

The measured and simulated gain, PAE and drain efficiency of the Doherty PA with slow-wave CPWs are plotted in Figs. 5.21 and Figure 5.22. It achieves 24% DE and 17% PAE at back-off, which is 4% and 5% higher than the ground- shielded CPW Doherty PA, demonstrating the benefit of the lower loss of the slow-wave transmission lines. The DE and PAE of the slow-wave CPW Doherty PA are 33% and

23% at peak output power, which is also 2% higher than the Doherty PA with ground-shielded CPW.

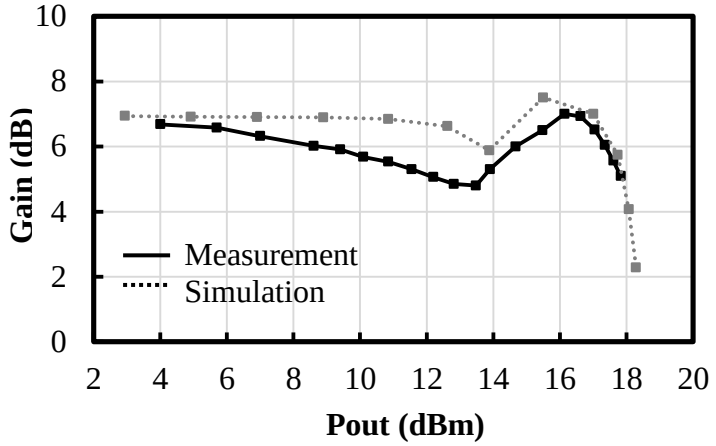


Figure 5.21. Gain as a function of output power of the Doherty PA with slow-wave CPW.

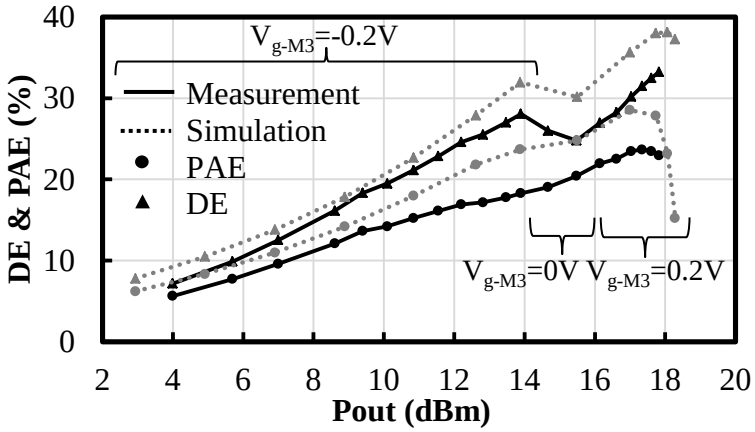


Figure 5.22. PAE and DE of the Doherty PA with slow-wave CPW.

The measured and simulated gain, PAE, and DE of the third design - the active phase-shift Doherty PA - are plotted in Figs. 5.23 and 5.24. It exhibits roughly 7.7 dB small-signal gain and it achieves 28% DE and 21% PAE at back-off. However, the *peak* PAE of the active phase-shift Doherty only reaches 20% which is 3% lower than the slow-wave Doherty and 1% lower than Doherty PA with ground-shielded CPW.

This is explained by the higher power consumption of this design, because of the additional phase-shifting amplifier.

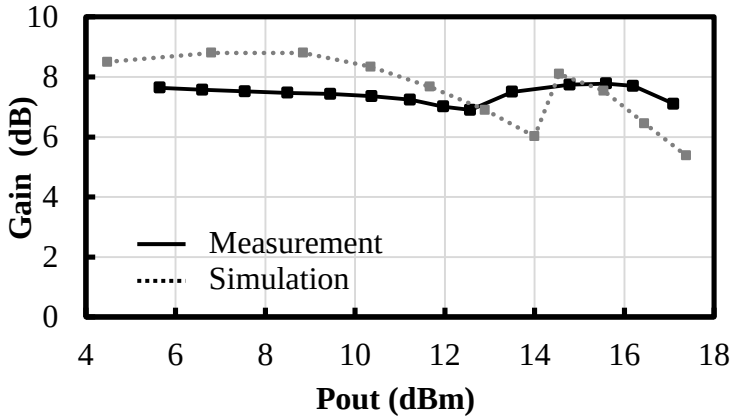


Figure 5.23. Gain as a function of output power of the active phase-shift Doherty PA.

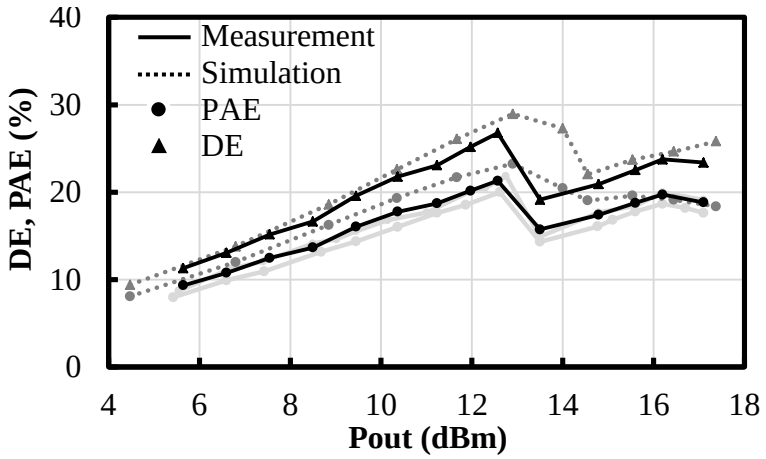


Figure 5.24. PAE and DE of the active phase-shift Doherty PA.

Figure 5.25 and Figure 5.26 compares the measured PAE and gain of all the three Doherty PAs, which demonstrates the advantage of the active phase-shift Doherty PA over the traditional designs.

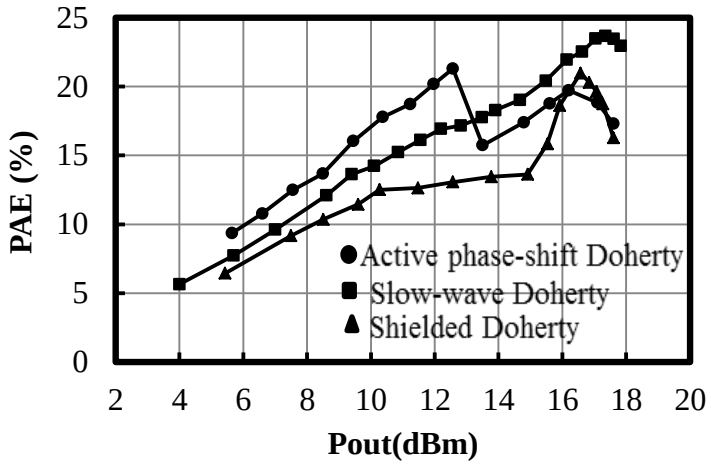


Figure 5.25. Comparison of the measured PAE of the three Doherty PAs.

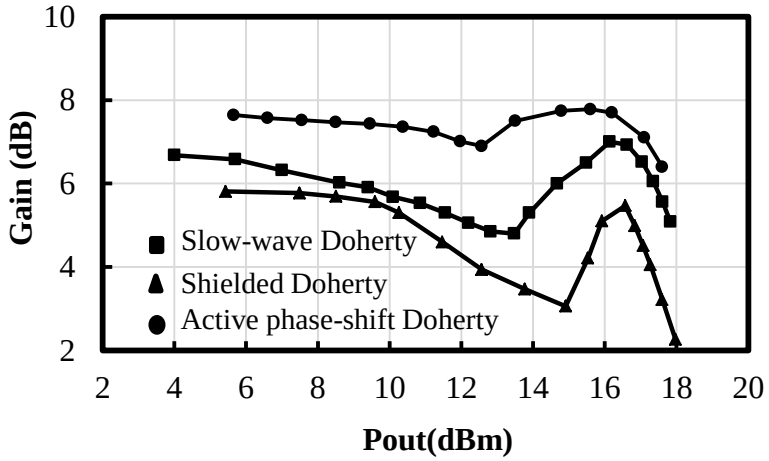


Figure 5.26. Comparison of the measured gain of the three Doherty PAs.

To ensure the reliable operation of the implemented PAs, each of them has been measured at 1-dB compression point with 2.5 V power supply for more than 3 hours and Figure 5.27 plots the measured gain as a function of time. No degradation is observed during this laboratory testing of the amplifiers.

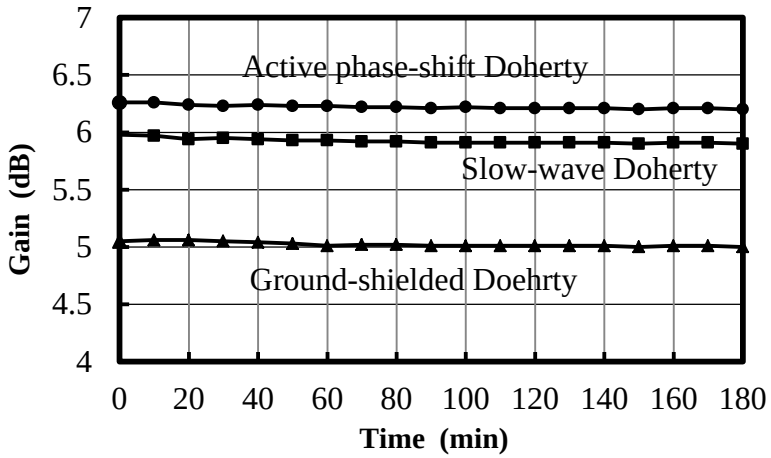


Figure 5.27. Measured gain at 1-dB compression point as a function of time for the three Doherty PAs.

Table 5.1.
Comparison to previous work.

References	Technology	Freq (GHz)	Supply (V)	Psat (dBm)	Peak PAE (%)	Back-off PAE(%)	Gain (dB)	Area (mm^2)
SW-CPW Doherty	45nm CMOS SOI	42	2.5	18	23	17	7	0.636
G-CPW Doherty	45nm CMOS SOI	42	2.5	18	21	12	6	0.77
Active phase-shift Doherty	45nm CMOS SOI	42	2.5 & 1.2	18	20	21	8	0.45
[52]	130nm MOS	60	1.6	7.8	3	1.5	13.5	1.8
[53]	GaAs HEMT	42	5	21.8	25	23	7	2
[54]	130nm Si-GE	60	4	23	6.4	2	13	0.256
[55]	65nm CMOS	53-68	1.8 - 1.2	18-17	5-3.1	2-1.1	14-16	0.462
[56]	65nm CMOS	60	1	17.9	11.1	4	19.2	0.83
[17]	130nm Si-Ge BiCMOS	60	1.8	20.1	18	7	20	0.72
[57]	90nm CMOS	55-71	3	18	12.2	3	26	0.64

Table 5.1 is a comparison of the three fabricated Doherty PAs in this work with other published results in the mm-wave frequency range. This work demonstrates the highest output power compared to all previous CMOS work as well as the highest efficiency for an amplifier operating under 6-dB back-off conditions.

V.G. Conclusion

In this Chapter, a traditional 45 GHz Doherty PA is designed with shielded CPWs in 45-nm SOI CMOS technology. To improve the performance and reduce the area, shielded CPWs are substituted with slow-wave CPW in a second PA, resulting in 20% smaller chip area, 1 dB more gain and 4% more PAE. Finally, an active phase-shift Doherty PA is proposed and implemented, which reduces the overall area by another 30% and increases the gain by 1.2 dB. At 6-dB back-off power, the active phase-shift Doherty achieves 21% PAE, which is 4% higher than the passive phase-shift Doherty amplifier with slow-wave CPW, and at the peak power, the PAE reaches 20%, which is 3% lower than the Doherty amplifier with slow-wave CPW. The Doherty PAs achievea saturated output power greater than 17.5 dBm.

Chapter 5, in part, is a reprint of material as it appears in "Multi-Drive Stacked FET Power Amplifiers at 90 GHz in 45-nm SOI CMOS," submitted to *IEEE Journal of Solid-State Circuits*. The authors are Amir Agah, Jefy Jayamon, Peter Asbeck, James Buckwalter and Lawrence Larson. The dissertation author is the primary author and investigator of this paper.

VI. Conclusion

Although the cut-off frequency of the highly scaled CMOS FETs permits mm-wave operation, low breakdown voltage of the FETs as well as the low quality factor of on-chip passive elements makes the power amplifier design a major bottleneck in the design of efficient mm-wave communication systems.

Previous work in mm-wave CMOS power amplifier design has been mainly focused on power combining techniques. However, designing a single efficient PA with high output power is critical for efficient power combining.

FET-stacking technique is investigated in detail in this research and shown to provide some major improvements in power amplifier design. The FET-stacking technique allows the use of a high voltage supply, which is n (number of stacked FETs) time the nominal drain-to-source breakdown voltage of FETs in the technology, hence increasing the output power without sacrificing reliability. Increasing the power supply voltage also increases the optimum load impedance for a given FET geometry required to achieve the highest output power and efficiency, lowering the quality factor of the output matching network and hence lowering the loss and improving the efficiency.

A stacked-FET power amplifier is designed and fabricated in 45nm SOI CMOS technology for 45 GHz operation, achieving 19dBm saturated output power with 34% PAE. A two-stack two-stage PA is also implemented for 90GHz with

15.6dBm saturated output power and 11% PAE, showing that stacking FETs provides fewer advantages as the operating frequency approaches the cut-off frequency of the FETs. A detailed analysis of the stacked-FET PA is provided in this research, showing that the gate resistance of the FETs and low quality factor of the capacitors are the key performance limiting factors in the design of the W-band PAs.

We proposed the multi-drive technique to overcome this limitation. In multi-drive stacked-FET PA, all the FETs in the stacked-FET PA are driven, keeping the ac current swing constant in the stacked-FET PA. Therefor the output power increases linearly by increasing the number of stacked FETs. Assuming that all the FET in the stack are identical, the power required to drive all stage are identical and therefore the power gain of the multi-drive stacked PA remains identical to the power gain of a common source PA with identical geometry.

A multi-drive stacked-FET PA is implemented in 45nm SOI CMOS for 90GHz operation, achieving more than 19.2dBm saturated output power with 14% PAE.

To show the capability FET-stacking technique to prove high data rates and high output powers, we have proposed and implemented a 45GHz digital-to-RF converter in 45nm SOI CMOS. In the proposed digital to RF converter a four-bit pseudo differential IQ DAC and an IQ mixer and a PA are stacked on top each other to achieve the best efficiency. The proposed design achieves more than 21dBm saturated output power and generates a 1.2Gbps QPSK signal with 4.4% EVM using digital predistortion.

Constant envelope modulations has always been popular for efficiency considerations. However the growing cost of the frequency spectrum and demand for

high data rates mandates the use of more complex modulation schemes with higher PAPRs, making it more important to design PAs with high efficiency at back-off powers. The Doherty power amplifier is one approach that provides maximum efficiency at back-off output power as well as the peak power.

A Doherty PA is made of two power amplifiers – main and auxiliary- and two quarter-wavelength transmission lines. Considering the 45GHz operating frequency the quarter-wavelength transmission line is only 800μm, allowing the fully integrated implementation of the Doherty PA. In this work, two fully integrated Doherty PAs are implemented in 45nm SOI CMOS for 45GHz operation, using grounded CPW and slow-wave CPW, achieving more than 18dBm saturated output power with 21% and 25% peak PAE, respectively. Use of slow-wave CPW is shown to improve the peak efficiency by 4% and reduce the area footprint of the fully integrated Doherty PA by about 20%. The Doherty PA with slow-wave CPW demonstrates about 18% PAE at back-off, 4% higher than the Doherty PA with ground-shielded CPW.

We have also proposed and implemented an active phase-shift Doherty PA, which created the required phase shift at the input of the auxiliary amplifier with a pre-amplifier, increasing the overall gain and back-off efficiency of the Doherty PA by 1.5dB and 4%, while reducing the overall area by more than 30% in comparison to the traditional Doherty PAs designed using slow-wave CPW.

Future work on the following topics to enhance the PA performance would be interesting:

- Power combining several multi-drive stacked-FET PAs using non-isolated power combiners to achieve watt level output powers in W-band regime.
- Analyzing the effect of multi-drive technique on the linearity of the stacked-FET power amplifiers.
- Study of the possibility of using multi-drive technique to increase the effective transconductance of the stacked-FET amplifier without sacrificing the reliability.

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