Title

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Modeling and Analysis of Switched-Capacitor Converters with Finite Terminal Capacitances

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Modeling and Analysis of Switched-Capacitor Converters with Finite Terminal Capacitances

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***Abstract*—In pre-existing analytical models of switched-capacitor (SC) converters, input and output capacitances (C_{in} and C_{out}) have long been neglected based on the assumption of input and output as ideal voltage sources. However, this paper reveals that, in practical applications, the terminal capacitances are usually not sufficiently large to ensure ideal input and output behavior and can have considerable effects on output impedance R_{out} and overall efficiency. To quantitatively investigate their effects, this paper proposes a general modeling and analysis methodology for SC converters that is capable of considering the effects of finite C_{in} and C_{out}. The proposed model is verified by experimental measurements from a 2-to-1 SC converter prototype with less than 8% relative error. It is revealed that the insufficiency of C_{in} can lead to a considerable increase in R_{out} and thus harms overall efficiency. On the contrary, smaller C_{out} can help reduce R_{out}, although this benefit comes at the cost of larger output voltage ripple. In addition, C_{out} has stronger effects on R_{out} in the slow switching region, while C_{in} is more influential at higher switching frequency, especially around the knee of the R_{out} curve at which the converter usually operates. Several design guidelines are provided based on these findings.**

I. Introduction

Switched-capacitor (SC) converters have been demonstrated to achieve higher power density and more effective switch utilization compared with traditional magnetic-based converters [1]–[3] in various applications include consumer electronics [4], data center power delivery [5], and CMOS integrated power conversion [6], [7]. Although pre-existing analytical models [8]–[11] and analyses [2], [12]–[14] of SC converters assume input and/or output to be ideal voltage sources, as illustrated in Fig. 1(a), practical implementations of SC converters involve input and output capacitances (C_{in} and C_{out}) to stabilize the terminal voltages, as illustrated in Fig. 1(b).

Theoretically, if C_{in} and C_{out} are much larger than the flying capacitor (C_{fly}) (i.e. C_{in}, $C_{\text{out}} \geqslant 10C_{\text{fly}}$) the input and output can be regarded as ideal voltage sources. However, in practical applications, the sizes of C_{in} and C_{out} are constrained by cost and space, and thus usually not large enough to ensure ideal input and output behavior. Fig. 2 illustrates the simulated output impedance with different C_{in} and C_{out}.

Despite the considerable effects of C_{in} and C_{out} on output impedance, currently there is no existing model that is able to quantitatively characterize their effects. In converter design, the selection of C_{in} and C_{out} is mainly based on engineering experiences and trial and error. However, in integrated circuits such as CMOS converters where the die area is limited and

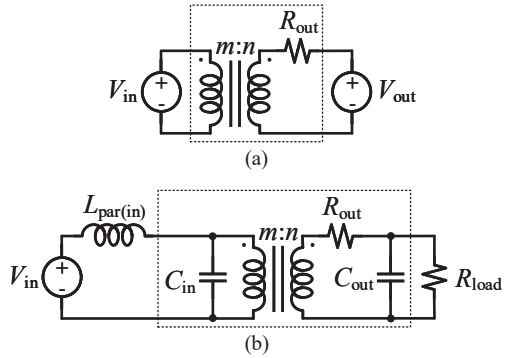


Fig. 1: General steady-state model of an SC converter. (a) Idealized input and output. (b) Practical input and output.

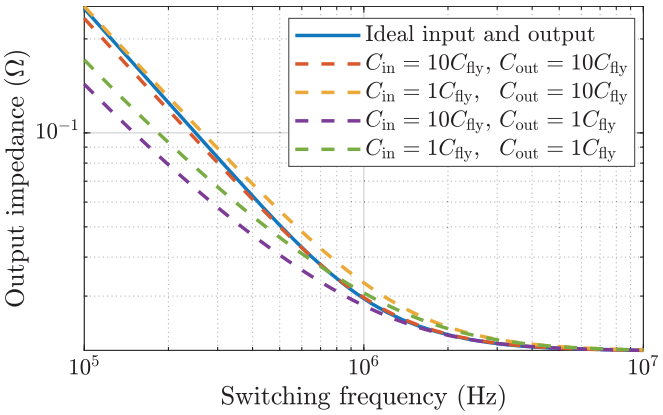


Fig. 2: Output impedance of a 2-to-1 SC converter with different C_{in} and C_{out}. ($C_{\text{fly}} = 10\mu$F, $R_{\text{ds(on)}} = 10$ mΩ)

valuable, quantitative optimizations should be performed to find out the best combination of the flying capacitances and terminal capacitances to achieve the lowest output impedance. This indicates the great need for a general analytical tool to analyze the effect of terminal capacitances.

In this paper, a general modeling and analysis methodology for SC converters is proposed to characterize the effects of finite C_{in} and C_{out}, with detailed model derivation provided in Section II. In Section III, a 2-to-1 SC converter prototype is specially designed to verify the proposed model and the modeling results agree well with experimental measurements with less than 8% relative error. To facilitate analysis, the proposed model is approximated with Taylor expansion in Sec-

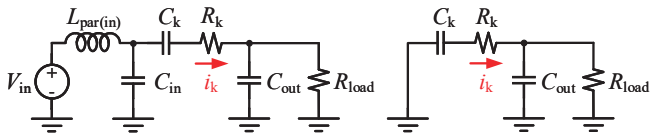


Fig. 3: Complete circuit model of an SC converter with finite C_{in} and C_{out}. (a) Case 1: the input terminal is connected to the source. (b) Case 2: the input terminal is grounded.

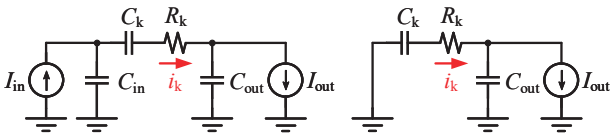


Fig. 4: Simplified circuit model of an SC converter with finite C_{in} and C_{out}. (a) Case 1: the input terminal is connected to the source. (b) Case 2: the input terminal is grounded.

tion IV-A to obtain a simpler and more intuitive mathematical form. Based on the proposed model and effect analysis, it is revealed in Section IV-B that the insufficiency of C_{in} can lead to a significant decrease in overall efficiency, while smaller C_{out} can actually help reduce output impedance and achieve higher efficiency, although this benefit comes at the cost of larger output voltage ripple. Based on the above findings, Section IV-C provides several design guidelines.

II. General Output Impedance Model of SC Converters With Finite Terminal Capacitances

In a general circuit state (or phase) k, an SC converter can be modeled as the equivalent circuit shown in Fig. 3 consisting of an equivalent resistance R_k and an equivalent capacitance C_k connected in series. Note that this general expression can capture any arbitrary SC topology, with suitable (topology-dependent) R_k and C_k values [9]. With nonideal input, two cases should be considered. Figs. 3(a) and (b) illustrate the equivalent circuits when the input terminal is connected to the source and when it is grounded, respectively.

Due to the existence of the parasitic inductance $L_{par(in)}$ (e.g. the parasitic inductance on the source cable) and the stable output voltage, it can be assumed that the ripples on the input and output currents are sufficiently small to be ignored. Therefore, for simplicity (and as conventionally done in topology analysis), the source and load are regarded as constant current sources I_{in} and I_{out}. Based on this assumption, the second-order complete circuit model shown in Fig. 3 can be simplified as the first-order model illustrated in Fig. 4.

In phase k of the first-order simplified circuit model shown in Fig. 4, the current through R_k can be expressed as

$$i_k(t) = (I_{0k} - I_{fk})\, e^{-\frac{t}{\tau_k}} + I_{fk} \tag{1}$$

where I_{0k} and I_{fk} are the initial value and forced component of i_k in phase k, and τ_k represents the time constant of the equivalent circuit. τ_k and I_{fk} can be expressed as

$$\begin{cases} \tau_k = R_k C_{k(eff)} \\ I_{fk} = p_k I_{out} \end{cases} \tag{2}$$

in which $C_{k(eff)}$ is the effective capacitance and p_k is a dimensionless ratio. In the two cases illustrated in Fig. 4, for an m-to-n SC converter, $C_{k(eff)}$ and p_k can be given as

$$\begin{aligned} \text{Case 1}: & \begin{cases} C_{k(eff)} = 1 \Big/ \left(\dfrac{1}{C_k} + \dfrac{1}{C_{in}} + \dfrac{1}{C_{out}} \right) \\ p_k = \dfrac{C_{k(eff)}}{C_{in} C_{out}} \left(C_{in} + \dfrac{n}{m} C_{out} \right) \end{cases} \\ \text{Case 2}: & \begin{cases} C_{k(eff)} = 1 \Big/ \left(\dfrac{1}{C_k} + \dfrac{1}{C_{out}} \right) \\ p_k = \dfrac{C_{k(eff)}}{C_{out}} \end{cases} \end{aligned} . \tag{3}$$

Since the resistive output impedance R_{out} accounts for all conduction losses in the SC converter, it can be calculated with the average conduction loss P_{loss} as

$$R_{out} = \frac{P_{loss}}{I_{out}^2}. \tag{4}$$

Note that P_{loss} is the power loss averaged in one switching cycle and thus can be expressed with the summation of the energy losses over all phases as

$$P_{loss} = f_{sw} \sum_k E_k \tag{5}$$

where f_{sw} is the switching frequency and E_k represents the energy loss in phase k which can be expressed as

$$E_k = \int_0^{T_{k(eff)}} R_k i_k^2(t)\, dt \tag{6}$$

in which $T_{k(eff)}$ is the effective duration of the phase k. Since there is no output inductor in SC converters that forces a freewheeling state during the deadtime, the effective duration $T_{k(eff)}$ can be calculated as

$$T_{k(eff)} = T_k - t_d \tag{7}$$

where T_k is the duration of phase k and t_d is the deadtime.

Substituting (1)-(3) and (5)-(7) into (4) yields

$$R_{out} = \hat{R}_{out} + \sum_k R_k p_k \left(2a_k - p_k f_{sw} T_{k(eff)} \right) \tag{8}$$

where

$$\begin{cases} \hat{R}_{out} = \dfrac{1}{2 f_{sw}} \sum\limits_k \dfrac{\hat{a}_k^2}{C_{k(eff)}} \coth\left(\dfrac{T_{k(eff)}}{2\tau_k} \right) \\ \hat{a}_k = a_k - p_k f_{sw} T_{k(eff)} \end{cases} \tag{9}$$

in which a_k is the ratio of the transferred charged in phase k to the total delivered charge in a switching cycle. The detailed derivation of (8) is provided in Appendix A. The definition and calculation of a_k can be found in [8].

With ideal input and output, $C_{k(eff)}$ and p_k become

TABLE I: Component List of the 2-to-1 SC converter prototype

Component	Part number	Parameters
GaN HEMT Q_1-Q_4	GaN Systems GS61004B	100 V, 16 mΩ (@ 25 °C)
Current sense resistor R_{CS1}-R_{CS4}	KOA Speer SLN5TTEDR200D	200 mΩ, 7 W, 75 PPM/°C
Flying capacitor C_{fly}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μF ×8
Input and output capacitors C_{in} and C_{out}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μF ×2-×40*
Gate driver	Analog Devices LTC4440	80 V, high-side
LDO voltage regulator	Texas Instruments LP2985AIM5-6.1/NOPB	2.5-16 V input, 6.1 V output
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky diode

* Measurements are performed with various terminal capacitances.

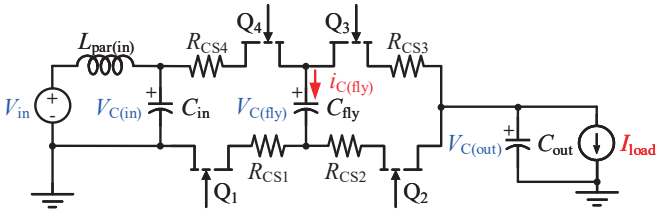


Fig. 5: Schematic of the 2-to-1 SC converter prototype.

$C_{k(eff)} = C_k$ and $p_k = 0$, so that

$$R_{out} = \hat{R}_{out} = \frac{1}{2f_{sw}} \sum_k \frac{a_k^2}{C_k} \coth\left(\frac{T_{k(eff)}}{2\tau_k}\right) \quad (10)$$

which is the same as has been derived in [11].

III. Model Verification

To verify the accuracy of the proposed general model, we compare the modeling results with circuit simulations and experimental measurements from a 2-to-1 SC converter. This verification also serves as an application example to demonstrate the effect of finite terminal capacitances on the output impedance of SC converters.

A. Experimental Setup

Figs. 5 and 6 show the schematic and photograph of the 2-to-1 SC converter prototype designed for model verification, with main components listed in Table I. The input and output voltages are measured with digital multimeters Keysight 34405A and 34401A, respectively, and the load current I_{load} is measured by the E-load Rigol DL3031.

B. Experiment Design Considerations

For the 2-to-1 SC converter, the topology-dependent parameters in (8) can be given as $C_k = C_{fly}$, $R_k = 2\left(R_{ds(on)} + R_{CS}\right) + ESR_{C(fly)}$, $a_k = \frac{1}{2}$, and $T_k = \frac{1}{2f_{sw}}$ $(k = 1, 2)$, where C_{fly} is the flying capacitance, $R_{ds(on)}$ is the on-resistance of switches Q_1-Q_4, R_{CS} is the resistance of current sense resistors R_{CS1}-R_{CS4}, and $ESR_{C(fly)}$ is the ESR of C_{fly}. The reason why R_{CS1}-R_{CS4} are added in series with the GaN switches will be explained below.

There are two key considerations to ensure effective model verification:

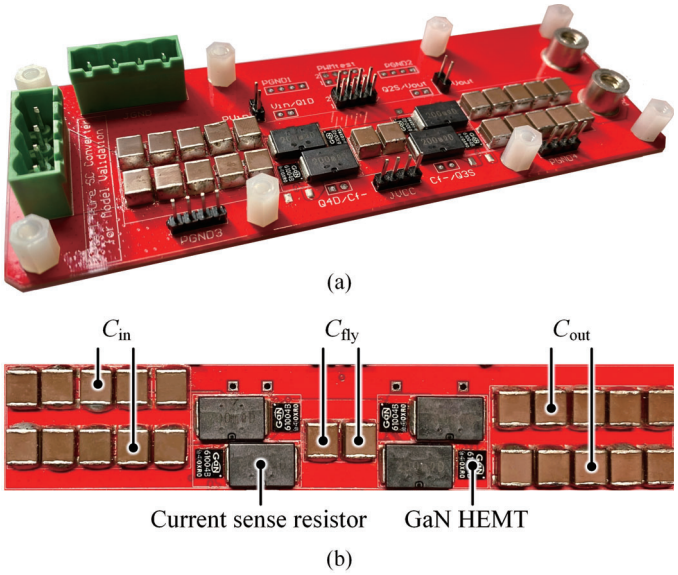
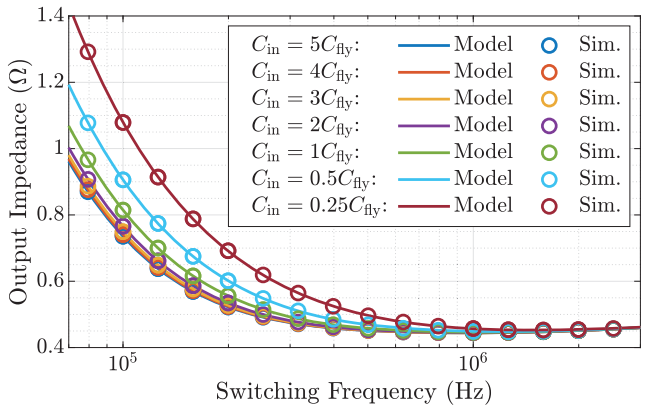


Fig. 6: Photograph of the 2-to-1 SC converter prototype. (a) Overall view. (b) Top view with key components annotated.

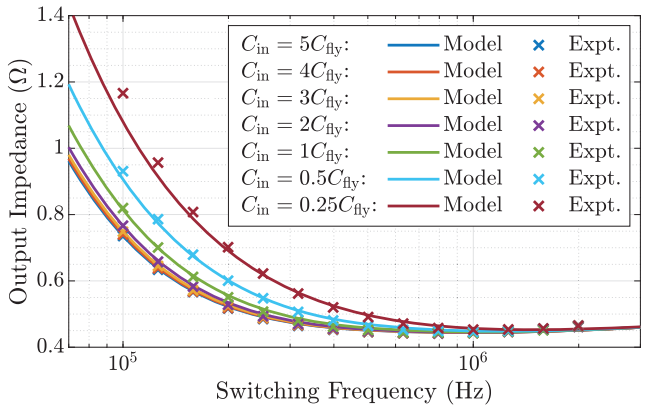
1) Ensure accurate parameter acquisition. The precision of the predicted results relies on not only the correctness of the model itself but also the accuracy of the parameters used in the model. Therefore, to verify the proposed model, we should ensure that the circuit parameters can be accurately acquired from the component datasheets and will not deviate from the nominal values in practice due to temperature variation, voltage bias, etc. The model parameters that are prone to variation can be classified into two categories: a) capacitances: C_{fly}, C_{in}, and C_{out}, and b) resistance: $R_{ds(on)}$ and $ESR_{C(fly)}$.

To minimize the variation of capacitances, we select the Class 1 capacitor with C0G dielectric KEMET C2220C474J5GACTU which features high capacitance stability over wide range of operating temperature and voltage bias, and extremely low ESR and ESL (i.e. $ESR_{C(fly)} \approx 0$).

Generally speaking, the $R_{ds(on)}$ of switching devices exhibits large variation under different operating conditions (e.g. junction temperature, drain-to-source current, gate-to-source voltage, etc.). The need of fast switching at MHz to reach the fast switching limit (FSL) with low switching loss necessitates the use of GaN switches. However, this further worsens the $R_{ds(on)}$ instability issue due to GaN HEMT's dynamic



(a)



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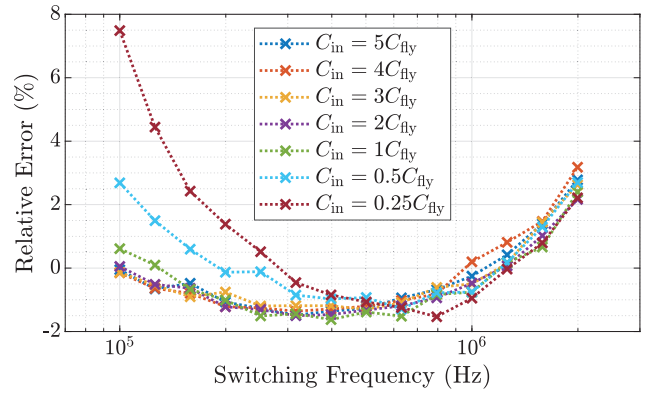
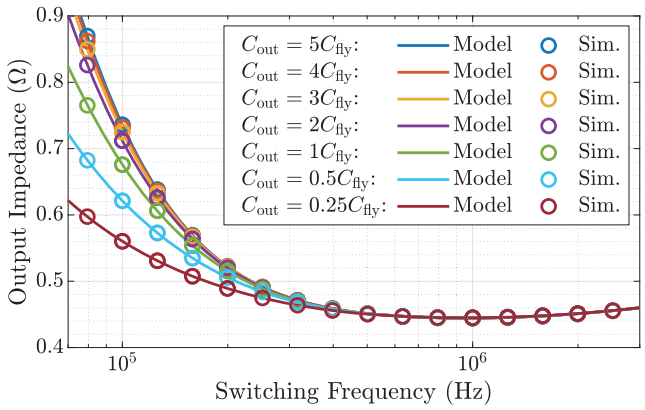
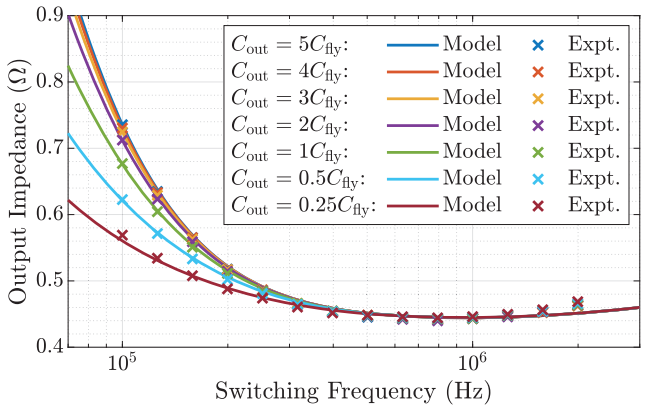


(c)

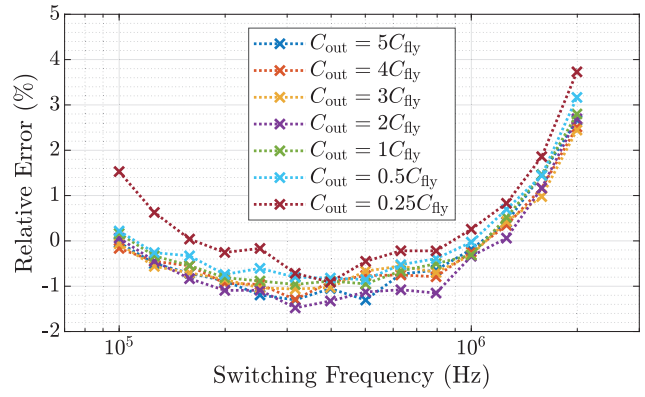
Fig. 7: Output impedance of the SC converter with various C_{in}. ($C_{\text{out}} = 5C_{\text{fly}}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated by PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.). (c) Relative error of modeling results with respect to experimental measurements calculated with (11).



(a)



(b)



(c)

Fig. 8: Output impedance of the SC converter with various C_{out}. ($C_{\text{in}} = 5C_{\text{fly}}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated by PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.). (c) Relative error of modeling results with respect to experimental measurements calculated with (11).

$R_{\text{ds(on)}}$ [15] that is hard to accurately capture. To address this problem, we add a high-precision current sense resistor KOA Speer SLN5TTEDR200D with high thermal stability (75 PPM/°C) in series with each GaN switch. Since R_{CS} =200 mΩ is much higher than the nominal $R_{\text{ds(on)}}$ =16 mΩ (@ 25 °C) of the GaN switch, R_{CS} will be able to dominate R_{k}, thus stabilizing it against the variation in $R_{\text{ds(on)}}$. Additionally, to minimize the $R_{\text{ds(on)}}$ variation resulting from the change in the drive voltage V_{drive}, we select the cascaded bootstrap circuit with LDOs [16] that can ensure stable V_{drive} to power

the gate drivers of the GaN switches.

2) Minimize the proportion of switching loss. Since the calculated output impedance accounts for only the conduction loss in the converter excluding the switching loss, it is necessary to ensure that the converter is conduction-loss-dominant under the designed operating condition. On the other hand, the converter has to operate at MHz to reach FSL. Due to this consideration, GaN switches with low switching loss and gate charge are used, and the external gate resistance is set to be 0 Ω to minimize the switching transition time.

In addition, the input voltage $V_{\rm in}$ and load current $I_{\rm load}$ should be carefully chosen. To minimize the switching loss, we should choose relatively low $V_{\rm in}$ since higher $V_{\rm in}$ can lead to both higher output capacitance ($C_{\rm oss}$) loss and overlap loss. As for $I_{\rm load}$, it should be sufficiently high to make conduction loss dominant, but we still want it to be relatively low since lower $I_{\rm load}$ means lower heat generation and smaller temperature rise of the board, thus helping stabilize circuit parameters mentioned above. In this experiment, the test condition is chosen as $V_{\rm in} = 24$ V and $I_{\rm load} = 1$ A.

C. Experimental Results

Figs. 7 and 8 present the comparison between the output impedances predicted by the proposed model (Model), simulated by PLECS (Sim.), and measured from the prototype (Expt.) with various $C_{\rm in}$ and $C_{\rm out}$. To quantitatively evaluate the accuracy of the proposed model, we calculate the relative error of modeling results with respect to experimental measurements as

$$\text{Relative error} = \frac{R_{\rm out(Model)} - R_{\rm out(Expt.)}}{R_{\rm out(Expt.)}} \times 100\% \quad (11)$$

where $R_{\rm out(Model)}$ and $R_{\rm out(Expt.)}$ are the $R_{\rm out}$ predicted by the model and measured from the prototype, respectively.

As can be observed in Figs. 7 and 8, the modeling results agree well with circuit simulations and experimental measurements for various $C_{\rm in}$ and $C_{\rm out}$ within 100 kHz-2 MHz switching frequency range, covering the slow switching limit (SSL) and FSL. The relative error of modeling results with respect to experimental measurements is less than 8%. This indicates that the proposed general model is able to accurately predict the output impedance of the SC converter with arbitrary terminal capacitance values and is applicable in a wide range of switching frequency.

The rise in relative error when the switching frequency increases is caused by the increase in switching loss. The high relative error in the small $C_{\rm in}$ cases at low $f_{\rm sw}$ results from the undesired oscillation between $L_{\rm par(in)}$ and $C_{\rm in}$.

IV. Effect Analysis of Terminal Capacitances

With the general model derived and verified in Sections II and III, we can now use it to explore the effect of the terminal capacitances on the output impedance of SC converters.

A. Model Approximation by Taylor Expansion

Although accurate and widely applicable, the output impedance model given in (8) can be too complex to provide intuitive engineering insight due to the existence of the hyperbolic function $\coth(x)$. Therefore, we first approximate (8) by Taylor expansion to obtain a simplified mathematical form. Inspired by the concepts of SSL and FSL [8], we also perform model approximation in slow and fast switching regions separately, and name the obtained models as *slow switching model (SSM)* and *fast switching model (FSM)*, respectively.

Similarly, here we take the 2-to-1 SC converter in Section III as an example, but note that the same approximation technique is also applicable to other SC topologies. For simplicity, we set $R_{\rm CS}$ =0 Ω and assume negligible capacitor ESR and deadtime $t_{\rm d}$. In the following examples, $C_{\rm fly} = 10\mu$F, $R_{\rm ds(on)}$ =10 mΩ.

By Taylor expansion, (8) for the 2-to-1 SC converter can be approximated as

$$\begin{cases} R_{\rm SSM} = \left(b + \dfrac{c}{s}\right) R_{\rm ds(on)}, & s < s_{\rm c} \\ R_{\rm FSM} = \left(2 + \dfrac{d}{s^2}\right) R_{\rm ds(on)}, & s \geqslant s_{\rm c} \end{cases} \quad (12)$$

where

$$\begin{cases} s = 8 f_{\rm sw} R_{\rm ds(on)} C_{\rm fly},\ s_{\rm c} = \dfrac{1 + k_{\rm in}/2\ + k_{\rm out}}{\sqrt{3}} \\ k_{\rm in} = \dfrac{C_{\rm fly}}{C_{\rm in}},\ k_{\rm out} = \dfrac{C_{\rm fly}}{C_{\rm out}} \\ b = 2 - \dfrac{(1 + k_{\rm in}/2\ )^2}{(1 + k_{\rm in} + k_{\rm out})^2} - \dfrac{1}{(1 + k_{\rm out})^2} \\ c = \dfrac{(1 + k_{\rm in}/2\ )^2}{1 + k_{\rm in} + k_{\rm out}} + \dfrac{1}{1 + k_{\rm out}} \\ d = \dfrac{(1 + k_{\rm in}/2\ )^2 + 1}{3} \end{cases} \quad (13)$$

in which s is a dimensionless product of $f_{\rm sw}$ and $R_{\rm ds(on)}C_{\rm fly}$ time constant and thus defined as the normalized switching frequency, $s_{\rm c}$ is the critical normalized frequency that marks the boundary between SSM and FSM, and $k_{\rm in}$ and $k_{\rm out}$ are the ratios of $C_{\rm fly}$ to $C_{\rm in}$ and $C_{\rm out}$, respectively. The detailed derivation of (12) is given in Appendix B.

In the slow switching region where complete charge transfer can be ensured, $s \ll 1$ and therefore yields the SSL as (14). When the switching frequency is sufficiently high so that the current through $C_{\rm fly}$ is almost constant in each phase, $s \gg 1$ and therefore yields the FSL as (14).

$$\begin{cases} R_{\rm SSM} \approx R_{\rm SSL} = \dfrac{c}{s} R_{\rm ds(on)}, & s \ll 1 \\ R_{\rm FSM} \approx R_{\rm FSL} = 2R_{\rm ds(on)}, & s \gg 1 \end{cases} . \quad (14)$$

With ideal input and output, $k_{\rm in}$ and $k_{\rm out}$ are approximately zero so that we get $R_{\rm SSL} = \frac{1}{4C_{\rm fly} f_{\rm sw}}$ and $R_{\rm FSL} = 2R_{\rm ds(on)}$, which is expected and well-known.

B. Effect of Terminal Capacitances

In this section, we first evaluate (12) to analyze the effect of terminal capacitances qualitatively, then perform quantitative analysis with numerical calculations, and finally explore the physical origins for these effects with circuit simulations.

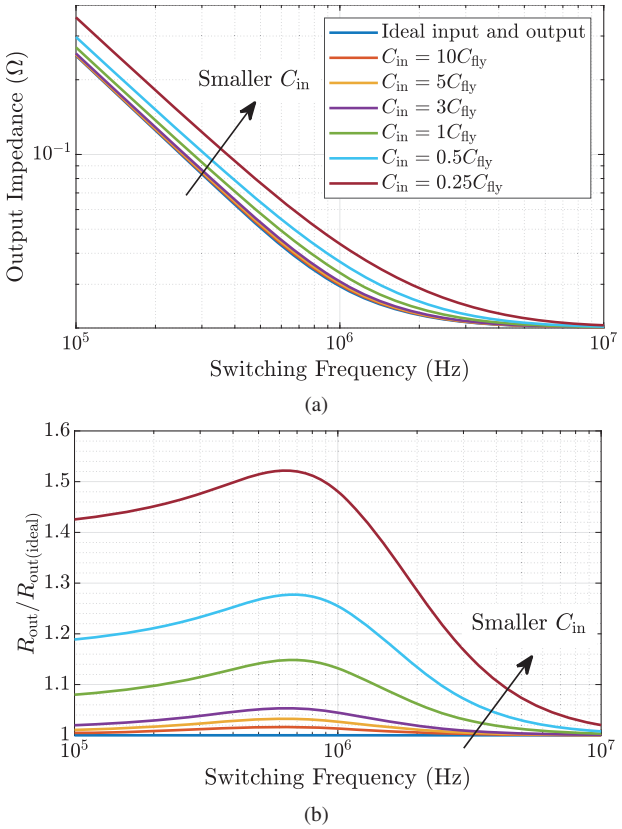


Fig. 9: Effect of C_{in} on output impedance. (Assuming ideal output) (a) R_{out} with various C_{in}. (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{\text{out(ideal)}}$.

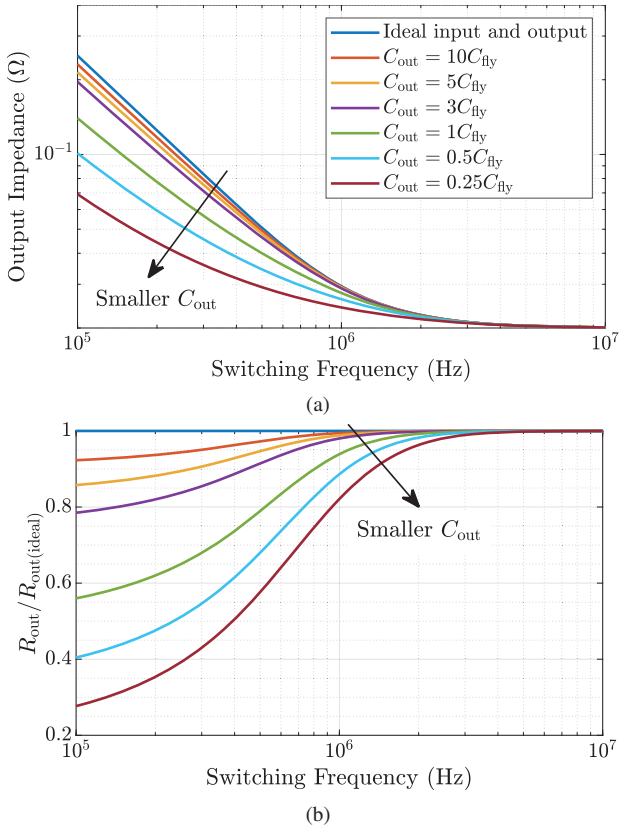


Fig. 10: Effect of C_{out} on input impedance. (Assuming ideal output) (a) R_{out} with various C_{out}. (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{\text{out(ideal)}}$.

1) Qualitative analysis. In the SSM of (12), c/s is dominant. When C_{in} becomes smaller, k_{in} increases so that c becomes greater, resulting in higher R_{SSM}. Conversely, with smaller C_{out}, k_{out} increases so that c becomes smaller, contributing to lower R_{SSM}. It is favorable, although counter-intuitive, that smaller C_{out} actually helps reduce the output impedance because this will contribute to both higher power density and higher efficiency. But note that C_{out} should still be sufficient to satisfy the ripple constraint on output voltage.

As can be seen in the FSM, the coefficient d contains only k_{in} but no k_{out}, which indicates that C_{out} has little effect on R_{FSM}. By inspection, we can find out that the reduction in C_{in} will lead to an increase in R_{FSM}.

The above analyses can also be validated with the simulation and experimental results presented in Figs. 7 and 8.

2) Quantitative analysis. Figs. 9 and 10 quantitatively illustrate the effect of the terminal capacitances on R_{out}. It can be observed that the insufficiency of C_{in} leads to higher R_{out}, while smaller C_{out} contributes to lower R_{out}. Also, C_{out} has no influence on R_{out} in the fast switching region, while C_{in} exhibits greater effect in the high frequency region, especially around the knee of the R_{out} curve at which the SC converter usually operates. These findings are consistent with those from the qualitative analysis above and the simulation and experimental results presented in Figs. 7 and 8.

Furthermore, we can see that $C_{\text{in}} = 3C_{\text{fly}}$ is sufficient to approximate an ideal input. However, further reduction of C_{in} to C_{fly} or an even smaller value can cause significant increase in R_{out}, which harms efficiency. On the contrary, we always favor smaller C_{out}. Moreover, in the low frequency region, C_{out} is quantitatively more influential than C_{in}. By comparing Fig. 9(b) to Fig. 10(b), we can find that different C_{in} can cause only up to 50% increase in R_{out}, while the change in C_{out} can help decrease R_{out} by half or even more.

3) Physical origins. Fig. 11 presents the comparison between the simulated waveforms of the 2-to-1 SC converter with large and small C_{in}, assuming ideal output. As listed in Table II, the current through C_{fly} ($i_{\text{C(fly)}}$) has the same average value (half-cycle) if the output current is kept the same. But with smaller C_{in}, the voltage difference seen by C_{fly} ($V_{\text{C(in)}} - V_{\text{C(out)}} - V_{\text{C(fly)}}$) becomes much higher than that with larger C_{in}. This causes a surge in the peak value of $i_{\text{C(fly)}}$ in the case 1 of Fig. 4 and increases the RMS value of $i_{\text{C(fly)}}$, resulting in higher loss and higher output impedance.

Fig. 12 shows the similar comparison between large and small C_{out} cases, assuming ideal input. Likewise, the average $i_{\text{C(fly)}}$ is kept to be the same in all cases. However, as can be seen in Table III, with smaller C_{out}, the voltage across C_{out} ($V_{\text{C(out)}}$) is able to follow $V_{\text{C(fly)}}$ more rapidly in the case 2 of Fig. 4. This means that $i_{\text{C(fly)}}$ will drop faster and thus

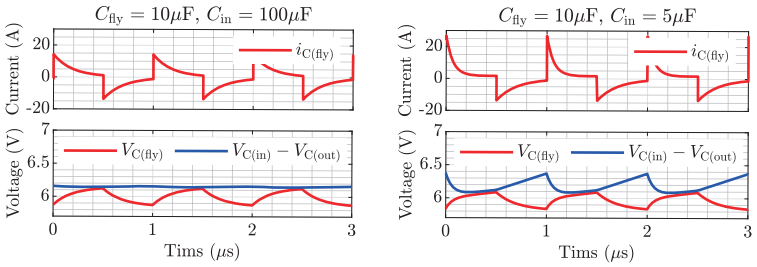


Fig. 11: Comparison of simulated waveforms between large and small C_{in} cases. (Assuming ideal output, $f_{\text{sw}} = 1$ MHz)

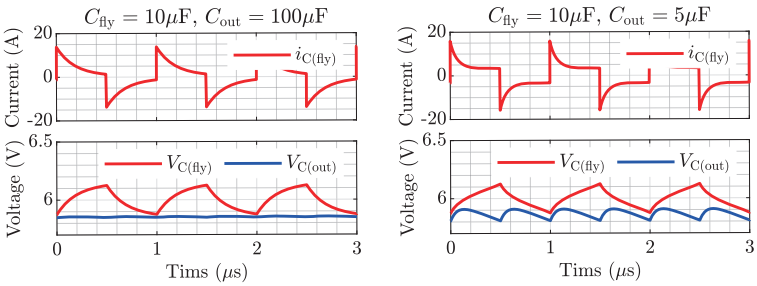


Fig. 12: Comparison of simulated waveforms between large and small C_{out} cases. (Assuming ideal input, $f_{\text{sw}} = 1$ MHz)

TABLE II: Comparison of the peak, average (half-cycle) and RMS values of the simulated $i_{\text{C(fly)}}$ waveforms between large and small C_{in} cases (Assuming ideal output, $f_{\text{sw}} = 1$ MHz)

$i_{\text{C(fly)}}$ \ C_{in}	100μF	30μF	10μF	5μF
Peak value	14.3A	15.8	20.1	26.7A
Average value	5.00A	5.00A	5.00A	5.00A
RMS value	6.12A	6.22	6.48	6.83A

TABLE III: Comparison of the peak, average (half-cycle) and RMS values of the simulated $i_{\text{C(fly)}}$ waveforms between large and small C_{out} cases (Assuming ideal input, $f_{\text{sw}} = 1$ MHz)

$i_{\text{C(fly)}}$ \ C_{out}	100μF	30μF	10μF	5μF
Peak value	13.8A	14.2	15.1	15.8A
Average value	5.00A	5.00A	5.00A	5.00A
RMS value	6.07A	6.02	5.90	5.73A

has lower RMS value, contributing to lower loss and output impedance.

C. Design Guidelines

- Size of C_{in}: Since the insufficiency of C_{in} will lead to an increase in R_{out} and harms overall efficiency, C_{in} should be sufficiently large to approximate the ideal input (at least $3C_{\text{fly}}$ in the 2-to-1 SC converter example analyzed in Section IV-B), especially considering the fact that C_{in} withstands higher voltage and thus can suffer from greater DC derating when Class 2 capacitors are used.
- Size of C_{out}: C_{out} can be appropriately reduced for both smaller physical size and lower R_{out} (i.e. higher power density and higher efficiency). Note that C_{out} should still be sufficiently large to satisfy the ripple constraint.

Further quantitative optimizations can be performed to find out the best combination of C_{in}, C_{out}, and C_{fly} to achieve the highest overall efficiency under a certain f_{sw} within the given voltage ripple constraints and total space limit.

V. Conclusions

This paper proposes a general modeling and analysis methodology that is able to characterize the effect of finite C_{in} and C_{out} on the output impedance of SC converters. A general output impedance model and its approximated form based on Taylor expansion is derived to facilitate analysis. It is revealed that larger C_{in} is favorable for efficiency improvement. On the contrary, smaller C_{out} can help reduce output impedance, which contributes to both higher efficiency and higher power density, although C_{out} should still be sufficiently large to satisfy the ripple constraint on output voltage. This work provides an analytical tool for future investigations such as design optimizations of SC converters with voltage ripple and physical volume constraints.

Appendix A
Derivation of the General Output Impedance Model

Denoting

$$\begin{cases} \hat{i}_{\text{k}}(t) = \hat{I}_{0\text{k}} e^{-\frac{t}{\tau_{\text{k}}}} \\ \hat{I}_{0\text{k}} = I_{0\text{k}} - I_{\text{fk}} \end{cases} \tag{15}$$

and

$$\hat{q}_{\text{k}} = \int_0^{T_{\text{k(eff)}}} \hat{i}_{\text{k}}(t)dt = \hat{I}_{0\text{k}}\tau_{\text{k}}\left(1 - e^{-\frac{T_{\text{k(eff)}}}{\tau_{\text{k}}}}\right). \tag{16}$$

Then

$$i_{\text{k}} = \hat{i}_{\text{k}} + I_{\text{fk}} \tag{17}$$

so that the transferred charge in phase k q_{k} can be calculated as

$$q_{\text{k}} = \int_0^{T_{\text{k(eff)}}} i_{\text{k}}(t)\,dt = \hat{q}_{\text{k}} + I_{\text{fk}} T_{\text{k(eff)}}. \tag{18}$$

On the other hand, q_{k} and I_{out} can be expressed as

$$\begin{cases} q_{\text{k}} = a_{\text{k}} q_{\text{out}} \\ I_{\text{out}} = f_{\text{sw}} q_{\text{out}} \end{cases} \tag{19}$$

where q_{out} is the total transferred charge to the output in a switching cycle.

Substituting (2) and (19) into (18) yields the relationship between $\hat{q}_{\text{k}}$ and q_{out} as

$$\hat{q}_{\text{k}} = \hat{a}_{\text{k}} q_{\text{out}} \tag{20}$$

in which the coefficient $\hat{a}_{\text{k}}$ has been given in (9).

Substituting (15) and (20) into (16) yields

$$\hat{I}_{0\mathrm{k}} = \frac{\hat{a}_{\mathrm{k}} q_{\mathrm{out}}}{\tau_{\mathrm{k}} \left(1 - e^{-\frac{T_{\mathrm{k(eff)}}}{\tau_{\mathrm{k}}}}\right)}. \tag{21}$$

Denoting

$$\hat{E}_{\mathrm{k}} = \int_0^{T_{\mathrm{k(eff)}}} R_{\mathrm{k}} \hat{i}_{\mathrm{k}}^2(t)\, dt = \frac{R_{\mathrm{k}} \hat{I}_{0\mathrm{k}}^2 \tau_{\mathrm{k}}}{2} \left(1 - e^{-\frac{2T_{\mathrm{k(eff)}}}{\tau_{\mathrm{k}}}}\right). \tag{22}$$

Then substituting (19) and (21) into (22) yields the expression of $\hat{R}_{\mathrm{out}}$ that has been given in (9) as

$$\hat{R}_{\mathrm{out}} = \frac{f_{\mathrm{sw}} \sum\limits_{k} \hat{E}_{\mathrm{k}}}{I_{\mathrm{out}}^2} = \frac{1}{2 f_{\mathrm{sw}}} \sum_{\mathrm{k}} \frac{\hat{a}_{\mathrm{k}}^2}{C_{\mathrm{k(eff)}}} \coth\left(\frac{T_{\mathrm{k(eff)}}}{2\tau_{\mathrm{k}}}\right). \tag{23}$$

Substituting (17) and (22) into (6) yields

$$E_{\mathrm{k}} = \hat{E}_{\mathrm{k}} + R_{\mathrm{k}} I_{\mathrm{fk}} \left(2\hat{q}_{\mathrm{k}} + I_{\mathrm{fk}} T_{\mathrm{k(eff)}}\right). \tag{24}$$

Additively combing (24) over all phases and substituting the summation into (4) and (5) yields the final expression of R_{out} that has been given in (8) as

$$\begin{aligned} R_{\mathrm{out}} &= \frac{f_{\mathrm{sw}} \sum\limits_{k} E_{\mathrm{k}}}{I_{out}^2} \\ &= \frac{f_{\mathrm{sw}} \sum\limits_{k} \hat{E}_{\mathrm{k}}}{I_{out}^2} + \frac{f_{\mathrm{sw}} \sum\limits_{k} R_{\mathrm{k}} I_{\mathrm{fk}} \left(2\hat{q}_{\mathrm{k}} + I_{\mathrm{fk}} T_{\mathrm{k(eff)}}\right)}{I_{out}^2} \\ &= \hat{R}_{\mathrm{out}} + \sum_{k} R_{\mathrm{k}} p_{\mathrm{k}} \left(2a_{\mathrm{k}} - p_{\mathrm{k}} f_{\mathrm{sw}} T_{\mathrm{k(eff)}}\right). \end{aligned} \tag{25}$$

Appendix B
Model Approximation by Taylor Expansion

By Taylor expansion, the hyperbolic function $\coth(x)$ $(x > 0)$ can be approximated as

$$\coth(x) \approx \begin{cases} \dfrac{1}{x} + \dfrac{x}{3}, & 0 < x \leqslant \sqrt{3} \\ 1, & x > \sqrt{3} \end{cases}. \tag{26}$$

For simplicity, here we consider a two-phase SC converter with 0.5 duty ratio and negligible deadtime (i.e. $T_{1(\mathrm{eff})} = T_{2(\mathrm{eff})} = \frac{1}{2f_{\mathrm{sw}}}$). Substituting (26) into the model (8) of this two-phase SC converter yields the contribution of phase k ($k = 1,\ 2$) to R_{out} as

$$\begin{cases} 2R_{\mathrm{k}} \left[p_{\mathrm{k}} \left(a_{\mathrm{k}} - \dfrac{p_{\mathrm{k}}}{4}\right) + \dfrac{\hat{a}_{\mathrm{k}}^2}{4 f_{\mathrm{sw}} \tau_{\mathrm{k}}}\right], & 0 < 4 f_{\mathrm{sw}} \tau_{\mathrm{k}} < \dfrac{1}{\sqrt{3}} \\ 2R_{\mathrm{k}} \left[a_k^2 + \dfrac{1}{3} \cdot \dfrac{\hat{a}_{\mathrm{k}}^2}{\left(4 f_{\mathrm{sw}} \tau_{\mathrm{k}}\right)^2}\right], & 4 f_{\mathrm{sw}} \tau_{\mathrm{k}} \geqslant \dfrac{1}{\sqrt{3}} \end{cases}. \tag{27}$$

Substituting the topology-dependent parameters mentioned in Section III-B and additively combing the components in all phases yields the SSM and FSM for the 2-to-1 SC converter that has been given in (12) and (13).

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