Sub-μV_{rms}-Noise Sub-μW/Channel ADC-Direct Neural Recording With 200-mV/ms Transient Recovery Through Predictive Digital Autoranging

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***Abstract*— Integrated recording of neural electrical potentials from the brain poses great challenges due to stringent dynamic range requirements to resolve small-signal amplitudes buried in noise amidst large artifact and stimulation transients, as well as stringent power and volume constraints to enable minimally invasive untethered operation. Here, we present a 16-channel neural recording system-on-chip with greater than 90-dB input dynamic range and less than 1-μV_{rms} input-referred noise from dc to 500 Hz, at 0.8-μW power consumption, and 0.024-mm^2 area per channel in a 65-nm CMOS process. Each recording channel features a hybrid analog–digital second-order oversampling analog-to-digital converter (ADC), with the biopotential signal coupling directly to the second integrator for high conversion gain and dynamic offset subtraction in the digital domain. This bypasses the need for high-pass filtering pre-amplification in neural recording systems, which often leads to signal distortion. The integrated ADC-direct neural recording offers record figure-of-merit with a noise efficiency factor (NEF) of the combined front end and ADC of 1.81, and a corresponding power efficiency factor (PEF) of 2.6. Predictive digital autoranging of the binary quantizer further supports rapid transient recovery while maintaining fully dc-coupled operation. Hence, the neural ADC is capable of recording ≤0.01-Hz slow potentials as well as recovering from ≥200-mV_{pp} transients within ≤1 ms that are important prerequisites to effective electrocortical recording for brain activity mapping. *In vivo* recordings from marmoset primate frontal cortex demonstrate its unique capabilities in resolving ultra-slow local field potentials indicative of subject arousal state.**

***Index Terms*— analog-to-digital converter (ADC)-direct front end, artifact recovery, autoranging, digital prediction, high dynamic range ADC, neural ADC, neural interfaces.**

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I. Introduction

HIGH-DENSITY multi-channel recording of neural electrophysiological signals, such as local field potentials (LFP) inside the brain and the electrocorticogram (ECoG) on the cortical surface, is essential to driving advances in neuroscience and neuroengineering, by increasing spatial resolution and dynamic range of brain–machine interfaces for high-throughput brain activity mapping and of neural prostheses for monitoring and treatment of neurological disorders. Great advances in spatial resolution and coverage of neural recording can be obtained by silicon integration of multi-channel brain–computer interfaces with high-density electrode arrays for electrical recording and stimulation [1] and their extreme miniaturization by encapsulating the electrode array along with a coil antenna for wireless power and data telemetry within a single mm-sized silicon chip [2]. Although the miniaturization of neural implants and their modular distribution across the brain toward full-brain coverage in high-resolution brain–machine interfaces offers various system-level advantages, such as better conformity to cortical curvature and a decrease in incidence of tissue inflammation, astroglial scarring, and cell death [3], [4], the extreme form factor and energy constraints raise severe challenges in signal quality of neural recording.

The limited amount of power delivery with an on-chip coil and multi-channel neural recording requires extreme energy efficiency in the design of neural recording without compromising its inherent design requirement, low input-referred noise (IRN) [5], [6] while also retaining small form factor in the design [7]–[9]. Full-duplex neural interfaces for closed-loop neural modulation require simultaneous operation of electrical recording and stimulation. Stimulation artifacts produce rapid and large-amplitude transients in the recorded signals that easily overwhelm the neural response signals, necessitating a paradigm shift in the design of neural recording toward very high input dynamic range and fast transient response [10].

To resolve small-amplitude neural signals, such as LFP and ECoG, ranging in the tens of microvolts, typical neural recording circuits include a high-gain, low-noise pre-amplification analog front-end (AFE) stage prior to digitization, as shown in Fig. 1(a) [11]. For low-noise operation, the AFE stage

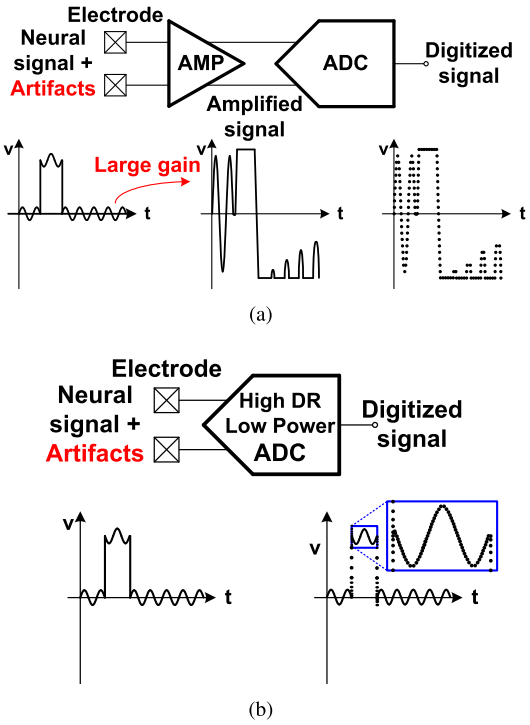


Fig. 1. Impact of neural recording architecture on dynamic range and transient response (a) separate AFE and ADC stages and (b) ADC-direct neural recording.

typically consumes substantially more power and area than the subsequent analog-to-digital converter (ADC) as the limiting factor in the energy efficiency and integration density of the overall system. Hence, most efforts in neural recording design have focused on optimizing the AFE. However, the separation between amplification and digitization stages for neural recording is prone to the saturation of the amplified signal under large transients caused by stimulation or motion artifacts. To this end, the latest designs use low-gain (18 dB) pre-amplification in the AFE to mitigate saturation effects [12].

Hybrid architectures utilizing oversampling ADCs with digital feedback to the AFE [8], [10] have seen recent adoption due to their increased power and area efficiency. Recent integrated designs combining AFE and ADC in one stage [9] offer further improvements in integration density and expanded input dynamic range. The challenge with previous ADC-direct approaches, however, is the kT/C sampling noise directly entering the signal path without attenuation, degrading noise-energy efficiency.

To address the confluence of these extreme design challenges for high-density integrated neural recording, a new ADC-direct approach is presented that combines a hybrid analog/digital second-order oversampling ADC with predictive digital autoranging (PDA) for high input dynamic range and rapid transient recovery at record noise-energy efficiency [13]. kT/C sampling noise is avoided altogether through boxcar sampling [14], [15] in mixed-signal feedback [8], while PDA avoids the need for substantial gain attenuation in the feedback loop leading to enhanced signal resolution at higher frequencies. PDA specifically addresses the problem of fast recovery from artifact and stimulation *transients*, by temporarily relaxing resolution through radix-2 expansion of the quantization step size to track large transient slope and rapidly returning to minimum quantization step noise-limited resolution upon transient completion. Applicable to a wide range of electrophysiological recording applications, the biopotential ADC (BioADC) chip resolves small signals while handling large input transients without saturation, as shown in Fig. 1(b).

This paper is organized as follows. The ADC-direct architecture and system operation of neural recording with PDA are described in Section II; circuits implementing the architecture are detailed in Section III; measurement results are presented in Section IV; and concluding remarks are offered in Section V.

II. ADC-Direct Front End

Each recording channel features a hybrid analog–digital second-order delta–sigma modulator (2DSM) oversampling ADC, with the biopotential signal coupling directly to the second integrator for high conversion gain and dynamic offset subtraction in the digital domain. More generally, as shown in Fig. 2(a), with dual inputs u and x into the first and second integrators, respectively, and with additive noise e modeling quantizer error, the dynamics of the 2DSM is given by

$$v[n] = v[n-1] + u[n] - y[n] \tag{1}$$

$$w[n+1] = w[n] + v[n] - y[n] + x[n] \tag{2}$$

$$y[n] = w[n] + e[n] \tag{3}$$

sampled at discrete time steps $t = nT$. The resulting output

$$y[n] = u[n-1] + (x[n-1] - x[n-2]) + (e[n] - 2e[n-1] + e[n-2]) \tag{4}$$

produces the usual second-order noise shaping with unity gain signal transfer function for an input u, but with the first-order differentiation in its signal transfer function for an input x. Presenting the signal input to the first integrator incurs greater complexity in analog circuit implementation and, more fundamentally, is prone to saturation in the 2DSM loop dynamics, which, for 1-bit quantization, is only conditionally stable for a narrow regime of inputs near zero, $u \approx 0$. In contrast, zeroing the input to the first integrator $u = 0$, and directly coupling the BioADC input x to the second integrator, ensures stable saturation-free 2DSM loop dynamics with only 1-bit quantization in the output y.

Continuous-time analog implementation of the second integrator, as shown in Fig. 2(b), obviates the need for sampling the time-varying input $x(t)$. Instead, the integrator continuously integrates the residue between the input $x(t)$ and the piecewise constant digital prediction signal $p[n]$

$$w[n+1] = w[n] + \frac{1}{T}\int_{nT}^{(n+1)T} (x(t) - p[n])\, dt \tag{5}$$

where the digital prediction

$$p[n] = -v[n] + y[n] = \sum_{i=0}^{\infty} y[n-i] + y[n] \tag{6}$$

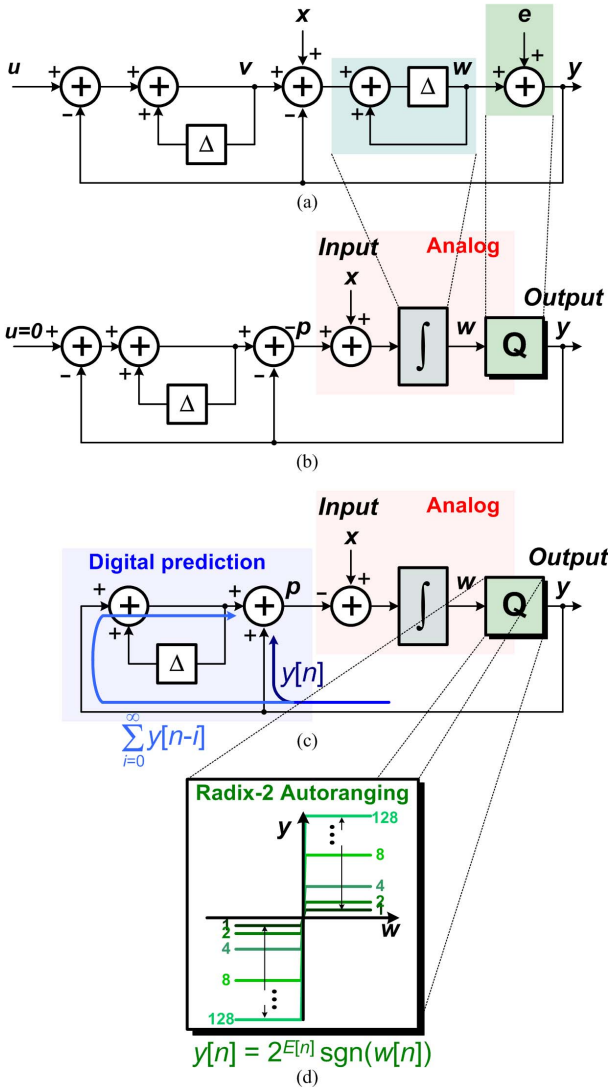


Fig. 2. ADC-direct neural recording with PDA. (a) Generalized 2DSM architecture. (b) Analog continuous-time implementation of the second integrator directly coupled to the input x. (c) Digital accumulator implementation of the first integrator with zero u generating digital prediction p. (d) PDA by radix-2 dynamic expansion and compression in the quantization y of the integrated residue $x - p$.

is produced by the first integrator digitally accumulating the quantizer feedback, as shown in Fig. 2(c), efficiently implemented by up/down counting. In turn, the analog input is reconstructed from (4) and (5) as

$$x[n] = \frac{1}{T}\int_{nT}^{(n+1)T} x(t)\,dt = \sum_{i=0}^{\infty} y[n-i+1] - (e[n+1] - e[n]). \quad (7)$$

Despite the appearance of the first-order (6 dB per octave) noise shaping of the quantization error $e[n]$ in (7), the extra first-order integrating (−6 dB per octave) loop gain in (7) contributed by the accumulation in the quantizer output $y[n]$ for digital prediction leads to the same 15-dB increase in the dynamic range for every doubling in oversampling ratio (OSR) as with the standard 2DSM [16]. The digital feedback along

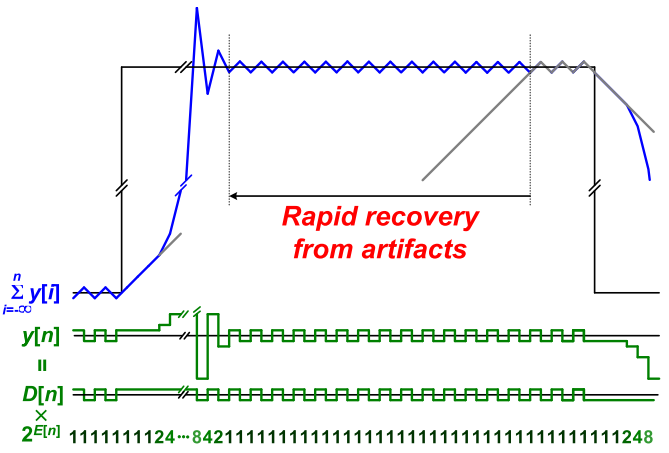


Fig. 3. Illustration of the effect of autoranging in digital prediction on dynamics of the signal output prior to decimation. Radix-2 PDA (blue line) significantly improves transient response over fixed-amplitude quantization (gray line) while maintaining the same noise-limited LSB-level resolution in steady state.

with the continuous analog integration implements the second-order predictive loop accommodating for potentially large offset and drift at the input, such as electrode dc offset (EDO) in the dc-coupled input, owing to the large loop gain at low frequencies.

The input dynamic range and transient response of the ADC loop are substantially improved by radix-2 autoranging of the quantizer, in which the history of the quantizer bits $D[n] = \text{sgn}(w[n])$ triggers either a factor two expansion or contraction in the digital feedback from the quantizer $y[n]$, as shown in Fig. 2(d)

$$y[n] = 2^{E[n]}\ D[n] \quad (8)$$

where the 3b exponent $E[n] = \{0, 1, \ldots 7\}$ covers seven octaves $(1, 2, \ldots 128)$ in digital gain. A run of five successive decisions with identical polarity increments the exponent expanding the range by two, whereas a run of three alternating polarity decisions decrements the exponent contracting the range by two

$$\begin{aligned} E[n] &\leftarrow E[n-1]+1 \quad \text{if } D[n] = \cdots = D[n-4] \\ E[n] &\leftarrow E[n-1]-1 \quad \text{if } D[n] = -D[n-1] = D[n-2] \\ E[n] &\leftarrow E[n-1] \quad \text{otherwise.} \end{aligned} \quad (9)$$

The rationale for this strategy is that a run of identical polarity decisions $D[n] = D[n-1]\ldots$ indicates the presence of a large transient, necessitating larger steps in digital prediction for faster recovery, whereas a run of alternating polarity decisions $D[n] = -D[n-1]\ldots$ indicates settling within the quantization limit, permitting smaller steps for higher accuracy. The precise choice of lengths of these runs prior to triggering radix-2 expansion/contraction in the range is not critical and is determined through behavioral simulation for optimal overall signal-to-noise-and-distortion ratio (SNDR) as a compromise between agility in transient recovery, resilience to variability in the signal, and stability in non-linear loop dynamics.

The combination of digital prediction and radix-2 autoranging constitutes PDA. PDA substantially improves transient

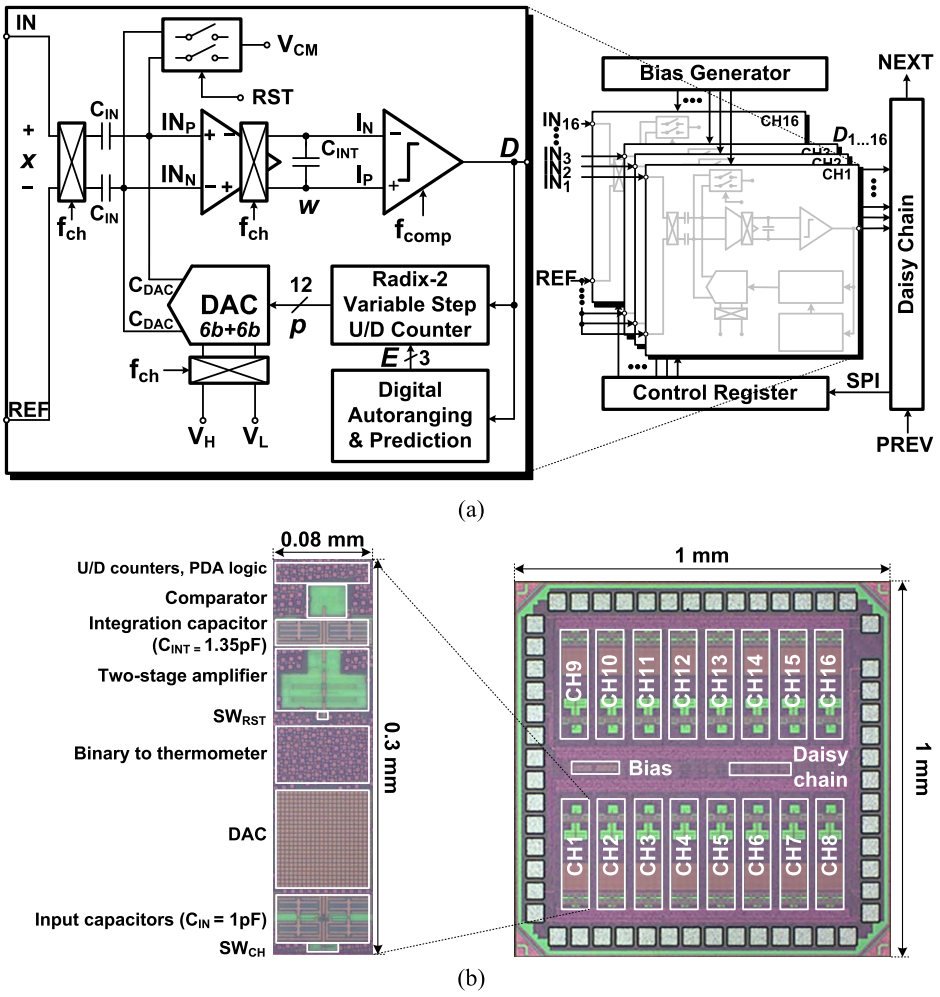


Fig. 4. 16-channel ADC-direct neural recording IC with PDA. (a) System diagram and circuit architecture with single-channel detail. (b) IC micrograph with corresponding single-channel detail.

response to large artifacts, tracking full-swing signal excursions without saturation while quickly reestablishing noise-limited resolution upon settling of the signal, as shown in Fig. 3. During the artifact transient, PDA temporarily relaxes the resolution with larger quantization step size to accommodate the fast response. This temporary relaxation of ADC resolution during the transient is governed by the following tradeoff between transient slope tracking response and quantization step size:

$$2^{E[n]} > \text{maximum signal step size} = \frac{2\pi f_{\text{sig}} A_{\text{sig}}}{f_{\text{comp}}} \qquad (10)$$

where (for a sinusoidal signal) A_{sig} is the signal amplitude referred to the digital-to-analog converter (DAC) LSB level (in units of 63 μV referred to the input), f_{sig} is the signal frequency, and f_{comp} is the sampling rate (see Fig. 4).

III. Circuit Design Implementation

Fig. 4 presents the system diagram circuit architecture and micrograph of the 16-channel neural-signal-acquisition integrated circuit (IC), with a detailed view of one of the 16 identical channels. Each channel implements the PDA hybrid analog–digital 2DSM of Fig. 2(d), digitally predicting the analog input at 12-bit resolution from a single-bit quantization of the continuously integrated residue at effective 32 OSR.

The continuous differential input $x(t)$ is chopped, and its digital prediction $p[n]$ is reconstituted by a correspondingly reference-chopped 12-bit 6b + 6b segmented DAC, prior to constructing the difference through capacitive coupling to the differential inputs IN_P and IN_N of a transconductance amplifier. For low-noise implementation, no specific sampling process through switching of capacitors is utilized, and the signal couples to the amplifier input entirely through charge redistribution in capacitive coupling, avoiding kT/C switching noise altogether. The common-mode dc bias at the IN_P and IN_N input nodes is set to V_{CM} by activating two switches at power-ON reset, which are subsequently deactivated and remain OFF throughout the entire operation. Junction diode leakage to bulk connections of these switches toward V_{CM} maintains common-mode dc bias with TΩ-range impedance, with no need for periodic reset.

The resulting residue $x(t) - p[n]$ is transconductance amplified and unchopped to baseband for continuous-time integration onto C_{INT}. A dynamic comparator produces the

binary quantizer output $D[n]$, which through barrel-shifting logic is combined with radix-2 autoranging $E[n]$ to produce the quantizer output $y[n]$ consistent with (8) and Fig. 2(d). The digital prediction $p[n]$, in turn, is obtained as the instantaneous sum of the digital feedback $y[n]$ and its running accumulation, completing the second-order loop. The 16 channels on-chip share common reference, bias, and control signals, and their outputs $D_{1\ldots16}$ are daisy-chained at the output to enable higher channel counts through cascaded multi-chip configuration. The 16-channel neural recording IC measures 1 mm $\times$ 1 mm, with 0.024 mm^2 per channel, in a 65-nm low-power bulk CMOS. Realized capacitance values for $C_{\rm IN}$ and $C_{\rm INT}$ are 1 and 1.35 pF, respectively, while the effective capacitance $C_{\rm DAC}$ of the 6b + 6b DAC referred to the integrator input is 128 fF.

A two-stage fully differential amplifier with two independent stages of common-mode feedback shown in Fig. 5(a) feeds into an integration capacitor $C_{\rm INT}$. Current biases for I_B1 and I_B2 are set to 375 and 25 nA, respectively. Current-reusing nMOS and pMOS input pairs in the first stage boost transconductance to 22 μS for improved noise efficiency factor (NEF) [17], while 600-mV$_{\rm pp}$ output swing at 0.8-V supply in the second stage increases a spurious-free dynamic range (SFDR). The simulated signal gain of the integrator is greater than 46 dB near the 32-kHz chopping frequency. Auxiliary amplifiers $A_{\rm CF}$ with conventional nMOS input differential pairs implement low-frequency common-mode feedback in each of the two stages, whereas capacitances $C_{\rm CM1} = 15$ fF and $C_{\rm CM2} = 8$ fF Miller-boosted for common-mode signals stabilize common-mode feedback loops.

A two-stage comparator shown in Fig. 5(b) [18] performs 1-bit quantization. Decision time ranges from 1.5 to 2 μs depending on input amplitude, dominated by capacitive loading ($C_T = 20$ fF) of the first-stage current-starved ($I_C = 20$ nA) pre-amplifier. Owing to the pre-amplification stage, simulated INR of the comparator is less than 80 $\mu V_{\rm rms}$. At 32-kHz operation, the comparator draws less than 3-nA current from the 0.8-V supply. The ONB clock signal, utilized in subsequent digital logic stages, is asserted when the decision is made.

Each of two differential segmented 6b + 6b DACs is implemented with two 64-element custom arrays of 2-fF unit capacitors C_0, bridged by 4% larger capacitor C_0', as shown in Fig. 5(c). The DAC reference levels V_H and V_L are tied to the supplies $V_{\rm DD} = 0.8$ V and $V_{\rm SS} = 0$ V, respectively. While current consumption from V_H is 50 nA, digital logic within the DAC consumes 10 nA from the 0.8-V supply at 32 kHz.

The implementation and timing control of the PDA is shown in Fig. 6. A 12-bit radix-2 variable-step up/down counter implements the update (6) in $p[n]$ in two phases: a double increment/decrement step $p[n] \leftarrow p[n] + 2\,y[n]$ activating the counter at its binary input position $E[n] + 1$, followed by a retracing step with opposite polarity $p[n] \leftarrow p[n] - y[n]$ and activating the counter at input position $E[n]$ just before the next cycle. Timing of the two-phase updates in the digital prediction state variable $p[n]$ is triggered by initiation and settling of the comparator output through the ONB signal as shown in the detailed logic diagram in Fig. 6(b). The thermometer-coded

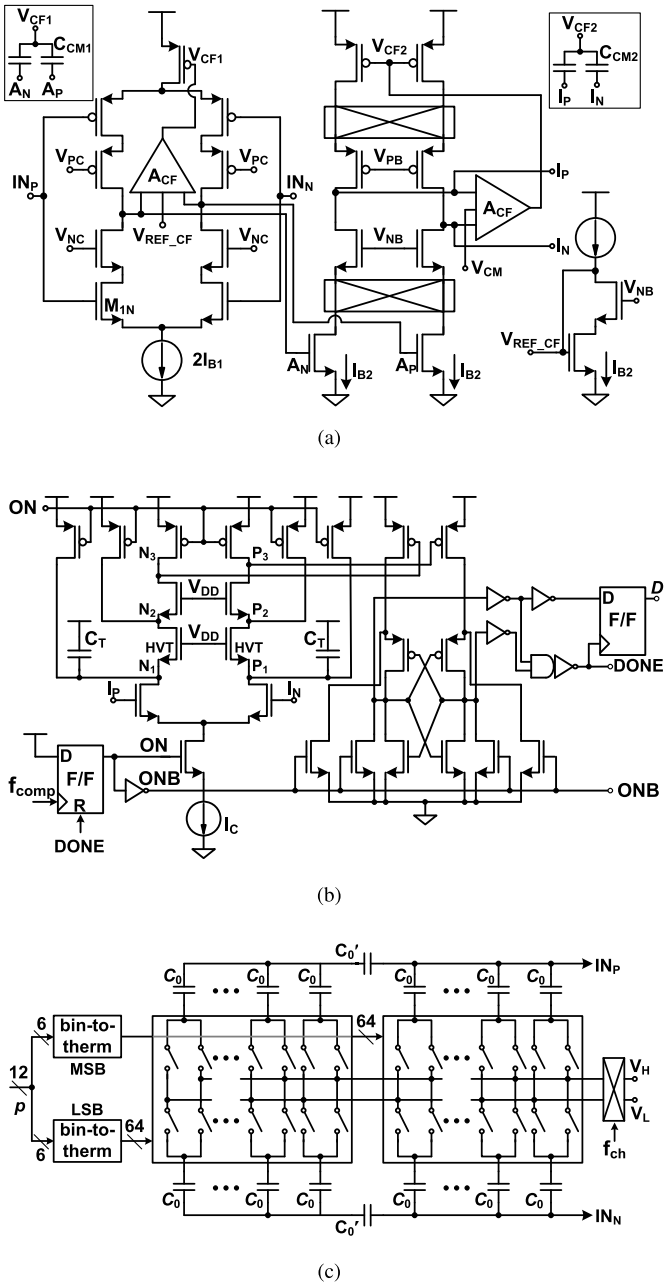
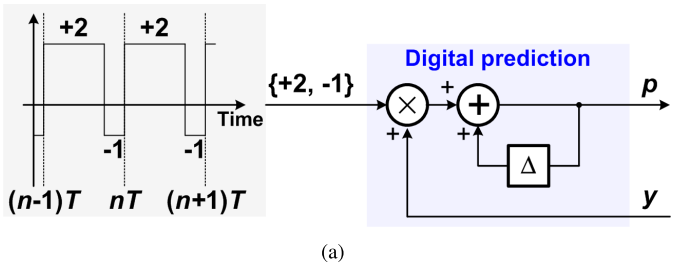


Fig. 5. Schematics of core analog circuits. (a) Transconductance amplifier for continuous-time integrator. (b) Dynamic comparator. (c) 6b + 6b segmented capacitive DAC.

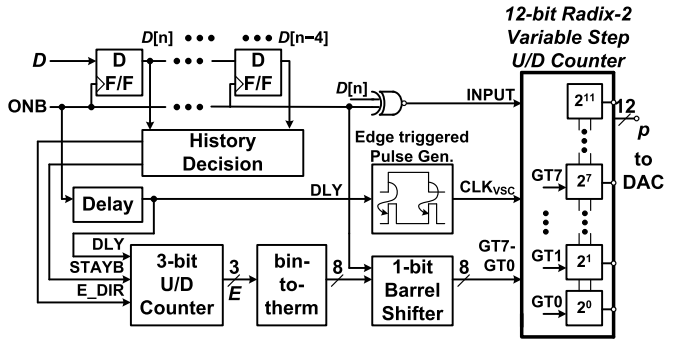
($GT0, \ldots GT7$) binary input position $E[n]$ of the radix-2 variable-step up/down counter is dynamically adjusted one point higher or lower, or stays put, based on the stored history in the quantization bits $D[n], \ldots D[n-4]$, according to (9). The PDA logic consumes less than 12-nW power at 32 kHz.

IV. Measurements

Benchtop characterization of several BioADC channels was performed with synthetic data, and *in vivo* validation tests were conducted in marmoset primate LFP recording. Unless otherwise noted, $I_S = 1$-μA channel supply current, an OSR of 32, and $f_{\rm ch} = 32$-kHz chopping frequency were utilized for



(a)



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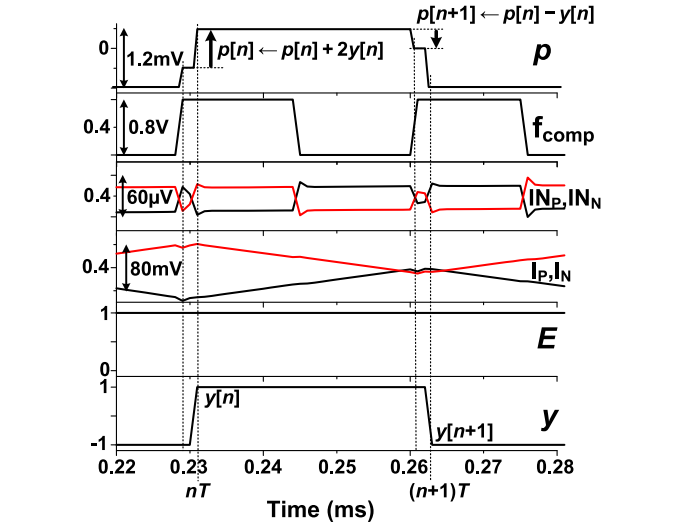


(c)

Fig. 6. PDA implementation and timing. (a) Simplified diagram and sequential activation of the digital prediction stage in Fig. 2(c) with up/down counters. (b) Detailed logic implementation. (c) Simulated time-domain waveforms illustrating internal operation.

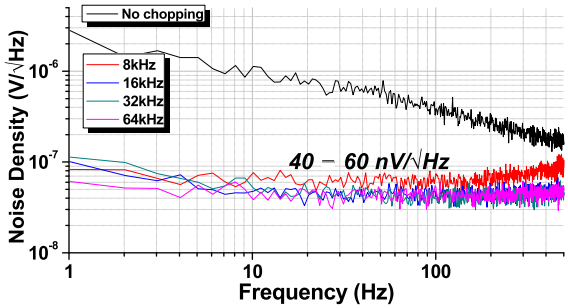


Fig. 7. Measured IRN spectral density for varying chopping frequencies at 1-μA channel current from 0.8-V supply.

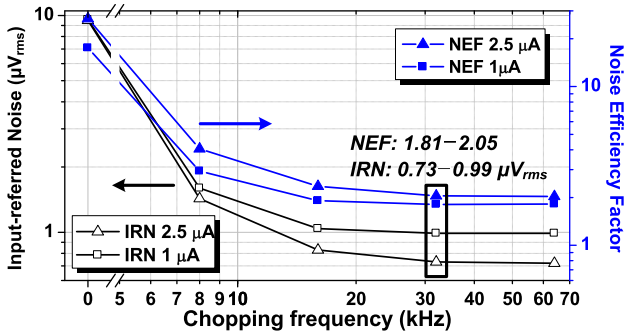


Fig. 8. Measured integrated IRN for varying chopping frequencies and supply current from 0.8-V supply.

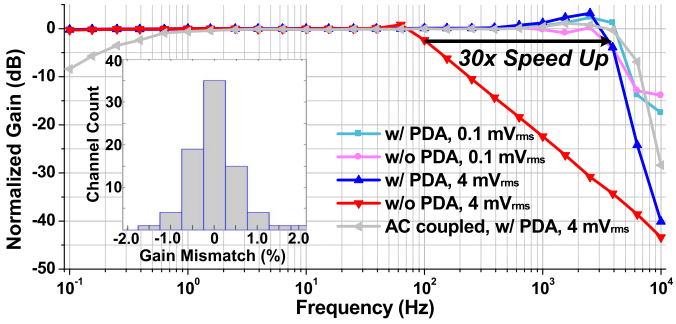
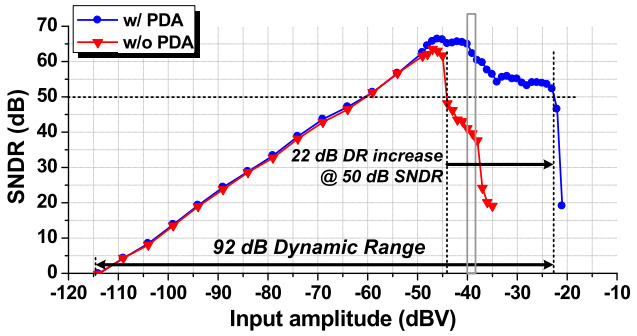


Fig. 9. Measured large-signal bandwidth with and without PDA offering a 30 times speed improvement. Inset: gain mismatch across channels.

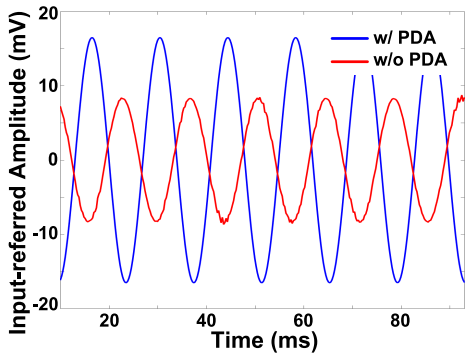
all measurements. The input impedance is a function of the chopping frequency, and at $f_{ch} = 32$ kHz, the measured input impedance is greater than 26 MΩ. The measured common-mode rejection ratio (CMRR), for a 28-mV_{pp} sinusoidal common-mode with zero differential input, is greater than 81 dB from dc to 60 Hz.

Figs. 7 and 8 show the measured IRN of the BioADC, with input shorted to the reference [IN = REF in Fig. 4(a)]. Without chopping technique (black line), $1/f$ noise is clearly visible. Chopping above 8 kHz reduces the noise density below 50 nV/$\sqrt{\text{Hz}}$, resulting in a 0.99-μV_{rms} integrated IRN over 500-Hz bandwidth and 1.81 NEF at 32-kHz chopping frequency and 1-μA supply. The major source of this noise is the first stage of the analog integrator. Measured IRN across chips is 0.94 μV_{rms} on average with 0.1-μV_{rms} standard deviation.

The measured effect of PDA on signal-dependent gain is highlighted in Fig. 9. Without PDA, the response to a large-step transient is slew-rate-limited due to unity increments/decrements in the digital feedback. With PDA, measurements show a 30 times speed improvement for 4-mV_{rms} amplitude signals, while for small input signals, no significant difference in speed is observed. Indeed, consistent with (10), a 4-mV_{rms} signal in the absence of PDA ($E[n] \equiv 0$) starts cutting off for frequencies above 57 Hz at 32-kHz sampling rate, with proportionally higher cutoff frequencies at lower signal amplitudes (e.g., 2.3 kHz at 100 μV_{rms}), whereas an activation of PDA achieves full bandwidth limited response independent



(a)



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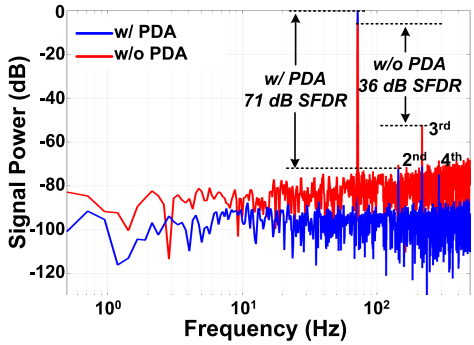

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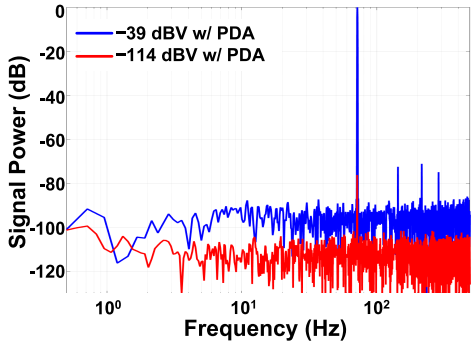
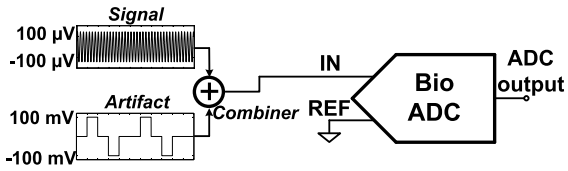


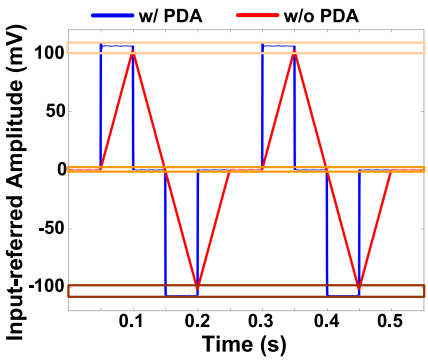
(d)

Fig. 10. Dynamic range with and without PDA. (a) Measured SNDR versus input amplitude. (b) Measured time-domain output and (c) corresponding spectra showing SFDR at −39-dBV input amplitude. (d) Measured spectra at −39- and −114-dBV input amplitudes.

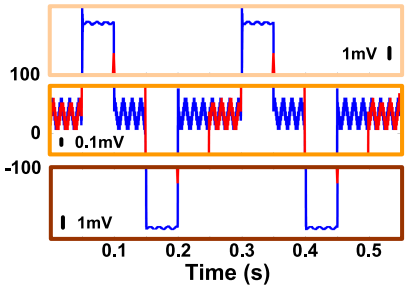
of signal amplitude by adjusting $E[n] > 0$. The measured 5.95 gain is flat at low frequencies down to dc. Measured relative mismatch (standard deviation over mean) in midband



(a)



(b)



(c)

Fig. 11. Transient response to large artifacts with and without PDA. (a) Test setup for controlled experiments using synthesized and combined signal and artifacts. (b) Measured time-domain waveforms. (c) Zoomed-in view of the waveform showing amplitude details in settling.

voltage gain is 4.5% across chips (inter-chip) and 0.7% across channels within the same chip (intra-chip).

The measured effect of PDA on increasing input dynamic range is shown in Fig. 10. PDA extends the input signal range, at greater than 50-dB SNDR, by 22 dB, approaching the full-scale range of the DAC, covering 92-dB input dynamic range. SNDR improvements by PDA at large input-signal amplitudes result from both reduced spurs and reduced noise floor, reaching 66 dB at −39 dBV, as shown in Fig. 10(b) and (c). However, lower than peak SNDR is reached for the larger amplitudes due to nonlinearities in PDA loop dynamics, which cause quantization noise and spurs to rise more than proportional to the signal as shown in Fig. 10(d), despite the same radix-2 factor simultaneous scaling of both the range and the quantization step by PDA. As such, the rapid transient recovery capability of PDA tracking large-slope artifacts comes at a temporary partial loss in signal resolution, which reestablishes its noise-limited level upon completion of the transient. Since typical neural signals are low amplitude and have a $1/f^2$ low-pass power spectrum profile [8], PDA according to (10) maintains near-optimal resolution in the absence of artifact transients.

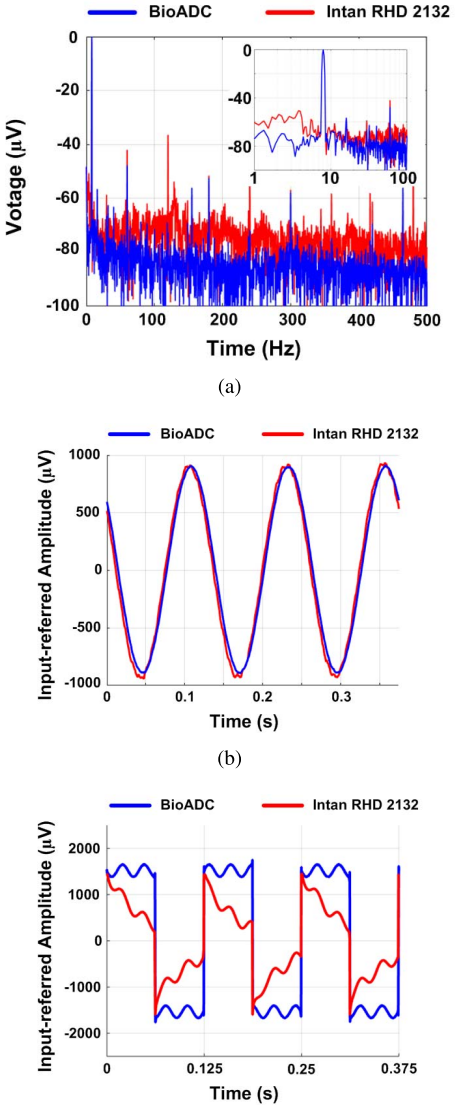


Fig. 12. Side-by-side comparison of the BioADC with a commercially available neural data acquisition system (Intan RHD-2132 [19], using the default fast-settling feature).

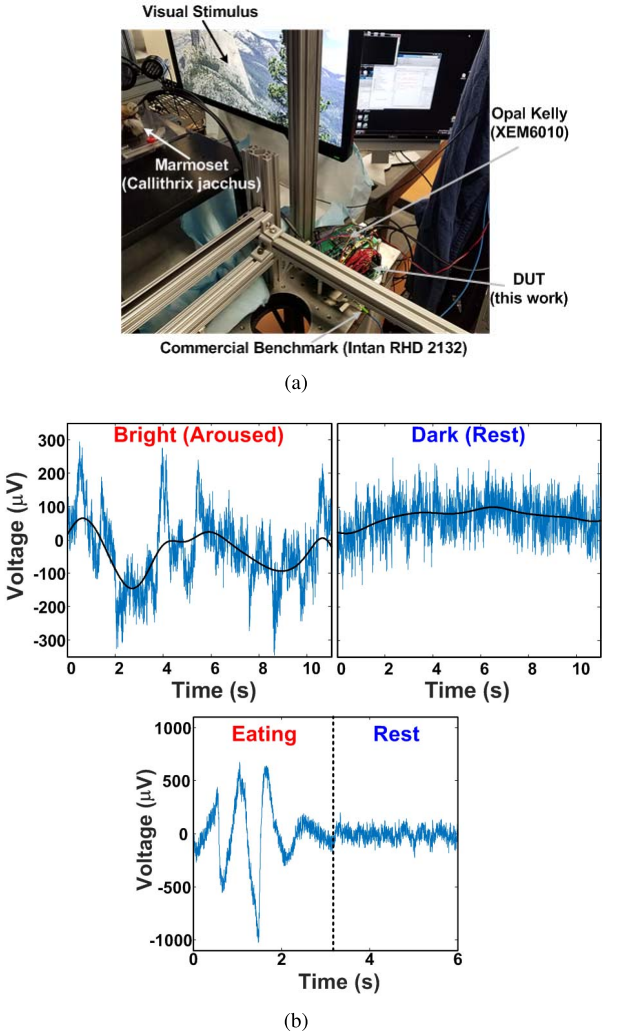


Fig. 13. (a) Experimental setup for *in vivo* recording of frontal cortex LFPs in a marmoset primate subject (Callithrix jacchus) under visual stimulation and (b) *in vivo* LFP recordings. Raw data (blue curve) are low-pass filtered ($\leq$1 Hz) to show slow potentials (black line).

Transient response is significantly improved by PDA. To characterize recovery time in a typical scenario of transients in electrophysiological recording due to movement artifacts or pulsed stimulation, we evaluated PDA response to a synthesized waveform as the combination of two signal sources: one 100-μV_{rms} sinusoidal signal and the other a 200-mV_{pp} pulsed artifact transient, as shown in Fig. 11(a). With PDA, fast tracking in the input was observed, recovering to the 200-mV_{pp} transients in less than 1 ms. In contrast, in the absence of PDA, the output is markedly slew-limited. The dc-coupled input is capable of capturing slow potentials ($\leq$0.1 Hz) while accommodating EDO up to $\pm$130 mV. For larger EDO, ac-coupled operation is obtained by connecting the dc-coupled input through a pair of external series capacitors (10 nF shown for ac-coupled reference in Fig. 9).

A side-by-side comparison between the BioADC and a commercially available benchmark (Intan RHD-2132, [19]) was performed with a combination of synthetic harmonic and transient signals to elicit various metrics in the comparison, as shown in Fig. 12. The BioADC consistently demonstrated the superior performance in an IRN, an input dynamic range, and a transient response over the RHD-2132 benchmark, which shows marked non-linear transients for even modest (3 mV_{pp}) input transients. The remarkably high high-pass corner of the benchmark in Fig. 12(c) is due to signal-dependent nonlinear conductance onto the input node of its ac-coupled front-end amplifier. This default "fast-settling" feature offered in the RHD-2132 for rapid recovery from large transients paradoxically introduces slow response transients for a range of amplitudes in signal transients.

In vivo LFP recordings using the 16-channel neural acquisition IC connecting to a NeuraLynx microwire electrode array inserted in frontal cortex of a marmoset primate (Callithrix jacchus) are shown in Fig. 13(a), resolving slow potentials ($\leq$0.1 Hz) of 200-μV_{pp} amplitude comparable to the ECoG signal range indicative of subject arousal state that is often missed by ac-coupled commercial neural instrumentation unless with severe degradation in SNR [20].

TABLE I
METRIC COMPARISON WITH STATE OF THE ART

	JSSC'14 [5]	ISSCC'17 [6]	Intan [19]	JSSC'15 [7]	ISSCC'17 [9]	VLSI'17 [10]	ISSCC'18 [12]	This work
Power/Ch (μW)	0.97	2.8	100	2.3	0.63	8	7.3	0.8
Supply (V)	1.8	1.2	3.3	0.5	1.2	1	1.2	0.8
Noise density (nV/√Hz)[a]	63	127	--	58	101	71	127	44
NEF	1.77[b]	7.4[b]	--	4.76	2.86	7.8	12.18	1.81
PEF ($NEF^2 V_{DD}$)	5.6[b]	66[b]	--	11.3	9.8	60.8	178	2.6
ENOB (bits)	9.57	--	--	--	11.7	10.2	14	10.7
Input DR (dB)	--	81[c]	--	50[c]	--	90	90	92
EDO range (mV_{pp})	AC-coupled	AC-coupled[d]	AC-coupled	100	rail-to-rail	100	AC-coupled[d]	260
CMRR (dB)	--	> 85	82	88	88	--	--[e]	81
Area/Ch (mm^2)	--	0.069[b]	0.5[f]	0.025	0.013	--	0.113	0.024
Process (nm)	180	40	--	65	130	180	40	65

[a] input-referred noise/√BW, differential configuration
[b] front-end amplifier only, excluding ADC
[c] SNDR = 0dB estimated from input-referred noise
[d] DC servo loop implements high-pass cut-off for AC-coupled recording
[e] tolerance to 700mV_{pp} common-mode interference
[f] estimated

Comparison of key metrics with the state of the art in neural recording ICs is given in Table I. In addition to NEF, the neural ADC achieves a power efficiency factor (PEF) of 2.6, almost a fourfold improvement among integrated front-end ADCs reported in the literature.

V. CONCLUSION

We presented an ADC-direct alternative to conventional approaches to integrated neural recording that alleviates common problems with amplifier saturation during large artifact transients and substantial signal attenuation of low-frequency biopotentials in ac-coupled operation, with further aggravated effects compounding these two through amplitude dependence of high-pass corner frequency. The unique 2DSM topology with kT/C-noise-free input coupling into the chopped second integrator delivers record energy-noise efficiency with NEF = 1.81 and PEF = 2.6. PDA handles a ±130-mV EDO and recovers from >200-mV_{pp} transient artifacts within <1 ms, offering >90-dB input dynamic range. Furthermore, using digital circuits for integration ensures the architecture benefits from process scaling, and the resulting compactness makes it suitable for incorporation in high-density recording arrays. *In vivo* LFP recordings from marmoset primate frontal cortex demonstrate its unique capabilities.

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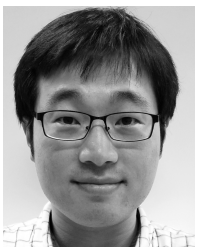

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