UNIVERSITY OF CALIFORNIA,
IRVINE

Towards Enhanced Range and Angular Resolution: A Dual-Band mmWave Radar Approach

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

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2025

DEDICATION

To my family.

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ACKNOWLEDGMENTS

First and foremost, I would like to thank my PhD advisor, Prof. Hamidreza Aghasi, for his invaluable support throughout my doctoral studies. He has been not only an outstanding professor but also a remarkable mentor, guiding me from electromagnetic simulation to measurement setup, and providing invaluable advice during manuscript preparation.

I would also like to thank my committee member, Prof. Heydari, for teaching me the fundamentals of RF Microelectronics in the EECS 270D course and providing the opportunity to join some joint group meetings with his team in the early stages of my PhD, which expedited my learning process. I also thank Prof. Boyraz for valuable discussions and his generous support in using their equipment.

Special thanks to the PhD students in the HIE group. Hedayatullah Maktoomi and I joined at nearly the same time, and he was the person I usually messaged whenever I had questions regarding EM simulations. Zhengyang Zhang joined the group last year and made substantial contributions to the MIMO radar project. His dedication and hard work were critical in ensuring the project's successful completion within the timeframe of my PhD.

I would also like to thank Huan Wang, Zisong Wang, Ahmadreza Danesh, and Shan-Hsuan Fu from the NCIC lab. Huan and Zisong served as my seniors and taught me a lot of design details during the early stage of my PhD. Henry and I often shared our thoughts on different possibilities for circuit design.

I would also like to thank Yaoyu Cao and Behnam Moradi from Prof. Michael Green's lab for their technical support, as well as Xun Li and Ataberk Atalar from Prof. Boyraz's lab for their continuous discussions comparing LiDAR and radar, and for their generous support with measurement equipment.

I would also like to thank Andrew Ding for many discussions about the PhD journey in general, and Jiacen Xu for opening my eyes to the newly emerging AI trends. Danmeng Wang from Prof. Andrei Shkel's lab also supported us as a last-resort backup for chip packaging.

Finally, I would like to thank my family, who have been supporting me all the time, both mentally and spiritually.

VITA

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A. Montazar, **X. Liu**, Z. Zhang and H. Aghasi, "A Hybrid CMOS-Polyimide Adaptive Force Radiometric Array With 3–5-GHz Wireless Connectivity," *IEEE Microwave and Wireless Technology Letters (LMWT)*, vol. 35, no. 6, pp. 880–883, 2025.

H. Aghasi, **X. Liu**, M. T. Taba, A. Tabatabavakili and E. Afshari, "Broadband Harmonic-Assisted Power and Efficiency Enhancement in a 174–232-GHz SiGe Voltage-Controlled Oscillator," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 60, no. 6, pp. 1921–1931, 2025.

X. Liu, B. Moradi and H. Aghasi, "A Single-Switch 3.1–4.7 GHz 194.52-dB FoM Class-D VCO With 495 µW Power Consumption," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCSII)*, vol. 71, no. 10, pp. 4451–4455, 2024.

B. Moradi, **X. Liu** and H. Aghasi, "A 76–82 GHz VCO in 65 nm CMOS With 189.3 dBc/Hz PN FOM and −0.6 dBm Harmonic Power for mm-Wave FMCW Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCSI)*, vol. 71, no. 1, pp. 51–61, 2024.

X. Liu, M. H. Maktoomi, M. Alesheikh, P. Heydari and H. Aghasi, "A 49–63 GHz Phase-Locked FMCW Radar Transceiver for High-Resolution Applications," *ESSCIRC 2023 – IEEE 49th European Solid-State Circuits Conference (ESSCIRC)*, pp. 509–512, Sept. 2023.

B. Moradi, **X. Liu**, M. M. Green and H. Aghasi, "A Compact CMOS 76–82 GHz Super-Harmonic VCO With 189 dBc/Hz FoM Operating Based on Harmonic-Assisted ISF Manipulation," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 215–218, June 2022.

ABSTRACT OF THE DISSERTATION

Towards Enhanced Range and Angular Resolution: A Dual-Band mmWave Radar Approach

By

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Doctor of Philosophy in Electrical Engineering

University of California, Irvine, 2025

Assistant Professor Hamidreza Aghasi, Chair

Millimeter-wave (mm-Wave) frequencies, due to their short wavelengths, have garnered significant interest for applications such as automotive driving, high-resolution sensing, and object detection. CMOS technology, with its low cost and high level of integration, presents a promising solution for incorporating more transceiver (TRX) channels and digital processing units into radar systems. However, most existing mm-Wave radar solutions operate within a single frequency band, which limits range resolution. On the other hand, improving angular resolution typically requires integrating a larger number of TRX channels, increasing system complexity. With many underutilized frequency bands available in the mm-Wave spectrum, adopting a dual-band radar architecture offers a compelling path to overcome these limitations in both range and angular resolution.

In the first part of this dissertation, a CMOS 49–63 GHz phase-locked stepped-chirp FMCW radar transceiver is presented. By implementing a coupled-PLL architecture—comprising a reference PLL operating from 49 to 56 GHz and a mixing PLL that replicates the lower-frequency chirp to the higher band at the same rate—the system achieves seamless frequency extension. Fabricated in GlobalFoundries 22 nm FD-SOI technology, the chip realizes a 14 GHz stitched bandwidth with a 10 GHz synthetic, enabling a range resolution of 1.4 cm after

combining the baseband outputs from both frequency bands.

The second part of this dissertation introduces a dual-band MIMO mm-wave FMCW radar transceiver that integrates both fundamental and third-harmonic transmit/receive paths on a single chip. A two-chip 4TX–4RX prototype leverages a non-uniform linear array (nULA) to exploit the angular-spectrum notches of each band to suppress aliasing from the other, thereby achieving alias-free angular resolution with fewer channels. Furthermore, independent phase shifters for each frequency band enable phase-dithering techniques that reduce grating-lobe levels by up to 10 dB. This prototype successfully demonstrates an angular resolution of 5.4°.

Finally, the third part of the dissertation presents an ultra-low-power Class-D voltage-controlled oscillator (VCO). By employing an RF choke to enforce a fixed ratio between the "floating" and single-ended capacitors, the design sharpens the zero-crossing of the oscillation waveform, thereby improving phase noise. Owing to its low power consumption and superior phase-noise performance, this VCO was subsequently adopted in a force radiometric array for low-power biomedical applications.

Chapter 1

Introduction to mmWave Radar Design Challenges

CMOS-based radar technology has gained wide adoption in Advanced Driver Assistance Systems (ADAS), drone and robotic sensing, and synthetic aperture radar (SAR) imaging due to its low cost, compact form factor, and high power efficiency, as illustrated in Fig. 1.1. Furthermore, mmWave signals, with their short wavelengths and non-ionizing nature, have enabled ultra–high-resolution medical sensing applications.

Figure 1.1: CMOS mmWave radar applications: (a) autonomous driving, (b) drone and robotic sensing, (c) SAR imaging.

Frequency Spectrum Considerations.

Radar systems can operate over a wide frequency range—from approximately 1 MHz to 1 THz. At frequencies below 30 GHz [1, 2], the relatively large wavelength limits achievable spatial resolution, and the scarcity of contiguous spectrum restricts range resolution. Conversely, at frequencies above 100 GHz, while some research efforts [3–5] have demonstrated high output power and effective isotropic radiated power (EIRP), these systems still suffer from degraded phase noise, lower receiver sensitivity, and excessive propagation loss as dictated by the Friis transmission equation—substantially reducing effective detection range.

MmWave frequencies (30–100 GHz) serve as a compromise between microwave and terahertz bands, offering a favorable compromise between detection accuracy, signal-to-noise ratio (SNR), and range coverage. In recent years, building blocks such as VCOs [6, 7], power amplifiers (PAs), and low-noise amplifiers (LNAs) and antennas [8] have been successfully demonstrated, establishing the feasibility of fully integrated CMOS mmWave radar transceivers [9].

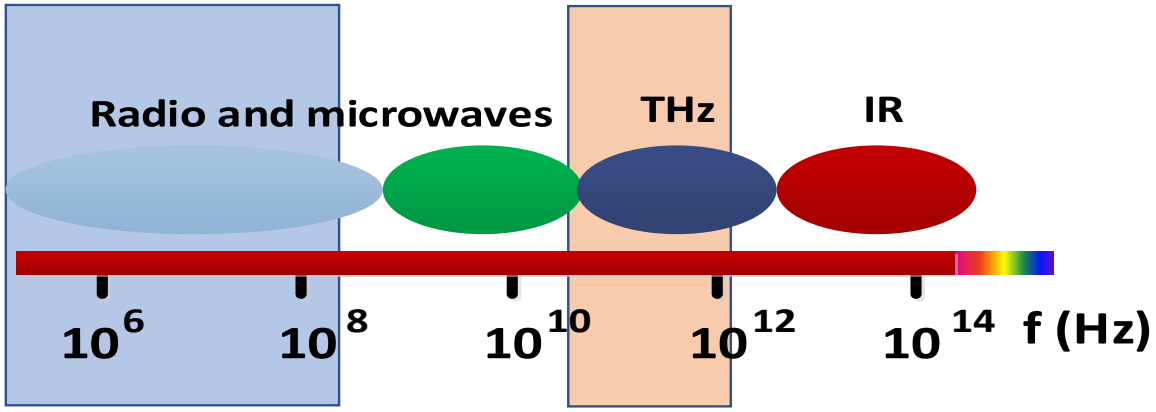

Figure 1.2: (a) Radar frequency band at mm-wave spectrum, (b) received power at 50m distance vs frequency based on radar Friss equation.

Range Resolution.

Range resolution defines the ability of a radar to distinguish between two targets closely spaced in range. As illustrated in Fig. 1.3, doubling the radar bandwidth while maintaining the same chirp rate doubles the baseband sampling interval. Consequently, two closely

spaced targets that previously appeared merged can now be resolved as separate peaks in the FFT domain.

The range resolution is given by:

$$d_{\text{res}} = \frac{c}{2B_{\text{chirp}}}. \tag{1.1}$$

where c is the speed of light and B_{chirp} is the instantaneous chirp bandwidth.

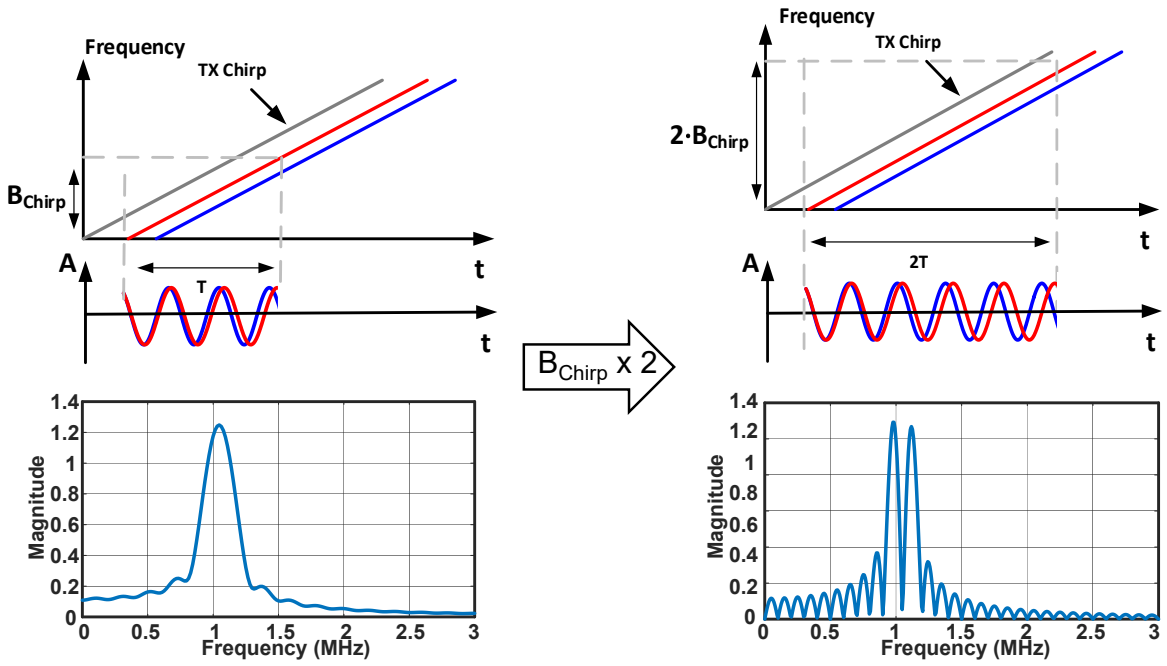

Figure 1.3: (a) Radar frequency band at mm-wave spectrum, (b) received power at 50m distance vs frequency based on radar Friss equation.

Angular Resolution and Spatial Considerations.

While range resolution can be enhanced relatively easily by increasing the chirp bandwidth, angular resolution—which governs the radar's ability to distinguish targets in the azimuth domain—often becomes the limiting factor in high-resolution sensing.

For example, assuming a feasible 5 GHz radar bandwidth yields a range resolution of about 3 cm independent of distance. However, for an angular resolution of 5°, the linear azimuth

resolution becomes approximately 17.75 cm, 43.6 cm, and 87.3 cm at 2 m, 5 m, and 10 m distances, respectively (Fig. 1.4).

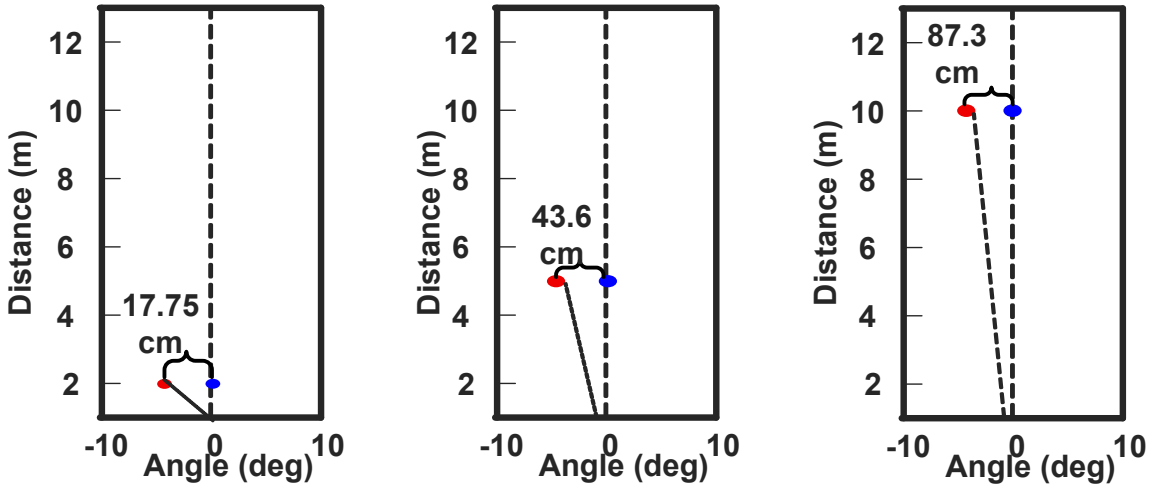

Figure 1.4: (a) Radar frequency band at mm-wave spectrum, (b) received power at 50m distance vs frequency based on radar Friss equation.

Methods for Enhancing Angular Resolution.

A conventional approach to improve angular resolution in FMCW radar systems is to increase the number of receiver channels, as shown in Fig. 1.5. Doubling the number of channels effectively halves the 3 dB beamwidth of the angular spectrum. The angular resolution for a uniform linear array (ULA) with $\lambda/2$ spacing between adjacent elements can be approximated by:

$$\theta_{\text{res}} = \frac{2}{N\cos(\theta)}, \tag{1.2}$$

where N is the number of receiver channels.

While straightforward to implement, achieving 5° angular resolution using a ULA demands a very large number of transceiver (TRX) channels—implying significant hardware cost and power consumption.

An alternative approach involves relaxing the $\lambda/2$ spacing constraint (e.g., using non-uniform arrays or larger inter-element spacing). However, this introduces angular aliasing, which restricts the field of view (FoV) and can lead to ghost targets, posing a major design trade-off for next-generation mmWave radars.

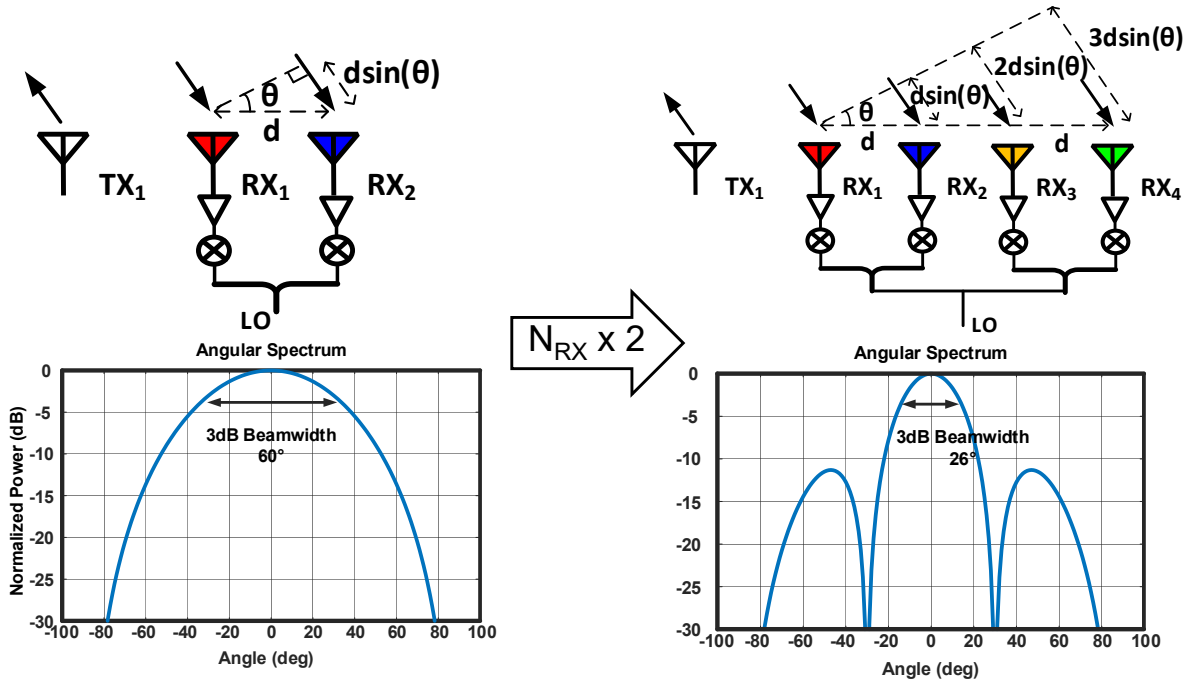

Figure 1.5: (a) Radar frequency band at mm-wave spectrum, (b) received power at 50m distance vs frequency based on radar Friss equation.

Chapter 2

A CMOS 49–63-GHz Phase-Locked Stepped-Chirp FMCW Radar Transceiver

2.1 Introduction

With the rapid evolution of advanced driver assistance systems (ADAS) [10, 11], Internet of Things (IoT) [12], smart industry[13, 14], and healthcare, the need for frequency modulated continuous-wave (FMCW) radar in both the unlicensed 60 GHz and 77 GHz band is growing substantially [15–17]. Emerging applications such as IoT-based local-area sensing call for large-scale deployment of power-efficient, miniaturized radar nodes[18, 19]. These sensors must cover ranges from 10 cm to 50 m and provide fine detection capability characterized by range resolutions[20]. The range of coverage depends on the transmitted power which should be sufficiently high to overcome the propagation loss of the medium (e.g., air) and achieve acceptable receiver sensitivity, yet remain within the bounds of existing

radiation/communication regulations. Additionally, these sensors must operate at high frequencies (i.e., small wavelengths) and across broad bandwidths, as both bandwidth and frequency of operation contribute to resolution.

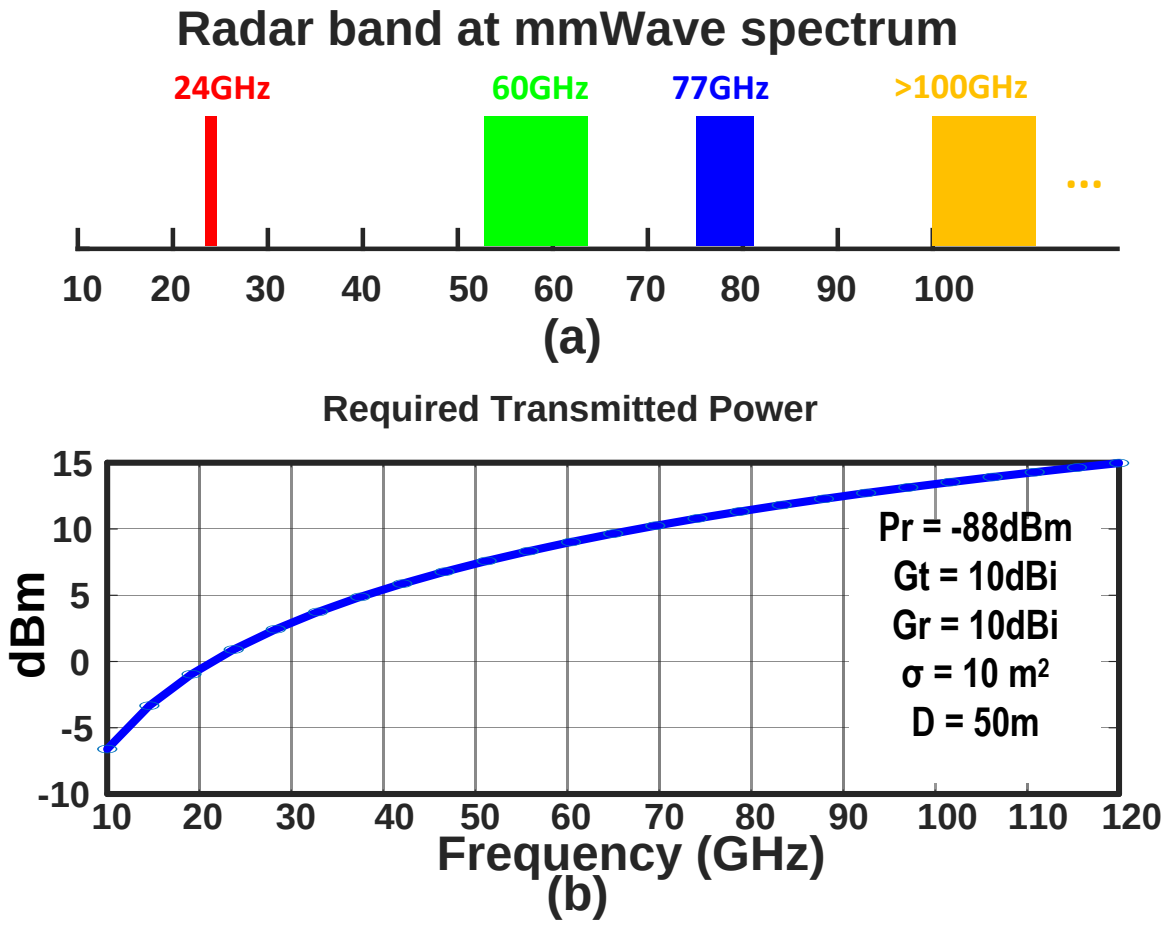

Figure 2.1: (a) Radar frequency band at mm-wave spectrum, (b) received power at 50m distance vs frequency based on radar Friss equation.

Existing commercial 24/60/77 GHz FMCW radar [21–25] exhibit relatively narrow bandwidths (Fig. 2.1(a)), which inherently limits the range resolution. While operating above 100 GHz [26] facilitates broader bandwidths for a smaller fractional bandwidth, the power generation efficiency and receiver sensitivity are severely degraded, thereby limiting the range. As shown in Fig. 2.1(b), for a receiver sensitivity of -88 dBm, transmitter (TX) and receiver (RX) antenna gains of 10 dBi and target with a radar cross section (σ) of 10 m^2 located 50 meters away, the required transmitted power to produce detectable signals on the RX

side based on radar's Friis equation for frequencies above 100 GHz should be higher than 13 dBm [27, 28]. Generating such levels of power in light of severely limited output power available from a MOS device beyond 100 GHz is challenging [29]. Another issue that becomes increasingly more significant at high frequencies is the signal transfer from the TRX chip to the high-gain antenna. In particular, the RF signal transfer to the package antennas encounters increased insertion loss and group delay variation at higher frequencies due to skin effect [30], chip-to-package parasitic impedances [31], and the interconnect dimensions becoming comparable to the wavelength. For example, a 500 μm wirebond behaves as a $\lambda/4$ transmission line at 150 GHz.

Rather than increasing the operating frequency to obtain a broader absolute bandwidth, a potential solution involves deploying multiple lower-frequency radars, each covering adjacent frequency sub-bands, and combining them to achieve the desired overall bandwidth. However, this approach mandates precise phase and frequency synchronization across the deployed bands, which poses significant challenges and often results in high power consumption. This work presents a stepped chirp based FMCW radar transceiver which consists of two sub-bands, with each covering 7GHz bandwidth. By splitting the bandwidth into two frequency bands, the wideband design challenges associated with critical components such as the power amplifier (PA), low noise amplifier (LNA), and voltage controlled oscillator (VCO) are largely mitigated. More importantly, the two bands are phase and frequency synchronized using low-power, scalable on-chip mechanism inspired by type-II analog PLLs, which is essential for the radar's high-resolution performance. The radar TRX chip is co-integrated with series-fed patch antenna arrays through a chip-to-package impedance matching network.

The rest of the section is organized as follows. Subsection 2.2 explains the necessity of widening the bandwidth to enhance range resolution and the operation of the frequency segmented phase locked TRX architecture. Subsection 2.3 introduces the design of critical circuit blocks and chip-to-board and board-to-antenna interface design. Subsection 2.4 demonstrates the

transceiver major performance measurements and the radar operation verification. Section 2.5 concludes this section.

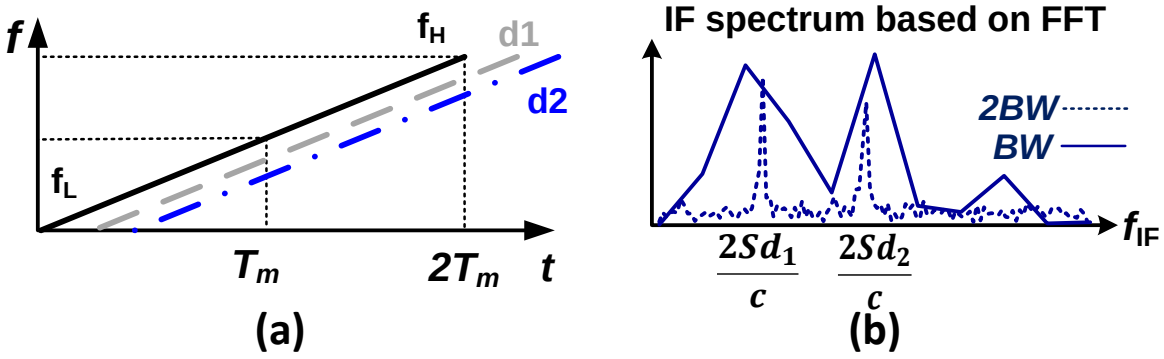

Figure 2.2: Relationship between Range Resolution and Synthetic Bandwidth.

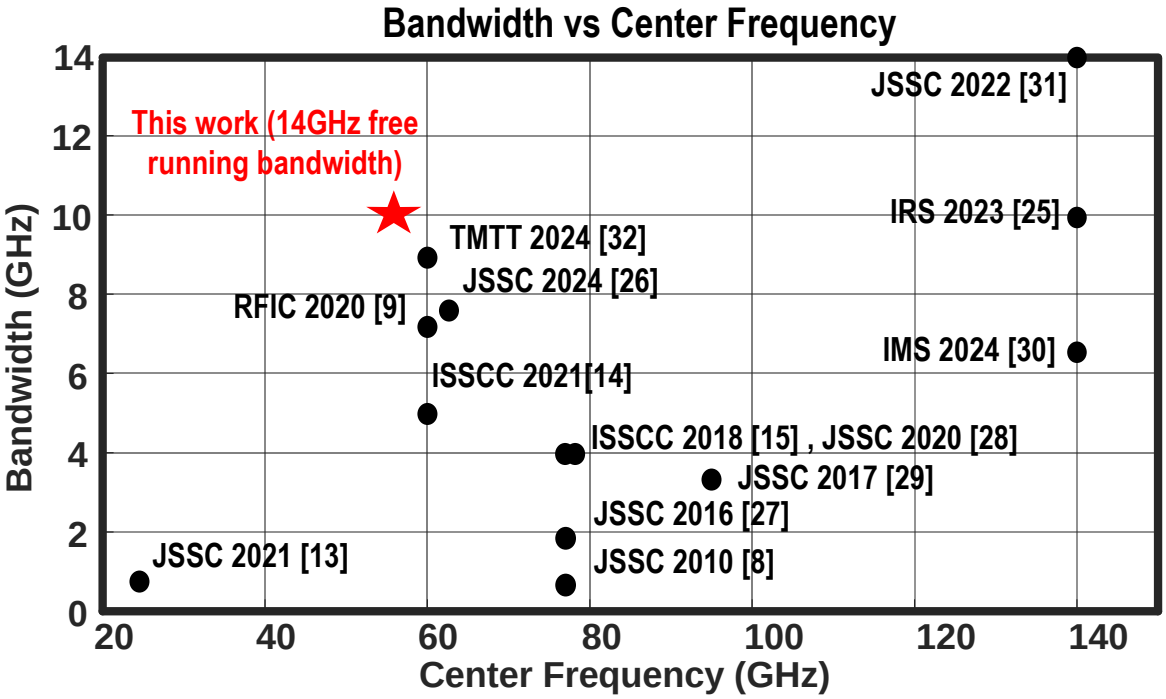

Figure 2.3: Bandwidth vs Center Frequency

2.2 System Architecture of Stepped Chirp Radar

Range resolution is a key radar performance metric that defines the minimum distance between two closely spaced targets that can be distinctly identified by the radar in a single

chirp interval [32]. The FMCW radar range resolution (RR) is inversely proportional to the chirp bandwidth (BW) [20, 33], as illustrated in Fig. 2.2, i.e., $RR = c/2BW$ where c is the speed of light. Therefore, to improve range resolution, an increase in chirp bandwidth is required. A larger bandwidth can (1) yield a greater frequency separation (Δf) for the same distance resolution (Δd) or (2) allow the same Δf but with a longer observation window for the same Δd. A snapshot of state-of-the-art phase-locked FMCW radars covering 20-140 GHz including this work is summarized in Fig. 2.3 [34–41]. Given the constraints on the fractional bandwidth of chirp generation circuits, such as VCOs utilizing varactor tuning, the majority of previous designs operating below 100 GHz have been limited to sub-10-GHz chirp bandwidth. This highlights the need for innovative frequency synthesis architectures to overcome these bandwidth challenges.

2.2.1 Frequency Synthesis Planning

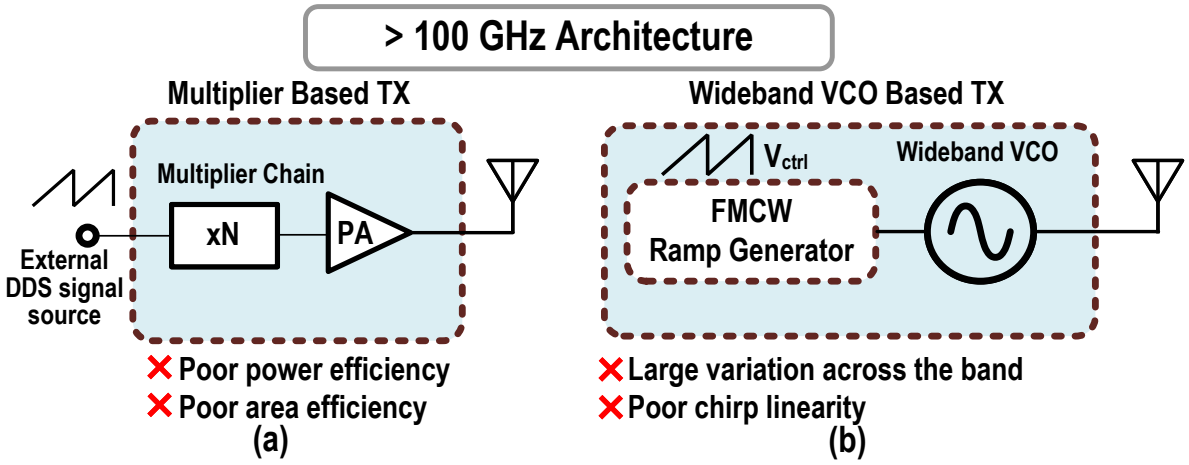

Figure 2.4: Above 100 GHz Wideband radar TX utilizing (a) multiplier chain, (b) VCO.

The present implementations of mm-wave radar are mostly centered around two predominant approaches for signal synthesis. To achieve greater bandwidth for range resolution, single-chirp implementations often target operating frequencies above 100 GHz, where radar systems encounter several challenges. As depicted in Fig. 2.4(a), the first method employs an external FMCW signal generated by a direct digital frequency synthesizer (DDFS), which

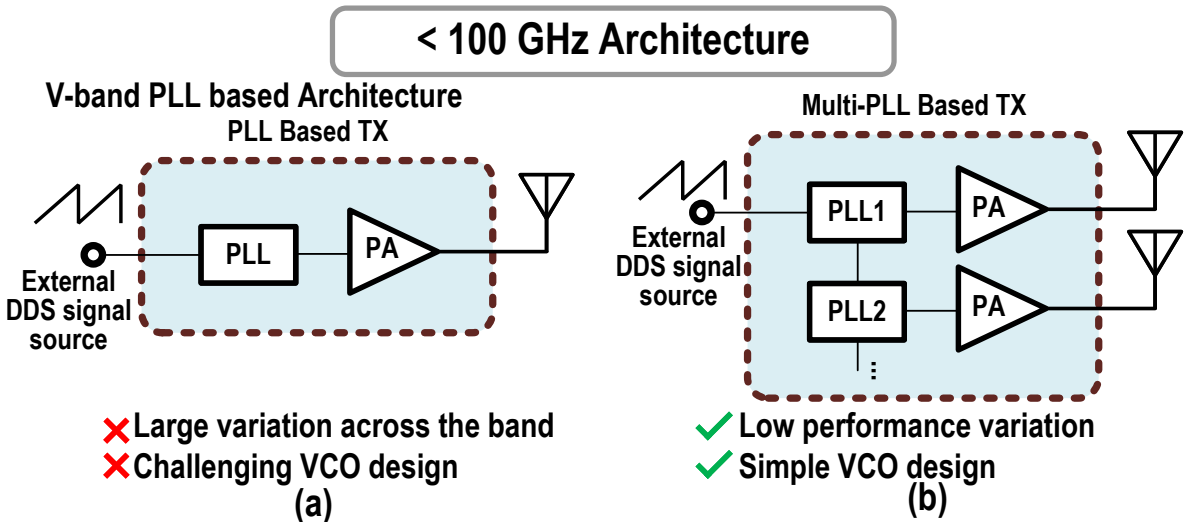

Figure 2.5: Below 100 GHz Wideband radar TX utilizing (a) one PLL (b) coupled PLL.

is subsequently passed through a chain of multipliers and a PA boost the signal's power. This method is inefficient in terms of both area and power consumption due to two main factors: (1) The requirement for additional multiplier stages as the frequency increases owing to challenges in achieving high-frequency DDFS outputs [40], and (2) the reduced gain and efficiency of transistors within the PA as frequency rises. Alternatively, the second method uses wideband VCOs (Fig. 2.4(b)), while mitigating some of the issues mentioned in Fig. 2.4(a). Nonetheless, this approach is not without its drawbacks, including the diminished quality factor of passive components and the augmented intrinsic noise of active devices at higher frequencies. This in turn degrades the oscillator's phase noise, adversely affecting the signal-to-noise ratio (SNR) of the intermediate frequency (IF) signal. Additionally, as shown in Fig. 2.4(b), calibration of the ramp generator to linearize the chirp for VCO-based FMCW radar is necessary to offset the impact of suboptimal K_{VCO} on the chirp's linearity [42].

Addressing the limitations and shortcomings of above 100-GHz configurations in Fig. 2.4, we explore PLL-based designs that can span below-100 GHz, e.g., a 49-63-GHz frequency range. Fig. 2.5 demonstrates two distinct configurations: one that employs a single PLL with wide bandwidth coverage ($\geq$10 GHz), and another that integrates several sub-band

PLLs. In Fig. 2.5(a), it is necessary for the VCO's fractional bandwidth to be accordingly increased, a challenge at mm-wave frequencies predominantly due to the prevailing effect of device parasitics. In Fig. 2.5(b), segmentation of the frequency band into smaller sub-bands significantly mitigates the design challenges of wideband TRX blocks, such as the VCO, PA, and LNA. This approach lowers PA output power variations, improves the VCO linear tuning range, and reduces the oscillator phase noise.

It is noted that the design challenge of critical mm-wave front-end blocks increases substantially with larger bandwidths mainly due to the limitations on wideband matching. On the radiation side, planar antenna configurations such as series-fed patch antennas, which are currently popular for FMCW radars due to their narrow Field-of-View (FoV), can hardly achieve a radiation bandwidth above 10 GHz. This is why despite achieving a total impressive bandwidth of 9 GHz in [41], the design challenges of ensuring all subblocks operate across the same bandwidth results in sub-optimal phase noise and output power compared to [15].

In light of these design challenges, we propose dividing the entire bandwidth into multiple smaller sub-bands, simplifying the design of critical building blocks, such as antennas, for each band. An architecture based on coupled PLLs, shown in Fig. 2.5(b), provides an effective means of extending the bandwidth while preserving a uniform narrowband chirp profile across various sub-bands. Nevertheless, this approach demands novel synthesizer solutions to reduce power consumption, particularly as the number of PLLs increases.

2.2.2 Stepped Chirp Transceiver Architecture

One solution to divide the bandwidth into smaller sub-bands is the stepped chirp architecture[43]. A stepped-chirp radar sensor can achieve a maximum range resolution of $c/(2BW_T)$, where BW_T is the total synthetic bandwidth comprised of N subbands with each covering a band-

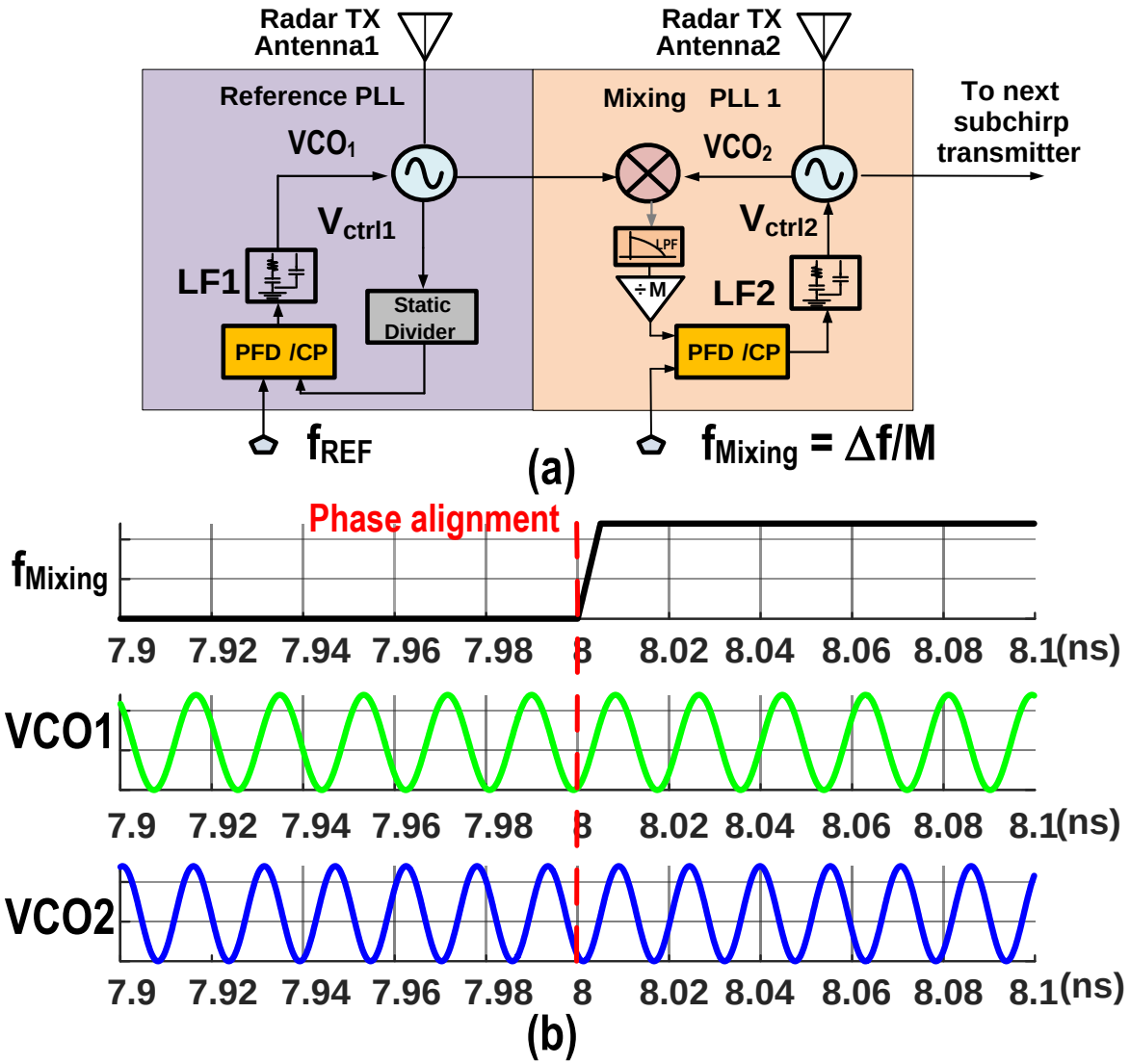

Figure 2.6: (a) Simplified TX block diagram, (b) timing diagram of VCO1 and VCO2 with respect to mixing PLL input reference.

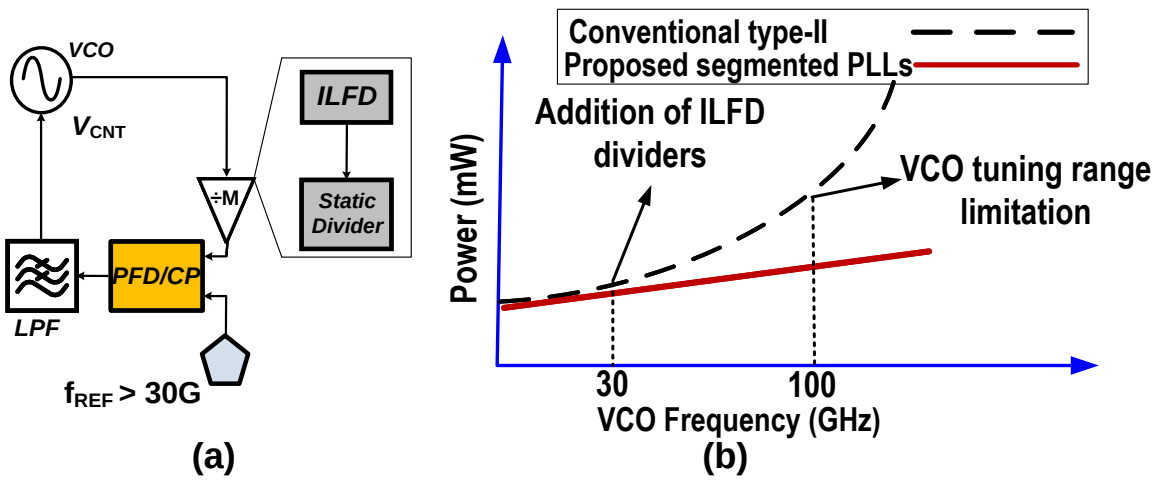

Figure 2.7: (a) Conventional type-II PLL architecture with ILFD at above 30GHz, (b) power saving by adopting mixing PLLs for frequency above 30GHz instead of type-II PLLs.

width of $BW{=}BW_T/N$. The range resolution associated with BW_T is only obtained if the slopes of chirps corresponding with the sub-bands are identical [44]. This requirement is extremely challenging to meet in practice if the stepped chirps are realized by free-running VCOs, as there is no feedback loop to force the constant frequency difference.

To resolve unwanted variations of free-running oscillators while significantly reducing the power consumption of the radar, we propose a new phase-locked stepped-chirp generation structure. On the TX side, shown in Fig. 2.6(a), N sub-bands with frequency coverage of BW and spacing of Δf are realized using a circuit comprising one reference PLL and $N{-}1$ *mixing PLLs*. In this structure, the outputs of each pair of adjacent VCOs are fed to a mixer inside a mixing PLL. Under the locking condition, the output frequency of the i^{th} mixing PLL, f_{mix_i} is locked to the mixer's difference frequency component, i.e., $f_{mix_i} = |f_{osc_{i+1}} - f_{osc_i}|$. By placing the mixer inside a PLL [45], the mixing spurs are substantially constrained. Following phase-locking acquisition, the TX frequency synthesizer in Fig. 2.6(a) ensures that the frequency difference between two adjacent PLLs are locked to Δf, while also promising the synchronized sweep of their corresponding chirps with respect to the chirp generated by the reference PLL. The linearized loop analysis of a type-II PLL comprising mixers is detailed in [46] and for brevity is not repeated here. The other advantage of this stepped-chirp architecture is the

deterministic phase relationship between two adjacent VCOs, as shown in Fig. 2.6(b), which facilitates the baseband signal stitching, discussed later.

The coupled mixing PLLs offer significant power saving advantage compared to conventional type-II PLLs for the following reason: Referring to power consumption breakdown in Fig. 2.7, a mm-wave type-II PLL consumes a considerable amount of power, as the VCO and divider chain's power consumption becomes increasingly significant with higher frequency/loop-division-ratios. The output frequency of the mixer inside the mixing PLL of the proposed architecture is set to Δf=7 GHz rather than the actual sub-band frequency, thereby significantly reducing the loop output frequency to a range manageable by digital dividers. This allows the removal of power-hungry frequency divider chains (e.g., injection-locked frequency dividers (ILFD) [47] and current-mode logic (CML) dividers [48]) and replacing them with only a low-power mixer inside the loop. Owing to the use of mixing PLLs, adding more sub-bands to this design leads to a linear increase in power consumption as opposed to the super-linear growth characteristic of type-II PLLs (Fig. 2.7(b)).

2.2.3 IF Processing and Resolution Enhancement

The proposed RX architecture of the stepped-chirp radar TRX is shown in Fig. 2.8(a), where the LNA and mixer operate within the bandwidth of each sub-band ($BW = BW_T/N$). Therefore, the integrated noise of each sub-band RX is almost 10log(N) smaller than that of the conventional RX ($(N-1)\Delta f + BW_T$). This smaller bandwidth leads to higher RX sensitivity, which allows for longer ranges of operation. On the other hand, the design of wideband linear LNAs is challenging due to the variations of passive components with wider bandwidth [49]. This issue is resolved in the proposed RX by operating the LNA across the bandwidth of $BW = BW_T/N$. Finally, a lower sub-band bandwidth, the results in higher achievable SNR than conventional FMCW RXs, thereby relaxing the ADC resolution and

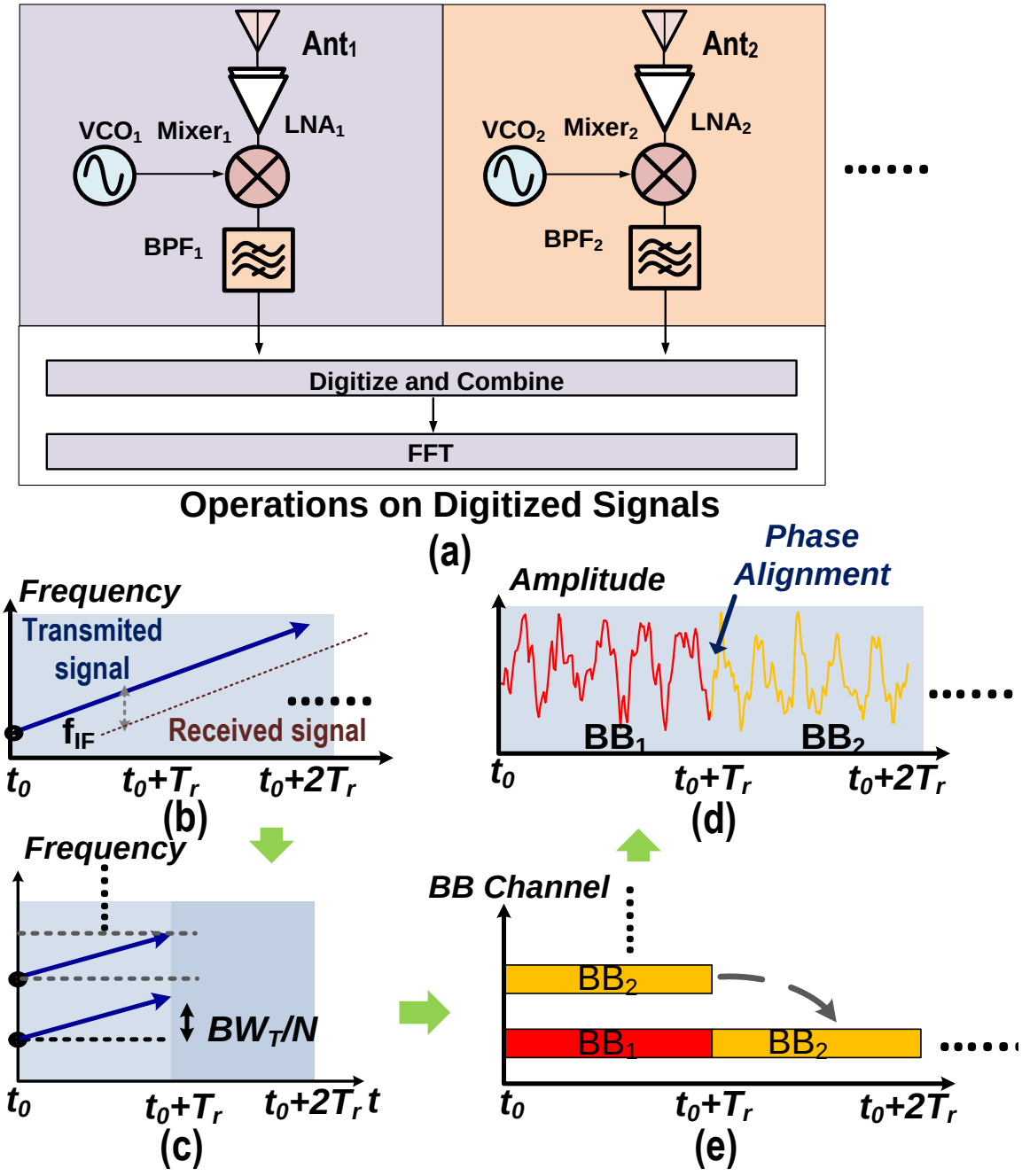

Figure 2.8: (a) Proposed stepped-band RX, (b) Conventional single-chirp FMCW signal, (c) stepped chirp FMCW signal, (d) stitched baseband signals in time domain with phase alignment, (e) resultant combined IF signal.

power consumption, ($P_{ADC} \propto f_{CLK} \times 2^{n_{bits}}$) [50].

As compared with one single-band FMCW radar 1TX-1RX architecture, where a single basedband signal is sampled by one ADC, the stepped chirp architecture has two baseband signals coming from RX_1 and RX_2, which combine in the digital domain to construct the same length of baseband signal as that of the single-chirp architecture. The signal processing is done by stitching different baseband signals [51] in time or frequency domain, as illustrated in Fig. 2.8(d)-(e). To analytically verify the RX principle of operation, we assume N transmitted chirps correspondings to the sub-bands of the form shown in Fig. 2.8(c):

$$TX_i(t) = \cos[2\pi(f_i + St) \cdot t + \theta_i], \;\; 0 \leq i \leq N-1, \tag{2.1}$$

where f_i is the initial frequency of the i-th chirp, $S = BW/T_r$ is the slope of each chirp, and θ_i is the initial phase of each chirp. Assuming a single target with a reflection coefficient σ_0 at distance R from the radar sensor, the reflected components of the sub-bands can be expressed as:

$$RX_i(t, R) = \sigma_0 \cos\{2\pi[f_i + S(t - \frac{2R}{c})] \cdot (t - \frac{2R}{c}) + \theta_i\} \\ , \quad 0 \leq i \leq N-1. \tag{2.2}$$

The intermediate frequency (IF) signal is obtained by mixing the TX and RX signals and get the lower frequency part as:

$$IF_i(t, R) = \frac{1}{2}\sigma_0 \cos(2\pi S \cdot \frac{2R}{c} \cdot t + 2\pi f_i \frac{2R}{c} - \pi S(\frac{2R}{c})^2) \\ , \quad 0 \leq i \leq N-1. \tag{2.3}$$

The term $\pi S(\frac{2R}{c})^2$ is small enough to be neglected. Therefore, the initial phase of IF signal is

only determined by the initial frequency f_i and round trip time $\frac{2R}{c}$. To validate the seamless stitching of the baseband waveform, consider two sub-bands. At the end point of the first sub-band (t = T_r), the phase of the first baseband is:

$$\varphi_{IF,1}(T_r, R) = 2\pi \cdot \frac{2R}{c} \cdot BW + 2\pi f_1 \frac{2R}{c}. \tag{2.4}$$

At the starting point of the second sub-band (t=0), the phase of the second baseband signal is:

$$\varphi_{IF,2}(0, R) = 2\pi f_2 \frac{2R}{c}. \tag{2.5}$$

The phase difference between these two points is given by:

$$\Delta\varphi_{IF} = \varphi_{IF,2}(0, R) - \varphi_{IF,1}(T_r, R) = 2\pi \cdot \frac{2R}{c} \cdot \Delta f. \tag{2.6}$$

where $\Delta f = f_2 - f_1$ is the frequency offset between the two sub-bands. In the real implementation, to mitigate frequency pulling, we selected f_1 = 50 GHz and f_1 = 57 GHz with BW = 5 GHz. The resulting phase difference $\Delta\varphi_{IF}$ is constant and independent of time.This constancy ensures that the baseband signals of the two sub-bands can be seamlessly aligned by compensating for $\Delta\varphi_{IF}$.

Moreover, because the chirp slope is identical across sub-bands (enforced by the mixing PLL), the stitched IF signal exhibits the same baseband peak as each IF signal. By applying FFT to the stitched baseband, an equivalent bandwidth of $N \cdot BW$ can be achieved, thus effectively enhancing the radar's range resolution.

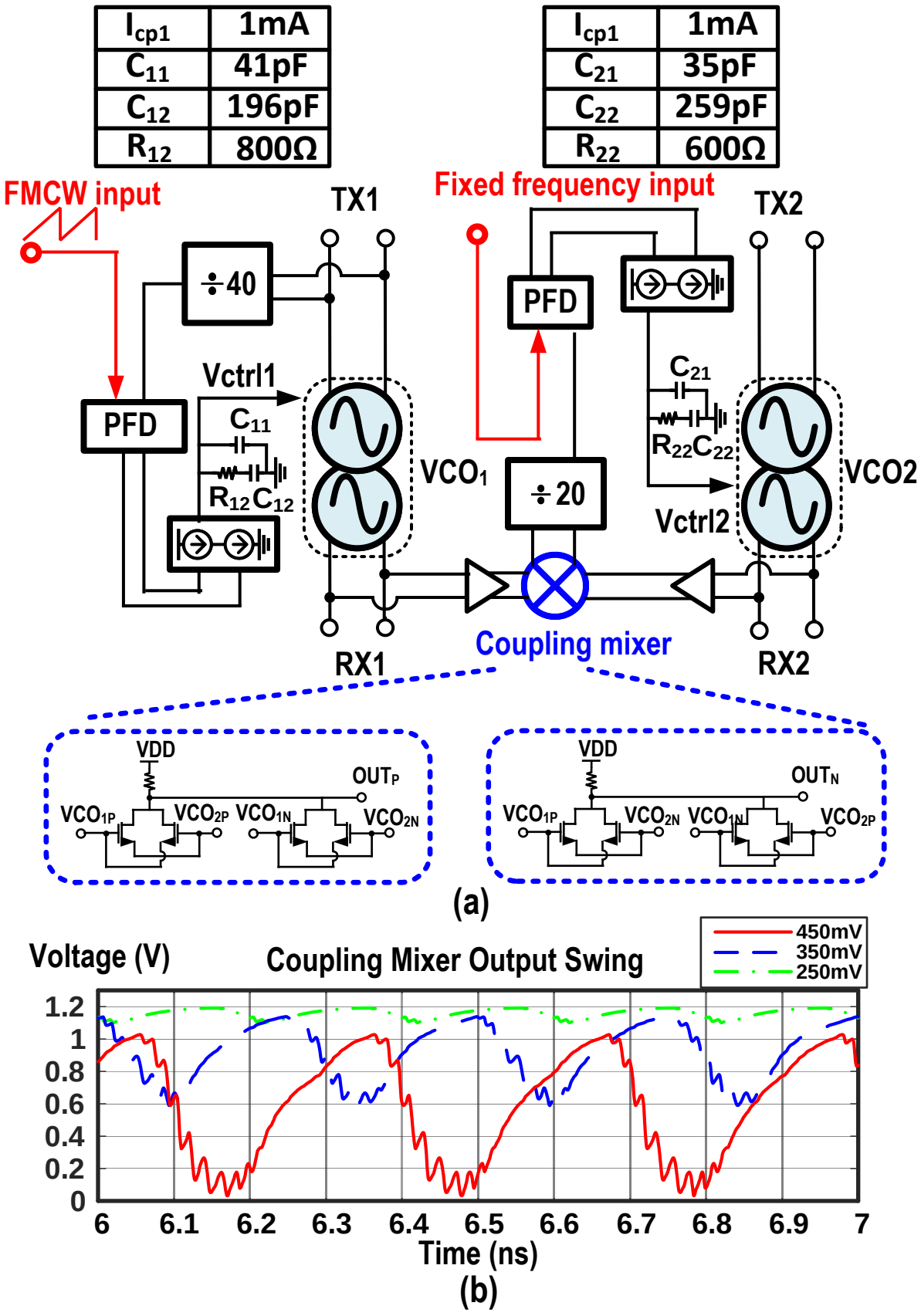

Figure 2.9: (a) Frequency synthesizer block diagram with values of RC loop filter and the schematic of the fully balanced coupling mixer. (b) Simulated output swing of the coupling mixer for input swings of 250 mV, 350 mV, and 450 mV.

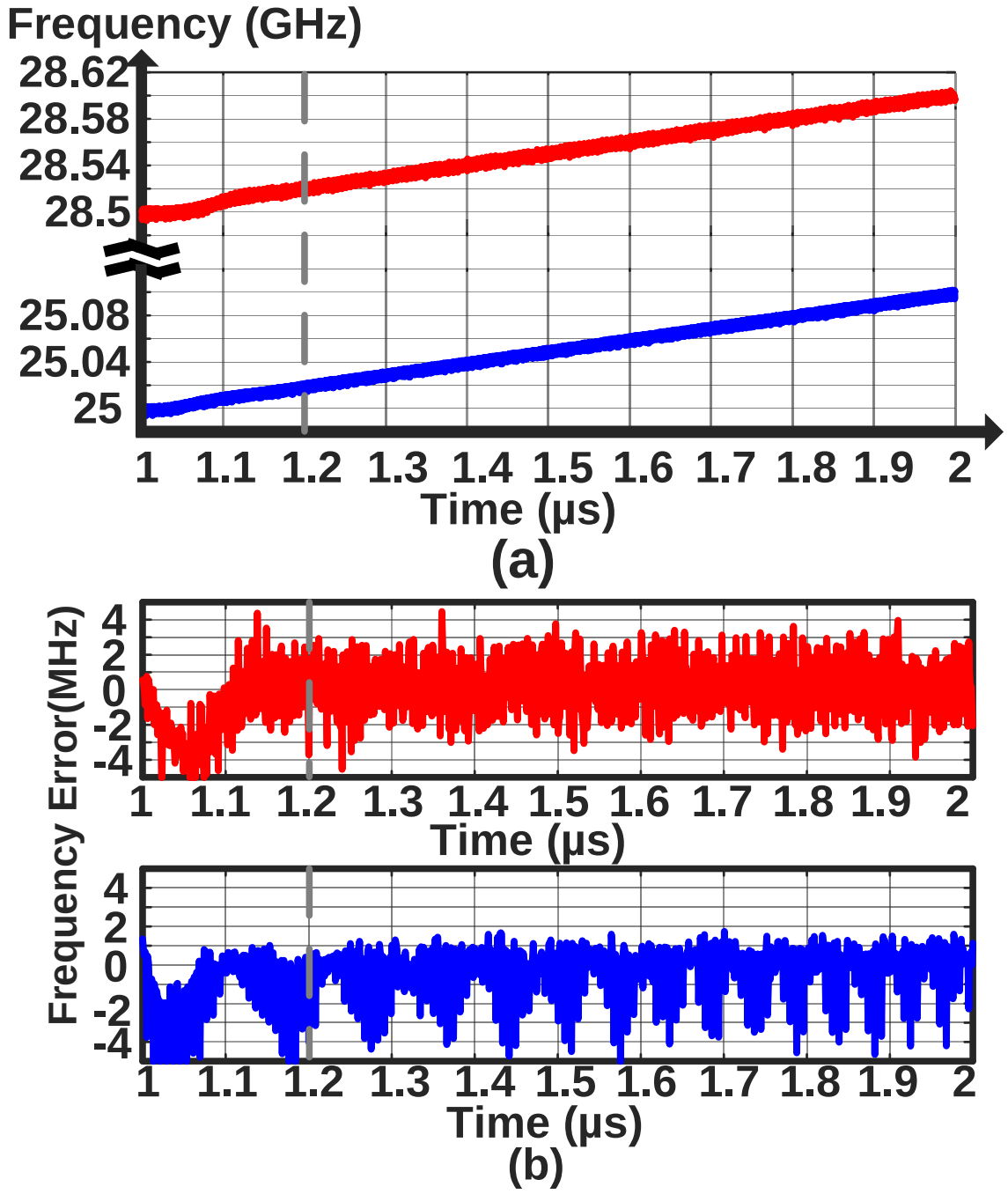

Figure 2.10: (a) Simulated chirp profile and (b) simulated freuqency error versus ideal chirp.

2.3 Circuit Implementation and Package

In this section, we will review the design and simulated performance of the circuit blocks inside the TX and RX, the chip-to-board interface and matching network, and the PCB patch antenna arrays.

2.3.1 Frequency Synthesizer

The frequency synthesizer block diagram is shown in Fig. 2.10. Both the reference and mixing PLLs are designed with a PFD, a CP, and a second-order loop filter. The outputs from both dual-core VCOs are directed to a low-power cross-connected differential fully balanced mixer block. The mixer's output is subsequently downconverted by a factor of 20. The input swing of the driving signal is crucial for properly driving the coupling mixer. The simulated output swing of the coupling mixer, as shown in Fig. 2.10 (b), demonstrates that a 450 mVpp driving signal is required to achieve a 1 Vpp output swing. To ensure this, we include a common-source (CS) buffer stage between the VCO and coupling mixer, which guarantees the 450 mV peak-to-peak input swing. The resulting 1 V peak-to-peak output is sufficient to drive the subsequent stage. The values of all the resistors and capacitors used in the second-order loop filter are provided in Fig. 2.10. The radar's targeted chirp rate is 200 MHz/μs, and the loop bandwidths of the reference and mixing PLLs are selected to be around 400 kHz and 380 kHz to meet the desired performance. The simulated chirp profile is shown in Fig. 2.10 (a). With the loop filter and charge pump current chosen accordingly, the chirp of the mixing PLL can be locked to that of the reference PLL. The frequency error between the simulated and ideal chirps is presented in Fig. 2.10 (b). Since the modulation of the mixing PLL chirp depends on the reference PLL, the RMS frequency error of the mixing PLL is higher than that of the reference PLL. Due to instability at the start of the chirp, the RMS frequency error is calculated from 1.2μs to 2μs. The simulated frequency RMS of

reference PLL and Mixing PLL are 1130kHz and 1564kHz respectively. The simulated power consumption of reference PLL and mixing PLL (excluding the VCOs) is 46.8 mW and 18.1 mW, respectively.

2.3.2 Voltage Controlled Oscillators

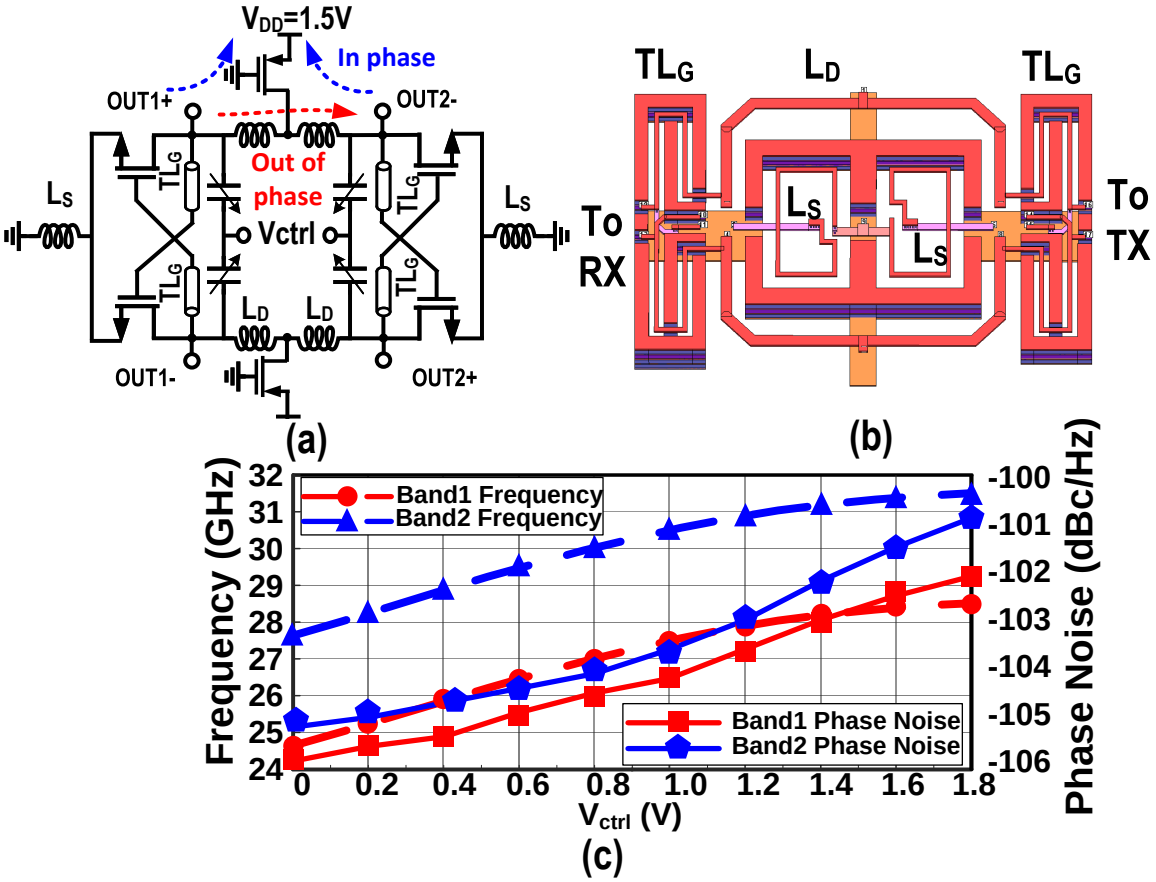

Figure 2.11: (a) Dual core VCO schematic (b) EM structure and (c) simulated frequency vs V_{ctrl} and phase noise at 1 MHz offset vs V_{ctrl}.

The principle of FMCW radar involves mixing the TX signal with a delayed and attenuated version received by the RX. Hence, it is common practice to share the LO signal between the TX and RX. In our design, we implement a dual-core coupled cross-coupled oscillator with source degeneration [6] as the core VCO for each sub-band, as shown in Fig. 2.11. The use of a dual-core VCO helps reduce signal routing complexity compared to using a

single-core VCO combined with buffers and power splitters. Additionally, the phase noise (PN) of the VCO can be improved by 10log(2)=3 dB by coupling two VCOs [52, 53]. The primary challenge in designing a functional dual-core VCO is the suppression of undesired oscillation modes. As illustrated in Fig. 2.11 (a), when OUT1+ and OUT2- are out of phase, they are in differential mode and the oscillatory current does not pass through the PMOS transistors connected to V_{DD}. Conversely, if OUT1+ and OUT2- are in phase (common mode operation), the current flows through the PMOS devices. In this case, the PMOS devices, with their gates grounded and operating in the triode region, act as lossy resistors that degrade the Q-factor of the LC tank. As a result, the common-mode oscillation is eliminated, allowing only the differential mode to persist.

Compared to conventional cross-coupled VCO, a short T-line is added between the gate and the drain to further boost the voltage swing at the transistor's gate [6]. A thick-oxide transistor is chosen to allow a gate voltage swing of up to 2.4 V ($2V_{DD}$), which contributes to larger voltage swings for better phase noise performance, while reducing flicker noise due to the larger gate area (W×L). The layout of each VCO is simulated with EM solvers to capture the coupling effect among the lines and inductors (Fig. 2.11(b)). Post-layout simulation results showing the frequency tuning range and phase noise characteristics of each sub-band VCO are shown in Fig. 2.11(c).

2.3.3 Doubler and Power Amplifier

In this design, we adopt a superharmonic configuration where the radiated frequency is twice that of VCO oscillation frequency in each sub-band. A push-push frequency doubler in Fig. 2.12(a) is adopted to upconvert the VCO signal, which is followed by a two-stage transformer-coupled differential PA [54, 55]. Since we use the differential signaling, the mutual coupling capacitors only help with differential mode stability [56]. A $4k\Omega$ resistor R_c is added at each

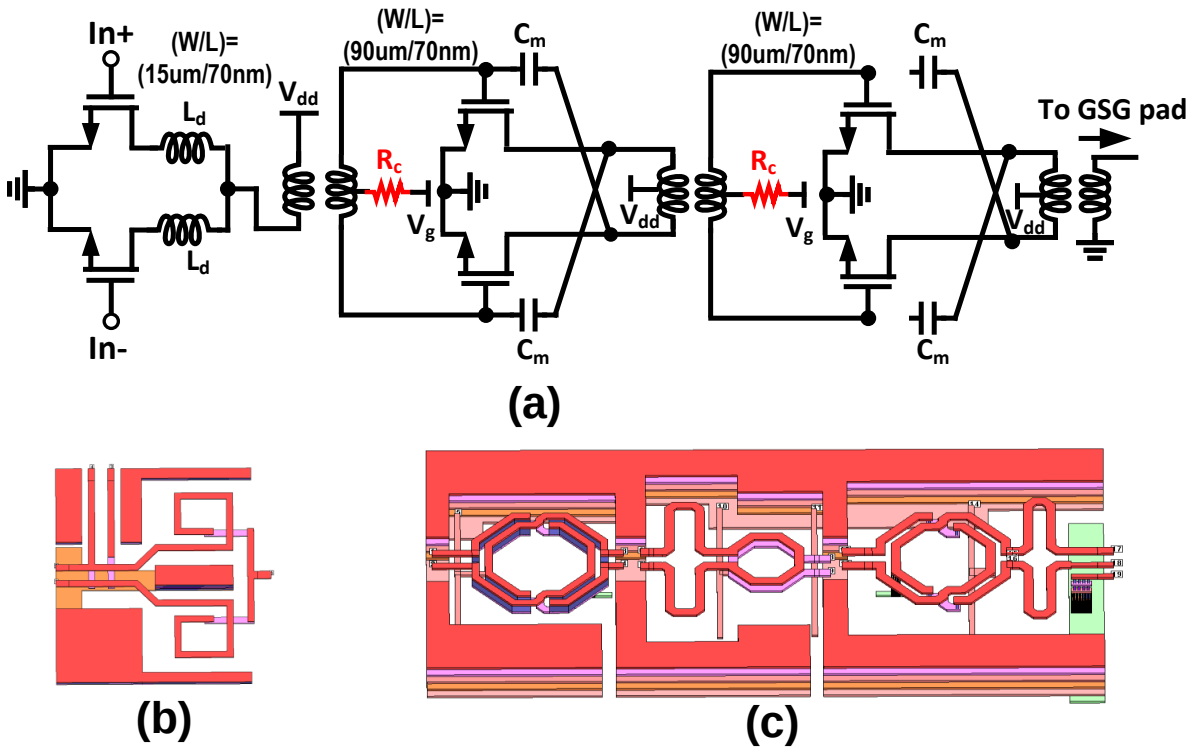

Figure 2.12: (a) Schematic of frequency doubler and PA, EM structure of (b) doubler and (c) PA.

gate bias DC node to suppress the common-mode oscillations.

For the first sub-band, the frequency doubler provides an output power of -5 dBm with an output impedance of $(20 + j10)$ Ω. A thick gate-oxide transistor with a 70-nm gate length is chosen for the PA to support higher supply voltage of 1.2 V, enhancing P_{sat}. The transistor widths for both stages are set at 30μm×3 for both stages based on the power and gain requirements. Impedance matching between the frequency doubler and PA input is accomplished using an input balun, while the interstage matching is achieved through a stacked transformer. To further enhance impedance matching across a 12 GHz bandwidth, an additional transmission line is incorporated within matching network. Finally, the output of the second stage is matched to 50-Ω load impedance through the output balun. Both the stages employ over-neutralization technique [57] to bring the device stability factor above $K_f = 1$, while increasing the gain. The EM-simulated layouts of the doubler and PA are shown in Figs. 2.12(b)-(c). The insertion loss of the input balun, interstage matching, and

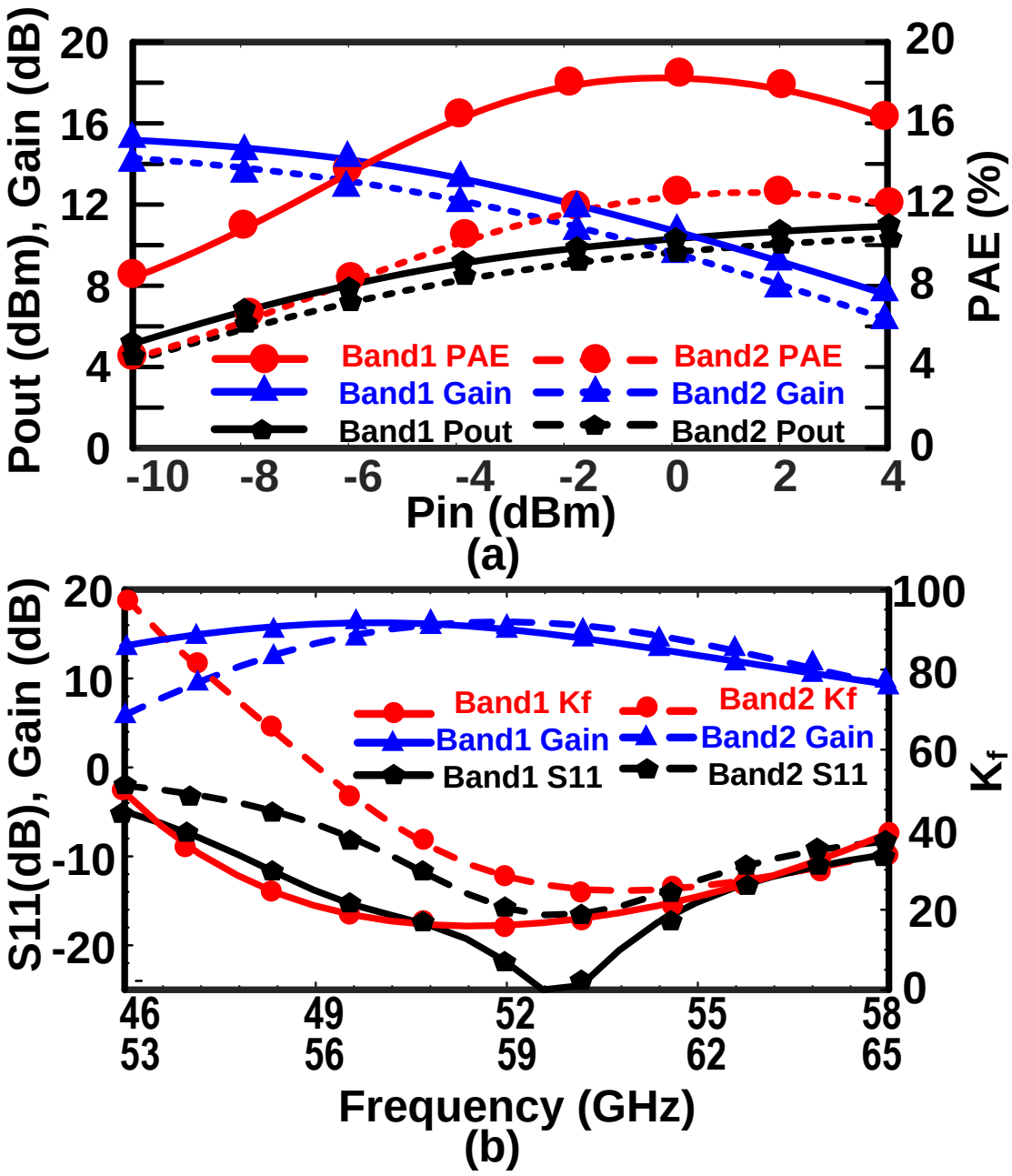

Figure 2.13: (a) PA Simulation results for band1 and band2 (a) P_{out}, Gain and PAE and (b) S_{11}, S_{21}, and K_f.

output balun varies between 1.2- and 1.8-dB. The S-parameter simulation results are shown in Fig. 2.13 (a) where 10 dB input-return is achieved across 46-58 GHz with a peak S_{21} of 16.3 dB and K_f of more than 24.7. The simulation plots for the output power (P_{out}), large signal gain, and power added efficiency PAE are shown in Fig. 2.13(b). A 6.75 dBm output power, 17.7% of PAE, and a large signal gain of 11.87 dB is attained for an input power of -5 dBm at 53 GHz.

The PA for the second sub-band, covering the 56-63 GHz frequency range, uses the same topology and device dimensions as the first band. The small signal S-parameter simulation results are presented in Fig. 2.13(a), showing a S_{11} better than]rc10 dB, a S_{21} of 14.5 - 15.8 dB, a K_f of greater than 15.9 across the designed band. The large signal simulation results, shown in Fig. 2.13(b), indicate that for the doubler's output power of -5 dBm and the output impedance of $(20 + j20)\ \Omega$, the PA delivers an output power of 6 dBm, a PAE of 11.5%, and a large-signal gain of 11 dB at 60 GHz.

2.3.4 LNA and Mixer

A three-stage single-ended cascode LNA is employed in this design, where the first-stage schematic is shown in Fig. 2.14(a). The LNA's EM layout is shown in Fig. 2.14(b) where inductors are co-simulated to capture any unwanted mutual coupling. The input transistor is biased at optimum DC current to achieve a lower NF_{min}. An inductor L_M is inserted between common-source and common-gate devices for a better power and noise matching [58, 59]. The EM-simulated layout of the LNA is shown in Fig. 2.14(b) and the simulated LNA single-stage gain and NF for each sub-band are shown in Fig. 2.14(c).

Following the LNA, a double-balanced passive mixer (Fig. 2.15(a)) is deployed. Since no DC current passes through the switching transistor [60–62], the flicker noise from these switching transistors is substantially reduced. Additionally, the mixer is connected to a large PMOS

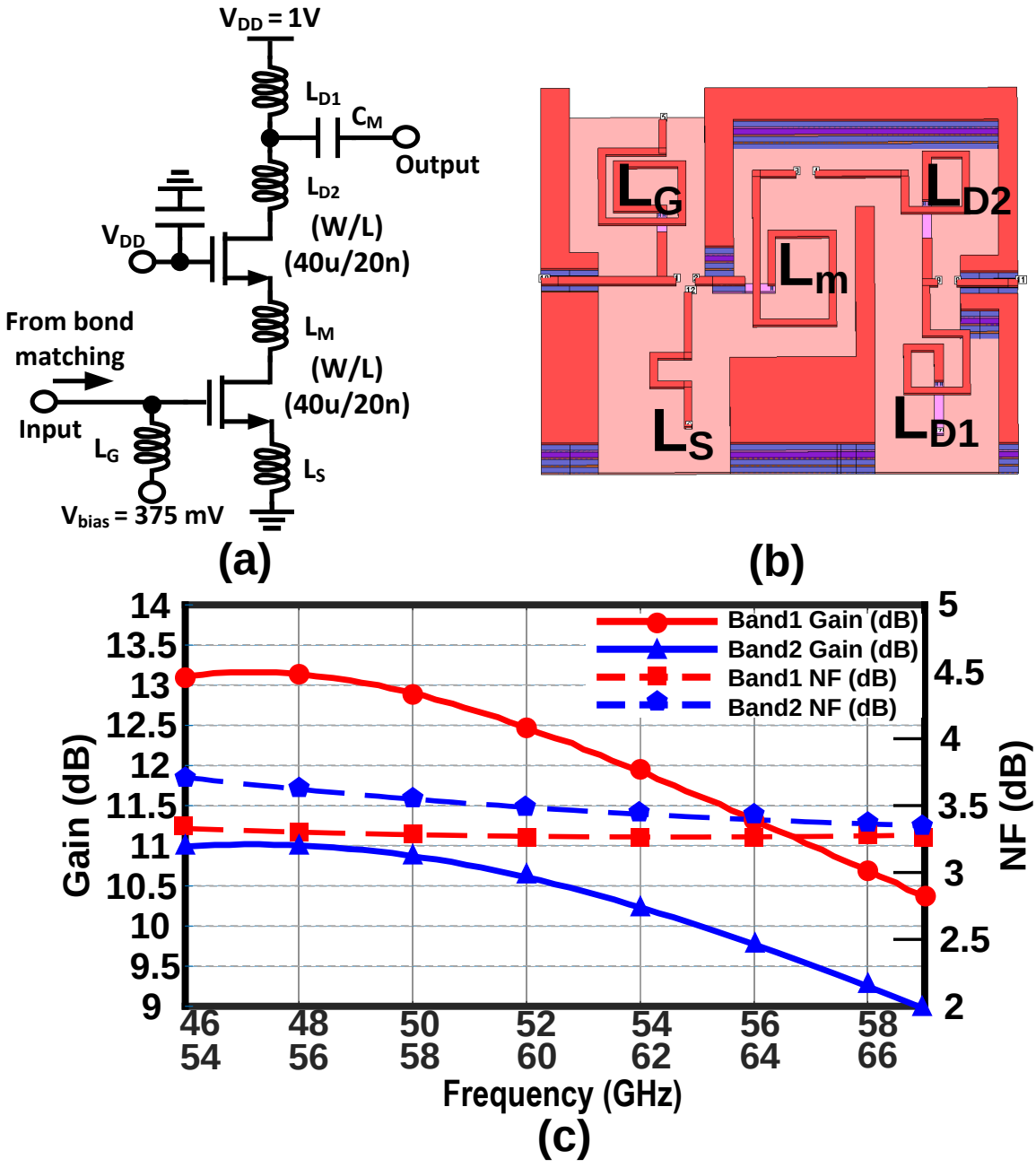

Figure 2.14: (a) LNA schematic (b) LNA EM structure, (c) Simulated conversion gain and NF for low frequency band and high frequency band.

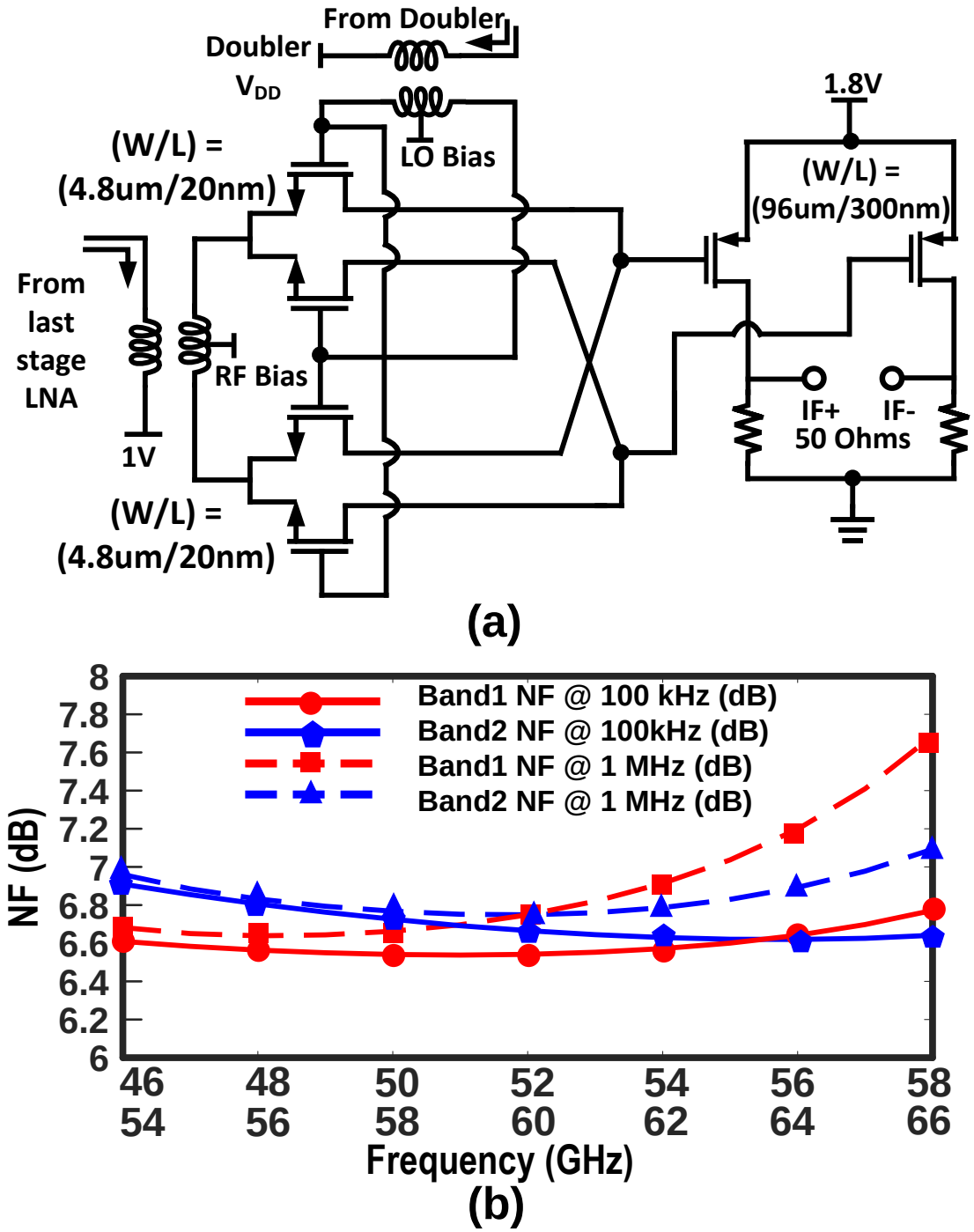

Figure 2.15: (a) Passive mixer and buffer schematic (b) simulated NF at 100 kHz and 1 MHz offset.

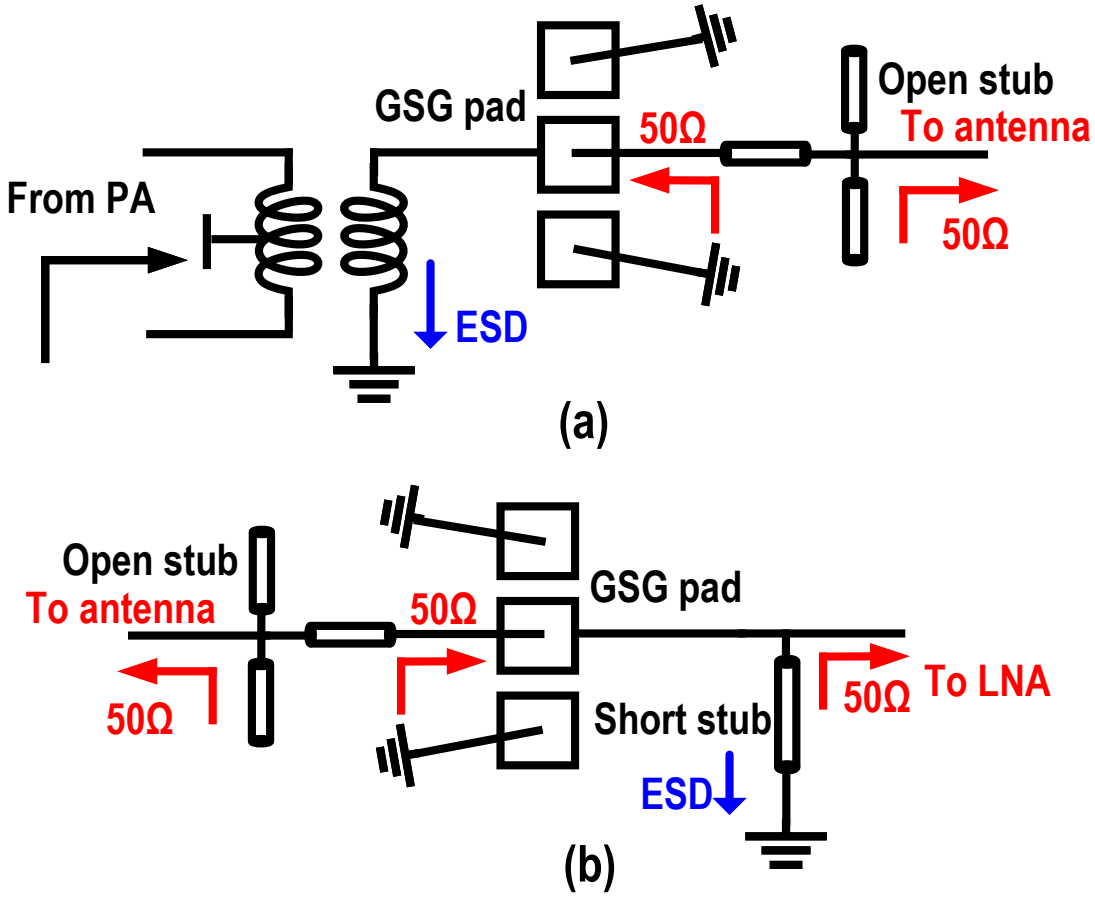

Figure 2.16: Illustration of (a) TX packaging matching and (b) RX packaging matching.

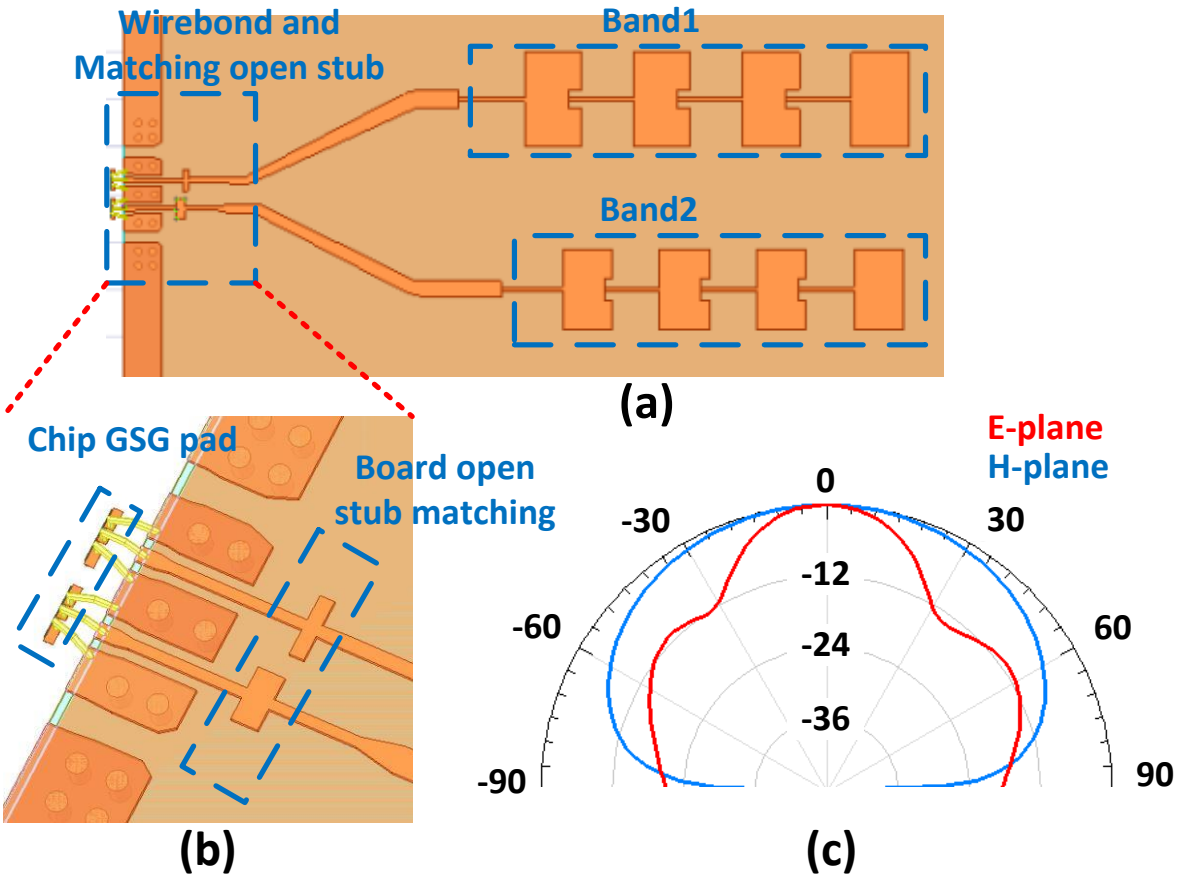

Figure 2.17: (a) Top view of antennas, (b) simulated radiation pattern.

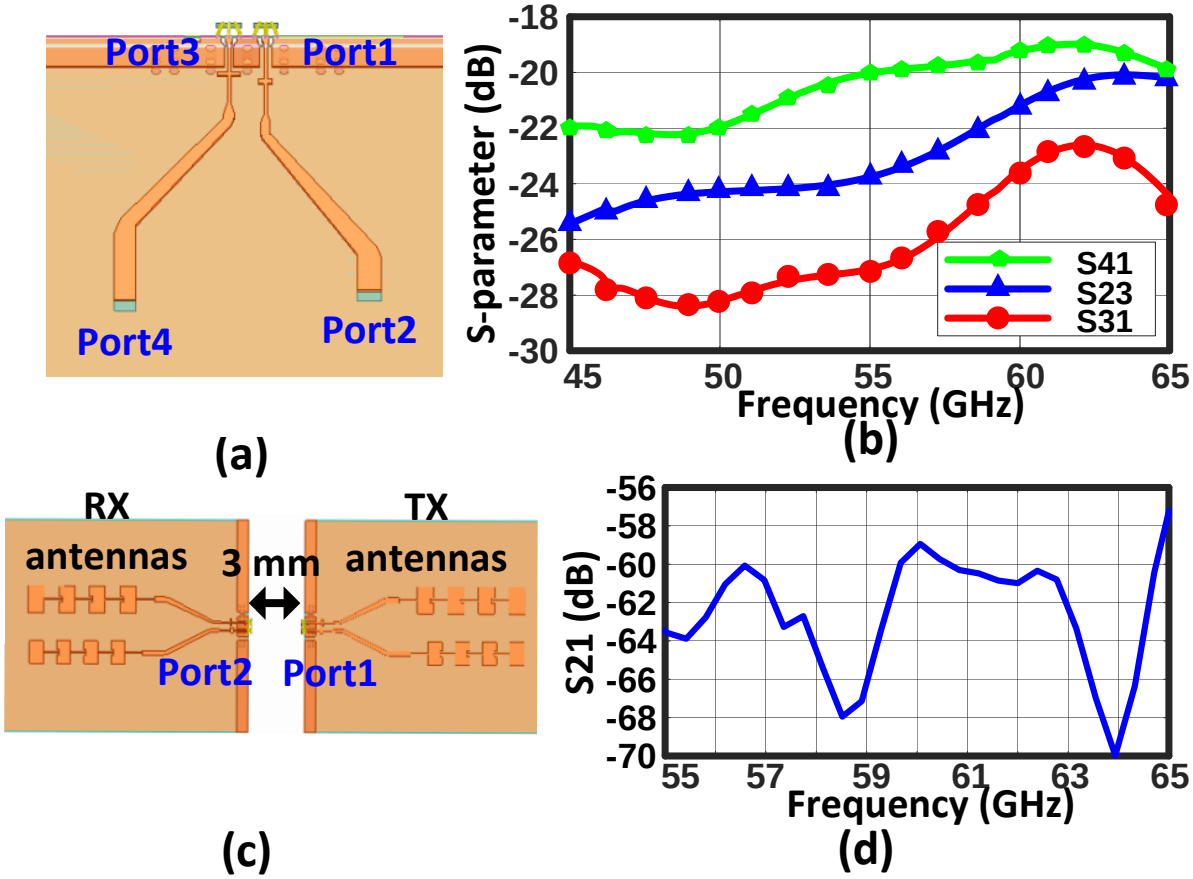

Figure 2.18: (a) EM simulation testbench for characterizing isolation between adjacent channels, (b) simulated S_{41}, S_{23} and S_{31}, (c) EM simulated TX to RX leakage characterization, (d) simulated S_{21} representing TX to RX leakage.

transistor (W/L = 96μm/300nm), introducing a large capacitive load to reduce the impact of flicker noise on the radar operation. In this design, flicker noise suppression is critical since the baseband range of interest is designed to be below 20 MHz. The total simulated NF at both 100 kHz and 1 MHz offset frequencies for both sub-bands is shown in Fig. 2.15 (b). The NF at 100 kHz offset is just around 1dB higher than that at 1 MHz, highlighting the advantage of passive mixer and large capacitive load.

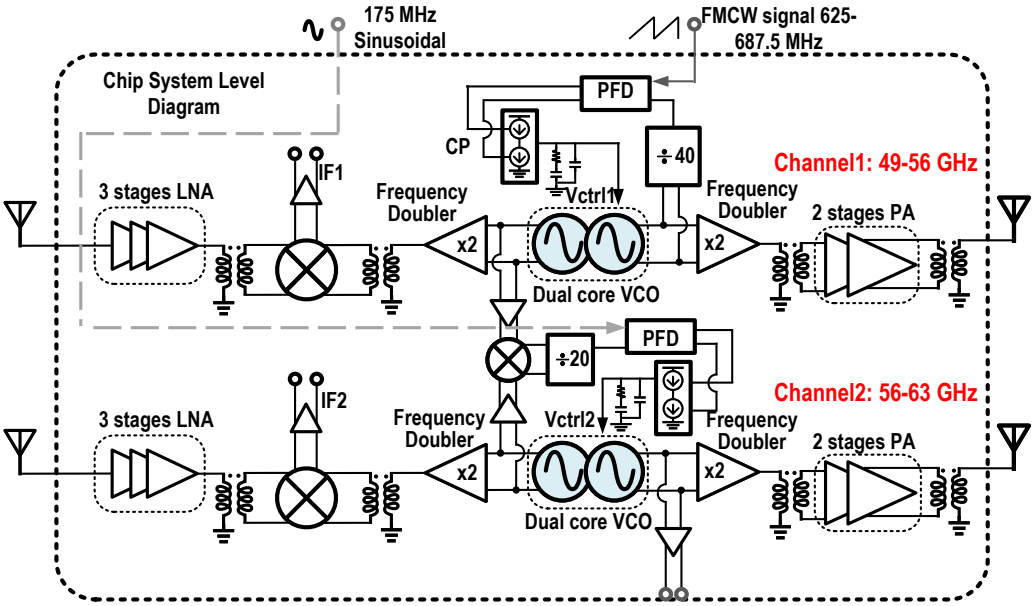

Figure 2.19: Detailed Transceiver block diagram.

2.3.5 Wirebond Matching and Antenna design

At higher operation frequencies, the design of the chip-to-board interface becomes crucial in minimizing losses between the PA and antenna, ensuring maximum radiated power. Wirebonding, while low cost and highly durable for low-frequency packaging, suffers from large parasitic inductance that limits the bandwidth. This limitation highlights the importance of the stepped chirp architecture, wherein each channel only needs to cover 7 GHz.

For matching on the chip side, electrostatic discharge (ESD) protection at the pad interface must be considered. On the TX side, a balun is used to convert the differential signal to

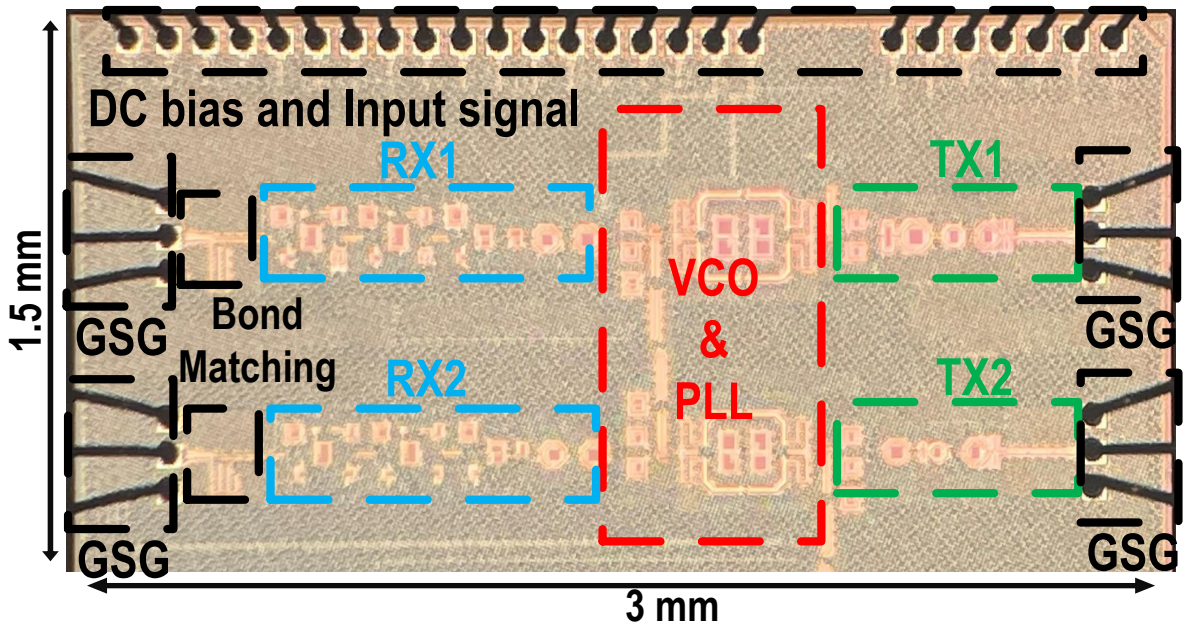

Figure 2.20: Chip Microphoto

single-ended. The short-to-ground inductor can serve as the ESD protection element while also matching the impedance at the GSG pad to 50Ω, as illustrated in Fig. 2.16(a). An open stub is added on the board to cancel out the parasitic effects introduced by the wirebond and transform the impedance back to 50 Ω for the antenna. The RX side matching is similar to the TX side, as shown in Fig. 2.16 (b). However, since the LNA is single-ended, a short stub is used to match the parasitic capacitance of the GSG pad. The HFSS view of chip-to-antenna interface is shown in Fig. 2.17(a), with a zoomed-in view of the interface shown in Fig. 2.17(b). Each sub-band employs a series-fed linear array of microstrip patch antennas. Patch antennas are commonly used in FMCW radars due to their compatibility with planar feed structures and their ability to provide broadside radiation [23, 63]. HFSS simulations indicate that the insertion loss of the interface network stays below 1.5 dB across both frequency bands, justifying the use of wirebond for the interface. The simulated radiation pattern of the antennas is shown in Fig. 2.17(c), where more than 7 dBi of realized gain is achieved for each sub-band antenna array. Two-band series-fed patch antennas are designed to balance between the FoV and directivity, e.g., wide beamwidth for H-plane and narrow beamwidth for E-plane, as shown in Fig. 2.17(c).

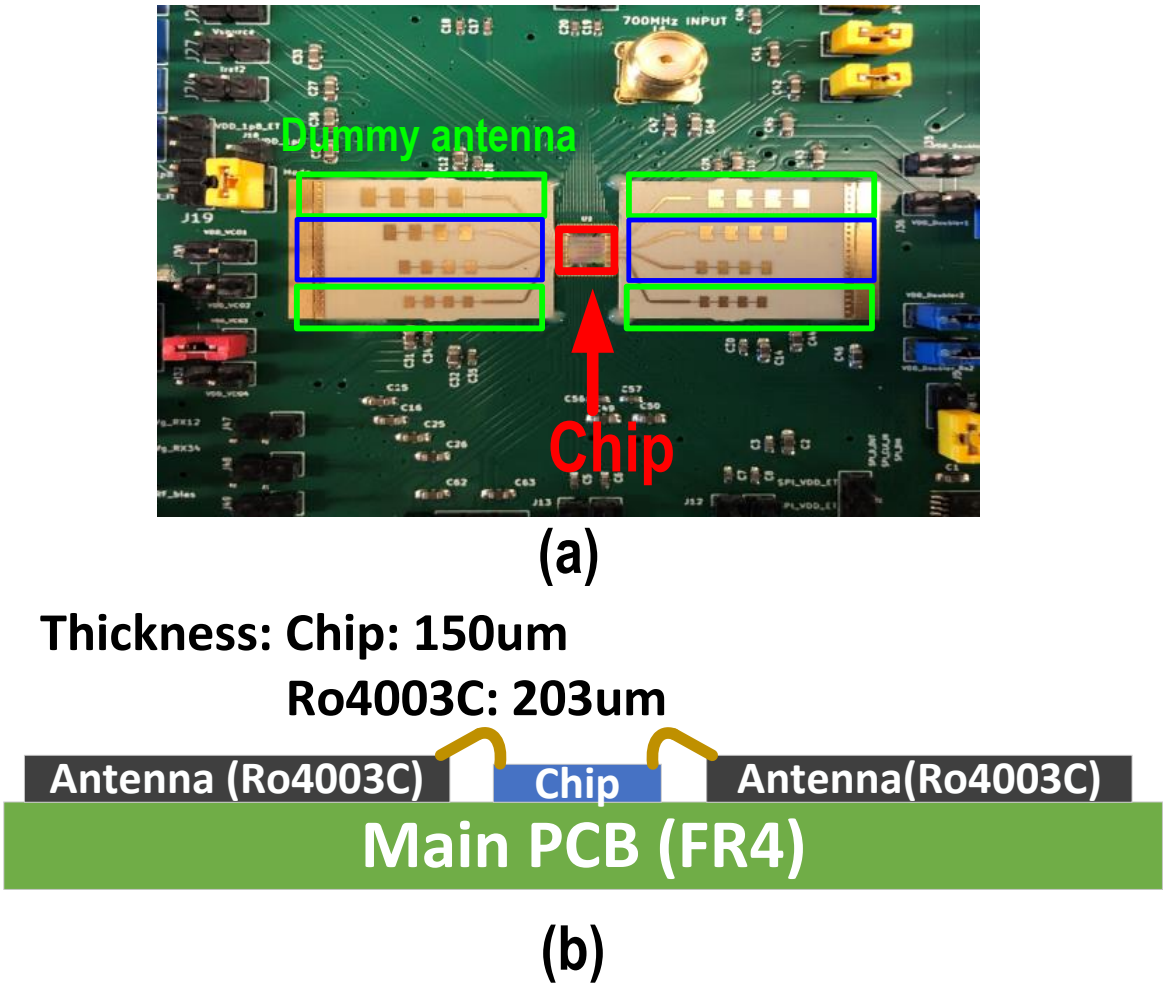

Figure 2.21: Board design: (a) top view, (b) cross-section view

The coupling between two adjacent bands was simulated by replacing the series fed patch antenna with a lumped port, as illustrated in Fig. 2.18(a). The electromagnetic (EM) simulation results, shown in Fig. 2.18(b), indicate attenuations exceeding 19 dB. The TX to RX leakage due to the standalone antenna was also simulated, as depicted in Fig. 2.18(c). The simulation setup places the two antenna boards at a separation distance of 3 mm to accommodate the chip. The isolation between TX and RX is below -58 dB across the 55 GHz to 65 GHz frequency range as shown in Fig. 2.18(d). It should be noted that this simulation only characterizes the coupling between the two antennas due to radiation and does not account for on-chip TX-to-RX leakage.Two other mechanisms in this design provide more isolation between adjacent bands for both transmitter and receiver antennas: (1) the bandpass profile of the antennas, each centered at its designated sub-band frequency, (2) the input matching network comprising the chip-to-board interface and the LNA input matching, designed to capture only the target sub-band bandwidth.

2.4 Measurement Results

The complete circuit block diagram of the CMOS transceiver excluding the antenna and interface is shown in Fig. 2.19. Shown in Fig. 2.20, the proposed radar TRX was fabricated in 22nm FD-SOI CMOS, occupying 4.5 mm^2 of die area including pads. The TX and RX antenna arrays, shown in Fig. 2.21(a), were fabricated using Rogers 4003C. The two dummy antennas, positioned at the top and bottom, were added to mitigate process variations caused by the bending of the Rogers material[23]. Each linear-fed antenna array can achieve up to 8% radiation bandwidth. As shown in Fig. 2.21(b), the antenna board and chip were glued on top of the platform FR-4 PCB, which also included the DC regulators and PLL input signal. To examine the operation of the proposed radar, three separate types of measurements were conducted; (I) stand-alone TX, (II) stand-alone RX, and (III) radar

transceiver measurements. In what follows, the specific measurements for each of these tests are provided and explained.

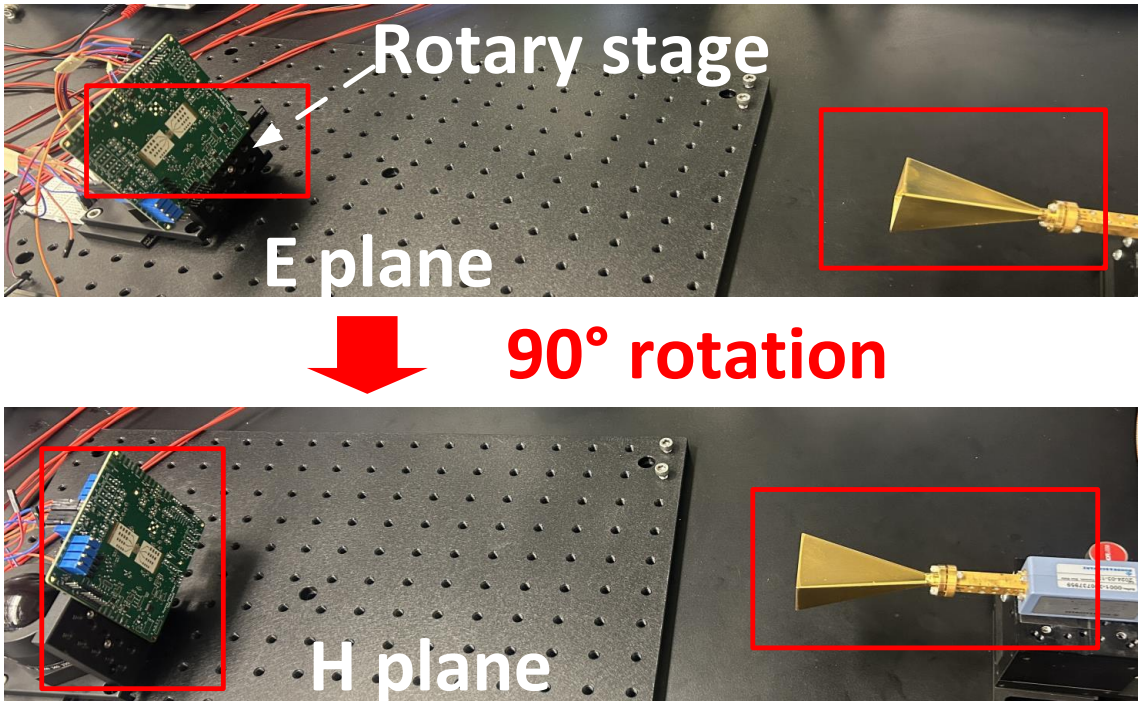

Figure 2.22: Antenna pattern measurement for both E-plane and H-plane.

2.4.1 TX Measurements

The TX/PLL measurement setup is shown in Fig. 2.24. To measure the radiation pattern of the TX antennas, the chip was mounted on a rotational optical stage and the diagonal horn antenna was kept still (Fig. 2.22). Both E-plane and H-plane measurements of the radiation pattern were conducted for both frequency bands using this technique and the results are provided in Fig. 2.23. Both antenna arrays achieve more than 6.5 dBi of measured realized gain.

Wireless testing was performed at distances exceeding 15 cm, beyond the Fraunhofer distance, to evaluate frequency and spectrum performance. The received signal was collected using a diagonal horn antenna, and the effective isotropic radiated power (EIRP) was mea-

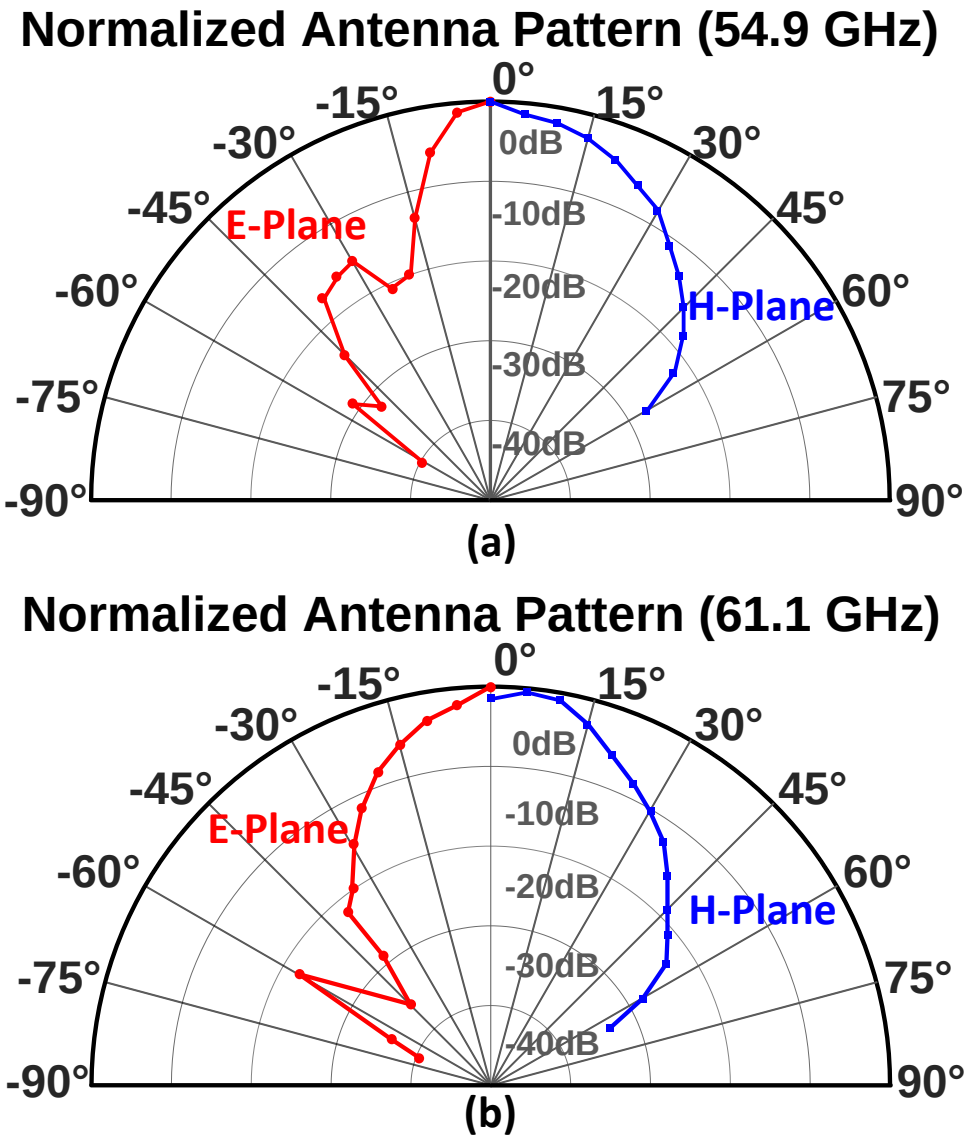

Figure 2.23: Measured normalized antenna pattern at (a) 54.9GHz (low frequency band) and (b) 61.1GHz (high frequency band).

sured with a power sensor and power meter. For phase noise and spectral measurements, the received signal was fed to a spectrum analyzer, with measurements taken in both free-running and phase-locked modes. In phase-locked mode, a 175 MHz external reference was injected into the mixing PLL, while a ramp input signal between 625-687.5 MHz was applied to the reference PLL.

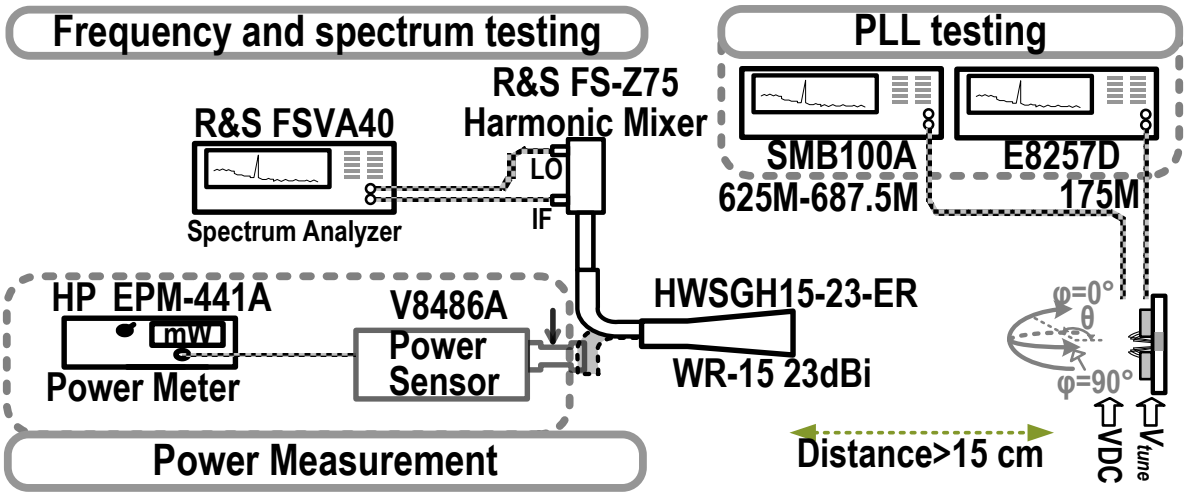

Figure 2.24: TX and PLL measurement setup

The far-field EIRP measurements were repeated for various distances, and are shown in Fig. 2.25(a), where a close match between the received power with that estimated by the Friis equation [27] are observed. The peak EIRP is above 9 dBm for low frequency band and above 8 dBm for high frequency band. The power variations across the two sub-bands is attributed to the frequency-band mismatch between antenna and PA as well as 3 dB loss for deviated PA output load impedance due to process variations and shift in operation frequency.

For spectral measurements, two separate sets of measurements were conducted for the free-running and phase-locked operations. On the TX side, the bandwidth of free-running and phase-locked operation and the corresponding phase noise profiles were measured, as shown in Figs. 2.26, 2.27, and 2.28, respectively. Each sub-band achieves close to 7 GHz of free-running bandwidth in Fig. 2.26. However, the preferred mode of operation for this radar is phase-locking mode, the frequency separation between the two sub-bands is precisely

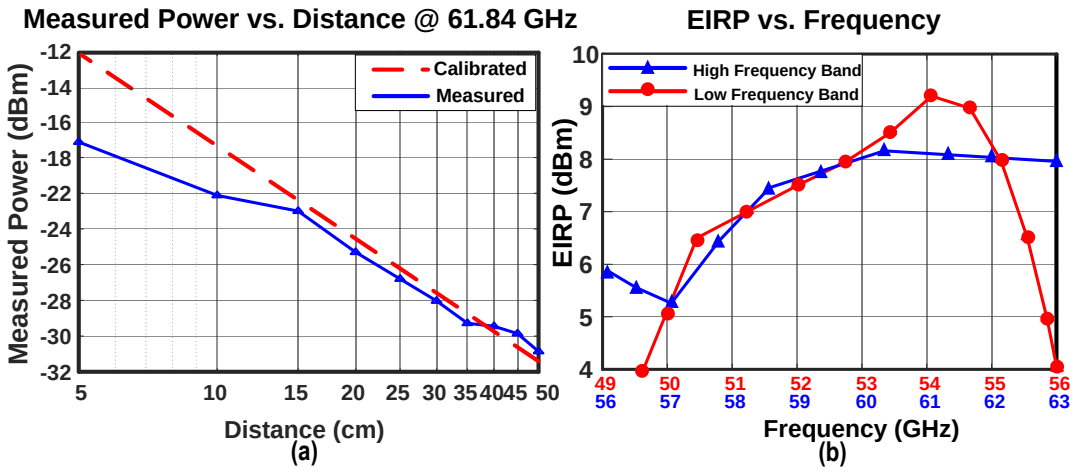

Figure 2.25: (a) Close match of power profile with Friis formula at 61.84 GHz (b) Measured EIRP from 49 GHz to 63 GHz.

controlled. This is demonstrated in Fig. 2.27 where the external input to the mixing PLL sets Δf to 7.5 and 7 GHz for the respective scenarios shown in Fig. 2.27. The two pairs of spurs introduced by the input signals do not impair radar operation, since their spacing ($\Delta f/40$) exceeds the 20-MHz IF bandwidth of this radar, with all the spurs occurring at multiples of $\Delta f/40$. According to the measurement results, the TX can achieve a phase-locked radiation bandwidth of 10 GHz. The smaller bandwidth of phase-locked mode compared to the free-running scenario is attributed to the PLL loop bandwidth, which limits the frequency tuning for stable loop operations. Phase noise measurement at different spot frequencies under phase-locked operation are shown in Fig. 2.28. The phase noise at 1-MHz offset are -96.39 and -101.7 at 52.16GHz and 56.01 GHz, respectively. The locked loop bandwidth varies between 200- to 500-kHz across all these samples.

To demonstrate the simultaneous phase-locked operation of the radar for the two adjacent sub-bands, multiple dual-band measurements were conducted where the reference and mixing PLLs were enabled for variable bandwidth associated with each sub-band. Three narrow-band operation scenarios (bandwidth of each band below 1.4 GHz), medium resolution (combined bandwidth of 8.2 GHz), and high-resolution (combined bandwidth of 10 GHz) were captured, and the corresponding spectrums are shown in Fig. 2.29. An impor-

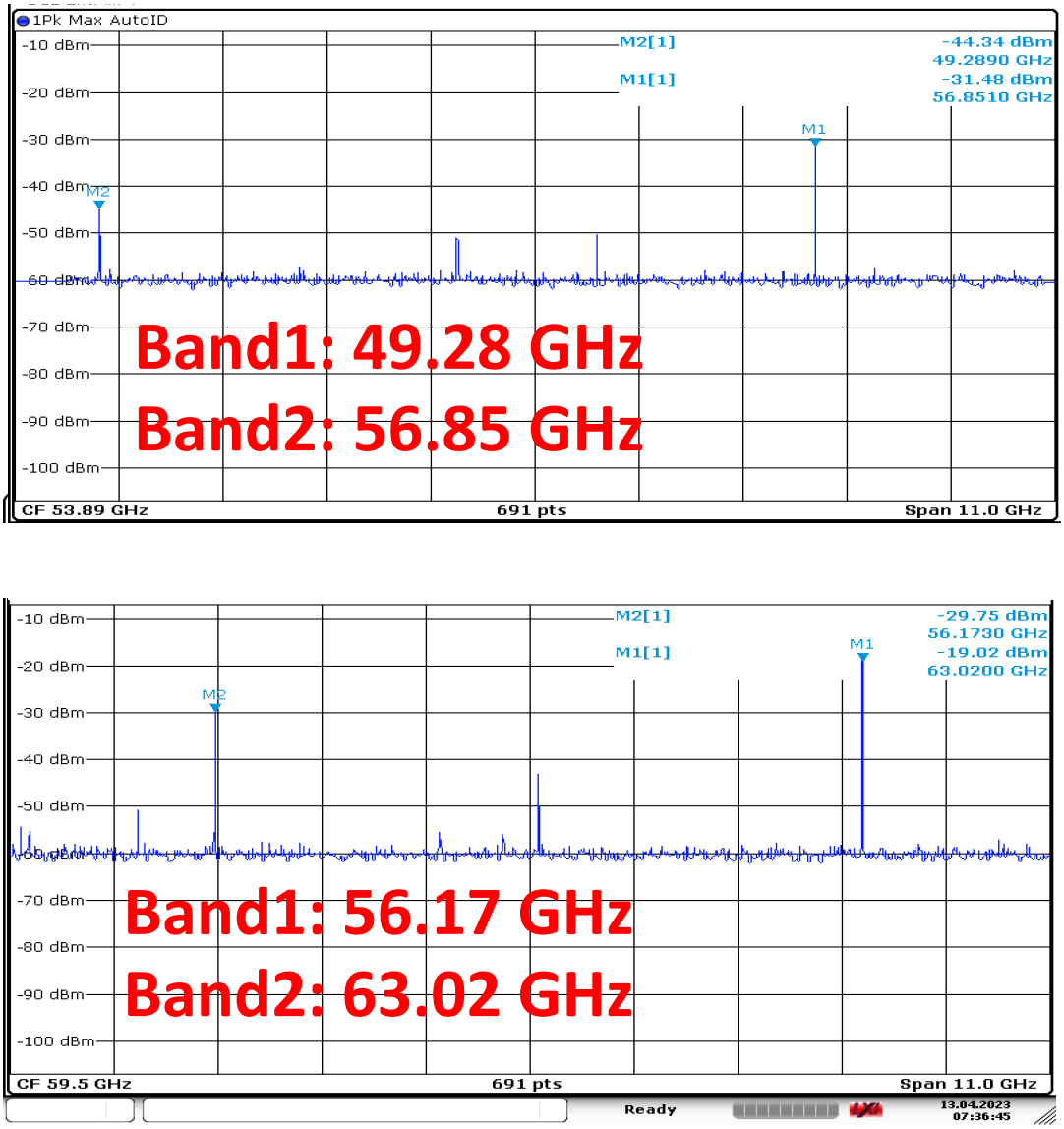

Figure 2.26: Free running operation at minimum and maximum frequencies.

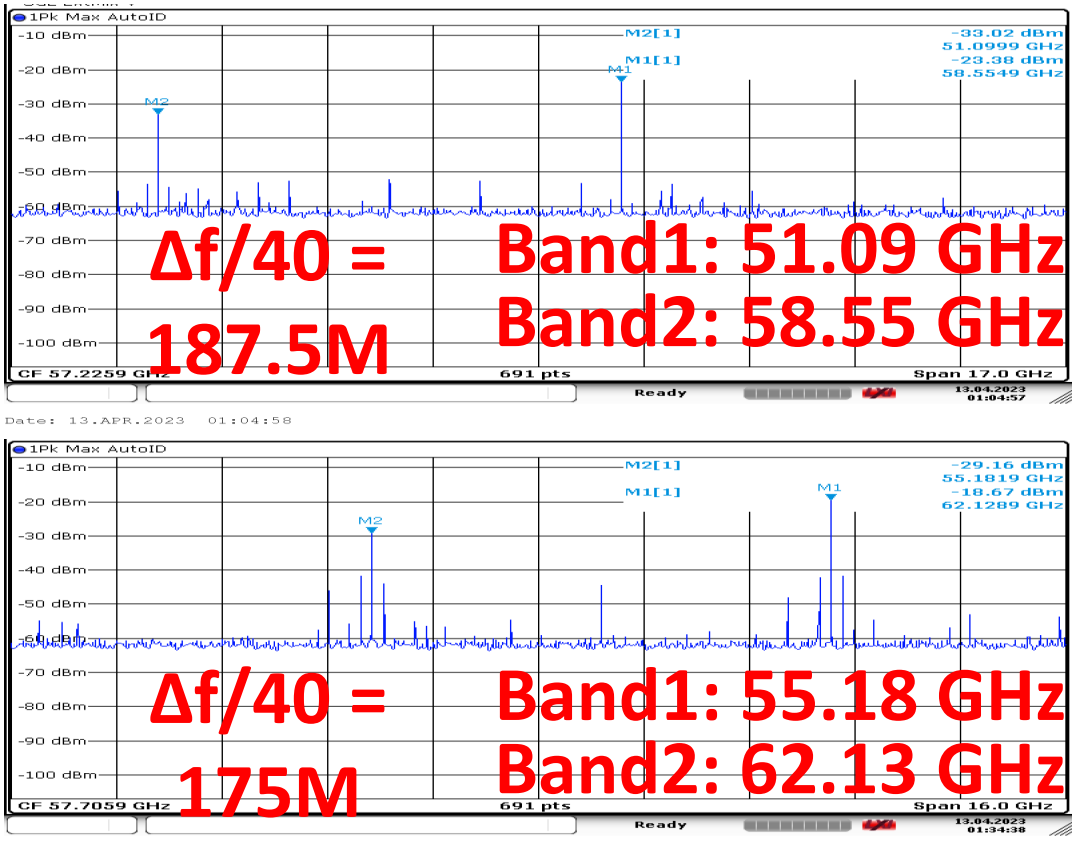

Figure 2.27: Phase locked operation at two distinct PLL reference frequencies.

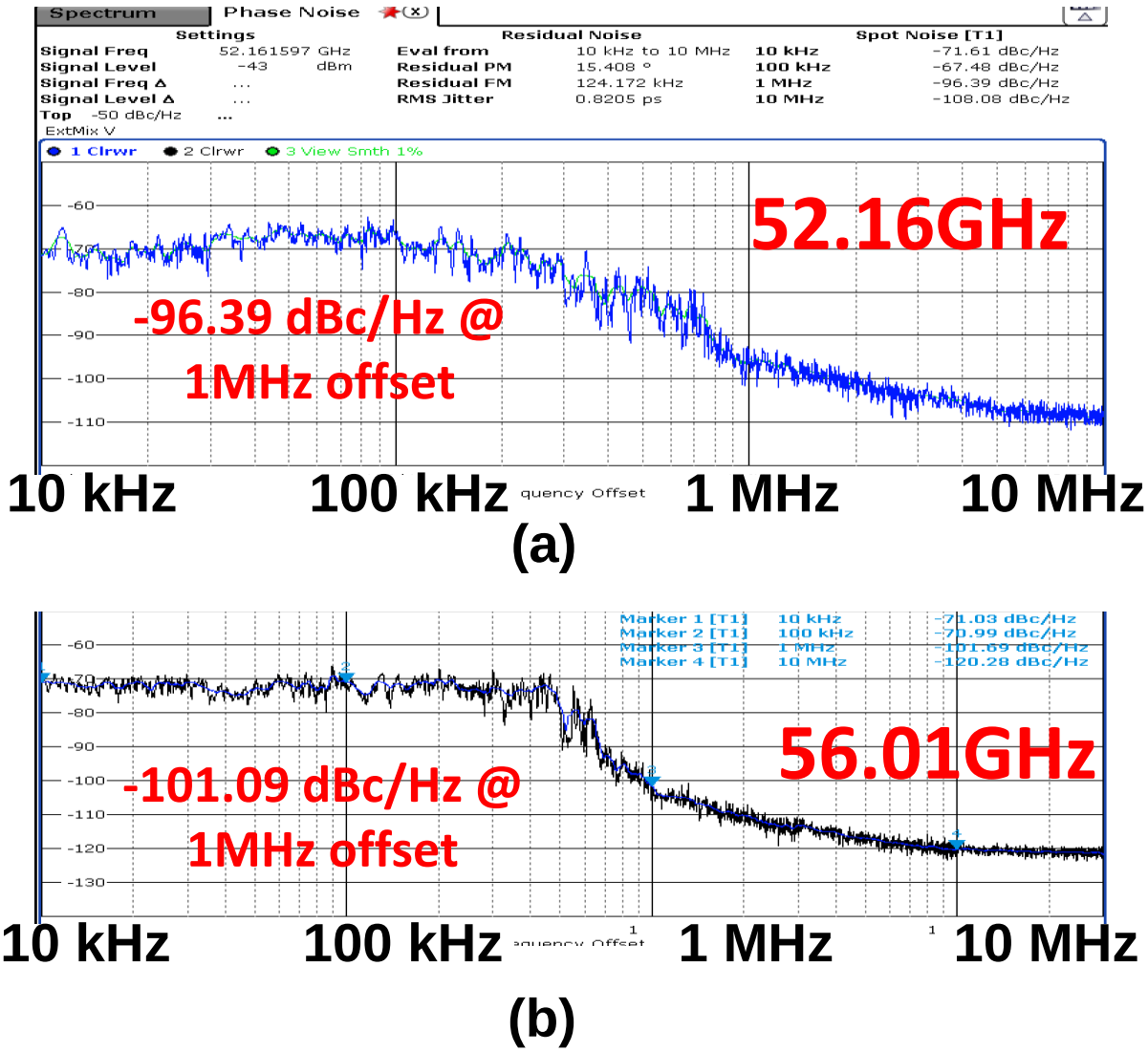

Figure 2.28: Measured phase-locked phase noise profile at 52.16 and 56.01 GHz.

tant feature of this radar is similar output power profiles of the two sub-bands under various bandwidths, enabling adjustable range resolution to suit different applications.

A chirp profile measurement was carried out using the measurement setup in Fig. 2.30 (a), where the tsignal was downconverted using an R&S FS-Z75 and analyzed on an R&S RTP164B with VSA software. The setup block diagram is shown in Fig. 2.30 (b). The measured dual-band chirp profiles under locking conditions are presented in Figs. 2.31 (a) and (b) for modulation bandwidths of 200 MHz and 1 GHz per sub-band, respectively. The measured RMS frequency errors for a 200 MHz modulation bandwidth in the low and high-frequency sub-bands were 716 kHz and 1.844 MHz, respectively. At a 1 GHz modulation bandwidth, the measured errors increased to 1.367 and 2.664 MHz in the low and high-frequency sub-bands, respectively.

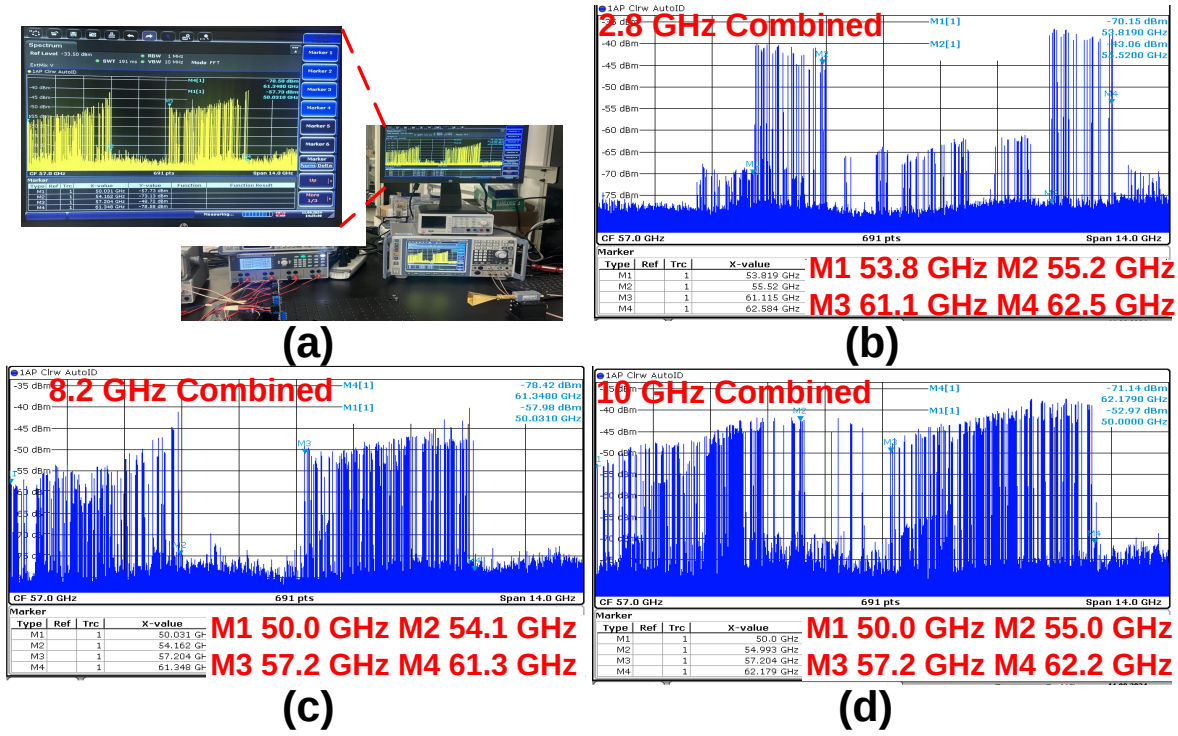

Figure 2.29: (a) Dual band operation measurement setup (b) 2.8 GHz bandwidth, (c) 8.2 GHz bandwidth, (c) 10 GHz bandwidth.

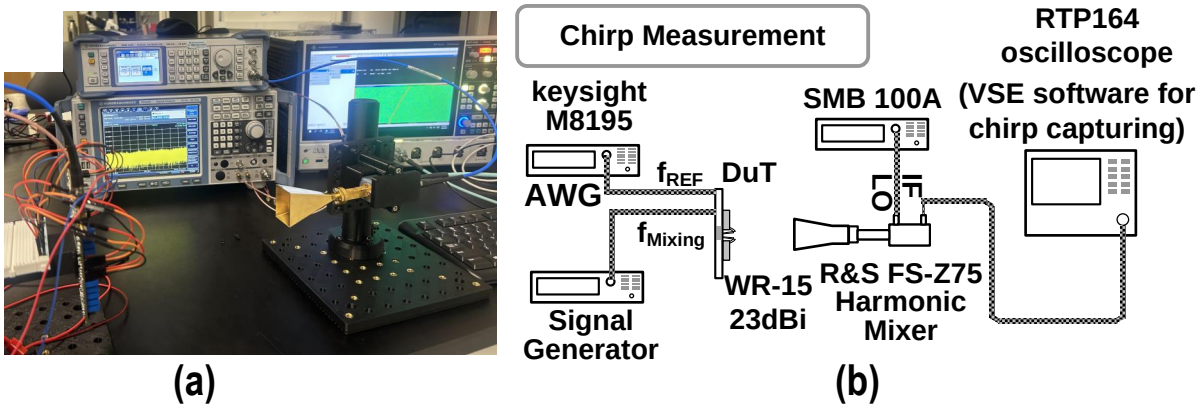

Figure 2.30: (a) Chirp measurement setup using an oscilloscope, (b) Block diagram of the measurement setup.

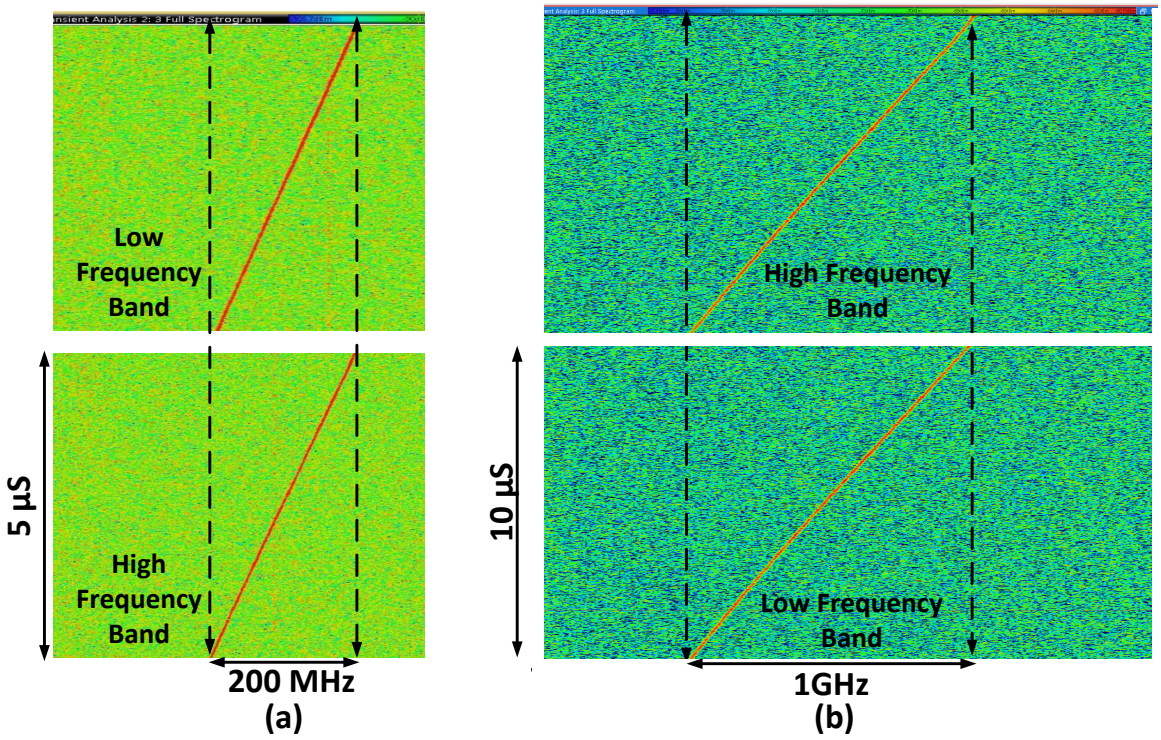

Figure 2.31: Dual-band chirp operation for (a) 200 MHz bandwidth and (b) 1 GHz bandwidth per band.

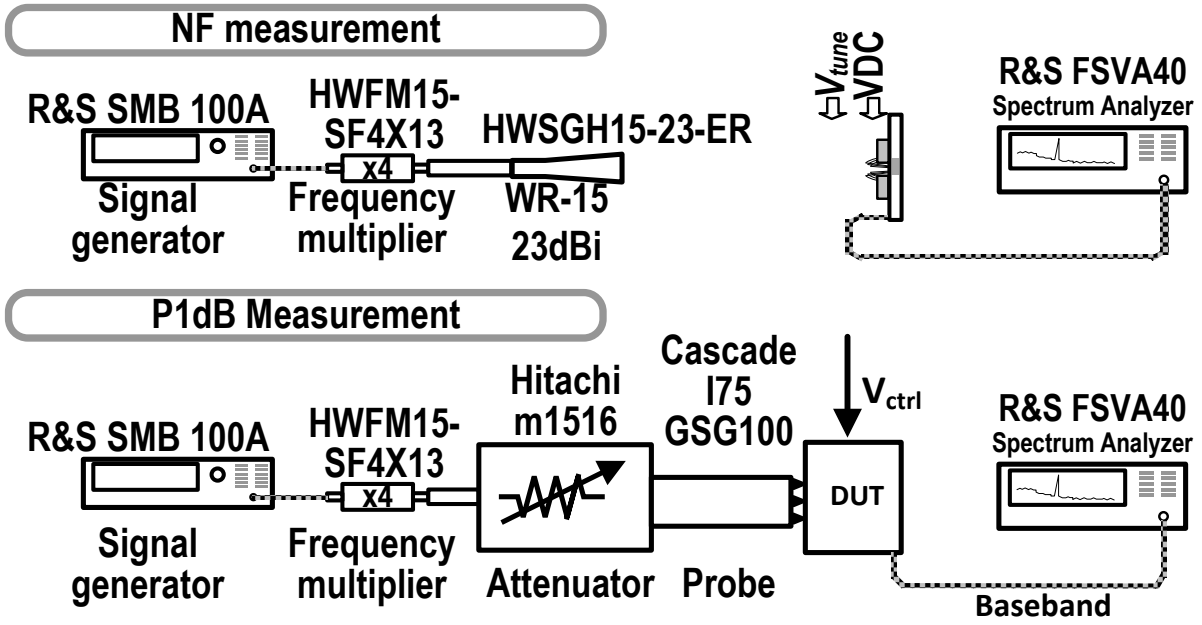

Figure 2.32: Measurement setup of Receiver noise figure (top) and P1dB (bottom).

2.4.2 RX Measurements

The RX measurement setup utilizing external signal generator is shown in Fig. 2.32. The objective of this measurement is to evaluate the RX baseband signal by positioning the chip in the far-field of the diagonal horn antenna and receiving signals at different distances to induce shifts in the resultant IF signal. The IF spectrum associated with this measurement is shown in Fig. 2.33 where two peaks at 2 MHz and 10 MHz were obtained by changing the distance between the horn antenna and chip. Both measurements indicate 30-dB SNR. The RX P1dB measurement was performed using a probe landing setup, with the input power adjusted through an attenuator, as illustrated in Fig. 2.32 (bottom). From the measurements, the RX P1dB is estimated to be approximately -33 dBm. The estimated NF measurement results are shown in Fig. 2.35.

The key advantage of the phase-locked stepped chirp architecture lies in its ability to enhance resolution by integrating multiple sub-bands. To demonstrate this feature, a radar field measurement was performed at a distance of 50 cm, the IF signals from both sub-bands

were extracted separately. The time-domain IF signals were then combined, as shown in Fig. 2.36(a). The FFT of the combined signal, shown in Fig. 2.36(b), reveals a significant enhancement of range resolution where closely spaced peaks become clearly distinguishable. For this measurement, the range resolution of each sub-band was 28 mm, and for the combined signals, the range resolution was enhanced to the finer value of 14 mm.

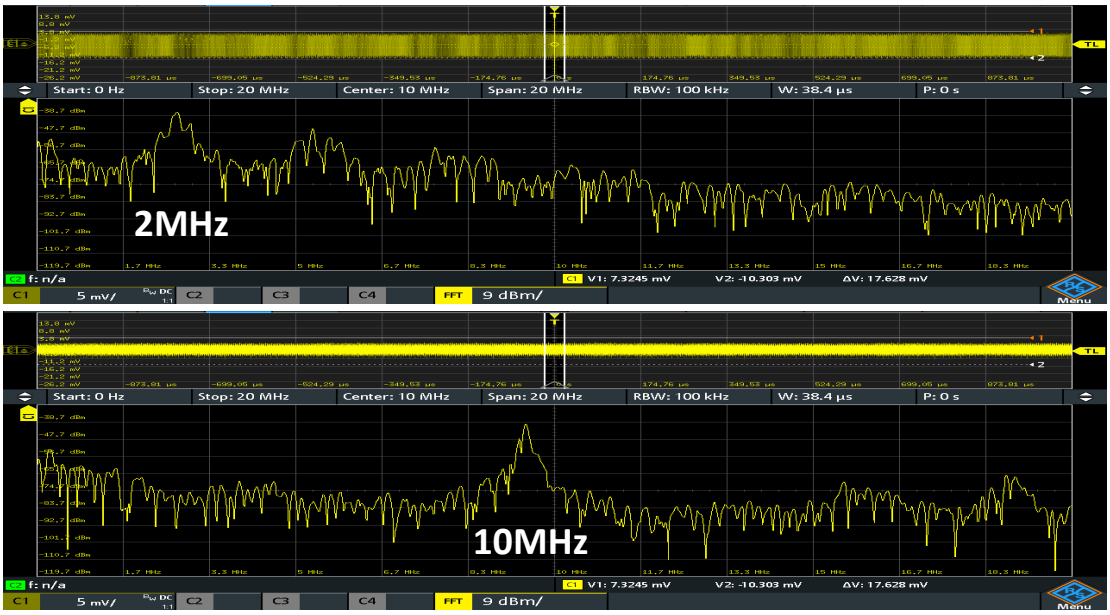

Figure 2.33: RX baseband fft spectrum with peak at 2MHz and 10MHz.

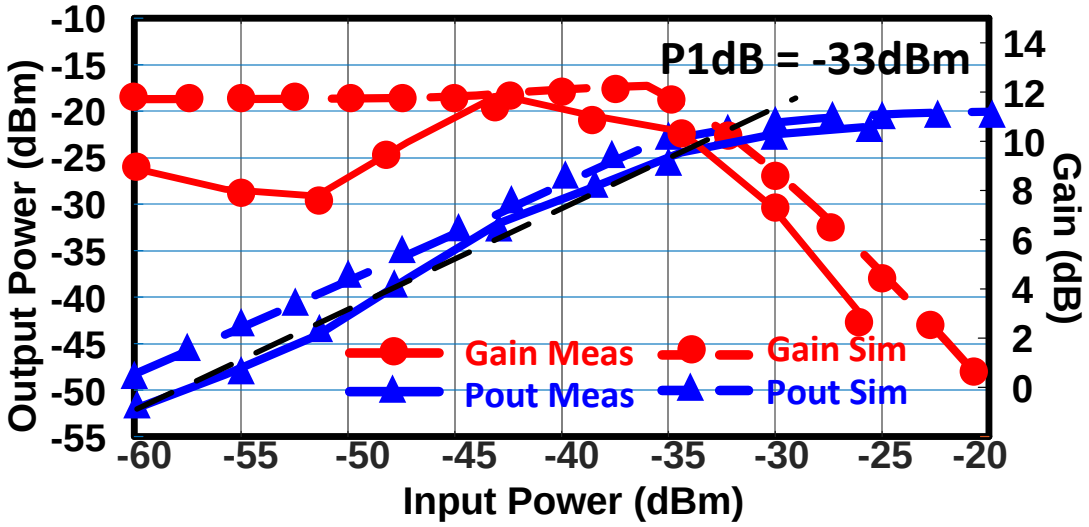

Figure 2.34: Simulation and measurement results of RX Gain and P_{out} vs P_{in}

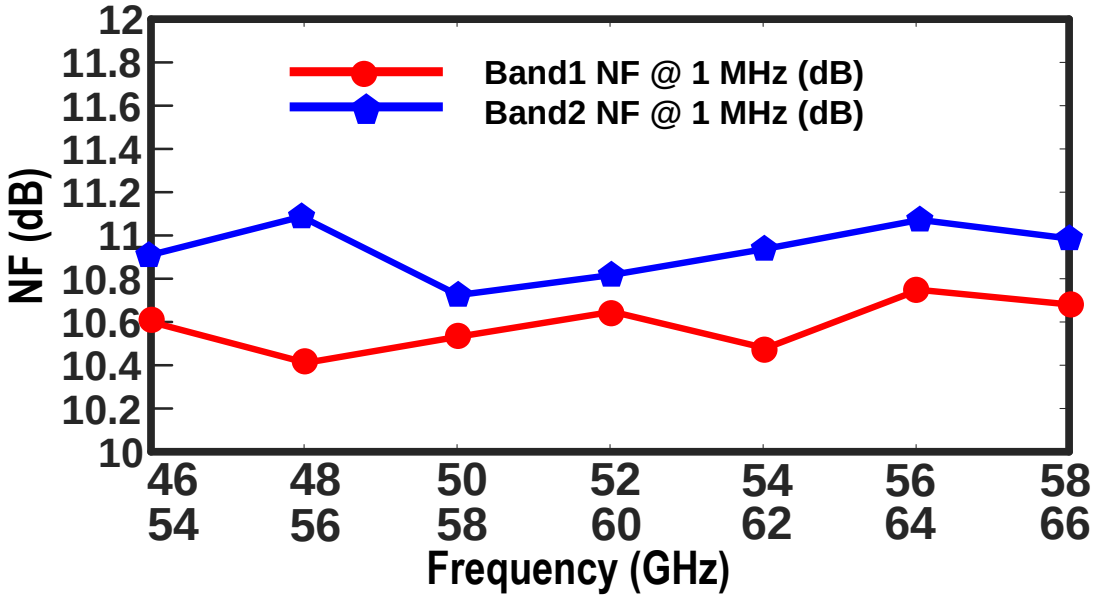

Figure 2.35: Estimated NF measurement from radiation based setup

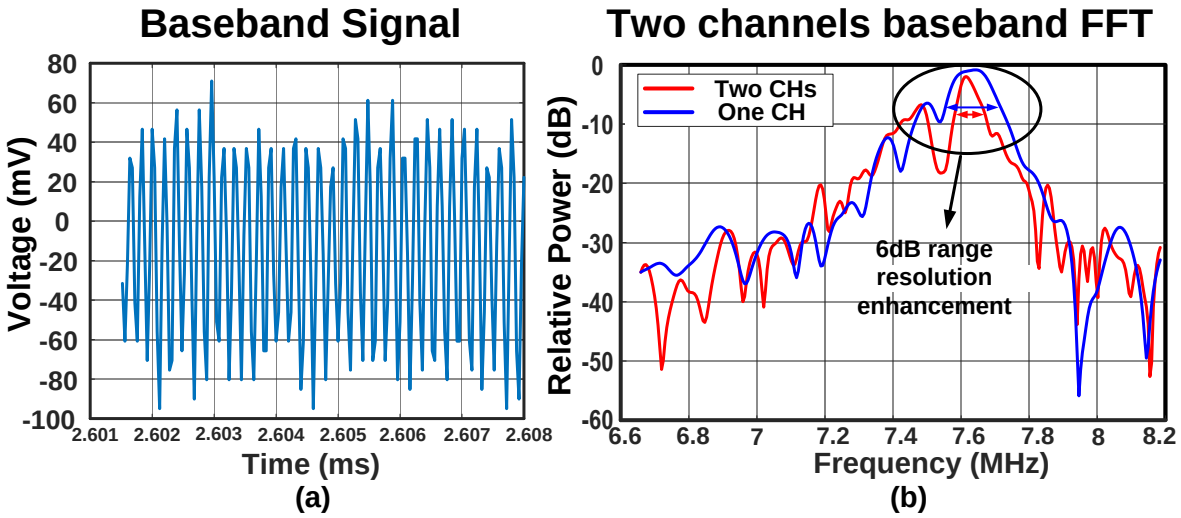

Figure 2.36: Enhancement of range resolution by applying FFT on the combined IF signal of the two sub-bands.

Table 2.1: PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS ARTS

	This work	[22]	[64]	[65]	[66]	[35]	[41]	[17]
Process	22nm FD-SOI	45nm CMOS	350nm SiGe	130nm SiGe	28nm CMOS	40nm CMOS	22nm FD-SOI	28nm CMOS
Phase Locked	Yes	Yes	No	No	No	Yes	Yes	Yes
N_{RX}/N_{TX}	2/2	4/3	4/2	1/1	3/2	2/2	2/2	1/1
Frequency [GHz]	49-63	57-64	57-64	58.3-63.9	57-64	54-69	57-66	57-66
Architecture	Coupled PLL	PLL	VCO	VCO	VCO	Cascaded-PLL	ADPLL	PLL
PN [dBc/Hz]@1MHz	-101.7	-93	-105	-	-99.4	-93.3	-73	-92.9
Bandwidth	14† 10†	4	-	5.6	9	7.2	9	7.2
TX P_{out} [dBm]	6	12.1	4(P_{sat})	6.4	10(P_{sat})	12.8(P_{sat})	1	8.1
Antenna gain [dB]	7‡	-	-	-	-	-	-	-
RX NF [dB]	10	12.5	9.5	-	12	10	30	10.5
RX Gain [dB]	20	-	19	-	77	20-87^	6	46
RX P1dB [dBm]	-33	-10/-14	-8.5	-8.1	-12	-11	-	-43 to -33
P_{dc} [mW]	400	3500	990	520	920	695	68◊	62
Area [mm^2]	4.5	-	20.25	1.03*	7.45	9.9	1.25	4.13

† 14 GHz free running bandwidth and 10GHz phase locked bandwidth
‡ Realized gain including matching structure
* TX and RX share same antenna
^ including basedband amplifier
◊ not including basedband amplifier and digital loop filter

2.4.3 Radar Field Measurements

Various field measurements of the radar are conducted at multiple distances between the radar transceiver and a reflector object. As shown in Fig. 2.37, a corner reflector object is placed at incremental distances ranging from 0.5 m to 5 m.

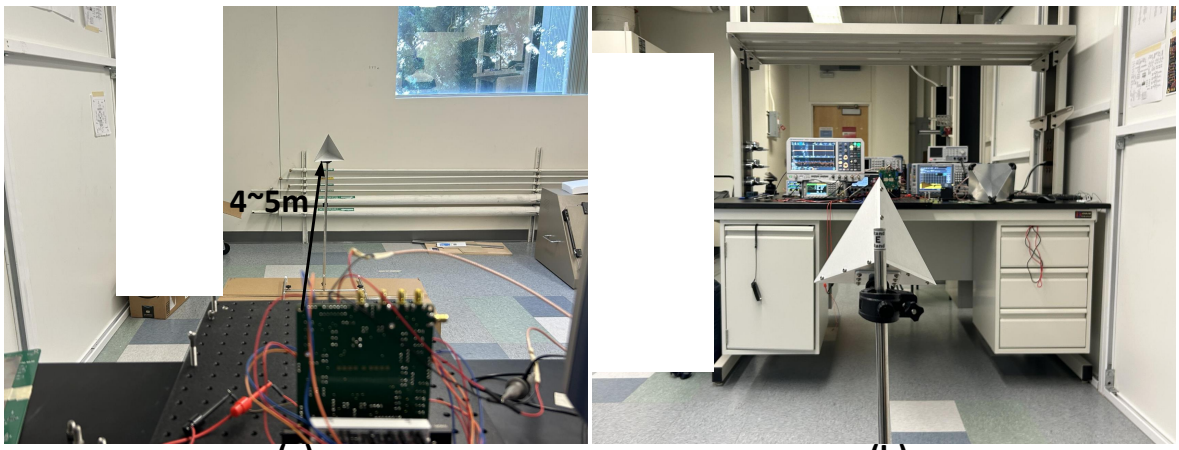

Figure 2.37: Radar field measurement with corner reflector object.

The range measurements of the radar for these different range scenarios are shown in Fig. 2.38. It is observed that for all the measurements, the radar maintains an IF SNR above 16 dB translating to 10 dB of NF_{SSB} for the RX chain. These measurements were conducted

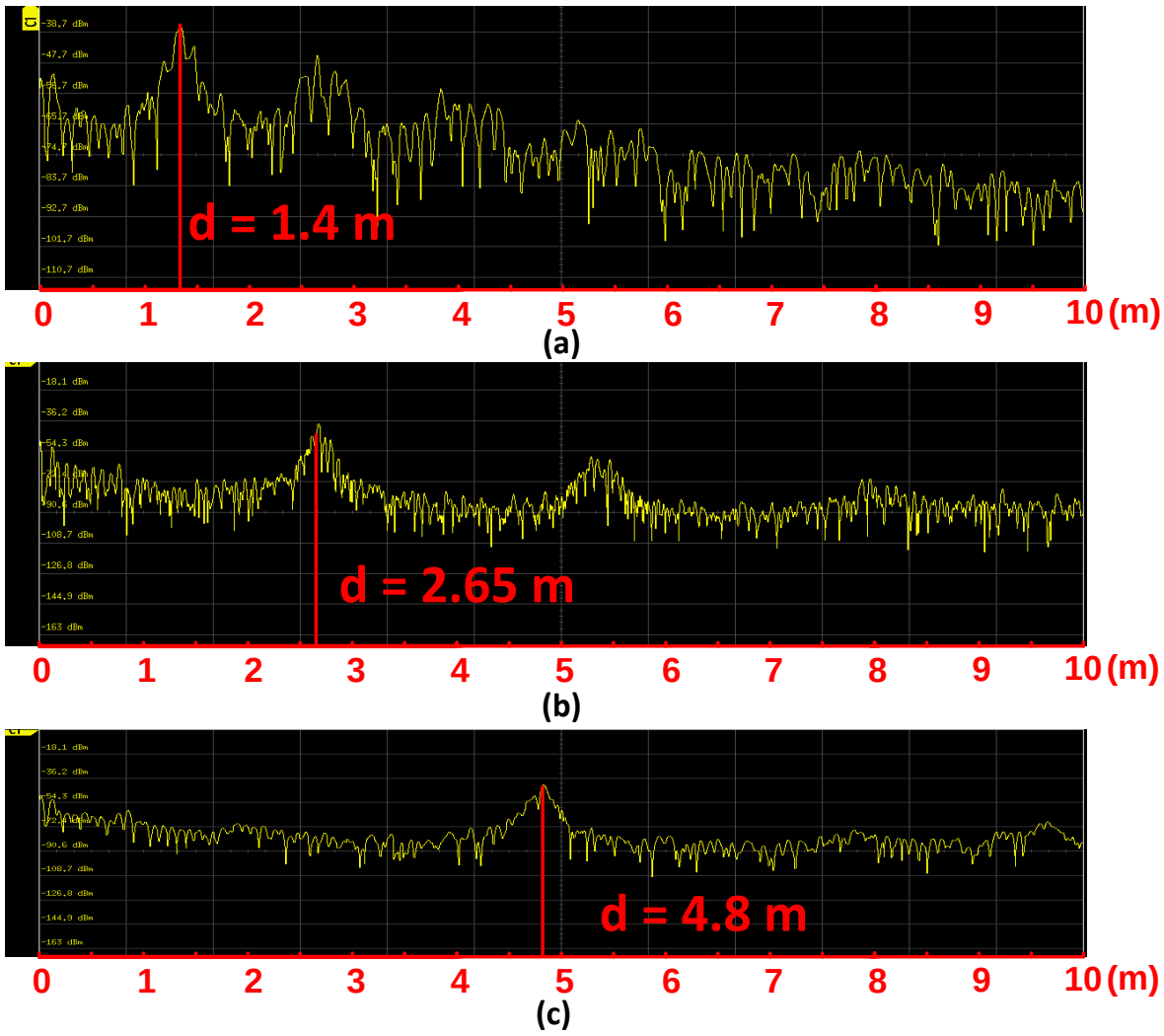

Figure 2.38: Radar field measurement at (a) 1.4 m, (b) 2.65 m, (c) 4.8 m.

at room temperature and with no aid from culminating Teflon lenses or silicon lenses to improve the EIRP of the TX.

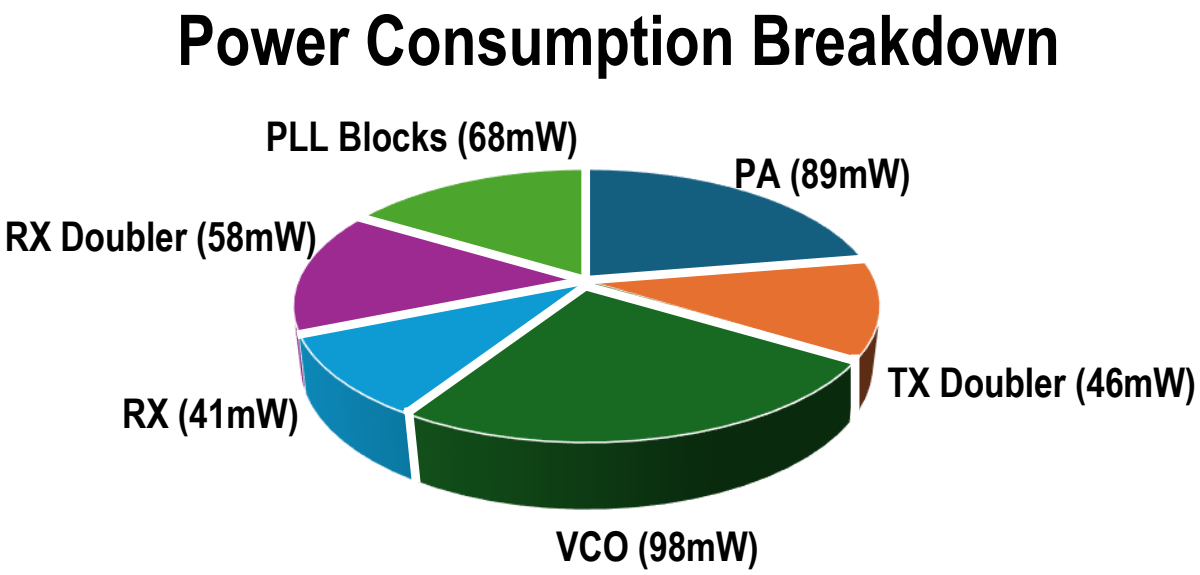

Figure 2.39: Measured power consumption breakdown

Fig. 2.39 summarizes the measured power breakdown of the circuit blocks in the TX and RX. The total power consumption of this two-band phase locked radar transceiver is 360 mW, significantly lower compared to the prior art. Table 2.1 compares the measurement results with prior art. This work outperforms the radars in the same frequency range in terms of phase noise, phase-locked bandwidth, and power consumption. This design demonstrates the first phase-locked stepped chirp radar with more than 10 GHz synthetic bandwidth, and few meters detectable range.

2.5 Conclusion

In this section, a fully integrated CMOS-based phase-locked stepped chirp radar transceiver at 49-63 GHz was presented. The TX side employed a novel PLL scheme which reduced the power consumption and the necessary division ratio compared to conventional type-II PLLs. The RX side incorporated frequency segmented narrow-band RXs which are combined in

the IF domain to enhance the range resolution. The phase-locked bandwidth of this radar was more than 10 GHz and achieved a peak EIRP of 9 dBm. Due to the selected frequency of operation and the total synthetic bandwidth of operation, this radar achieved meter-scale range of coverage and centimeter-scale (1.4 cm) range resolution simultaneously. This radar TRX with a low power consumption of 400 mW offers a potential candidate for future mm-wave radars for automotive, crack detection, and surface monitoring applications.

Chapter 3

A Dual-Band MIMO mm-Wave FMCW Radar Transceiver

3.1 Introduction

Millimeter-wave (mm-wave) frequency modulated continuous wave (FMCW) radars have emerged as a critical technology technology for short-range sensing in advanced driver-assistance systems (ADAS), autonomous robots and drones, vital-sign monitoring, gesture recognition, and indoor localization. Their fine spatial resolution, immunity to lighting or weather conditions, and compact form factor make them complementary—or even superior—to optical and ultrasonic sensors. CMOS processes, meanwhile, provide a low-cost path to large-scale deployment: aggressive transistor scaling pushes f_{T} and f_{max} well into the mm-wave regime, while enabling digital control, on-chip calibration engines, and monolithic integration with analog baseband and digital processing accelerators. The confluence of high f_T devices, mature RF models, and wafer-scale volume thus positions CMOS as an attractive platform for ubiquitous mm-wave radar front-ends.

A radar's ability to distinguish two targets in range is governed by its occupied radio-frequency bandwidth B via $\Delta R \approx c/(2B)$. Increasing B typically entails shifting the carrier toward higher frequencies, where a wide contiguous spectrum is available. However, transmit power from CMOS power amplifiers falls sharply beyond 60 GHz, and the free-space path loss grows as $(4\pi Rf/c)^2$, degrading the signal-to-noise ratio (SNR) at the receiver. Designers therefore face a fundamental range-coverage versus range-resolution trade-off: broad bandwidth promises centimeter-level resolution, but link-budget constraints limit the maximum detectable distance unless costly compound-semiconductor power devices or bulky high-gain antennas are employed.

Angular resolution, on the other hand, scales inversely with the physical aperture and number of virtual elements in a multiple-input multiple-output (MIMO) radar array. Contemporary CMOS research pursues ever-larger virtual arrays—from 3TX/4RX to 36TX/48RX to attain sub-10 degree to sub-degree resolution [67, 68]. Such solutions demand dozens of TXs/RXs channels, high frequency LO distribution, and stringent phase coherence calibration for alignment across the arrays. The resulting increase in die area, package complexity, DC power, and calibration overhead complicates deployment in cost-sensitive or battery-powered platforms, motivating alternatives that enlarge the aperture without proportionally multiplying TXs and RXs channels.

This work introduces a harmonically related dual-band 4×4 MIMO radar that challenges both trade-offs simultaneously. By co-transmitting FMCW waveforms at $23-27$ GHz and its third harmonic $69-81$ GHz through a shared patch antenna set, the system exploits the lower band's superior link budget to preserve long-range coverage, while the composite 12 GHz bandwidth and three-times shorter wavelength of the harmonic band furnish 1.25 cm range resolution and a three-fold finer angular resolution. Crucially, the two bands remain phase-synchronous through fractional-N frequency generation and shared baseband, enabling coherent joint processing without the need for additional transceiver cores or external syn-

chronization trees. Measured results confirm that appropriate inter-element spacing relaxes field-of-view (FoV) limits—predicted by $\theta_{\max} = \sin^{-1}(\lambda/2d)$—so the dual-band aperture attains wide FoV and fine resolution concurrently.

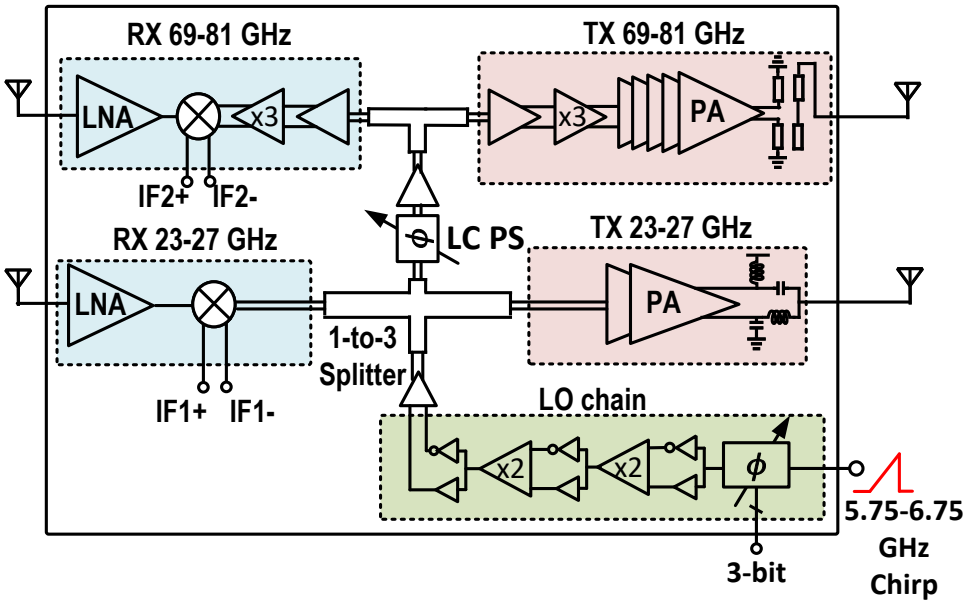

Figure 3.1: Chip block diagram with LO generation chain, 23-27 GHz TRX and 69-81 GHz TRX.

Fig. 3.1 shows the system arrangement and chip block diagram of the proposed FMCW radar array. The system consists of two chips with the same input chirp signal and deterministic phase relationship due to the on-chip LO synchronization, utilizing patch antennas for both transmission and reception.

The remainder of this section is organized as follows. Sub-Section 3.2 details the system architecture and underlying dual-band operating principle. Section 3.3 describes the circuit blocks, antenna array, and printed-circuit-board implementation. Section 3.4 presents measured SISO characterization, dual-band MIMO results with and without phase dithering. Finally, Section 3.5 concludes this section.

3.2 System Architecture Considerations

In single-band operation, mmWave radars face a fundamental trade-off between range resolution and coverage. A higher local oscillator (LO) frequency enables greater absolute bandwidth and thus finer range resolution, while a lower LO frequency provides extended coverage, as dictated by the radar Friis equation. A similar trade-off exists in angle-of-arrival estimation: single-band millimeter-wave MIMO radars can improve angular resolution by increasing aperture size or antenna count, but this comes at the cost of increased hardware complexity when maintaining the same FoV. This section first revisits the trade-off between range resolution and range of coverage, followed by the scaling laws that constrain single-band MIMO arrays. It then introduces a dual-band architecture that relaxes these limitations by judiciously combining low-frequency (LF) and high-frequency (HF) TRX channels.

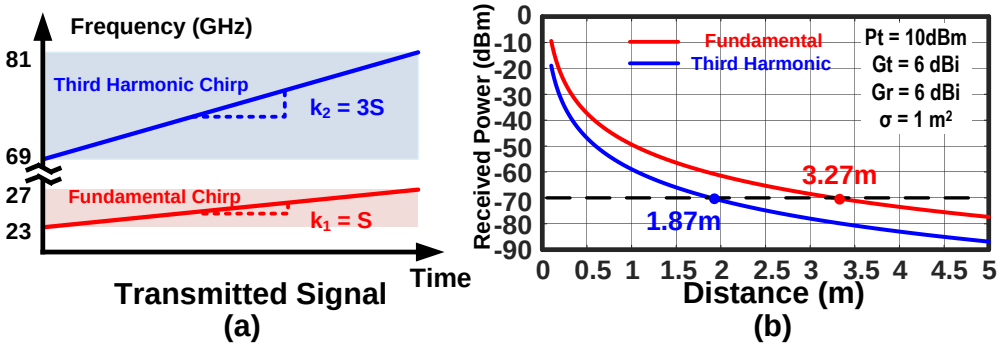

Figure 3.2: (a) Illustration of chirp slope of fundamental and third harmonic signal, (b) range ofcoverage comparison for fundamental and third harmonic.

3.2.1 Range–Resolution Decoupling via Dual–Band Operation

For FMCW or stepped-frequency radars, range resolution obeys

$$\Delta R = \frac{c}{2B}, \tag{3.1}$$

With more available bandwidth, finer range resolution can be achieved. However, this comes at the cost of reduced coverage. According to the radar Friis equation,

$$P_r \propto \frac{\lambda^2}{R^4}, \tag{3.2}$$

The received power decreases as the wavelength decreases. For a fixed SNR—implying the same required received power, assuming a constant noise figure in the receiver chain—the maximum detection range decreases with increasing frequency. Let the LF chirp bandwidth B_{L} and wavelength λ_{L}. Assuming that the difficulty of achieving the same relative bandwidth is comparable across different center frequencies, the achievable HF chirp bandwidth is $B_{\mathrm{H}} = KB_{\mathrm{L}}$ and the wavelength is $\lambda_{\mathrm{H}} = \lambda_{\mathrm{L}}/K$ with integer $K \geq 2$. The achievable range resolution ratio is:

$$\frac{\Delta R_{\mathrm{H}}}{\Delta R_{\mathrm{L}}} = \frac{B_{\mathrm{L}}}{B_{\mathrm{H}}} = \frac{\lambda_{\mathrm{H}}}{\lambda_{\mathrm{L}}} = \frac{1}{K}, \tag{3.3}$$

whereas the range of coverage ratio is given by:

$$\frac{R_{\mathrm{max,H}}}{R_{\mathrm{max,L}}} = \left(\frac{\lambda_{\mathrm{H}}}{\lambda_{\mathrm{L}}}\right)^{1/2} = \frac{1}{\sqrt{K}}, \tag{3.4}$$

which reflects a degradation in detection range due to the higher path loss at shorter wavelengths.This trade-off between the range and resolution can be relaxed by utilizing a dual-band radar.

As illustrated in Fig. 3.2 (a), the third-harmonic chirp is generated by tripling the fundamental chirp, resulting in a bandwidth three times larger than that of the fundamental. This makes the high-frequency (HF) band more suitable for achieving finer range resolution. On the contrary shown in in Fig. 3.2 (b), to achieve a received power of -70 dBm—assuming the same P_t, G_t, G_r, and radar cross-section σ—the coverage range of the LF band (3.27 m) is approximately $\sqrt{3}$ times that of its HF counterpart (1.87m). In summary, the LF band offers longer detection range, while the HF band enables finer range resolution. By

combining the strengths of both LF and HF, the trade-off between resolution and coverage can be effectively overcome.

3.2.2 Limits of Single-Band Scaling

For a uniformly linear virtual array of $N_v = N_{\mathrm{TX}} N_{\mathrm{RX}}$ elements with half-wavelength spacing $d = \lambda/2$, the classical small-angle resolution is

$$\Delta\theta_{\mathrm{SB}} \approx \frac{\lambda}{N_v d} = \frac{2}{N_v}\ (\mathrm{rad}), \tag{3.5}$$

so achieving a resolution improved by a factor of k forces $N_v \to kN_v$. Scaling the number of TX and RX elements comes with natural challenges on signal routings, synchronization, area, and power consumption. Meanwhile, the maximum unambiguous FoV obeys

$$\theta_{\max} = \sin^{-1}\!\left(\tfrac{\lambda}{2d}\right) = \pm 90^{\circ}, \tag{3.6}$$

but shrinks when $d > \lambda/2$.

3.2.3 Dual-Band MIMO: Synthetic Array-Factor Engineering

For a uniform linear array of N elements spaced by d in a single-band radar, the baseband received signal can be expressed as:

$$A_i(\theta) = \sum_{m=0}^{N-1} w_m\, e^{-jk_i dm \sin\theta}, \qquad k_i = \frac{2\pi}{\lambda_i}, \tag{3.7}$$

where N is the total number of array elements, d the uniform spacing between adjacent elements, w_m the complex weight applied to element m, $k_i = 2\pi/\lambda_i$ the wavenumber, and θ the scan (or arrival) angle measured from broadside; the steering vector is $\mathbf{a}_i(\theta) =$

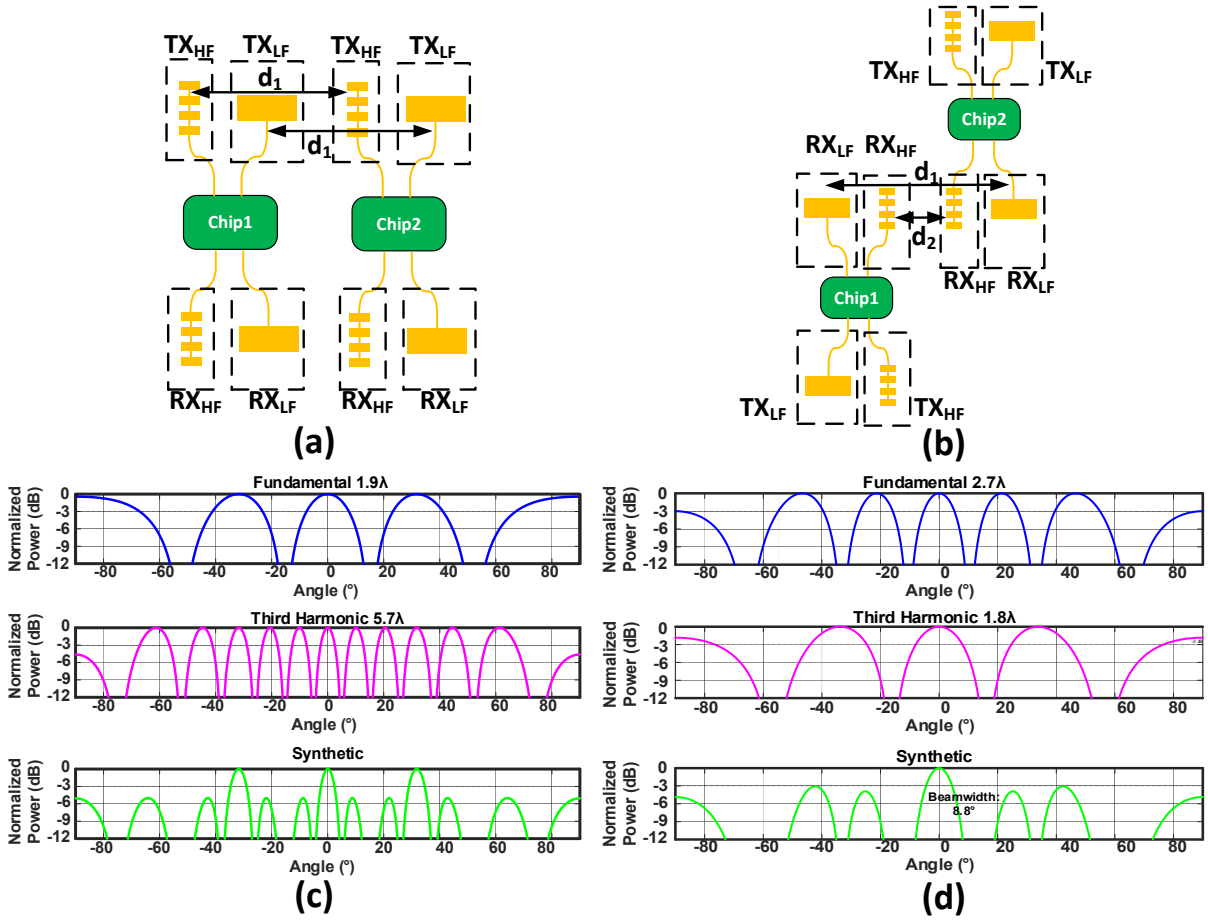

Figure 3.3: (a) Identical spacing and (b) non-identical spacing between the antenna of both bands; MIMO array synthesis by (c) identical physical spacing and (d) non-identical spacing between the antennas of the two bands.

$\left[e^{-jk_i d 0 \sin\theta}, \ldots, e^{-jk_i d(N-1)\sin\theta}\right]^{\mathrm{T}}$.

The broadside half-power beamwidth (HPBW) of a uniformly weighted array is approximately $\Delta\theta_{\mathrm{HPBW}} \simeq 0.886\,\dfrac{\lambda_i}{Nd}$. Hence the angular resolution improves (smaller $\Delta\theta_{\mathrm{HPBW}}$) as the electrical aperture Nd increases, either by adding elements or widening their spacing. However, the maximum grating-lobe-free scan angle is bounded by the constraint $d \leq \frac{\lambda_i}{1+|\sin\theta_{\max}|}$, which simplifies to the familiar $d \leq \lambda_i/2$ when a full $\pm 90°$ FoV is required. Increasing d toward this limit tightens the main lobe but simultaneously reduces the scan range before grating lobes appear, shrinking the usable FoV. Conversely, choosing a smaller d (e.g. $d \ll \lambda_i/2$) enlarges the FoV at the expense of a broader main lobe, i.e. poorer angular resolution. Therefore, single-band arrays inevitably exhibit a trade-off: narrow beams

(high resolution) come with a limited FoV, whereas wide-angle coverage must accept coarser angular resolution under the condition of fixed number of TRX channels. For a uniformly weighted N-element linear array the normalized power pattern at wavelength λ_i and spacing d_i is

$$P_i(\theta) \;=\; \left| \frac{\sin\big(N\pi\beta_i \sin\theta\big)}{N\,\sin\big(\pi\beta_i \sin\theta\big)} \right|^2, \qquad \beta_i = \frac{d_i}{\lambda_i}. \tag{3.8}$$

The principal maxima occur at $\sin\theta_{i,m} = m/\beta_i$ $(m \in \mathbb{Z})$, whereas the first nulls lie midway between successive maxima. For a dual-band radar at center frequencies f_1 and f_2, the power patterns at each band will exhibit a unique profile for maxima and nulls and the synthetic (dual-band) pattern is formed through the Hadamard product, i.e.,

$$P_{\text{syn}}(\theta) = P_1(\theta) \odot P_2(\theta). \tag{3.9}$$

where P_{syn} is the resultant synthetic power profile and P_i is the power profile at the i-th frequency band. To construct a MIMO array with dual-band radars, two major possibilities are conceived: I) antenna placement at the two frequency bands with identical physical distances. In this case, if the center frequencies of the two bands are at f_1 and f_2, the electrical length of antenna spacing for the bands, d_1 and d_2 are proportional, i.e.,

$$\frac{l_1}{l_2} = \frac{f_1}{f_2} \tag{3.10}$$

An example of this case is shown in Fig. 3.3(a). II) In the second scenario, the antennas are placed with arbitrary electrical distances that do not follow the frequency relationships of the two bands, i.e.,

$$\frac{l_1}{l_2} \neq \frac{f_1}{f_2}. \tag{3.11}$$

An example of this formation is shown in Fig. 3.3(b). In what follows, we study the synthetic angular resolution and FoV of dual-band radars under both scenarios.

3.2.4 Identical Spacing

Under this condition,

$$P_{syn}(\theta) \;=\; \left| \frac{\sin\big(N\pi\beta_1 \sin\theta\big)}{N\,\sin\big(\pi\beta_1 \sin\theta\big)} \frac{\sin\big(M\pi\beta_1 \sin\theta\big)}{M\,\sin\big(\pi\beta_1 \sin\theta\big)} \right|^2 \quad M = \frac{f_2}{f_1} N. \tag{3.12}$$

Under the harmonic–spacing constraint of (3.12), the synthetic response is the squared product of two Dirichlet kernels that share the angular argument $x = \pi\beta_1 \sin\theta$, where $\beta_1 = d_1/\lambda_1$ is the element–spacing factor referenced to the lower frequency f_1. Introducing the K^{th}-order Dirichlet kernel

$$D_K(x) = \frac{\sin(Kx)}{K \sin x}, \tag{3.13}$$

we may rewrite the pattern as $P_{\text{syn}}(\theta) = |D_N(x)\, D_M(x)|^2$ with $M = \frac{f_2}{f_1} N$. Each kernel attains its global maximum only at $x = 0$; consequently the product preserves a single principal maximum at boresight ($\theta = 0°$) while suppressing all subsidiary lobes, because any secondary peak of one factor coincides with a deep minimum of the other. the third harmonic lobes are aligned so they can't be suppressed

A numerator zero of either kernel produces a synthetic null provided its denominator is non-zero:

$$\sin\theta = \frac{m}{K\beta_1}, \qquad K \in \{N, M\},\ m \in \mathbb{Z} \setminus \{0\}. \tag{3.14}$$

Since $M > N$, the closest product-null to boresight is located at $\sin\theta_{\text{null}} = 1/(M\beta_1)$. The first-null spacing therefore confines the main lobe to

$$\Delta\theta_{3\text{dB}} \simeq \frac{0.886}{M\beta_1}\ \text{rad}\ \approx \frac{50.8°}{M\beta_1}, \tag{3.15}$$

indicating that the angular resolution is narrowed by the same integer factor M that relates the carrier frequencies.

Grating lobes appear when $|\sin\theta| \geq 1/\beta_1$ for either band, but the composite pattern remains free of such replicas as long as $|\sin\theta| < 1/(M\beta_1)$. The maximal unambiguous scan range is therefore

$$\mathrm{FoV} = 2\arcsin\Big(\tfrac{1}{M\beta_1}\Big), \tag{3.16}$$

therefore the alias-free field-of-view cannot extend beyond the nulls immediately adjacent to the main beam. In other words, harmonic spacing guarantees grating-lobe cancellation, but it does not enlarge the FoV beyond the angular separation set by the closest high-band nulls; it merely preserves that sector while sharpening the resolution within it. With the simulated parameters $d_1 = 1.9\lambda_1$ ($\beta_1 = 1.9$) and $M = 3$, the theory yields $\theta_{\text{null}} = \arcsin(1/5.7) \approx 10.1^\circ$ and $\Delta\theta_{3\text{dB}} \approx 9.8^\circ$.

3.2.5 Non-identical Spacing

Let the physical inter–element spacings at the two carrier frequencies f_1 and $f_2 = k\,f_1$ ($k \in \mathbb{N}_{>1}$) be d_1 and d_2, respectively, and denote the corresponding normalised spacings by

$$\beta_1 = \frac{d_1}{\lambda_1}, \qquad \beta_2 = \frac{d_2}{\lambda_2} = k\,\frac{d_2}{\lambda_1}.$$

The synthetic pattern is still $P_{\text{syn}}(\theta) = |D_N(\pi\beta_1\sin\theta)\,D_M(\pi\beta_2\sin\theta)|^2$ with $M = kN$, but now β_1 and β_2 are *a priori* independent. We can write the ratio of the two spacings in lowest terms, i.e.,

$$\frac{\beta_1}{\beta_2} = \frac{A}{B},\ A, B \in \mathbb{N},\ \gcd(A, B) = 1. \tag{3.17}$$

Grating–lobe maxima of the fundamental array occur at $\sin\theta = p/\beta_1$ ($p \in \mathbb{Z} \setminus \{0\}$); those angles will be *cancelled* in the product pattern if they coincide with numerator zeros of the high–band kernel, i.e.

$$\frac{p}{\beta_1} = \frac{m}{M\beta_2} \implies m = \frac{p\,M\,\beta_2}{\beta_1} = p\,k\,\frac{B}{A}.$$

This is possible for *all* integers p exactly when $A \mid M$ (equivalently, $A \mid kN$). By the same argument the grating lobes of the high–band array, which lie at $\sin\theta = q/\beta_2$, are cancelled by numerator zeros of the fundamental kernel provided $B \mid N$. Hence the sufficient condition for complete lobe cancellation is

$$\boxed{\beta_1/\beta_2 = A/B,\ \gcd(A,B) = 1,\ A \mid M,\ B \mid N}. \tag{15}$$

When (15) is satisfied *every* potential grating–lobe direction of either sub-array is suppressed by the complementary band, so the composite response contains *no* sidelobe maxima in the entire visible hemisphere $|\theta| \le 90°$. The only remaining extrema are the main lobe at boresight and the predictable sequence of deep nulls that emanate from the integer lattice of numerator zeros; these nulls do not create DOA ambiguities and therefore do not restrict the usable scan sector. Consequently the alias-free field of view equals the full $\pm 90°$.

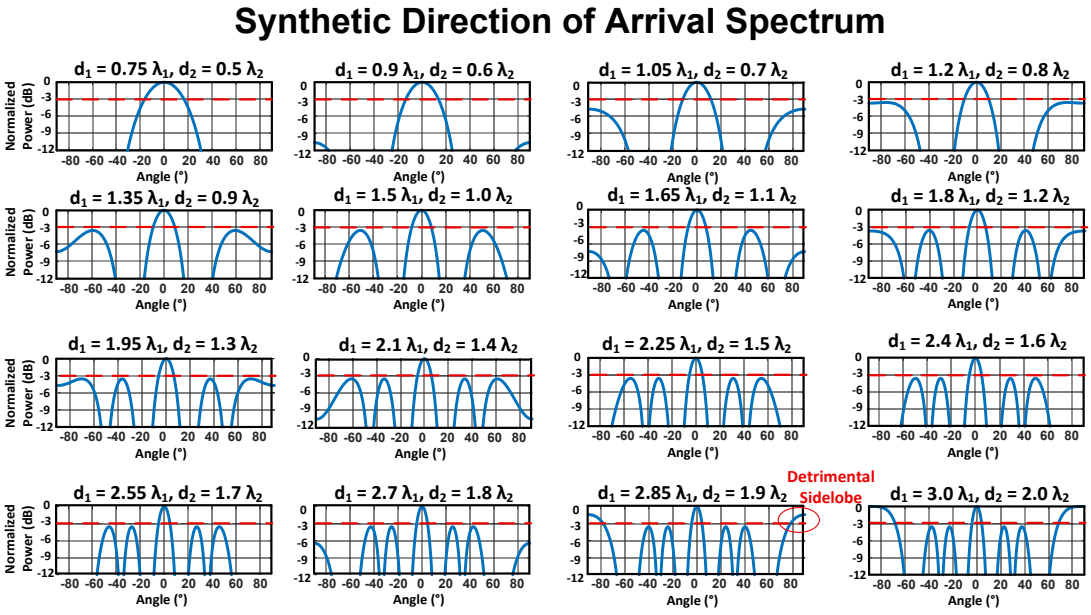

Figure 3.4: Synthetic direction-of-arrival (DOA) spectrum with d_2 ranging from $0.5\,\lambda_2$ to $2.0\,\lambda_2$ and d_1 from $0.75\,\lambda_1$ to $3.0\,\lambda_1$. Detrimental sidelobes begin to emerge as d_2 exceeds $1.9\,\lambda_2$.

The simulation in Fig. 3.4 employs $d_1 = 2.7\lambda_1$ ($\beta_1 = 2.7$) and $d_2 = 1.8\lambda_2$ ($\beta_2 = 1.8$), giving

the reduced ratio $\beta_1/\beta_2 = 3/2$. With two elements per band ($N = 2$) the harmonic order is $M = kN = 6$. Because $A = 3 \mid M$ and $B = 2 \mid N$, condition (15) holds and the green "Synthetic" trace indeed shows a single main lobe with no spurious maxima over the entire $\pm 90°$ range, while maintaining a $\sim 8°$ 3-dB beamwidth dictated by the larger of β_1 and β_2. This example illustrates that, by an appropriate choice of the relative spacings rather than identical spacings, dual-band arrays can simultaneously achieve wide, alias-free scan and high angular resolution.

Table 3.1: Dual-band synthesis outperforms single-band radars even with only two or four elements per array.

Arch.	**# of Elem. (TX × RX)**[†]	**$\Delta\theta_{3dB}$ (deg)**	**Clear FoV (deg)**
SB–2	2×2	50.8	± 60
SB–4	4×4	25.4	± 60
DB–2+2	2×2	12.7	± 90
DB–4+4	4×4	4.2	± 90

[†]SB: 75 GHz, $\lambda/2$ spacing. DB: 25/75 GHz, (d_1, d_2, M) chosen to cancel the first fundamental-band lobe $\left[(2\lambda_1, \frac{2}{3}\lambda_1, 3)$ for $N=2$; $(2\lambda_1, \lambda_1, 3)$ for $N=4\right]$.

Discussion of Table 3.1. The dual-band architectures (DB–2+2, DB–4+4) exploit Hadamard-product synthesis to eliminate grating lobes and to leverage the shorter 75 GHz wavelength for angular resolution, while using the widely spaced 25 GHz array to preserve a broad $\pm 90°$ unambiguous FoV (wrong claim). With only two physical elements per band, the DB–2+2 array attains a 12.7° beamwidth—four times narrower than the single-band two-element case (SB–2) and comparable to a single-band four-element array, yet with a FoV enlarged by 50%. Scaling to four elements per band (DB–4+4) tightens the beam to 4.2°, outperforming the single-band counterpart while maintaining the same total RF-chain count. These results substantiate that dual-band operation can simultaneously relax aperture size and RF hardware requirements without compromising angular resolution or coverage.

3.2.6 Scaling of Micro-cells and Macro-cells

Each MMIC that carries one low-band (f_1) and one high-band (f_2) Tx/Rx pair is referred to as a *micro-cell*; the two-chip assembly sketched in Fig. 3.3(b) is a *macro-cell*. Let d_1 denote the centre-to-centre pitch between successive micro-cells and d_2 the fixed spacing between the two f_2 elements inside a single macro-cell. With the wavelength definitions $\lambda_1 = c/f_1$ and $\lambda_2 = c/f_2$, we introduce the normalised spacings $\beta_1 = d_1/\lambda_1$ and $\beta_2 = d_2/\lambda_2$. Following Sec. II-E, a macro-cell contains N low-band elements and $M = kN$ high-band elements, where $k = f_2/f_1$; an array composed of S such macro-cells is therefore Sd_1 meters long. The shorthand $D_K(x) = \sin(Kx)/(K\sin x)$ denotes the K-th-order Dirichlet kernel used throughout this section.

For the fully uniform layout of Fig. 3.3(a) the array factor is the single-micro-cell response multiplied by D_M, so tiling M micro-cells merely narrows the main lobe by the same factor while the $\pm 90^\circ$ field of view is preserved. In the sparse layout of Fig. 3.3(b) only whole macro-cells can be appended without disrupting the high-band geometry. Replicating S macro-cells multiples the single-cell response by D_S, yielding the per-band steering vectors

$$A_{1,S}(\theta) = D_S\big(\pi\beta_1 \sin\theta\big)\, D_N\big(\pi\beta_1 \sin\theta\big), \tag{3.18}$$

$$A_{2,S}(\theta) = D_S\big(\pi\beta_1 \sin\theta\big)\, D_M\big(\pi\beta_2 \sin\theta\big). \tag{3.19}$$

The dual-band synthetic power pattern is therefore

$$P_{\mathrm{syn},S}(\theta) = \big|D_S(\pi\beta_1 \sin\theta)\big|^2 \,\big|D_N(\pi\beta_1 \sin\theta)\, D_M(\pi\beta_2 \sin\theta)\big|^2. \tag{3.20}$$

Because D_S tightens the main lobe while the product $D_N D_M$ retains the grating-lobe can-

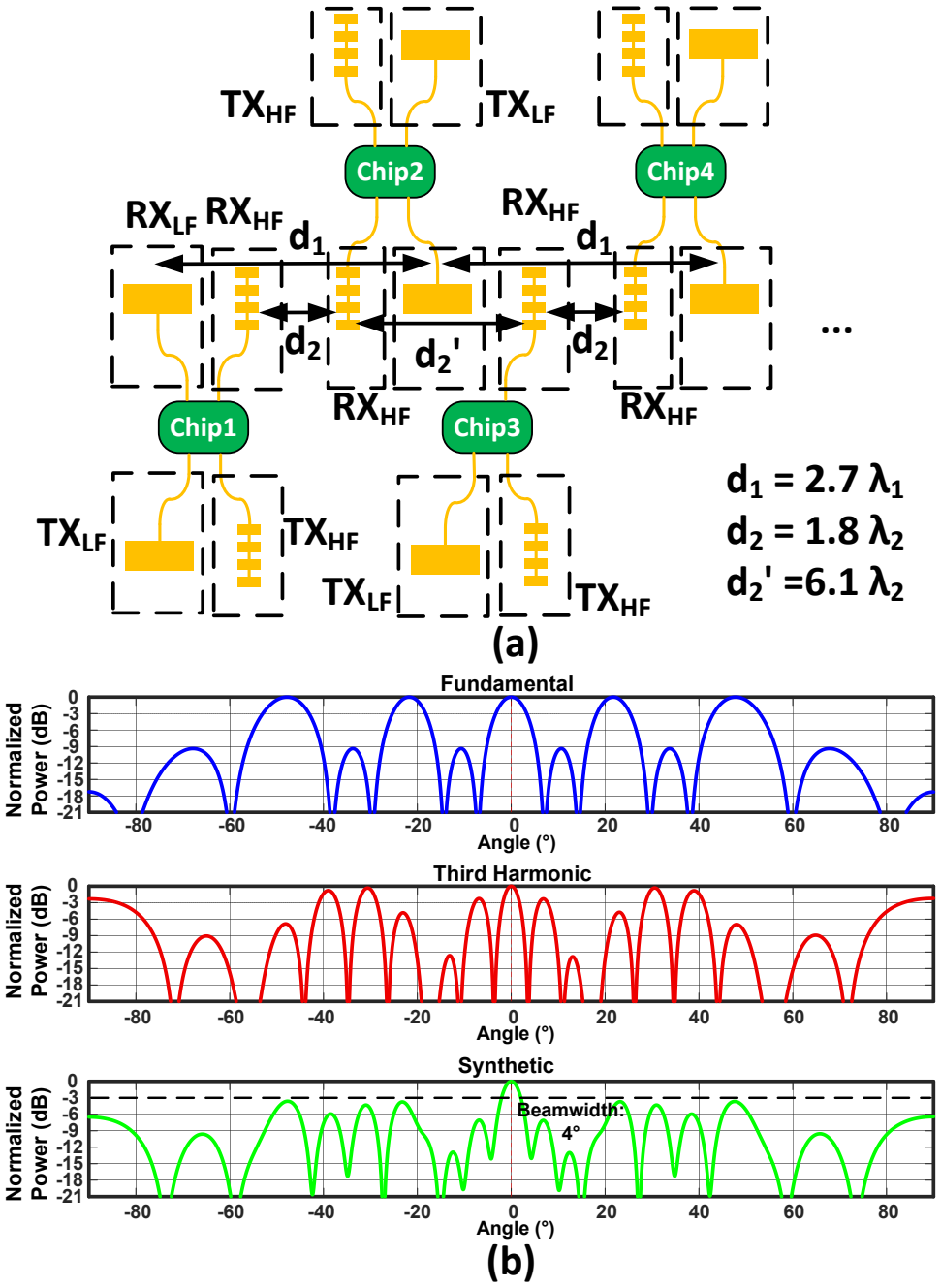

Figure 3.5: (a) Scaling to 4 chips with 7TXs and 7RXs, (b) angular spectrum for each band and the synthetic angular spectrum

cellation established for a single macro-cell, the 3-dB beamwidth scales approximately as

$$\Delta\theta_{3\mathrm{dB}} \simeq \frac{0.886}{S\,\max\{N\beta_1,\, M\beta_2\}},$$

and the alias-free angular span remains the full $\pm 90°$. The impact of scaling for uniform and non-uniform scenarios under various counts of elements are shown in Fig. 3.5(a,b) respectively.

3.2.7 Phase Dithering for Grating Lobe suppression

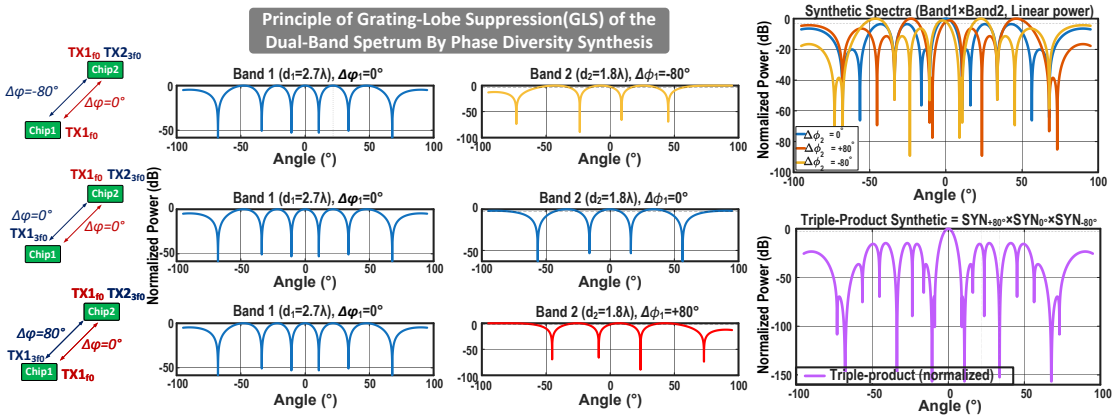

Figure 3.6: Phase dithering illustration to suppress grating lobe by 20 dB

Building on the optimum non-uniform array as shown in Fig. 3.6, a second layer of diversity—phase dithering—is introduced to further enhance grating-lobe suppression and beam sharpness. The system repeats the dual-band measurement across three distinct phase states (e.g., $\Delta\phi = -\phi_0, 0, +\phi_0$), applied exclusively to the higher-frequency transmit or receive paths, while the lower-frequency band remains phase-constant. As shown in Fig. 2 (bottom), each phase state slightly shifts the angular response of the high-frequency band, producing complementary spectra. These modified high-frequency spectra, denoted $P_2^{(-)}(\theta)$, $P_2^{(0)}(\theta)$, and $P_2^{(+)}(\theta)$, are each multiplied with the fixed low-frequency spectrum $P_1(\theta)$ to form three dual-band responses: $P_{\mathrm{syn}}^{(i)}(\theta) = P_1(\theta) \odot P_2^{(i)}(\theta), \quad i \in \{-\phi_0, 0, +\phi_0\}$. Finally, the three phase-dithered dual-band responses are combined via Hadamard product to form the angu-

lar spectrum: $P_{\text{final}}(\theta) = P_{\text{syn}}^{(-)}(\theta) \odot P_{\text{syn}}^{(0)}(\theta) \odot P_{\text{syn}}^{(+)}(\theta)$. This stepwise synthesis compresses the main beam and strongly attenuates grating lobes by enforcing destructive interference across the phase-shifted profiles. Unlike conventional single-band MIMO systems that rely on large spatial apertures and extensive time-division multiplexing, this approach exploits frequency and phase as additional degrees of diversity to achieve $\sim 5^\circ$ resolution and grating lobe suppression (GLS) $\simeq$ 20 dB, using a drastically reduced number of RF channels and calibration complexity.

3.3 Circuit Implementation

3.3.1 Phase Synchronization for Angular Resolution

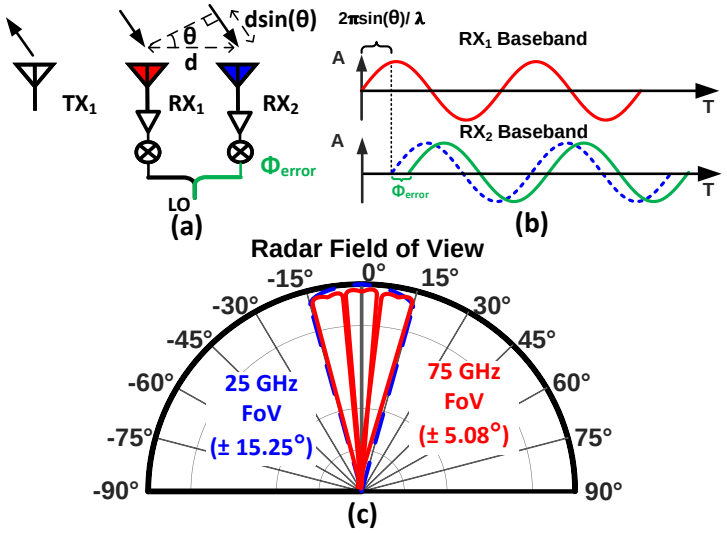

Figure 3.7: (a) Angle of arrival measurement with LO phase mismatch ϕ, (b) illustration of baseband phase shift due to the LO phase mismatch, (c) FoV of fundamental and third harmonic.

The phase method used to measure the angle of arrival in a 1TX-2RX setup, for example, is illustrated in Fig. 3.7. The angle of arrival can cause a difference in travel distance of the reflected signal. The difference can be calculated by trigonometry as $d\sin(\theta)$, and the

corresponding phase difference at baseband due to this travel distance difference is [69]:

$$\phi_{angle} = \frac{2\pi d \sin(\theta)}{\lambda} \tag{3.21}$$

This equation is based on the condition that the LO signals provided to both RXs are precisely in phase. In a multi-chip MIMO system, the phase alignment is hard to achieve. Suppose there is a LO phase mismatch between RX1 and RX2 as illustrated in Fig. 3.7. The total phase due to both the angle of arrival and the LO phase mismatch is $\phi_{total} = \phi_{angle} + \phi_{mismatch}$. The calculated θ contains both the angle and the phase mismatches. To alleviate the impact of phase alignment on the measured angle of arrival, phase shifters are needed for both fundamental and third harmonics. In this radar TRX, a 5.75-6.75 GHz delay-based phase shifter is employed to calibrate the LO phase mismatch between different channels, and an additional LC phase shifter before the third harmonic TRX to calibrate the phase misalignment between the TRXs of 2 frequency bands. The detailed implementation will be expanded in Section III.

Another critical consideration in radar system design is the tradeoff between FoV and angular resolution [69]. The maximum unambiguous FoV ($\theta_{\max}$) that two antennas can measure is given by:

$$\theta_{\max} = \pm \sin^{-1}\left(\frac{\lambda}{2d}\right) \tag{3.22}$$

while the angular resolution (θ_{res}) is expressed as:

$$\theta_{\text{res}} = \frac{\lambda}{d\cos(\theta)} \tag{3.23}$$

Increasing the antenna separation d improves the angular resolution at the expense of a reduced FoV. For the configuration shown in Fig. 3.1(a), with fundamental and third har-

monic antennas positioned as depicted, the maximum FoV for the fundamental and third harmonic bands is calculated to be ±15.25° and ±5.08°, respectively, as shown in Fig. 3.7 (c). The fundamental band can compensate the unambiguous narrow FoV of the third harmonic band. The angular resolution is enhanced within ±15.25° by 3 times with the third harmonic band.

3.3.2 Phase Shifters

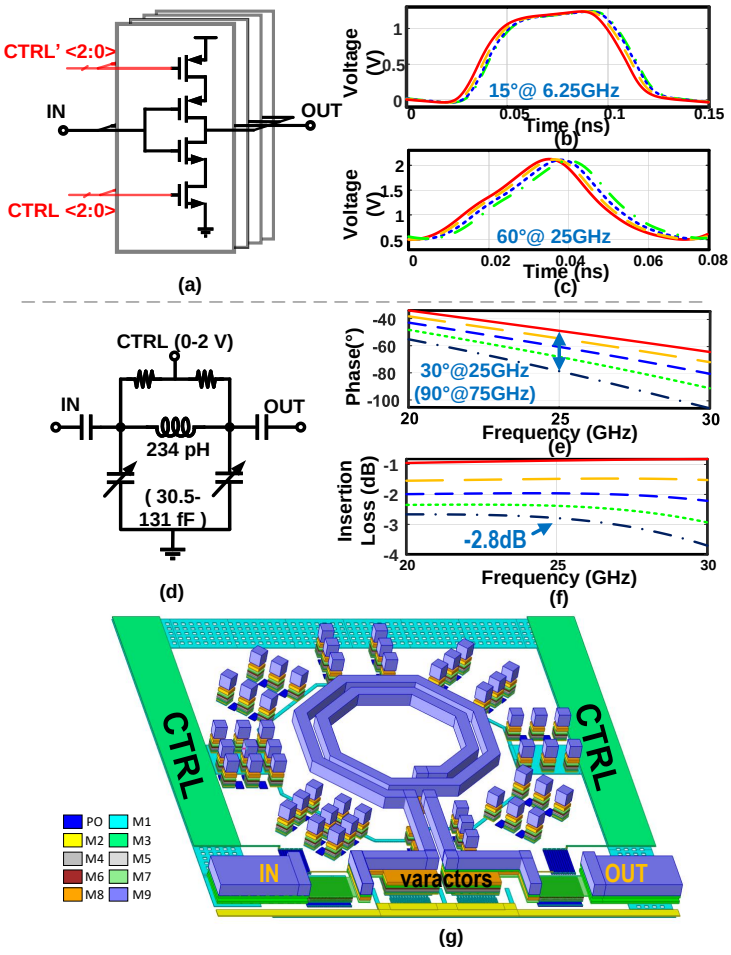

Figure 3.8: (a) The delay-based phase shifter with 3-bit control at 5.75 - 6.75 GHz, (b) Simulated transient at the output of the phase shifter at 6.25 GHz, (c) Corresponding transient at 25 GHz. (d) Schematic of an LC-based phase shifter at 25 GHz, (e) Simulated phase response at 25 GHz (f) Simulated insersion loss at 25GHz. (g) EM structure.

At below 10 GHz, inductor-based or transmission-line-based phase shifters can occupy large

chip area. While delay-based phase shifters are very area-efficient since no EM structure is required, and the power overhead they have to pay at this frequency for the intrinsic broadband behavior is only marginal in modern CMOS technology. The implemented delay-based phase shifter (PS) schematic is shown in Fig. 3.8 (a). Since the subsequent frequency multipliers multiply phase differences by 4x, the delay-based PS is situated at the beginning of the LO chain. The input chirp is pre-buffered to a square wave and then delayed by code-controlled inverter slices, generating phase differences. The signal is then recovered into a square wave by subsequent fan-out inverters. The resulting phase difference at the output of the LO chain at 25 GHz is up to 60 degrees.

An additional LC-PS is employed before instead of after the frequency tripler to achieve the desired phase relationships between the two bands. Thus, the phase shift range and insertion loss requirements are both relieved. The schematic, simulation results and EM view are shown in Fig. 3.8. The lower plates of the varactors are biased at 1 V to maximize their tuning range. The phase shift at 25 GHz is up to 30 degrees, equivalent to 90 degrees after the frequency tripler, with a maximum insertion loss of only 2.8 dB.

3.3.3 Frequency Tripler

A frequency tripler is required on both the TX and RX sides to radiate the third harmonic. As shown in Fig. 3.9(a), the tripler incorporates a second-harmonic-trap at the common-mode source node to generate a large second harmonic swing, enabling transistors' self-mixing with the input fundamental tone. To selectively enhance the third harmonic while suppressing the fundamental tone, a filter is implemented at the drain node, effectively attenuating the fundamental without compromising the third harmonic gain. The simulated output power with a 0 dBm input is illustrated in Fig. 3.9(b), demonstrating that the tripler achieves suppression of over 18 dB for all other harmonics.

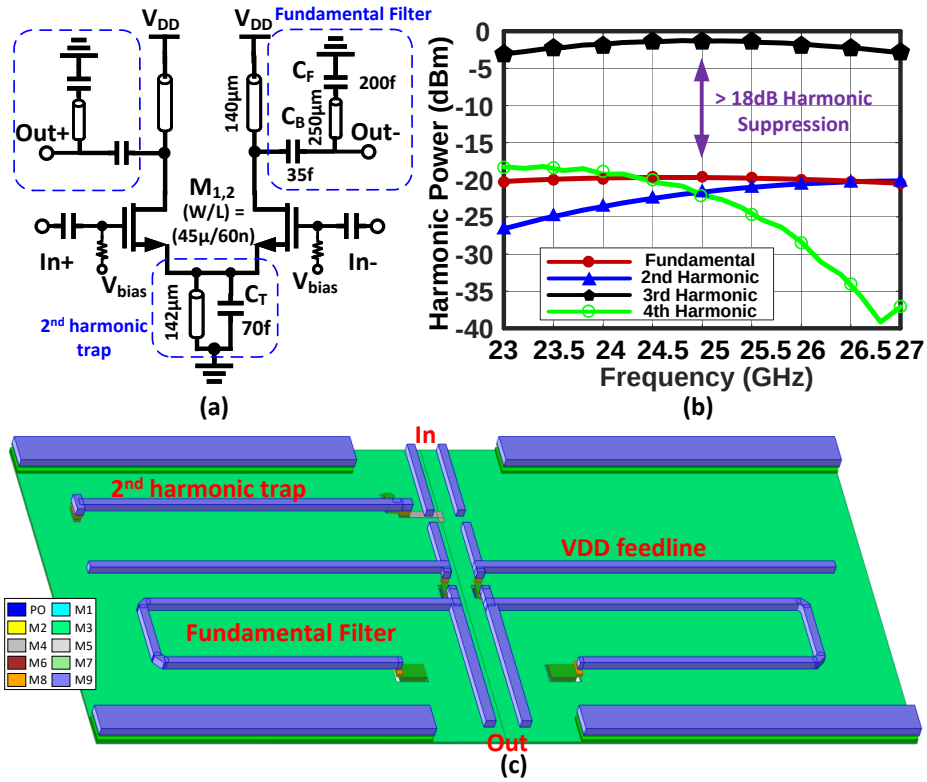

Figure 3.9: (a) Frequency tripler schematic, (b) Simulated output power at different harmonics for 0 dBm input fundamental power. (c) EM structure.

On the input side, the lower-band LO signal after the 1-to-2 spliter is first buffered and directly driving the gate of the tripler for maximum gate swing to trigger its nonlinearity. The output matching of the tripler for RX is co-optimized with the LO port impedance of the down-conversion mixer for maximum gate swing. While on the TX side it's matched to 50 Ω. The EM structure of the tripler is shown in Fig. 3.9 (c), the transmission lines have their signal traces on M9 and reference ground plane on M3.

3.3.4 Power Amplifier

The PA schematic at fundamental and third harmonic are plotted in Fig. 3.10 (a) and (b). At the fundamental band, two stages of differential cascode PAs are cascaded, and the output is fed to an LC-based balun. At the third harmonic band, due to the lower available G_{max}, a differential pair with neutralization capacitors is implemented for each stage, with a total

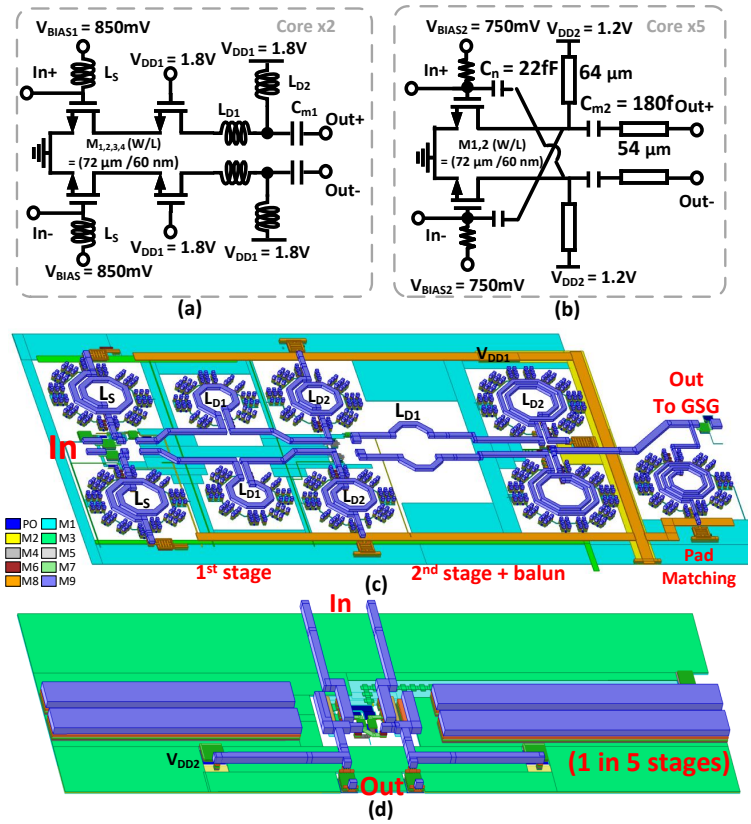

Figure 3.10: Schematic of the PA at (a) fundamental frequency band, (b) third harmonic band; EM view of the PA at (c) fundamental band, (d) third harmonic band (1 in 5 stages).

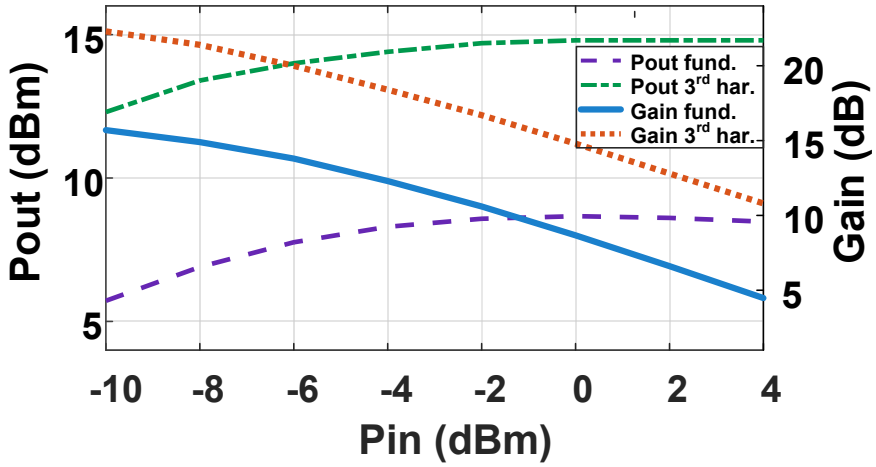

Figure 3.11: Simulated PA P_{out} and power gain vs P_{in}.

of 5 stages cascaded. The output of the third harmonic PA is fed to a Merchand balun.The simulated P_{out} and power gain vs P_{in} for both bands are shown in Fig.3.11.

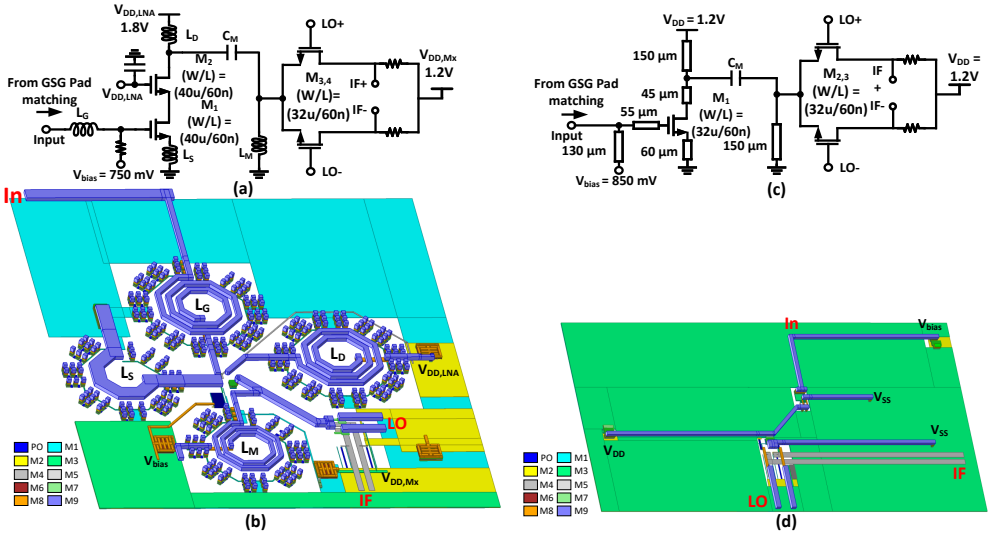

Figure 3.12: (a) Schematic and (b) EM view of the fundamental band RX; (c) Schematic and (d) EM view of the third harmonic band RX.

3.3.5 Low Noise Amplifier

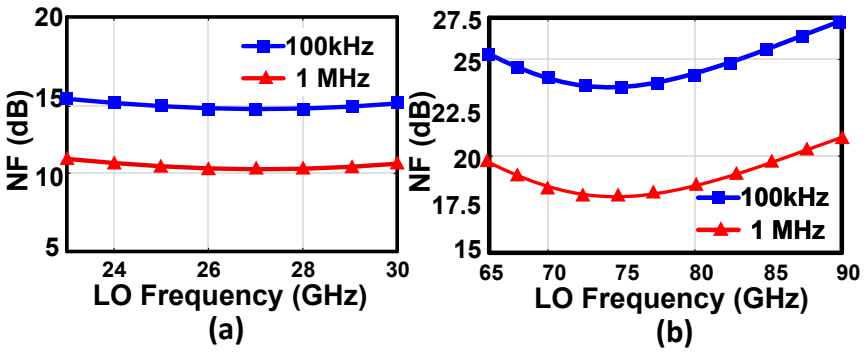

Figure 3.13: Simulated RX noise figure at (a) fundamental band and (b) third harmonic.

A cascode LNA stage with inductive source degeneration is implemented at the fundamental band, and a common source stage with inductive source degeneration LNA is implemented for the higher band, as shown in Fig. 3.12 (a) and (b), respectively. The simulated RX (1-stage LNA + mixer) noise figures at both bands are shown in Fig. 3.13.

3.4 Measurement Results

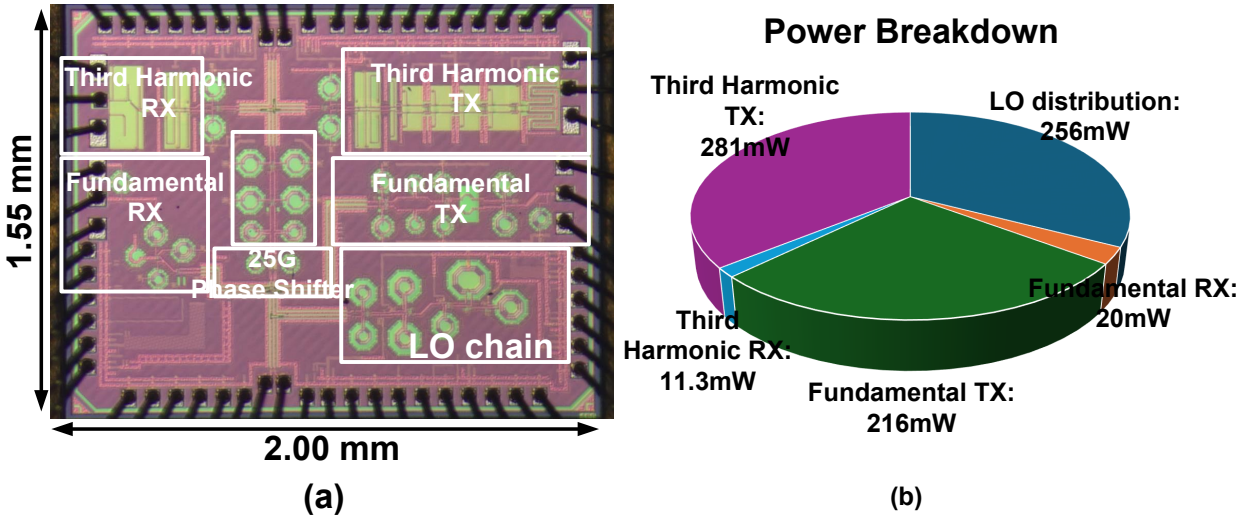

Figure 3.14: (a) Chip microphoto and (b) measured power consumption breakdown of a single chip.

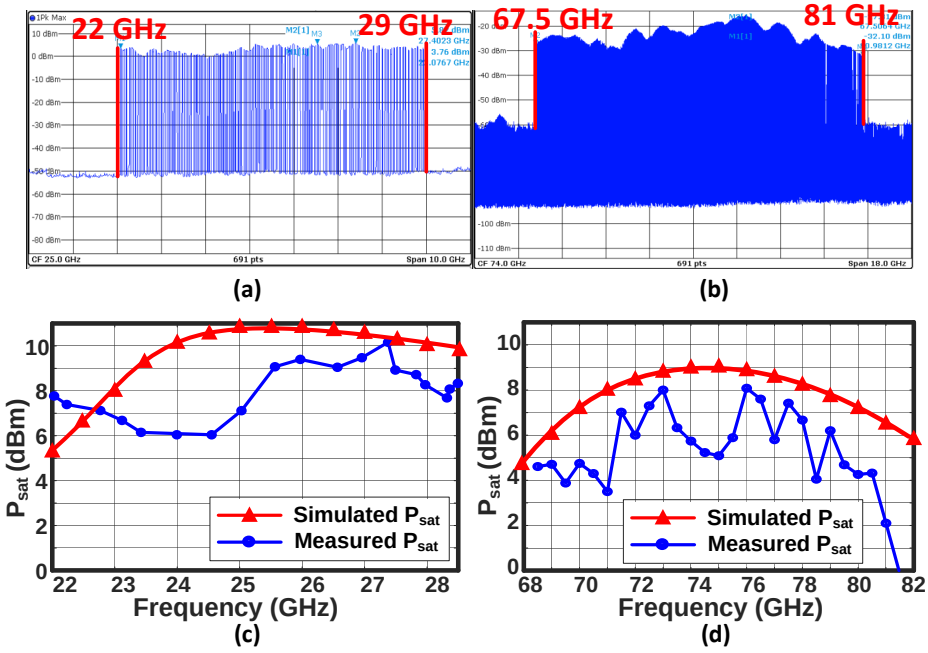

Figure 3.15: Measured chirping spectrum at (a) fundamental and (b) third harmonic. Simulated and measured P_{sat} at (c) fundamental and (d) third harmonic.

The proposed dual-band radar prototype is fabricated using 65nm bulk CMOS technology. As shown in Fig. 3.14 (a), each chip occupies $2 \times 1.55\,\text{mm}^2$ (3.1 mm^2) and consumes 784 mW with both bands operating. The single-chip power consumption breakdown is shown in Fig. 3.14 (b). The measured TX output powers are 10.1 dBm at the fundamental and 8.1

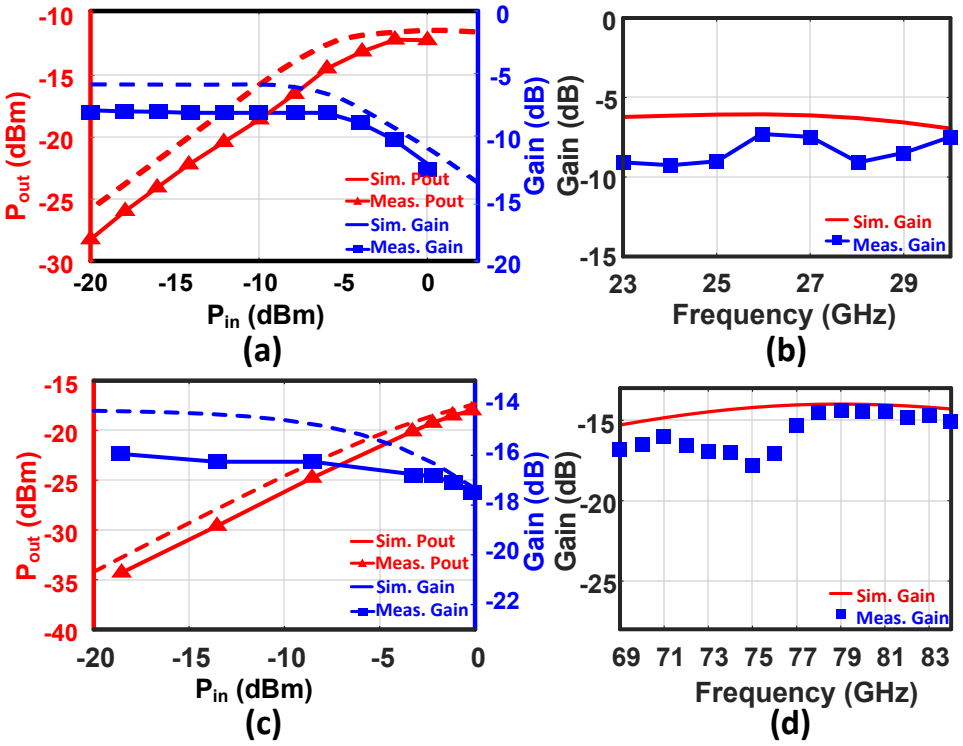

Figure 3.16: Measured and simulated (a) fundamental RX P_{out}, Gain vs P_{in}, (b) conversion gain without baseband amplifier, (c) fundamental RX P_{out}, Gain vs P_{in}, (d) conversion gain without baseband amplifier.

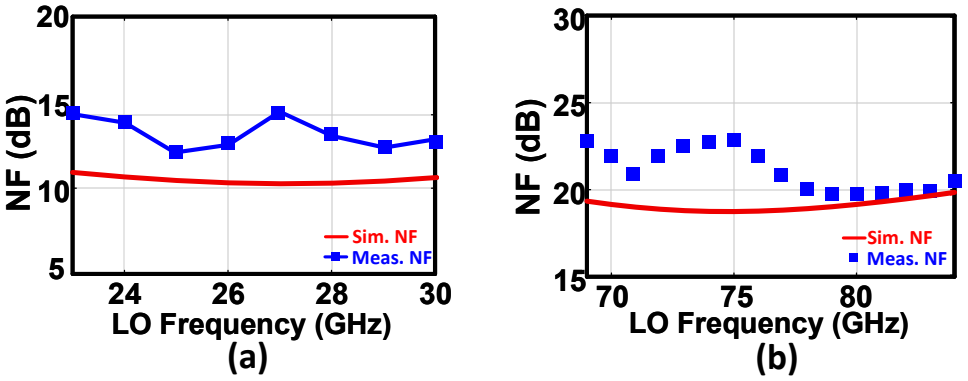

Figure 3.17: Measured and simulated noise figure for (a) fundamental and (b) third harmonic RX at 1 MHz offset.

dBm at the third-harmonic. The PA output spectrum under chirping is shown in Fig. 3.15 (a) and (b) and the measured RX performance is presented in Fig. 4 (top-left) and top-right panel. The RX achieves IP1dB of -5 dBm (25 GHz) and -4 dBm (75GHz) with noise figure of 12.5 dB and 19.6 dB respectively.

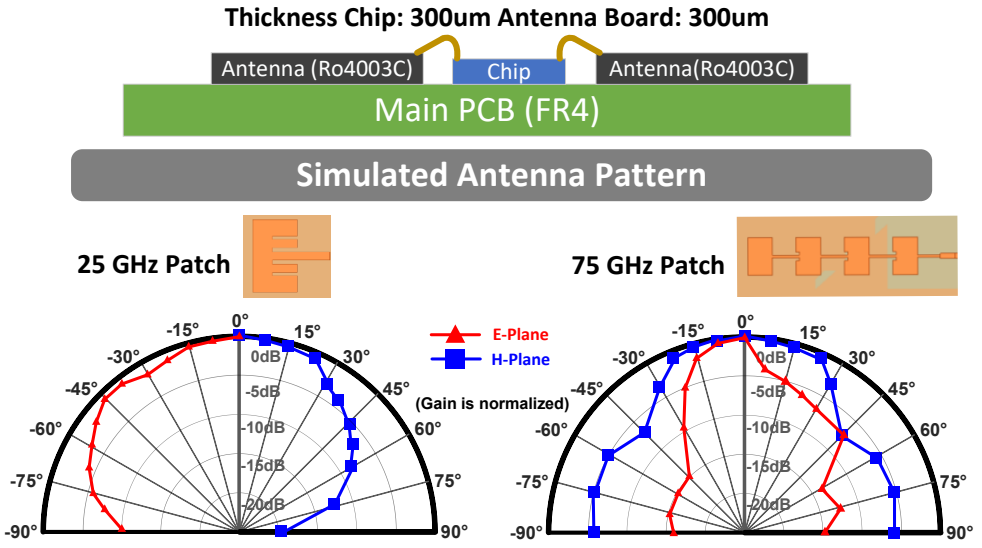

Figure 3.18: Chip package illustration and simulated antenna pattern

The chips are co-packaged with Rogers 4003C patch-antenna boards and mounted on an FR4 PCB with baseband amplifiers, forming a 2TX–2RX system for each band (Fig. 3.18). Two different antenna spacing configurations are implemented (Fig. 3.19). $1.9\lambda_1$ at 25 GHz, $5.7\lambda_2$ at 75 GHz and 2). $2.7\lambda_1$ at 25 GHz and $1.8\lambda_2$ at 75GHz. For over-the-air (OTA) measurements, the injected FMCW signal is generated by a Keysight M8195A arbitrary waveform generator, with baseband signal captured by an R&S RTB2004 oscilloscope. Angular measurements are performed by rotating a corner reflector using protactor (angle-finder) and laser alignment. For configuration 1), the FFT spectrum of the the RX at 25GHz and 75GHz differ by a factor of three times difference due to the three times chirp rate ratio. While this configuration show an excellent synthetic angular resolution of 3.8°, strong grating-lobes severely restricts its FoV. In contrast, the synthetic angle spectrum for configuration 2) shows a 8.8° angular resolution with a 3dB GLS. Applying ±80° phase dithering

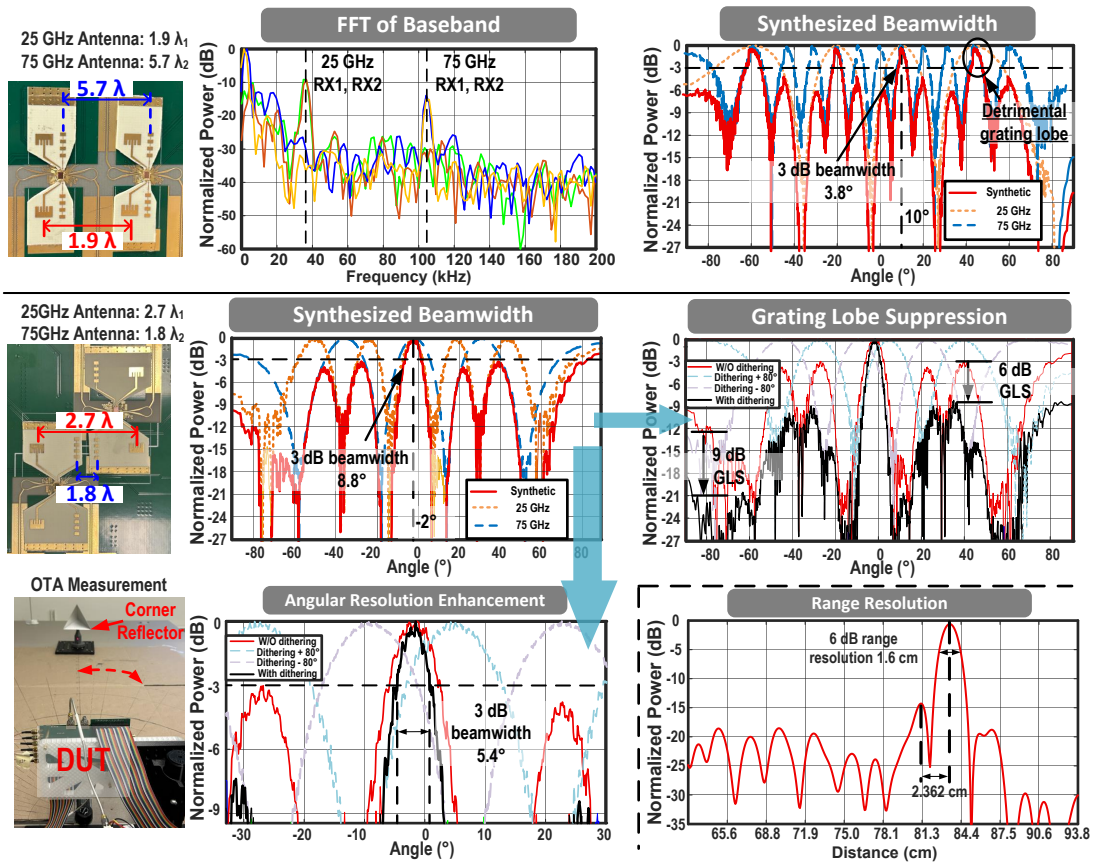

Figure 3.19: Chip package illustration and simulated antenna pattern

significantly enhances GLS (up to 10 dB) and further improves the 3-dB angular resolution to 5.4°. A two-target range-resolution test (Fig. 3.19) demonstrates the radar functionality to resolve nearby targets corresponding to a measured 6-dB range resolution of 1.6 cm. The performance comparisons are summarized in Table 3.2 [70–75].

Table 3.2: Performance Summary and Comparison with State-of-the-Art

Reference	This work	RFIC 2025 [70]	ISSCC 2025 [71]	ISSCC 2023 [72]	ISSCC 2021 [73]	ISSCC 2018 [74]	JSSC 2023 [75]
Process	**65nm CMOS**	65nm CMOS	55nm CMOS	40nm CMOS	45nm CMOS	45nm CMOS	28nm CMOS
Modulation	**FMCW**	FMCW	FMCW	FMCW	FMCW	FMCW	FMCW
Angular Resolution (°)	**5.4**	6	7.64^ / 1.8*	28.66^	9.55^	9.55^	7.17^
#VRX**	**21**	19^	15 / 64*	4	12	12	16
#RX, #TX	**4,4**	12,3	8,8	4,1	4,3	4,3	8,2
Frequency (GHz)	**25/75**	15/30/60	77	85	77	77	77
Modulation BW (GHz)	**4.5/13.5**	1/2/4	8	10	5	4	7.2
TX Pout (dBm)	**10.1/8.1**	11.8/10.1/11.95	-	10	12.1***	10.8	8.1
RX IP1dB (dBm)	**-5/-4**	-0.7/1.5/-0.2***	-	-0.7****	-10	-7	-7
RX NF (dB)	**12.5/19.6**	12.8/15.6/15.4	16.8	11.3	13.8	18	11.2
Total Power (mW)	**1568**	789/821/802	6720	580	3500	3500	3570
Area/Chip (mm^2)	**3.1**	TX:2.16 RX:4.9	67.24	3.26	–	22	33.64

^Calculated from θ=2/#VRX.
*Implemented value / Theoretical value with λ/2 spacing.
**Corresponding to angular resolution, normalized to λ/2 spacing.
***Combined output power.
****IP1dB measured by feeding a CW tone below the 20 kHz LPF.

3.5 Conclusion

This section presents a dual-band, harmonically related FMCW radar transceiver operating at 23–27 GHz and 69–81 GHz. The measured peak output powers are 10.1 dBm at 23–27 GHz and 8.1 dBm at 69–81 GHz. The transceiver is implemented in a 4T4R MIMO module incorporating a patch-antenna board. By applying a non-uniform linear array (nULA) configuration, the aliasing from each frequency band is consolidated into an alias-free grating lobe with approximately 3 dB suppression. Further suppression of up to 10 dB is achieved

through phase-dithering techniques. This architecture delivers an angular resolution of 5.4° and demonstrates a range resolution of 1.6 cm.

Chapter 4

A Single-Switch 3.1-4.7 GHz 194.52-dB FoM Class-D VCO

4.1 Introduction

With the widespread adoption of CMOS integrated circuits (ICs) for the development of Internet of Things (IoT) and implantable biomedical applications [76], there is a growing demand for ultra-low-power CMOS-based frequency synthesizers. The output signal of these synthesizers is used to generate on-chip clocks for digital systems [77] or provide carrier signals for communication and sensing systems [78]. Recent advancements in digital phase-locked loops (DPLL) [79], all-digital phase-locked loops (ADPLL) [80], and other variants of frequency synthesizers have successfully reduced the system-level power consumption to the order of several milliwatts for enhanced system integration. Consequently, reduction of VCO power consumption to sub-mW level in these applications, while maintaining satisfactory phase noise and frequency tuning range, is desirable.

In light of the low-voltage operation of class-D VCOs, there has been a growing research

interest to implement low-power signal sources in the advanced CMOS nodes with scaled power supply. In some of the previous class-D VCO work presented in [81–83], a switch-based transistor model was used to derive the steady state waveform and identify the optimal values for the tank floating capacitors (C_F) and single-ended capacitors (C_{SE}) that achieve the lowest phase noise. Despite impressive phase noise and low-power consumption (sub-5 mW), a trade-off between increasing the tuning range and keeping the optimal phase noise performance across the tuning range has been noted in the prior class-D VCO designs. This is mainly because realization of C_F and C_{SE} by switching capacitors and tuning varactors does not allow to consistently enforce the optimum capacitance ratio C_F/C_{SE}.

Another design consideration for low-power VCOs is the two-point modulation capability when they are deployed in a PLL [84]. The two-point modulation can result in constant modulation sensitivity regardless of the loop bandwidth. It is widely adopted that using multiple switched capacitor banks together with small varactors increases the tuning range while maintaining a small tuning sensitivity (K_{VCO}) for loop stability consideration. However, multi-bit digital switches incorporated in previous CMOS VCOs to extend the tuning range, demand high-resolution logic circuits (e.g., ADCs) to control the switch states which add to the power consumption [85]. With a one-bit switch, a simple one-bit digital functional block (Bang-bang control logic) can be implemented to support two-point modulation as shown in Fig. 4.1. The implemented one-bit switch should also maintain low-phase-noise performance across the tuning range along with identical frequency tuning curves (invariant K_{VCO}) at low frequency (LFB) and high frequency (HFB) bands.

To address the aforementioned challenges, this section presents a one-bit class-D VCO with a new tank architecture deploying varactors and RF chokes that alleviates the C_F/C_{SE} ratio variation by frequency. The presented VCO also achieves almost identical tuning characteristics, i.e., K_{VCO}, for both switching states. The rest of the section is organized as follows. Subsection 4.2 conducts a comparative analysis of steady-state waveforms and their

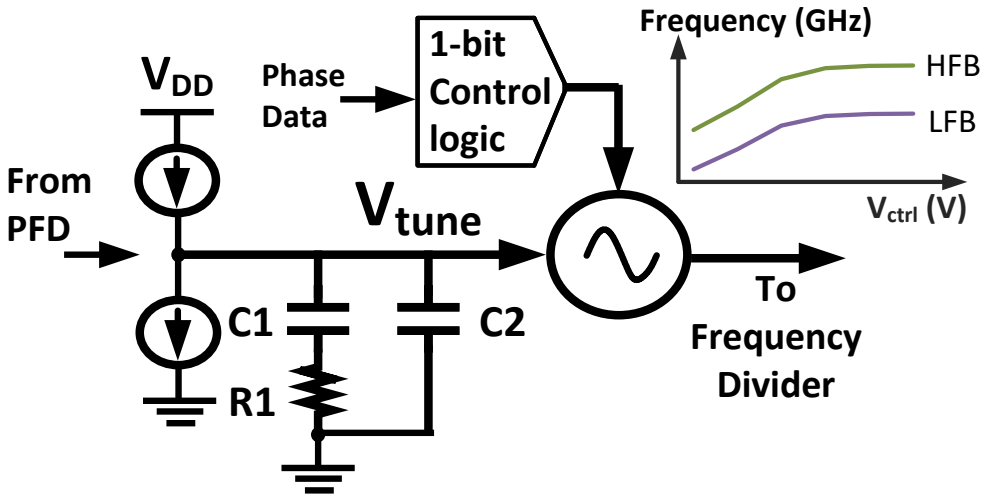

Figure 4.1: Block diagram of VCO with one-bit switch in a phase locked loop.

corresponding phase noise performance to highlight the importance of maintaining a constant C_F/C_{SE} ratio. Subsection 4.3 discusses the realization of the VCO focusing on a novel tank architecture with a constant C_F/C_{SE} ratio. Subsection 4.4 presents the simulation and measurement results that justify the low-power and low-noise performance of the fabricated VCO. Subsection 4.5 concludes this section.

4.2 Optimum C_F/C_{SE} ratio for Waveform shaping

The class-D VCO with both C_F and C_{SE} in the oscillation tank is shown in Fig. 4.2 (a). The transistors are usually biased near threshold voltage so that for half of the period, there is no current in either side of the tank[82]. This low-voltage bias, upon satisfying the oscillator start-up condition, reduces power consumption and at the same time reduces the thermal noise contribution to the phase noise. Three operational scenarios of only C_{SE}, only C_F, and both C_F and C_{SE} present in the tank while the total capacitance is constant, can be perceived in Fig. 4.2(a). Consequently, three different steady state oscillation waveforms can be achieved as shown in Fig. 4.2 (b). It is observed that only under the hybrid condition with both C_F and C_{SE} in the tank at a certain C_F/C_{SE} ratio, the oscillation waveform can

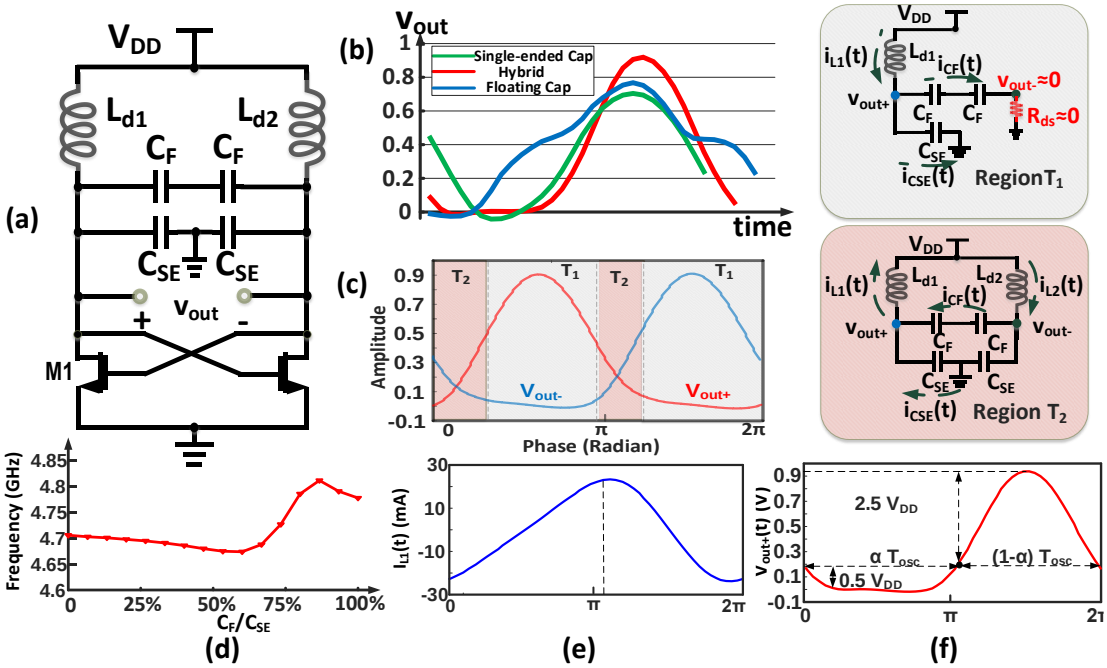

Figure 4.2: (a) Block diagram of Class-D VCO with C_F and C_{SE}, (b) steady state waveforms under all three operational scenarios, (c) steady state oscillation waveform of hybrid condition and the corresponding circuit block diagrams, (d) oscillation frequency under under different C_F/C_{SE} ratios, (e) voltage and (f) current waveform under hybrid condition.

be boosted to close to $3V_{DD}$. Therefore, we focus on the high-swing waveform of hybrid condition and separate the waveform into two regions, T_1 and T_2, as shown in Fig. 4.2(c). The equivalent circuit for each region is shown with the same color on the side of Fig. 4.2(c). During region T_1, the transistor is pushed into triode region and is modeled as a small "ON" resistor on one side, whereas during region T_2 both transistors are in saturation region, which can be treated as open circuit. Therefore, two corresponding tank frequencies, i.e., $\omega_{\text{tank1}} = 1/\sqrt{L_d(C_{SE} + \frac{C_F}{2})}$ and $\omega_{\text{tank2}} = 1/\sqrt{L_d(C_{SE} + C_F)}$ exist during one oscillation period. As shown in Fig. 4.2(d), the simulated oscillation frequency remains relatively unchanged with respect to different C_F/C_{SE} ratios for an invariant $(C_F + C_{SE})$, therefore we can approximate:

$$\omega_{\text{osc}} \simeq \omega_{\text{tank2}}. \tag{4.1}$$

To find the optimum C_F/C_{SE}, the ratio between ω_{tank1} and ω_{tank2} should be calculated. Based on Fig. 4.2 (e,f), when $v_{\text{out+}}(t) = 0$ (region T_1), the inductor current i_{L1} is calculated

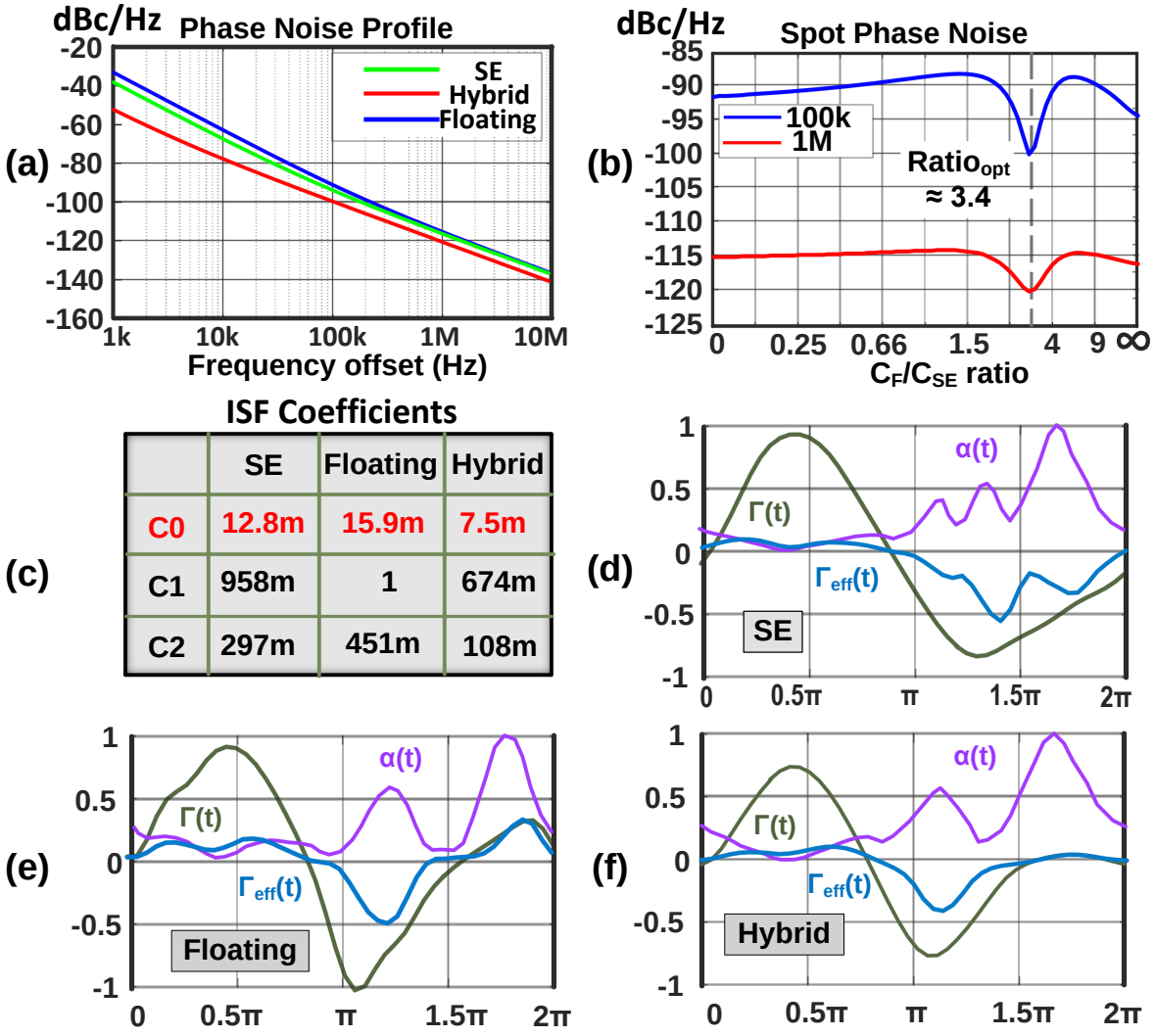

Figure 4.3: (a) Phase noise profile under all three scenarios, (b) phase noise at 100kHz and 1MHz offset for various C_F/C_{SE} ratios in hybrid scenario, (c) table of coefficients of simulated ISF function. $\Gamma(t)$, $\alpha(t)$ and $\Gamma_{\text{eff}}(t)$ of (d) SE (e) floating, and (f) optimum ratio hybrid scenaios.

as:

$$i_{L1}(t) = -I_0 + \frac{1}{L_{d1}} V_{DD} t, \quad 0 \leq t \tag{4.2}$$

$$I_0 = \frac{1}{2} \frac{1}{L_d} V_{DD} \cdot \alpha \cdot T_{osc}, \tag{4.3}$$

$$T_{osc} = \frac{2\pi}{\omega_{\text{osc}}} = \frac{2\pi}{\omega_{\text{tank2}}}, \tag{4.4}$$

$$\frac{\omega_{\text{tank1}}}{\omega_{\text{tank2}}} = \frac{1}{2(1-\alpha)}. \tag{4.5}$$

In (4.5), α is the ratio of the duration of the region with linear current to oscillation period (T_{osc}) as illustrated in Fig. 4.2 (e). Thus, the current when $v_{\text{out+}}(t)) \neq 0$ can be approximated as:

$$i_{L1}(t) = I_0 \cos[\omega_{tank1}(t - \alpha T_{osc})], \quad \alpha T_{osc} \leq t \leq T_{osc}, \tag{4.6}$$

The voltage v_{out+} can be calculated by integrating the current flowing through the capacitor when $v_{\text{out+}}(t)) \neq 0$, which gives:

$$\begin{aligned} v_{out+}(t) = \frac{1}{(C_{SE} + \frac{C_F}{2})} \frac{I_0}{\omega_{tank1}} \sin[\omega_{tank1}(t - \alpha T_{osc})] \\ +0.5V_{DD}, \quad \alpha T_{osc} \leq t \leq T_{osc}, \end{aligned} \tag{4.7}$$

According to Fig. 4.2(f) we approximate $0.5V_{DD}$ as the transition point between linear current region and sinusoidal current region. Therefore, the maximum V_{out+} can be expressed as:

$$V_{out+} = \pi V_{DD} \alpha \frac{\omega_{tank1}}{\omega_{tank2}} = \pi V_{DD} \frac{\alpha}{2(1-\alpha)}. \tag{4.8}$$

To boost the maximum swing to $3V_{DD}$, V_{out+} should be approximately $2.5V_{DD}$, for which α is 0.61, hence:

$$\frac{\omega_{\text{tank1}}}{\omega_{\text{tank2}}} = 1.28, \tag{4.9}$$

and the corresponding optimum C_F/C_{SE} ratio that leads to $3V_{DD}$ swing in the hybrid scenario is 3.5. Under this optimal ratio, the voltage swing is maximized.This optimum ratio is different than that reported in [86, 87] where an ideal sinusoidal signal and a tank including the coupling coefficient k between the inductors were considered, respectively.

Simulation results of phase noise profile for the three operational scenarios and spot phase noise for various C_F/C_{SE} ratios are depicted in Fig. 4.3(a) and (b), respectively. To evaluate the phase noise, we deploy the linear time-invariant model presented in [88]. Accordingly, the simulated impulse sensitivity function (ISF), $\Gamma(t)$, for the transistor noise is extracted. The ISF Fourier coefficients, ISF time-domain function, noise modulating function (NMF) denoted by $\alpha(t)$, and resulted effective ISF for the SE, floating, and hybrid scenario under optimum capacitance ratio are depicted in Fig. 4.3 (c)-(f), respectively. The effective ISF (Γ_{eff}) is calculated as $\Gamma_{eff}(t) = \Gamma(t) \cdot \alpha(t)$ [88]. According to Fig. 4.3 (c), the optimum C_F/C_{SE} ratio in the hybrid scenario achieves the smallest Fourier coefficients of $\Gamma_{eff}(t)$, specially the DC term (C_0). This is because under maximized oscillation swing for a low-voltage bias, the amplitude of $\alpha(t)$ diminishes due to a decrease in the conduction angle, yielding smaller C_0 and thus 1/f noise up-conversion. As mentioned in [88], C_0 will directly impact the corner frequency of flicker noise. Therefore, the proposed optimum ratio not only impacts the suppression of thermal noise, but also helps to reduce the up conversion of flicker noise into PN.

4.3 Circuit Implementation

4.3.1 RF choke based floating capacitor

The conventional method for implementing SE and floating capacitors in VCO leverages continuous tuning varactors and discrete switching capacitors, as illustrated in Fig. 4.4 (a).

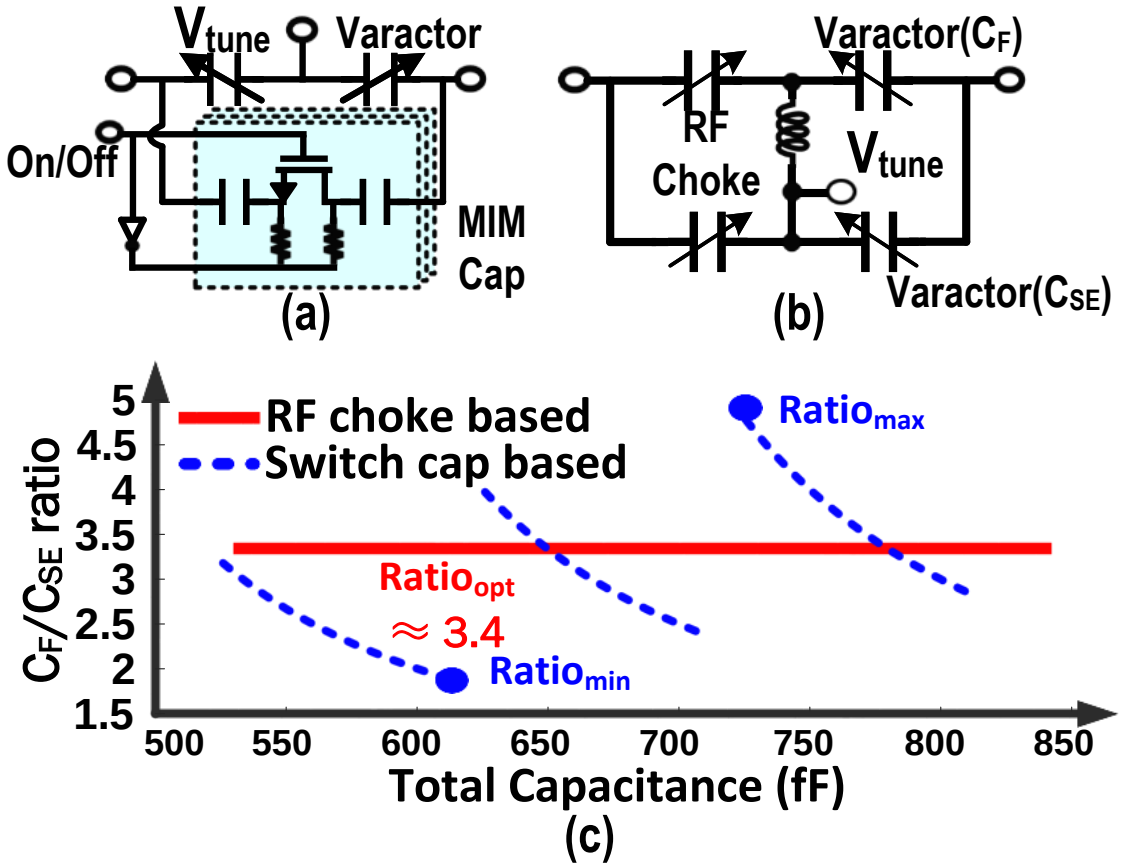

Figure 4.4: Comparison of C_F/C_{SE} ratio with RF choke and switched capacitor

The continuous tuning varactors are regarded as SE capacitors, given that V_{tune} is considered as AC ground, whereas the discrete switching capacitors can be treated as floating capacitors because of the switching transistor's low turn-on resistance.The proposed realization using varactors for both floating and SE paths is shown in Fig. 4.4 (b). An RF choke is incorporated for the floating path and for the varactor implementation, a standard element varying from 17.6 fF to 30.8 fF is used with an array of 9 elements implemented for the SE bank and 31 elements for the floating bank, which enables precise control of the C_F/C_{SE} ratio. The simulated C_F/C_{SE} ratio for both designs is shown in Fig. 4.4(c) highlighting the advantage of proposed design in Fig. 4.4(b) over the conventional design in maintaining a constant optimum C_F/C_{SE} ratio.

The total Q factor of the VCO in Fig. 4.2(a) when the C_{SE} and C_F are designed based on

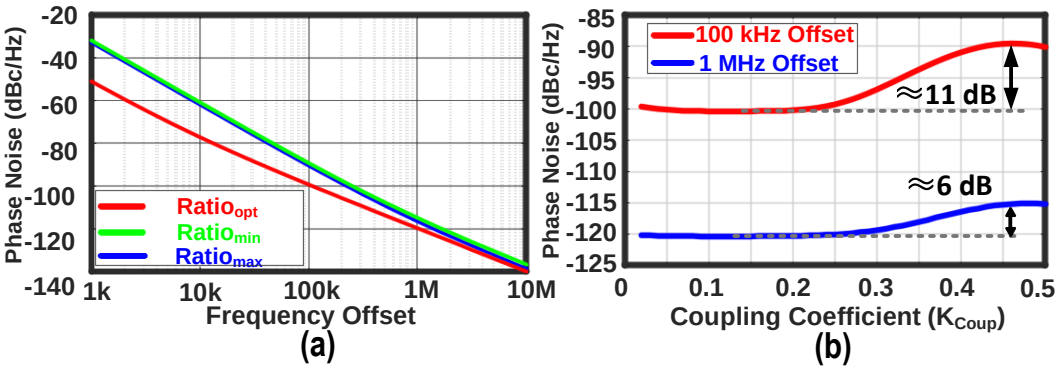

Figure 4.5: (a) Phase noise profile for maximum, minimum and optimum ratio in Fig. 4.4 (c), (b) simulated spot phase noise at 100 kHz and 1 MHz offset vs coupling coefficient K_{coup}.

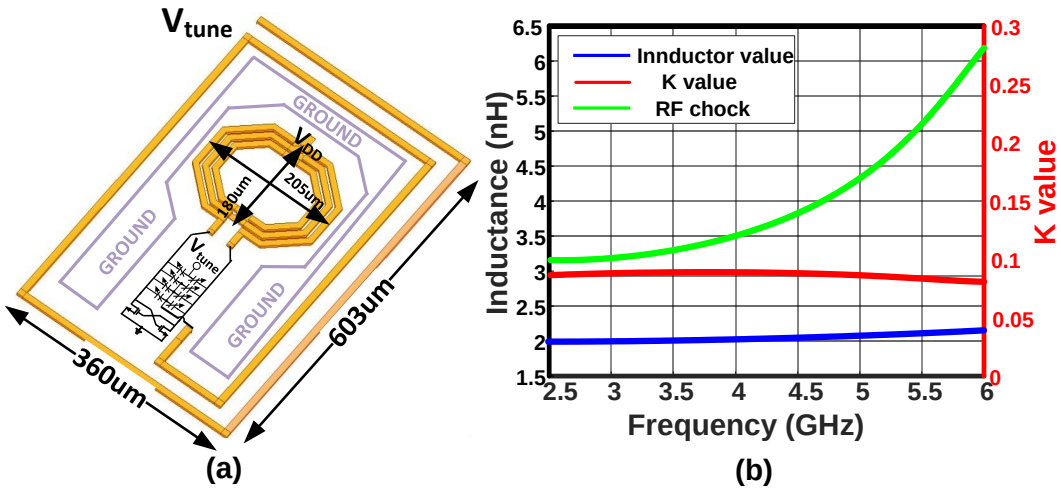

Figure 4.6: (a) HFSS view of RF choke and L_d, (b) simulated inductance of RF choke and tank inductor and coupling coefficient K_{coup}.

Fig. 4.4(a) is calculated by:

$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{C_{\text{var}}}{C_{tot}}\frac{1}{Q_{\text{var}}} + \frac{nC_u}{C_{tot}}\frac{1}{Q_{\text{bank}}}, \tag{4.10}$$

where Q_{tot}, Q_L, Q_{var}, and Q_{bank} are the quality factor of the tank, inductor, varactors, and switching capacitor bank and C_{tot}, C_{var}, C_u, and n are the total capacitance, varactor capacitance, switching capacitor bank, and the number of switches, respectively. In the proposed capacitive network design in Fig. 4.4(b), the total Q factor is determined by $1/Q_{tot} = 1/Q_L + 1/Q_{\text{var}}$ where the Q of the RF choke does not impact the differential fundamental oscillation. Although the Q factor of switching capacitor bank and varactor

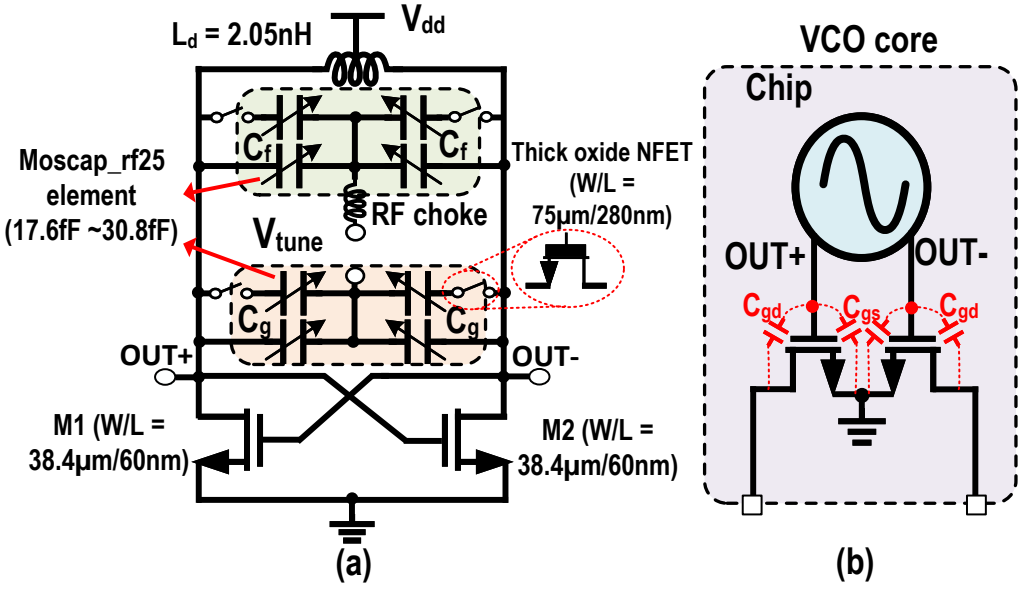

Figure 4.7: Circuit of (a) implemented VCO and (b) open-drain buffer.

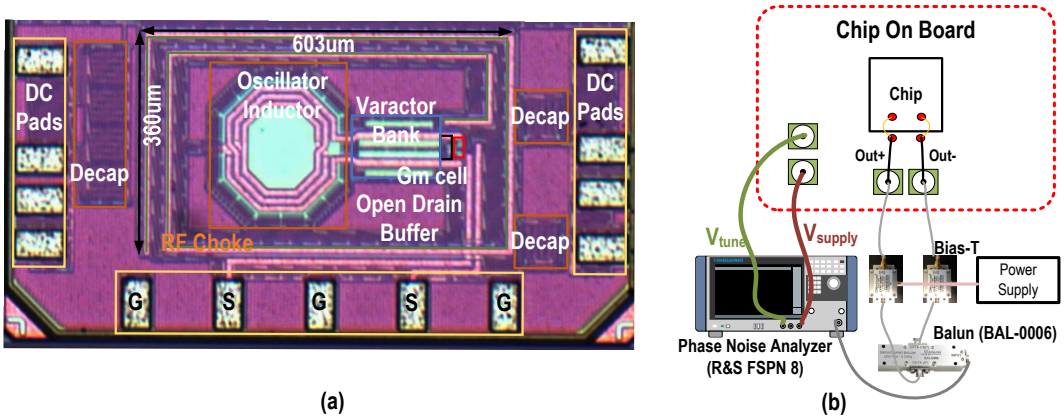

Figure 4.8: (a) Chip photograph of implemented VCO and open-drain buffer, (b) measurement setup.

may vary by the deployed CMOS technology, the total Q is predominantly influenced by the Q factor of the inductor at frequencies below 10 GHz [89] ($Q_{tot} \approx Q_L$), hence a noticeable Q variation between Fig. 4.4(a) and Fig. 4.4(b) is not foreseen. In Fig. 4.5 (a), the simulated phase noise of $ratio_{min}$, $ratio_{max}$ and $ratio_{opt}$ in Fig. 4.4 (c) are plotted and compared. The phase noise of $ratio_{min}$ and $ratio_{max}$ are 10dB and 5dB higher than that of optimum ratio at 100 kHz and 1 MHz offset frequencies, respectively. Therefore it is evident that the inability of the conventional design in Fig. 4.4(a) to maintain the optimum ratio, adversely impacts the phase noise in a wideband VCO.

Although for the design in Fig. 4.4(b), the phase noise variation across the whole tuning range is substantially reduced, the coupling between the RF choke and the tank inductor should be meticulously evaluated. Fig. 4.5(b) illustrates that when the coupling coefficient between the two inductors, K_{coup}, exceeds 0.4, there is a noticeable deterioration in phase noise: an increase of 11 dB at 100 kHz offset and 6 dB at 1 MHz offset. Therefore, the layout of RF choke is characterized in the HFSS EM solver to identify the routing losses and mutual couplings. Since the purpose of RF choke is only to provide a floating point, the performance of VCO is not sensitive to its precise inductance value. Furthermore, to ensure a reliable floating condition for the varactors, a minimum inductance of 3 nH across the tuning range is considered and since the self-resonance frequency (SRF) of the RF choke is close to 10 GHz, on the higher end of the tuning, the inductance rises further to 6.5 nH which creates a higher impedance open circuit. By incorporating minimum 20-μm-thick distributed ground walls between the tank inductor and the choke, the RF choke is winded around the VCO core to achieve reduced K_{coup} and maintaining a compact area, Fig. 4.6(a). The tank inductance value of VCO core and RF choke, as well as coupling coefficient, K_{coup}, were simulated in HFSS EM solver and the simulation results are shown in Fig. 4.6(b). The tank inductor value stays invariant in the presence of RF choke and K_{coup} remains around 0.1 for the entire tuning range which does not degrade the phase noise according to Fig. 4.5(b).

4.3.2 One-bit switch to enhance tuning range

The completed schematic of this VCO is shown in Fig. 4.7(a). To boost the tuning range, a one-bit switch is incorporated for both SE and floating varactor pairs. The deployed switches are implemented by thick oxide transistors (W/L=75μm/280nm) to achieve a small "ON" resistance. The varactor pairs in the switching and non-switching branches are sized such that the C_F/C_{SE} ratio does not vary between "ON" and "OFF" states.

For reliable measurability, a differential open-drain buffer is also designed as shown in Fig.

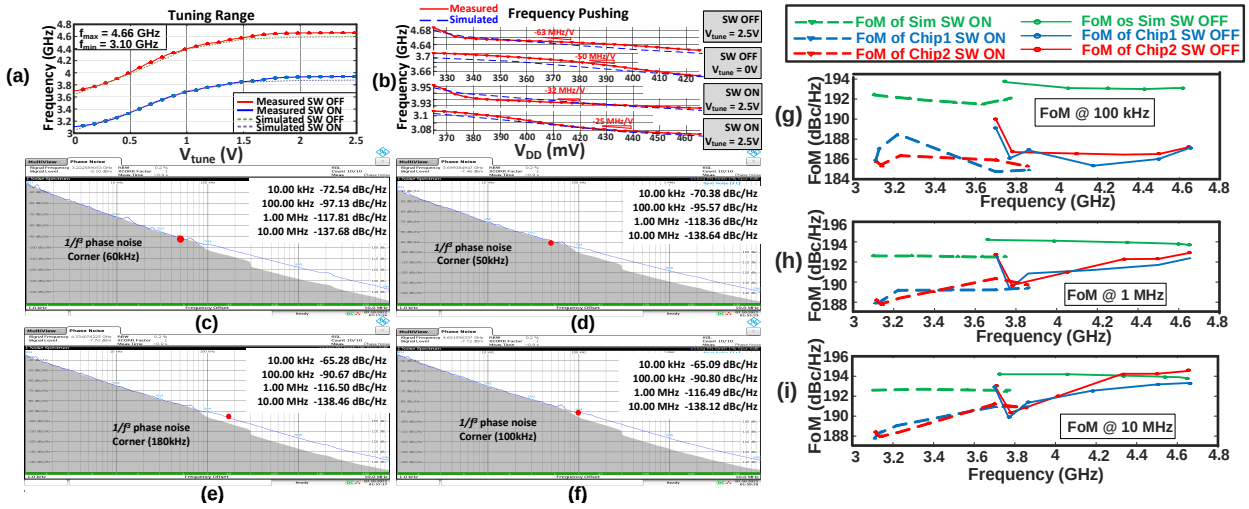

Figure 4.9: Simulated and measured (a) tuning range for both SW on and off, (b) frequency pushing for both SW on and off at V_{tune} = 0 and 2.5V. Measured PN at (c) 3.22 GHz, (d) 3.70 GHz, (e) 4.33 GHz, (f) 4.65 GHz. Simulated and measured FoM of two chips at (g) 100 kHz, (h) 1 MHz, (i) 10 MHz offset.

4.7(b), which introduces extra capacitors to the LC tank. The parasitic C_{gs} =24 fF and C_{gd} =27 fF of the buffer can be treated as SE capacitor using the Miller effect.

4.4 Measurement Results

This VCO is fabricated in 65nm bulk CMOS technology and the chip photograph is shown in Fig. 4.8(a) with a core area of $0.21mm^2$. Fig. 4.8(b) shows the measurement setup. Two bias-Ts are utilized to supply power to the open-drain buffer which is followed by a differential to single-ended balun that is fed into the R&S phase noise analyzer FSPN8. The tuning voltage is directly provided by the phase noise analyzer that is further low pass filtered by on-board decoupling capacitors. The VCO draws 1.5mA from 330mV V_{DD} when Switch is off and 2.1mA from 360mV V_{DD} when Switch is on. Due to the loss associated with switching transistors, a higher V_{DD} is required when switch is on to ensure the oscillation startup.

As shown in Fig. 4.9 (a), when SW is ON, the tuning range is from 3.10 GHz to 3.93 GHz,

and when SW is off, the tuning range is from 3.70 GHz to 4.66 GHz. The combined tuning range from 3.1 GHz to 4.66 GHz corresponds to 40.2% continuous frequency tuning. The tuning curves at lower and higher frequency bands are similar, leading to almost identical K_{VCO} for the same V_{tune} in either of the SW states which is critical for low-power PLL design according to Fig. 1. The frequency pushing for four different conditions of SW states and V_{tune} are measured and shown in Fig. 4.9 (b) which confirm relative robustness against power supply variations.

The phase noise profile is measured averaging 10 iterations for each frequency across the whole band as shown in Fig. 4.9 (c)-(f). The variation of PN in the $1/f^2$ region (due to thermal noise) across the tuning range is less than 2 dB at 1 MHz offset and less than 1 dB at 10 MHz offset, which confirms the effectiveness of the proposed design to maintain the optimum C_F/C_{SE} ratio. The simulated and measured FoM of two chip samples at various frequency spots are depicted in Fig. 4.9(g)-(i). Both chip samples attain similar values for PN and FoM, confirming the robustness against process variations. The FoM when SW is on is slightly lower than when SW is off due to a higher power consumption. The measured VCO exhibits a very low power consumption of only 0.495 mW, while achieving phase noise performances of -118.36 dBc/Hz and -138.64 dBc/Hz at 1 MHz and 10 MHz offsets, respectively. This results in best FoM of 192.89 and 194.52 dBc/Hz at 1 MHz and 10 MHz offsets respectively. The performance comparison with state-of-the-art is summarized in Table I [81–83, 90–95]. According to Table I, this VCO exhibits an state-of-the-art performance in terms of frequency tuning range, power consumption, and phase noise, while attaining high FoM at 10 kHz - 10 MHz offset frequencies and a very low $1/f^3$ corner frequency.

Table 4.1: Performance Summary and Comparison with State-of-the-Art

	Topology	Tech.	V_{DD} (V)	Frequency (GHz)	Tuning range (FTR) (%)	Power (mW)	PN @ (dBc/Hz)			FoM# @ (dBc/Hz)			FoM$_T$## @10MHz dBc/Hz	$1/f^3$ Corner (kHz)	Core area (mm^2)
							100kHz	1MHz	10MHz	100kHz	1MHz	10MHz			
This work	Class-D	65nm	0.33 / 0.36	3.10-4.66	**40.2**	**0.495**	-95.57	-118.36	-138.64	**187.20**	192.89	**194.52**	**206.6**	**50**	0.21
[75]	Class-D	65nm	0.4 / 0.5	3.0-4.8	46	4.0 / 6.8	-102†	-128†	-143.5	183.2	189.2	192*	205.26	800	0.15
[76]	Class-D	65nm	0.35	3.67-4.44	18.7	4.95 - 4.2	-104.4	-129.1	-150.5	188.7	193.5	194.9	200.34	230	0.12
[77]	Class-D	28nm	0.225	2.4	NA	0.171	-90.2	-115.9	-136†	185.5	191.1	191.0*	NA	800**	0.18
[84]	Class-C DCO	28nm	0.3	2.02-2.87	35	0.75	-93.98	-118.19	-133.98	184.4	188.1	184.4	199	60	0.14
[85]	Switching I_{DC}	40nm	0.5	4.0-5.0	22.2	0.58	-89	-113.99	-134.54	183.4	188.4	188.9*	195.83	250	0.14
[86]	Triple Coil VCO	180nm	1	4.2-4.6	9	7.4	-97**	-126.3	-149.3	181.11**	190.5	193.2	192.37	600**	0.52
[87]	Series Res VCO	55nm BiCMOS	1.2	9.96-10.9	9	600	-117	-138	-150**	189	190	182**	181.08	NA	0.54
[88]	Dual Core-VCO	22nm FinFet	1.1	7.1-16.8	80.6	13.5	NA	-116.1	-137.9	NA	186.1	187.6	205.7	1100	0.05
[89]	Class-E	180nm	0.7	4-4.45	10.6	4.9	-102.5	-129.5	-152.75	187.6	194.6	197.9	198.07	1100	0.23

$\text{FoM} = -\text{PN} + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{\text{DC}}/1\text{ mW})$

$\text{FoM}_{\text{T}} = \text{FoM} + 20\log_{10}(FTR/10)$

* FoM not mentioned for a particular frequency offset ** Estimated from measured PN plot

4.5 Conclusion

This section introduced a single-switch class-D VCO capable of improving the power efficiency and maintaining the phase noise performance. It was shown that the largest voltage swing from a class-D VCO is only achievable when the oscillator tank encapsulates both single-ended (SE) and floating capacitors at a certain ratio. Moreover, a novel hybrid varactor bank technique, comprising both floating and single-ended varactors was introduced which was capable of shaping waveforms to achieve higher amplitudes. The novel implementation of floating varactors using an on-chip RF choke was demonstrated, highlighting the practicality of the proposed approach. The method's effectiveness was confirmed through simulations and multiple chip measurements. Given the presented attributes, this VCO is deemed suitable for low-power applications.

Bibliography

[1] X. Liu, B. Moradi, and H. Aghasi, "A single-switch 3.1–4.7 GHz 194.52-dB fom class-d VCO with 495W power consumption," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 10, pp. 4451–4455, 2024.

[2] A. Montazar, X. Liu, Z. Zhang, and H. Aghasi, "A hybrid cmos-polyimide adaptive force radiometric array with 3–5-ghz wireless connectivity," *IEEE Microwave and Wireless Technology Letters*, vol. 35, no. 6, pp. 880–883, 2025.

[3] H. Aghasi, X. Liu, M. Tavakolli Taba, A. Tabatabavakili, and E. Afshari, "Broadband harmonic-assisted power and efficiency enhancement in a 174–232-GHz sige voltage-controlled oscillator," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 6, pp. 1921–1931, 2025.

[4] Z. Wang, H. Wang, Y. O. Hassan, and P. Heydari, "A cmos fully integrated 120-gbps rf-64qam f-band transmitter with an on-chip antenna for 6g wireless communication," in *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2024, pp. 343–346.

[5] M. H. Maktoomi, Z. Wang, H. Wang, S. Saadat, P. Heydari, and H. Aghasi, "A subterahertz wideband stacked-patch antenna on a flexible printed circuit for 6g applications," *IEEE Transactions on Antennas and Propagation*, vol. 70, no. 11, pp. 10 047–10 061, 2022.

[6] B. Moradi, X. Liu, M. M. Green, and H. Aghasi, "A compact CMOS 76–82 GHz superharmonic vco with 189 dBc/hz fom operating based on harmonic-assisted isf manipulation," in *2022 Radio Freq. Integr. Circ. Symp. (RFIC)*, 2022, pp. 215–218.

[7] B. Moradi, X. Liu, and H. Aghasi, "A 76–82 GHz VCO in 65 nm cmos with 189.3 dBc/hz pn fom and 0.6 dBm harmonic power for mm-wave FMCW applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 1, pp. 51–61, 2024.

[8] M. Alesheikh, M. H. Maktoomi, S. Saadat, and H. Aghasi, "An electronically tunable 28-34 ghz 2-d steerable leaky wave antenna," in *2024 IEEE International Symposium on Antennas and Propagation and INC/USNC-URSI Radio Science Meeting (AP-S/INC-USNC-URSI)*, 2024, pp. 379–380.

[9] X. Liu, M. H. Maktoomi, M. Alesheikh, P. Heydari, and H. Aghasi, "A cmos 49–63-ghz phase-locked stepped-chirp fmcw radar transceiver," *IEEE Journal of Solid-State Circuits*, pp. 1–15, 2025.

[10] C. Waldschmidt, J. Hasch, and W. Menzel, "Automotive radar — from first efforts to future systems," *IEEE J. Microwaves*, vol. 1, no. 1, pp. 135–148, 2021.

[11] J. Hasch, E. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microwave Theory and Techniques*, vol. 60, no. 3, pp. 845–860, 2012.

[12] J. Weiß, R. Pérez, and E. Biebl, "Improved people counting algorithm for indoor environments using 60 GHz FMCW radar," in *2020 IEEE Radar Conference (RadarConf20)*, 2020, pp. 1–6.

[13] R. Jacobi and A. Aginskiy, "Choosing 60-GHz mmWave sensors over 24-GHz to enable smarter industrial applications," *Nov 2018, Texas Instruments*, 2018.

[14] M. Alesheikh, R. Feghhi, F. M. Sabzevari, A. Karimov, M. Hossain, and K. Rambabu, "Design of a high-power gaussian pulse transmitter for sensing and imaging of buried objects," *IEEE Sensors Journal*, vol. 22, no. 1, pp. 279–287, 2022.

[15] X. Liu, M. H. Maktoomi, M. Alesheikh, P. Heydari, and H. Aghasi, "A 49-63 GHz phase-locked FMCW radar transceiver for high resolution applications," in *ESSCIRC 2023-IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, 2023, pp. 509–512.

[16] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 ghz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, 2010.

[17] S. Park, A. Kankuppe, P. Renukaswamy, D. Guermandi, A. Visweswaran, J. C. Garcia, S. Sinha, P. Wambacq, and J. Craninckx, "A 62mw 60ghz FMCW radar in 28nm CMOS," in *2020 IEEE Radio Freq. Integr. Circ. Symp. (RFIC)*, 2020, pp. 31–34.

[18] H. Aghasi and P. Heydari, "Millimeter-wave radars-on-chip enabling next-generation cyberphysical infrastructures," *IEEE Communications Magazine*, vol. 58, no. 12, pp. 70–76, 2020.

[19] B. van Berlo, A. Elkelany, T. Ozcelebi, and N. Meratnia, "Millimeter wave sensing: A review of application pipelines and building blocks," *IEEE Sensors Journal*, vol. 21, no. 9, pp. 10 332–10 368, 2021.

[20] S. Rao, "Introduction to mmWave sensing: FMCW radars," *Texas Instruments (TI) mmWave Training Series*, pp. 1–11, 2017.

[21] Y.-P. Su, C.-Y. Huang, and S.-J. Chen, "A 24-GHz fully integrated CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3307–3317, 2021.

[22] K. Dandu, S. Samala, K. Bhatia, M. Moallem, K. Subburaj, Z. Ahmad, D. Breen, S. Jang, T. Davis, M. Singh, S. Ram, V. Dudhia, M. DeWilde, D. Shetty, J. Samuel, Z. Parkar, C. Chi, P. Loya, Z. Crawford, J. Herrington, R. Kulak, A. Daga, R. Raavi,

R. Teja, R. Veettil, D. Khemraj, I. Prathapan, P. Narayanan, N. Narayanan, S. Anandwade, J. Singh, V. Srinivasan, N. Nayak, K. Ramasubramanian, B. Ginsburg, and V. Rentala, "2.2 high-performance and small form-factor mm-wave CMOS radars for automotive and industrial sensing in 76-to-81GHz and 57-to-64GHz bands," in *2021 IEEE Int. Solid-State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 39–41.

[23] B. P. Ginsburg, K. Subburaj, S. Samala, K. Ramasubramanian, J. Singh, S. Bhatara, S. Murali, D. Breen, M. Moallem, K. Dandu, S. Jalan, N. Nayak, R. Sachdev, I. Prathapan, K. Bhatia, T. Davis, E. Seok, H. Parthasarathy, R. Chatterjee, V. Srinivasan, V. Giannini, A. Kumar, R. Kulak, S. Ram, P. Gupta, Z. Parkar, S. Bhardwaj, Y. C. Rakesh, K. A. Rajagopal, A. Shrimali, and V. Rentala, "A multimode 76-to-81GHz automotive radar transceiver with autonomous monitoring," in *2018 IEEE Int. Solid-State Circuits Conference - (ISSCC)*, 2018, pp. 158–160.

[24] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22–29-GHz/77–81-GHz BiCMOS transceiver for automotive radars," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, 2009.

[25] A. Arbabian, S. Callender, S. Kang, M. Rangwala, and A. M. Niknejad, "A 94 GHz mm-wave-to-baseband pulsed-radar transceiver with applications in imaging and gesture recognition," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1055–1071, 2013.

[26] F. Norouzian, E. G. Hoare, E. Marchetti, M. Cherniakov, and M. Gashinova, "Next generation, low-thz automotive radar – the potential for frequencies above 100 GHz," in *2019 20th Int. Radar Symp. (IRS)*, 2019, pp. 1–7.

[27] D. M. Pozar, *Microwave engineering: theory and techniques*. John wiley & sons, 2021.

[28] M. I. Skolnik, *Introduction to radar systems*. McGraw-hill New York, 1980, vol. 3.

[29] H. S. Son, J. Y. Jang, D. M. Kang, H. J. Lee, and C. S. Park, "A 109 GHz CMOS power amplifier with 15.2 dbm psat and 20.3 db gain in 65-nm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 7, pp. 510–512, 2016.

[30] A. E. Jarihani, S. Sarafi, M. Köberle, J. Sturm, and A. M. Tonello, "Characterization of on-chip interconnects: Case study in 28 nm CMOS technology," in *2019 Austrochip Workshop on Microelectronics (Austrochip)*. IEEE, 2019, pp. 93–99.

[31] M. H. Maktoomi, S. Saadat, O. Momeni, P. Heydari, and H. Aghasi, "Broadband antenna design for terahertz communication systems," *IEEE Access*, vol. 11, pp. 20 897–20 911, 2023.

[32] S. Samala, "Signal processing and frequency generation in FMCW radar," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, 2018, pp. 1–73.

[33] I. V. Komarov and S. M. Smolskiy, *Fundamentals of short-range FM radar*. Artech House, 2003.

[34] A. Bourdoux, M. Bauduin, K. Vaesen, M. Glassée, E. D. Greef, T. Gielen, and L. Ocket, "A CMOS-based 140 GHz 4x4 mimo radar prototype with 10 GHz bandwidth," in *2023 24th Int. Radar Symp. (IRS)*, 2023, pp. 1–10.

[35] C. Xu, X. Liao, M. Yang, F. Hong, P. Ju, W. Chen, P. Diao, H. Gong, X. Liu, X. You, and D. Zhao, "A packaged 54-to-69-GHz wideband 2t2r FMCW radar transceiver employing cascaded-pll topology and ptat-enhanced temperature compensation in 40-nm CMOS," *IEEE J. Solid-State Circuits*, pp. 1–16, 2024.

[36] H. Jia, L. Kuang, W. Zhu, Z. Wang, F. Ma, Z. Wang, and B. Chi, "A 77 GHz frequency doubling two-path phased-array FMCW transceiver for automotive radar," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2299–2311, 2016.

[37] T. Ma, W. Deng, Z. Chen, J. Wu, W. Zheng, S. Wang, N. Qi, Y. Liu, and B. Chi, "A CMOS 76–81-GHz 2-TX 3-RX FMCW radar transceiver based on mixed-mode pll chirp generator," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 233–248, 2020.

[38] A. Townley, P. Swirhun, D. Titz, A. Bisognin, F. Gianesello, R. Pilard, C. Luxey, and A. M. Niknejad, "A 94-GHz 4TX–4RX phased-array FMCW radar transceiver with antenna-in-package," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1245–1259, 2017.

[39] A. Ahmed, L. Li, M. Jung, and G. M. Rebeiz, "A 140 GHz FMCW ultra wideband high dynamic range radar utilizing 8x8 phased arrays," in *2024 IEEE/MTT-S Int. Microwave Symp. - IMS 2024*, 2024, pp. 489–492.

[40] X. Chen, X. Yi, M. I. W. Khan, X. Li, W. Chen, J. Zhu, Y. Yang, K. E. Kolodziej, N. M. Monroe, and R. Han, "A 140-GHz FMCW TX/RX-antenna-sharing transceiver with low-inherent-loss duplexing and adaptive self-interference cancellation," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3631–3645, 2022.

[41] S. Cerida Rengifo, F. Chicco, E. Le Roux, and C. Enz, "An ultralow power short-range 60-GHz FMCW radar in 22-nm FDSOI CMOS," *IEEE Trans. Microwave Theory and Techniques*, vol. 72, no. 4, pp. 2548–2559, 2024.

[42] A. Mostajeran, S. M. Naghavi, M. Emadi, S. Samala, B. P. Ginsburg, M. Aseeri, and E. Afshari, "A High-Resolution 220-GHz Ultra-Wideband Fully Integrated ISAR Imaging System," *IEEE Trans. Microwave Theory and Techniques*, vol. 67, no. 1, pp. 429–442, 2019.

[43] V. Kafedziski and G. Josifovski, "Usrp implementation of a high resolution FMCW radar using a stepped chirp waveform," in *2024 31st International Conference on Systems, Signals and Image Processing (IWSSIP)*, 2024, pp. 1–5.

[44] L. Zhang, Z. Qiao, M. Xing, Y. Li, and Z. Bao, "High-resolution isar imaging with sparse stepped-frequency waveforms," *IEEE Trans. Geoscience and Remote Sensing*, vol. 49, no. 11, pp. 4630–4651, Nov 2011.

[45] R. Behzad, *RF microelectronics*. Prentice hall New York, 2012.

[46] H. Afzal, R. Abedi, R. Kananizadeh, P. Heydari, and O. Momeni, "An mm-wave scalable PLL-coupled array for phased-array applications in 65-nm CMOS," *IEEE Trans. Microwave Theory and Techniques*, vol. 69, no. 2, pp. 1439–1452, 2020.

[47] S.-L. Jang, W.-C. Lai, G.-Y. Lin, and C. Y. Huang, "Injection-locked frequency divider with a resistively distributed resonator for wide-locking-range performance," *IEEE Trans. Microwave Theory and Techniques*, vol. 67, no. 2, pp. 505–517, 2018.

[48] F. Centurelli, G. Scotti, and G. Palumbo, "A very-low-voltage frequency divider in folded mos current mode logic with complementary n-and p-type flip-flops," *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, vol. 29, no. 5, pp. 998–1008, 2021.

[49] K. Hadipour, A. Ghilioni, A. Mazzanti, M. Bassi, and F. Svelto, "A 40 GHz to 67GHz bandwidth 23dB gain 5.8 dB maximum NF mm-Wave LNA in 28nm CMOS," in *2015 IEEE Radio Freq. Integr. Circ. Symp. (RFIC)*. IEEE, 2015, pp. 327–330.

[50] B. Razavi, "Lower bounds on power consumption of clock generators for adcs," in *2020 IEEE Int. Symp. on Circuits and Systems (ISCAS)*. IEEE, 2020, pp. 1–5.

[51] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, "A 220-to-320-GHz FMCW radar in 65-nm CMOS using a frequency-comb architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 327–339, 2021.

[52] S. A.-R. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, "Analysis and design of a multi-core oscillator for ultra-low phase noise," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 63, no. 4, pp. 529–539, 2016.

[53] L. Iotti, A. Mazzanti, and F. Svelto, "Insights into phase-noise scaling in switch-coupled multi-core lc vcos for e-band adaptive modulation links," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1703–1718, 2017.

[54] W. L. Chan and J. R. Long, "A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, 2010.

[55] D. Pan, Z. Duan, Y. Wang, C. Wang, Y. Li, L. Sun, and L. Cheng, "A 77-GHz power amplifier with digital power control for multi-mode automotive radar in 28-nm bulk CMOS," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 875–879, 2023.

[56] V.-S. Trinh and J.-D. Park, "Common-mode stability test and design guidelines for a transformer-based push-pull power amplifier," *IEEE Access*, vol. 8, pp. 42 243–42 250, 2020.

[57] Z. Wang and P. Heydari, "A study of operating condition and design methods to achieve the upper limit of power gain in amplifiers at near- f_{max} frequencies," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 64, no. 2, pp. 261–271, 2017.

[58] M. Sayginer and G. M. Rebeiz, "A W-band LNA/phase shifter with 5-dB NF and 24-mW power consumption in 32-nm CMOS SOI," *IEEE Trans. Microwave Theory and Techniques*, vol. 66, no. 4, pp. 1973–1982, 2018.

[59] L. Gao, E. Wagner, and G. M. Rebeiz, "Design of E- and W-band low-noise amplifiers in 22-nm CMOS FD-SOI," *IEEE Trans. Microwave Theory and Techniques*, vol. 68, no. 1, pp. 132–143, 2020.

[60] T. Murakami, N. Hasegawa, Y. Utagawa, T. Arai, and S. Yamaura, "A 9 dB noise figure fully integrated 79 GHz automotive radar receiver in 40 nm CMOS technology," in *2019 IEEE Radio Freq. Integr. Circ. Symp. (RFIC)*, 2019, pp. 307–310.

[61] H. Wang, H. Afzal, and O. Momeni, "A highly accurate and sensitive mmWave displacement-sensing doppler radar with a quadrature-less edge-driven phase demodulator," *IEEE J. Solid-State Circuits*, 2023.

[62] S. Zhou and M.-C. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, 2005.

[63] M. Kalantari, W. Li, H. Shirinabadi, A. Fotowat-Ahmady, and C. P. Yue, "A W-band single-antenna FMCW radar transceiver with adaptive leakage cancellation," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1655–1667, 2021.

[64] I. Nasr, R. Jungmaier, A. Baheti, D. Noppeney, J. S. Bal, M. Wojnowski, E. Karagozler, H. Raja, J. Lien, I. Poupyrev, and S. Trotta, "A highly integrated 60 GHz 6-channel transceiver with antenna in package for smart sensing and short-range communications," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2066–2076, 2016.

[65] E. Öztürk, D. Genschow, U. Yodprasit, B. Yilmaz, D. Kissinger, W. Debski, and W. Winkler, "A 60 GHz SiGe BiCMOS monostatic transceiver for radar applications," in *2017 IEEE MTT-S Int. Microwave Symp. (IMS)*, 2017, pp. 1408–1411.

[66] J. Rimmelspacher, R. Ciocoveanu, G. Steffan, M. Bassi, and V. Issakov, "Low power low phase noise 60 GHz multichannel transceiver in 28 nm CMOS for radar applications," in *2020 IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2020, pp. 19–22.

[67] K. Dandu and et al, "2.2 High-performance and small form-factor mm-wave CMOS radars for automotive and industrial sensing in 76-to-81GHz and 57-to-64GHz bands," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 39–41.

[68] D. Schwarz, N. Riese, I. Dorsch, and C. Waldschmidt, "System performance of a 79 GHz high-resolution 4D imaging MIMO radar with 1728 virtual channels," *IEEE Journal of Microwaves*, vol. 2, no. 4, pp. 637–647, 2022.

[69] S. Rao, "Introduction to mmWave sensing: FMCW radars," *Texas Instruments (TI) mmWave Training Series*, pp. 1–11, 2017.

[70] R. Liao, H. Wang, J. Zhang, W.-H. Yu, Y. Song, H. An, H. Liu, and K. Kang, "A 15/30/60-ghz 1tx/4rx radar chipset achieving 6° angular resolution using frequency dimension for virtual aperture expansion," in *2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2025, pp. 395–398.

[71] Z. Zhang, Y. Lu, W. Xu, B. Cui, C. Hu, Z. Zhang, S. Sun, Z. Ren, C. Zhang, Z. Wang, G. Chen, C. Shi, L. Huang, L. Xu, and R. Zhang, "10.1 a 77ghz hybrid tdma-mimo phased-array radar with 186m detection range and 3cm range resolution," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 01–03.

[72] J. Zhang, A. Singhvi, S. S. Ahmed, and A. Arbabian, "18.1 a w-band transceiver array with 2.4ghz lo synchronization enabling full scalability for fmcw radar," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 282–284.

[73] K. Dandu, S. Samala, K. Bhatia, M. Moallem, K. Subburaj, Z. Ahmad, D. Breen, S. Jang, T. Davis, M. Singh, S. Ram, V. Dudhia, M. DeWilde, D. Shetty, J. Samuel, Z. Parkar, C. Chi, P. Loya, Z. Crawford, J. Herrington, R. Kulak, A. Daga, R. Raavi, R. Teja, R. Veettil, D. Khemraj, I. Prathapan, P. Narayanan, N. Narayanan, S. Anandwade, J. Singh, V. Srinivasan, N. Nayak, K. Ramasubramanian, B. Ginsburg, and V. Rentala, "2.2 high-performance and small form-factor mm-wave cmos radars for automotive and industrial sensing in 76-to-81ghz and 57-to-64ghz bands," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 39–41.

[74] B. P. Ginsburg, K. Subburaj, S. Samala, K. Ramasubramanian, J. Singh, S. Bhatara, S. Murali, D. Breen, M. Moallem, K. Dandu, S. Jalan, N. Nayak, R. Sachdev, I. Prathapan, K. Bhatia, T. Davis, E. Seok, H. Parthasarathy, R. Chatterjee, V. Srinivasan, V. Giannini, A. Kumar, R. Kulak, S. Ram, P. Gupta, Z. Parkar, S. Bhardwaj, Y. C. Rakesh, K. A. Rajagopal, A. Shrimali, and V. Rentala, "A multimode 76-to-81ghz automotive radar transceiver with autonomous monitoring," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2018, pp. 158–160.

[75] Z. Duan, B. Wu, Y. Wang, Y. Fang, Y. Li, Y. Wu, T. Zhang, C. Zhu, Y. Dai, L. Sang, and H. Gao, "A 76–81 ghz 2×8 mimo radar transceiver with broadband fast chirp generation and 16-antenna-in-package virtual array," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 11, pp. 3103–3112, 2023.

[76] S. J. Kim, C. S. Park, and S.-G. Lee, "A 2.4-GHz ternary sequence spread spectrum OOK transceiver for reliable and ultra-low power sensor network applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2976–2987, 2017.

[77] Z. Wang and P. R. Kinget, "A 65nm CMOS, 3.5-to-11GHz, less-than-1.45LSB-inlpp, 7b twin phase interpolator with a wideband, low-noise delta quadrature delay-locked loop for high-speed data links," in *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 292–294.

[78] X. Liu, M. H. Maktoomi, M. Alesheikh, P. Heydari, and H. Aghasi, "A 49-63 ghz phase-locked fmcw radar transceiver for high resolution applications," in *ESSCIRC 2023-IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, 2023, pp. 509–512.

[79] Y.-H. Liu, J. Van Den Heuvel, T. Kuramochi, B. Busze, P. Mateman, V. K. Chillara, B. Wang, R. B. Staszewski, and K. Philips, "An ultra-low power 1.7-2.7 GHz fractional-n sub-sampling digital frequency synthesizer and modulator for iot applications in 40 nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 5, pp. 1094–1105, 2016.

[80] T. Jang, S. Jeong, D. Jeon, K. D. Choo, D. Sylvester, and D. Blaauw, "8.4 a 2.5 ps 0.8-to-3.2 GHz bang-bang phase-and frequency-detector-based all-digital PLL with noise self-adjustment," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2017, pp. 148–149.

[81] X. Lin, J. Yin, P.-I. Mak, and R. P. Martins, "A swing-enhanced Class-D VCO using a periodically time-varying (PTV) inductor," *IEEE Solid-State Circuits Letters*, vol. 5, pp. 25–28, 2022.

[82] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, 2013.

[83] Y. Yoshihara, H. Majima, and R. Fujimoto, "A 0.171-mW, 2.4-GHz Class-D VCO with dynamic supply voltage control," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, 2014, pp. 339–342.

[84] S. Lee, J. Lee, H. Park, K.-Y. Lee, and S. Nam, "Self-calibrated two-point delta–sigma modulation technique for rf transmitters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 7, pp. 1748–1757, 2010.

[85] B. Bechen, T. v. d. Boom, D. Weiler, and B. J. Hosticka, "Theoretical and practical minimum of the power consumption of 3 adcs in sc technique," in *2007 18th European Conference on Circuit Theory and Design*, 2007, pp. 444–447.

[86] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A 1/f noise upconversion reduction technique for voltage-biased rf cmos oscillators," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, 2016.

[87] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in lc oscillators," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, 2017.

[88] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE journal of solid-state circuits*, vol. 33, no. 2, pp. 179–194, 1998.

[89] G. Li, L. Liu, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, 2012.

[90] J. Du, Y. Hu, T. Siriburanon, and R. B. Staszewski, "A 0.3V, 35% tuning-range, 60kHz 1/f3-corner digitally controlled oscillator with vertically integrated switched capacitor banks achieving FoMt of -199dB in 28-nm CMOS," in *2019 IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1–4.

[91] M. Babaie, M. Shahmohammadi, and R. B. Staszewski, "A 0.5V 0.5mW switching current source oscillator," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2015, pp. 183–186.

[92] Y. Sun, W. Deng, H. Jia, Z. Wang, and B. Chi, "A 4.4-GHz 193.2-dB FoM 8-shaped-inductor based LC-VCO using orthogonal-coupled triple-coil transformer," *IEEE TCAS II: Express Briefs*, vol. 69, no. 10, pp. 4028–4032, 2022.

[93] A. Franceschin, D. Riccardi, and A. Mazzanti, "Series-resonance BiCMOS VCO with phase noise of-138dBc/Hz at 1MHz offset from 10GHz and-190dBc/Hz FoM," in *2022 IEEE ISSCC*, vol. 65, 2022, pp. 1–3.

[94] J. Gong, B. Patra, L. Enthoven, J. van Staveren, F. Sebastiano, and M. Babaie, "A 0.049 mm2 7.1-to-16.8 GHz dual-core triple-mode VCO achieving 200dB FoM in 22nm FinFET," in *2022 IEEE ISSCC*, vol. 65. IEEE, 2022, pp. 1–3.

[95] M. Barzgari, A. Ghafari, A. Nikpaik, and A. Medi, "Even-harmonic Class-E CMOS Oscillator," *IEEE JSSC*, vol. 57, no. 6, pp. 1594–1609, 2022.