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A HIGH-SPEED 4096-CHANNEL ANALOGUE-DIGITAL CONVERTER FOR PULSE HEIGHT ANALYSIS

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ABSTRACT

A 12-bit analogue-digital converter of the successive binary approximation type is described. The unit accepts input pulses less than 1 μsec long and produces a 12-bit digital output in a register in less than 25 μsec. Use of the random pedestal technique described by Gatti[1)] and careful design results in essentially equal channel widths from channel 40 to 4000. Integrated circuits are used for all digital operations, producing a compact unit despite the circuit complexity of the successive approximation technique. The unit is designed for convenient linking to a computer using either its program interrupt or direct memory access facilities, but can be operated equally well with any memory unit.

INTRODUCTION

Amplitude analysis of electrical impulses from radiation detectors plays a major role in nuclear spectroscopy. Recent developments in semiconductor detectors and associated low-noise amplifiers have resulted in considerable improvements in energy-resolution capabilities and have placed emphasis on the development of pulse-height analyzers having many more channels than were formerly required for scintillation spectroscopy. The importance of this problem may be illustrated by considering two examples:

a) γ-ray spectroscopy in the energy range up to 1.5 MeV with a full-width at half maximum (FWHM) resolution of about 2 KeV, is now possible using germanium detectors. The ideal analysis system should cover the entire range from about 15 KeV to 1.5 MeV (i.e. a 100:1 range) and should give 10 measurement points (channels) within the FWHM of a peak. Each channel therefore corresponds to a 200 eV energy increment and 7,500 channels are required to cover the entire energy range. While we may be rather generous in requiring 10 points in a peak, we must note that the resolution capability at low energies improves to about 1 KeV (FWHM) giving only 5 points on low energy peaks. Moreover, interest in γ-ray spectroscopy up to about 10 MeV is increasing, and as the energy resolution due to statistical processes in the detector* increases only as $\sqrt{\text{Energy}}$, the channel requirements are even more stringent.

*Other effects such as trapping, baseline fluctuation at high counting rates, etc. often mask the detector statistics, but there can be no doubt that detector statistics will become the major limitation in the 1 to 10 MeV range in the near future

b) Nuclear reaction measurements in the 50 MeV range can now be performed with an energy resolution (FWHM) of about 0.05% using silicon detectors. If the criteria of 10 points per peak is applied to this situation and if the entire energy range is to be covered, 20,000 channels would be required. Fortunately, it is rarely necessary to cover more than a fraction of the full energy range, so that 5,000 - 10,000 channels seems to represent a reasonable objective for these applications at this time.

These requirements are difficult to meet, due in part to the high cost of adequate memory systems but due also to the problem of designing sufficently fast and accurate analogue-digital converters. The memory problem may be solved in the future by cheaper forms of mass storage or by the use of associative memory techniques;[2] at present, magnetic-tape recording provides an interim rate-limited answer to the storage problem. This paper deals with the second problem, that of designing an analogue-digital converter capable of digitizing signals with 12-bit accuracy in a very short time (~ 25 μsec)--a performance adequate for all practical requirements at the present time.

CHOICE OF METHOD

General purpose analogue-digital converters, such as those used in digital voltmeters, have always been quite different in principle of operation from those employed in pulse-height analyzers. The method most commonly used in general measurement is the "Successive Binary Approximation" technique while that used in pulse-height analyzers is termed a "rundown" technique (first proposed by Wilkinson [3]). In the binary approximation scheme, the input voltage level is compared with an analogue voltage developed by a digital-analogue converter driven by a binary register until the best match is found between the two voltages. Bits in the binary register are set in sequence starting with the most significant, a comparison is made after the setting of each bit, and the bit is reset if the stretched input level is smaller than the analogue output of the register. Rundown methods, on the other hand, generally require charging a memory capacitor to the signal amplitude, then discharging the capacitor linearly back to zero level. Accurate measurement of the rundown time, using a clock-pulse generator which feeds a scaler, results in a final number stored in the scaler which is proportional to signal amplitude.

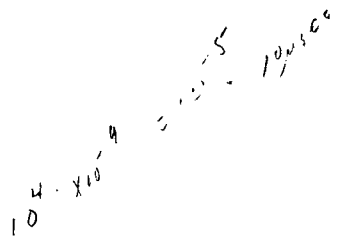
The reason for the difference in philosophy lies in the dominant importance of differential accuracy in pulse-height analysis compared with the need for integral accuracy in other types of measurement. In pulse-height analysis, unlike most applications of analogue-to-digital converters, we are measuring a statistical distribution of pulses by counting the number that falls in each digital increment or "channel" of the digitizer. This implies that the width of all increments or channels must be equal, so that a simple relationship shall exist between the number of counts per channel and the pulse-height distribution. The special problems of pulse-height analysis may be illustrated by considering an digital voltmeter producing a 10-bit (i.e. 1024_{10}) code with a full scale range of 10.24 volts. If a voltage of precisely 10.00 is fed into a typical digital voltmeter with this specification, we might expect the output reading to be in the range 9.99 to 10.01 (i.e. $\pm 0.10\%$ integral accuracy). If the input voltage were

changed to 10.01 volts we would be satisfied if the output reading were in the range 10.00 to 10.02. Therefore, we would accept a situation where no change in the output reading occured for the .01 V input change from 10 to 10.01 volts. In the case of a pulse-height analyzer, however, this situation would be completely intolerable. If a 10.00 volt pulse is fed into a pulse-height analyzer we can well tolerate a reading error greater than 0.1% but, if the input pulse amplitude is increased slowly and the absolute input pulse amplitudes at which the output code changes are noted (a_1, a_2, a_3, a_4---), we require the differences ($a_2 - a_1$), ($a_3 - a_2$), etc. to be equal to better than 1%. Hence, we see that the differences are the important parameters.

In practice it is easier to achieve the required differential accuracy using the rundown rather than the binary approximation method. We will discuss the problems of the latter method in the next section but, for the moment, will cite these problems as the major reason for the almost universal use of rundown methods in pulse-height analysis. Over and above these rather fundamental problems in the binary approximation method, elaborate circuits are needed. Before the advent of integrated circuits, a binary approximation ADC was a complex and expensive instrument. Integrated circuits alter this picture and were one factor in our re-examination of the method for pulse-height analysis.

The major reason for using a successive binary approximation method relates to the coding time in the two systems. In each case, the coding process requires a decision or series of decisions as to the equality or otherwise of two voltage (or current) levels. In the rundown method, the time required to make the decision determines the maximum clock rate which can be used. In recent ADC's [4,5] clock rates of 50 and 100 MHz have been achieved, implying a decision time as short as 10 ns. A much greater time per decision is needed for the binary-approximation method, since large level changes can occur immediately before the decision is to be made, whereas the approach to equality of the two levels is gradual in the rundown method. However, for 12-bit approximation method, we need only 12

decisions, and even if we assume a 50 ns time constant T, and allow a settling time of 10T, we still require only 0.5 μs per decision. For 1,000 (10-bit) or more channels, the speed advantage is clearly on the side of the binary step method. We have used a 2 μs decision time, allowing for the use of very slow circuitry, and even here the encoding time for 4,000 channels is only 24 μs compared to 40 μs for a 100 MHz rundown converter. The ratio becomes more impressive if a shorter decision time is used for the binary method -- or if we consider more than 4096 channels. For 2^{13} or 2^{14} channels, the factor is respectively 2 and 4 times better. Moreover, the high clock rates still represent major problems even at the present state of the electronics art, while the numbers quoted here for the binary approximation method are very conservative and can readily be improved by a significant factor.



THE SUCCESSIVE BINARY APPROXIMATION METHOD

The operation of a binary approximation type of coder is best illustrated by considering Fig. 1. The basic 12-bit coder, which we will deal with first, is shown to the left of the dotted line dividing this diagram. The basic code output to a computer or memory (to select the storage address in the pulse-height analysis mode of operation) could be obtained from the 12 output lines of the 12-bit data register. The overall sequence of operations following arrival of an input signal consists of a coding period, during which the coder generates a 12-bit code in the data register (the numerical value of the code being proportional to the signal amplitude), then a storage cycle in the memory (or computer) during which it reads and stores the data from the data register. During this whole sequence of operations, further signals are prevented from entering the system.

In more detail, the positive input signal is stretched by a signal stretcher causing a steady current $I_s = \frac{V_s}{R_s}$ to flow into the input terminal of a comparator. The comparator is a high gain amplifier which drives its output to saturation in one direction or the other when its input terminal deviates very slightly from zero. The stretcher stores the peak amplitude of the input signal, and immediately after the peak, produces a start pulse for coding operations. The timing sequence of the coding process is dictated by the control circuits -- the first action of which is to close the input gate to the signal stretcher -- keeping it closed until coding and storage operations are complete.

In addition to being driven in a positive direction by the signal current in R_s, the input terminal of the comparator is driven in a negative direction by the current from an accurate digital-analogue converter driven by the data register. The object of the encoding sequence is to store in the data register the number which most accurately makes the net current into the comparator equal to zero. It will be clear that this requires that

The maximum current in the D-A line to the comparator be equal to the maximum current in R_s. i.e. $\frac{V_s\ (max)}{R_s} = \frac{V_{ref}.2^{12}}{R}$

$$\text{OR} \qquad R_s = \frac{V_s\ (max)}{V_{ref}} \cdot \frac{R}{2^{12}}$$

To achieve the balance in minimum time, the data register is initially set with only bit 11 in the "1" condition. The current I is then equal to $V_{ref}.2^{11}$ or half its maximum value. The comparator output is examined; if this indicates $I_s > I^*$, bit 11 of the data register remains set; if $I_s < I$, bit 11 is reset. The same operations are now carried out on bit 10 and the remaining bits of the data register in succession.

A shift register is used to control the location in the data register to be operated upon in a given cycle. In our case this is advanced every 2 μsec and the inspection of the comparator output is carried out about 1.5 μsec after each step of the register. When the shift register steps, the n^{th} flip-flop being reset generates a pulse which

i) sets the next (i.e. n+1) binary in the shift register

ii) sets the following (i.e. n+1) bit in the data register

iii) resets the n^{th} bit in the data register unless the comparator output inhibits this reset.

The complete code is thereby produced in the data register about 24 μsec after the start of the input signal.

We have seen that the differential accuracy requirements are the major problem in applying this well known scheme to pulse height analysis. The difficulties center on the accuracy of the D-A converter

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* We assume at this stage that $I_G = 0$

and are particularly apparent for input signal levels close to those where the D-A converter current flows for the most part in only one of its resistors. To illustrate the problem we will consider the effect of slowly increasing the input signal amplitude and noting the precise amplitudes at which the output code changes from 2047 to 2048, then to 2049 ($2^{11} = 2048$). When the output code is 2047 the signal current I_s is being balanced by D-A current I supplied by resistors R10, R9, R8 --- R1 in parallel. As the number changes to 2048 all the D-A current flows in R11. When it becomes 2049, R11 and R0 supply the current I. If we represent the change in input current I_s to change the output code from just n to just m by $\Delta I_s\ (n \rightarrow m)$ we have:

$$\therefore \Delta I_s\ (2047 \rightarrow 2048) = V_{ref} \left\{ \frac{1}{R11} - \left(\frac{1}{R10} + \frac{1}{R9} + \frac{1}{R8} \text{---} + \frac{1}{R0} \right) \right\}$$

$$\therefore \Delta I_s\ (2048 \rightarrow 2049) = V_{ref} \left\{ \frac{1}{R11} + \frac{1}{R0} - \frac{1}{R11} \right\} = \frac{V_{ref}}{R0}$$

$$\frac{\Delta I_s\ (2047 \rightarrow 2048)}{\Delta I_s\ (2048 \rightarrow 2049)} = R0 \left\{ \frac{1}{R11} - \left(\frac{1}{R10} + \frac{1}{R9} + \frac{1}{R8} + \text{---} \frac{1}{R0} \right) \right\}$$

By design we choose $R_{11} = \frac{R0}{2^{11}} = \frac{R0}{2048} = \frac{R}{2048}$

and $$\left\{ \frac{1}{R10} + \frac{1}{R4} + \text{---} \frac{1}{R1} + \frac{1}{R0} \right\} = \frac{2047}{R}$$

and therefore make the design value of $\frac{\Delta I_s\ (2047 \rightarrow 2048)}{\Delta I_s\ (2048 \rightarrow 2049)} = 1$

However, the design values of the resistors in the ADC are subject to manufacturing tolerances and these tolerances tend to make the two channels unequal. For example, we might assume $\pm$ .01% tolerance in the resistors and examine a worst case, situation:

$$\left\{ \frac{1}{R10} + \frac{1}{R9} + \frac{1}{R8} + \text{---} \frac{1}{R1} + \frac{1}{R0} \right\} = \frac{2047}{R} + .01\% = \frac{2047.2}{R}$$

and

$$\frac{1}{R11} = \frac{2048}{R} - .01\% = \frac{2047.8}{R}$$

In this case; $\Delta I_s\ (2047 \rightarrow 2048) = \frac{0.6}{R}$

while $\Delta I_s\ (2048 \rightarrow 2049) = \frac{1}{R}$

Therefore the channel 2047 → 2048 is 40% smaller than the following one. This is an intolerable situation and illustrates the problem of achieving 1% differential accuracy (i.e. 1% equality of channel widths) in this type of ADC. Similar but smaller problems occur at channels 1023-1024, 511-512, etc., the problem becoming smaller by factors of two for each step in the series.

We must also note the effect of differences in voltage drop in the diodes CR11 - CR0 in Fig. 1. These drops reduce the effective value of Vref and differences between the diode voltage drops produce the same effect as resistor tolerances in R11-R1. In this unit Vref = -16V and the critical diodes are matched to 1mV, so the effect of diode variations is expected to be somewhate smaller than that due to .01% resistors (the tolerance of resistors in the D-A converter is .01%, but they are purchased in sets matched to .005%).

Two measures are employed in the unit to achieve the better than 1% channel equality required in pulse-height analysis. The first of these is to use good circuit practice to minimize the error due to resistor and diode tolerances. Figure 2 shows the actual circuit used for the most significant bits of the D-A converter. The four most significant sections are arranged so that all resistors are equal and so are diode and resistor currents. Moreover, the diodes and resistors in the second section can relatively easily be selected to lie in the middle range of the one used in the first section, etc. This effectively reduces the problem of resistor and diode tolerances, and channel width errors of less than 10% are normally observed if this is the only remedy used.

The second technique employed is due to Gatti [1]. This results in the additional elements shown to the right of the dotted line in Fig. 1. A 6-bit scaler is driven by a gated pulser which steps the scaler regularly except that it is frozen during the coding process by a waveform produced by control circuits. The scaler drives a 6-bit D-A converter which produces a third current at the input to the comparator. The coding operation still works to make the total current at the input of the comparator equal to zero (i.e. $I + I_g + I_s = 0$). It is easy to see that this results in the data register containing a number N smaller than it would have done in the absence of the additional current Ig (where N is the number which happens to be in the 6-bit scaler at this time). Fixed amplitude input pulses therefore result in output codes from the data register which fluctuate over a range of 64 values depending on the random number in the 6-bit register. By digitally adding the contents of the 6-bit register to those of the data register in a 12-bit adder, the correct code is obtained at the final output wires. However, the interesting consequence of this system, is that the main 12-bit D-A converter has been caused to work at different positions for the fixed amplitude input pulses. This has the effect of averaging the previously discussed error due to resistors and diodes over 64 channels -- thereby easily achieving the required 1% channel equality.

In practice two modifications to this method have proved to be necessary. To avoid problems at very low amplitudes, a pedestal equal to 64 channels (i.e. 128mV in our case) is developed in the stretcher. The data register then contains a minimum of zero at the end of the coding process. The output adder is modified to digitally subtract 64 to correct for the presence of the pedestal. (i.e. output code = 0 for signal = 0). We should note also that the top 64 channels of the analyzer contain only overflow pulses due to the operation of this system, but this is of little consequence in the total of 4096 channels.

In addition to the effect of resistor and diode tolerance in the D-A converter, we also note that any droop on the stretcher output produces another source of channel inequality (although this would be averaged out by a Gatti scheme employing only a single bit). The effect of stretcher droop is illustrated in Fig. 3. The error occurs due to the time difference between setting the most and least significant bits into the data register. We see from Fig. 3 that a droop in the top of the signal of 1/2 a channel results in channel 2047 having about half the width of a normal channel while 2048 is 50% greater than a normal channel. To reduce this effect the stretcher is designed to produce very little droop at its output -- in our case the droop in the 24 μsec coding time is only about 100 μV or 1/20th of a channel. The stretcher will be described in some detail in a later section. Two minor side effects of the random pedestal technique are discussed below*.

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* SECONDARY EFFECTS OF GATTI SCHEME ON ADC PERFORMANCE

I. Small systematic errors are possible. If one channel without the random pedestal was 32% too wide or narrow, then the random pedestal of 64 channels would make the 64 adjacent lower channels all count at an average rate of 0.5% too high or low respectively. Thus an error of 0.25% in background subtraction; or 0.5% in relative counting rate could result.

II. The statistical distribution of counts per channel should show a larger deviation due to the random probabilities that a particular wide or narrow step in the ADC will contribute more of fewer count to each of the 64 memory channels which it affects because the random pedestal is used.

However, any one step will contribute an average of only 1.6% to the counts in each of 64 channels and only this part is subject to additional randomness.

Statistical fluctuations were measured using an input spectrum of 10^4 counts per channel derived by sampling a sawtooth waveform at random times. The distribution of counts per channel about the mean showed slightly less randomness than would be expected from a Poisson distribution.

OVERALL SYSTEM

The ADC was developed for use in a variety of data-taking systems. These include computer-controlled as well as more conventional nuclear spectroscopy systems. A typical system is shown in Fig. 4.

The analog input part of the unit includes a pulse stretcher (accepting a maximum of +8V input signal), low level discriminator, variable down to 25 mV, and an input linear gate. This "front end" section of an ADC determines input signal requirements and can have important effects on the high counting-rate performance of a system. The circuit is built on a single plug-in card which can be replaced for special applications, or for compatibility with future improved amplifiers.

The main part of the ADC which performs the coding operation was described in the previous section. This feeds the digital output part of the unit which was designed to ensure ease of connection to various types of memories and computers. The 12-bit output code is held in a register whose outputs can be gated by an external data request signal. (Note: If the external signal is not connected, the output gates remain open at all times.) An additional (gated) 10-bit register can be loaded along with each input pulse from external "routing" or "label" signals. Provision is made to allow selection by the experimenter of a total of 17 bits to be presented to the computer or memory from these two registers, by use of a prewired

"program plug". This feature is invaluable in multiparameter experiments, as it allows a "label" code to be attached to each pulse-amplitude code. The routing register can also be incremented in steps; if the "add-1" signal is a clock pulse, the label code can represent a time delay after an initial event. The output signals from both registers are taken through a single buffer card which can be matched to the voltage level requirements of particular storage and computer systems.

A signal and echo system is used for communication between the ADC and the memory. A "data-ready" signal is generated by the ADC when a signal has been encoded, and a "code-accepted" pulse is fed back by the memory system when it has accepted the code. An "ADC-busy" signal is also available for use by any associated equipment. The ADC circuitry includes provision for "live-time" determined experiments. An externally supplied clock signal is gated by the linear gate control signal, producing a channel-zero code at the ADC output whenever a clock pulse is accepted. The number of counts in channel zero, divided by the clock-pulse rate, provides a precise measure of the time that pulses were being accepted by the ADC, corrected for system dead-time. In a typical application using a PDP-7 computer, and additional provision is made to use the first two words (18-bits each) for storage of clock pulses.

The ADC was designed to operate as a self-contained unit, with all necessary power supplies. In order to facilitate off-line testing, and avoid possible error lockup condition, the digital circuits are arranged to reset automatically after about 1ms if the data-ready signal is not recognized by the external memory.

The unit performs its single function of pulse-height conversion as unobtrusively as possible. The only controls available to the operator are a power switch, a switch to enable an external gate, and a switch to disable the "data-ready" signal. During operation of a spectroscopy system, control of data taking will normally be associated with the memory system. The program plug provides the main flexibility of the ADC. It determines which signal shall be fed to the memory, and also the mode of operation of the routing register. Using several different prewired program plugs, a number of radically different data taking systems can readily be prepared. A vital feature of the ADC is the provision of front panel electrical test-points connected to all input-output signals of the unit and to a number of the intermediate points within the ADC. The use of these test-points, placed on a front panel signal-flow diagram, is of great value when setting up a new experiment of system, or when testing for suspected malfunction or improper connections in the system.

MEASURED PERFORMANCE

Six of these ADC's have been used for several months in nuclear spectroscopy experiments controlled by PDP-5 and PDP-7 computers.

Electronic tests show that:

(i) Drift is no more than one channel over an eight hour period.

(ii) Count rate shift is less than 5 channels (0.12% full scale) as the count rate changes from 200 Hz to 20 KHz using 1 μs flat-topped pulses. This is independent of amplitude.

(iii) The counting rate is equal to within $\pm$ 1% for all channels above channel 60 when the ADC is fed with a source of randomly distributed pulses from an electronic sweeping pulser. This is a measure of differential linearity (differential channel width).

(iv) A change in temperature of 20°C produces a drift of less than 1 channel in 4000.

(v) 95% of all counts fall in a single channel with randomly timed single amplitude pulses at an average rate of 1 KHz. At 100 KHz 90% of the counts fall in two adjacent channels, indicating excellent high rate resolution.

CIRCUIT DETAILS

Digital circuits required to carry out the encoding process described in Sections 3 and 4 have been implemented with RTL micrologic gates and flip-flops. They are quite conventional and will not be described in detail here.

Two circuit elements justify more detailed description. These are the signal stretcher and the comparator. We have already mentioned the importance of keeping the droop on the top of the stretcher pulse to a very small amount and this presents the first challenge in the design of the stretcher. We also require that the output code from the ADC be practically independent of the signal counting rate. This results in the use of dc coupling from the input of the stretcher to the comparator. Consequently dc drifts in the elements of the stretcher become important and a servo loop is included in the comparator to correct the effect of these drifts. Before proceeding to describe the circuits, it is well to recollect that a single channel in the 4096 channel ADC corresponds to 2 mV and we aim for a precision in our measurements much better than this.

a) Signal Stretcher (see Fig. 5)

The positive signal enters this unit via an ac coupling with dc restoration diode returned to an adjustable level control. This is adjusted so that the stretcher output is close to zero. We note that the diode and transistor base-emitter drops are balanced in the signal path (Q1-CR8; Q2-CR1; Q3-Q8) right to the output of the stretcher, thereby minimizing the effect of temperature on the dc level at the output of the unit. The measured temperature coefficient of the output level of a typical unit is less than 500 μV/°C.

The input gate is normally open so the signal appears on the anode of diode CR1 and on the input of the low-level discriminator. If a signal is already being processed by the ADC the gate control circuit holds the input gate in its closed position thereby preventing any signal from passing through the gate. Furthermore, circuits are included in the gate control circuit to prevent the input gate being opened when a signal is present at its input. This eliminates the possibility of partial pulses being processed by the ADC.

The signal stretching function is carried out in the feedback stretcher consisting of transistors Q3, 5 (a field-effect transistor), 6, 7, diodes CR2, 3 and memory capacitor C1. Q3, 5 act as a difference amplifier, amplifying the difference in voltage between the input signal, which appears at the base of Q3 via the diode CR1, and the voltage across the memory capacitor (the time constant R4C1 is small so the previous statement is true on the time scale of interest in this general discussion). If the base of Q3 suddenly rises above its equilibrium value, the current in Q3

increases, driving Q6 into heavier current and causing C1 to charge via CR2. On the other hand, a sudden fall in voltage at the base of Q3 cannot be followed quickly by the voltage across C1 since diode CR2 tends to become non-conducting.

In the equilibrium state of this circuit:

i) the bases of Q6 and 7 are at +12V

ii) Q3 passes 0.5 mA

iii) Q4 is a constant current tail for the difference amplifier and is passing 4.5 mA, so the FET Q5 passes 4mA.

iv) CR3 is conducting a current of 2 mA (discharge current) supplied by the low-level discriminator. Therefore CR2 is also passing 2 mA.

v) Q6 is passing 4 mA so Q7 is passing 2 mA.

Appearance of a positive signal pulse at the anode of CR1 causes the low-level discriminator to trip (trip-level about 25mV) removing the 2 mA from CR3 and causing CR4 to pass about 100uA, thereby locking the anode of CR4 and cathode of CR3 to the base waveform on Q3. This base is driven positive by the signal via CR1 and the feedback stretcher causes the voltage on the gate of Q5 to follow the signal as long as it moves in a positive direction. We note that the current in Q7 during this phase is 4 mA; this is insufficient to trigger the signal peak discriminator so no waveform occurs on the lower end of R2 or R3. We also note that the source of the FET follows its gate potential and drives the White emitter-follower so that the signal output, feedback clamp and bootstrap lines all follow the

signal during this stage of the sequence. To a close approximation this means that the drain of the FET and the anodes of CR5, 6 follow the signal thereby maintaining the bias across these elements at the same value as in the quiescent condition.

On the back edge of the signal, the anode of CR1 falls, the base of Q3 falls until CR5 conducts (i.e. a fall of about 1V), Q6 becomes nonconducting and its collector falls until CR6 conducts (i.e. a fall of about 1.5V). CR2 is now nonconducting and since CR3 is also nonconducting (the low-level discriminator holds over until reset by the control circuit in the ADC), the capacitor C1 remains charged to the value it assumed at the peak of the input signal. The current in Q6 is now very small or zero and the current in Q7 becomes large enough to trigger the signal peak discriminator which develops a positive 128mV pedestal across R4 and hence, via the memory capacitor C1, at the gate of Q5. This produces a pedestal in the output signal but, in addition, ensures that Q3 is completely nonconducting for the remainder of the processing cycle.

Several aspects of the circuit which influence its performance will now be discussed:

i) The clamping effect of CR5 and CR6 on the back edge of the signal prevents any significant capacitive feedthrough effects which might otherwise occur on the back-edge of large input signals.

ii) The quality of the capacitor C1 is important in this application. Dielectric charge storage effects may produce an unwanted transient decay on the top of the stretched pulse; to avoid this we use a polystyrene capacitor.

iii) Leakage in diodes CR2, CR3 causes a droop on the top of the pulse. In some applications this may represent a serious problem and consequently special care is required in the choice of type for these diodes. We have found that the base emitter diodes of 2N709 transistors serve very well here, with leakage less than 10^{-9} A at 1V reverse bias at room temperature.

iv) To avoid further loading (and consequent droop) across the memory capacitor, the output from the stretcher is taken from the source of Q5 which therefore acts as a source follower of the voltage across C1. In order to maintain the gate to source voltage at the same value as it was before the entry of a signal into the system, we arrange that the FET's drain-source voltage and its source current are the same following the signal peak as they were in the quiscent condition. This is achieved by deriving the drain voltage from the "bootstrap" line and by reducing the current in Q4 after the signal peak by an amount equal to the quiescent current in Q3. This is achieved by changing the voltage across R2 by use of the peak discriminator waveform.

v) The dc connection from the input to the gate through to final output results in excellent performance even at very high duty factors. However, a sudden change in counting rate can result in a change in the output pulse-height unless account is taken of thermal effects in

certain transistors.[4] An example of this problem is the case of Q6 and Q7. During the period of the stretched pulse, the power in Q6 is zero and that in Q7 is quite large (∿ 150 mW) whereas the power was more equally balanced between the two transistors in the quiescent condition. The change in power in Q6 and Q7 would result in changes in temperature and base-emitter drops at high counting rates if normal transistors were used in these positions. To avoid this problem two transistors in a single header are used here; since the total power dissipation in Q6 and Q7 remains almost constant and the two are in good thermal contact the thermal problem is almost eliminated.

vi) The dc connection of the whole circuit and the use of clamp diodes CR5, 6 (which must be reverse biased by only a small amount in the quiescent condition of the circuit) place some restrictions of the acceptable characterstics of the FET Q5. To ensure satisfactory operation of the circuit we require that the gate=source voltage shall be -1 $\pm$0.5V for 4mA source current. Several commercial units easily meet this requirement in practice, but, as the limits are tighter than specified by the manufacturer, some selection is necessary.

When the main ADC has finished its coding operation, the low-level discriminator is reset, causing the discharge current in CR3 to discharge C1 back to its quiescent state. However, the input gate remains closed until the memory or computer to which the ADC is attached has accepted the data; it then opens and further signals can be processed.

b) Comparator Servo Loop (see Fig. 6)

The principal element in the comparator is a high gain dc amplifier consisting of two inverting operational amplifiers, each with diode limiting in both directions shunting the feedback resistors. During most of the coding process the amplifiers are saturated in one direction or the other and prompt recovery from this situation with no significant voltage movement at the input to the comparator is a necessary performance requirement. The signal enters the comparator from the stretcher via a 562Ω resistor (R1) so that each channel (i.e. a signal change of 2mV) corresponds to a 3μA change through R1 and, following the gain of the amplifier, a 375mV change at the base of Q1.

The purpose of the comparator is to allow detection of departure from equality of the sum of signal current and that from the D-A converter connected to the data register. Equality is signified by a net current of zero at the input to the comparator, and consequently zero output at the base of Q1. If the D-A converter current is smaller than the signal current in R1, the base of Q1 will be at a positive potential and conversely. When the strobe pulse is applied to the base of Q3, the common emitter current of Q1, 2, 3 flows either in Q2 or Q1 depending upon the poloraity of the base of Q1. Therefore, if the D-A converter current is too small, Q2 conducts at the strobe time, triggering the one-shot and thereby inhibiting the reset waveform to the most recently set bit position in the data register.

The operation is complicated by the possibility of zero offset in the signal which is unavoidable in the dc coupled stretcher circuit. To correct for this offset, the slow servo loop shown in Fig. 6 feeds current in resistor R8 to maintain the quiescent

net current into the input of the comparator amplifier at zero. The servo action is inhibited whenever a signal is being processed by the ADC, by applying the signal gate waveform to the base of Q5. The gain of the servo loop is sufficient to correct normal zero offset in the stretcher even when the servo is activiated only for much less than 25% of the total time (i.e. for a duty factor of > 75% in the ADC).

ACKNOWLEDGEMENTS

H. Cingolini assisted in the early stages of design of this unit and D. Landis, J. Meng and D. Schurr have all contributed ideas and time to the project. M. Brown originally carried out the measurements which showed that small wirewound resistors adequate for the D-A converter were now commercially available. The work was performed as part of the Nuclear Chemistry Electronics Program under AEC contract W-7405-eng-48.

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LIST OF FIGURES

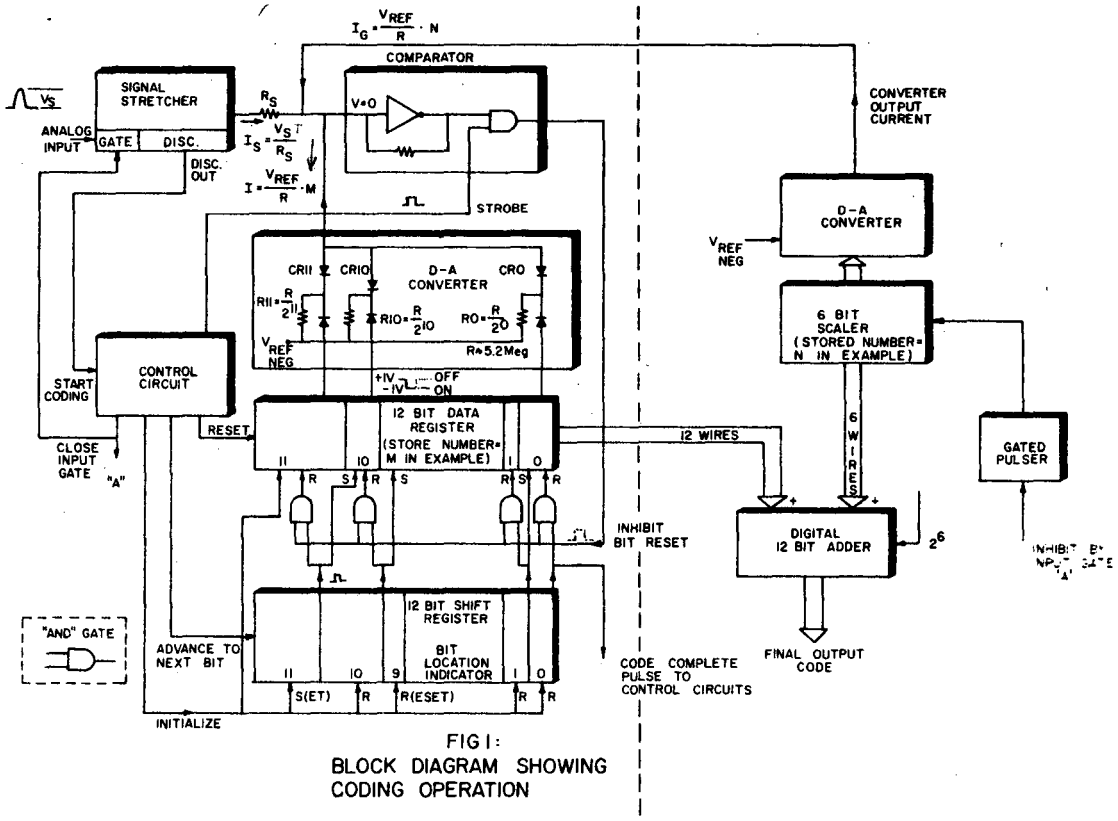

FIG I:
BLOCK DIAGRAM SHOWING
CODING OPERATION

XBL 682-111

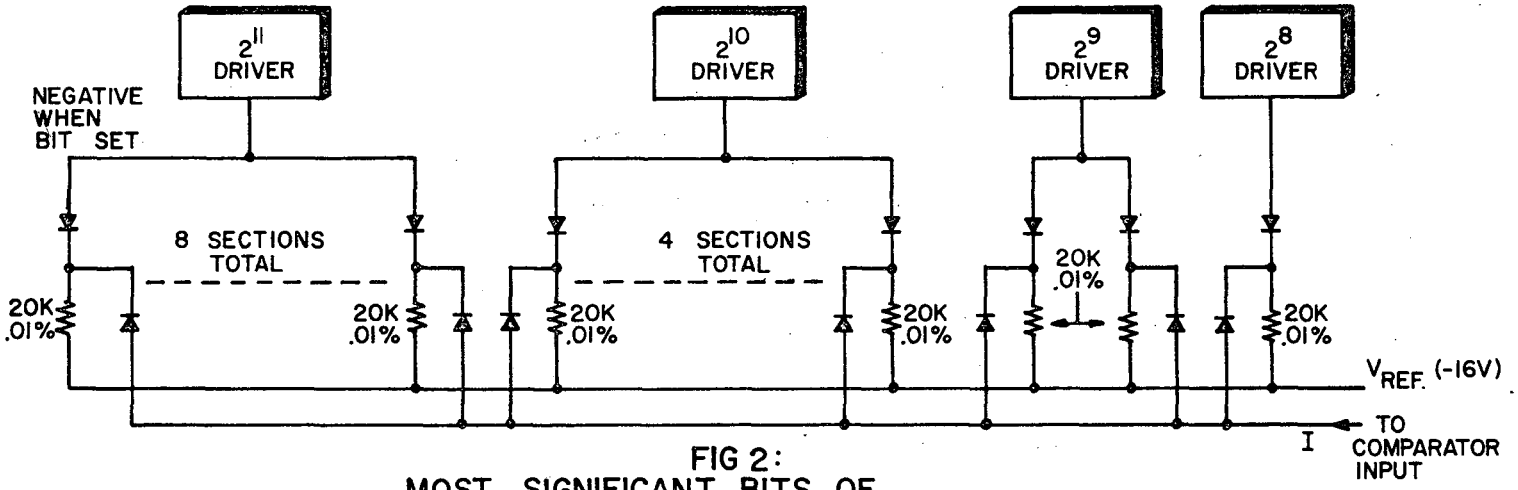

FIG 2:
MOST SIGNIFICANT BITS OF
12 BIT D-A CONVERTER

XBL 682-109

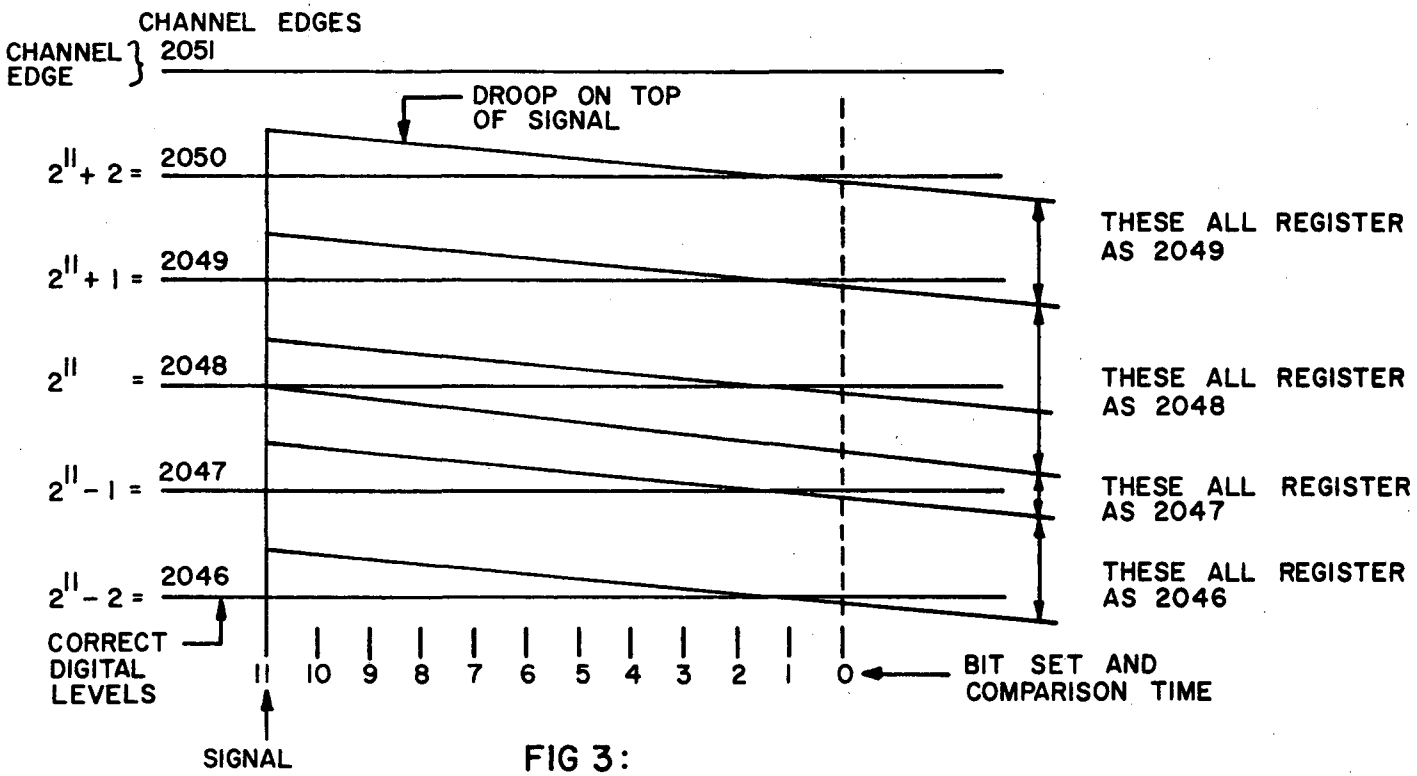

FIG 3:
THE EFFECT OF STRETCHER DROOP

XBL 682-110

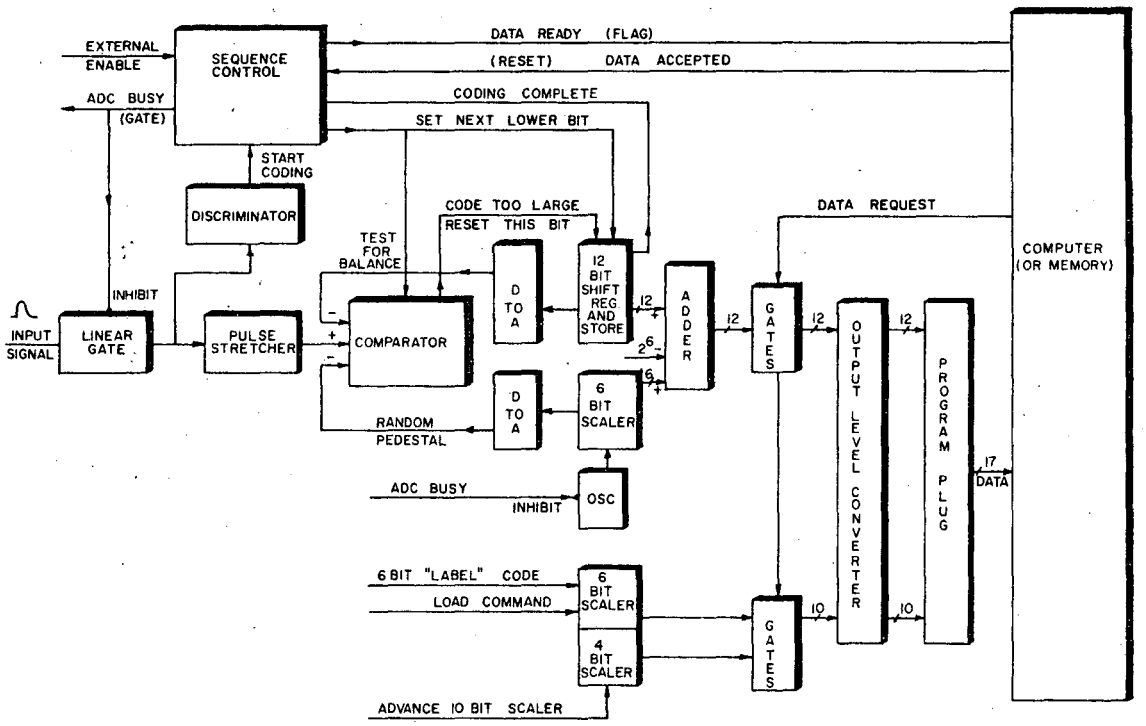

FIG 4:
ADC TO COMPUTER CONNECTIONS

XBL 682-112

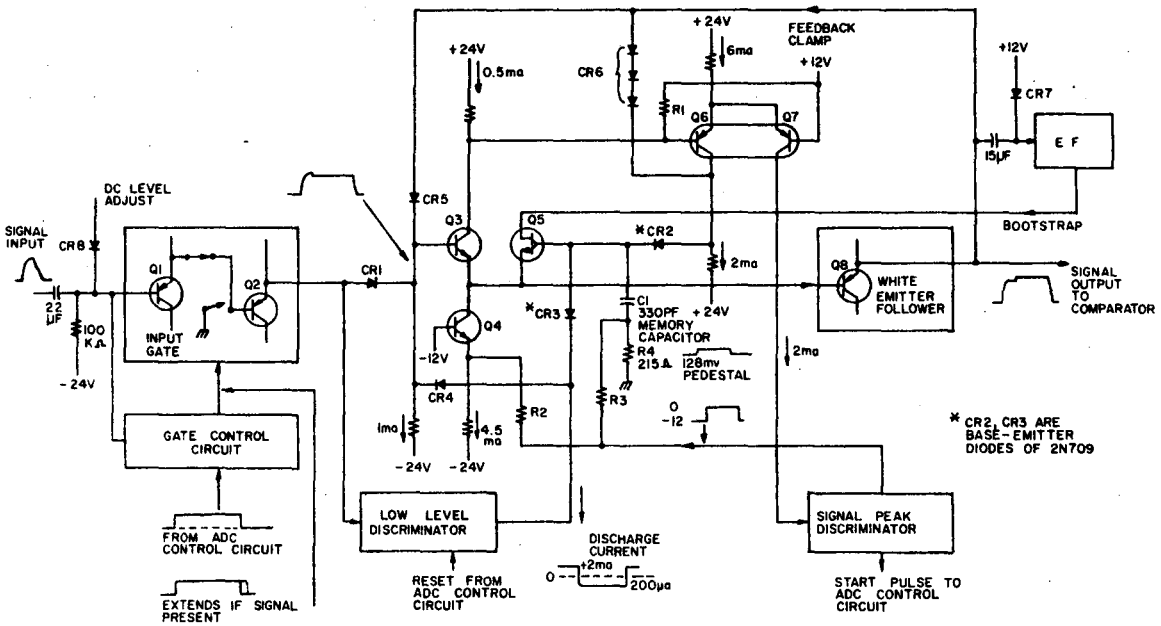

FIG 5:
SCHEMATIC OF SIGNAL STRETCHER

XBL 682-113

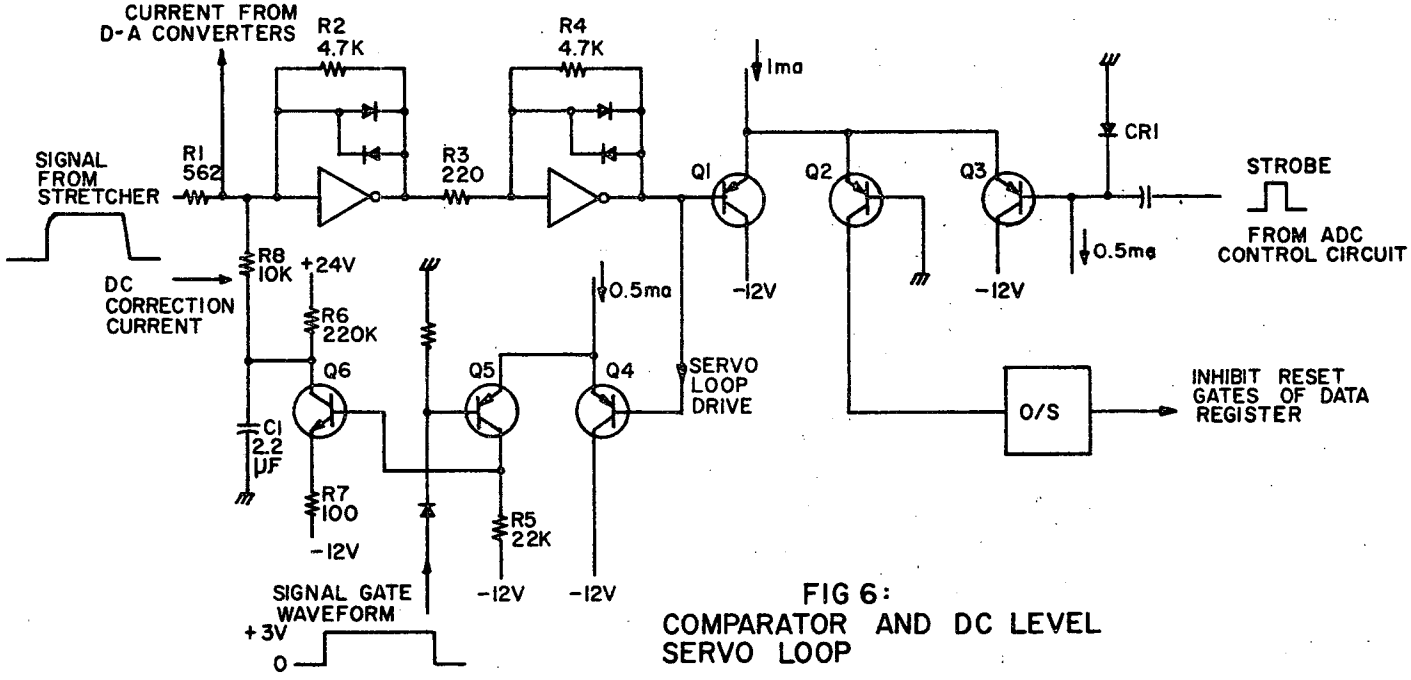

FIG 6:
COMPARATOR AND DC LEVEL SERVO LOOP

XBL 662-108