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Design of A 0-3Ghz Spectrum Scanner Using Sampled Linear and Periodically Time Varying Circuit



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# Design of A 0-3GHz Spectrum Scanner Using Sampled Linear and Periodically Time Varying Circuit

A thesis submitted in partial satisfaction

of the requirements for the degree of

Master of Science in Electrical and Computer Engineering

by

Jiyue Yang

2018

ABSTRACT OF THE THESIS

# Design of A 0-3GHz Passive Spectrum Scanner Using Sampled Linear and Periodically Time Varying Circuit

by

Jiyue Yang,

Master of Science in Electrical and Computer Engineering

University of California, Los Angeles, 2018

Professor Sudhakar Pamarti, Chair

As the number of wireless network users increases in the modern communication systems, cognitive radio becomes an attractive solution to the crowded communication spectrum. A key technology that enables the application of cognitive radio is the circuit that can sense the available spectrum for communication, as known as: Spectrum Scanner. Previous work has demonstrated a passive spectrum scanner using the sampled LPTV RC circuit that achieves 0-1Ghz scanning range and 40dB stopband attenuation. However, the parasitic capacitors in the resistor DAC limits the stop band attenuation from 60dB to 40dB. Chapter 1 and 2 will provide the background of sampled LPTV RC filter as a spectrum scanner. Chapter 3 will provide the analysis of parasitic capacitor's effect on filter's frequency response and a RDAC switching technique as a solution. Chapter 4 and 5 present the circuit design of a 0-3Ghz spectrum scanner using return-to-infinity RDAC to remove parasitic capacitor's influence on filter's stopband attenuation.

The thesis of Jiyue Yang is approved.

Chih-Kong Ken Yang

Danijela Cabric

Sudhakar Pamarti, Committee Chair

University of California, Los Angeles

2018

To My Parents for Their Love and Support.

# Table of Contents

# List of Tables

# List of Figures

# Acknowledgements

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# Chapter 1

## Introduction to Spectrum Sensing

As the number of wireless network users increases in the modern communication systems, cognitive radio becomes a popular solution to the crowded communication spectrum. The idea of the cognitive radio is to dynamically search for empty communication channels and allocate them to the users, therefore increasing the capability of the current communication system. One necessary technology that supports the cognitive radio is to sense the available spectrum over time, called spectrum sensing. The spectrum scanner sweeps through a wide range of potential frequency channels and sense the strength of the signals in those channels. The information of the spectrum availability is then passed to the cognitive engine. The cognitive engine decides the usage of the spectrum and coordinate with users' devices.

The work from this thesis introduces the design of a previously proposed passive spectrum scanner using LPTV RC circuit. The spectrum scanner implemented in [] suffered from degraded stopband attenuation because of the parasitic capacitance within the RDAC. This work uses a RDAC switching technique that improves the stopband attenuation by 20dB. The organization of the thesis is such that chapter 1 introduces the background of spectrum sensing, chapter 2 introduces using

LPTV RC circuit as a spectrum scanner, chapter 3 explain a return-to-infinity RDAC switching technique to remove parasistic's influence on filter shape and chapter4,5 talks about the circuit design of the improved spectrum scanner.

## Key Requirement for a Spectrum Scanner

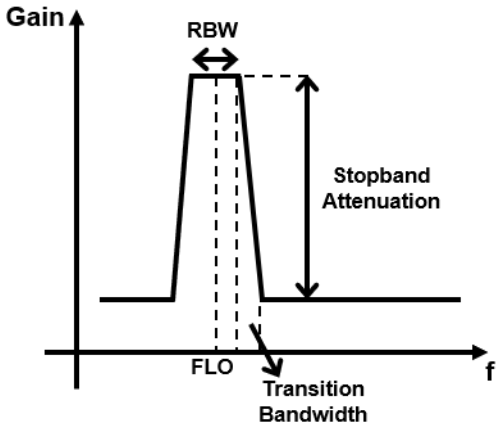



Figure 1.1: Frequency response of a bandpass filter.

- **Scanning Range, Resolution Bandwidth and Scanning Time**

  Scanning range indicates the range of frequencies that the spectrum scanner can detect. Scanning all frequencies within the scanning range is achieved by sweeping the LO's frequency of a BPF, shown in figure 1.1. And detects the energy of the BPF's output. A wide scanning range is usually preferred to cover as many spectrum as possible. Resolution bandwidth of the spectrum scanner indicates how frequency selective the filter is. Although a high selectivity is preferred to differentiate two signals with small frequency offset, a very small RBW will increase the scanning time.

- **Linearity**

  The ideal spectrum scanner is without any nonlinear distortion. However, almost all active device has limited linearity. For many commercial system such as LTE and GSM, large

blockers exist at the out of band spectrum. The third order inter-modulation nonlinearity will create unwanted signals that may fall into the passband of the scanner. This will result in false detection. Therefore, a good spectrum scanner should have a very high linearity.

- **Sensitivity**

  Sensitivity means the smallest input signal that the spectrum scanner can pick up. A high sensitivity is required for the spectrum scanner to detect the smallest signal possible. However, circuit usually adds noise to the signal. It appears as a noise floor at spectrum scanner's output.

- **Power**

  For a spectrum scanner with the application in the mobile device, the power consumption is critical because of the limited battery life. Therefore, a low power consumption is preferred.

# Chapter 2

# Prior Art: Background of the LPTV RC Filter

## 2.1 Introduction to Sampled LPTV System

A linear time varying system has a time dependent impulse response, denoted by $h(t,\tau)$. Its impulse response can be understood as applying an impulse at time t – $\tau$ and observe the output of a system at time t. Therefore, for a system given an input x(t), the output is given by the convolution integral, as shown in (2.1). For a linear and periodically time varying (LPTV) system, the time dependent impulse response becomes periodical: $h(t,\tau) = h(t + K * T_s, \tau)$

$$y(t) = \int_0^\infty x(t-\tau) \times h(t,\tau) d\tau \tag{2.1}$$

If the LPTV system's output is also sampled at the same rate, the output becomes:

$$y(nT_s) = \int_0^\infty x(nT_s-\tau) \times h(nT_s,\tau) d\tau \tag{2.2}$$

Since LPTV system's impulse response is periodical $h(t,\tau) = h(t+nT_s,\tau)$, LPTV system's impulse response becomes a function independent of $t$ if we only look at the output sample at $nT_s$. The sampled output is simplified in equation 2.3.

$$y[n] = \int_0^\infty x(nT_s - \tau) \times h(0,\tau) d\tau \tag{2.3}$$

This implies that the sampled LPTV system is equivalent to an LTI system, if only the sampled output can be observed. This property greatly simplifies the complexity in analyzing the system's response in time and frequency domain.

A sharp and passive spectrum scanner was implemented using the concept the LPTV system introduced above[2][3]. The core of the circuit is shown in the Figure 2.1 . The resistor is periodically changing and the output voltage at the capacitor is sampled at the same rate. This chapter will provide the background that is needed to understand how it achieves a sharp filter.

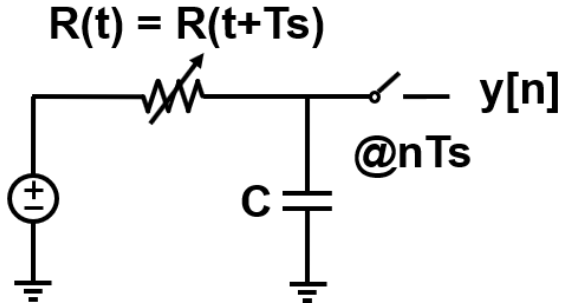



Figure 2.1: Sampled LPTV RC circuit

## 2.2 Filtering by Aliasing: An Intuitive Understanding of the Sampled LPTV RC Filter

Let $h(t,\tau)$ be the impulse response of the sampled LPTV RC circuit shown in Fig2.1 . The resistor value is periodically changing and voltage is periodically sampled at the ouptut of the capacitor. Since the impulse response $h(t,\tau)$ is a periodical function in term of $t$, it can be expanded using the Taylor Series:

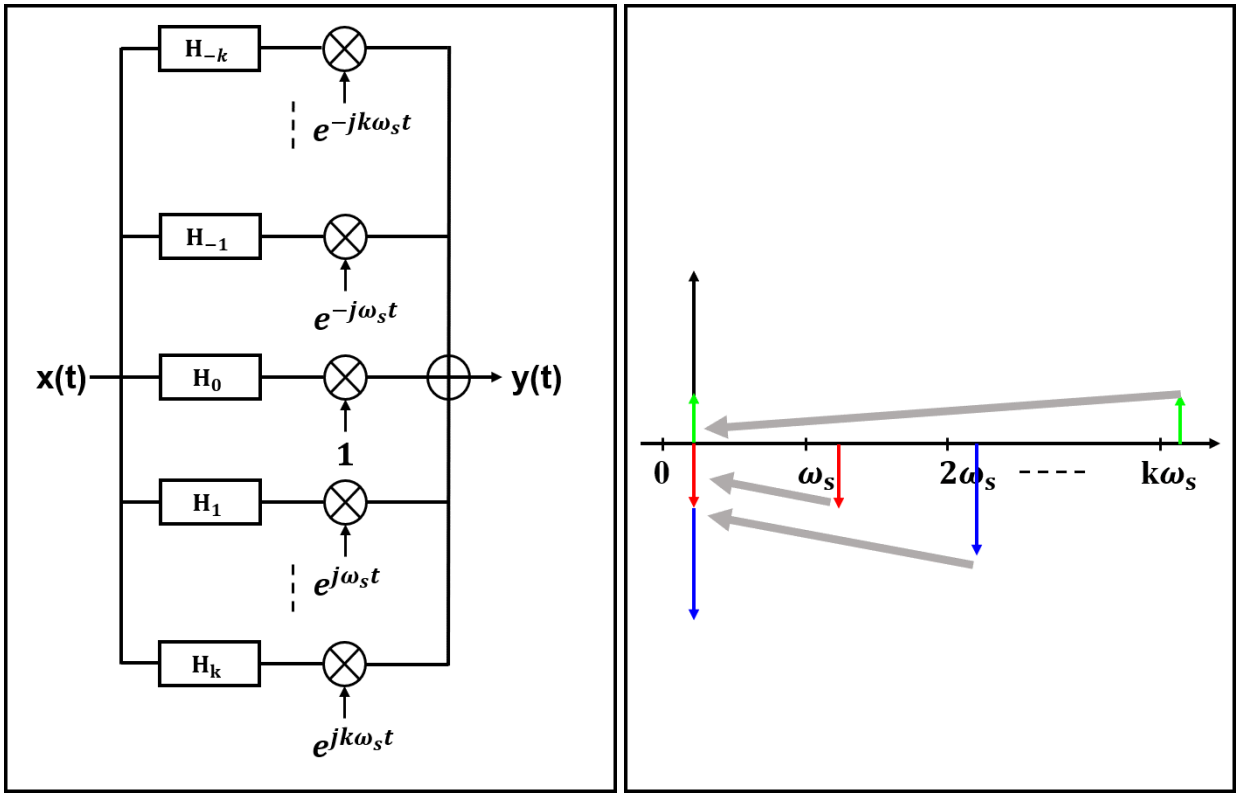
$$h(t,\tau) = \sum_{k=-\infty}^{\infty} H_k(\tau) \times e^{jk\omega_s t}, \omega_s = \frac{2\pi}{T_s} \tag{2.4}$$

If the sampled LPTV system is given a complex exponential input $e^{j\omega t}$, the output signal before it is sampled is:

$$\begin{aligned}
y(t) &= \int_0^{\infty} e^{j\omega(t-\tau)} \times h(t,\tau) d\tau \\
&= e^{j\omega t} \times \int_0^{\infty} (e^{-j\omega\tau} \times \sum_{k=-\infty}^{\infty} H_k(\tau) \times e^{jk\omega_s t}) d\tau \\
&= e^{j\omega t} \times \sum_{k=-\infty}^{\infty} e^{jk\omega_s t} (\int_0^{\infty} e^{-j\omega\tau} \times H_k(\tau) d\tau) \\
&= \sum_{k=-\infty}^{\infty} e^{j(\omega+k\omega_s)t} \times (\int_0^{\infty} e^{-j\omega\tau} \times H_k(\tau) d\tau) \\
&= \sum_{k=-\infty}^{\infty} e^{j(\omega+k\omega_s)t} \times H_k(j\omega_\tau)
\end{aligned}$$

From the derivation, we can see that an LPTV system effectively creates harmonics at the frequencies that are integer multiples of $\omega_s = \frac{2\pi}{T_s}$ away from the input frequency with different complex gains. A diagram that shows the harmonics generation is presented in the Figure 2.2a). If the output is periodically sampled at the same rate $\omega_s$, all the harmonics that are created by the LPTV system will alias back to the range $(-\frac{\omega}{2}, \frac{\omega}{2})$ at the same frequency, as shown in Figure 2.2b). By carefully designing the coefficients $H_k(j\omega_\tau)$, sharp attenuation can be achieved for unwanted signal, while

signals in the passing spectrum are preserved.




(a) (b)

Figure 2.2: a) LPTV system creates harmonics, b) Harmonics alias back to input frequency

## 2.3 Impulse Response and Frequency Response of the Sampled LPTV Spectrum Scanner

A very sharp filter is based on the concept of sampled LPTV circuit. The core of the LPTV Spectrum Scanner is shown in Figure 2.3. It consists of a periodically varying resistors, a passive mixer that allows changing the center frequency of a band pass filter, a capacitor and a periodic sampler. The Input is a voltage source with source resistance of $Rs$. The periodically varying resistor is changing to a new resistance value every $T_{CLK}$ and has a period of $Ts$.Therefore in every

period, the resistor changes K time and $K = \frac{T_s}{T_{CLK}}$.The passive mixer is implemented by a pair of differential commutating switches. The spectrum scanner sweep across the spectrum by changing the LO frequency of the mixer, effectively changing the center frequency of the BPF. To understand how the circuit works, the impulse response and the frequency response are derived.

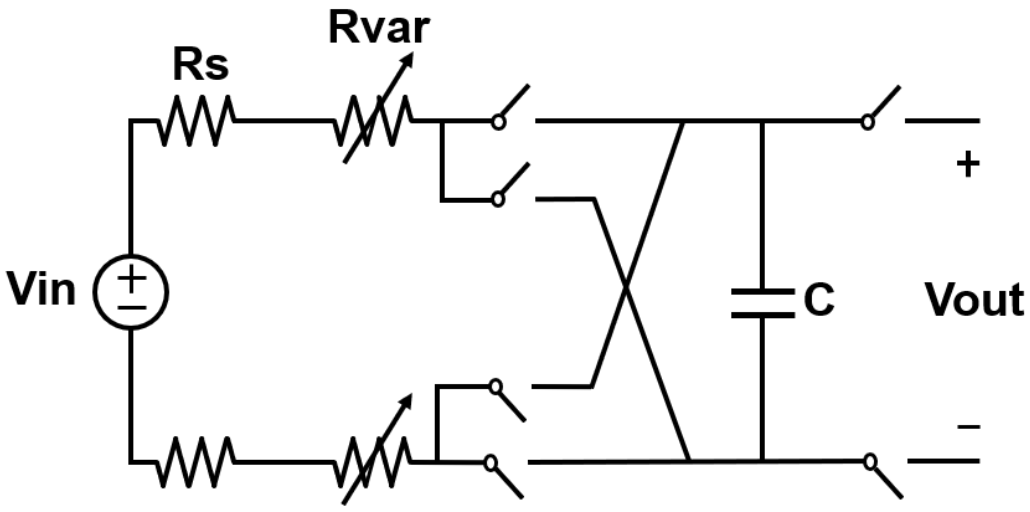



Figure 2.3: LPTV RC Filter

The impulse response can be found by using the general method for sampled LPTV circuit describe in [4]: $(a)$, Apply an voltage impulse at $t_i = T_s - \Delta t$ at the input of the circuit. $(b)$, Observe the output voltage at time $T_s$ to get the response $h(T_s, \Delta t)$. $(c)$, Sweep $\Delta t$ from 0 to $\infty$ to get $h(T_s, \tau)$. The circuit setup that is used to find its impulse response is shown in Figure 2.4.

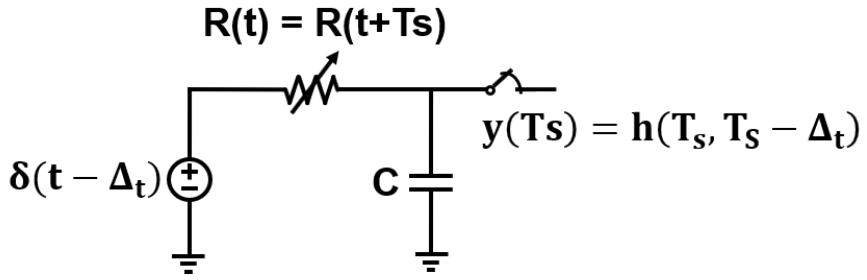



Figure 2.4: Find impulse response of the sampled LPTV RC circuit

By solving the KCL differential equation of the circuit shown in Figure 2.4, the impulse response of the sampled LPTV RC circuit can be found to be:

$$h(T_s,\tau) = \frac{1}{R(T_s-\tau)C} \times e^{\int_{T_s-\tau}^{T_s} -\frac{1}{R(u)C}du} \tag{2.5}$$

An example resistor variation and the impulse response of the LPF is shown in Figure 2.5.

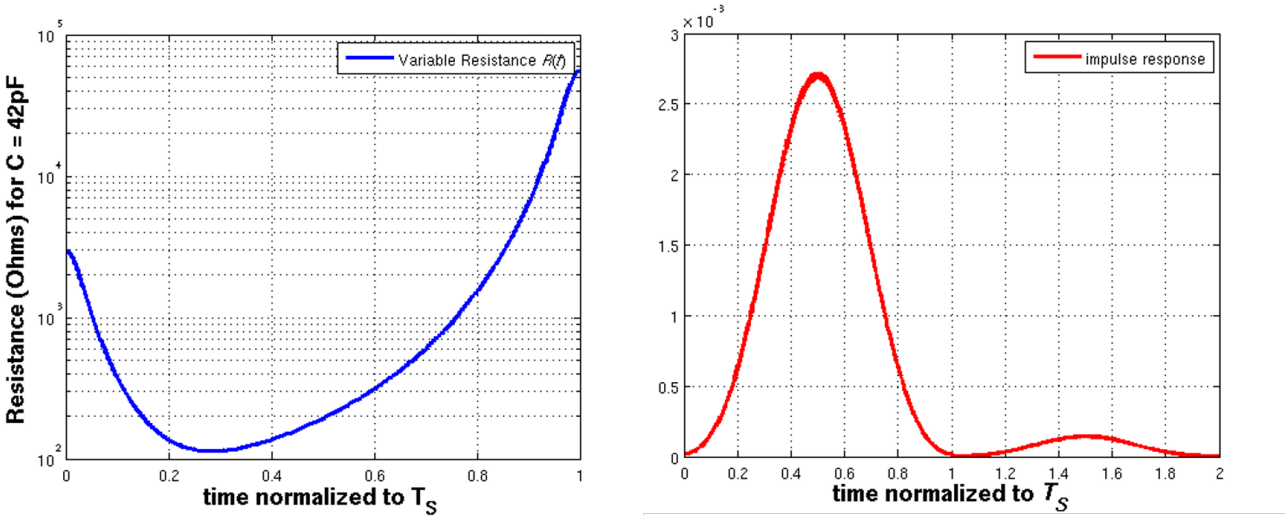



Figure 2.5: Left: Resistor variations over a period, Right: Impulse response of a designed LPF

## From Impulse Response to Frequency Response

The resistance value varies every $T_{CLK}$. Since the RC constant is orders of magnitude larger than $T_{CLK}$, the impulse response of every resistor tap can be considered as an scaled impulse function convolved with a rectangular pulse function. Let's define:

$$\begin{aligned} h[k] &= \frac{1}{R[-k]C} \times e^{\Sigma_{n=-k}^{0} -\frac{T_{CLK}}{R[n]C}} \\ &\approx \frac{1}{R[-k]C} \times \prod_{n=-k}^{0} (1 - \frac{T_{CLK}}{R[n]C}) \end{aligned}$$

and a rectangular pulse function:

$$\Pi_{T_{CLK}}(t) = \begin{cases} 1, \text{ if } 0 < t < T_{CLK} \\ 0, \text{ else} \end{cases}$$

Then the impulse reponse can be rewritten as:

$$\begin{aligned} h(T_s, \tau) &= \sum_{n=0}^{\infty} h[n] \Pi_{T_{CLK}}(t - (T_s - nT_{CLK})) \\ &= (\sum_{n=0}^{\infty} h[n] \delta(t - (T_s - nT_{CLK}))) * \Pi_{T_{CLK}}(t) \end{aligned}$$

The impulse response can be seen as a weighted sum of impulse train convolved with a rectangular pulse function $\Pi_{T_{CLK}}(t)$. By doing a continuous time fourier transform of the impulse response, the frequency response can be written as:

$$H(j\omega) = (\sum_{n=0}^{\infty} h[n] e^{-j\omega n T_{CLK}})(T_{CLK} * Sinc(\omega \frac{T_{CLK}}{2}))$$

And it can be further expanded by using the periodical property of the LPTV circuit:

$$h[k] = h[k-K] \times \prod_{0}^{K-1} (1 - \frac{T_{CLK}}{R[n]C})$$

K is number of varing resistor values in one period. The frequency response can be simplified by

the property of geometric series:

$$H(j\omega) = \frac{(\sum_{n=0}^{K-1} h[n]e^{-j\omega nT_{CLK}})}{1-(\prod_{n=0}^{K-1}(1-\frac{T_{CLK}}{R[n]C}))e^{-j\omega KT_{CLK}}}(T_{CLK} * Sinc(\omega\frac{T_{CLK}}{2}))$$

It can be seen from the frequency response of the filter that the LPTV RC filter can be mapped to an analog IIR filter convolved with rectangular pulse function. The equivalent IIR filer in direct form 1 is shown in figure 2.6, and $\beta = (\prod_{n=0}^{K-1}(1-\frac{T_{CLK}}{R[n]C}))e^{-j\omega KT_{CLK}}$. There are K poles in the IIR part of the filter spread evenly on a circle, therefore not contributing to the filtering. In a design process, a FIR filter can be designed first then iteratively map the a filter tap to a resistor values.

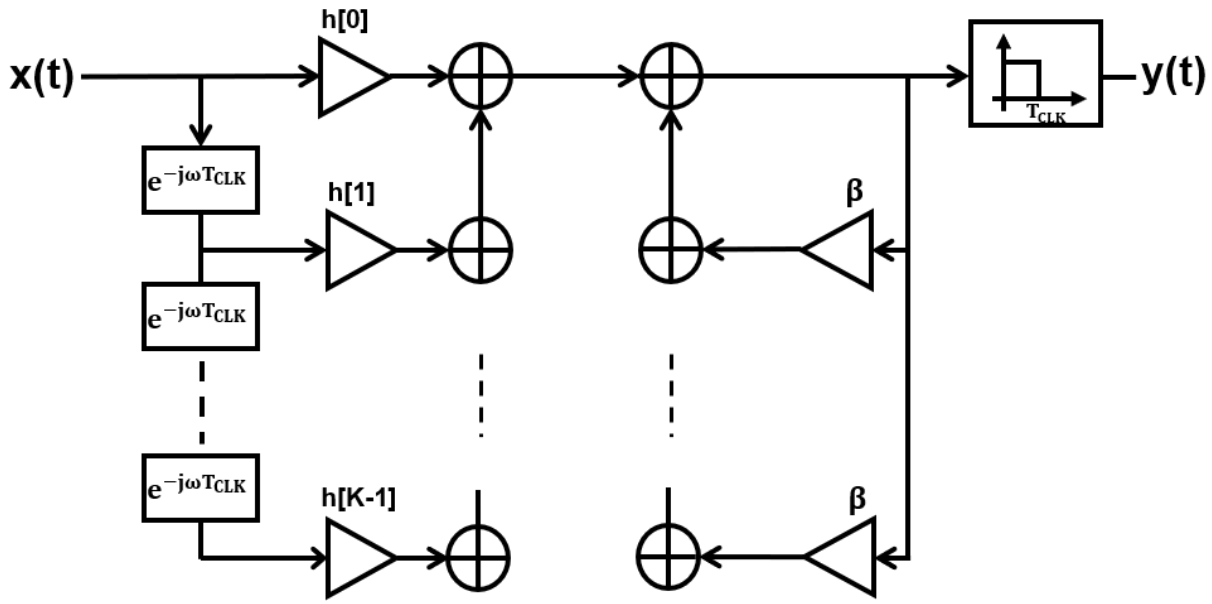



Figure 2.6: Map the sampled LPTV RC circuit to an equivalent IIR direct form 1 filter

## 2.4 Practical Limitation of the Filter and Previous Implementation.

The previous implementation of the sampled LPTV RC filter is a 0 to 1Ghz spectrum scanner achieving 31dBm OOB IIP3, 40dB stop band attenuation and 8mW of power consumption, explained in [1]. The main factors that limit the filter from achieving its ideal frequency response are the parasitic capacitors within the RDAC. Figure 2.7 shows the parasitic capacitors within one resistor unit of the RDAC.

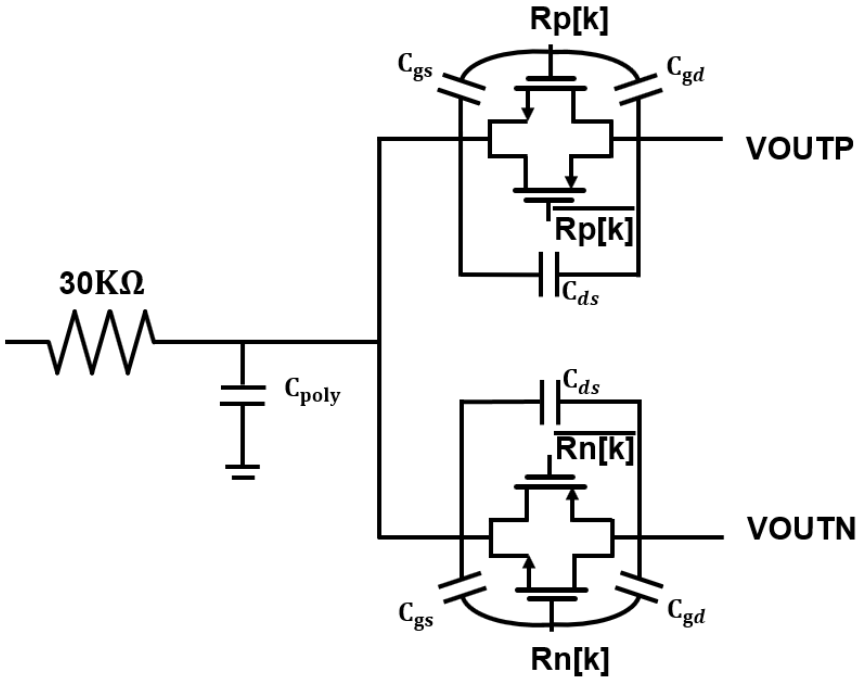



Figure 2.7: One resistor unit within RDAC.

- **RDAC with Integrated Mixer Removes $C_{ds}$'s influence.**

  Switches that remains off in the RDAC acts like a capacitor because of the existance of $C_{ds}$. The purpose of having a mixer in every resistor unit is such that the total amount of $C_{ds}$ can scale with number of resistor units between input and output. $C_{ds}$ and the main capacitor $C$

forms a voltage division from input to output. If $C_{ds}$ scales with number of resistor units that are turned on within a tap, the effect of the capacitive voltage division is also following the shape of the designed impulse response. Therefore the influence because of $C_{ds}$ is removed by using the integrated mixer. The detailed explanation can be also found in [1].

- **Sine Wave Mixing for Harmonic Rejection**

  Mixing with a square wave in conventional passive mixer creates odd order harmonics at the output. This is because conventional passive mixer is mixing with a square wave that only has two levels: +1 and -1. However the sampled LPTV RC filter can program the impulse response to an arbitrary waveform. And a sine wave mixing will result a perfect harmonic rejection. To convert a LPF to a BPF, the impulse response of a LPF is multiplied by a sine wave at the LO frequency: $h_{BPF}(t) = h_{LPF} \times sin(\omega_{LO}t)$.

The spectrum scanner built with mixer integrated RDAC and harmonic rejection mixing is implemented in [1]. The measured filter response is shown in figure 2.8. However, only 40dB stop band is achieved, which is around 20dB worse than the filter that is designed to be. The rest of the thesis shows that parasitic capacitors ($C_{poly} + C_{gs}$) causes the degradation of the filter's stop band attenuation. And a return-to-infinity(RTI) RDAC switching technique is implemented to remove the parasitic capacitor's influence on the filter's frequency response.

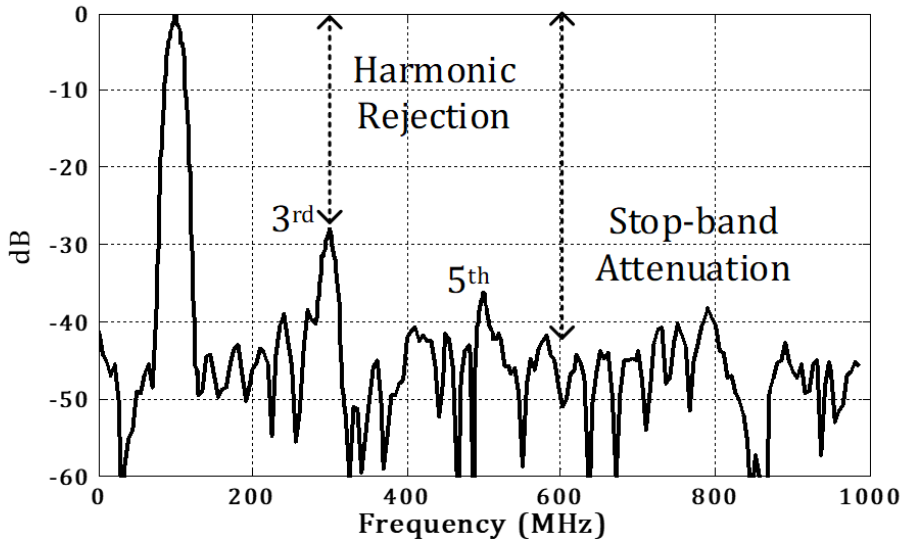



Figure 2.8: Measured frequency response of the spectrum scanner implemented in [1]

# Chapter 3

# Return-to-Infinity(RTI) RDAC Switching Technique to Remove Parasitic Capacitor $C_1$'s Influence on Filter Shape

## 3.1 Parasitic capacitors $C_1$ inside the RDAC

The varying resistors in the sampled LPTV RC filter are implemented by a digitally controlled binary resistor DAC. This chapter will discuss how the parasitic capacitance inside the RDAC, $C_1$, influence the filter's frequency response and introduce a RDAC switching technique to remove $C_1$'s influence. Figure3.1 shows the structure of the RDAC with the parasitic capacitor $C_1$ highlighted. The diagram lumps together all the elements controlled by the same bit into an equivalent resistor and a parasitic capacitor. In the actual implementation, it is built by parallel copies of unit cells to reduce mismatch. The parasitic capacitor $C_1$ is located at the junction of resistor and its corresponding switch. It includes the parasitic capacitance between resistor's polysilicon layer

to substrate layer and the transmission gate switches' gate-to-drain capacitance ($C_{gd}$). The layout extraction shows that the magnitude of the $C_1$ is around 1.5fF for one unit cell.These parasitic capacitance eventually becomes an equivalent switch capacitor circuit resistance . Let's see how $C_1$ influences the filter's operation.

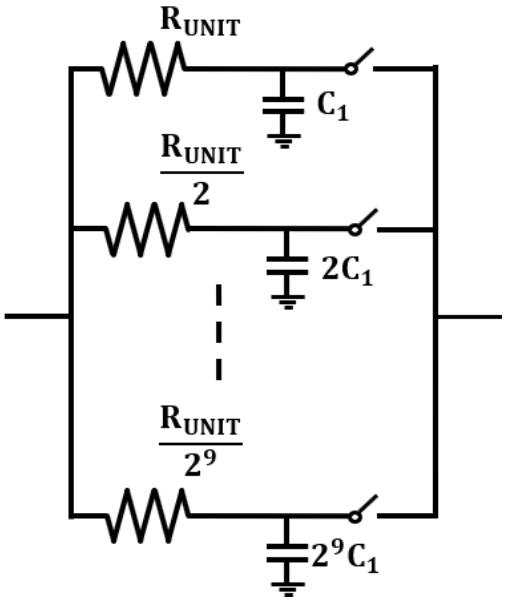



Figure 3.1: Resistor DAC without the Integrated Mixer, highlight parasistic capacitance C1

## 3.2 Switch Capacitor Model of Parasitic Capacitor $C_1$ During Switching

To demonstrate the effect of the $C_1$, let's take a 3-bit RDAC as an example, as shown in Figure3.2. At the first cycle when $t = nT_{CLK}$, assume the resistor code is 6. The switches at the second and the third bit of the RDAC are closed. And the switch at the first bit is open. Since the time constant of $R_{UNIT}$ and $C_1$ is an order of magnitude smaller than $T_{CLK}$, the voltage across the $C_1$ is tracking $V_{in}[n]$ . Therefore, the quantity of charges accumulated at the $C_1$ is $q = C_1 V_{in}[n]$. At the next cycle when $t = (n+1)T_{CLK}$, resistor code becomes 3. The RDAC is switching the $1^{st}$ bit from open

to close and the $3^{rd}$ bit from close to open, while the $2^{nd}$ bit remains unchanged. Since $C_1$ is now directly connected to output, the quantity of the charges accumulated at the $C_1$ is changed to $q = C_1 V_{out}[n+1]$. The amount of the charge transferred from the input to the output in the $1^{st}$ bit is proportional to the difference of input and output voltage. And the average current due to $C_1$'s charge transfer can also be written, as shown in the following equations.

$$\Delta_q = C_1 (V_{in}[n] - V_{out}[n+1]) \tag{3.1}$$

$$I = \frac{\Delta_q}{T} = \frac{C_1}{T_{CLK}} (V_{in}[n] - V_{out}[n+1]) \tag{3.2}$$

Therefore the switched capacitor circuit formed by $C_1$ equivalently becomes a resistor. However, when $C_1$ is connecting to output, there is still current flowing from input to output through a resistor. This is clearly different from a stand-alone switched capacitor circuit.

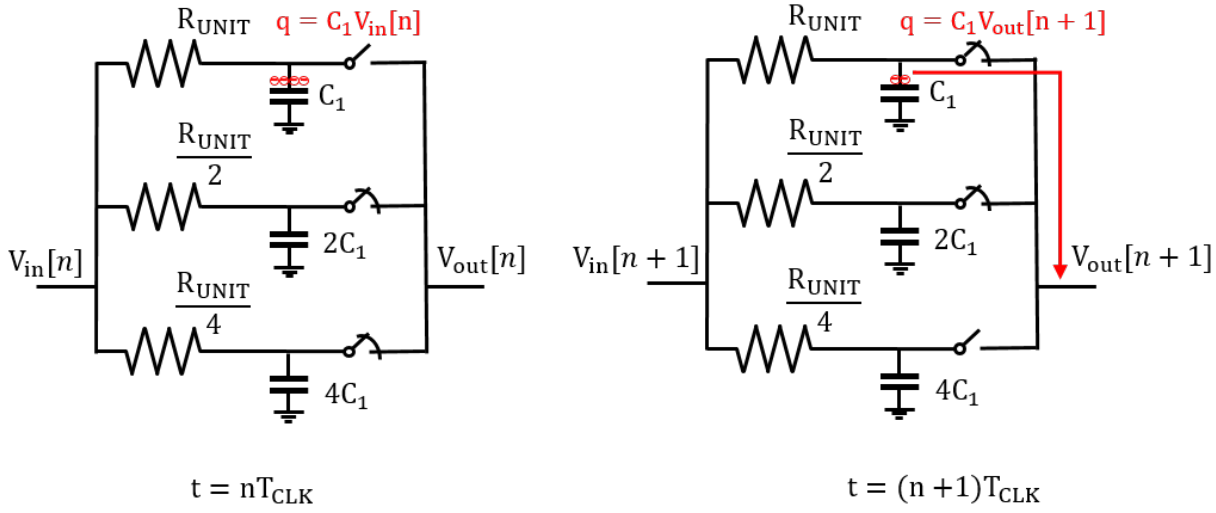



Figure 3.2: A 3 bit RDAC demonstrates $C_1$'s effect on filter operation

The stand-alone switched capacitor circuit samples input voltage at one cycle, and transfer the charges on the capacitor to the output at the next cycle with input disconnected. However, the switched capacitor circuit formed by $C_1$ within the RDAC is slightly different. While capacitor $C_1$ samples the input voltage at $t = nT_{CLK}$, it transfer charges to output while input is still connected

to output with a resistor R at $t = (n+1)T_{CLK}$. A table that compares the stand-alone switched capacitor circuit and the switched capacitor circuit formed by $C_1$ is shown in Figure 3.3.

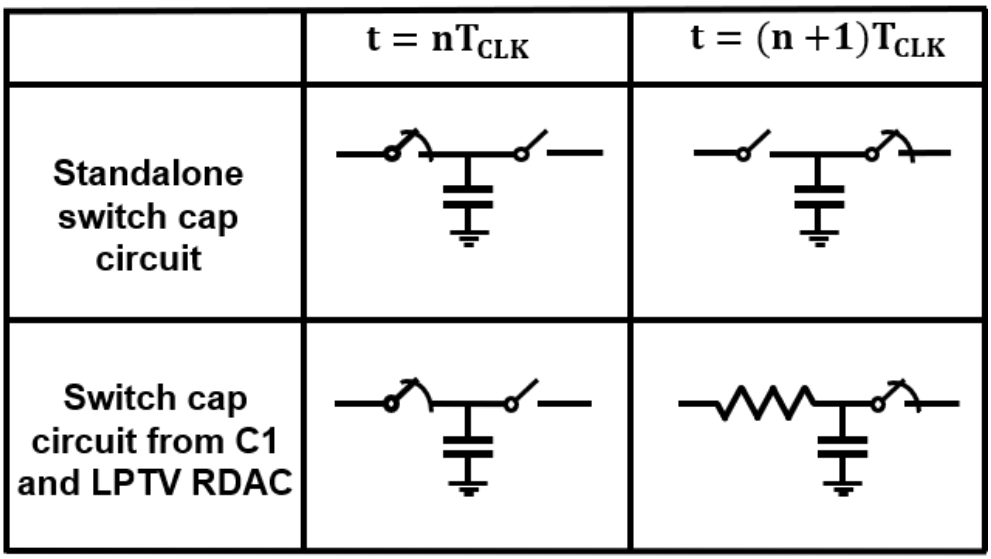



Figure 3.3: Comparison between stand-alone switched capacitor circuit and switched capacitor circuit from C1 within RDAC

Since the switch's resistance is orders of magnitude smaller than $R_{UNIT}$, all the charges are transferred to output instead of input. Therefore, $R_{UNIT}$ can be removed when we only consider the effect from $C_1$. The equivalent circuit of the combination of $R_{UNIT}$ and $C_1$ is a stand-alone switched capacitor circuit form by $C_1$ in parallel with $R_{UNIT}$, as shown in Figure 3.4. By further simplifying the switched capacitor circuit into an equivalent resistor, it becomes $R_{UNIT}$ in parallel with switched capacitor resistance $R_{SC} = \frac{T_{CLK}}{C_1}$. In the previous sampled LPTV RC filter design, $R_{UNIT} = 33K\Omega$, $C_1 = 2.5fF$. For a filter operating at $f_{CLK} = 2Ghz$, the equivalent switched capacitor resistance of $C_1$ is: $R_{SC} = \frac{1}{f_{CLK} * C_1} = 200K\Omega$. If the filter is designed to triple the original scanning range, the filter would operate three times faster than before, such that $f_{CLK} = 6Ghz$. The equivalent switched capacitor resistance becomes $R_{SC} = 66.7K\Omega$, which is only 2 times larger than the $R_{UNIT}$, therefore greatly changing the actual resistor value.

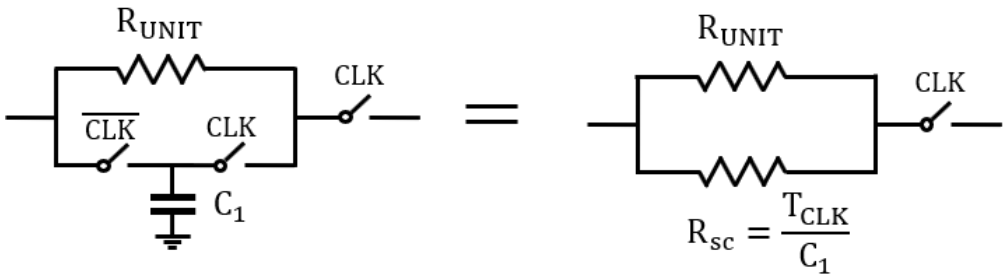



Figure 3.4: RDAC resistor in parallel with switched capacitor circuit resistor from C1

## 3.3 Parasitic Capacitor $C_1$ Changes Filter's Response

It should be emphasized that not every parasitic capacitor $C_1$ within the RDAC is forming an equivalent switched capacitor circuit. Only the $C_1$s that are switched from the input to the output are forming a parallel switched capacitor circuit with the RDAC. The amount of $C_1$ that forms the switch capacitor circuit depends on the switching behavior of the RDAC, and it is a nonlinear function with the resistance value. Because of the extra nonlinear resistors in parallel with the RDAC resistor at every cycle, the filter's impulse response and frequency response is altered. Fig 3.5 shows the comparison of an ideal impulse response and an impulse resposne with $C_1$ present. The shown impulse response is from a low pass filter operating at $f_{clk} = 6Ghz$ and the parasitic capacitor $C_1$ in each unit resistor is $1.5fF$. The corresponding frequency response of the ideal filter and the filter with $C_1$ present is shown in Fig3.6.

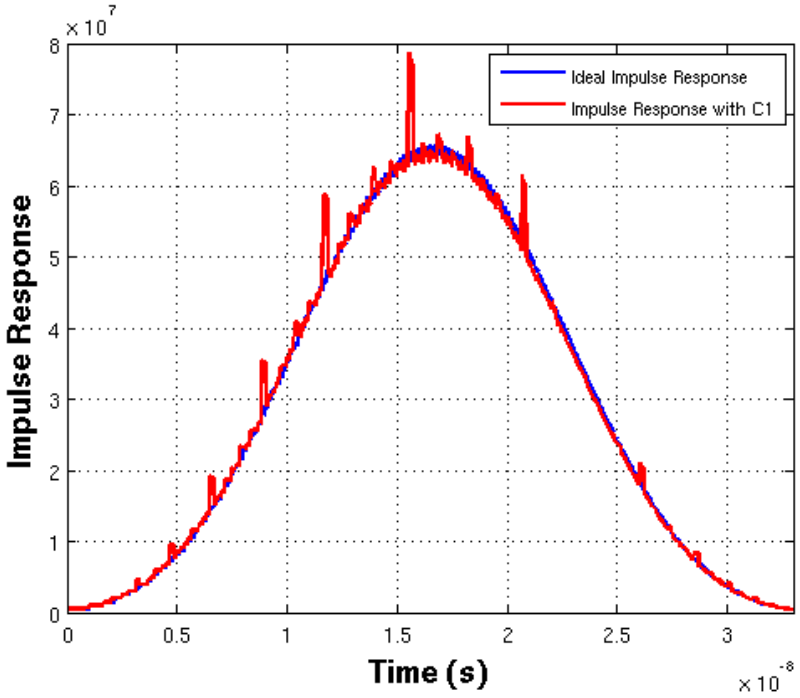



Figure 3.5: Impulse response of an ideal low pass filter (in blue), and the impulse response of the same low pass filter with C1 present (in red).

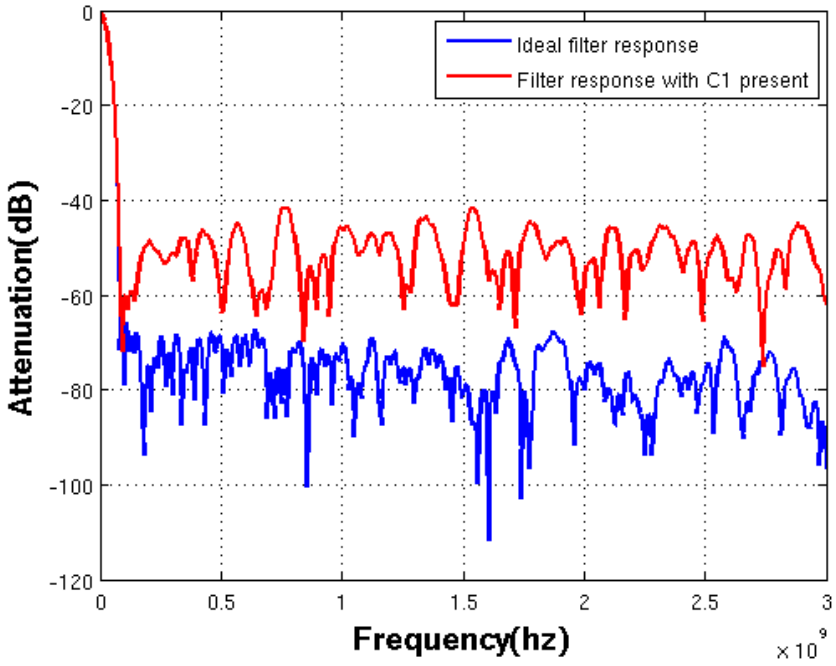



Figure 3.6: Frequency response of an ideal low pass filter (in blue), and the Frequency response of the same low pass filter with C1 present (in red).

A band pass filter with center frequency at $1.65Ghz$ is also simulated. And the frequency response of the with and without parasitic $C_1$ is shown in Figure3.7.

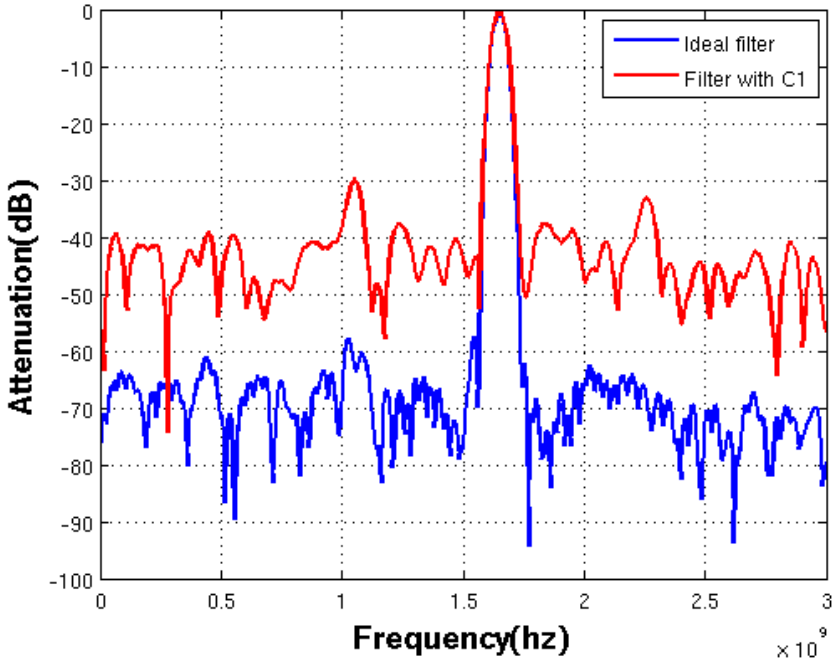



Figure 3.7: Frequency response of an ideal band pass filter centered at $1.65Ghz$ (in blue), and the frequency response of the same band pass filter with C1 present (in red).

It can be concluded from both the lowpass filter and the bandpass filter's frequency response that $C_1$ significantly degrades the filter's stop band attenuation. In the example of the filter operating at $f_{clk} = 6Ghz$ and parasitic capacitor $C_1 = 1.5fF$, the filter's stop band attenutation is degraded from 60dB to 40dB. Therefore, a way to remove the $C_1$'s influence on the filter's stop band attenuation is needed.

## 3.4 Return-to-Infinity(RTI) RDAC Switching Technique to remove the influence of $C_1$

Parasitic capacitor $C_1$ acts like a nonlinear resistors in parallel with RDAC and degrades the filter's stop band attenuation by more than 10dB. To remove the influence of $C_1$, a return-to-infinity (RTI) RDAC switching technique is proposed in [5]. The idea is to make the RDAC an open circuit before it is switched to the next resistance value. A diagram demonstrating the operation of the return-to-infinity RDAC switching tehcnique is shown in figure 3.8.

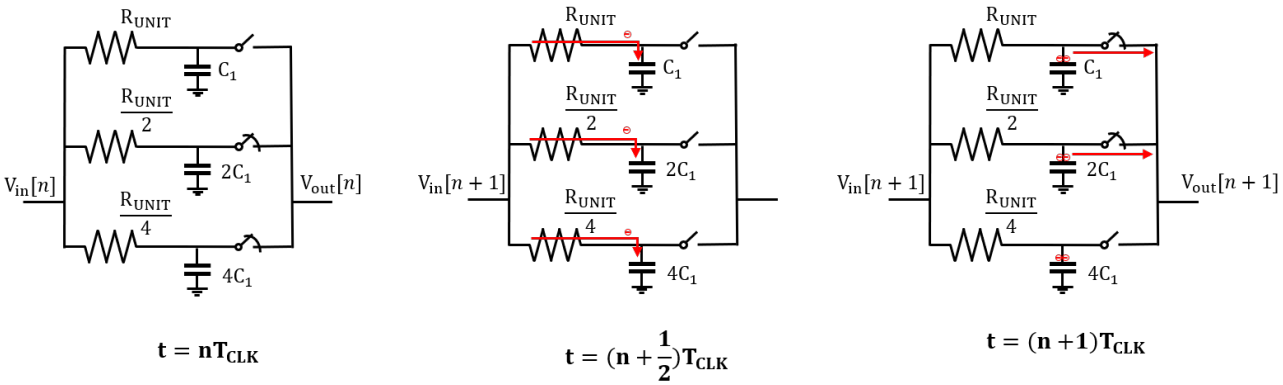



Figure 3.8: RTI RDAC switching: make RDAC an open circuit between two resistor taps.

By opening the switch of every resistor unit between two resistor tap, $C_1$ in every resistor unit forms a switched capacitor circuit. The equivalent effect is that every *Runit* has an extra resistor in parallel because of $C_1$. Figure 3.9 shows the comparison between an ideal 10 bit RDAC and the equivalent circuit of the RDAC using the return-to-infinity switching operations. By doing RTI, the resisotr formed by switched $C_1$ circuit becomes a linear resistor. Although it changes the equivalent value of $R_{unit}$, $R'_{unit} = R_{unit} || \frac{T_{clk}}{C_1}$, the shape of the impulse response is preserved and the filter's stop band attenuation is not degraded.

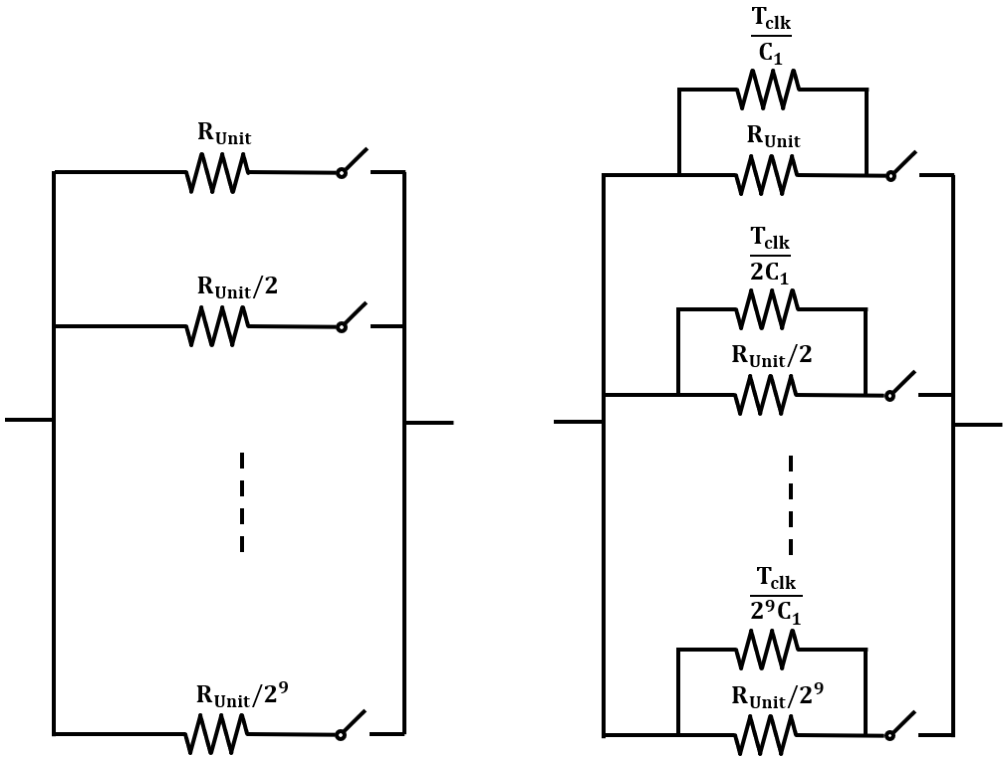



Figure 3.9: Left: Ideal RDAC , Right: Equivalent circuit of RDAC with C1 using RTI switching.

The impulse response of an ideal LPF and a LPF with $C_1$ but uses RTI RDAC is shown in figure 3.10. Its frequency response is shown in figure 3.11. The stop band attenuation is preserved, while the transition bandwidth is slightly influenced. Figure 3.12 shows the comparison of and ideal BPF and a BPF with $C_1$ using RTI RDAC.

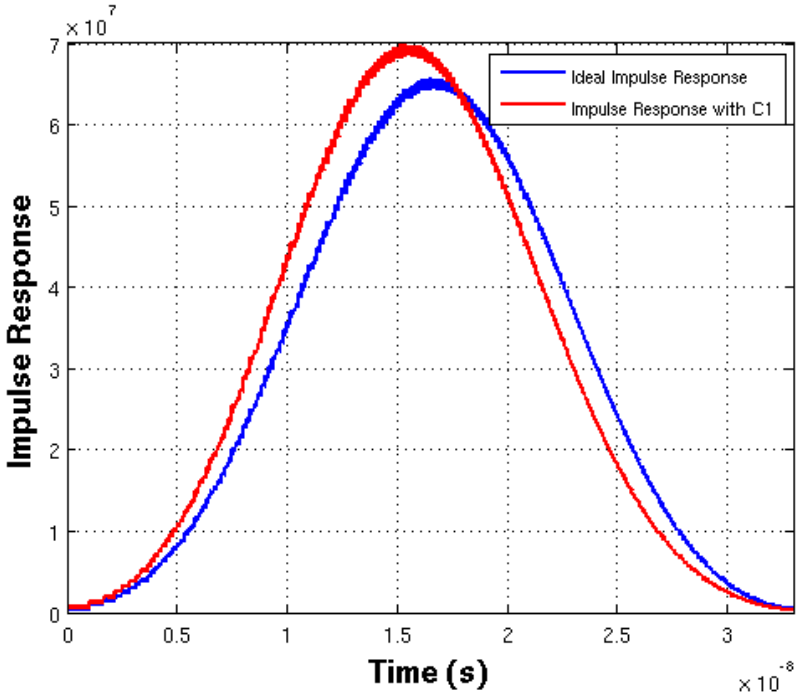



Figure 3.10: Comparison of the impulse response of an ideal LPF(in blue) and the impulse response of LPF with C1 using RTI RDAC(in red).

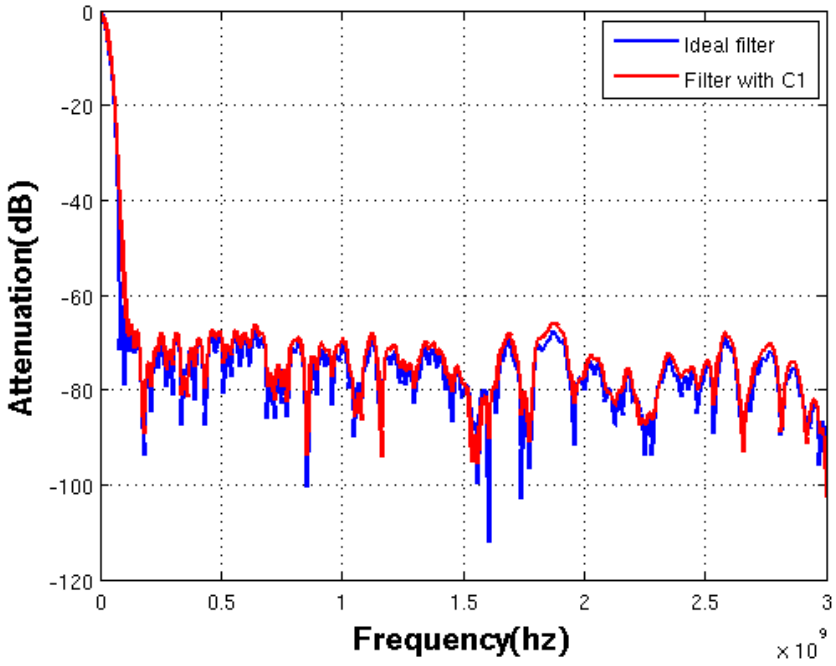



Figure 3.11: Frequency response of an ideal LPF(in blue) and the LPF with C1 using RTI RDAC(in red).

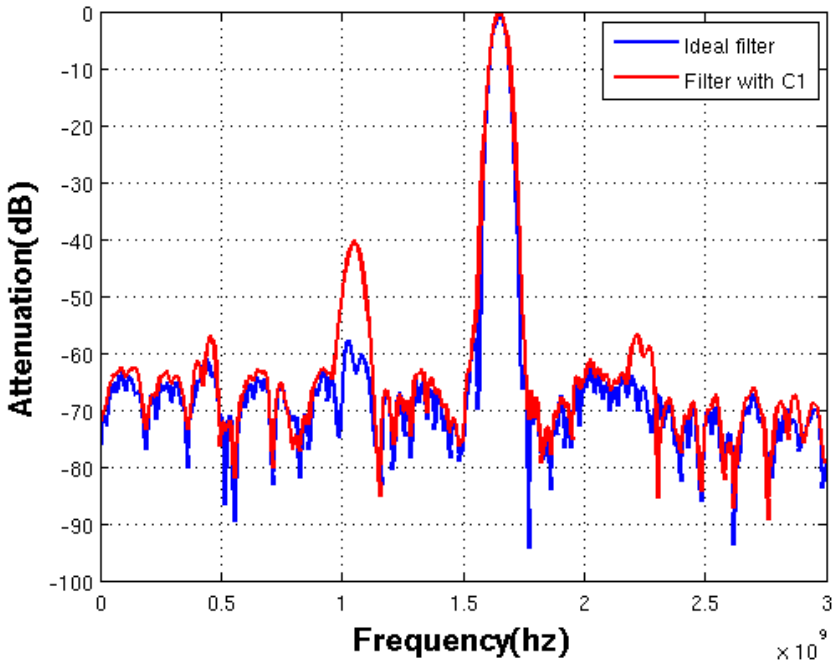



Figure 3.12: Frequency of an ideal BPF centered at 1.65Ghz(in blue) and a BPF with C1 using RTI RDAC(in red).

The stop band attenuation of the BPF is preserved, while the 3rd order and 5th order harmonic rejection ratio is degraded. It is caused by the change of resistance value within RDAC. Although RDAC's unit resistance is scaled from $R_{unit}$ to $R_{unit}||\frac{T_{clk}}{C_1}$ , the input resistance is a 50Ω differential resistance, not scaled. It creates an odd order harmonics of the LO sinewaves in the impulse response. A mathematical proof can be found by writing the impulse response of the filter.

The filter taps derived in chapter 2 are:

$$h[k] \approx \frac{1}{R[-k]C} \times \prod_{n=-k}^{0} (1 - \frac{T_{CLK}}{R[n]C})$$

If we only consider the impulse response of the sine wave LO signal and use the approximation:

$h[k] = 1/R[-k]C$. The ideal impulse response is:

$$\begin{aligned} h[k] &\approx \frac{1}{R[-k]C} = sin(\omega_{LO} k T_{clk}) \\ &= \frac{1}{(R_s + \frac{R_{unit}}{n_k})C} \end{aligned}$$

When $C_1$ is considered, the equivalent effect is that $R_{unit}$ is changed to $R_{unit}||\frac{T_{clk}}{C1}$. Let $R_{unit}||\frac{T_{clk}}{C1} = \alpha R_{unit}$. The impulse response when $C_1$ is present becomes:

$$\begin{aligned} h[k]' &= \frac{1}{(R_s + \alpha\frac{R_{unit}}{n_k})C} \\ &= \frac{1}{(R_s + \frac{R_{unit}}{n_k})C} \times \frac{1}{1 - ((1-\alpha)\frac{R_{unit}}{n_k}\frac{1}{Rs + \frac{R_{unit}}{n_k}})} \\ &\approx \frac{1}{(R_s + \frac{R_{unit}}{n_k})C} \times (1 + ((1-\alpha)\frac{R_{unit}}{n_k}\frac{1}{Rs + \frac{R_{unit}}{n_k}}) + ((1-\alpha)\frac{R_{unit}}{n_k}\frac{1}{Rs + \frac{R_{unit}}{n_k}})^2) \\ &= sin(\omega_{LO} k T_{clk}) \times (1 + ((1-\alpha)\frac{R_{unit}}{n_k} sin(\omega_{LO} k T_{clk})) + ((1-\alpha)\frac{R_{unit}}{n_k} sin(\omega_{LO} k T_{clk}))^2) \end{aligned}$$

As can be seen in the result, impulse response of the LO sine wave when $C_1$ is present has terms of LO frequencies' harmonics.

## 3.5 Polyphase Implementation of the RTI RDAC

Inserting an open circuit in the RDAC between two resistor taps is equivalent to upsampling the impulse response of the original filter. This will cause the 3 dB bandwidth of the filter become half of the orignal filter. In order to preserve the original filter, two RDACs are operating in a polyphase fashion. Figure 3.13 shows the polyphase implementation of the RTI RDAC. While one RDAC is conducting current from the input, the other RDAC is an open circuit. In this way, the upsampling

effect because of the return to infinity is avoided. The amount of the $C_1$ switched from input to output is proportional to number of $R_{unit}$ in parallel. Therefore, switched $C_1$ forms a linear resistor in parallel with all $R_{unit}$s between input and output.

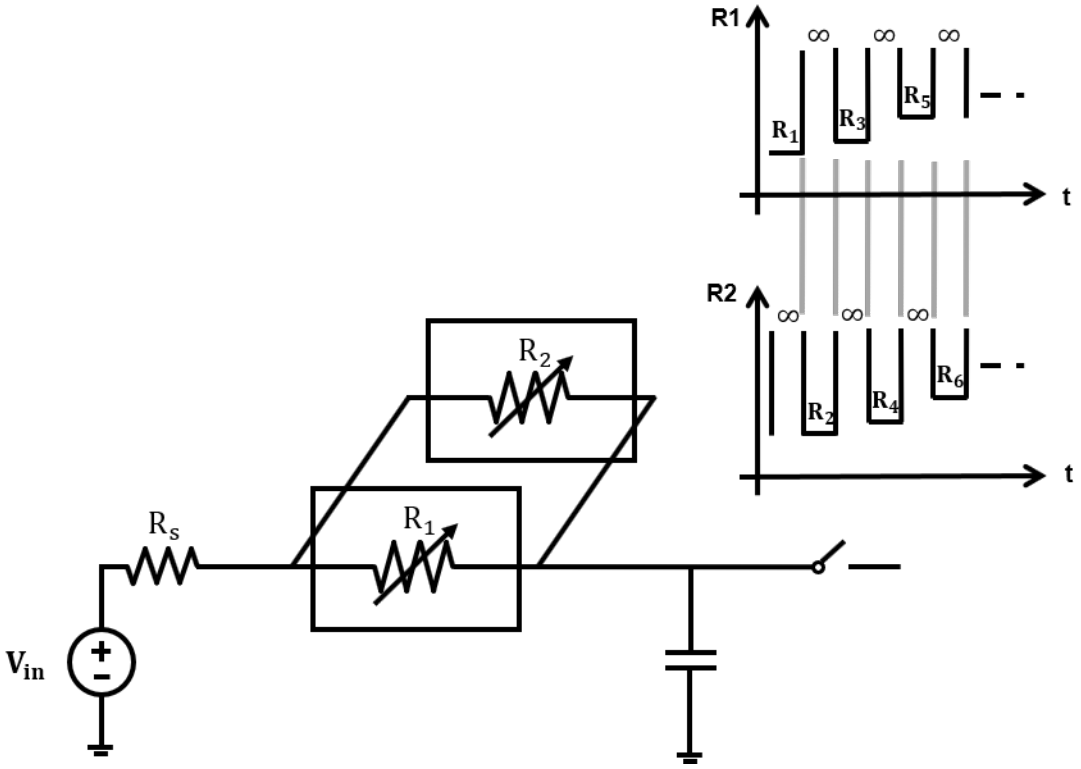



Figure 3.13: Polyphase implementation of the RTI RDAC.

# Chapter 4

# Design of a 0-3Ghz Spectrum Scanner with Return-to-Infinity RDAC to remove $C_1$'s influence on stopband attenuation

This chapters will present the details of the circuit design for the spectrum scanner with the scanning range of 0 to 3*Ghz*. The RDAC of the spectrum scanner uses the return-to-infinity switching technique introduced in the Chapter 3 to remove $C_1$'s influence on the filter's stopband attenuation. To avoid upsampling of the filter's impulse response, a ployphase implementation of two RDACs is used. Each RDAC is operating at 3*Ghz*, but in a time interleaving fashion, therefore the filter is effectively operating at 6*Ghz*. Special care is given to make sure that the critical circuit blocks are able to function correctly at a 6*Ghz* rate.

## 4.1 Architecture of the Spectrum Scanner Using RTI RDAC Switching Technique

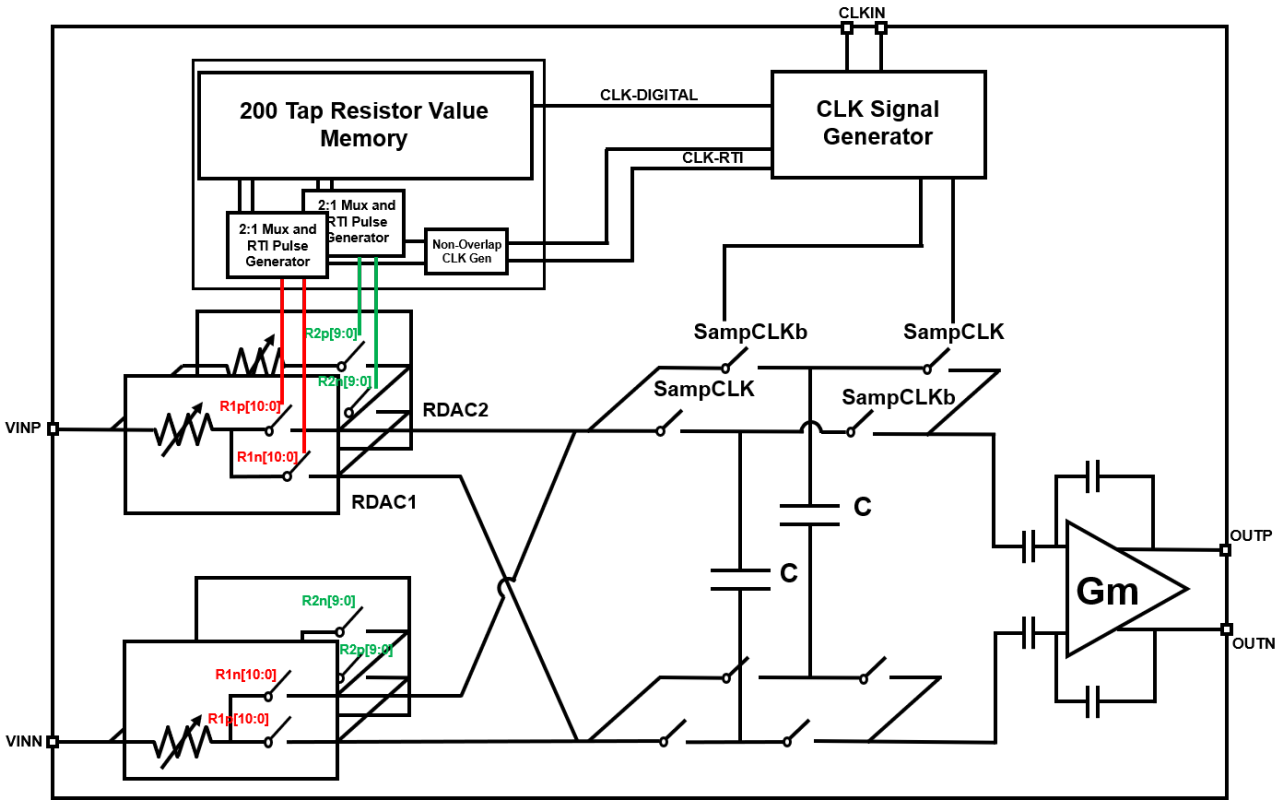



Figure 4.1: System diagram of the spectrum scanner.

Figure4.1 presents the top level block diagram of the proposed spectrum scanner implementing the return to infinity RDAC switching technique to remove the parasitic capacitor $C_1$'s influence on the filter's frequency response. The whole circuit can be partitioned into several main blocks: resistor DAC, capacitor band, ping-pong sampling circuit, resistor value memory, clock generation block and output voltage buffer. The following sections will go into the design details of each block.

## 4.2 Resistor DAC with Integrated Mixer

The values of the resistor is designed to be quantized into 10 bit such that the influence of quantization on filter's stop band attenuation is less than 5dB. Each tap of resistor value is stored in the on-chip memory and read out serially to the digital-to-analog resistor bank. The LSB resistor unit value is $33K\Omega$. The subsuquent bit in the RDAC is built by copying multiples of the LSB resistor units in parallel to lower the effect of mismatch. Figure 4.2 a) shows the structure of one resistor unit. Each resistor unit also includes a passive mixer built from two transmission gate switches. It has been shown in [1] that integrating mixer in resistor unit will remove the influence of $C_{ds}$ of the transmission gate switch on filter shape. Since parasitic capacitors within resistor unit are critical to filter's frequency response, they are extracted from layout and shwon in Figure 4.2 b). The total parasitic capacitance at the junction of resistor and switches is $C1 = 1.1fF$.

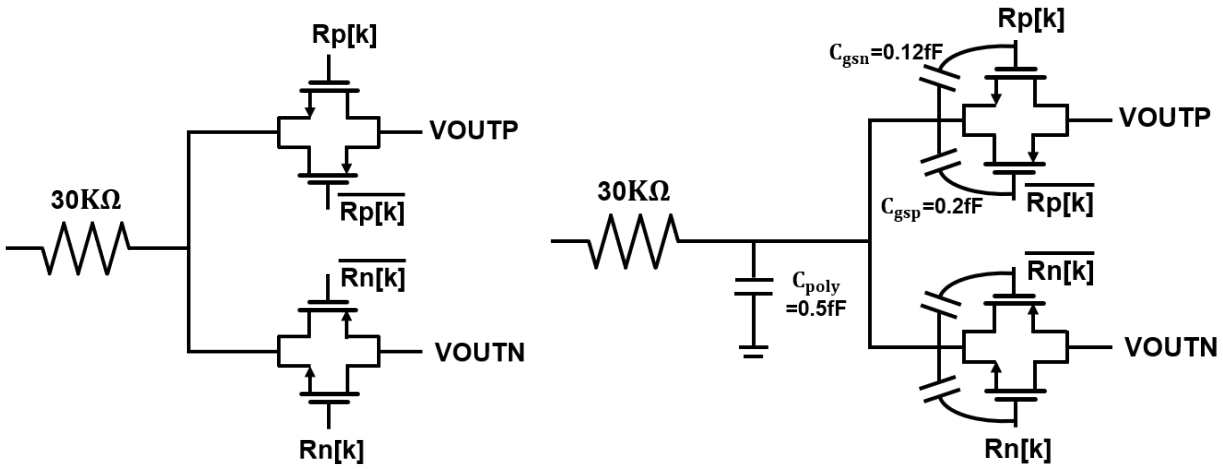



Figure 4.2: a) One resistor unit, b) Resistor unit with extracted parasitic capacitors.

Transmission gate's on resistance is chosen to be less than 10% of the $R_{unit}$ to meet linearity requirement. The simulated value of transmission gate's on resistance vs switch's bias voltage in different corners is shown in Figure 4.3. Different corners compensated by calibrated the RDAC and pre-diostort the resistor codes.

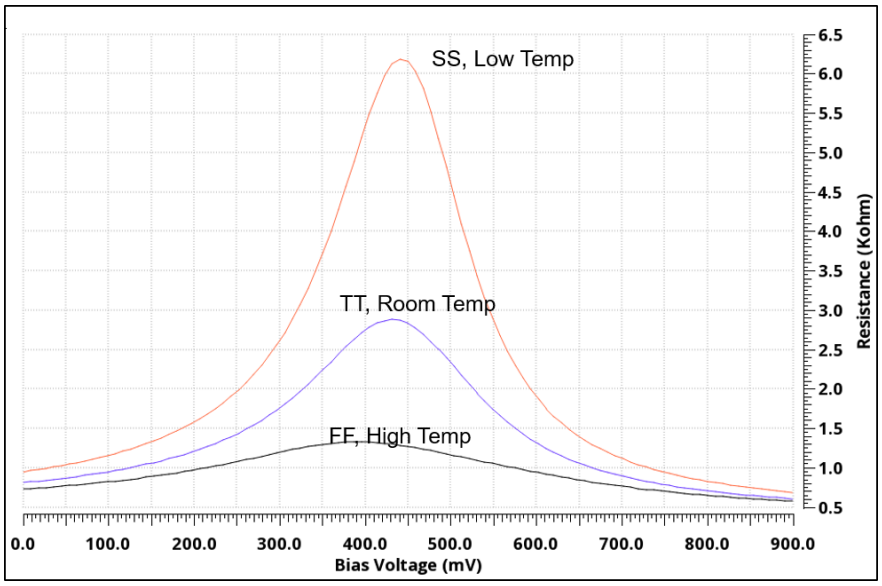



Figure 4.3: Transmission gate resistance vs DC biased voltage

The $k^{th}$ bit of the RDAC consists of $2^k$ resistor units in parallel. They are laid out in a common centroid way to have a better matching.

## 4.3 RDAC Control Signal Generation

In order to remove parasitic capacitor $C_1$'s influence on filter's frequency response, return to infinity RDAC switching technique is implemented by time interleaving two RDACs. While one RDAC is conducting current from the input, the other RDAC remains open, having an ideally infinite resistance value. The ployphase implementation of two RDACs avoids upsampling of the impulse response, therefore maintaining the same 3-dB bandwidth for the filter. Figure 4.4 shows the resistor values of the two RDACs vs time.

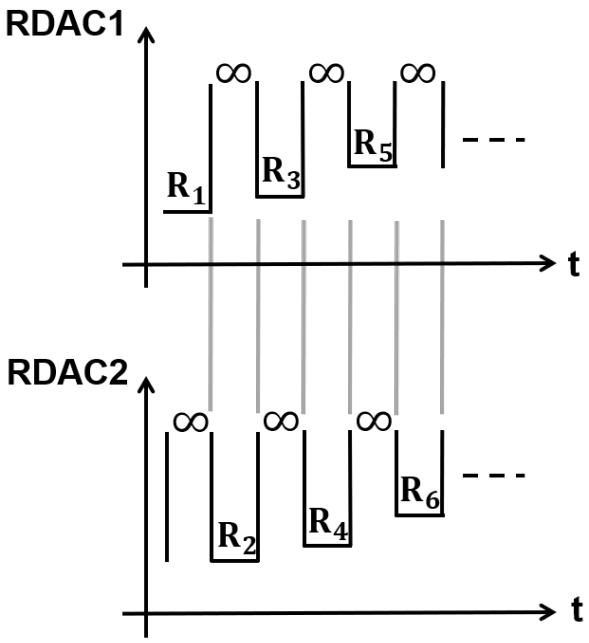



Figure 4.4: Resistor values of two time-interleaved RDACs vs time

When resistance value goes to infinity, the control signal for the RDAC returns to zero. Therefore, each RDAC is controlled by a return-to-zero waveform. Two RDACs' control signals are ideally 180 degree out of phase. However, because of the mismatch of the buffer chains between two RDACs, control signals will overlap if each of the signal has a 50% duty ratio. The overlap creates a periodical glitch in the filter's impulse response, degrading filter's stopband attenuation. If the duty ratio of the control signal is slightly less than 50%, the overlap between two signals can be avoided. The non-overlapping control signals are generated by doing an AND operation between a less than 50% clock signal and the control signals.The non-overlapping clock signal are generated by an non-overlapping clock generator, which is essentially a RS latch. The circuit diagram of the Non-overlapping clock generator is shown in figure 4.6. The inverter buffers in the non-overlapping clock generator are used to change the non-overlapping duration between two output signals.Figure 4.6 shows the output of the non overlapping generator. The simulated non overlapping duration in each period is $16ps$.

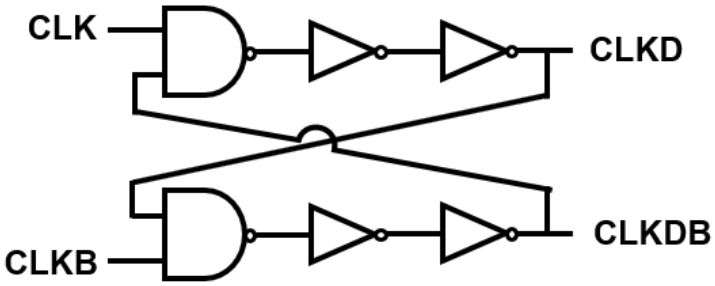



Figure 4.5: Non overlapping clock generator.

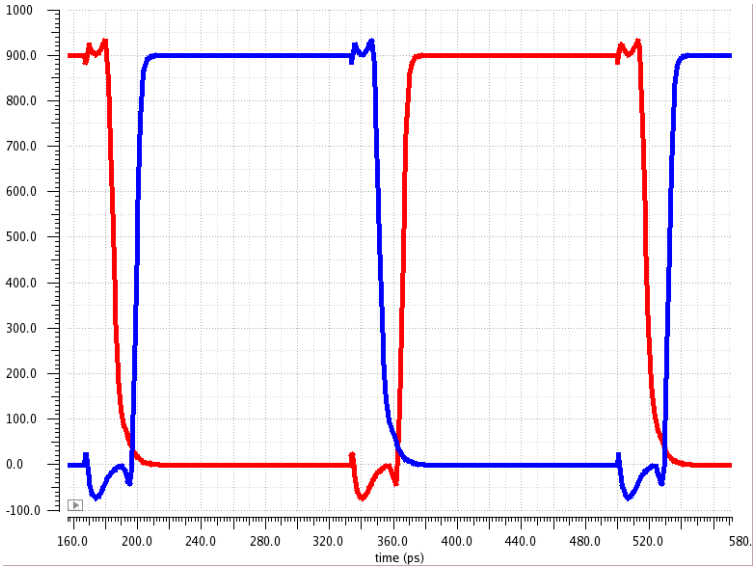



Figure 4.6: Output of the non overlapping clock generator.

Two hundred resistor values are stored in serial-in-parallel-out (SIPO) shift registers. And a 200-to-1 multiplexer serially reads the resistor values. To lower the power consumption of the digital block, the resistor value memory is divided into two halves. Each memory block produces output at half the rate of the RDAC's control signal, $\frac{f_{clk}}{2}$. Figure4.7 shows the organization of the resistor value memories.

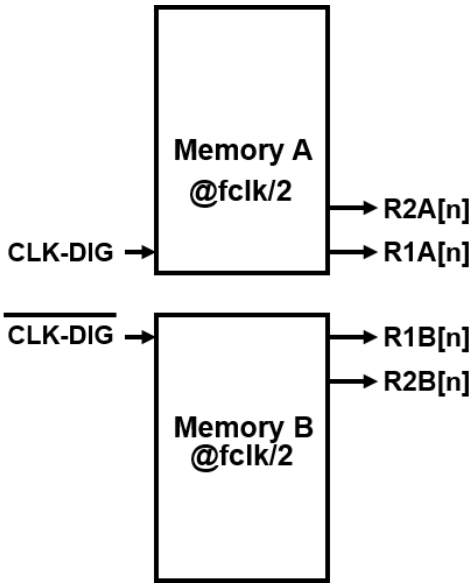



Figure 4.7: Split resistor memory in half to reduce power consumption

A 2-to-1 serializer is used afterwards to double the rate of memory output to $f_{clk}$. Figure 4.8 shows the timing diagram of the serializers and RTI pulse generator using AND gates. The clock signal at the AND gate's input has to align with the output of the 2-to-1 multiplexer, otherwise producing glitches to the RDACs. The alignment technique and how different clocks are generated will be explained in the next section.

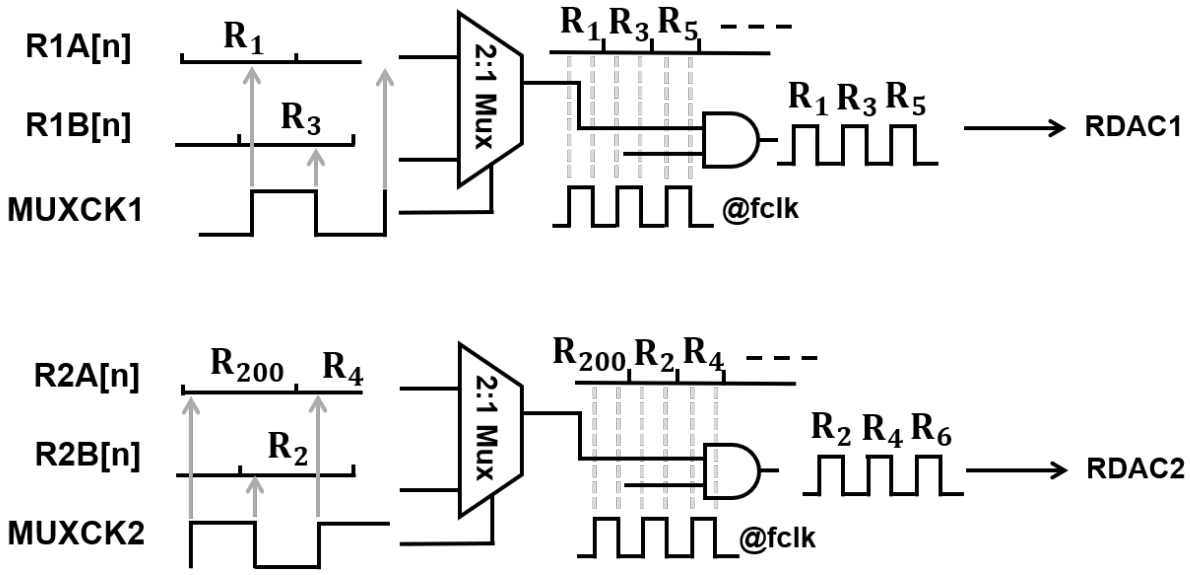



Figure 4.8: 2-to-1 serializer and RTI Pulse Generator

## 4.4 Clock Signal Generations

Generating clock signals are critical part of the circuit. The blocks controlled by clock signals are resistor value memories, serializer, RTI pulse generator and sampling circuit. An overview of the on-chip clock signals derived from the external signal sources is shown in figure 4.9.

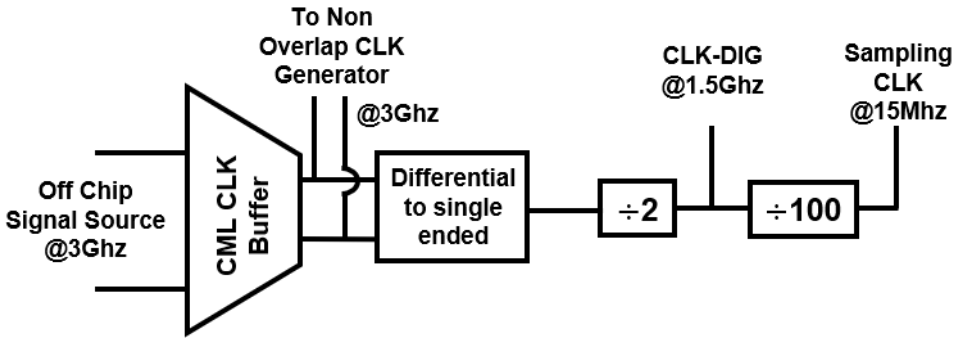



Figure 4.9: Overview of the on-chip clock signals derived from external signal source.

The chip receives a differential clock signal from an external signal source, then buffered by a

differential current mode logic buffer, shown in Figure4.10. The differential outputs of the buffer go to the non-overlapping clock generator, which controls serializer and RTI pulse generators. The outputs of the clock buffer are also converted into a signal ended signal. The signal is then divided by half to control the resistor value memories. And the CLK-DIG is further divided by 100 to control the sampling circuit.

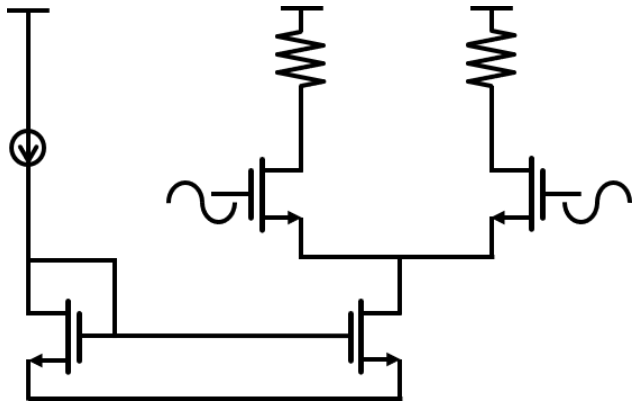


Figure 4.10: CML Clock Buffer

## Data alignment at the RTI Pulse Generator

Return to infinity RDAC is implemented by controlling RDAC with a return-to-zero signal. It is created by doing an AND operation between output of the serializer and a clock signal running at $f_{clk}$. In order to generate the signal without a glitch, the phase difference between output of the serilizer and the clock signal has to be controlled. Figure 4.10 shows the data alignment circuit for the RTI pulse generator.Non overlapping clock generator creates a pair of differential clocks signals, CLK1 / CLK1b, running at $f_{clk}$.

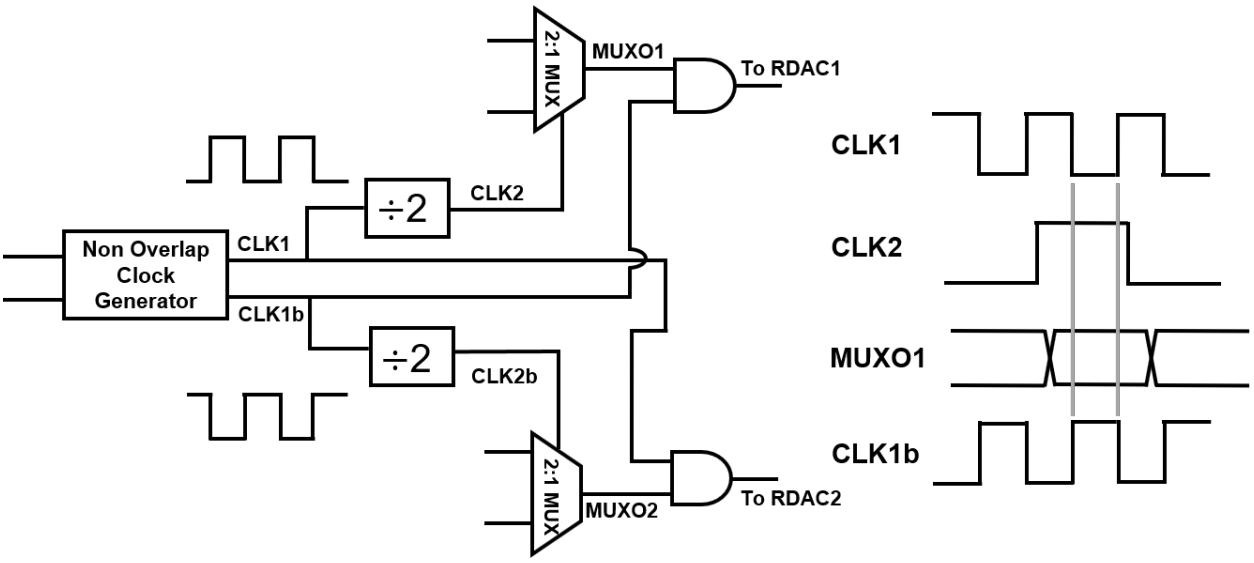



Figure 4.11: Data Alignment at the RTI Pulse Generator

CLK1 is divided by 2 and drives two 2:1 serilizers. The circuit diagram of the 2:1 serializer is shwon in figure 4.11.

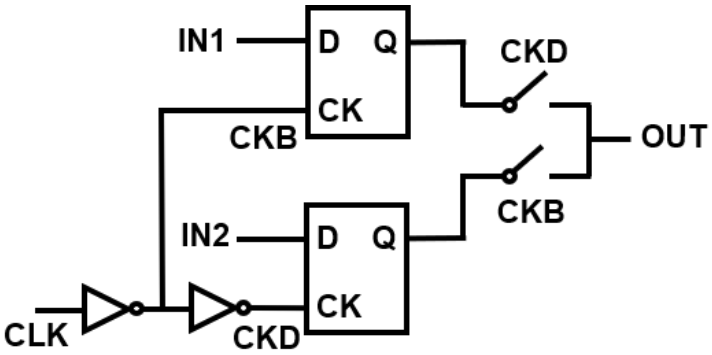



Figure 4.12: 2 to 1 serializer

The delay from CLK1 to the output of the 2-to-1 serializer MUXO1 is $t_{CLK1-MUXO1} = t_{ck-q} + t_{ck-q} + 2 \times t_{inv}$. ( $t_{ck-q}$ is flip flop's clock to q delay and $t_{inv}$ is inverter's propagation delay). The serializer output MUXO1 has the frequency of $f_{clk}$, therefore MUXO1 has a pulse width of $T_{clk}$. As long as the clock signal at the AND gate input lags MUXO1 by a time that is larger than 0

and smaller than $\frac{T_{clk}}{2}$, the output of the AND gate will not create a glich. To express the timing constraint between clock signal at AND gate and CLK1, we get:

$$t_{CLK1-MUXO1} < t_{CLK1-ANDCLK1} < t_{CLK1-MUXO1} + \frac{T_{clk}}{2} \tag{4.1}$$

For CLK1b, $t_{CLK1-ANDCLK1} = \frac{T_{clk}}{2}$. If

$$\frac{T_{CLK}}{2} > t_{CLK1-MUXO1}, \tag{4.2}$$

the timing constraint is met for signal CLK1b. Table 4.1 summarizes the simulated CLK1 to MUXO1 delay in different PVT corners. The worst case delay is less than $\frac{f_{clk}}{2} = 166.7ps$. Therefore, CLK1b pulse will be centered in the middle of one MUXO1 data output. And it will guarantee that the output of the RTI pulse generator does not have any glitch.

| | SS, Low Temp | TT, Room Temp | FF, High Temp |
|---|---|---|---|
| $t_{CLK1-MUXO1}$ | 133ps | 110ps | 95ps |

Table 4.1: CLK1 to MUXO1 delay at different PVT corners.

# Chapter 5

# Result and Conclusion

The chip is designed and manufactured in UMC28nm process. Since the chip is still under testing, only simulation data is presented here. A table that compares this work with the previously implemented LPTV RC filter is shown in Figure 5.1. The main improvements over the past design in [1] is the wider scanning range and >15dB better stopband attenuation due to RTI RDAC switching technique.

| | Technology | Scanning Range | Stopband Attenuation | Supply | Power |
|---|---|---|---|---|---|
| [1] | 65nm | 0-1Ghz | 40dB | 1.2V | 8mW |
| This Work | 28nm | 0-3Ghz | 58dB | 0.9V | 10.5mW |

| | Spurious Image | Analog RBW | Sensitivity | Area | |
|---|---|---|---|---|---|
| [1] | -24 | 10Mhz | <-142dBm/hz | $1.68mm^2$ | |
| This Work | -25 | 30Mhz | <-142dBm/hz | $1.06mm^2$ | |

Figure 5.1: Comparison table between this work and prior art.

Frequency response of the filter is simulated with extracted parasitic capacitors added to the schematic. Both LPF and BPF with different center frequencies are tested. Figure5.1 shows the frequency response of a LPF and figure 5.2, 5.3 show the frequency response of BPFs. Both LPF and BPF show >58dB stopband attenuation. The spurious image is not improved because RTI switching RDAC changes equivalent resistance and creates LO's harmonics terms.

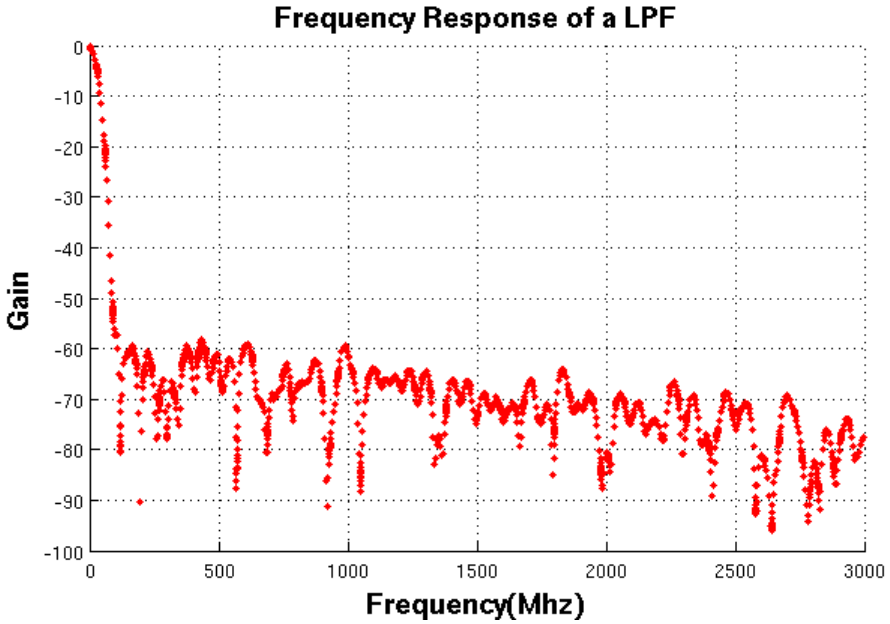



Figure 5.2: Frequency response of a LPF.

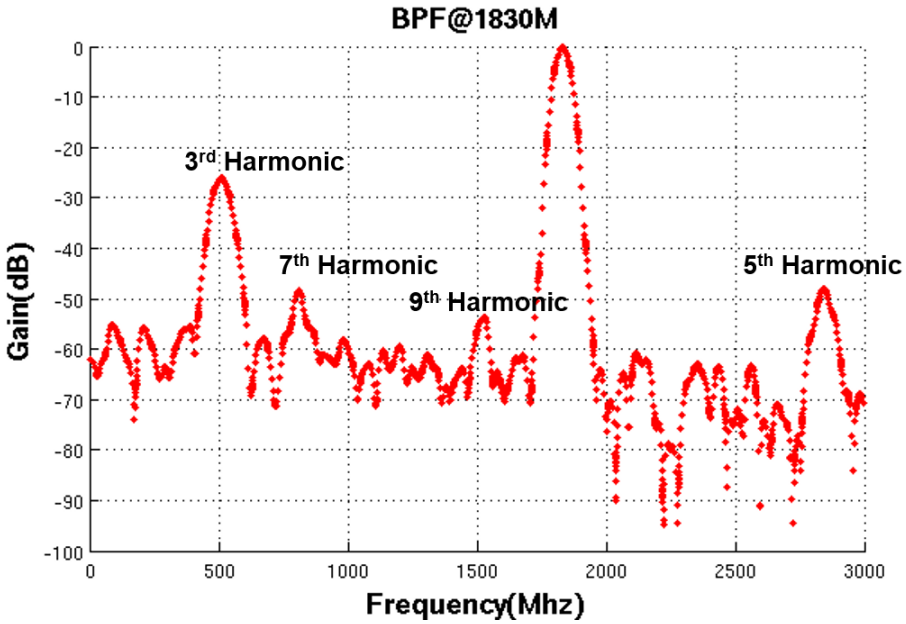



Figure 5.4: Frequency response of a BPF@1830MhZ

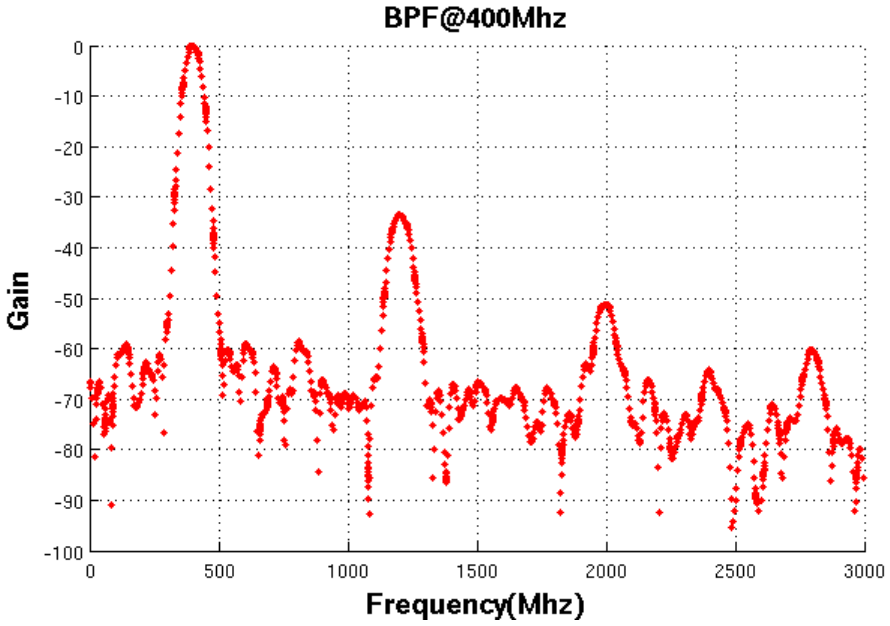



Figure 5.3: Frequency response of a BPF@400Mhz.

The lay out of the chip is shown in Figure 5.4.

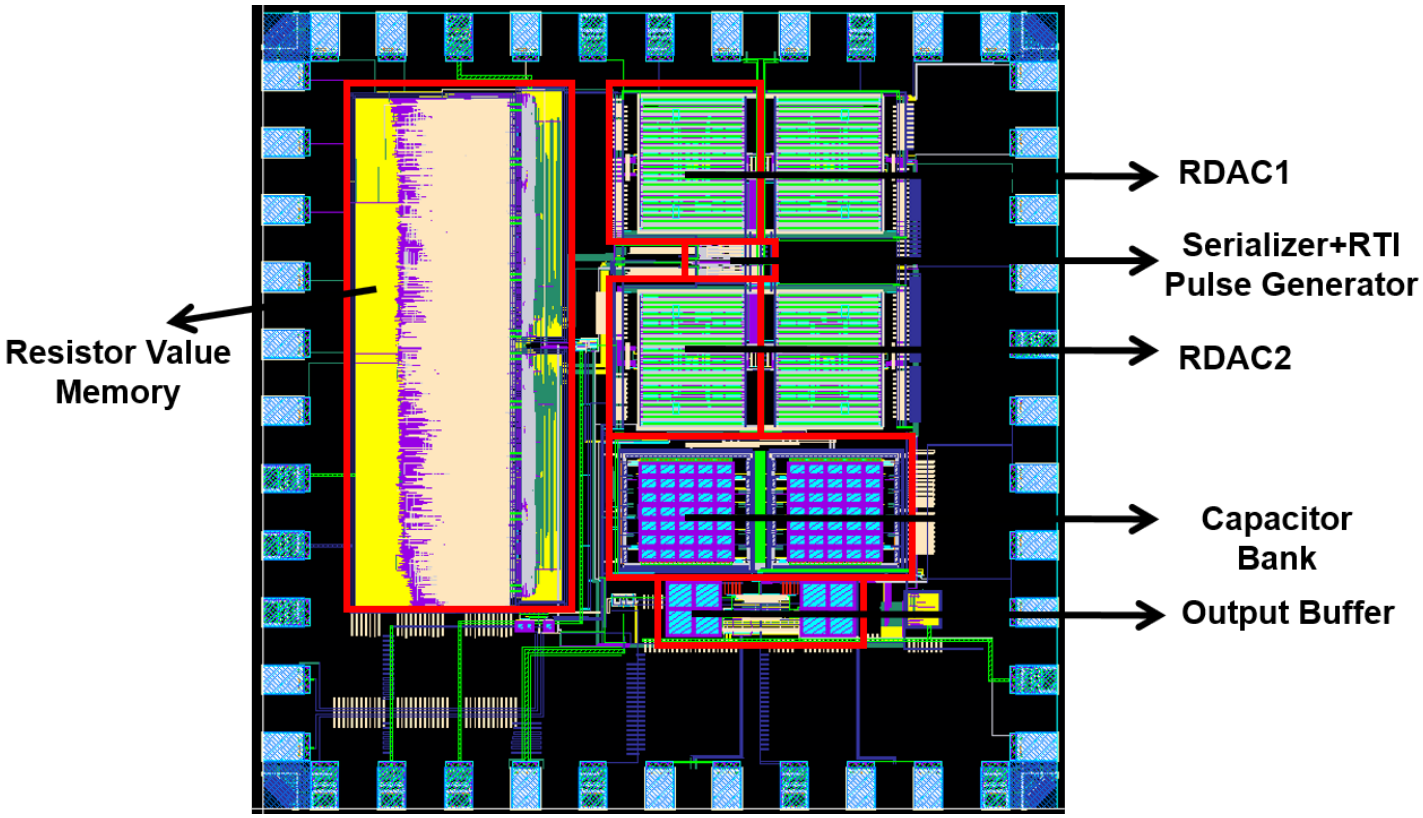



Figure 5.5: Lay out of the chip.

**Conclusion and Future Work**

Previous implementation of a spectrum analyzer using sampled LPTV circuit suffers from degradation of stop band attenuation because of parasitic capacitors within RDAC. This thesis shows a switch capacitor circuit model to analyze the effect of parasitic capacitors on filter's frequency response. A improved spectrum analyzer with wider scanning range and improved stop band attenuation using RTI switching RDAC is designed and manufactured in umc28nm process. This thesis presents the circuit design of the chip.

The RTI technique removes $C_1$'s influence on stop band attenuation. However, the technique does not suppress the harmonic spurs. The future work could explore the way to solve the problem of harmonic rejection.

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