Title
Integrated Process and Characterization for Defect-free Copper Electroplating of Through Wafer Vias (TWVs)

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Integrated Process and Characterization for Defect-free Copper Electroplating of Through Wafer Vias (TWVs)

A thesis submitted in partial satisfaction of the requirements

for the degree Master of Science

in Materials Science and Engineering

by

Ko-Ching Hou

2020

ABSTRACT OF THE THESIS

Integrated Process and Characterization for Defect-free Copper Electroplating of Through Wafer Vias (TWVs)

by

Ko-Ching Hou

Master of Science in Materials Science and Engineering

University of California, Los Angeles

Professor Subramanian S. Iyer, Chair

One of the most important packaging techniques is copper electroplating. A successful electroplating, whether for back-end-of-line (BEOL) interconnects or packaging applications, depends on finding the right additives for increasing plating quality or bottom-up fill, maintaining a stable bath composition and minimizing the impurity level in the plated copper. When it comes to changes in new barrier layer, seed layer and aspect ratio, challenges arise as the process flow becomes much more complicated.

In silicon interconnect fabric approach, we aim to replace traditional printed circuit board (PCB) by silicon substrate. With silicon substrates, not only can we achieve high interconnect density but also high-power applications since silicon possesses outstanding thermal properties comparing with organic substrates such as PCB. However, a dense die integration requires a high-power delivery (0.7-1W/mm^2) and generates a huge amount of heat (0.5-0.7W/mm^2). The power delivery through periphery I/O is not able to supply such a great amount of power (more than 50kW on 12-inch wafer).

As a result, power has to be distributed using through wafer vias (TWVs). An excellent copper electroplating process during the fabrication is a critical process since a good quality of plating provides lower IR drops and lower heat losses. In this thesis, we develop through wafer vias (TWVs) for Si-IF to deliver the power from the back of Si-IF to the front side of the wafer which can be used for potential wafer-scaled integration or attached with power delivery/cooling system.

In this work, we first demonstrate the characterization of copper electroplating process including the uniformity test and surface roughness measurement. Then we move on to the development of a reliable fabrication flow of TWVs for Si-IF that enables 3D integration packaging.

This thesis of Ko-Ching Hou is approved.

Dwight C. Streit

Mark S. Goorsky

Subramanian S. Iyer, Committee Chair

University of California, Los Angeles

2020

Acknowledgement

I would like to take this opportunity to thank Professor Subramanian Iyer for his education. I am really grateful that Professor Iyer has given his biggest support to me since the first day I joined this lab. Without his help, my research would become impossible. Additionally, I would like to thank Arpan Dasgupta and HaoXiang Ren who are both my colleagues in UCLA CHIPS for their assistance and guidance. I am also sincerely thankful to all members at UCLA CHIPS for providing me new ideas whenever I encountered problems. I would also like to thank Chuck Hirbour at Technic Inc for his generous help to supply us the chemicals for copper electroplating. Furthermore, I would also thank my committee for their help to review the thesis.

Finally, I am grateful to my family for their love and support.

Table of Contents

List of Figures

List of Tables and Charts

Chapter 1 Introduction

Semiconductors are the foundation of electronic industry. These partially conductive devices include chips, transistors and other electronic control parts which are integrated to modern equipment such as mobile phones, cars and robots.

Chips and transistors are all made with semi-conductive materials such as silicon which has characteristics of both conductors and insulators but doesn't fit into either category. To produce these parts, semiconductors must undergo several manufacturing processes:

1. Wafer production: Semiconductors usually starts with a wafer-thin slice. These wafers are produced by heating the materials, molding it, processing it to cut and grinding it to smooth wafers.
2. Deposition: Wafers are heated and exposed to pure oxygen in a diffusion furnace. It produces a thin-film silicon dioxide layer on the surface of the wafers.
3. Patterning and masking: Also called photolithography, this process patterns parts on the thin film or the wafer. With the help of a photosensitive chemical called photoresist, the designed layout can be patterned onto the wafer.
4. Etching: Wafers are baked to harden the photoresist. After baking, wafers are exposed to chemical solution to eat away areas that are not covered by the photoresist
5. Doping: Atoms with one less or one more electron than silicon is introduced into the exposed wafer area to alter electrical properties of silicon. For silicon, these are boron (B) and phosphorous (P) respectively.
6. Dielectric deposition and plating: Devices are connected by metals and insulators. They both protects the circuit and creates a connection between inner workings of semiconductors and the outside world.

Since semiconductors came out, researchers have endeavored searching different metals for back-end-of-line (BEOL) interconnects in the semiconductor industry. This search became more difficult as feature sizes shrink to accommodate Moore's Law [1]. The requirement of an ideal metal used in semiconductors must include low electrical resistance, low power consumption and high reliability.

Aluminum was once a predominant metal since it is cost-effective and highly conductive. Nevertheless, with new technology nodes shrinking into nanometer scales, metals with low resistivity become preferable choices [2][3]. These metals include copper (Cu), tungsten (W), gold (Au) and silver (Ag). Copper emerged as a clear winner since it resulted in a 45% decrease in the overall chain resistance thereby significantly reducing the signal delay. Additionally, improved reliability performance and low cost also make copper a strong candidate to replace aluminum.

Copper electroplating, also abbreviated as ECP or ECD in semiconductor industry, is commonly used in the manufacturing of packages. Copper electroplating is used widely to deposit the copper metallization schemes in IC packages, enabling the electrical connections within the structure. More specifically, copper electroplating helps the deposition of copper in the key interconnect structures including bumps, copper pillars, redistribution layers (RDLs) and through-silicon-vias (TSVs). Each of them is applied for a particular package type and has different challenges to be overcome.

At Center for Heterogeneous Integration and Performance Scaling (CHIPS), University of California, Los Angeles (UCLA), Silicon Interconnect Fabric (Si-IF), a novel packaging technique is developed to achieved broader bandwidth, lower latency and reduced power consumption. The Si-IF is fabricated with traditional BOEL process with copper damascene interconnects but replaces both packaging laminate and printed circuit board (PCB) used in conventional packaging technique [4]. Since the copper interconnects occupy an important position in Si-IF technology, performance scaling of copper electroplating becomes extremely crucial during the fabrication.

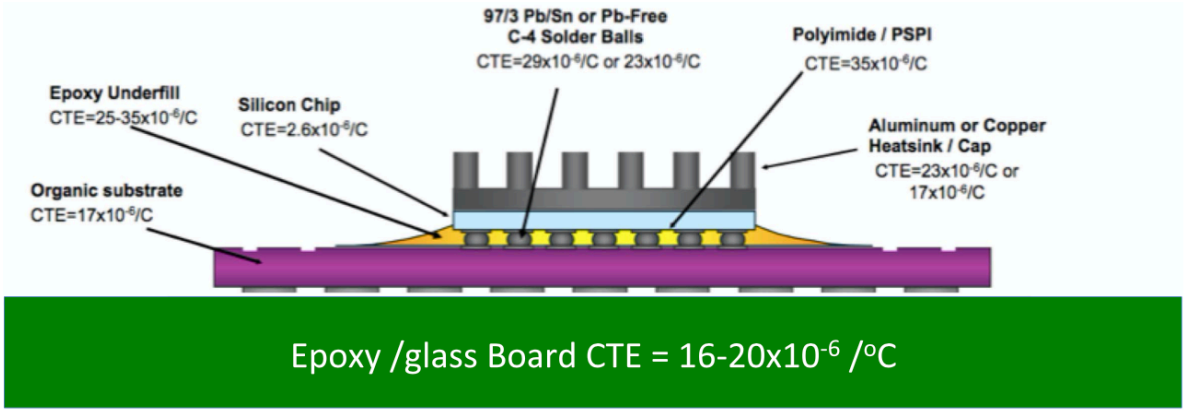

Fig 1.1 Anatomy of a traditional organic package [5].

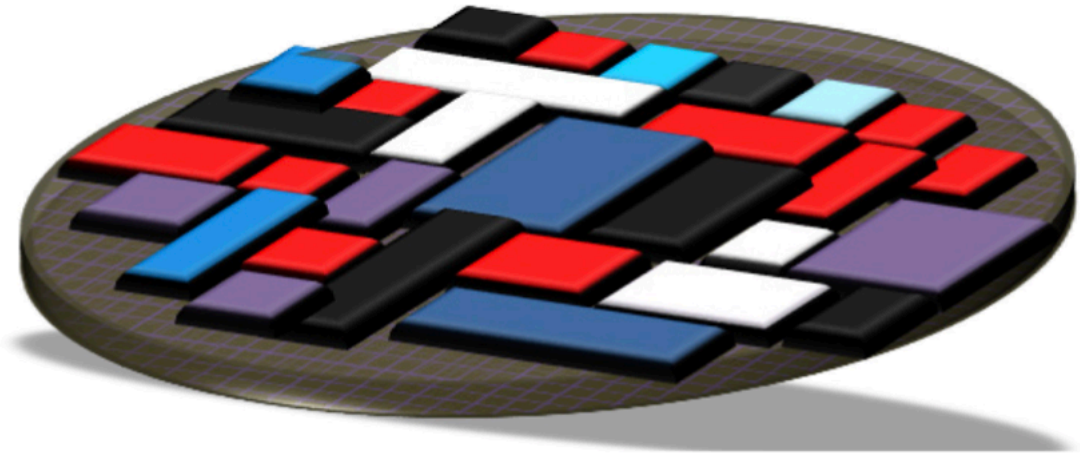

Fig 1.2 Schematic of a Si-IF with mounted dielets [4].

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[1] Moore, G.E. (1965) Cramming More Components onto Integrated Circuits. Electronics, 38, 114-117.

[2] Torres, J. (1995) Advanced Copper Interconnections for Silicon CMOS Technologies. Applied Surface Science, 90, 112-123.

[3] Andricacos, P.C. (1997) Copper On-Chip Interconnections: A Breakthrough in Electrodeposition to Make Better Chips. The Electrochemical Society Interface, 8, 32-37.

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[5] S. S. Iyer, "Heterogeneous integration for performance and scaling," IEEE Trans. Components, Packag. Manuf. Technol., vol. 6, no. 7, pp. 973–982, 2016.

Chapter 2 Background Knowledge

2.1 Copper electroplating

2.1.1 Basic bath setup

The introduction of electroplating into device fabrication has been developed for decades. The advantages of Cu relative to Al for chip wiring includes lower resistance and higher current density [1]. To develop a robust copper electroplating process, the most crucial equipment is the bath. Both chemistry and dynamics reacting in the bath influence the electroplating quality, filling performance and uniformity. The basic setup of a copper electroplating bath requires a bath with copper sulfate, a copper anode, a target metal cathode and a power supply.

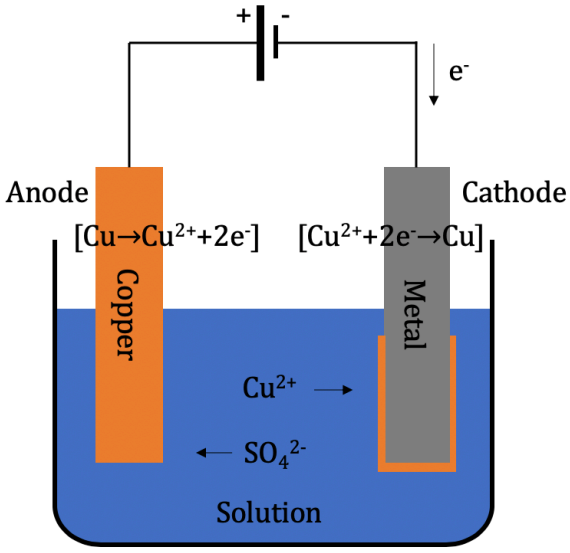


Fig 2.1 Basic setup of a copper electroplating bath.

A basic copper electroplating bath is shown in Figure 2.1. The full reaction can be divided into two parts: the current flow part and the ions flow part. For the current flow part, electrons leave from the anode and enter the cathode. Electrons leave the copper anode and thus induces the copper oxidation Cu → Cu^{2+}+$2e^-$ whereas electrons flow into the metal cathode, inducing the copper reduction Cu^{2+}+$2e^-$ → Cu and bring about the thin film copper deposition. For the ions flow part, it happens in the chemical bath. It helps replenish and balance the electrical difference causes by the current flow. As the electrons flow away from the copper anode, it leaves cuprous ions (Cu^{2+}) into the bath. Sulfate ions (SO_4^{2-}) are attracted by the positive charges from the cuprous ions. On the other hand, the electrons

flowing into the anode leave negative charges at the surfaces of the anode. Cuprous ions are attracted by the negative charges and thus form the copper film.

2.1.2 Electrolyte

To improve the overall performance for copper electroplating, not only do we make some adjustment of the electrolytes we used in the bath, we also add more additives to achieve specific electroplating chemistry. The electrolytes we use generally consist of sulfuric acid (H_2SO_4), hydrogen chloride (HCl) and copper sulfate ($CuSO_4$). Both sulfuric acid and copper sulfate improve the overall conductivity contribution and charges balancing whereas hydrogen chloride gives a relatively complexed chemical reaction. We will discuss hydrogen chloride 2.1.3.

2.1.3 Chloride ions

Chloride ions (Cl^-), produced by hydrogen chloride, plays a crucial role in the via-filling performance and electroplating quality. Chloride ions are mainly added to reduce anodic polarization as well as improve the blocking effect of other additives. The addition of Cl^- promotes copper deposition in the absence of additives [2]. The suppression effect will not only refine the grain size of copper deposited onto the anode, but also enhance the via-filling performance. In the studies of Wei-Ping et al. [3][4], they change the concentration of 3-mercapto-1-propanesulfonate (MPS, brightener) and sodium chloride to improve the filling performance. It was found that by increasing the concentration of brightener in the bath, a higher concentration of chloride is required to achieve a bottom-up filling. The interaction between the additives dictates the CuCl generation that eventually gets accumulated in the via features and undergoes reduction to elemental copper. The work from Min et al.'s [5] related to another brightener bis-(3-sodiumsulfopropyl) disulfide (SPS) also gave a similar result as Wei-Ping et al. A deposition saturation point is observed when only brighteners are added to the solution. However, the addition of small amount of chloride ions rapidly increase the deposistion rate. This may imply that Cl^- competes or inhibits the excessive adsorption of the brightener. Thus, the copper deposition is enhanced. Shao et al. [6] gave a more comprehensive understanding how chloride ions react during the process. With low concentration of Cl^-, copper deposition occurs with the

adsorption of chloride ions and the subsequent reduction of CuCl. In contrast, at high concentration of Cl^-, localized interfacial concentration causes the inhibition of copper deposition. To sum up, the Cl^- in the plating solution is able to give a bottom-up fill.

2.1.4 Brighteners

Additives also play an important role in copper electroplating. Additives can be divided into three types: brighteners (accelerator), carriers (suppressor) and levelers. Brighteners, usually are organic compounds in semiconductor industry, accelerate the electroplating rate. Common brighteners we used industry are disulfide or thiol-based compounds such as 3-mercapto-1-propanesulfonate (MPS) or bis-(3-sodiumsulfopropyl) disulfide (SPS) [7]. In general, brightener molecules are smaller than carriers. As a result, brighteners usually diffuse faster during electroplating process and thus enhance electrodeposition and bottom-up deposition.

In Philippe et al. [8], they discussed about 5 different reactions including (1) copper comproportionation, (2) redox reactions with SPS, (3) adsorption, (4) exchange reactions and (5) complexation that may impact copper deposition during electroplating process using only brighteners. Redox reactions with SPS are the main reaction that involves with brighteners. As shown in the equations below, there are two possible pathways to form elemental copper deposition, namely the electrochemical reduction of SPS to MPS and subsequent formation of Cu-thiolate complex or direct reaction with SPS.

$$SPS + 2H^+ + 2e^- \rightleftharpoons MPS$$

$$2Cu^{2+} + 4MPS \rightleftharpoons 2Cu(I)(thiolate)_{ad} + SPS + 4H^+$$

$$4Cu^+ + SPS \rightleftharpoons 2Cu^{2+} + 2Cu(I)(thiolate)_{ad}$$

2.1.5 Carriers

As mentioned above, carrier molecules are larger than brightener molecules to enable accumulation. Carriers we used commonly are polymers with high molecular weights such as polyethylene glycol (PEG). In the work of Wei-Ping et al. [9], different molecular weight of PEG were added into the bath to test the filling performance. As indicated in Fig 2.2, two different vias were

tested with different molecular weight of PEG. The filling performance is the best when PEG Mw is between 6000 to 8000 g/mol. When PEG Mw is larger than 8000 g/mol, the drop extent for filling performance is larger in big via. It suggests that the fluid motion acts easily in big via comparing with small via. As a result, the inhibition effect of copper deposition is much more obvious at the bottom of the via.

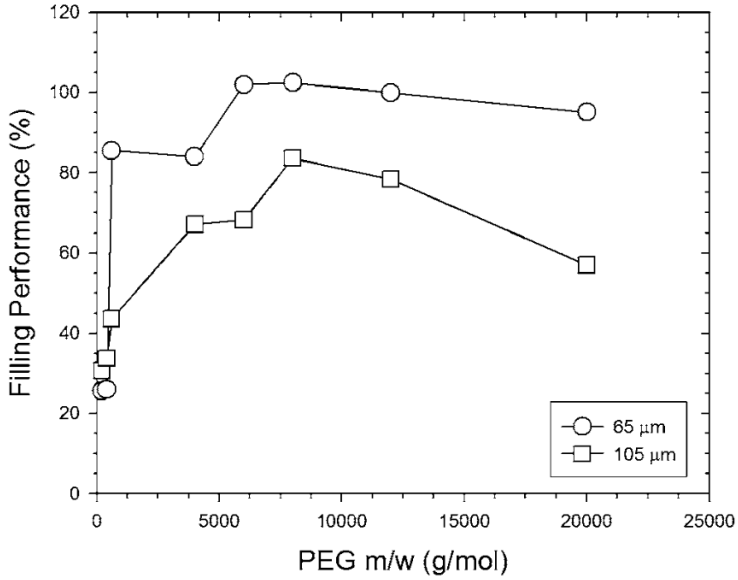


Fig 2.2 Relationship between molecular weight of PEG and filling performance [9].

2.1.6 Levelers

So far, we have discussed about the brighteners' and carriers' effect on copper electroplating. Numerous experimental and theoretical studies demonstrated that the "bottom-up" filling is achieved by preferential adsorption of accelerating species or suppressing species on the wafer surface. However, copper will continue to grow at a rapid rate to the adjacent field. In other words, excessive copper might form across the die. The excess copper layer (copper overburden) over the patterns might increase the difficulty of the copper removal by using chemical mechanical polishing (CMP). As a result, levelers become an important character to reduce the copper overburden.

Leveler or leveling agent normally has a nitrogen functional group and is added to the bath at a relatively low concentration. Similar to the carriers, the adsorption rates and mass transfer characteristics of levelers are crucial parameters to be considered. In J. Zhou and J. Reid's work [10],

they discussed about the impact of a model leveler, polyvinylpyrrolidone (PVP) at molecular weight from 3,500 to 1,300,000 on damascene bottom-up fill rate and leveling behavior of different PVP concentration. The partial fill rate discussed in the article is measured with brightener-carrier only solution used as baseline (unity). PVP at molecular weights of 3,500, 10,000 and 29,000 decreased the efficiency of bottom-up fill even as solution concentration was increased. This behavior suggested that all PVP molecules were diffused into the via, leading to a full suppressing effect of bottom-up fill. At 55,000 molecular weight, the fill rate is enhanced at 5mg/L concentration but decreased at 20mg/L concentration. This behavior reflects the reduced diffusion of PVP at this molecular weight. However, at 1,300,000 molecular weight, the partial fill rate is enhanced at all concentration, indicating there is limited diffusion of PVP into the via to cause leveling effect.

2.1.7 Filling mechanism

Filling mechanism is a crucial factor when conducting copper electroplating experiments. In

general, filling mechanism can be divided into three types as shown in Fig 2.3 [1]: (1) subconformal filling (void-defect filling), (2) conformal filling (seam-defect filling) and (3) superfilling (defect-free filling).

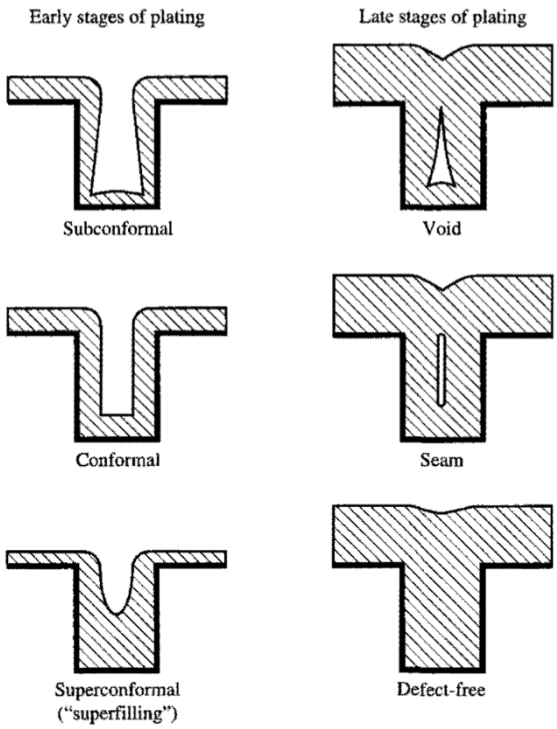
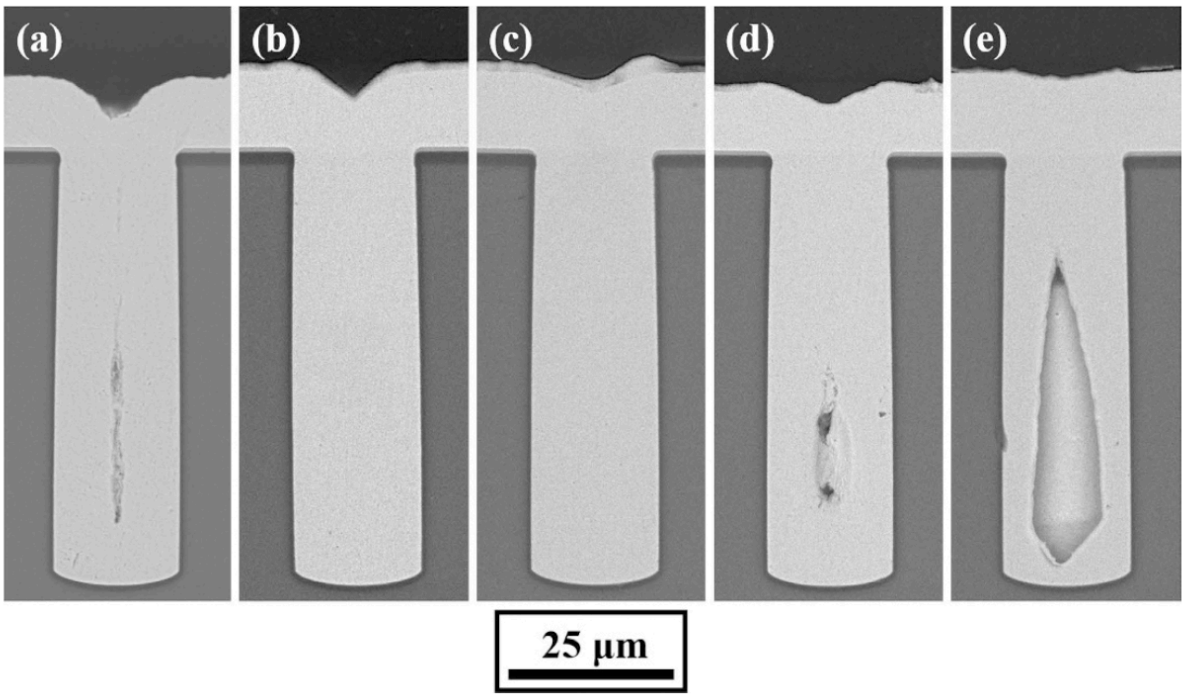


Fig 2.3 Different types of copper electroplating [1].

To achieve a defect-free copper filling, a superfilling mechanism is required. Since there are less carriers at the bottom of the via because of the huge molecular size comparing with brighteners, the deposition rate at the bottom of the via is larger than the top of via is an ideal condition for superfilling. Superfilling is affected by several parameters such as bath chemistry, seed layer quality and current density. As mentioned above, the concentration and chemistry of the chloride ions and additives can largely affect the filling performance. Additionally, in Wang, F et al.'s work [11], dynamic via-filling process is investigated under different current density. Under low current density, the overall deposition rate is low and the copper ions and additives have sufficient time to diffuse to the bottom. Thus, brighteners and carriers are both adsorbed and a uniform deposition rate is found at sidewalls, the bottom and the top. This results in a conformal filling that might generate a seam in the via at the end of the electroplating process. However, as the current density increases, increased

deposition rate is found everywhere inside the via but a much higher deposition rate is found at the bottom of the via because the carriers diffuse to the bottom to a smaller extent. Hence, the carriers are gradually replaced by brighteners at the bottom. This leads to a superfilling mechanism since the deposition rate is much faster at the bottom. With high current density, the reaction of copper ions at the bottom could not be replenished in time due to the particularly high deposition rate. This leads to a greater deposition rate at the top of the via and results in a void after the process finishes. To sum up, low current density leads to a seam-defect via, medium current density leads to a defect-free via and high current density leads to a void-defect via. Cross-sectional SEM images are shown in Fig 2.4 of 20x65μm blind-vias with different current density conditions.

Fig 2.4 Cross-sectional SEM images with different average current densities, (a) 4mA/cm^2, (b) 5mA/cm^2, (c) 7mA/cm^2, (d) 10mA/cm^2, (e) 15mA/cm^2 [11].



In Fig 2.5, an ideal “bottom-up filling” or “super-filling” is achieved by controlling the bath chemistry and dynamics to reduce the copper growth on the sidewall and enhance the copper growth at the bottom.

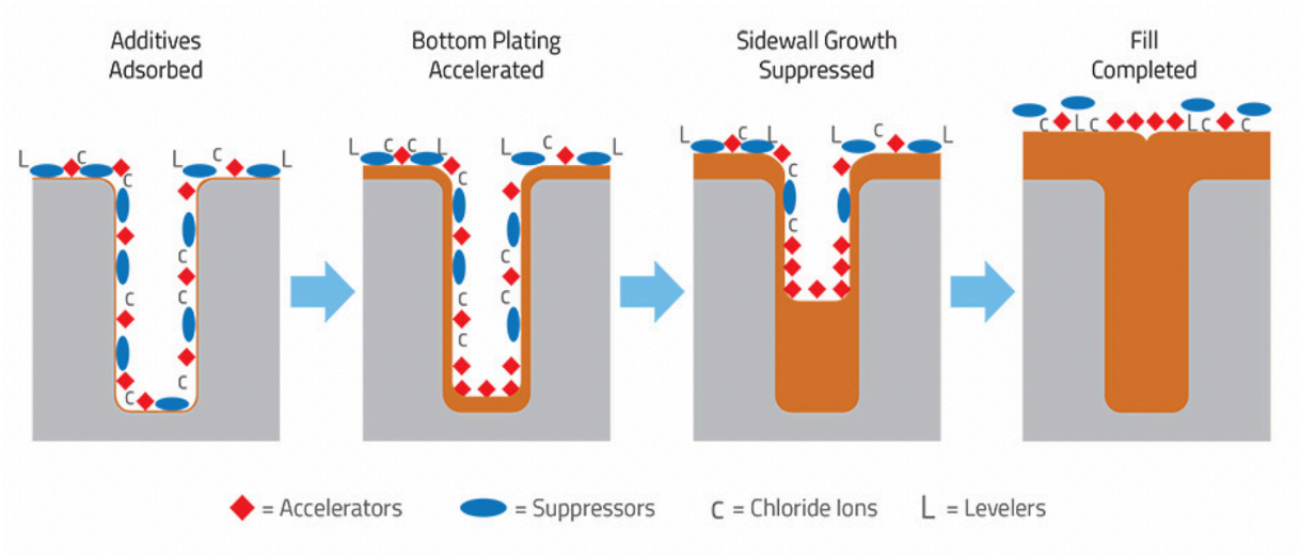


Fig 2.5 Demonstration of copper superfilling with chloride ions and additives.

2.2 Surface morphology

So far, we have known that in order to achieve a bottom-up filling mechanism, the existence of brightener, carrier and leveler are essential. Moreover, the chloride ions also play an important role in the bath to offer functionality to these additives. For a damascene process which we will discuss in 2.3, a copper seed layer is sputtered on the dielectric, namely SiO_2. The grain orientation of the seed layer depends on the underlying material. However, a dielectric layer causes a random grain orientation of the copper seed layer while a metallic layer causes a strong (111) grain orientation. As a result, based on the seed layer orientation, surface roughness might occur after copper electroplating.

According to the work from Tobias Schwarz and Alfred Lechner [12], the surface interaction of the chloride ions which form a direct chemical bond with the metal surface is the key factor that influences the surface roughness. The specific adsorption of chloride ions is influenced by the crystal orientation and the chloride ions can completely block reaction sites on the metal surface. In order to investigate the impact of the specific adsorption of chloride ions on the crystal orientation, surface roughness values were measured under different concentration of chloride ions in the electrolyte. The roughness decreases initially as concentration of Cl^- increases. However, the surface roughness raises linearly as the chloride ion concentration increases further. As a result, the competitive adsorption

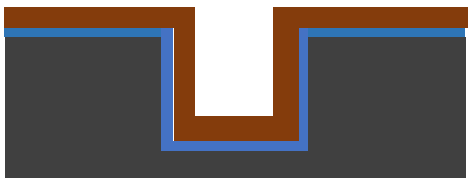
between Cl^- and additives determines the surface morphology after copper electroplating.

2.3 Damascene electroplating

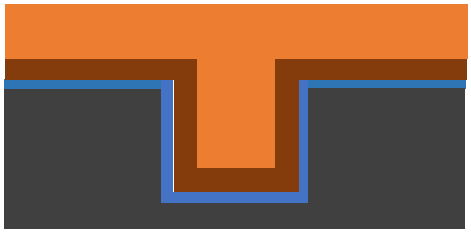
Integrated circuits, used in modern devices, are formed by two essential parts: transistors and interconnects. The transistors perform the logic functions and the copper interconnects provide the wiring between transistors.

The process used by semiconductor industry to fabricate copper interconnects is called the "dual damascene" process. As shown in Fig 2.6, vias and trenches are first etched in a dielectric layer (e.g. SiO_2). After that, a diffusion barrier layer is deposited onto the dielectric layer. Sputter-deposited titanium (Ti), titanium nitride (TiN) or tantalum nitride (TaN) are typically used as a copper diffusion barrier layer. Then, a layer of copper seed layer is sputtered, followed by bottom-up copper electroplating to achieve void-free metallization. Finally, excess copper formed by electroplating process is polished away by using chemical mechanical polishing (CMP). Patterning, copper filling and CMP is repeated sequentially to assemble the multilayered interconnect structure.

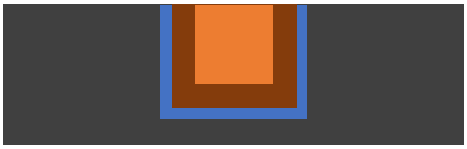
1. Vias etched in SiO_2



3. Diffusion barrier and copper seed deposited



2. Copper electroplated

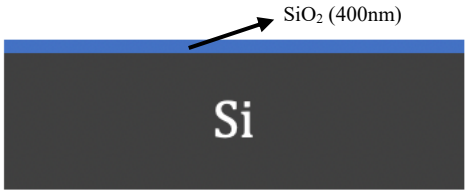


4. CMP of excess copper overburden

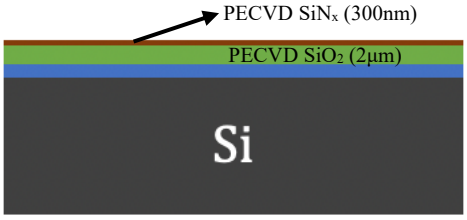
Fig 2.6 Schematic of copper interconnects fabrication flow from patterning, copper filling to chemical mechanical polishing.

2.4 Silicon Interconnect Fabric (Si-IF)

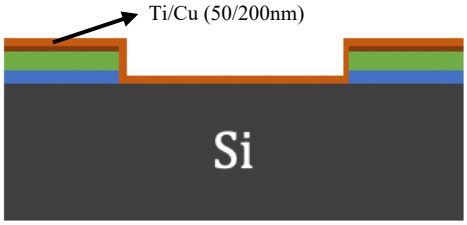
Traditional package methods including system-on-chip (SoC) approach enabled us to increase the functionality of complex chips. However, disadvantages such as chip-package interactions, coefficient of thermal expansion (CTE) mismatch and connection inefficiency still appear. One of the most important technique at UCLA CHIPS is Silicon Interconnect Fabric (Si-IF). Silicon Interconnect Fabric, where we introduced a silicon-based substrate rather than a printed circuit board and packaging laminate, allows us to interconnect dies at fine pitch. The Si-IF is fabricated using traditional back-end-of-line (BOEL) processing with copper damascene interconnects. The wire pitches are in the range of 1-10μm and is terminated with copper pillars of 2-5μm height and diameter. Fine pitch traces (1-5μm) with fine pitch interconnects (2-10μm) and good heat dissipation as silicon substrate are key advantages of Si-IF. The fabrication process of Si-IF is shown in Figure 2.7. In this group, I focus on the improvement of the copper electroplating process in the whole Si-IF fabrication process.



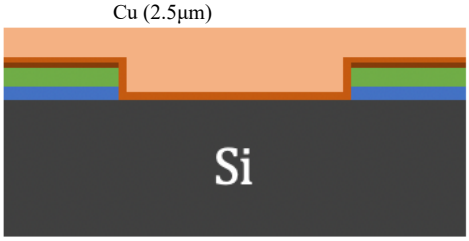
1. Thermal oxidation



2. Insulation and seed layer deposition

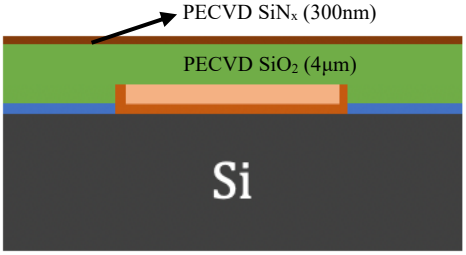


3. Patterning, barrier and seed layer deposition

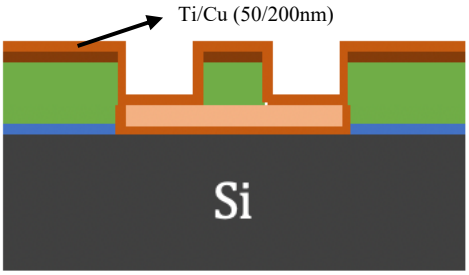


4. Electroplating of first copper layer

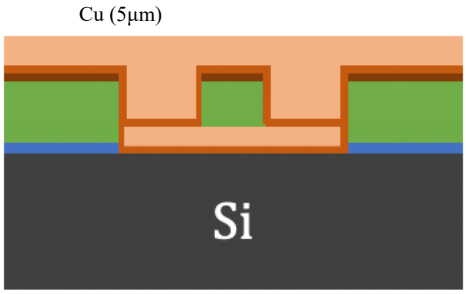
5. CMP of excess first copper layer



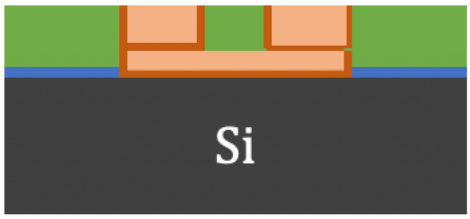
6. Insulation and stop layer deposition



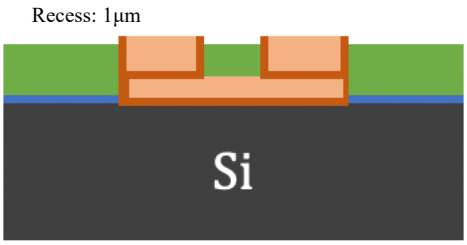
7. Patterning, barrier and seed layer deposition



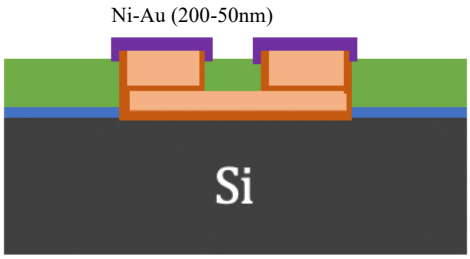
8. Electroplating of second copper layer



9. CMP of excess second copper layer



10. Exposure of copper pillars



11. Electroless plating of Ni-Au

Fig 2.7 Fabrication process of Si-IF.

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Chapter 3 Results and Discussion

3.1 Uniformity test and thickness measurement

3.1.1 Overview and process flow for uniformity and thickness test

In a controlled copper electroplating process, the thickness growth and thickness variation of copper film are critical parameters to investigate. To measure these parameters, we made the copper film into several 1mm x 1mm squares with specific fabrication flow.

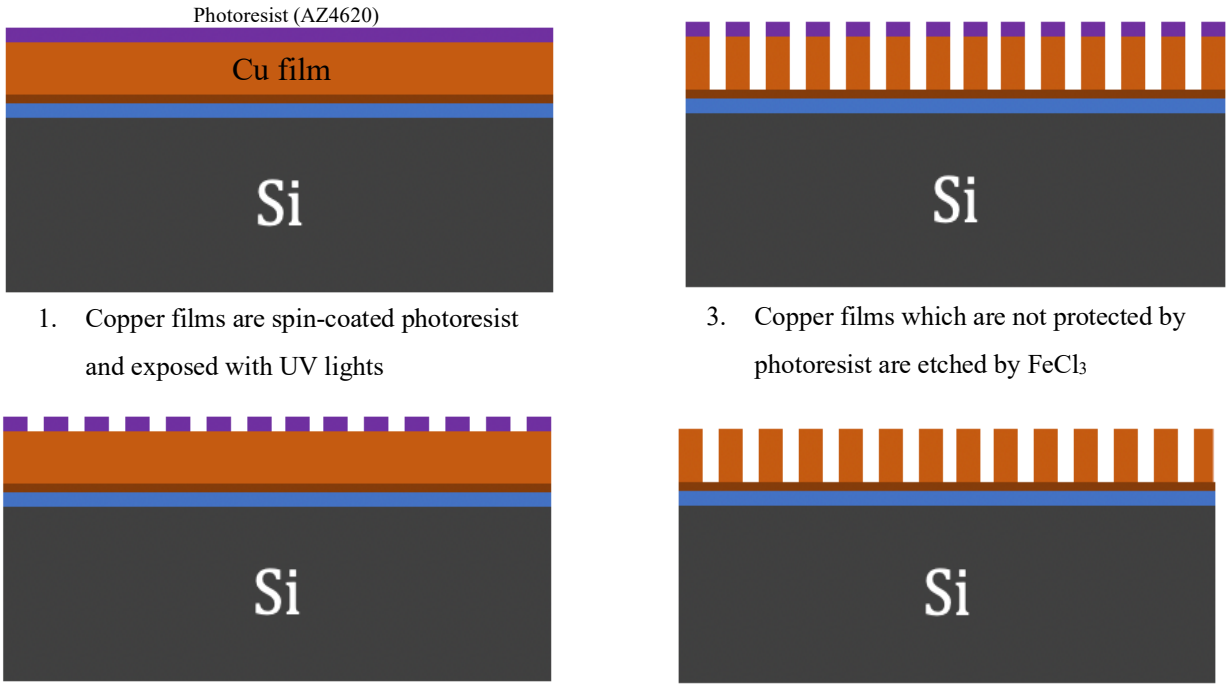
After we operated thermal oxidation inside the furnace to grow 1μm of silicon dioxide layer, we sputtered a titanium layer (barrier layer) and a copper seed layer. The thickness of titanium layer and copper layer are 50nm and 200nm. We then conducted copper film thickness experiment by changing different parameters shown in Table 3.1 that might affect the thickness growth of copper film. Namely, the current and plating time.

	150mA	250mA
30min	0.84μm	2.39μm
45min	1.96μm	3.27μm
60min	2.84μm	3.85μm
90min	4.27μm	6.42μm

Table 3.1 Thickness growth of copper under various current and plating time.

After the copper electroplating experiment is finished, we spin coated the wafer with photoresist AZ 4620, prebaked the photoresist for 1 minute and operated the lithography process with Karl Suss Lithography tool. Lithography process is a photographic process by which a light-sensitive polymer, called a photoresist is exposed and developed to form a 3D relief images on the substrate. In order to remove the photoresist on the exposure sites, wafers are developed with AZ300MIF developer for 5 minutes after they are exposed with UV light. After the developing process, copper films which were

not protected with photoresist were etched with ferric chloride 30% ($FeCl_3$) for 2 minutes. We then removed the rest of photoresist with acetone, isopropanol and DI water. This process allows us to measure the thickness of copper films across the whole wafer with Dektak surface profiler. The process flow of lithography, developing and etching is shown in Fig 3.1. The photos of the mask and the final wafer are shown in Fig 3.2.



1. Copper films are spin-coated photoresist and exposed with UV lights
2. Photoresist film is developed with MIF 300 to remove the exposed photoresist
3. Copper films which are not protected by photoresist are etched by $FeCl_3$
4. The rest of photoresist is washed of and the wafer is ready for thickness measurement

Fig 3.1 Process flow of lithography, developing and etching for thickness experiment.

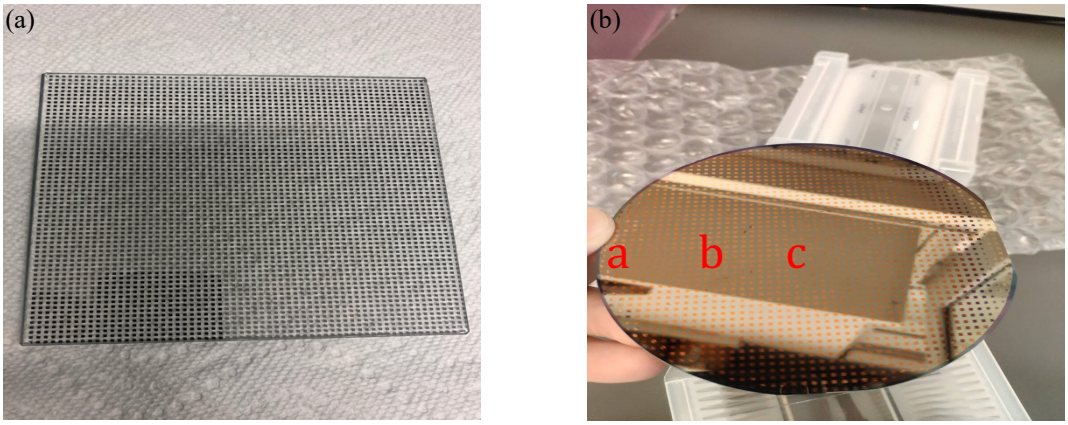


Fig 3.2 Photos of (a) mask for lithography process and (b) final wafer sample.

3.1.2 Results for uniformity and thickness test

With different plating current and plating time shown in Table 3.1, thickness of copper films was measured with Dektak surface profiler. In both sets of experiment, the copper grows linearly as plating time increases. However, there is an abrupt increase of the growth rate when plating time reaches 60 minutes. We assume that as copper film grows to a certain thickness under specific plating current, the copper film increases the conductivity of the whole plating process. As a result, the growth rate increases abruptly. The results are shown in Chart 3.1 for 150mA plating current and Chart 3.2 for 250mA plating current respectively.

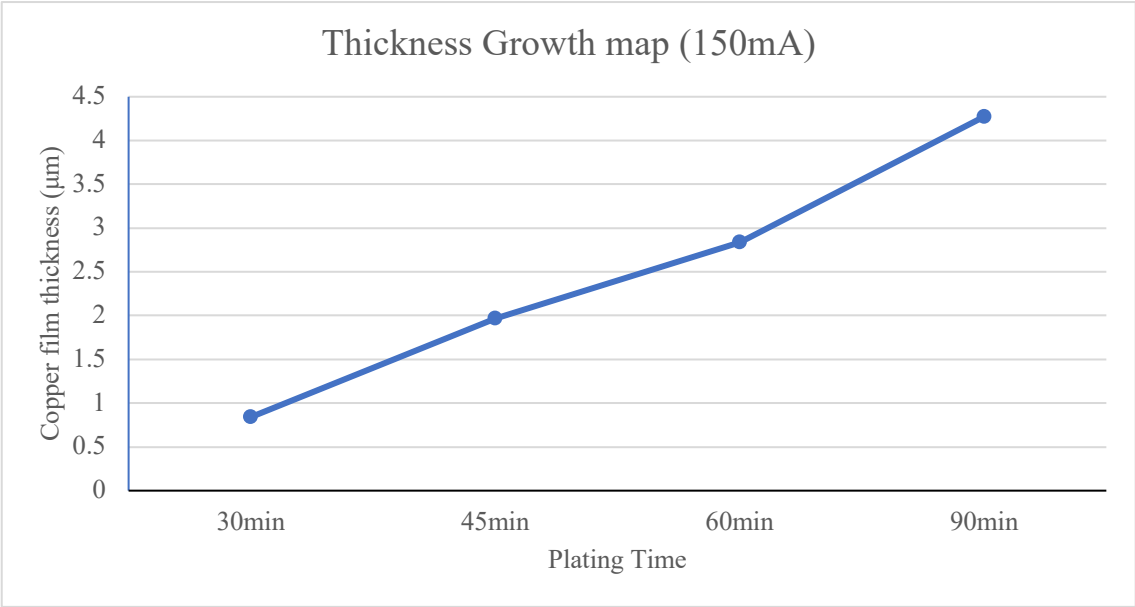


Chart 3.1 Copper thickness growth map for 150mA plating current.

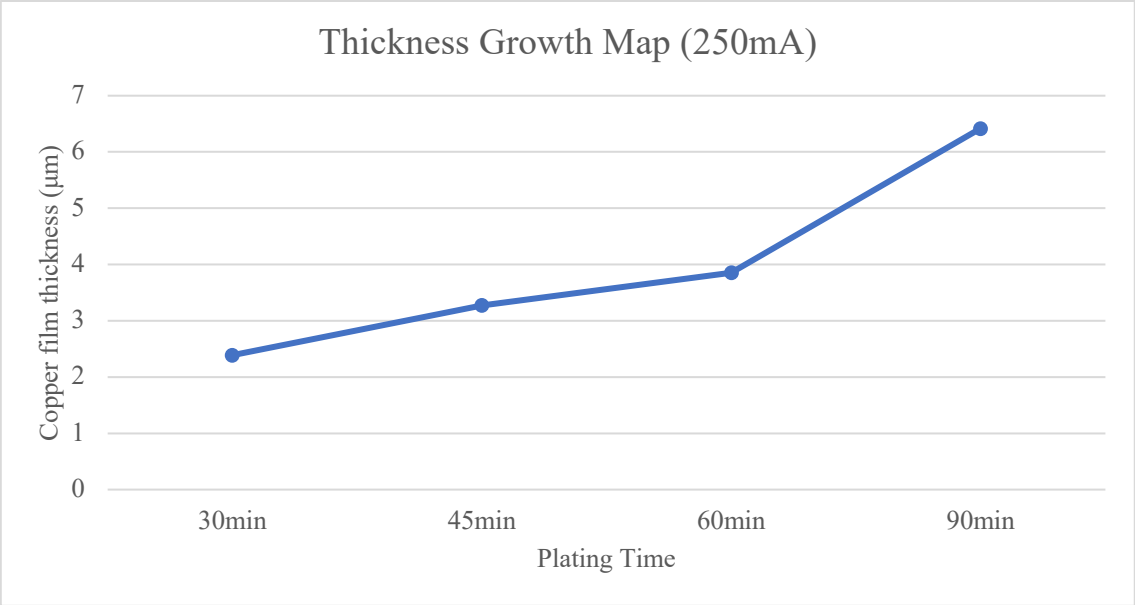


Chart 3.2 Copper thickness growth map for 250mA plating current.

In addition to the thickness growth map of different plating current, we also investigated the individual thickness variation of a single wafer, namely the uniformity test. We assigned three different areas of wafer as shown in Figure 3.2 (b), (a) the edge part, (b) the middle part and (c) the center part. Five measurements were conducted at each part thus there are 15 measurements for each wafer. In Chart 3.3, since the current inputs from the edge of the wafer to the center of the wafer, it is obvious that the thickness difference between edge and center (|a-c|) is larger than the thickness difference between the middle and the center (|b-c|). In addition, the difference between |a-c| and |b-c| becomes larger as the plating time increases. Since as plating time increases, the copper film grows at the edge of the wafer much faster than the center because the edge is much closer to the input of power.

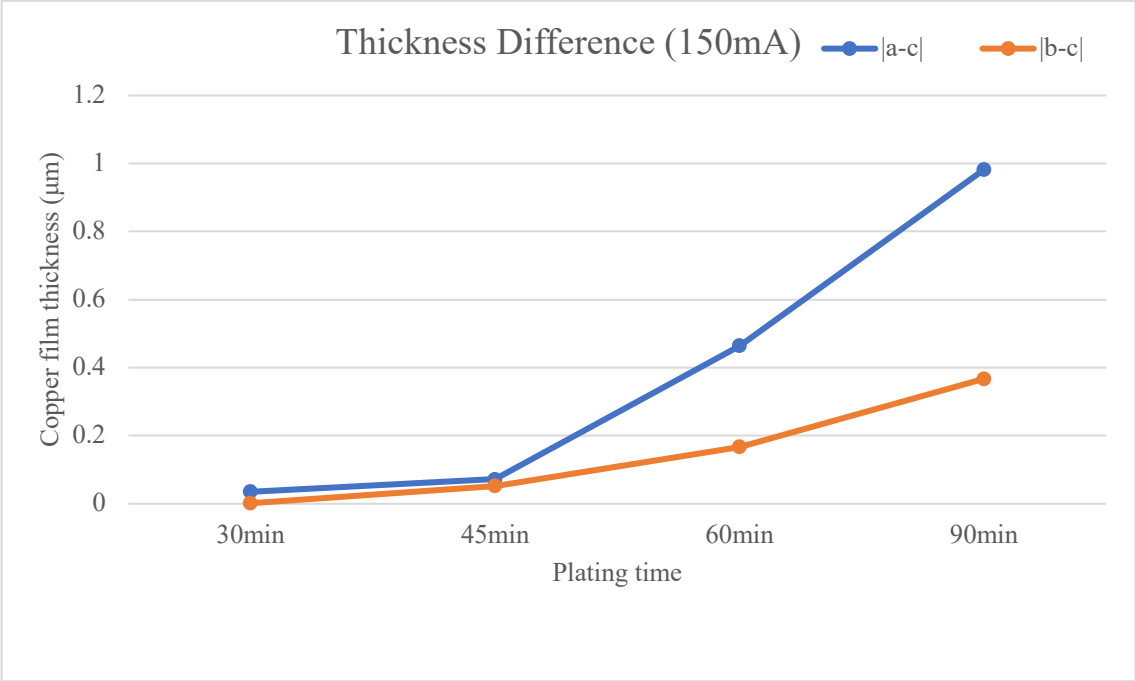


Chart 3.3 Copper thickness difference map under plating current 150mA. |a-c|: the thickness difference between the edge and the center, |b-c|: the thickness difference between the middle and the center.

In general, the average copper thickness increases 1μm every 30 minutes under plating current 150mA. We did not use 250mA as plating current because we discovered burning effect which gives extremely dark brown films. The copper thickness difference between the edge and the center is around 1μm under a 5μm film. The overall uniformity is still a problem that needs to be solved in the future work.

3.2 Characterization of Surface Roughness

3.2.1 Overview and process flow for surface roughness characterization

In addition to the uniformity experiments abovementioned, in order to achieve a better understanding of surface profile, we also conducted microscope inspection and atomic force microscope (AFM) measurement and included both results in this thesis.

For the fabrication flow, we first started with the furnace thermal oxidation to grow 3μm of SiO_2 which serves as an electrical insulation layer. Next, a 50nm layer of titanium adhesion layer and a 200nm of copper seed layer is sputtered on the SiO_2. Then, we move onto the copper electroplating step. Finally, we spin coated the wafer with photoresist AZ 4620 as protection layer for the electroplated copper film to prevent contamination when we diced the wafer. The fabrication flow is shown in Fig. 3.2.

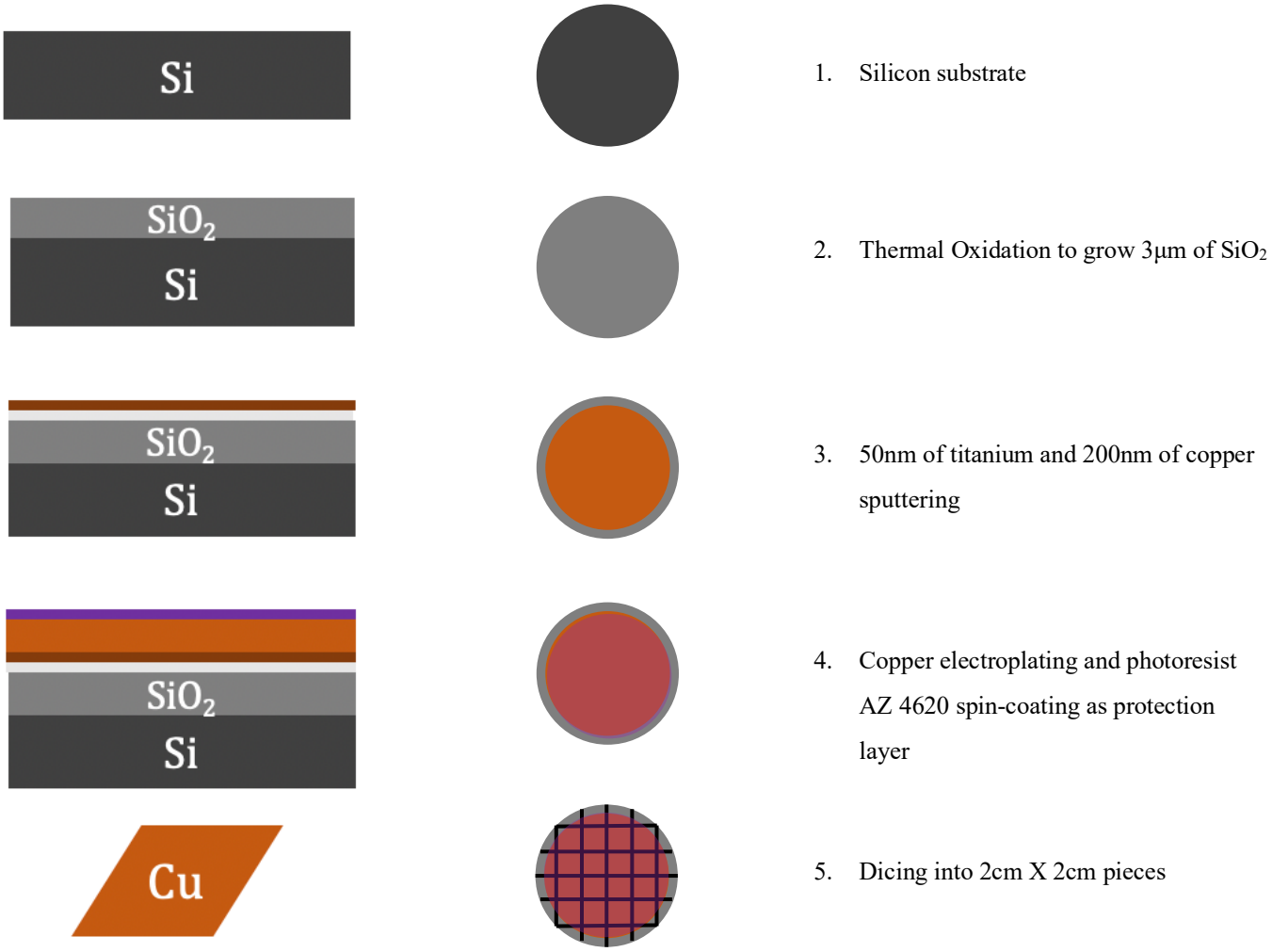


Fig 3.2 Fabrication flow of surface roughness experiment.

3.2.2 Results for surface roughness characterization

In a traditional Cu damascene electroplating process, the chemical bath requires brighteners and carriers as additives and $CuSO_4$, H_2SO_4, HCl as electrolyte. For the brighteners, typically consist of bis(3-sulfopropyl) disulfide (SPS) and 3-mercapto-1-propanesulfonate (MPS) [10], enable a uniform current density at the interface of $CuSO_4$ electrolyte and the sidewall of via. On the other hand, the carriers usually consist of polyethylene glycol (PEG) or polyalkylene glycol (PAG) that create a diffusion layer at the anode to suppress the electroplating rate [11]. In our experiment, we started with virgin makeup solution which only possesses electrolyte without any additives. As shown in Fig 3.3(a), under 250mA of plating current and 30 minutes of plating time, we got a coarse copper film. However, after the addition of additives including both brighteners and carriers without changing plating current and plating time, the copper film became much smoother and the plating quality becomes better as shown in Fig 3.3(b). After we even lowered the plating current to 150mA, an extraordinary of plating quality is achieve under optical microscope observation as shown in Fig 3.3(c).

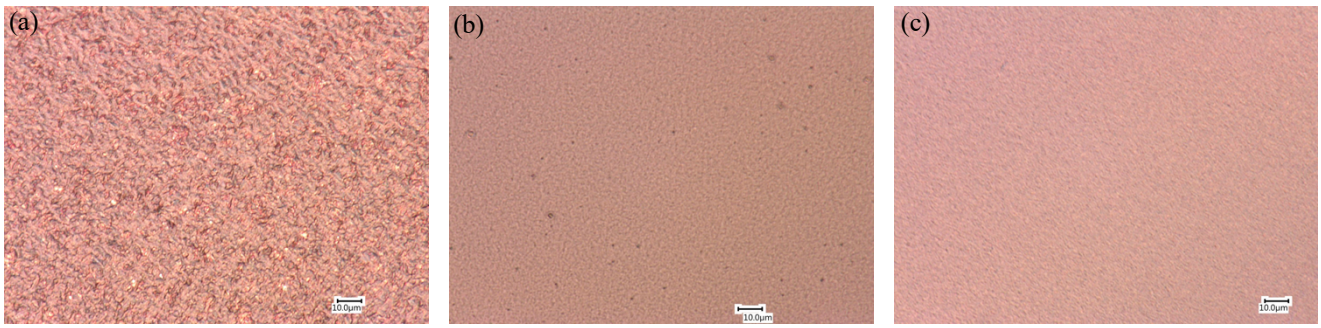


Fig 3.3 Images of optical microscope of (a) virgin makeup solution under 250mA plating current and 30 minutes of plating time (b) addition of additives within the virgin makeup solution under 250mA plating current and 30 minutes of plating time and (c) addition of additives within the virgin makeup solution under 150mA plating current and 30 minutes of plating time.

We also adjusted the surface roughness with different plating time under fixed concentration of brighteners and carriers (both are 7ml/L of electrolyte) and fixed plating current (150mA). In Fig 3.4, as plating time increased, the surface became rougher.

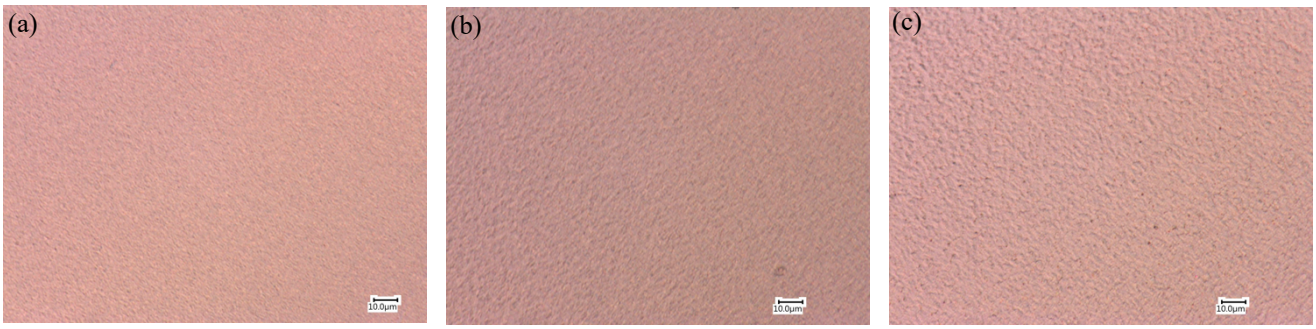


Fig 3.4 Images of optical microscope of (a) 30 minutes of plating time (b) 60 minutes of plating time (c) 90 minutes of plating time under fixed concentration of additives and fixed plating current.

After optical microscope observation, we diced the wafers into 2cm X 2cm pieces and performed topology characterization under AFM. AFM uses a cantilever with a very sharp tip to scan over a sample surface. The deflection towards or away the surface by the cantilever is detected with a laser beam. By scanning the cantilever over a region of interest, the topography of a sample surface can be imaged. Fig 3.5 shows the AFM images with different plating time under fixed concentration of additives (brighteners and carriers) and fixed plating current. As plating time increases, the average surface roughness becomes higher which matches the results in Fig 3.4. In addition, the resolution of AFM images become lower due to the increase of average roughness.

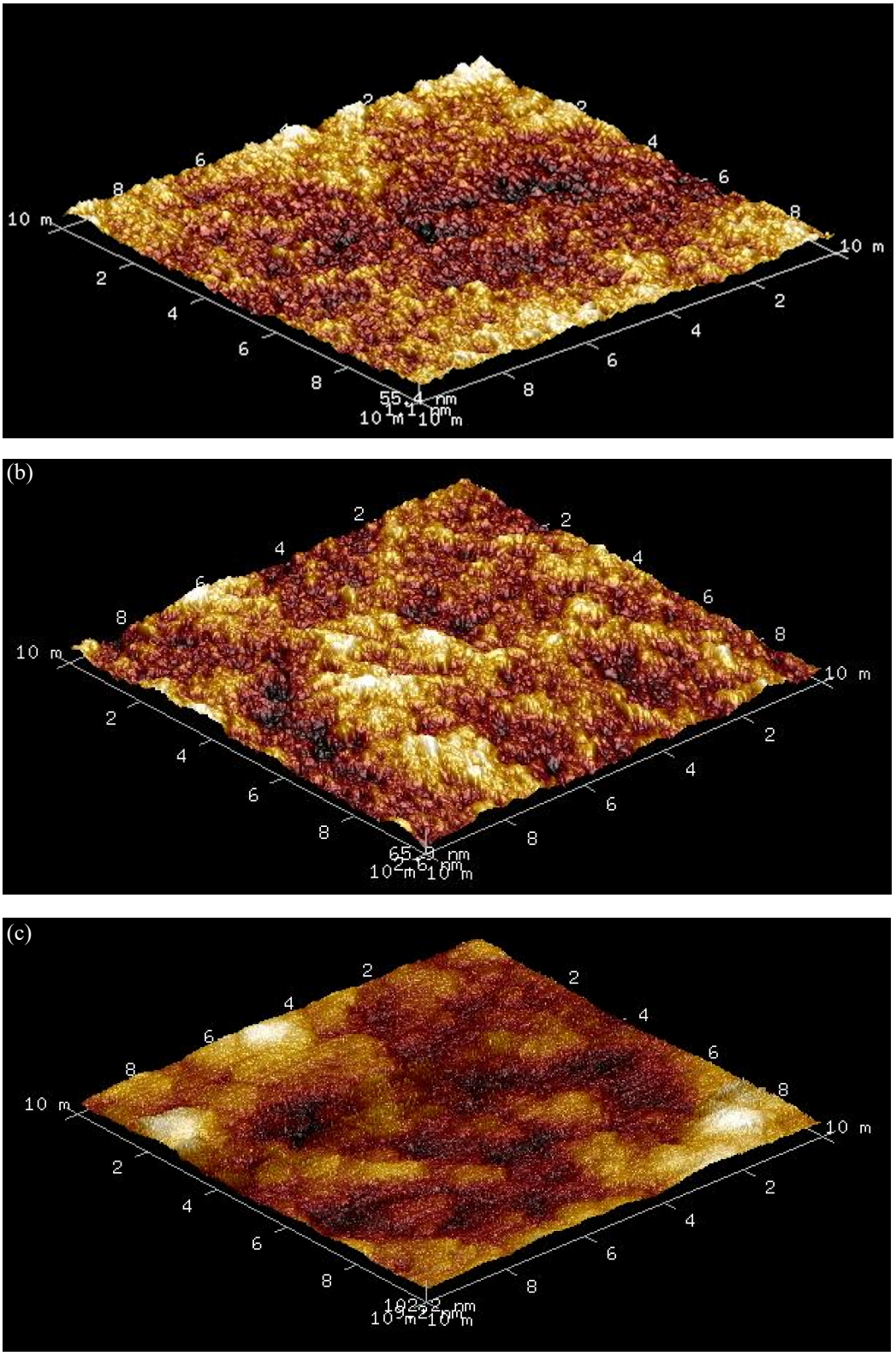


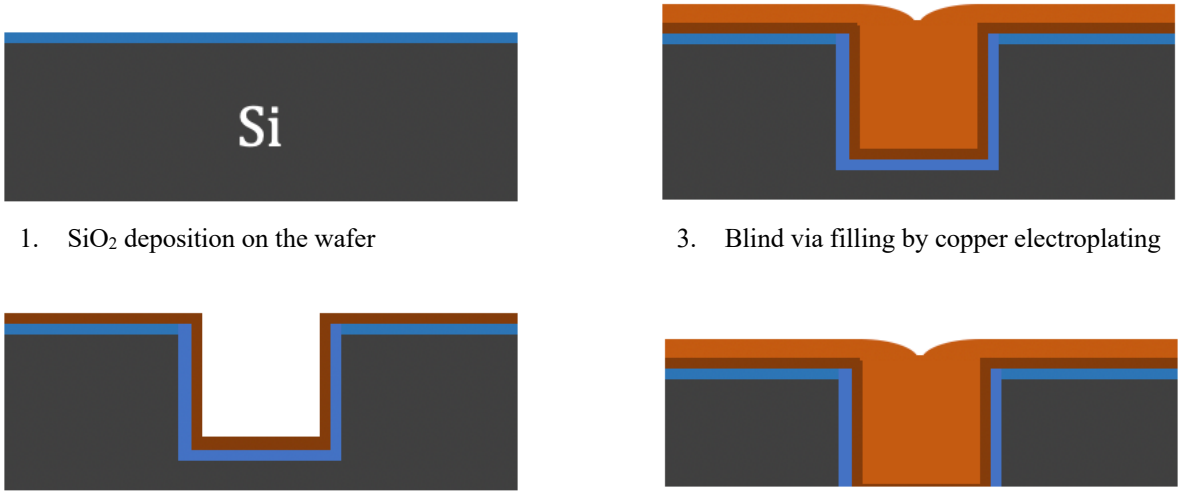
Fig 3.5 AFM images and topography of wafers after electroplating for (a) 30 minutes (b) 60 minutes (c) 90 minutes. Each average roughness (R_a) is (a) R_a=13.0nm (b) R_a=15.2nm (c) R_a=21.2nm.

3.3 Through-wafer via (TWV) fabrication and characterization

3.3.1 Overview of TWV

Through-wafer via (TWV) or through-silicon via (TSV) is a vertical electrical connection that passes completely through a silicon wafer or die. TWVs are high-performance interconnect technique that is regarded as alternatives to wire bond or flip chips to create 3D packages [1,2]. In silicon interconnect technique, traditional TWVs are not suitable for the structure because traditional TWVs only offer 50~100μm wafer thickness that might cause overall instability after we place dies onto wafers. As a result, a large-scale TWVs are required to fabricate to fit Si-IF design.

In traditional TWVs process flow, two common fabrication processes are blind via process and through via process. In a conventional blind via process [3], it includes via-drilling, seed layer deposition, via-filling by copper electroplating and wafer thinning. One of the most critical problems might arise during blind via process is the via-filling process. As you can see in Fig 3.6, as aspect ratio of the via goes higher, blind via filling becomes more challenging since the electroplating rates at the via bottom, the via sidewall and the wafer surface have to be well controlled in order not to induce voids or seams trapped inside the via.



1. SiO_2 deposition on the wafer
2. Via drilling at active side and seed layer deposition
3. Blind via filling by copper electroplating
4. Backside wafer thinning

Fig 3.6 Traditional blind via process flow of TWVs.

Another method to fabricate TWVs is through-via process. Traditional through via process also includes via-drilling, seed layer deposition and via filling by copper electroplating [4]. However, the integration of copper electroplating and chemical mechanical polishing (CMP) becomes extremely difficult since copper overburden may exist on both sides of wafer. As a result, either side of wafer might not be a flat surface to proceed CMP process. A process flow of through via process is shown in Fig 3.7.

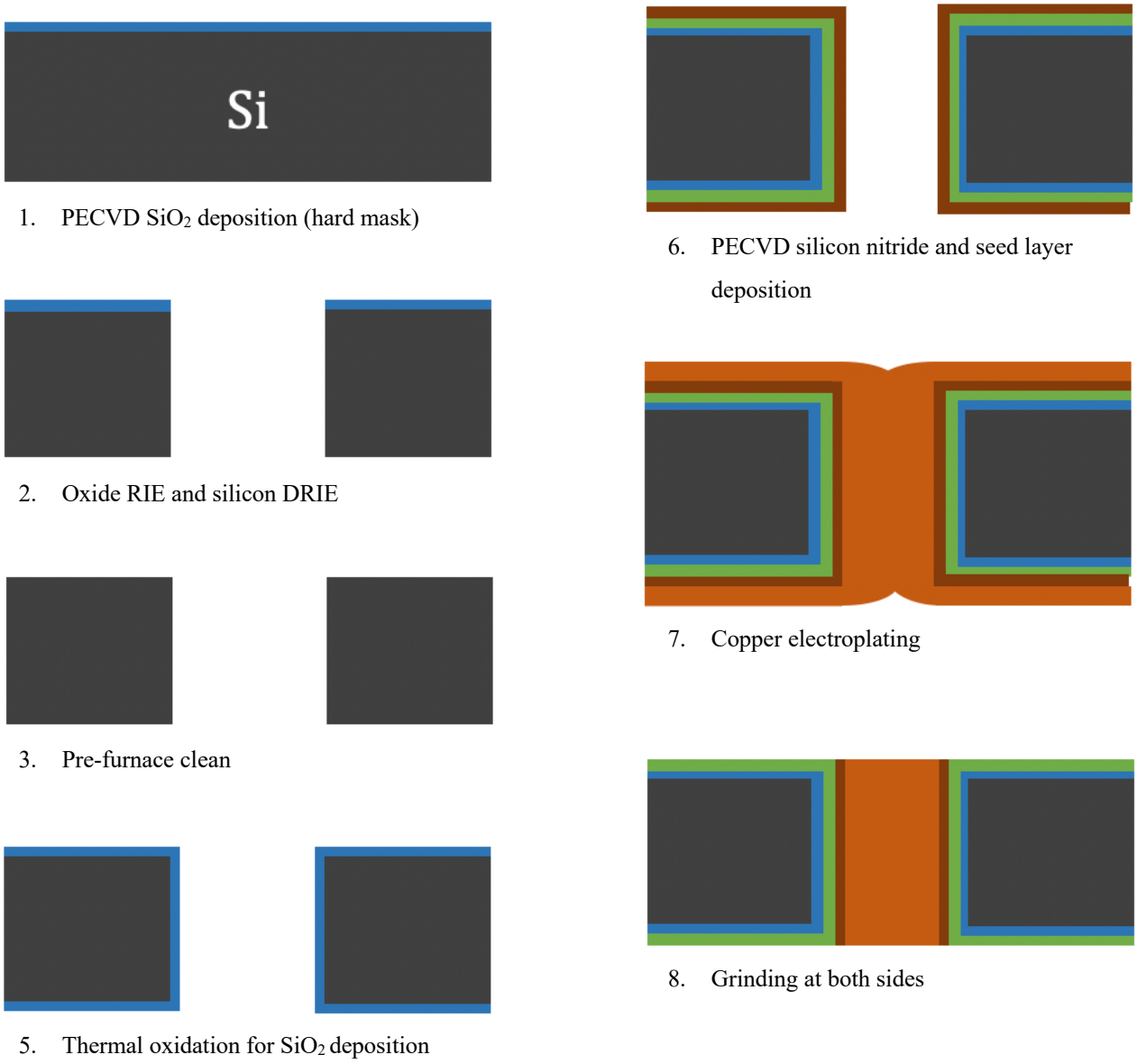


Fig 3.7 Traditional through via process flow of TWVs.

In order to overcome the via filling problem, we developed our top-down TWV fabrication flow for Si-IF. The detailed top-down TWVs process flow for Si-IF is shown in Fig 3.8.

1. SiO_2 deposition hard mask by thermal oxidation

2. Spin coating photoresist and lithography to create patterns

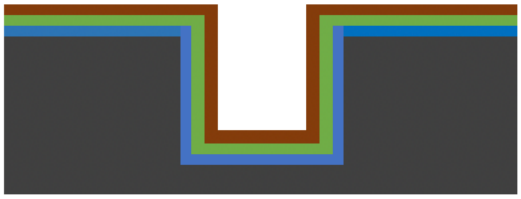
3. SiO_2 dry etch

4. Remove photoresist with acetone and isopropanol

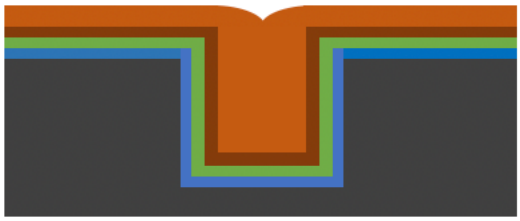
5. Silicon etch with DRIE

6. Get rid of SiO_2 with 49% HF

7. SiO_2 deposition by furnace oxidation



8. Silicon nitride deposition and seed layer deposition (TiN/Ti/Cu)



9. Copper electroplating to fill the via (with levelers)

10. Active side CMP and backside wafer thinning

Fig 3.8 Top-down TWVs process flow for Si-IF.

3.3.2 Detailed process flow of top-down TWVs for Si-IF

3.3.2.1 Thermal oxidation

a. Piranha clean: Before wafers are sent into the furnace for thermal oxidation, it is required to do pre-furnace clean (PFC) to remove the organic and metallic contaminants on wafers. In the public cleanroom Nanolab, there is a PFC tank for us to do the piranha clean. Turn on the PFC tank and wait for the bath temperature to increase to 100°C and start the PFC tank timer for 10 minutes. Immerse the whole wafer box into the tank to make sure each wafer is cleaned. After 10 minutes, move the wafer box into the dump rinser tank to get rid of piranha residuals with cyclic deionized water clean. In the end, replenish the PFC tank with 250 ml of hydrogen peroxide.

b. Spin dry: After piranha clean, put the wafer box into the spin dryer and wait for 200 seconds for the tool to completely dry the wafers.

c. Thermal oxidation: Contact ISNC staff for 3μm thermal oxidation growth. The oxidation temperature is around 1100°C for 30 hours.

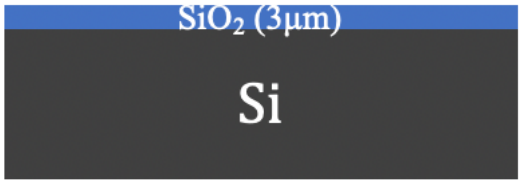


Fig 3.9 Thermal oxidation.

3.3.2.2 Photoresist coating

a. Preclean the wafer and adhesion promoter coating: Before photoresist coating, the wafer is rinsed with acetone, isopropanol (IPA) and deionized water (DI water) in order. Acetone is used to get rid of organic particles while IPA repels acetone and DI water removes all chemicals. After the preclean step, the wafer is put on a hot plate with temperature 150°C to dehydrate the wafer for 2 minutes. Then the wafer is kept inside a box with hexa-methyl-disilazane (HMDS) for another 2 minutes. HMDS is an adhesion promoter which helps photoresist stick onto the wafer.

b. Photoresist spin coating: Setup the spin coater with the recipe is as follows:

Step 1: Speed = 500 rpm, Ramp = 100 rpm, Time = 5 seconds

Step 2: Speed = 2000 rpm, Ramp = 1000 rpm, Time = 30 seconds

Step 3: Speed = 0 rpm, Ramp = 1000 rpm, Time = 0 seconds

Turn on the vacuum chuck between the wafer and the coater. After the recipe setup of the spin coater, pour photoresist AZ5214E onto the wafer and start the spin coater. The wafer should be coated evenly after 35 seconds.

c. Soft baking: The wafer is then put on a hot plate with temperature 110°C to soft bake the photoresist.

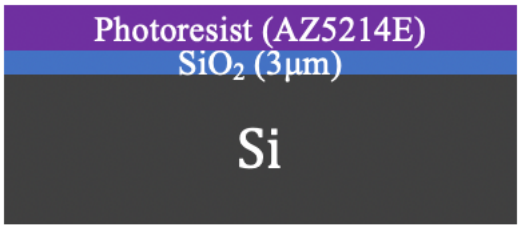


Fig 3.10 Photoresist spin coating.

3.3.2.3 Exposure and Development of photoresist

a. Exposure: The required tool for exposure in Nanolab is the Karl Suss Lithography tool. The recipe for the tool is as follows:

1. Program: Hard Contact (HC)
2. Exposure time: 60 seconds

Put on the TWV mask and start the tool. After 60 seconds of exposure, the wafer is ready to developed.

b. Development: Pour the AZ300MIF Developer into a beaker and dip the exposed wafer into the developer for 1 minute. Rinse the wafer with DI water to remove the developer.

c. Hard bake: Put the wafer on a hot plate with temperature 120°C. The high temperature helps the linkage of the polymers from photoresist and prevent them from degassing.

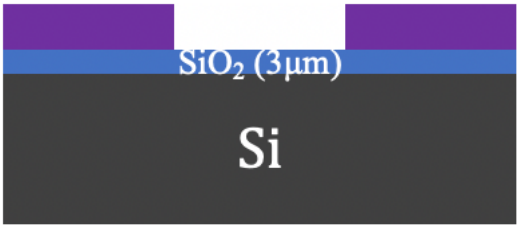


Fig 3.11 Exposure and development for photoresist.

3.3.2.4 SiO_2 oxide etch

The required tool is STS AOE tool in this step. Put the wafer on the loading deck and send into the chamber to start the oxide etching process. The recipe to be use is OXIDAPIC and takes 9 minutes to etch the oxide layer. To check if the oxide is etched away, we can simply check the thickness of the oxide film in Nanospec.

Fig 3.12 Oxide etching.

3.3.2.5 Silicon etch

The required tool is UNAXIS Fast DRIE (FDRIE) to proceed the Bosch etch process. The Bosch process is a cyclic process where one cycle etches the silicon while the other one passivates the sidewall. There is more detailed information during the results part for the fabrication. The recipe we used is UCLA FAST NANO-DY. To etch 350μm to 450μm of silicon via, it requires 60 minutes to 80 minutes to etch a blind via. There will be some variation because of the renewal of etching gas of the tool.

Fig 3.13 Silicon etching.

3.3.2.6 Removal of photoresist and oxide hard mask

a. Ashing: The required tool is Matrix Asher to remove the photoresist with oxygen plasma. The 3 minutes oxygen recipe is required to get rid of the photoresist.

b. Hard mask removal: Pour 49% of hydrogen fluoride (HF) inside a plastic beaker (glass beaker is made of SiO_2 which will be etched off by HF). Immerse the wafer into the beaker for 90 seconds to strip off the silicon dioxide. Then, rinse the wafer into a beaker with DI water thoroughly and dry it with nitrogen gun.

Fig 3.14 Photoresist and hard mask removal.

3.3.2.7 SiN_x silicon nitride deposition

a. Thermal oxidation: Furnace oxidation of the wafer for 1μm of SiO_2 to create electrical isolation and prevent the stress issue from the direct attachment between silicon and silicon nitride.

b. Nitride deposition: The required tool is STS PECVD to deposit silicon nitride. The recipe is 4-LSSN and takes 30 minutes to deposit silicon nitride.

Fig 3.15 Silicon nitride deposition.

3.3.2.8 Seed layer deposition

The required tool is CVC Sputter. In CVC Sputter, there are only two targets which are titanium and copper. Fewer targets gives the CVC Sputter tool a better choice among all sputter tool because of less cross contamination. Two layers are needed to be sputtered. The first one is 50nm of titanium which serves as an adhesive inter-layer and diffusional barrier. It takes 4 minutes to sputter. The second layer is 200nm of copper which serves as the seed layer for copper electroplating in the next step. The sputtering time for copper is 90 minutes.

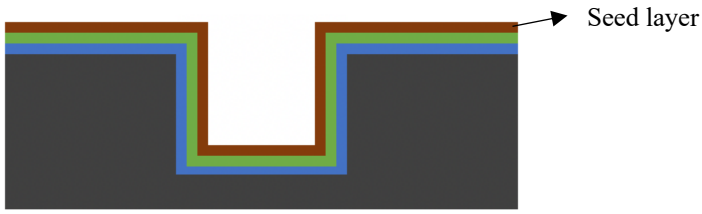


Fig 3.16 Seed layer deposition.

3.3.2.9 Copper electroplating

Prior to copper electroplating, we need to make sure the copper is plated in the TWV. It shortens a lot of time for copper electroplating and also makes sure that the uniformity is as low as possible.

a. Photoresist coating: The wafer is first kept inside a box with HMDS for 2 minutes and setup the spin coater with the recipe is as follows:

Step 1: Speed = 500 rpm, Ramp = 100 rpm, Time = 5 seconds

Step 2: Speed = 2000 rpm, Ramp = 1000 rpm, Time = 30 seconds

Step 3: Speed = 0 rpm, Ramp = 1000 rpm, Time = 0 seconds

Turn on the vacuum chuck between the wafer and the coater. After the recipe setup of the spin coater, pour photoresist AZ4620 onto the wafer and start the spin coater.

b. Hard baking: The wafer is then put on a hot plate with temperature 110°C to soft bake the photoresist.

c. Exposure and development: The required tool is Karl Suss Lithography tool and the recipe is set with Hard contact (HC) and exposure time is 60 seconds. Develop the wafer in AZ300MIF developer for 1 minute.

d. Copper electroplating: This step has yet to be optimized but we have already setup the electroplating cell. Other than the traditional bath solution which includes electrolyte ($CuSO_4$, H_2SO_4, HCl), brighteners and carriers, we also introduce the levelers into the solution to minimize the current crowding at the corner of the via, inhibit the growth of copper on the sidewall and create a bottom-up copper filling mechanism.

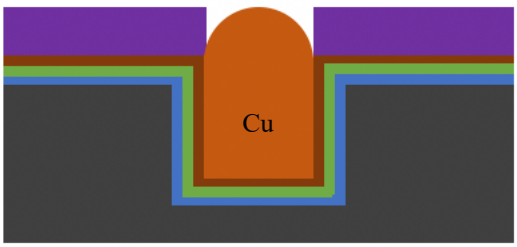


Fig 3.17 Copper electroplating.

3.3.4 Results and discussion of top-down TWVs process

For our top-down process, we first deposited the wafers with SiO_2 for 3μm by thermal oxidation to create a hard mask on the wafers. A thick SiO_2 is required to achieve a smooth sidewall profile during the silicon etching process of 500μm of silicon. We then pattern the via with lithography process and dry etch SiO_2. The via holes are formed by deep reactive-ion etching process similar to the Bosch process [5]. The Bosch process includes cyclic isotropic etching and fluorocarbon-based protection film deposition by quick gas switching. The SF_6 plasma (gas etchant) cycle etches silicon while the C_4F_8 plasma cycle creates a protection layer as passivation [6]. As a result, we are able to control the etching depth by controlling the number of cycles. When we were conducting DRIE trial, we first began with a high etch rate DRIE recipe (~9μm/min) for around 50 minutes. However, as you can see in Fig 3.18 (a), the via depth is around 358μm in our experiments rather than the expected 450μm because the exposed silicon areas are different than the standard areas. We then extended the etching time to 60 minutes using the same recipe and it gave us a via depth of 386μm shown in Fig 3.18 (b).

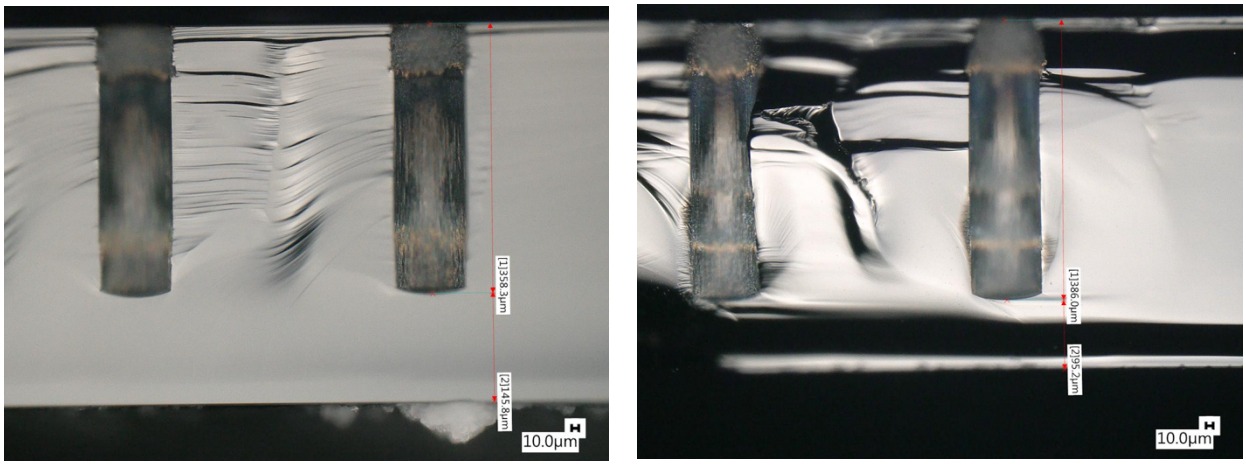


Fig 3.18 DRIE etching optical microscope images for (a) 50 minutes etching time (b) 60 minutes etching time.

Prior to the seed layer deposition, 1μm of silicon dioxide layer is formed as an electrical isolation

layer by thermal oxidation. A 400nm of silicon nitride layer is then deposited by PECVD to act as a stop layer for the final CMP process. After the stop layer deposition, a layer of titanium nitride is deposited on to the silicon nitride to serve as the diffusion barrier [7] by atomic layer deposition. The diffusion barrier is able to protect the diffusion of metals such as titanium and copper into silicon substrate and oxide layer during high temperature or high current process [8]. Then a 50nm of titanium layer is sputtered as an adhesion layer between SiN_x and Cu seed layer [9]. Finally, prior to copper electroplating process, a 200nm of copper seed layer is sputtered along the sidewalls and the bottom of the via. The seed layer offers electroplating copper to deposit on the sidewalls and the bottom. In Fig 3.19, after dicing the cross-sectional area of the via, we can see the sputtered copper layer inside the via by visualizing the bronze color at the top of the via.

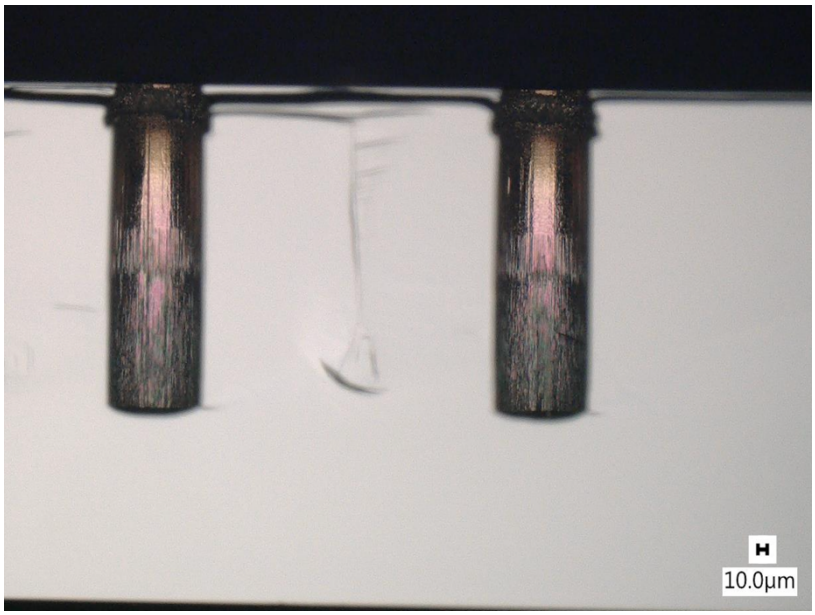


Fig 3.19 Optical microscope image of the via after titanium and copper sputtering. Copper seed layer is only sputtered at the top of the via.

Electroplating the copper onto the seed layer is the next step. Other than the electrolyte, brighteners and carriers, we also introduced levelers into the chemical bath in the copper electroplating step. As mentioned in the background studies, levelers offer the bottom-up filling quality for the via filling process. Additionally, the thickness of copper overburden will also be inhibited by levelers as

the plating time goes longer. As a result, the chemicals in our bath include $CuSO_4$, H_2SO_4, HCl, brighteners, carriers and levelers. However, the sputter seed layer could not reach the bottom of the via as we proceed our fabrication. As a result, we might need other methods to fill up the bottom of the via by either using evaporator or using nanoparticles to form the bottom seed layer.

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Chapter 4 Conclusions and Future Directions

In order to fill the via with copper, the copper seed layer on the sidewall of the via takes an important role. So far, we have achieved half of the sidewall sputtered with copper seed layer but the sidewall at the bottom half of the via is still lack of copper. It might lead to a huge void at the bottom of the via. We are currently adjusting the parameters of the CVC sputter tool and in the meantime trying to use copper nanoparticles to fill the bottom of the via.

Another promising fabrication method is bottom-up fabrication flow we designed for Si-IF that overcomes the sputtering limitation which causes the void appearance at the bottom of the via. The core idea for this fabrication flow is to create a copper seed layer which “only” appears at the bottom of the via. By eliminating the copper seed layer on the sidewall, not only can we overcome the sputtering limitation, but we also don’t have to be worried about voids or seams during copper electroplating step since copper will only grow from the bottom seed layer. Namely, a guaranteed bottom-up filling mechanism can be achieved. Nevertheless, in order to maintain the structural stability of the bottom seed layer, a thin layer of silicon nitride and a layer of silicon dioxide must be deposited using PECVD. The detailed process flow for bottom-up TWVs has already been designed and is shown in Fig 3.11.

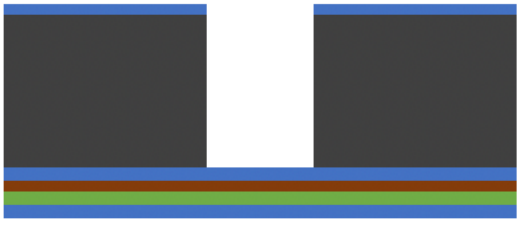
In this thesis, we have demonstrated the uniformity, surface roughness and the top-down process flow of through wafer vias for silicon interconnect fabric. Most processes in TWVs of top-down process have been optimized and the bottom-up process is an alternative process under development.

1. PECVD to grow silicon oxide at both sides of wafer

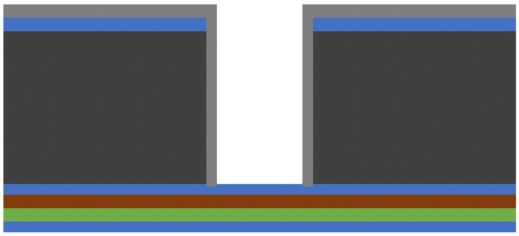
2. Copper seed layer sputtered for 200nm at the back side of wafer

3. SiN_x silicon nitride deposited for 50nm above the copper seed layer by PECVD

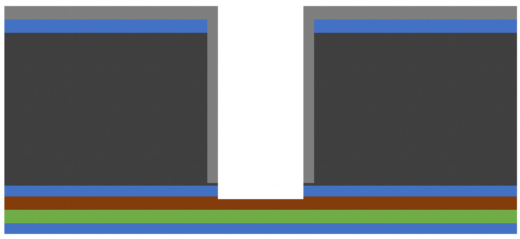
4. SiO_2 deposited on top of silicon nitride by PECVD to maintain structural stability



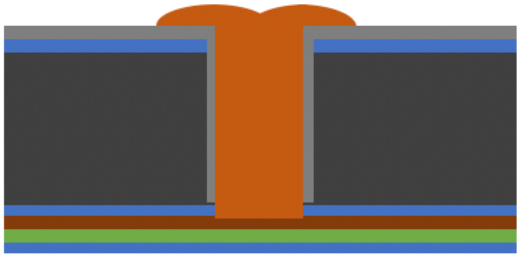
5. DRIE etching to create the through via from the active side of the wafer



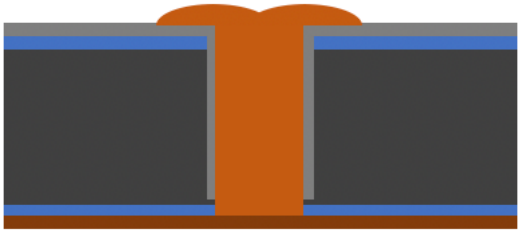
6. TiN deposited to create diffusional barrier by atomic layer deposition (ALD)



7. SiO_2 etching to expose the copper seed layer and create a bottom copper layer



8. Copper electroplating



9. SiO_2 and SiN_x etching at the backside of the wafer

10. CMP at the active side of the wafer and etch off backside SiO_2 layer and SiN_x layer

Fig 4.1 Bottom-up TWVs process flow for Si-IF.