UNIVERSITY OF CALIFORNIA,
IRVINE

Efficient Low Power Headphone Driver

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Khaled Abdelfattah

Dissertation Committee:
Professor Michael Green, Chair
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DEDICATION

To

my beloved wife Rania Sultan whose support was the most important major element to my success in getting this work accomplished.

To

my parents who always gave me the moral support and the urge to continue every time I stumble.

To

my kids who were always there to keep me going on.

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PUBLICATIONS

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ABSTRACT OF THE DISSERTATION

Efficient Low Power Headphone Driver
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Professor Michael Green, Chair

In recent years, the consumer electronics market for battery-powered devices such as smartphones and tablets has been rapidly expanding. The requirements for audio CODEC in these portable devices have extended from merely supporting voice calls to high-fidelity music playback. As a result, audio driver performance has become one of the most important differentiating factors among products from different suppliers. There are three basic performance metrics that are typically used to benchmark audio modules: the maximum delivered output power, the audio fidelity measured in terms of dynamic range, THD+N, and finally the battery life. Maximizing all three of these performance metrics has proven to be an exceptionally hard task as portrayed by the research publications.

This work presents an attempt to push all three of these metrics together and provide an acceptable balance which is achieved by selecting the right topology. Conventionally, headphone drivers are designed using a linear amplifier topology for many reasons- most prominently- to achieve a superior THD+N and PSRR requirement which in the past was essentially the only key performance metric needed. This came at the expense of realizing mediocre power efficiency targets, thereby wasting battery life. This picture changed

dramatically over the last decade with smartphones and other portable devices becoming the first choice of the young generation. These devices are extremely power hungry due to the unlimited functions and features they provide and therefore battery life has come to the spotlight as a key resource that need to be preserved. As a result, in this work a headphone driver is based on a switching topology that is able to deliver more than 230mW of power (or equivalently 2Vrms) to a 16Ω load while achieving better than -98dB of THD+N , more than 108dB of SNR, and about 108dB PSRR while still maintaining a peak power efficiency of more than 84%.

CHAPTER 1 INTRODUCTION

1.1 Motivation

With the advances of portable electronics over the last decade, customer demands on audio systems have evolved dramatically. In particular, demands for higher output power while maintaining excellent sound fidelity for portable devices are continuously growing. At the same time, in order to maximize the battery charging cycle; power dissipation from the battery should be minimized. This translates into an increased demand for highly efficient designs that can maintain high fidelity [1-3].

Traditionally, linear topologies are used because of their superior sound quality and low distortion; however, it remains challenging for such topologies to meet the continuous demands placed on portable electronics to achieve a longer battery charging cycle. As a result, many improvements to decrease the power dissipation, and increase power efficiency have been introduced in the literature. Some of these approaches combine different topologies and switch between them depending on the signal amplitude, or by modulating their supply in either discrete or continuous fashion [4-13].

On the contrary, switching topologies, which are characterized by their high-power efficiency, yet poor distortion, have been continuously used for audio subsystems that do not demand the same fidelity, such as loudspeaker drivers [14-17]

In this work, a switching topology is used to achieve both very high fidelity and very high efficiency for a headphone subsystem.

1.2 Audio Signals

Audio signals have some distinct features [20], which are listed here:

1. Their amplitude probability density function has a Gaussian distribution. As shown in Figure 1.1, audio signals possess a large peak to average ratio (also known as crest factor) of about 15dB on average, which means that audio signals spend most of their time near the average.

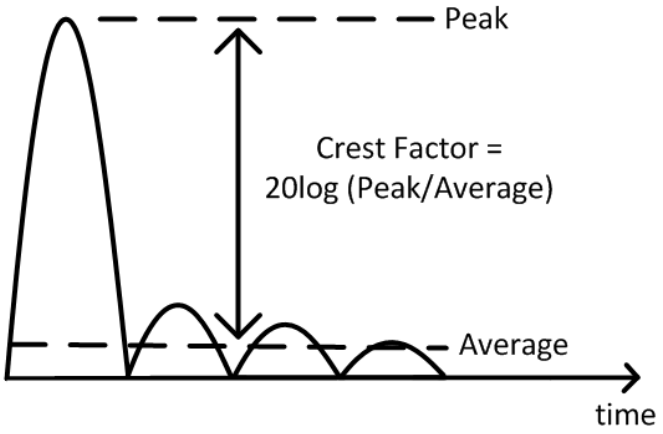


Figure 1.1 Crest factor for an audio signal

2. Their frequency range, which is set by the limited frequency response of the ear, is between 20 Hz and 20kHz as shown in Figure 1.2. However, given that most people cannot hear 20kHz tones, the power is mainly concentrated at medium frequencies and peaks near 1-2kHz.

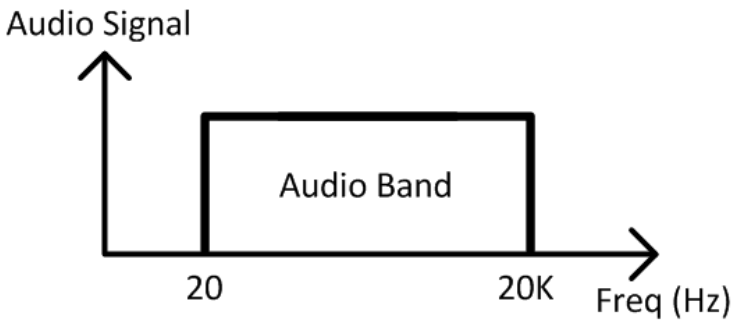


Figure 1.2 Audio band

3. In addition, the ear has a large dynamic range of several decades of sound pressures (SPL). For example, low-level background noise can be as low as 50dB, whereas rock band music is around 110dB, and usually the required signal-to-noise ratio of an audio system is usually more than 80dB.

1.3 Audio Codecs

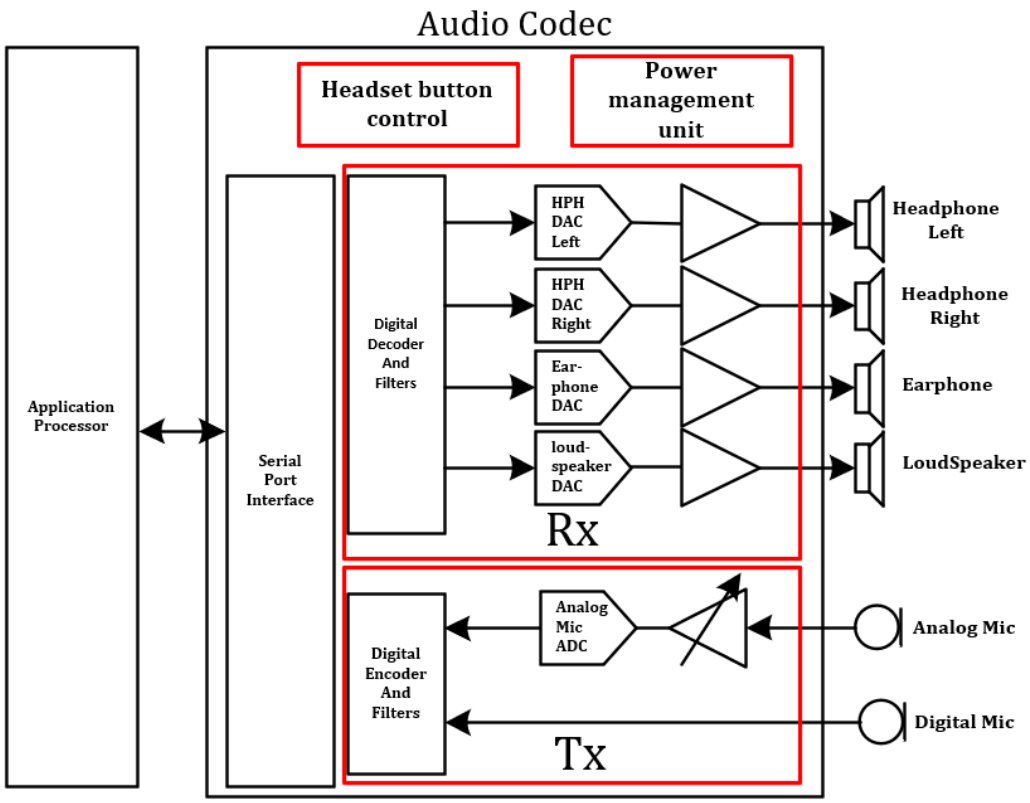


Figure 1.3 Simplified diagram for a typical audio codec chip

Audio codecs are continuously evolving and continue to include many complex functions and support advanced features [21]. Figure 1.3 shows the most basic functions that exist in an audio codec chip, which are:

1. Several receiver channels (Rx), which send the audio signals to different audio peripherals such as earpiece, headphone, lineout, and speakerphone. These channels receive their input signals in PCM digital format from the device application processor (AP) and then pass through digital filters followed by a sigma-delta modulator to reduce their number of bits -which can be as high as 24 bits depending on the quality of the source- down to few bits. As the number of bits goes down, the bit rate increases from 48Kb/s to few Mb/s.

   The high-rate, low-resolution signal is used to drive a high-fidelity digital-to-analog converter (DAC), followed by an efficient audio driver to drive the load.

   Depending on the receiver channel, the load can be electrically represented by different simplified models:

   b. Headphone load: 16 or 32Ω single-ended ground-referenced resistor.
   c. Earpiece load: 32Ω differential resistor.
   d. Loudspeaker load: Differential load consisting of 4 or 8Ω resistor in series with a ~64μH inductor.
   e. Lineout: Can be either differential or single-ended, and load is usually a resistor on the order of a few kΩ.

2. Several transmitter channels (TX) are used to receive audio signals from the microphones and then send them to the device application processor for storage or for playback. External microphones can be either analog or digital; digital

microphones digitize the audio signals, which are directly routed to the application processor. If an analog microphone is used, then a codec chip receives the analog data that passes through a programmable gain stage (PGA) to maintain a predefined signal-to-noise ratio and then to an anti-aliasing filter followed by analog-to-digital converter (ADC). The output digital stream is then filtered and sent to the application processor.

Analog microphones come in different types, such as dynamic, electret, or MEMS-based. The most common high-fidelity type is the electret microphone, which requires a low-noise bias voltage to operate. This voltage, commonly referred to as mic bias, is usually designed in the Tx path using a low noise reference and an LDO to drive the external electret mic.

3. Power management unit usually receives a single supply (in most cases the battery voltage itself) and is used to generate:
    a. Band-gap based voltage and currents used to set the ADC and DAC references, as well as the DC bias current for various analog blocks.
    b. Class-H or Class-G power supplies, that supply the final audio driver to increase the efficiency.
    c. Negative supply for headphone drivers.
    d. Regulated supplies for the sensitive parts of the system, such as front-end stages to enhance PSRR.
4. Headset button control unit keeps track of the Tx and headphone ports to detect an insertion, and then sends an interrupt signal to the application processor before identifying the plug-in accessory type. The unit also measures the

headphone impedance and detects whether any of the multi-function buttons on the headset is pressed and estimates the duration for which the button is pressed in order to for the AP to correctly decode the function that the user intends.

1.4 Key performance parameters for audio drivers

This section focuses on the receive path and discusses the different key parameters that are used to evaluate the performance of a specific receiver path.

1. Audibility and battery life

a. Maximum power delivered to the Rx load

End-users usually are interested in more loudness coming out of their portable device; typical speakerphone output power is usually in the range of a few watts, while headphone and earpiece output power is usually lower than 100mW.

b. Quiescent current

This is an important parameter primarily because of the audio signal high crest factor. As discussed before, audio signals spend most of the time in low amplitude, in which case the power consumed by the device is dominated by the quiescent power more than the output power. Reducing the quiescent current is important to maximize the battery life for all Rx channels, and especially critical for the headphone path since it is the most used for music playback.

c. Since it is desirable to increase output power while decreasing the quiescent current, a figure-of-merit (FOM) is introduced to combine these two parameters to benchmark audio drivers, defined by:

$$FOM \equiv \frac{I_{load,peak}}{I_{Quiscent}} \tag{1.1}$$

d. Power Efficiency

It is defined as:

$$Power\ Efficiency\ \equiv \frac{Output\ Power}{Power\ consumed\ from\ the\ battery} \tag{1.2}$$

This parameter is usually measured as a function of the output power. It is always desirable to increase the power efficiency at all power levels to maximize battery life; therefore, special types of audio drivers are used to maximize the power efficiency. For example, loudspeakers use Class-D output stage, which can deliver up to 90% power efficiency at maximum output power. On the other hand, headphone drivers typically use a Class-AB output stage to maximize the power efficiency while maintaining excellent audio quality.

2. Fidelity

Since the human ear has high sensitivity to noise and distortion, several parameters are used to quantify the effects of the noise and distortion introduced by the audio drivers to evaluate their fidelity.

a. Signal-to-noise-ratio (SNR)

Defined as the ratio of the full-scale rms signal to the integrated noise within a 20kHz frequency band. The noise is usually measured with no signal and weighted with a special filter known as A-weighting, which imitates the ear response.

b. Dynamic Range (DR)

Dynamic range is a measure to rate the ratio of both random noise and the ΣΔ quantization noise to the output full scale. A small signal (-60dB) is applied to the input to avoid the effect of any nonlinearities, and the output is integrated within the audio band. 60dB is added back in order to refer back to full-scale input, as shown in the following equation:

$$DR \equiv \frac{Signal\ @-60dB}{Integrated\ noise\ floor(20-20KHz)} + 60dB \qquad (1.3)$$

c. Total Harmonic Distortion+ Noise (THD+N) ratio

This measure quantifies the effect of both system noise and nonlinearities in presence of a signal. It is usually measured as a function of the input signal and span a few decades of signal range.

d. Power Supply Rejection Ratio (PSRR)

Power supply rejection ratio is an especially important parameter for portable devices working in a GSM network. On such a network, the mobile device may transmit in either the 800 or 1900MHz bands with RF power up to 3W. In GSM transmission, the mobile device pulses its RF transmitter on and off at a rate of 217Hz with a duty cycle of about 10%. While in the "on" state, the RF

transmitter draws a large amount of current. Since the battery is the only source of power in a mobile device, and it has a finite source resistance (R_{BAT}) as shown in Figure 1.4, the supply voltage of the codec effectively becomes modulated with about 500mV peak-to-peak square wave at 217Hz. This disturbance becomes audible if it propagates to the audio port, and thus it is necessary for the audio driver to reject the supply disturbance.

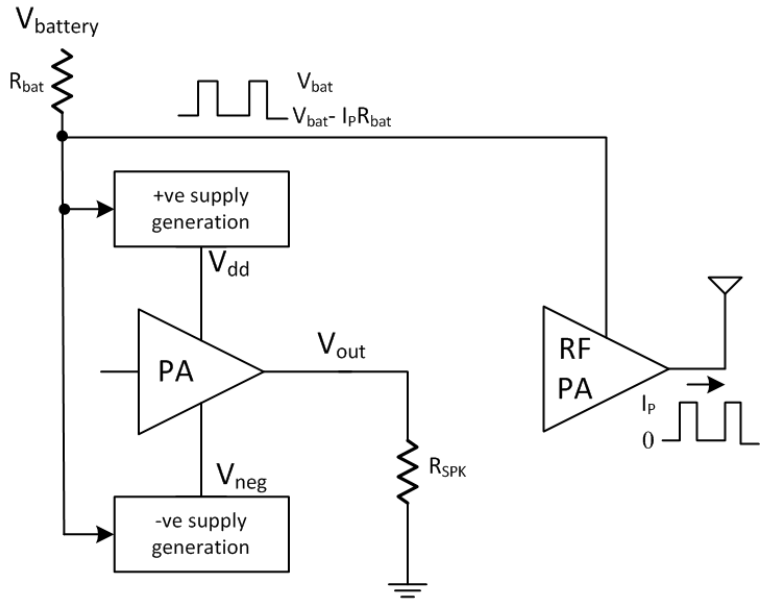


Figure 1.4 Effect of finite battery internal resistance on audio drivers

Figure 1.5 shows a typical PSRR measurement result where a 217Hz 500mV_{PP} disturbance is applied on the battery. Battery disturbance and the audio output spectrum are plot and compared.

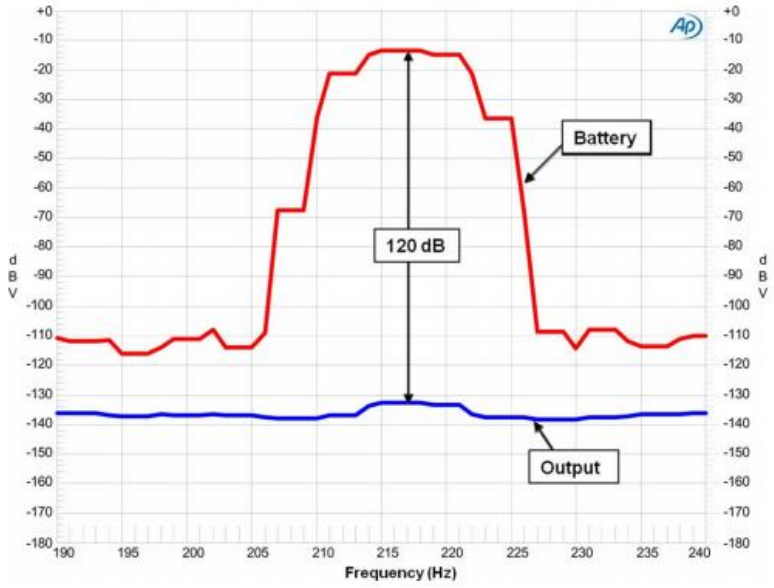


Figure 1.5 A typical PSRR measurement result

1.6 Headphone path

As explained in Section 1.4, there are several Rx receiver modules within a codec chip, each having its own unique requirements in terms of the acceptable fidelity as well as output power. Of these modules, the headphone module presents the most challenging design because of its stringent fidelity demands that exceeds those of other Rx channels as well as ever increasing demands for higher output power without degrading the efficiency [2,3].

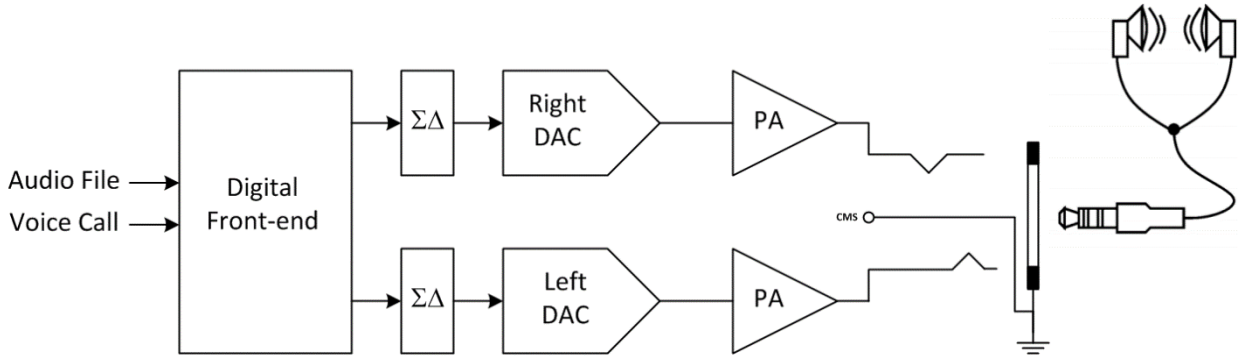


Figure 1.6 Stereo Headphone Module

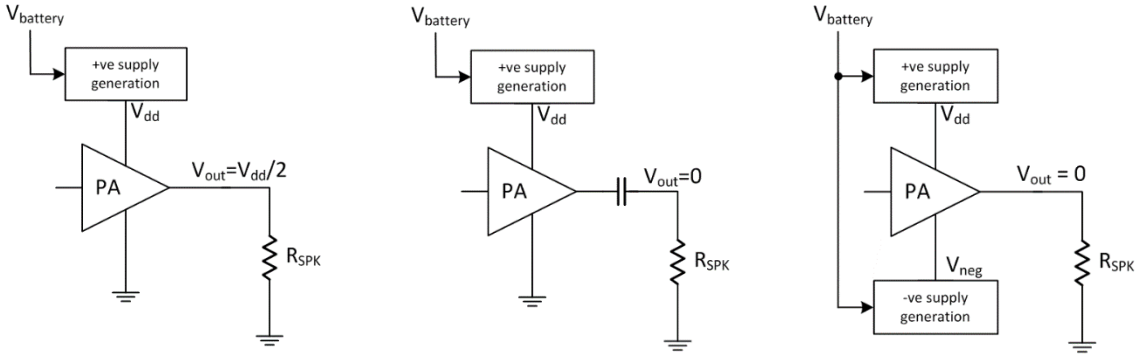
Figure 1.6 depicts the overall stereo headphone module consisting of identical left and right channels. The headphone module receives two streams of data, one for each channel, from the digital front-end module. This module controls several functions such as gain companding, signal pre-distortion, and several other signal conditioning functions. In a typical Hi-Fi audio CODEC, words for prerecorded CD quality data are 24 bits wide sampled at 48, 192, or 384kHz. In order for this data to drive the speaker, a high-accuracy DAC is needed to convert the signal from digital to analog while preserving the CD audio quality. A typical ΣΔ DAC consists of a digital ΣΔ modulator followed by a DAC, the basic idea being to oversample the incoming data stream and then truncate it. The truncation error, which has a white spectrum is shaped by the ΣΔ modulator such that the in-band portion is significantly reduced down to the system requirement, while the out-of-band error is increased. The oversampled and truncated ΣΔ output data has fewer levels; thus, a fast, low-resolution DAC is needed. Due to fewer DAC levels, fewer unit elements are needed, which results in die area savings. Another advantage of using a ΣΔ DAC is the ability to easily implement dynamic element matching [18-19] for the DAC elements, which is often required to reduce the impact of the unit mismatch on the overall THD+N performance. The DAC analog output is then passed through the PA (power amplifier) feedback loop conventionally configured as a linear power topology, such as Class-AB, to drive the 16Ω speaker load. The PA driver loop uses the common-mode-sense input (CMS) to couple any noise on the headphone ground back to the module output.

This arrangement provides ground noise immunity, particularly important in an SoC environment.

In this work, the focus is on the design of the PA driver loop, where highly efficient switching topology is used to increase the output power, which increases the overall efficiency while maintaining high fidelity.

1.7 Headphone PA supply

The headphone load can be modeled simply as a load resistor (normally 16 or 32 Ω) referenced to ground. Early PA designs used a single supply and set the common mode at the output to half the supply voltage as shown in Figure 1.7(a). This approach means that the PA is realized as a Class-A amplifier and therefore suffers from very poor efficiency when no signal is present. In addition, applying a DC voltage to the speaker for an extended period of time may eventually damage it. Figure1.7(b) shows a second approach to use a blocking capacitor to block the DC while allowing only the ac variation to propagate to the speaker load. While this approach is safer for the speaker and would result in better efficiency, the blocking capacitor along with the speaker load form a high-pass filter whose cutoff frequency must be less than 20Hz. If the speaker load resistance is set to 16Ω , this translates into a capacitor value of approximately 500μF, which would be very costly and bulky [9].



i. (b) (c)

Figure1.7 Evolution of headphone PA supply arrangement, (a) single supply and CM set to mid-supply, (b) single supply and decoupling cap, (c) dual supplies.

A better approach, shown in Figure 1.7(c), which has recently become the usual for headphone PA design now is to use dual supplies: positive and negative, so that the output common mode can be comfortably set to ground without the need for a blocking capacitor [9]. This solution simplifies the design of the PA at the expense of adding the complexity of designing some circuitry that can generate a negative on-chip supply with high enough efficiency.

Designing the PA supplies has been an integral part of achieving a high power efficiency for the entire headphone module. PA supplies could be either constant as in Class-A, AB, and B topologies, or it can depend on the signal, which can be either discrete as in Class-G, or continuous as in Class-H. In the next section, an overview of the different types of PA topologies will be discussed.

1.8 Overview of power amplifier topologies

There are two categories for PA topologies, linear and switching. Linear topologies such as Class-A, AB and G/H are designed to have a smooth transition between different devices in delivering the output power throughout the signal swing. This way, when the audio signal transitions from positive to negative swing, the amplifier smoothly reduces the transconductance of the pmos side --which delivers positive swing to the output-- and increases the transconductance of the nmos side in a similar way. This smooth transition usually results in very low distortion for the output signal, and therefore linear topologies have been extensively used for headphone PA design. However, since the nmos and pmos drivers require sufficient headroom across them in order to effectively handle the signal swing with no distortion issues, this headroom results in power dissipated inside the PA, effectively lowering the power efficiency of the design.

On the other hand, switching topologies rely on operating the driving transistors with minimum headroom as they are used merely as switches while delivering audio-encoded PWM/PDM signal to the output, and therefore the power dissipation is significantly lower increasing the overall efficiency. However, this results in sudden transitions between the nmos and pmos driving sides, which degrades the PA signal-to-distortion ratio.

Switching topologies have been used extensively for high-power audio drivers such as speaker phone drivers, at the expense of high distortion.

a. Linear topologies

1. Class-A

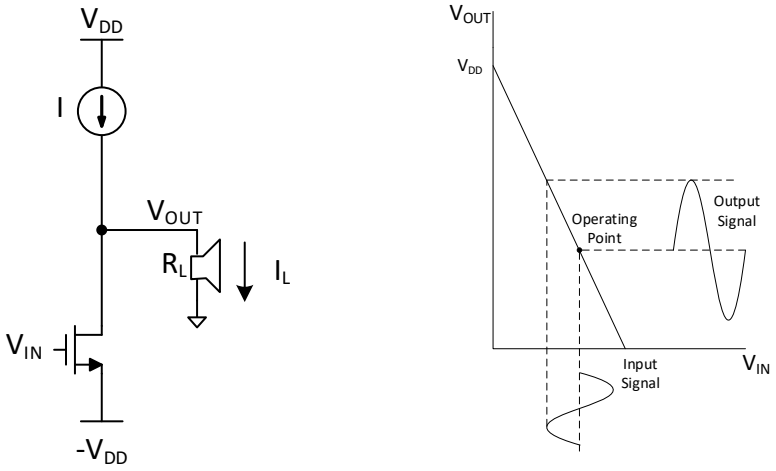


Figure 1.8 Class-A topology. (a) Circuit Diagram, (b) Signal transfer function.

Figure 1.8(a) shows a simple Class-A PA output stage consisting of one output device (nmos or pmos) and a current source. The signal transfer function shown in Figure 1.8(b) shows a very linear relationship between V_{OUT} and V_{IN} due to the output device remaining in the saturation region throughout the signal swing. The power efficiency (η) is defined as:

$$\eta \equiv \frac{Power\ delivered\ to\ the\ load}{Power\ consumped\ from\ the\ supplies} \tag{1.4}$$

Since power delivered to the load is $\frac{{V_{out,peak}}^2}{2R_L}$, and the average power drawn from each supply is $V_{DD}I$, then the efficiency is calculated as:

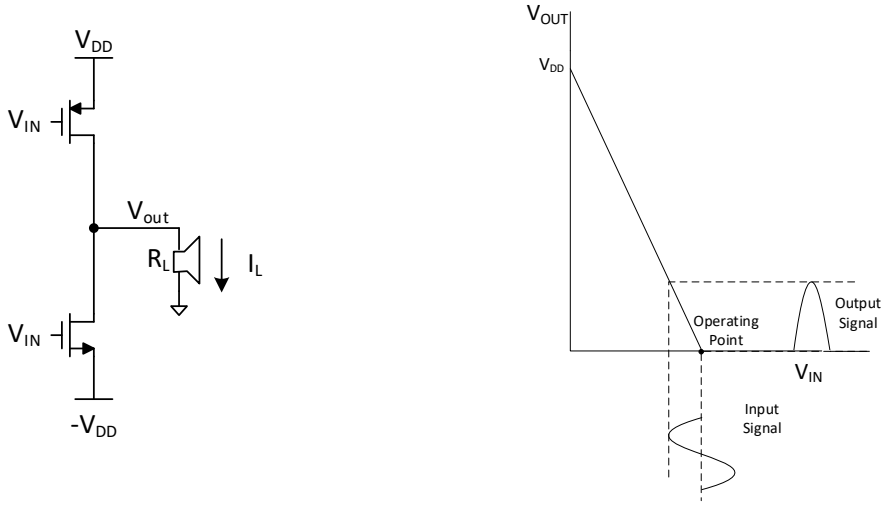
$$\eta = \frac{1}{4}\frac{V_{out,peak}}{V_{DD}}\frac{V_{out,peak}}{IR_L} \tag{1.5}$$

Since $V_{out,peak}$ is always smaller than V_{DD} and IR_L, the maximum efficiency is limited to only 25%.

This poor efficiency is a direct result of the fact that this amplifier is always on and never cut off, regardless of the magnitude or polarity of the input, as the Class-A amplifier has a 360^0 conduction angle, meaning it is on and conducts throughout a full cycle of the input sine wave.

2. Class-B

The Class-B amplifier uses a "push-pull" arrangement with a pair of complementary amplifier devices Nmos/Pmos, each biased at cutoff with the conduction angle of each amplifier at 180^0 (half cycle) as shown in Figure 1.9. When the bipolar, zero-centered input signal goes positive, one device comes out of cutoff and goes into its saturation region, conducts, and amplifies; when the signal goes negative, the other device does the same while the first one is cutoff and thus dissipating near-zero power.



(a) (b)

Figure 1.9 Class-B topology. (a) Circuit Diagram, (b) Signal transfer function.

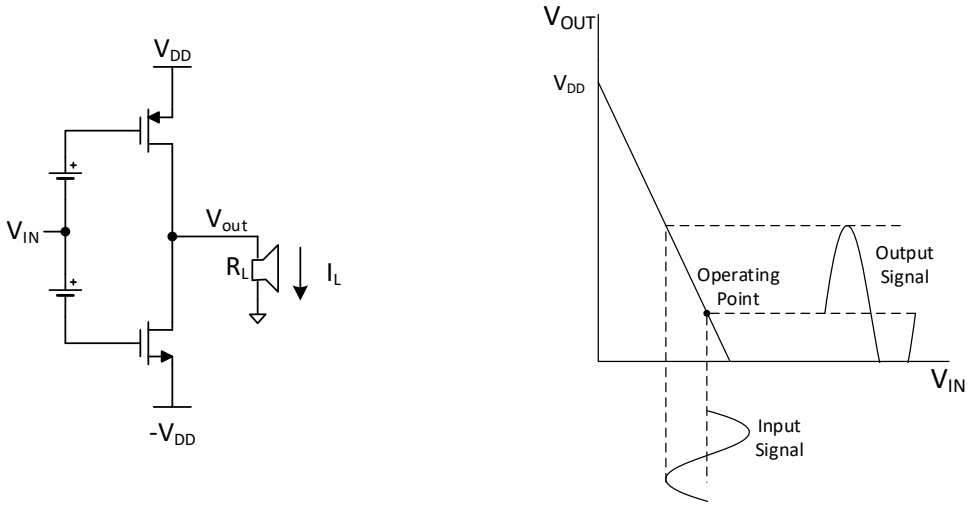
Class-B amplifiers suffer from crossover distortion, which generates harmonics, arising because of the slight lag or discontinuity as one active element turns on while the other turns off. Distortion is typically 10-20%. This may be acceptable for some situations but not for higher-quality audio designs. On the other hand, the realized efficiency is much better than Class A and is given by:

$$\eta = \frac{\pi}{4}\frac{V_{out,peak}}{V_{DD}} \tag{1.6}$$

The maximum efficiency is limited to only 78% when $V_{out,peak}$ equals V_{DD}

3. Class-AB

The Class-AB amplifier is a blend of Class-A and Class-B and strives to offer a compromise in efficiency and performance [4-6].



(a) (b)

Figure 1.10 Class-B topology. (a) Circuit Diagram, (b) Signal transfer function.

In this topology, shown in Figure 1.10, each active element is biased slightly in the saturation region, so there is some overlap between the two at the turn-on/turn-

off center point. This reduces distortion to a low level – typically 1% and even down to 0.1% – at a slight increase in power dissipation. There is a tradeoff between the conduction angle, which is somewhat greater than 180^0, and resulting distortion, with increased conduction angle and associated dissipation yielding lower distortion. Class-AB efficiency is slightly less than that of Class-B, due to the quiescent current that flows from V_{DD} to $-V_{DD}$ when no signal is present.

Due to the compromise between efficiency and distortion that Class-AB offers, it is probably the most commonly used headphone audio amplifier approach.

4. Class-G

The Class-G topology makes use of the fact that music and voice signals have a high crest factor with most of the signal content at lower amplitudes [7-11]. The Class-G topology uses multiple power supplies, operating from the power rail that provides the optimum combination of headroom and power dissipation. A Class-G powered module uses a minimum of two different supply rails. The module operates from the lower supply rail until the signal swing required exceeds what the lower supply rail can accommodate, at which point the module switches the output stage to the higher supply rail. Once the output signal drops below a predetermined level, the module switches back to the lower rail. Power dissipation is greatly reduced for typical musical or voice sources.

Figure 1.11 shows an example where a sine wave is playing through the Class-G amplifier, while the Class-G supply is changing between V_{DD} and $\frac{V_{DD}}{r}$, where r > 1, according to the instantaneous value of the sine wave.

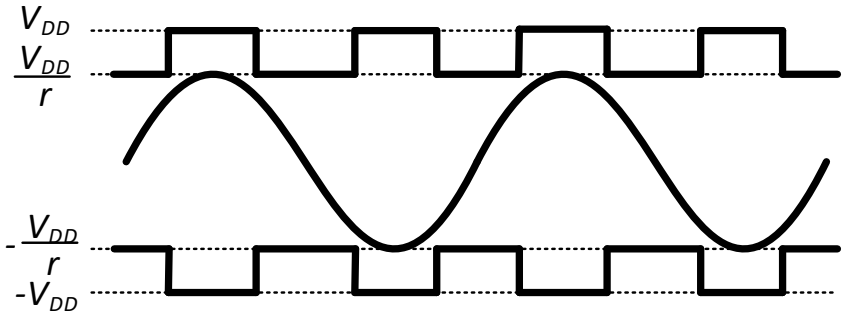


Figure 1.11 Class-G topology, supply modulation

For a sinewave output, with two level supplies, Class-G efficiency is given by:

$$\eta = \frac{\pi r}{4} \frac{\frac{V_{out,peak}}{V_{DD}}}{1 + (r-1)\cos\theta} \tag{1.7}$$

where θ is given by:

$$\theta = \sin^{-1}\left(\frac{V_{DD}}{rV_{out,peak}}\right) \tag{1.8}$$

Figure 1.12 shows a comparison of the power efficiency between Class-AB, two-level Class-G with r=2, and two-level Class-G with r=4, all plotted versus normalized output power $\frac{P_L}{P_{Lmax}}$, where $\frac{P_L}{P_{Lmax}}$ is given by [9]:

$$\frac{P_L}{P_{Lmax}} = \left(\frac{V_{out,peak}}{V_{DD}}\right)^2 \tag{1.9}$$

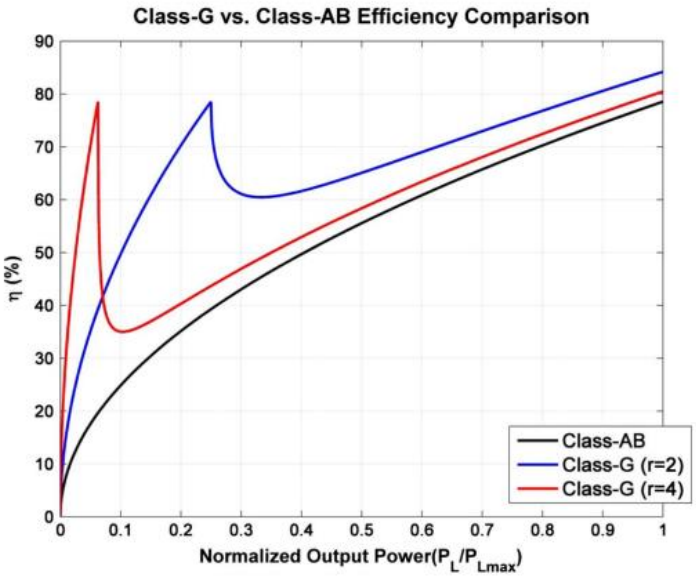


Figure 1.12 Relative comparison between Class-AB, and Class-G (r=2, r=4)

If the supply generation module is assumed to be lossless, then the power consumed from the source must equal to the power delivered to the load, i.e. if the module draws $I_{V_{DD}}$ from the input supply (V_{DD}), then by generating a smaller output voltage $\left(\frac{V_{DD}}{r}\right)$, the output current available to the load increases by the same factor r; i.e,

$$I_{Load} = r\, I_{V_{DD}} \tag{1.10}$$

As an example, if r=2, then the current drawn by the output is halved when referred to the input, which is a huge power saving. Practically speaking, Class-G supply generation circuit is lossy and often times consumes both static and dynamic power, which lowers the overall achieved efficiency improvement.

Although the Class-G idea looks very attractive, it suffers from the following disadvantages:

1. Due to the limited slew rate of the supply generation circuit, it is hard to use it over the entire audio band. Thus, the power savings is only limited to low-frequency audio, and the supply is fixed at V_{DD} for the high-frequency content.
2. To prevent excessive distortion to the output signal, it is critical that the supply generation circuit switches back from $\frac{V_{DD}}{r}$ to V_{DD} at the correct time. If any delay is incurred, it would result in increased distortion. Usually, enough margin is implemented in the transition point to make sure that under worst propagation delay, the output signal is still perfect. This margin is another limitation on how much power saving can be achieved.

5. Class-H

Class-H amplifiers take the idea of Class-G one step further creating an infinitely variable supply rail [12-13]. An example of a class-H amplifier is shown in Figure 1.13.

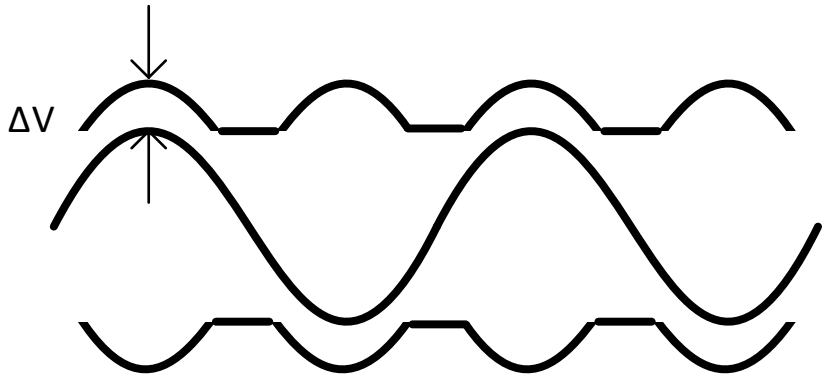


Figure 1.13 Class-H topology, supply modulation

A Class-H supply is usually designed to leave a fixed headroom (ΔV) on each side to keep the distortion low while maximizing the efficiency, given by:

$$\eta = \frac{V_{out,peak}}{V_{out,peak} + \frac{4\Delta V}{\pi}} \tag{1.11}$$

Although Class-H presents more efficiency improvement, it comes with the same disadvantages as in Class-G: (1) lacking the ability to track the signal over the entire audio band, and thus limiting the efficiency improvement to low frequency and (2) the inherent tradeoff in the choice of ΔV to avoid any instantaneous misalignment between the signal and the supply.

The Class-H positive supply is usually generated by a buck converter that receives its reference from the same digital engine that sends the audio signal to be played back. A digital word representing the instantaneous supply value is received, then converted to analog and used as a reference for the buck converter loop as shown in Figure 1.14.

The negative supply can be generated by an inductor-based flyback loop as in Figure 1.14, or by simply taking the buck output and inverting it using a negative charge pump (NCP).

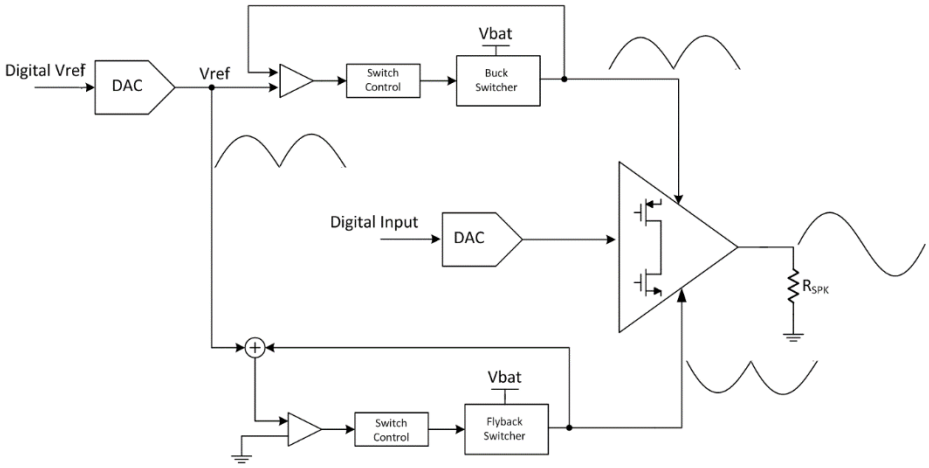


Figure 1.14 Class-H amplifier supplies by a buck converter (positive supply), and flyback converter (negative supply)

It is worth noting that both the buck and flyback (or NCP) dissipated additional quiescent currents, which adds to the overall power consumption. In addition, this solution uses two external inductors on the PCB in order to generate the required supplies.

b. Switching topologies

The Class-D is the most common switching topology in which the output stage devices operate as switches, and not as linear gain devices as in the linear topologies. These switches commutate between the supply rails to generate a train of pulses, which represent the required output signal modulated by a high-frequency carrier. The modulation scheme can be either pulse width, or pulse density modulation. The output audio content can be retrieved back by low-pass filtering before being applied to the speaker [15,17]. Since the output devices are never both "on" at the same time, only one device is used to connect either supply to the output, and since each switch is ideally either an open circuit or a short circuit, they dissipate very low power, resulting in very high efficiency, often close to ~90%.

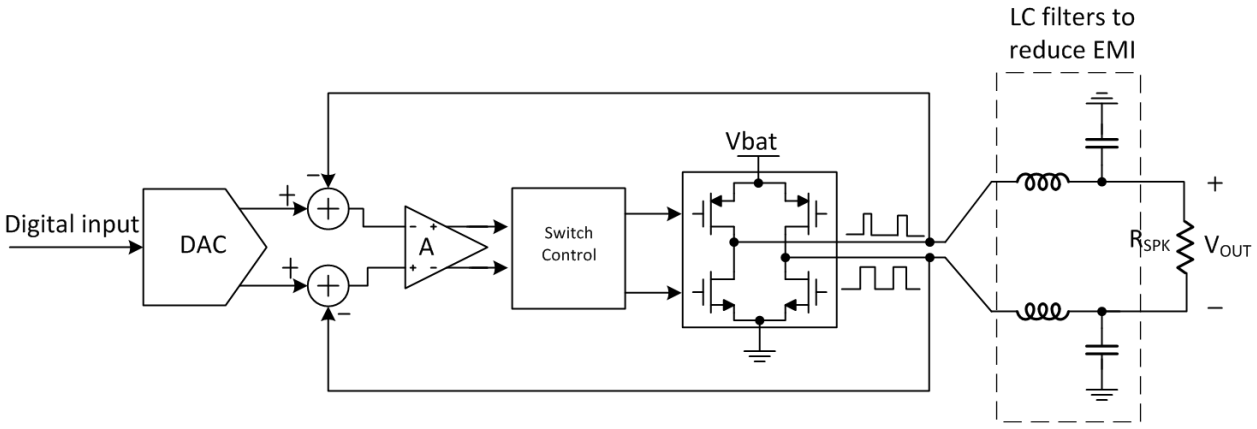


Figure 1.15 Class-D loop driving differential loudspeaker load

A Class-D amplifier can be used in a single-ended (SE) structure to drive single-ended loads such as headphone, or in a differential structure known as bridge-tied-load (BTL) for differential loads such as speakerphones as shown in Figure 1.15. The Class-D amplifier is characterized by the need for a series external LC filter to reduce the high-frequency content and smoothen the output sharp edges in order to comply with electromagnetic interference (EMI) requirements. Placing the LC filter close to the chip ensures that radiated emission from either the PCB traces or the connected wires, which could act as antennas, is limited.

Due to the required high output power for speakerphone applications, the Class-D amplifier has been commonly used in the literature. For an output power as high as 5-10W, the power dissipated on the chip is nearly 10% (0.5-1W) if the Class-D is used. In comparison to other power amplifier classes, limiting the on-chip power dissipation by choosing the Class-D topology saves on the required chip area needed to dissipate the heat to maintain a reasonable device junction temperature.

Next, the pros and cons for the different modulation schemes to encode the data for Class-D are discussed followed by a discussion of the main drawbacks of using the Class-D for high-fidelity applications

Class-D modulation schemes:

1. Pulse-Width Modulation (PWM)

   This is the most widely used scheme due to the simple circuitry and low power dissipation. In this type, the PWM is generated by comparing the output of the error amplifier shown in Figure 1.15 to a sawtooth periodic signal at the

carrier frequency to produce PWM train of pulses as shown in Figure 1.16 [15,17].

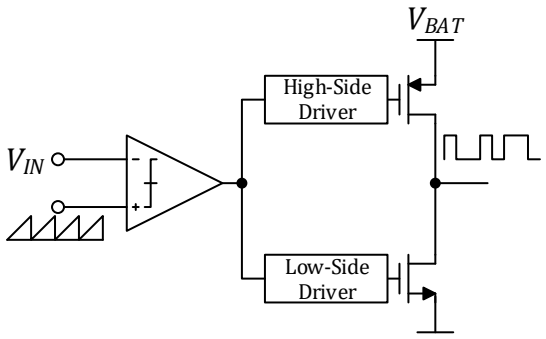


Figure 1.16 Block diagram for PWM switch control

2. Sigma-Delta Modulation (ΣΔ)

In this modulation scheme, the error amplifier output is quantized into a single bit using a synchronous comparator as shown in Figure 1.17.

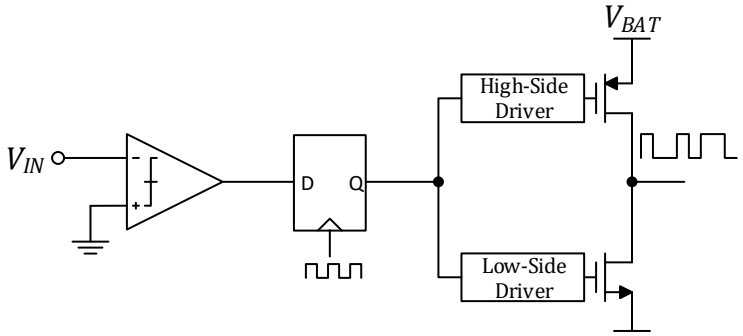


Figure-17 Block diagram for ΣΔ switch control

By choosing higher carrier frequency, the non-linearities and in-band quantization noise, can be reduced. However, this comes at the cost of higher dynamic power, and added complexity to maintain the fidelity of the high-frequency clock source. Another option is to use a higher-order modulator, which increases the hardware complexity and the power dissipation.

3. Sliding-mode Control

In this type, the synchronous comparator is replaced by a hysteretic comparator as shown in Figure 1.17 resulting in a variable carrier frequency as a function of the signal [14,16], thereby, eliminating issues related to the fidelity of the clock source as well as all quiescent current needed to generate it.

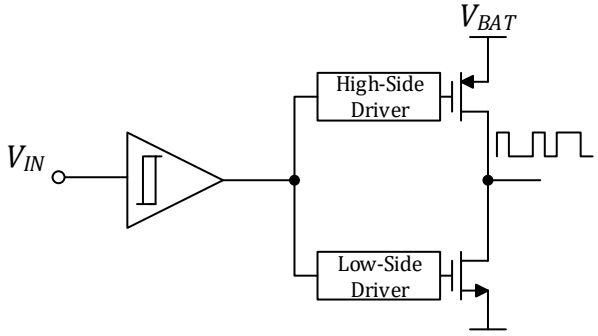


Figure 1.17 Block diagram for a sliding mode switch control

Drawbacks for using Class-D for high fidelity applications:

All types of Class-D loops suffer from higher THD due to the following reasons:

a. A typical Class-D output spectrum shown in Figure 1.18 has the signal and distortion components present around the carrier frequency (and its harmonics), and since the loop internally mixes the fed-back output spectrum with the carrier frequency, it inadvertently folds back the distortion components into the audio band and thereby reducing the THD+N.

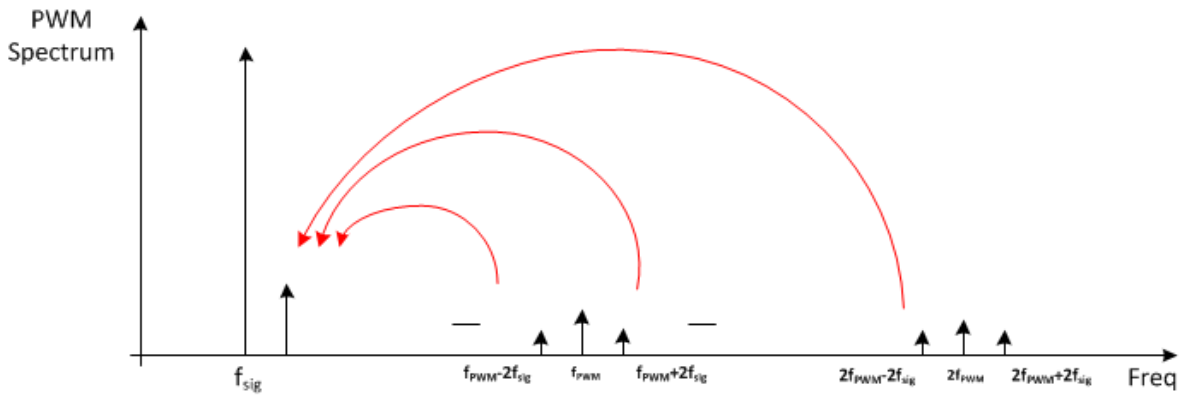


Figure 1.18 Illustration of the nonlinearity foldback issue in Class-D

b. Except for the sliding mode control, all other modulation schemes have a fixed carrier frequency, which is usually chosen to guarantee high loop bandwidth at the signal zero crossings. When the signal is at its positive or negative peak, the loop doesn't need to have the same carrier frequency and therefore dissipates more dynamic power than necessary.

c. As described before, an LC output filter is needed to comply with the stringent EMI specifications. If either the inductance and/or the capacitance exhibits variation as a function of the signal amplitude, the audio band gain may vary as a function of the signal amplitude resulting in added distortion components.

1.9 Focus of this dissertation and flow of next chapters

This dissertation focuses on increasing the overall PA efficiency by using a switching topology while maintaining high fidelity performance similar to the linear topologies. Sliding-mode control is employed to implement a Class-D loop while an additional current sensing loop is implemented in order to improve the THD+N without increasing the loop order or the carrier frequency.

In chapter 2, a summary of most recent or widely used state-of-the-art headphone amplifier designs is presented and discussed. In chapter 3, the proposed system architecture is introduced along with an analysis of the loop dynamics and an explanation of the system advantages. Chapter 4 explains the design of the key analog building blocks in details. Experimental results are discussed in Chapter 5, and a summary of the work and conclusions are discussed in chapter 6.

CHAPTER 2 State-of-the-art designs

In this chapter, several recent publications covering the topologies that were discussed in Chapter 1 are presented. The focus is on the innovations in these papers as well as their measurement results.

2.1 JSSC Oct 2016 Class-G [8]

In this paper, a load-adaptive Class-G headphone amplifier with supply-rejection bandwidth enhancement technique was introduced. Depending on the load impedance, the amplifier selects proper voltage rails and controls the Class-G switching activities to minimize the power loss of the amplifier and the Class-G power generator.

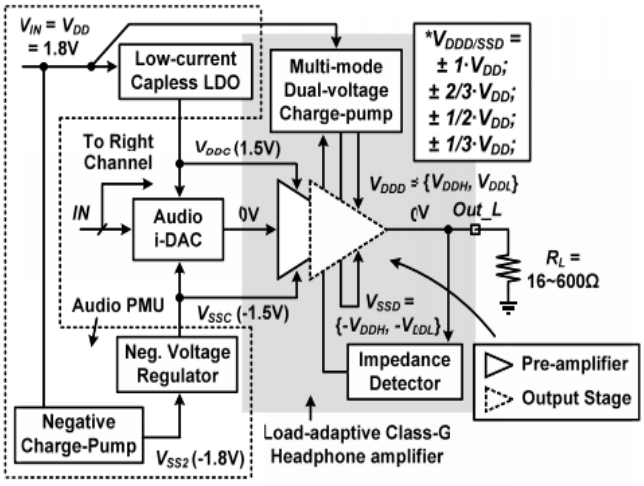


Figure 2.1 Load-adaptive Class-G stereo headphone amplifier architecture

Figure 2.1 depicts the architecture of the load-adaptive Class-G stereo headphone amplifier, which is powered from a 1.8 V output buck converter with 85% efficiency. The amplifier consists of two identical audio channels with an audio power

management unit (PMU). The PMU includes a negative charge pump (NCP) that provides a fixed –1.8 V negative supply, a low-current capless LDO, and a negative-voltage regulator, which provide regulated supplies to the critical analog circuits. A multi-mode dual-voltage charge-pump (MMDV-CP) and an impedance detector are embedded in the amplifier for the load-adaptive Class-G operation. The MMDV-CP generates either a high (±VDDH) or a low (±VDDL) supply level according to the input digital signal level, where the values of VDDH and VDDL are decided by the headphone impedance and the gain setting of amplifiers. For different impedance levels, the charge-pump can provide four voltage rails ($\pm V_{DD}$, $2/3V_{DD}$, $1/2V_{DD}$ and $1/3V_{DD}$) to best fit the signal profile and reduce the power loss of the amplifier. The Class-G switching scheme is mainly determined by the power efficiency of the MMDV-CP. Frequent switching of the supply rails is prohibited if the increase of the current efficiency by the Class-G operation is less than the current dissipated by the Class-G charge-pump. Different from heavy loads (under 50Ω), the load current reduction by the Class-G operation for light loads is not obvious. For the same output power requirement, the load current delivered to a 600Ω is much smaller than the current into a 16Ω load.

To improve the power efficiency of the Class-G charge pump during the supply rails switching, a hold-time mechanism is used in the charge-pump controller design to prevent frequent switching of the supply rails. By increasing this hold time, the switching power loss of the Class-G charge-pump is reduced. For higher headphone impedance with less current benefit by the Class-G operation, a longer hold time is recommended to reduce the power loss of charge pump. The switching period for

their realization is set to 1msec, and the hold time for a 600Ω load is approximately 40msec. In addition, the authors highlighted the underlying PSRR issue in the Class-G output stages, where the supply switching due to the Class-G operation may degrade audio signal quality. The authors introduced an additional correction loop within the PA to help reduce this effect.

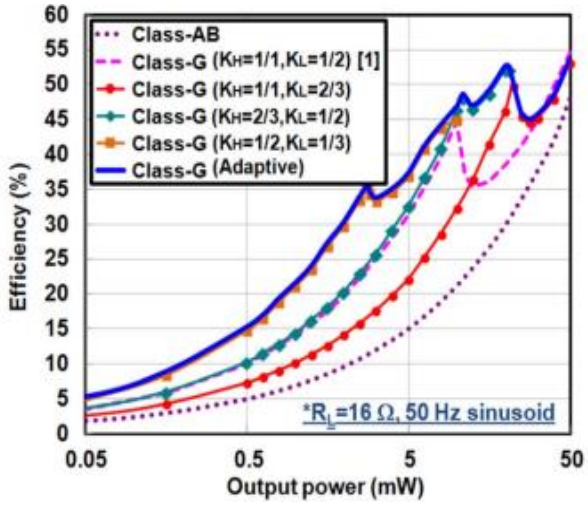


Figure 2.2 Total-path efficiency versus output power level

The authors solution achieves a maximum output power of 62mW, 108 dB DR, -95dB minimum THD+N, and 1.35mA/channel quiescent current from the 1.8V supply.

Figure 2.2 shows the total path power efficiency comparison between this solution, several other Class-G solutions (with different supply configurations), and the classical Class-AB implementation. Due to the adaptive nature of this design, the power efficiency tracks the envelope of the several other Class-G solutions, which of course comes at the expense of added complexity and circuitry that enables the supply to track the gain and load changes.

2.2 JSSC Nov 2014 Class-D [17]

In this paper, the authors implemented several techniques to enhance THD+N and PSRR for the classical Class-D audio driver.

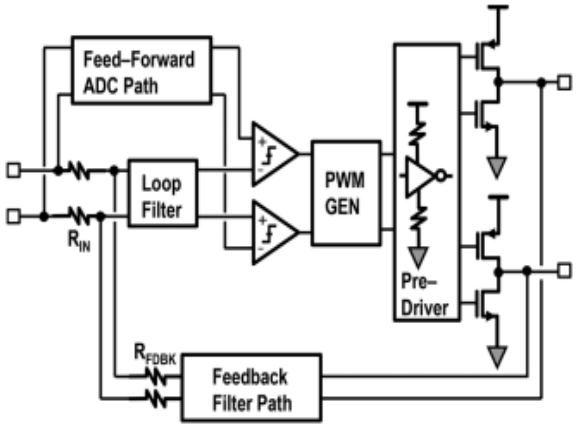


Figure 2.3 Class-D structure of the JSSC Nov 2014 paper

The architecture shown in Figure 2.3 includes a feed-forward ADC path, feedback filter, and edge-rate control in the driver stage. The feed-forward path is designed to process the signal so that the loop filter can process only the difference between the input and the feedback signals. Thus, the loop filter responds primarily to errors injected into the loop. This architecture extends the operating range of the loop filter to support a larger signal level and, therefore, a larger output power capability. To avoid PSRR performance degradation due to the feed-forward architecture, the loop filter, feedback, and feed-forward paths are powered by an internally-compensated LDO, which consumes 50 µA of quiescent current and requires less than 1% of the Class-D amplifier area. Instead of using simple resistor feedback, the proposed architecture includes filters in the feedback path to reduce the high-frequency intermodulation distortion associated with

direct feedback and eliminate the loop filter input common-mode disturbance from the Class-D output. The design is implemented using a 180 nm CMOS and achieves 1.75 W into an 8Ω speaker, 105 dB SNR, 95% efficiency, -88dB peak THD+N, and 96dB PSRR at 217Hz. The quiescent current is not reported but can be estimated to be close to 5mA from the efficiency plot.

2.3 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS

Sep 2016 Class-AB [4]

In this paper, the authors are focused on optimizing the quiescent current consumption of the headphone driver. This is done by an attempt to solve a classical problem in which the transconductance of the output stage of a linear amplifier design has a wide variation as a function of the load current, and therefore stability optimization becomes complicated. A brute-force solution is to conduct enough quiescent current in the output stage, so the stability is guaranteed in the worst case (i.e. for a zero-amplitude output). In this paper, the authors propose a new solution where the output load current is sensed and used to adjust the second-stage pole for a Class-AB three-stage driver to guarantee the stability for all load current conditions. Figure 2.4 shows the Class-AB amplifier used, which consists of three stages and a current sensing block, which senses the load current through the gate voltage of the output devices and controls the small signal resistances of M21 and M22 inside the second stage to change the second pole location as a function of the load current.

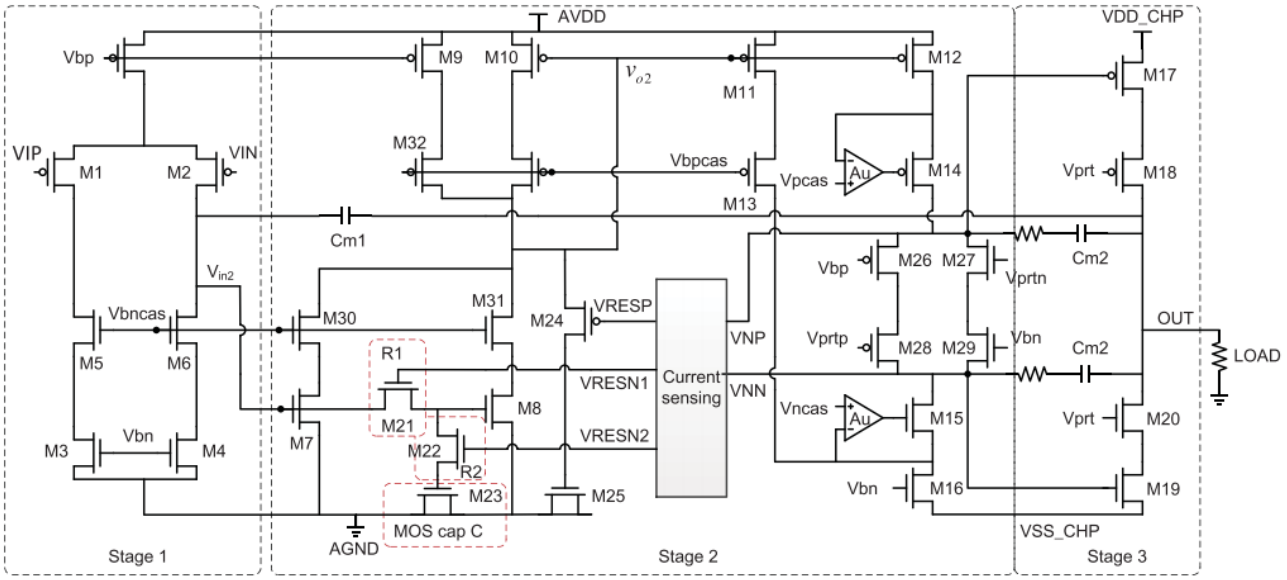


Figure 2.4 Class-AB driver schematic

The prototype chip is implemented in a 55 nm CMOS process. The measured static current consumption of the core circuit is 0.35 mA with a 1.8 V supply voltage. Measurement verified −85 dB THD+N, 106 dB signal dynamic range, and 55 mW output power under a wide range of load capacitances from 5 pF to 20 nF.

Figure 2.5 shows the measured THD+N vs signal for the driver when powered by a fixed supply and a Class-G supply. The THD+N degradation starts approximately at a signal amplitude of -18dBV for both cases but gets much worse for Class-G supply.

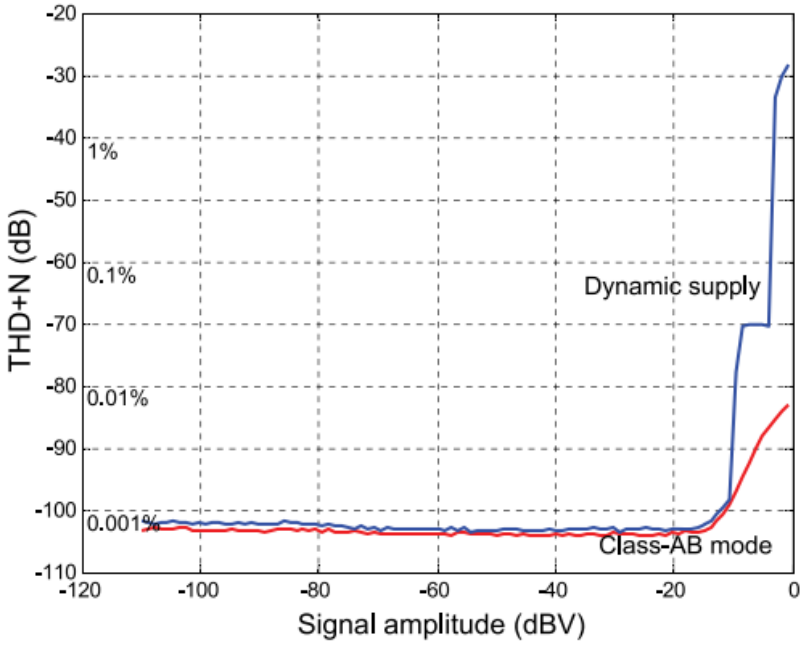


Figure 2.5 Measured A-weighted THD+N versus input signal amplitude for 1 kHz signal frequency, 0 dB gain

2.4 IEEE TRANSACTIONS ON VLSI SYSTEMS JUNE 2017

Class-H [13]

This paper presents a Class-H power amplifier aiming for audio applications on battery-powered electronic devices. The power supply of the amplifier is adaptively adjusted to track the instantaneous input signal amplitude for higher power efficiency. By embedding audio input signal amplitude information into the Class-AB amplifier's output common-mode voltage level, the amplifier can operate with only single-rail power supply. This solution is not applicable as a headphone driver because it assumes a differential load and thus it uses a differential amplifier.

However, it is still useful to discuss this paper here to develop some understanding of the achievable THD performance when Class-H is used.

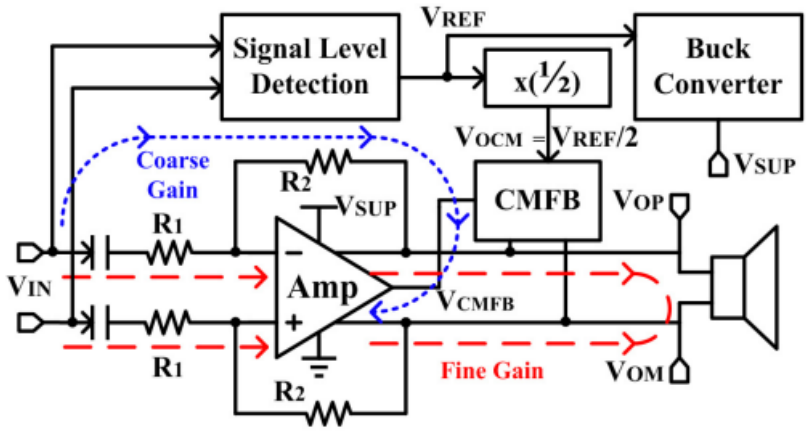


Figure 2.6 System-level illustration of the proposed Class-H amplifier

Figure 2.6 illustrates the proposed amplifier, which consists of three building blocks: A fully differential Class-AB amplifier, an input amplitude detection (IAD) block, and a buck converter. The audio input signal VIN is fed simultaneously into the main Class-AB amplifier as well as the IAD block, through which, the instantaneous signal amplitude is measured and processed. Output voltage VREF is used as the reference voltage of the buck converter. To ensure maximal output swing at all times, 1/2 VREF is taken as the reference voltage to the common-mode feedback (CMFB) circuit of the Class-AB amplifier VOCM.

As illustrated in Figure 2.7, the proposed design has two operation modes, which are dependent on the input signal amplitude. For small input signal levels, the amplifier works like a normal Class-AB amplifier with its output CM level VOCM biased at half of VDDL. When the input signal exceeds this threshold, the system

enters Class-H mode where VOCM tracks the extracted reference voltage. This process makes one of the output nodes swing up with a doubled gain and the other stay at a predefined dc level VDSAT.

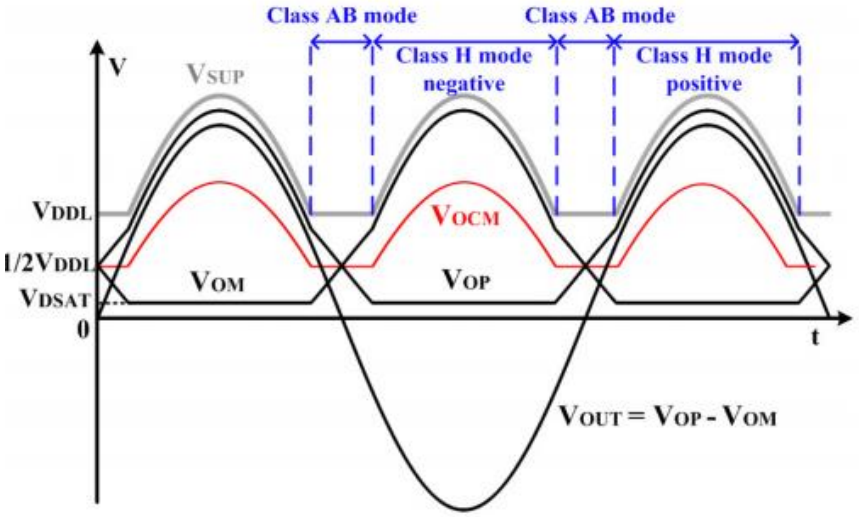


Figure 2.7 Amplifier output waveforms with sinusoidal input signals

The prototype was fabricated in a 0.18-μm CMOS process, and consumes 3.52 mW quiescent power, not including the supply generation circuit. The circuit is able to deliver up to 263 mW peak output power to a 16Ω load and achieves a peak THD+N ratio of −80 dB. The peak power efficiency of the system is 80.4%. Figure 2.8 shows the measured efficiency plot. Quite interestingly the authors argued that using Class-H instead of Class-D reduces the external component cost because of saving the external LC components; however, in order to generate the Class-H supply, the authors had to use a buck converter, which inevitably uses an external LC filter.

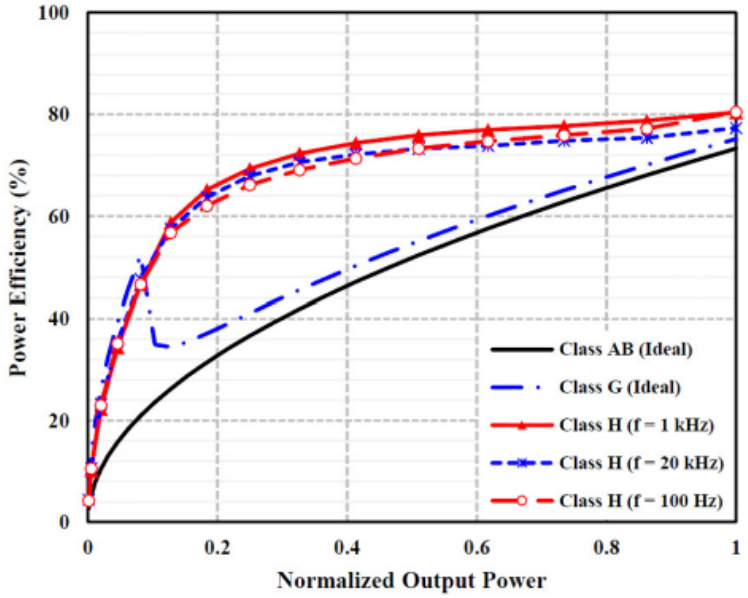


Figure 2.8 Class-H measured efficiency plot

2.5 JSSC Oct 2011 Sliding-mode class-D [14]

A hysteretic modulator consisting of a third-order self-oscillating Class-D audio amplifier that utilizes a hysteretic comparator is presented. The hysteretic modulator potentially allows for a low-cost implementation by eliminating the requirement for an external high-quality carrier. The authors argued that one of the concerns in the design of hysteretic modulators is the decrease of the switching frequency with input amplitude, which can deteriorate the loop gain and linearity performance as the output power level increases, or even cause stability problems in a high-order design. As a solution, the authors presented a frequency stabilization

technique based on continuous variation of the hysteresis window in response to the input amplitude to minimize the variation of the switching frequency.

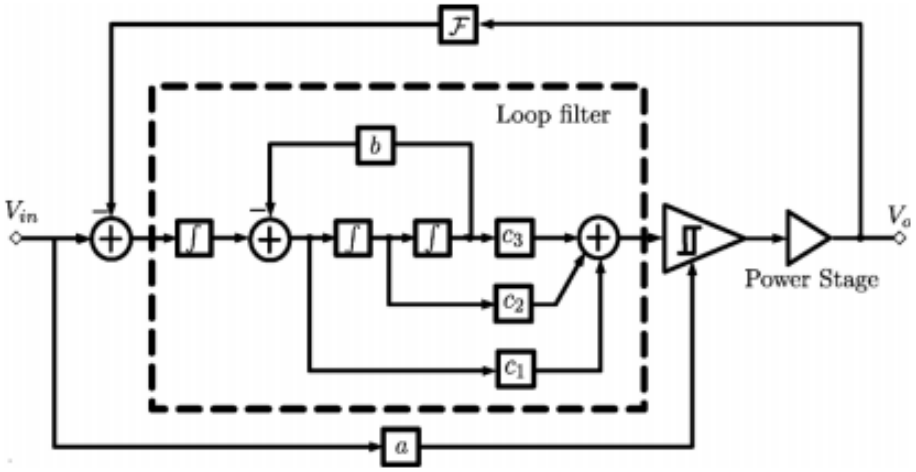


Figure 2.9 Sliding-mode system architecture

Figure 2.9 shows the system architecture used in this paper, which consists of a third-order loop with a hysteretic comparator. For such a high-order loop filter, the swing of the first integrator is limited by the hysteretic comparator itself; however, the last two integrators, are prone to clipping due to power supply limitation when the integrators try to generate a large error correction term in response to a large input. When the switching frequency decreases below a certain value, the output of the third integrator clips, and the loop gain, and error correction degrade rapidly. Consequently, the performance becomes worse than that of a first-order modulator.

To alleviate this degradation, the hysteresis factor is varied in response to the input level, so that the switching frequency can be adjusted properly to reduce the swing of the last integrator. By using this technique, high linearity is achieved with consistent distortion performance up to relatively high-power levels; i.e., nearly 90% of the maximum output power.

The chip prototype is implemented in a 0.7μm CMOS process and realizes a fully differential topology driving an 8Ω load while achieving DR of 116.5 dB, a THD+N of 0.0012%, and output power of 125 mW. Using a 5V power supply the amplifier can deliver 1.45 W into the load with a 5% THD. The efficiency is greater than 84% for output power larger than 1 W. The authors did not report the power consumption, but it can be estimated that the quiescent current is about 20mA from their efficiency plot.

Figure 2.10 shows the measured THD+N vs the output power.

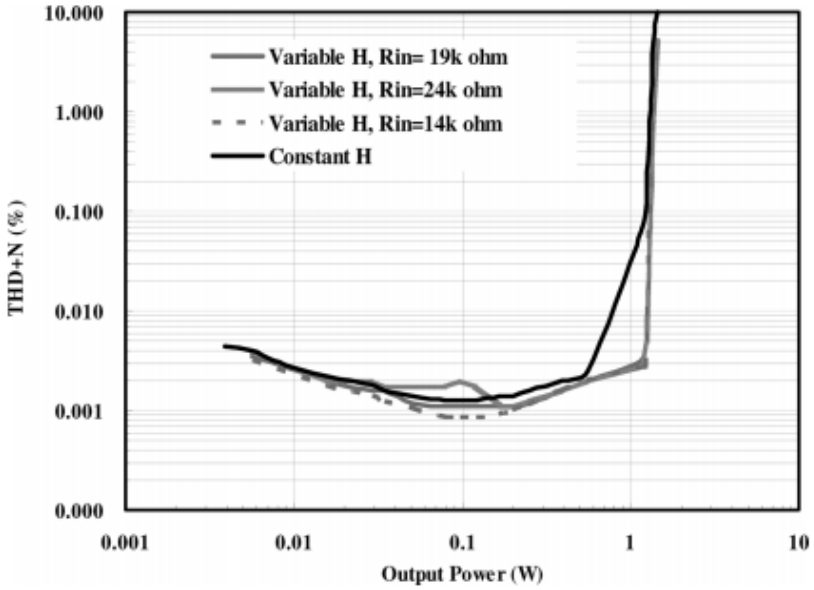


Figure 2.10 Measured THD+N vs output power plot

CHAPTER 3 Proposed System Architecture

3.1 Architecture

The proposed architecture is a switching topology that consists of a single-ended switching output stage followed by an LC filter whose output is fed back to the error amplifier. A simplified version of the system architecture is shown in Figure 3.1.

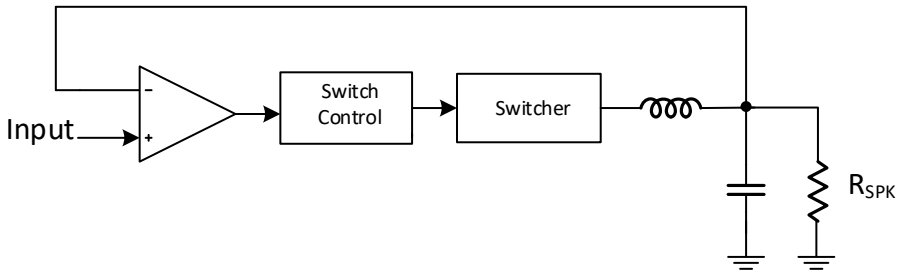


Figure 3.1 Simplified proposed architecture

Unlike classical switching topologies, the LC loop filter is included in the feedback loop, which offers several advantages:

1. Attenuating the output switching ripples:

The PWM spectrum has a low-frequency signal content in addition to the upconverted signal and harmonics around the carrier frequency, as shown in Figure 3.2. Since, the output signal is fed back to the error amplifier, whose output gets sampled within the loop, the harmonic content around the carrier frequency gets mixed with the carrier frequency and all the harmonics are folded back into the audio band, degrading the linearity of the system as shown in Figure 3.2a. The proposed architecture addresses this point by including the LC filter within the loop

before the feedback point, thereby filtering the output of the switching stage before being fed back. Depending on the LC corner frequency, the high-frequency harmonics are attenuated, and the audio foldback can be tolerated, which results in overall better linearity performance as shown in Figure 3.2b.

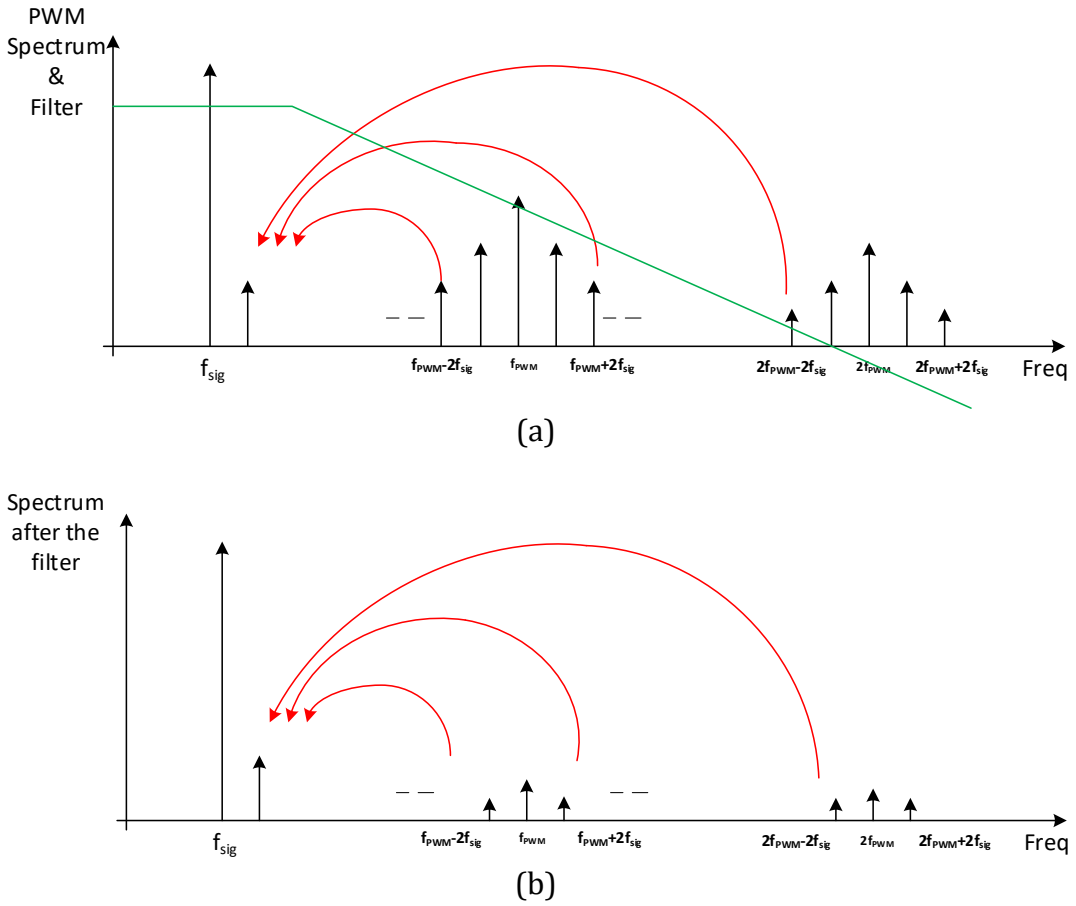


Figure 3.2 (a) PWM spectrum before filter and filter response, (b) PWM spectrum after filtering.

2. LC filter non-linearity is also attenuated:

The switching topologies usually employ an LC filter to attenuate the Electromagnetic Interference (EMI), which is an FCC requirement [22]. The LC filter is typically placed off-chip between the Class-D driver and the load. However, the

variations of the inductance and capacitance [23, 24] can lead to a variation of the audio band gain as a function of the signal swing, which translates into distortion.

In the proposed architecture, since the LC is pushed inside the loop, any change to the corner frequency is corrected by the negative feedback action, and therefore the distortion components are attenuated by the in-band loop gain.

3.2 Power Stage and Control Scheme.

Before discussing the details of the system design, it is important to first discuss the power stage architecture to lay foundations for later discussions on how the system control works. More detailed discussion on the power stage details and comparison against other possible options will be elaborated on in Chapter 4. Figure 3.3 shows a simplified version of the power stage, which is a half-bridge Class-D topology with dual supplies (also known as a buck converter).

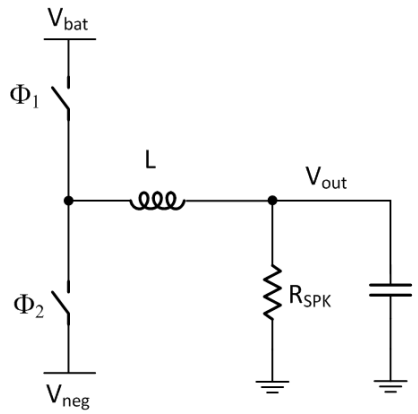


Figure 3.3 Simplified power stage

The high- and low-side switches, usually PMOS and NMOS respectively, are controlled by a non-overlapping clock generator that is embedded inside the switching control block as shown in Figure 3.4.

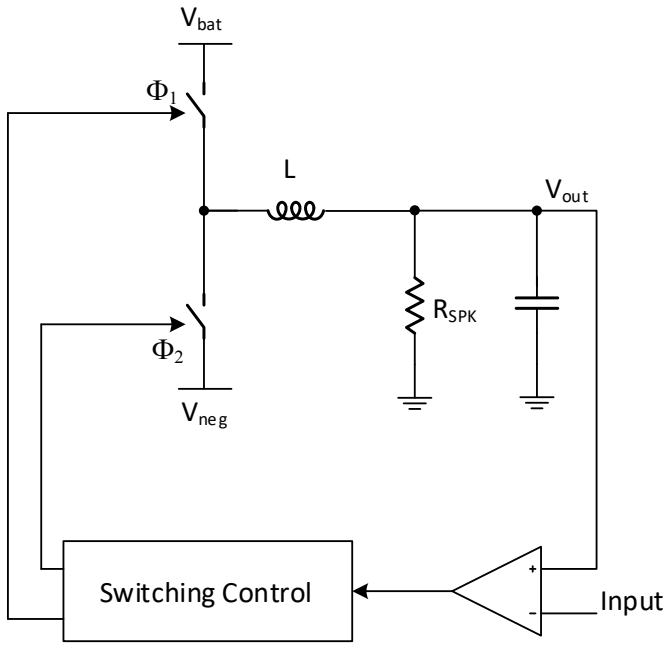


Figure 3.4 A simplified block diagram for the switching regulator

The switching control block receives an error signal that results from comparing the output to the input signal. This error signal then drives the output stage to ensure the output tracking. The switching regulator loop, as the name implies, converts an input voltage to a desired output voltage by turning the input voltage on and off; i.e., this method involves chopping the input voltage and smoothing it out to match the required output voltage. There are two principal methods by which the input voltage is chopped:

(1) Pulse Frequency Modulation (or Discontinuous Conduction Mode), abbreviated as PFM/DCM [25].

(2) Pulse Width Modulation (or Continuous Conduction Mode), abbreviated as PWM/CCM [25].

Details on how the two schemes work are described below.

3.2.1 PFM/DCM Approach

The PFM method is of two types: fixed-on time or fixed-off time. An example of the fixed-on type is shown in Figure 3.5, for which on-time is fixed, and off-time is variable; this means that the length of time it takes for V_{bat} to connect to the output next time varies. When the load current increases, the number of on-times in a given length of time is increased to keep pace with the load. Thus, under a heavy load, the frequency increases, and under a light load it diminishes.

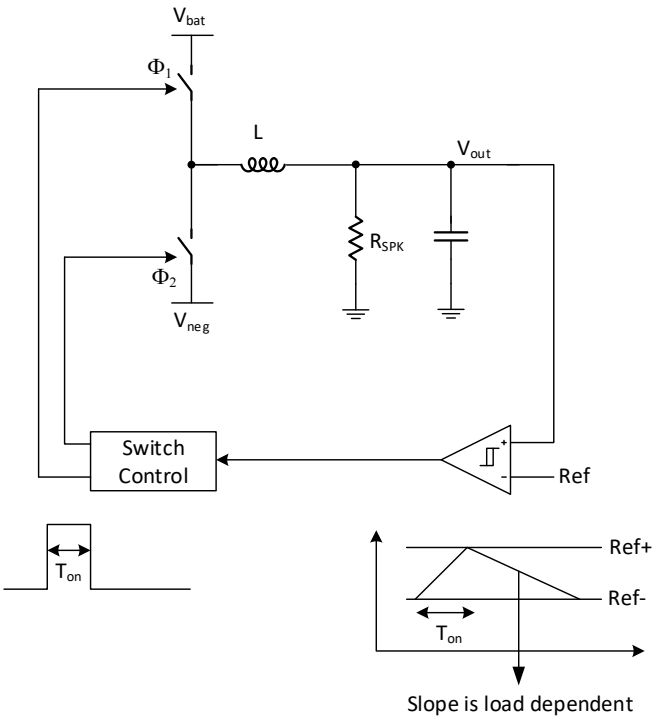


Figure 3.5 Fixed on-time PFM/DCM scheme

Figure 3.6 shows how the output stage control, inductor current, and output voltage vary under a light load condition. The output voltage is bounded between two levels set by V_{High} and V_{Low}, and the output is continuously being compared against these 2 thresholds, and once it falls below the lower threshold, V_{Low}, the control block enables the high-side switch for a fixed period T_{ON}, during which the current in the inductor ramps up from 0 to I_{Peak}. As a result, V_{OUT} increases, then follows a period T_{OFF} during which the inductor current ramps down to zero. The operation repeats until V_{OUT} reaches the high threshold V_{High}, after which V_{OUT} is left unregulated while the output capacitor discharges because of the current loading. Once V_{OUT} drops below V_{Low}, the overall procedure repeats.

This scheme is attractive to use for light loading condition, because of the reduced switching frequency, which translates to less dynamic power losses and thus, higher efficiency. On the negative side, for a light load the loop is kept unregulated during $T_{OFF,}$ which means that for an audio input, no rejection of any nonlinearity or disturbance is applied during this time, and therefore distortion or supply disturbances may impact the fidelity of $V_{OUT.}$

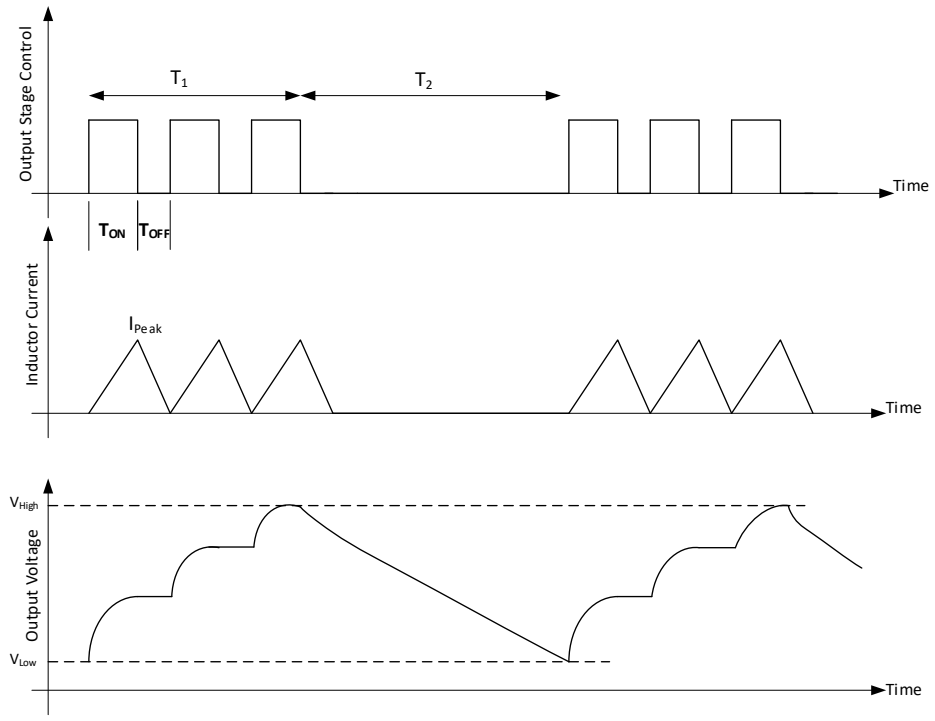


Figure 3.6 Output stage control, inductor current, and output voltage for PFM/DCM scheme

3.2.2 PWM/CCM Approach

The PWM method represents the most commonly employed voltage control method. In this method, the duty cycle of the switching pulses changes to produce the required average output value. The switching action is continuous even for a light load, which forces the output to follow the audio input at the expense of more switching losses and less efficiency compared to PFM.

The continuous switching action for CCM enables the continuous application of a negative feedback mechanism. This ensures that the average output can follow the input signal closely while rejecting the disturbance on either the negative or positive switching stage supply by modulating the pulse width.

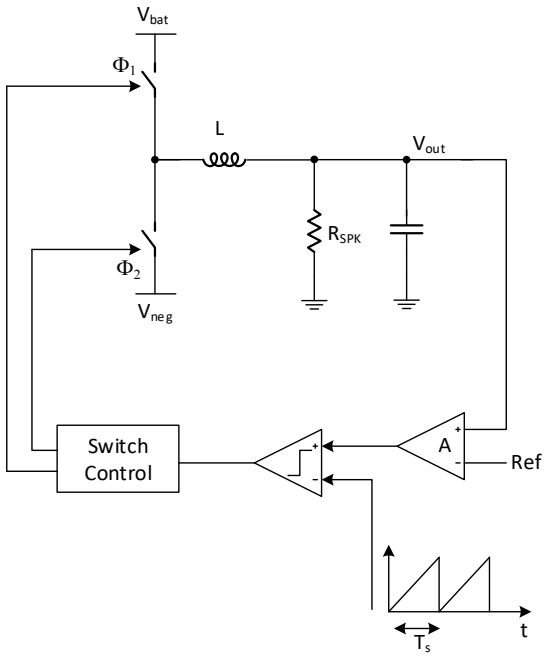


Figure 3.7 PWM/CCM control scheme

Figure 3.7 shows an example for a PWM system, where an error amplifier with large gain (A) compares the input reference with the output, from which the error signal is compared to a periodic sawtooth waveform with a frequency ($1/T_S$). Thanks to the sawtooth waveform, the comparator output can produce a pulse-width-modulated signal as a function of the error amplifier output. Slope compensation is often required for PWM systems if the output duty cycle is larger than 50% to prevent loop instability [25].

In this work PWM is used to ensure that the audio output can track the input reliably for all input levels and load conditions.

3.3 Study of Loop Stability

3.3.1 Switcher AC model

To study the PWM loop stability, an ac model for the switcher needs to be devised and all the required parameters for the ac model are labeled on Figure 3.8.

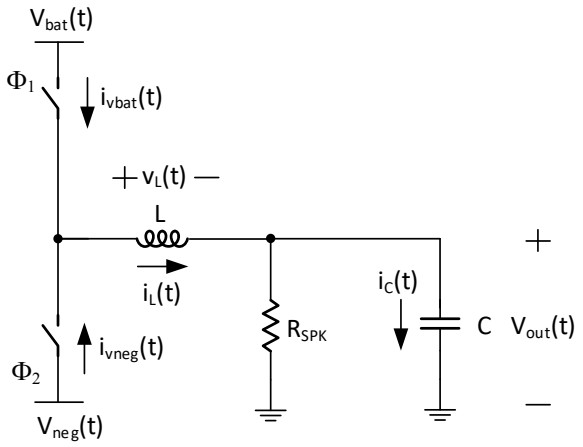


Figure 3.8 Output stage diagram with the ac model parameters labeled

Clock phases ϕ_1 and ϕ_2 are assumed to be non-overlapping with duty cycle d(t) and d'(t) respectively, and a period T_S. Each of the parameters shown in Figure 3.8 has a low- frequency, and high-frequency component due to the switching action. For example, V_{bat} carries a DC value and a high-frequency switching ripple while $V_{out}(t)$

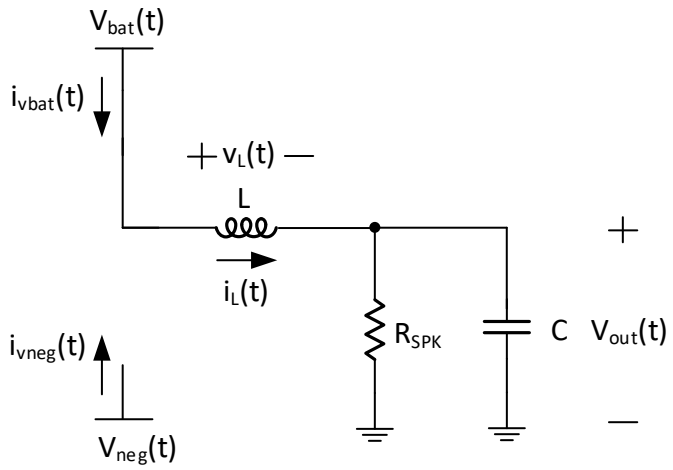


Figure 3.9 Output stage during ϕ_1

carries the output audio signal and a high-frequency switching ripple. For the purpose of the stability analysis, the high-frequency ripples are eliminated, and the moving average technique is used to extract the low-frequency content for $v_{bat}(t)$, $v_{neg}(t)$, $v_{out}(t)$, $i_L(t)$ in order to calculate the average value for $v_L(t)$, $i_C(t)$, $i_{vbat}(t)$, and $i_{vneg}(t)$ in both phases.

During ϕ_1, the output stage can be simplified as shown in Figure 3.9, and the following equations hold:

$$v_L(t) = \langle v_{bat}(t) \rangle_{T_S} - \langle v_{out}(t) \rangle_{T_S} \tag{3.1}$$

$$i_C(t) = \langle i_L(t) \rangle_{T_S} - \frac{\langle v_{out}(t) \rangle_{T_S}}{R_{SPK}} \tag{3.2}$$

$$i_{vbat}(t) = \langle i_L(t) \rangle_{T_S} \tag{3.3}$$

$$i_{vneg}(t) = 0 \tag{3.4}$$

Where $\langle x(t)\rangle_{T_S}$represents the moving average for $x(t)$ over one period and is given by:

$$\langle x(t, T_S)\rangle_{T_S} = \frac{1}{T_S}\int_{t}^{t+T_S} x(\tau)d\tau \tag{3.5}$$

Since $x(t)$ represent a stationary process, then $\langle x(t, T_S)\rangle_{T_S}$= $\langle x(t)\rangle_{T_S}$

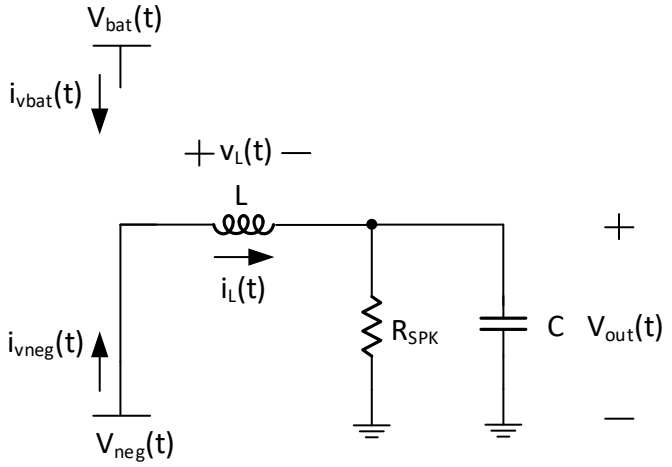


Figure 3.10 Output stage during ϕ_2

During ϕ_2, the output stage can be simplified as shown in Figure 3.10:

$$v_L(t) = \langle v_{neg}(t)\rangle_{T_S} - \langle v_{out}(t)\rangle_{T_S} \tag{3.6}$$

$$i_C(t) = \langle i_L(t)\rangle_{T_S} - \frac{\langle v_{out}(t)\rangle_{T_S}}{R_{SPK}} \tag{3.7}$$

$$i_{vneg}(t) = \langle i_L(t)\rangle_{T_S} \tag{3.8}$$

$$i_{vbat}(t) = 0 \tag{3.9}$$

Now that $v_L(t)$, $i_C(t)$, $i_{vbat}(t)$ average values are calculated in ϕ_1 and ϕ_2 where the duty cycle is d and d' respectively, a weighted average over the entire cycle is given by:

$$\langle v_L(t)\rangle_{T_S} = d(t).\left[\langle v_L(t)\rangle_{T_S}\right]_{\emptyset 1} + d'(t).\left[\langle v_L(t)\rangle_{T_S}\right]_{\emptyset 2}$$

$$= d(t).\langle v_{bat}(t)\rangle_{T_S} + d'(t).\langle v_{neg}(t)\rangle_{T_S} - \langle v_{out}(t)\rangle_{T_S} \quad (3.10)$$

$$\langle i_C(t)\rangle_{T_S} = \langle i_L(t)\rangle_{T_S} - \frac{\langle v_{out}(t)\rangle_{T_S}}{R_{SPK}} \quad (3.11)$$

$$\langle i_{vbat}(t)\rangle_{T_S} = d(t).\langle i_L(t)\rangle_{T_S} \quad (3.12)$$

$$\langle i_{vneg}(t)\rangle_{T_S} = d'(t).\langle i_L(t)\rangle_{T_S} \quad (3.13)$$

For the purpose of the stability analysis, an ac perturbation is applied to d and d' such that $d(t) = D + \hat{d}(t)$ and $d'(t) = D' - \hat{d}(t)$. Due to this perturbation, each of the current and voltage variables (e.g. x(t)) can now be assumed to have two low-frequency components: Intended low-frequency content (X) and an ac component ($\hat{x}(t)$).

Substituting into (3.10) -(3.13) results in:

$$V_L + \hat{v}_L(t) = \left(D + \hat{d}(t)\right).\left(V_{bat} + \hat{v}_{bat}(t)\right) + \left(D' - \hat{d}(t)\right).\left(V_{neg} + \hat{v}_{neg}(t)\right) - \left(V_{out} + \hat{v}_{out}(t)\right) \quad (3.14)$$

$$I_C + \hat{\imath}_C(t) = I_L + \hat{\imath}_L(t) - \frac{V_{out} + \hat{v}_{out}(t)}{R_{SPK}} \quad (3.15)$$

$$I_{vbat} + \hat{\imath}_{vbat}(t) = \left(D + \hat{d}(t)\right).\left(I_L + \hat{\imath}_L(t)\right) \quad (3.16)$$

$$I_{vneg} + \hat{\imath}_{vneg}(t) = \left(D - \hat{d}(t)\right).\left(I_L + \hat{\imath}_L(t)\right) \quad (3.17)$$

To simplify (3.14)-(3.17), it is important to note that at steady state

$$i_L(t + T_S) = i_L(t) \quad (3.18)$$

$$V_C(t + T_S) = V_C(t) \quad (3.19)$$

This means that the average of $v_L(t)$ taken over entire cycle $\left(i.e.:\ \langle v_L(t)\rangle_{T_S}\right)$ must have a zero average, i.e.:

$$V_L = 0 = D.V_{bat} + D'.V_{neg} - V_{out} \tag{3.20}$$

Similar argument applies yields that:

$$I_C = 0 = I_L - \frac{V_{out}}{R_{SPK}} \tag{3.21}$$

Substituting (3.20) and (3.21) into (3.14) -(3.17) and neglecting the second-order terms yields:

$$\hat{v}_L(t) = D.\hat{v}_{bat}(t) + D'.\hat{v}_{neg}(t) + \hat{d}(t).\left(V_{bat} - V_{neg}\right) - \hat{v}_{out}(t) \tag{3.22}$$

$$\hat{\imath}_C(t) = \hat{\imath}_L(t) - \frac{\hat{v}_{out}(t)}{R_{SPK}} \tag{3.23}$$

$$\hat{\imath}_{vbat}(t) = D.\hat{\imath}_L(t) + I_L.\hat{d}(t) \tag{3.24}$$

$$\hat{\imath}_{vneg}(t) = D'.\hat{\imath}_L(t) - I_L.\hat{d}(t) \tag{3.25}$$

The last set of equations can be used to derive the ac model for the switcher circuit as shown in Figure 3.11:

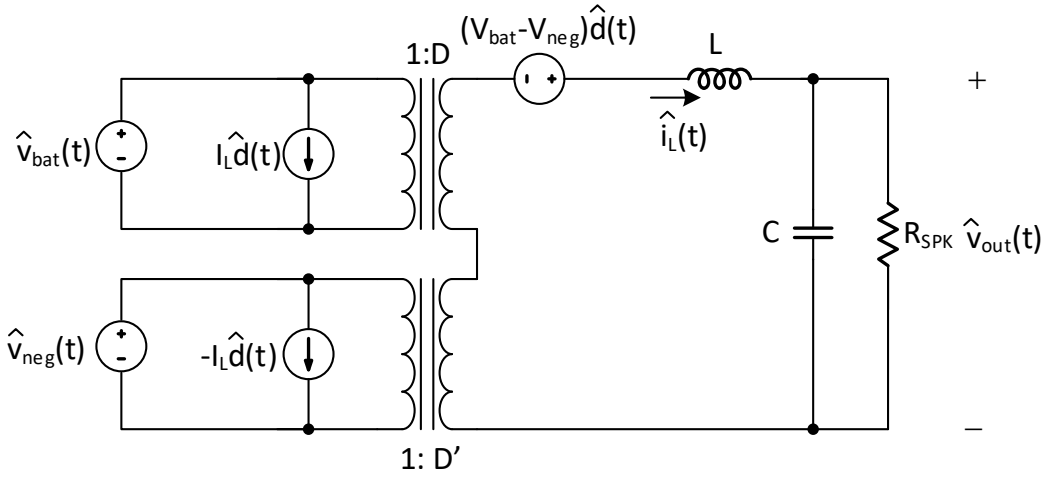
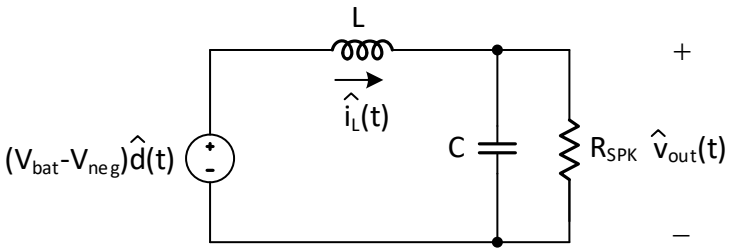


Figure 3.11 AC model for the output stage

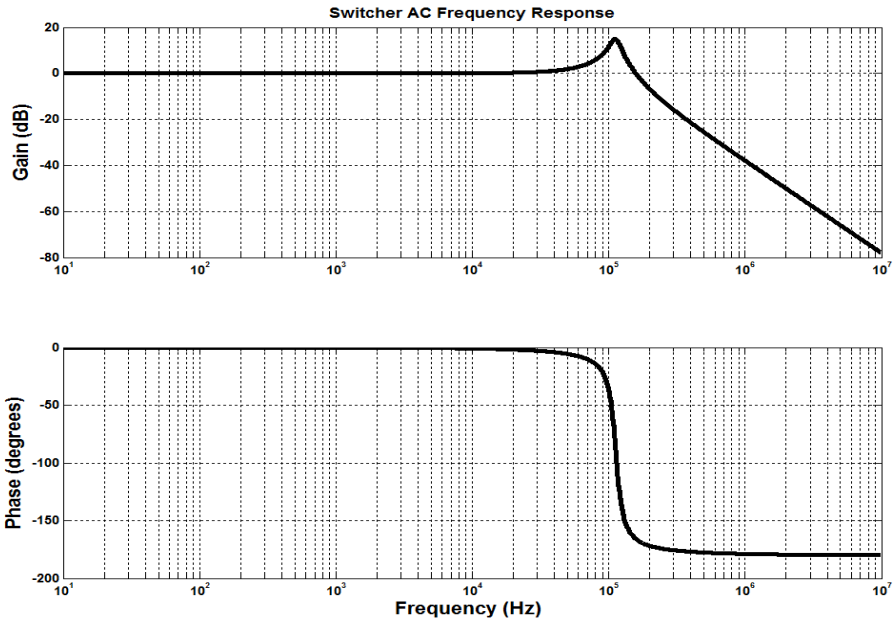
In the next section, the model derived in Figure 3.11 will be used to study the open loop stability of the control loop.

3.3.2 Open-loop AC model for the control loop

To analyze the control loop stability, the switcher AC model shown in Figure 3.10 can be simplified by setting the supply perturbations $\hat{v}_{neg}(t)$, and $\hat{v}_{bat}(t)$ to zero.



(a)



(b)

Figure 3.12 (a) Simplified switcher AC model, (b) Its frequency response

The resulting simplified model predicts the change in the output $\hat{v}_{out}(t)$ as a function of the change in the control $\hat{d}(t)$. Figure 3.12(a) shows the simplified ac model, which consists of the LC filter loaded by the speaker resistance (R_{SPK}); whereas Figure 3.12(b) shows the magnitude and phase Bode plots.

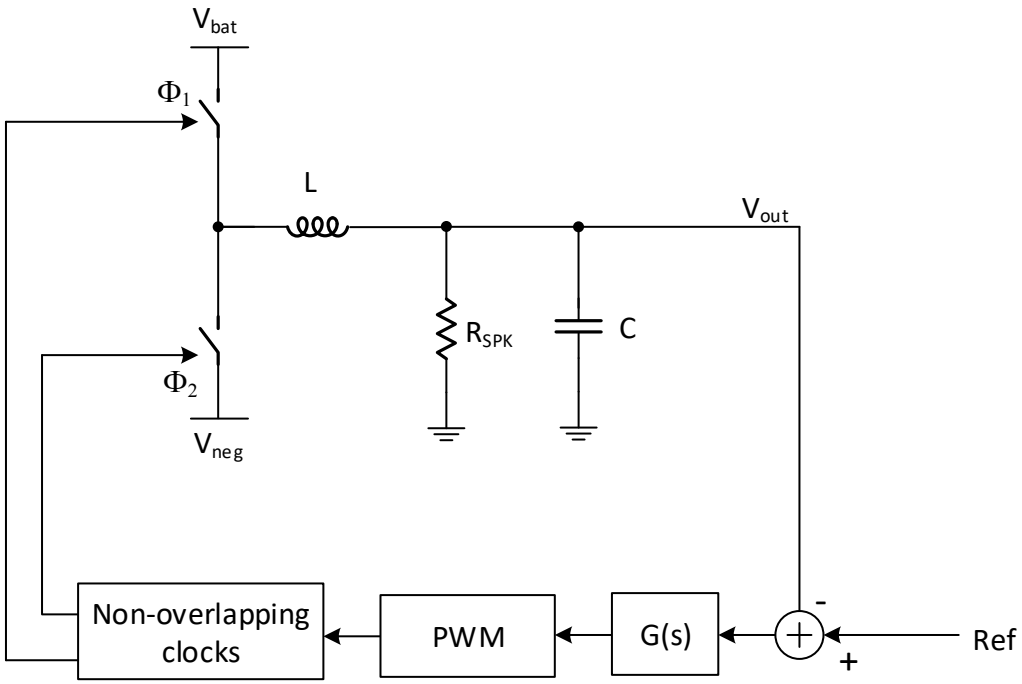


Figure 3.13 Block Diagram for the PWM loop

For a first-order analysis, assuming the voltage ripple is less than 50mV, and switching frequency is 1MHz; then the resonance frequency of the LC tank is approximately 100kHz. Figure 3.13 shows a block diagram of the basic feedback voltage control loop for a PWM/CCM loop. For the control loop to have bandwidth higher than 100kHz, the complex conjugate LC poles would need to be cancelled by on-chip zeros. Unfortunately, it is very hard to realize on-chip zeros that track the

poles realized by external components. The non-correlated tolerance of the on-chip and off-chip components would lead to a large part to part variation in loop dynamics.

Another alternative is to decrease the loop bandwidth such that the open loop unity-gain frequency is lower than the LC resonant frequency, and therefore the LC conjugate poles would have minimal impact on the loop dynamics. If the minimum desired open-loop gain in the audio band is set to 40dB (for a reasonable SNDR), then this solution necessitates at least a third-order loop as shown in Figure 3.14. A higher loop order is a costly solution because of the added complexity as well as the increase in the current consumption.

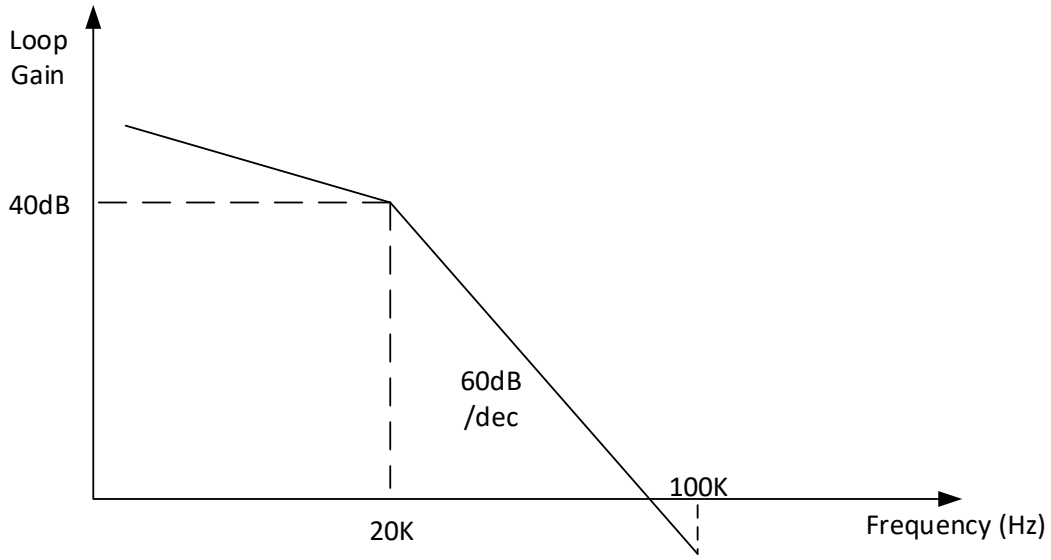


Figure 3.14 Hypothetical open loop gain to push LC poles outside audio band

3.3.3 Current-mode control

To reduce the loop order and maintain stability for the voltage control loop, current mode control is employed [25]. As illustrated in Figure 3.15 (a), the voltage control loop is excited by the dependent voltage source $\left(V_{bat} - V_{neg}\right)\hat{d}(t)$. If the

excitation source changes to a dependent current source of the form $G_m\big(V_{bat} - V_{neg}\big)\hat{d}(t)$ as shown in Figure 3.15 (b), then the effect of the inductor on the loop gain is nullified and the LC conjugate complex poles are replaced by a left-half plane real pole whose value is $1/(2\pi RC)$.

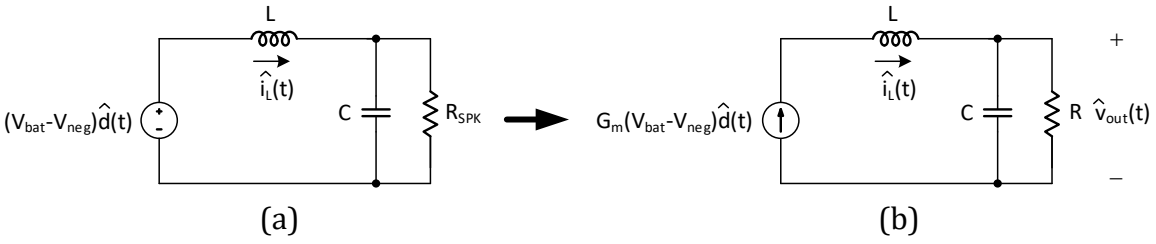


Figure 3.15 (a) Voltage mode excitation, (b) Current mode excitation

There are different ways to implement the current-mode control [25], and they all share the basic concept, which is to sense the inductor current, convert it to voltage, and compare it to the loop filter output and then use the comparator output to generate the PWM control for the output switches.

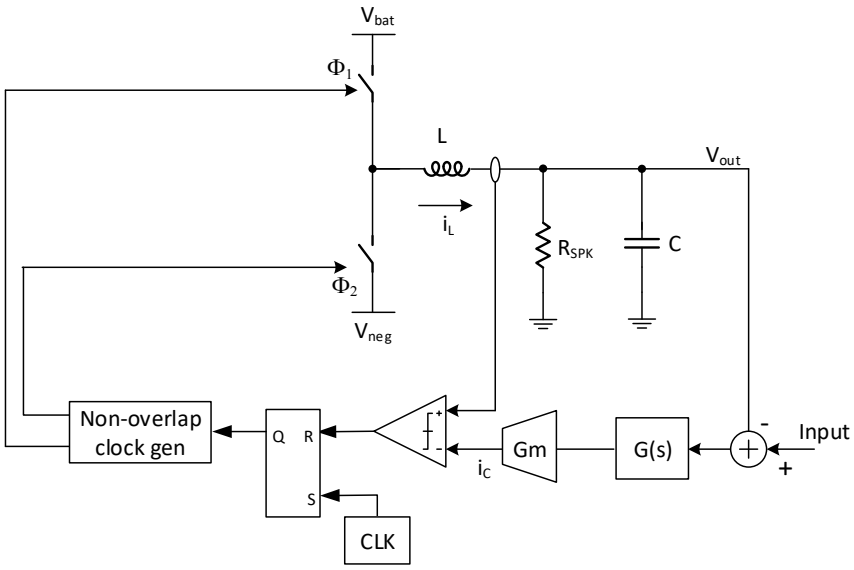


Figure 3.16 Peak-current control for current mode CCM loop

Figure 3.16 shows an example for current-mode control, where the inductor current is sensed and compared to the loop filter output G(s). The comparator output is then used to drive the "reset" port of an SR flip-flop, with the "set" port driven by a clock at frequency F_S; therefore, fixing the switching rate to F_S.

The SR flip-flop resets and the high-side switches turns off, while the low-side switch turns on every time the inductor current (i_L) increases above the control current (i_C), which results in the inductor current ramping down. Once the CLK triggers SR flip-flop to "set", the output stage switches state, and therefore the inductor current starts increasing again.

The inductor current carries a low-frequency content equal to i_C , with a variable ripple that ranges from 0 to i_C. If we ignore the high-frequency ripple, the inner current-mode loop maintains i_C very close to i_L, which changes the excitation source for the output RLC to be a current source instead of a voltage source.

The main drawback of the peak current-mode control is the inherent instability of the system for duty cycles higher than 0.5 and therefore a compensation sawtooth signal is usually used to guarantee stability [25]. For this work, however, a peak-valley current mode scheme, also known as sliding mode control [25], illustrated in Figure 3.17, is used.

In this scheme, the inductor current is compared to the loop filter output using a hysteretic comparator with a hysteresis window of 2ΔI, where ΔI is a constant design parameter. This means that while the outer voltage control loop forces the

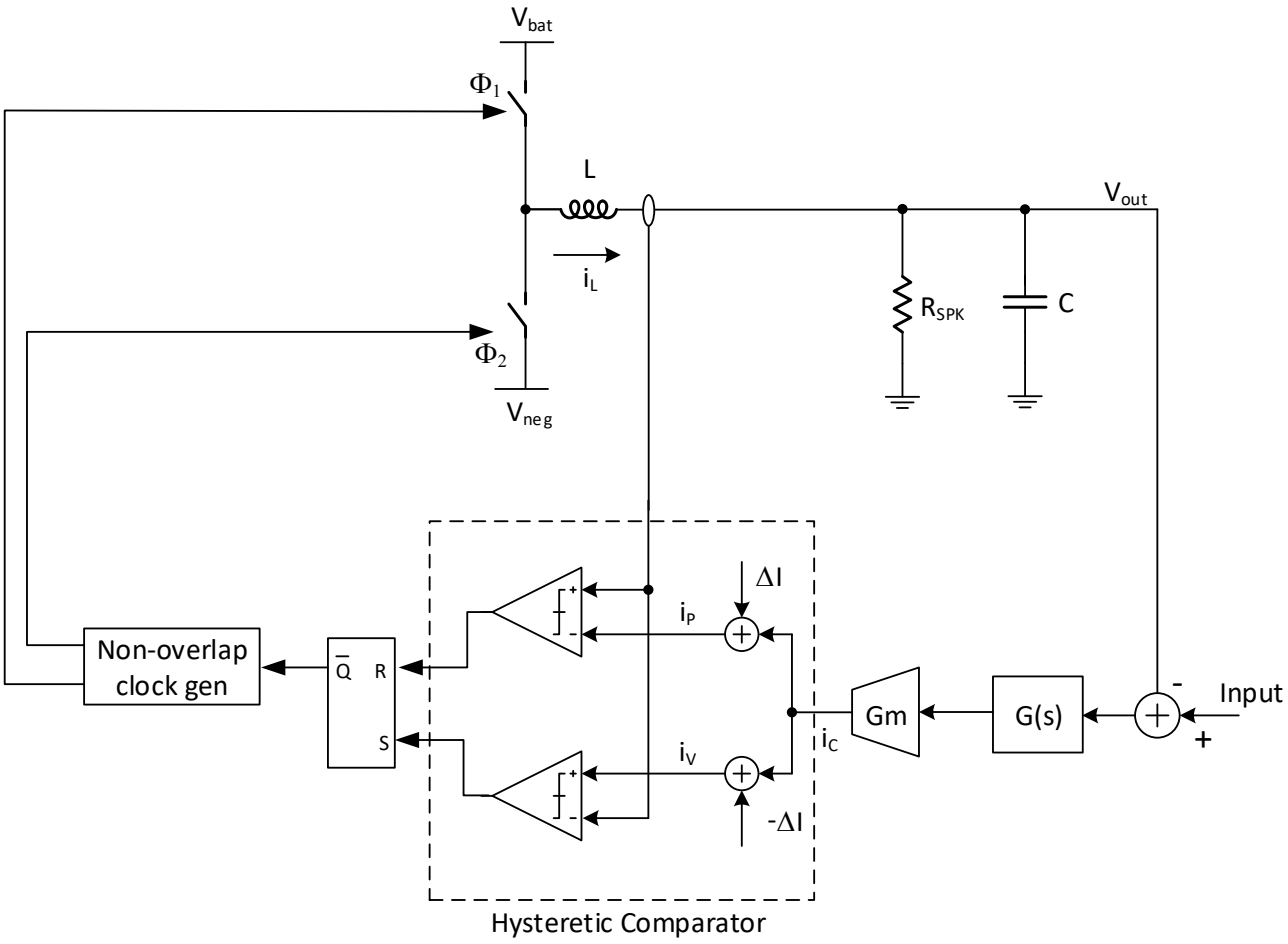


Figure 3.17 Peak-Valley current mode control scheme

average output voltage to be equal to the input, the inner current loop mode forces the average inductor current to be equal to i_C and the inductor ripple to be bounded by ±ΔI.

If the inductor current increases above i_C + ΔI then the hysteretic comparator triggers and resets the SR flip-flop output, thereby turning off the high-side switch and turning on the low-side switch, which causes the current to start ramping down. Similarly, if the inductor current decreases below i_C - ΔI then the hysteretic comparator sets the SR flip-flop output, thereby turning on the high-side switch and turning off the low-side switch, resulting in ramping down for the inductor current.

Figure 3.18 depicts the interaction of both voltage and current feedback loops. The voltage control loop forces the error signal (G(s) output) profile to follow the input signal.

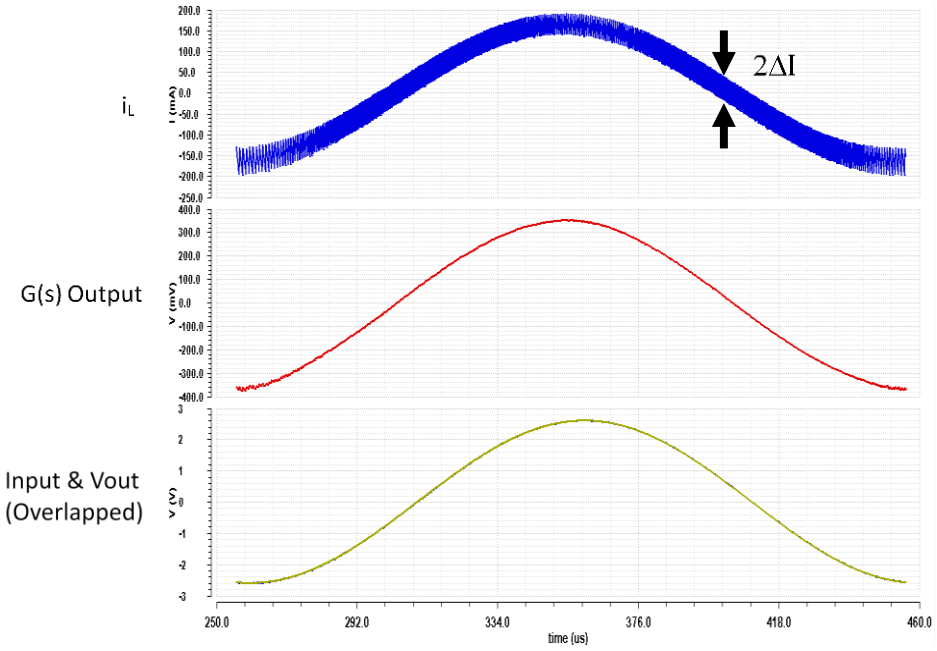


Figure 3.18 Inductor current, G(s) output, and output waveforms for CCM loop

The current feedback loop forces the low-frequency content of the inductor current (i_L) to follow G(s) output while bounding the high-frequency ripples to 2ΔI.

3.3.4 Loop Analysis

To study the loop stability, the switching frequency is assumed to be much higher than the small-signal unity-gain bandwidth. Under this assumption, the internal current-mode loop can be assumed to have a closed-loop gain of unity. Thus, the output current of the transconductance (G_m) flows directly into the inductor as depicted in Figure 3.19.

The open-loop gain is given by:

$$G(s).\ \frac{G_m.R_{SPK}}{1+s\,R_{SPK}C} \tag{3.26}$$

This equation shows that to the first order, the inductance plays no role in setting the loop dynamics, and that the output stage pole is given by $1/2\pi R_{SPK}C$. For a reasonable value for capacitance C, this pole falls within the loop bandwidth. The equation also

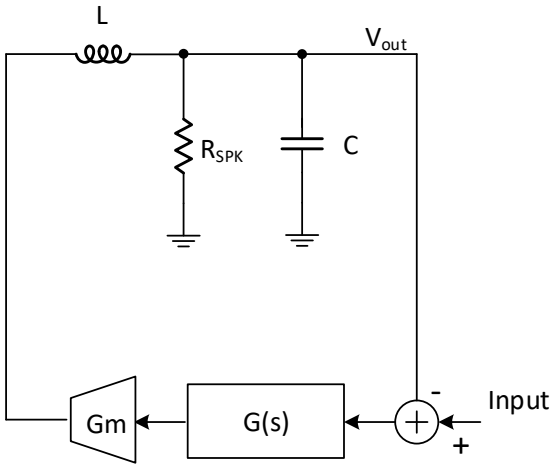


Figure 3.19 AC model for the loop

shows that R_{SPK} affects the open-loop gain, but not the closed-loop bandwidth, which means that the loop dynamics are expected to be independent of the headphone impedance (e.g. 16, 32, or 600Ω).

The loop filter G(s) is designed to have high enough gain in the audio band to suppress the nonlinearities from the subsequent stages while maintaining acceptable loop stability. An active RC lossy integrator is designed to realize the loop filter G(s) as

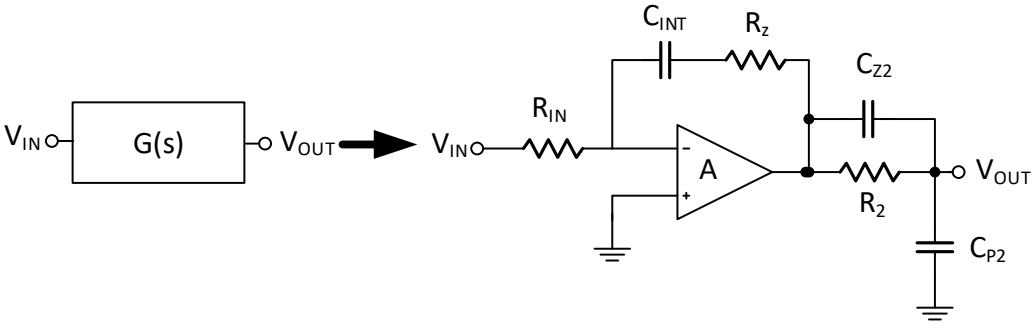


Figure 3.20 Realization of the loop filter G(s)

shown in Figure 3.20. The loop filter has 2 poles and 2 zeros, with one of the poles at DC to increase the loop gain in the audio band.

Assuming infinite gain (A) for the amplifier, then G(s) is given by:

$$G(s) = \frac{V_{OUT}}{V_{IN}} = \frac{1 + sC_{INT}R_Z}{sC_{INT}R_{IN}} \frac{1 + sC_{Z2}R_2}{1 + s(C_{Z2} + C_{P2})R_2} \tag{3.27}$$

The RC network that follows the integrator, which consists of R_2, C_{Z2}, and C_{P2}, creates a pole and a zero at frequencies higher than 20kHz but still lower than the unity-gain bandwidth. This network helps reduce the loop bandwidth in order to guarantee that the switching frequency is sufficiently higher than the unity-gain bandwidth, thereby validating the model shown in Figure 3.19.

Substituting G(s) in the loop gain equation yields:

$$Loop\ Gain = \frac{1 + sC_{INT}R_Z}{sC_{INT}R_{IN}} \frac{1 + sC_{Z2}R_2}{1 + s(C_{Z2} + C_{P2})R_2} \frac{G_m . R_{SPK}}{1 + s\,R_{SPK}C} \tag{3.28}$$

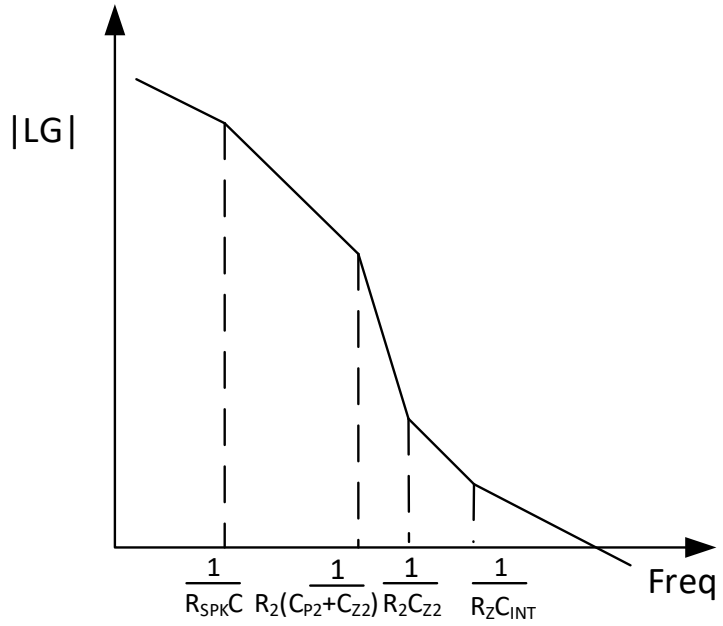


Figure 3.21 Open-loop gain versus frequency showing locations of all poles/zeros

Figure 3.21 shows the magnitude of the Loop Gain (LG) as a function of frequency with all the poles and zeros of (3.30) shown on the x-axis. Table 3.1 shows the component values used in the design:

Table 3.1 System key parameters and component values

R_{IN}	C_{INT}	R_Z	C_{Z2}	R_2	C_{P2}	G_m	C
20 kΩ	24 pF	10 kΩ	3 pF	800 kΩ	4 pF	1 S	0.4 µF

A rough estimation for the unity-gain frequency is given by:

$$f_{unity} = \frac{1}{2\pi}\frac{R_Z}{R_{IN}}\frac{C_{Z2}}{(C_{Z2}+C_{P2})}\frac{G_m}{C} = \frac{1}{2\pi}\frac{1}{2}\frac{3}{7}\frac{1}{0.4.10^{-6}} \approx 400kHz \qquad (3.29)$$

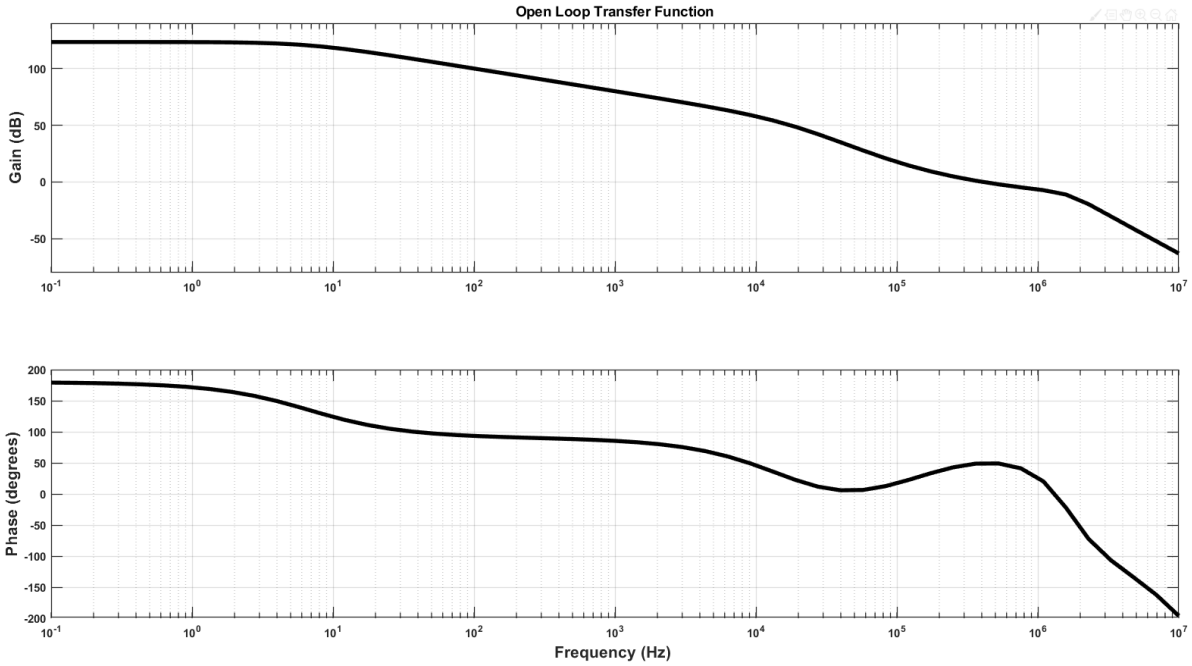


Figure 3.22 Open loop Bode plots

Figure 3.22 shows the open-loop gain and phase versus frequency. The plot shows that the unity-gain frequency matches the calculation, and that the minimum gain in the audio band equals 50dB at 20kHz. Phase margin and gain margin can be extracted from the plot to be roughly 50 degrees, and 10dB.

3.3.5 Loop Switching Frequency

A distinctive feature of the peak-valley current-mode control scheme is its variable switching frequency. Since, in this scheme, the current ripples are set to a predefined value, then the only degree of freedom for the loop to be able to pump enough charge to track a variable input is to change the switching frequency. This means that for a sinusoidal input, higher switching frequency is expected whenever the input is near zero, and lower switching frequency is expected at the peaks.

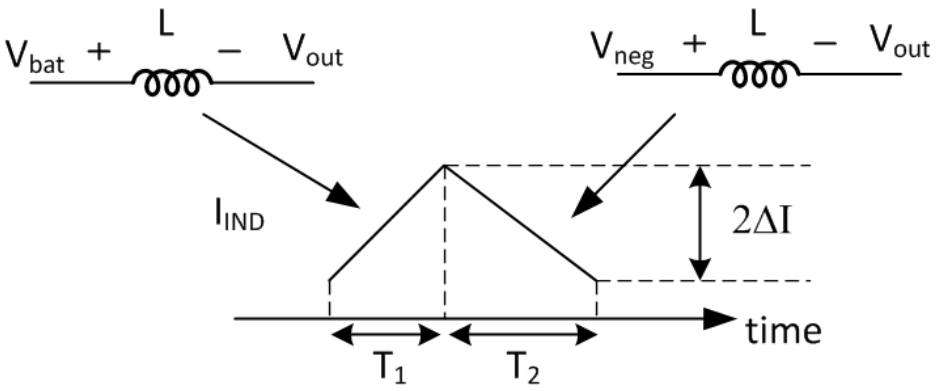


Figure 3.23 Voltage across the inductor during the 2 phases

If the supplies V_{bat} and V_{neg} are assumed to be constants during the switching cycle, then the inductor current ripple during the two phases can be assumed to follow a linear relationship as shown in Figure 3.23. Therefore, T_1 and T_2 can be expressed as:

$$T_1 = \frac{L.2\Delta I}{V_{bat} - V_{out}} \tag{3.30}$$

$$T_2 = \frac{L.2\Delta I}{V_{out} - V_{neg}} \tag{3.31}$$

Combining T_1 and T_2, the switching frequency (F_{SW})can be expressed by:

$$F_{SW} = \frac{1}{T_1 + T_2} = \frac{V_{bat} - V_{neg}}{L.2\Delta I} D(1 - D) \tag{3.32}$$

where D is the duty cycle. The equation shows that the switching frequency changes as a function of the square of the duty cycle, which in turn is a direct function of the output if the supplies are constant, as shown in Figure 3.24.

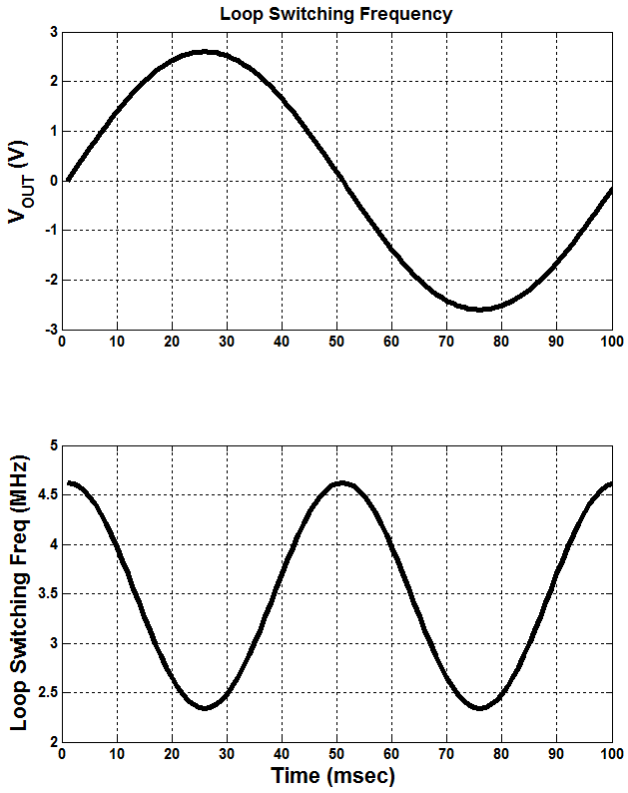


Figure 3.24 Loop switching frequency and output voltage vs. time

Having a higher switching frequency at zero crossings helps the loop better track the signal by pumping charges faster, although this comes at the expense of more dynamic power dissipation for a given THD performance.

In a voltage mode PWM Class-D, a fixed switching frequency is employed and is usually chosen to be high enough to guarantee that the loop can track the signal at zero crossings with a certain fidelity. However, since the switching rate is constant, the loop continues to dissipate the same amount of dynamic power even after the signal leaves the high slew rate region, which leads to more dynamic power dissipation. Therefore, the peak-valley control scheme is the right choice when higher efficiency is sought.

In addition, the output voltage ripples (ΔV_{ripple}) for a buck converter is given by [25]:

$$\Delta V_{ripple} = \frac{\Delta I}{8 C F_{SW}} \tag{3.33}$$

where ΔI is the current ripple, C is the output capacitance, and F_{SW} is the switching frequency. Equation (3.33) suggests that increasing F_{SW} can decrease the ripples, which results in better THD+N due to the reduced fold back into the audio band. However, this comes at the expense of higher dynamic power consumption, which results in higher quiescent current. The design approach is to keep increasing the switching frequency until either THD+N is no longer limited by the foldback or the maximum target quiescent current is exceeded.

CHAPTER 4 Proposed system detailed block design

4.1 Detailed system description

Figure 4.1 shows a more detailed block diagram of the proposed system described in chapter 3, which consists of:

a. G(s): Loop filter, which was described in section 3.3.4

b. G_m: Transconductance amplifier

c. R_P: Transimpedance converter.

d. Peak-Valley hysteretic comparator

e. Non-overlapping clock generator

f. Switching output stage

g. Negative charge pump to generate V_{neg}

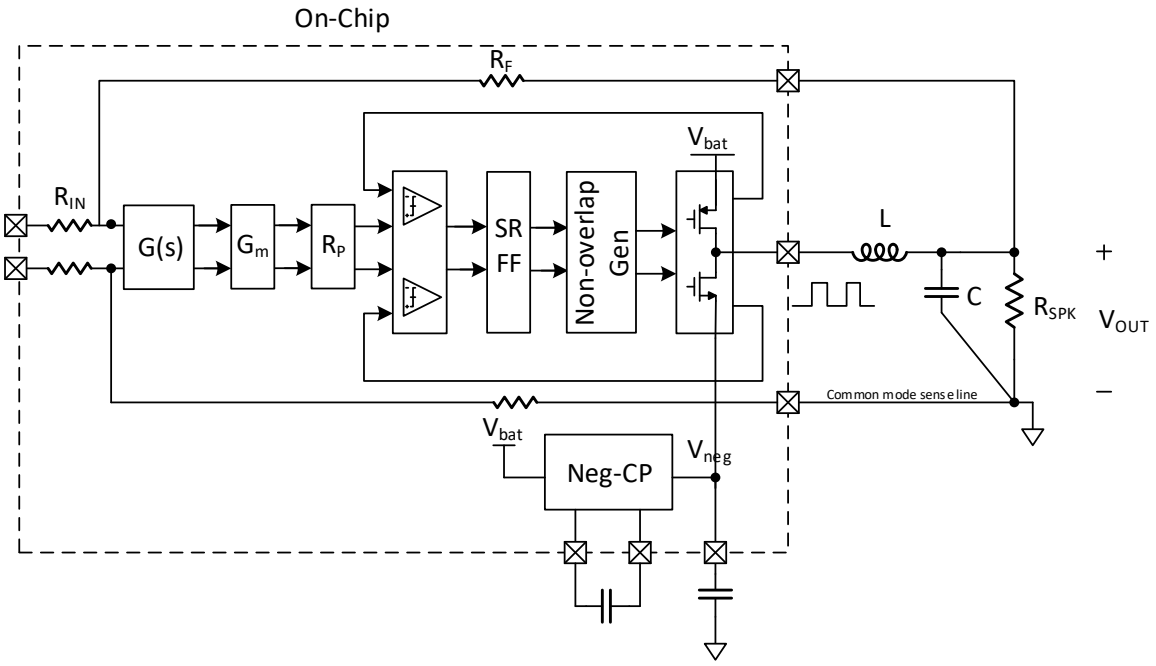


Figure 4.1 Simplified proposed architecture

As described in Chapter 3, there are two concurrent active loops: (1) a voltage-controlled PWM-based loop that senses the output across R_{SPK} and feeds back to the loop filter G(s) through the feedback resistor R_F; (2) a peak-valley current-controlled loop that senses a voltage proportional to the inductor current I_{IND}, and feeds back to the hysteretic comparator, which compares it to a scaled-version of the loop filter output. The output of the hysteretic comparator controls the set/reset states of the SR FF, which in turn controls a non-overlapping clock generator that controls the output stage switching state.

The output stage is powered by a battery voltage that ranges from 2.9-4.5V, and the output of an unregulated negative charge-pump that ranges from -2.9 to -4.5V when unloaded.

Since the negative side of the headphone load is connected to the local PCB ground, any local PCB ground bouncing, would deteriorate the performance and would be audible. The conventional solution is to sense the local PCB ground and route it back to the chip through the “common mode sense” (CMS) pin as shown in figure 4.1. The gain from the CMS pin to the loop filter output is unity, and therefore any disturbance or noise sensed on CMS is replicated at the headphone jack; hence, the differential output across the headphone load is free from CMS noise/disturbance.

In the next few sections, each of the blocks is described in more detail, along with more quantitative analysis.

4.1.1 Output stage

4.1.1.1 Topology

There are two available options to implement the switching output stage:

1. Watkins-Johnson shown in Figure 4.2 [25]

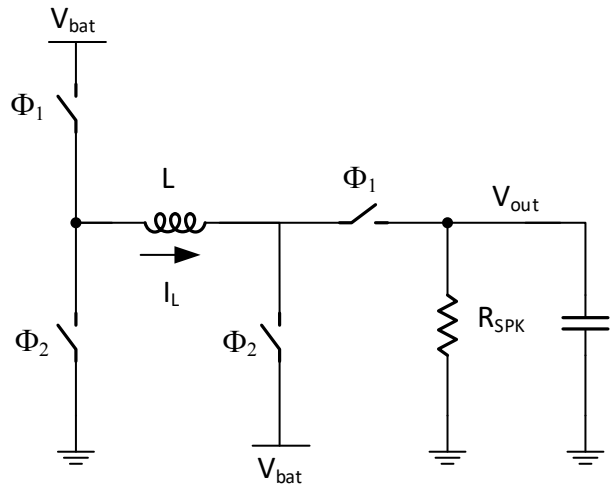


Figure 4.2 Watkins-Johnson output stage

This type of switching stage has the advantage of being able to drive a ground-referenced load, and therefore can generate positive and negative output swing from a single positive supply without the need for a negative charge pump. This translates into both an area saving and efficiency improvement; however, it comes at the cost of the system linearity as shown below.

During ϕ_1, the inductor is connected between V_{bat} and V_{out}, and therefore, the current ramps up as shown in Figure 4.3. During ϕ_2, the inductor is connected between 0 and V_{bat}, which forces the inductor current to ramp down. To produce a

positive output, the duty cycle will be larger than 0.5, which means that more time is spent during ϕ_1 so that the net current flowing to the load is positive. On the other hand, if the output voltage is negative, then the duty cycle is less than 0.5, which

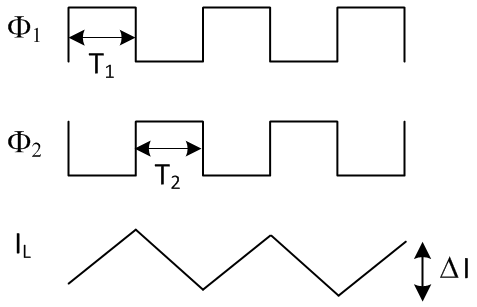


Figure 4.3 Inductor waveform during the two phases

enables the inductor to build enough negative current during ϕ_2 that is passed to the output during ϕ_1, effectively making the net current flowing to the load negative.

To calculate the switching stage gain, ΔI can be expressed as:

$$\Delta I = \frac{T_1(V_{bat} - V_{out})}{L} = \frac{T_2(V_{bat} - 0)}{L} \tag{4.1}$$

Re-writing the equation in terms of the duty cycle (D) yields:

$$\frac{V_{out}}{V_{bat}} = \frac{2D - 1}{D} \tag{4.2}$$

This equation represents a nonlinear relationship between V_{out} and duty cycle (D) as shown in Figure 4.4. This nonlinearity represents a limitation on the achievable THD performance of the overall driver. Another disadvantage to this topology is the number of clocked series switches with the inductor in each clock phase, which increases the ohmic losses and reduces the power efficiency. In order to reduce the

ohmic losses, the size of each switch needs to grow, thereby increasing the dynamic losses.

A third disadvantage is the transfer function compression for the negative swing. For example, the output voltage (V_{out}) negative swing can double from -0.5 to -1V for a change in the duty cycle from 0.4 to 0.33. This fast change in the output for an incremental change in the duty cycle necessitates more precision in generating the PWM pulse to produce the correct output voltage.

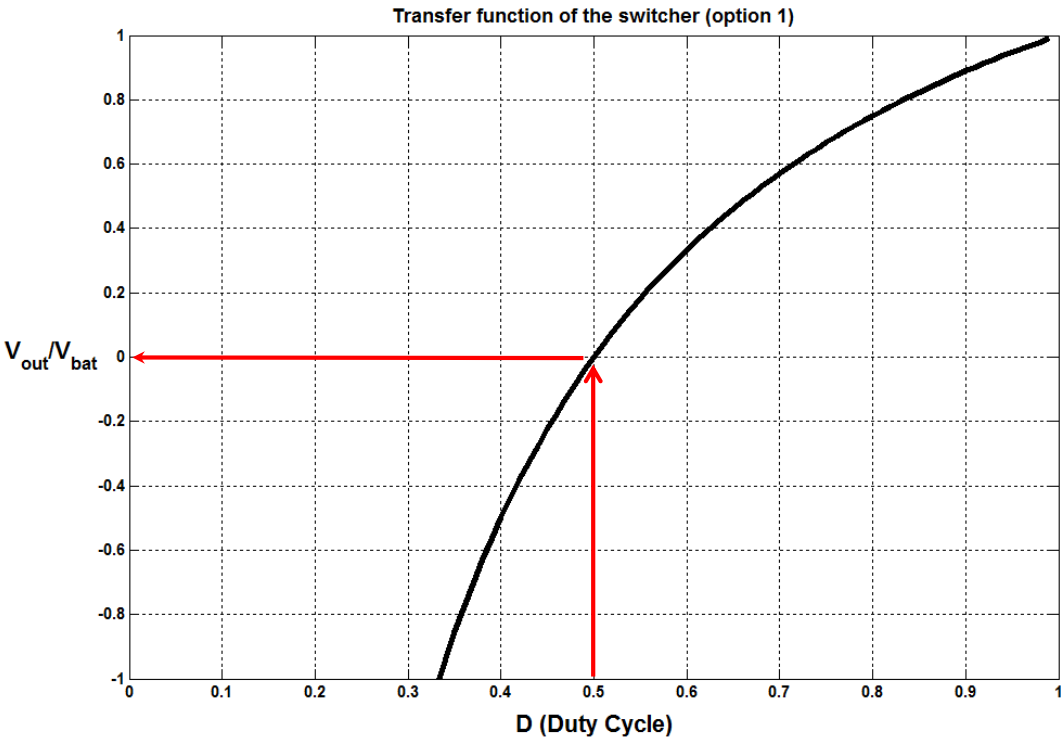


Figure 4.4 Transfer function vs. duty cycle for Watkins-Johnson

2. Half bridge Class-D with dual supplies [known as buck switcher]

This type of switching stage has the advantage of a simple design, and one switch/phase, which reduces the ohmic losses. It also provides a linear characteristic

as will be mathematically proven below. However, its main limitation is the lack of negative swing support, which is needed to drive headphone loads. To overcome this limitation, this stage is powered between a positive and a negative supply to support both positive and negative swing as shown in Figure 4.5.

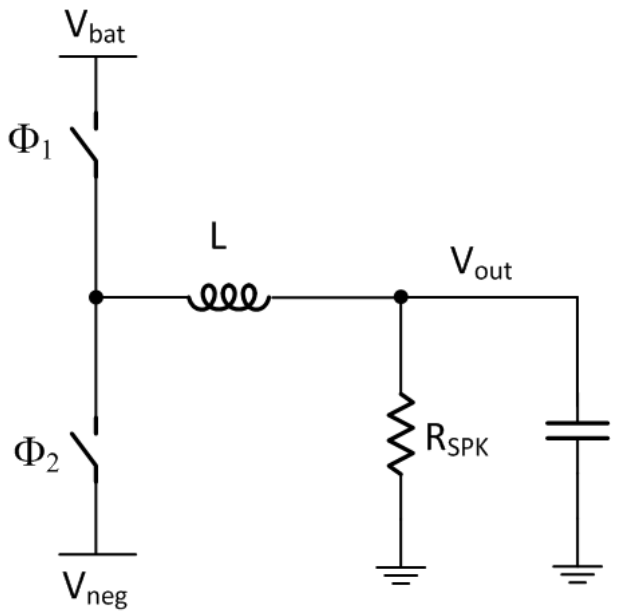


Figure 4.5 Half bridge Class-D switching stage

During ϕ_1, the inductor is connected between V_{bat} and V_{out}, and therefore, the current ramps up linearly as shown in Figure 4.6. During ϕ_2, the inductor is connected between V_{neg} and V_{out}, which forces the inductor current to ramp down. The gain of this topology can be calculated in a similar fashion:

$$\Delta I = \frac{T_1(V_{bat} - V_{out})}{L} = \frac{T_2(V_{out} - V_{neg})}{L} \tag{4.3}$$

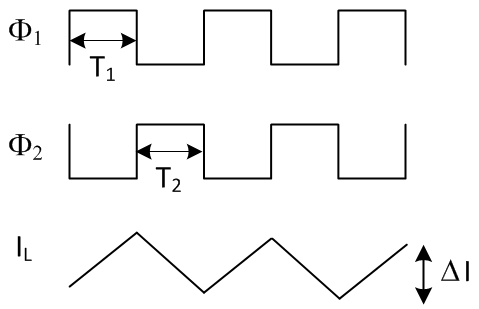


Figure 4.6 Inductor waveform during the two phases

Re-writing the equation in terms of the duty cycle (D) yields:

$$V_{out} = DV_{bat} + (1 - D)V_{neg} \tag{4.4}$$

V_{neg} is generated on-chip using an unregulated Negative Charge Pump (NCP) as will be explained later in this chapter. The output of an unregulated NCP depends on the load current and can reach a value of $-V_{bat}$ when the NCP is not loaded. With the assumption of light loading, equation (4.4) can be rewritten as a function of V_{bat}:

$$\frac{V_{out}}{V_{bat}} = 2D - 1 \tag{4.5}$$

Equation (4.5) is plotted in Figure 4.7 and shows a perfectly linear characteristic, which can help improve the THD of the overall solution.

In this work the second option is chosen to minimize the ohmic losses and to enhance the overall system linearity, while the added cost and efficiency loss of adding NCP is minimized by design.

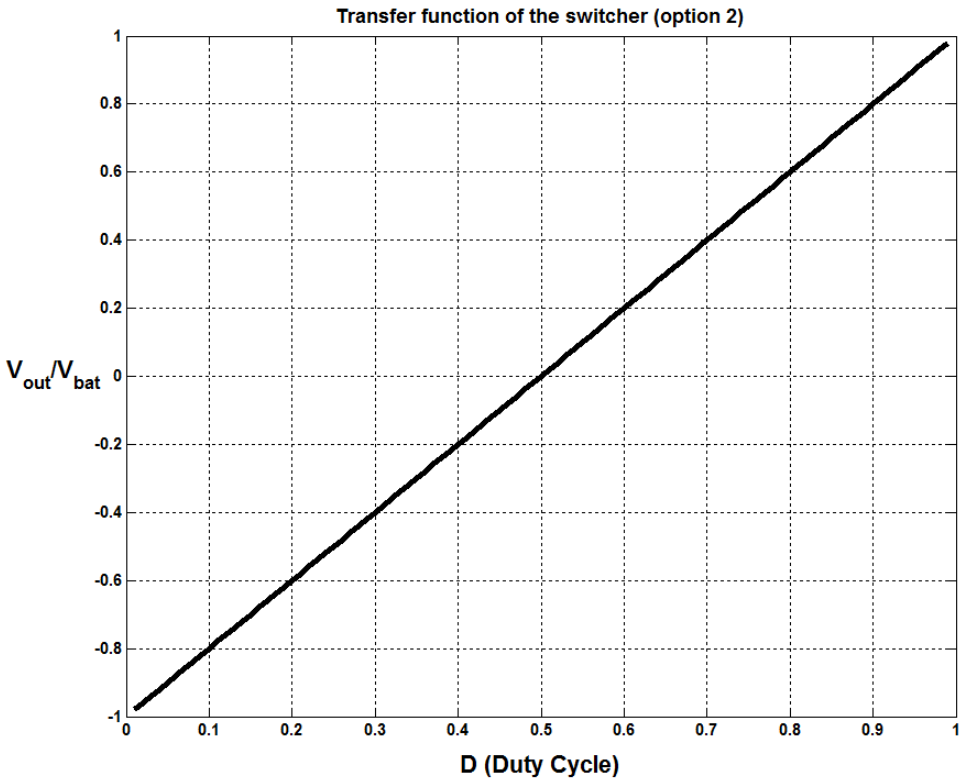


Figure 4.7 Transfer function vs. duty cycle for half bridge Class-D with dual supplies

4.1.1.2 Implementation

Figure 4.8 shows the actual implementation used for the output stage. The prototype chip is using a 0.18μm process that provides both 1.8V and 5V devices. The 5V devices can sustain a maximum of 5.5V across gate-to-source or gate-to-drain junctions or across drain to source. This means that a cascode device (M_{NCAS}/M_{PCAS}) is needed for each of the low- and high-side switches to protect the main switching devices. The cascode devices do not need to switch and hence the gate is connected to ground.

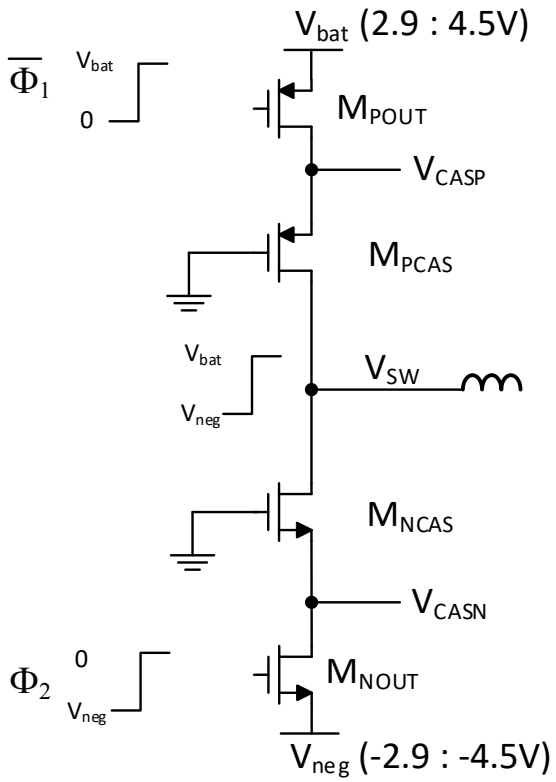


Figure 4.8 Actual implementation for the output stage

The cascode device prevents the drain-to-source and gate-to-drain voltages for the main switch (M_{POUT}/M_{NOUT}) from reaching 5.5V, which is the reliability limit. For example, if V_{bat} equals 4.5V (implying V_{neg} equals -4.5V), and ϕ_1 is high, then V_{SW} is pulled up to V_{bat}. With M_{NCAS} used as a cascode device, the gate-to-drain voltage of M_{NOUT} is -3.5V, and its drain-to-source voltage is 3.5V assuming V_T = 1V, and at the same time, VGD/VDS for the cascode device M_{NCAS} are -4.5/5.5V.

Similarly, if the low-side switch is on, and the high-side switch is off, then M_{PCAS} protects VGD and VDS for M_{POUT} while staying in the safe operating region itself.

The “on” resistance for the combined high-side switch (MPOUT in series with MPCAS) is designed to be equal to 2Ω, while the “on” resistance for the low-side switch is 1Ω. All device dimensions are shown in Table 4.1.

Table 4.1: Output stage device sizes

	M_{POUT}	M_{PCAS}	M_{NCAS}	M_{PCAS}
W/L	8000/0.5	8000/0.5	4800/0.6	4800/0.6
Ron @ 3.7V	1Ω	1Ω	0.5Ω	0.5Ω

4.1.2 Inductor Current Sensing Scheme

As explained in Section 3.3.3, current-mode control is essential in improving the THD by neutralizing the effect of the inductor on the loop response. This concept is based on comparing the inductor current with the loop filter output and using the difference to control the output stage switches.

There are multiple ways of measuring the inductor current [26,27], and they are all based on converting the inductor current into a proportional voltage, which is then used for the current-mode loop processing. In the following sections, two different schemes are discussed and compared.

4.1.2.1 Using RC sense network (Option I)

In this option, an integrated RC network is connected across the inductor terminals [26] as shown in Figure 4.9, where the voltage across the capacitor V_C is given by:

$$V_C(j\omega) = \frac{j\omega L}{1 + j\omega RC} I_{ind} \approx \frac{L}{RC} I_{ind} \quad for\ f > \frac{1}{RC} \tag{4.6}$$

Thus, for sufficiently high switching frequency the capacitor voltage (V_C) can be used to sense the inductor current (I_{ind}). The main drawback in this scheme, is that the proportionality constant depends on values for L, R and C. This RC time constant by itself can vary over process, and temperature by as much as ±40% if integrated on chip. Moreover, the external inductor may have an additional ±20% tolerance, which means L/RC can vary by as much as ±60%. This variation limits the accuracy of the current sensing and could translate into higher ripple currents, which degrades the overall efficiency and THD. Even if an on-chip RC calibration circuit is used, the inductance tolerance by itself would limit the use of this technique.

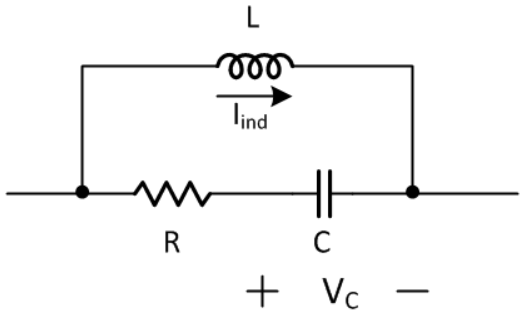


Figure 4.9 Sensing I_{ind} using RC sense network

4.1.2.2 Using the switching node (Option II)

In this option, the output switch "on" resistance is used to generate a voltage that scales with the inductor current, as illustrated in Figure 4.10 [27]. During ϕ_1, the inductor current flows through the high-side switch, and thus V_{bat}-V_{SW} changes linearly with the inductor current:

$$V_{bat} - V_{SW} = I_{ind} R_{on,p} \tag{4.7}$$

Similarly, during ϕ_2, the inductor current flows through the low-side switch, and thus $V_{SW} - V_{neg}$ changes linearly with the inductor current:

$$V_{SW} - V_{neg} = I_{ind} R_{on,n} \tag{4.8}$$

These relationships can be exploited to sense the inductor current in both phases. Figure 4.10 illustrates how the switching node (V_{SW}) changes with time when either ϕ_1 or ϕ_2 is active.

During ϕ_2, the inductor current (with the direction shown next to the plot) ramps down from its peak (I_P) to its valley (I_V), where I_P is assumed to be larger than I_V by $2\Delta I$, and the absolute value for both I_P and I_V depends on the instantaneous signal level. The inductor current in this phase flows through the low-side switch and thus V_{SW} changes from V_{neg}-$I_P.R_{on,n}$ to V_{neg}-$I_V.R_{on,n}$. Thus, the change in V_{SW} captures the inductor current scaled by the $R_{on,n}$. Similarly, during ϕ_1, the inductor current ramps from its valley (I_V) to its peak (I_P). The inductor current in this phase flows through the high-side switch and thus V_{SW} changes from V_{bat}-$I_V.R_{on,p}$ to V_{bat}-$I_P.R_{on,p}$. As a result the change in V_{SW} captures the inductor current scaled by the $R_{on,p}$.

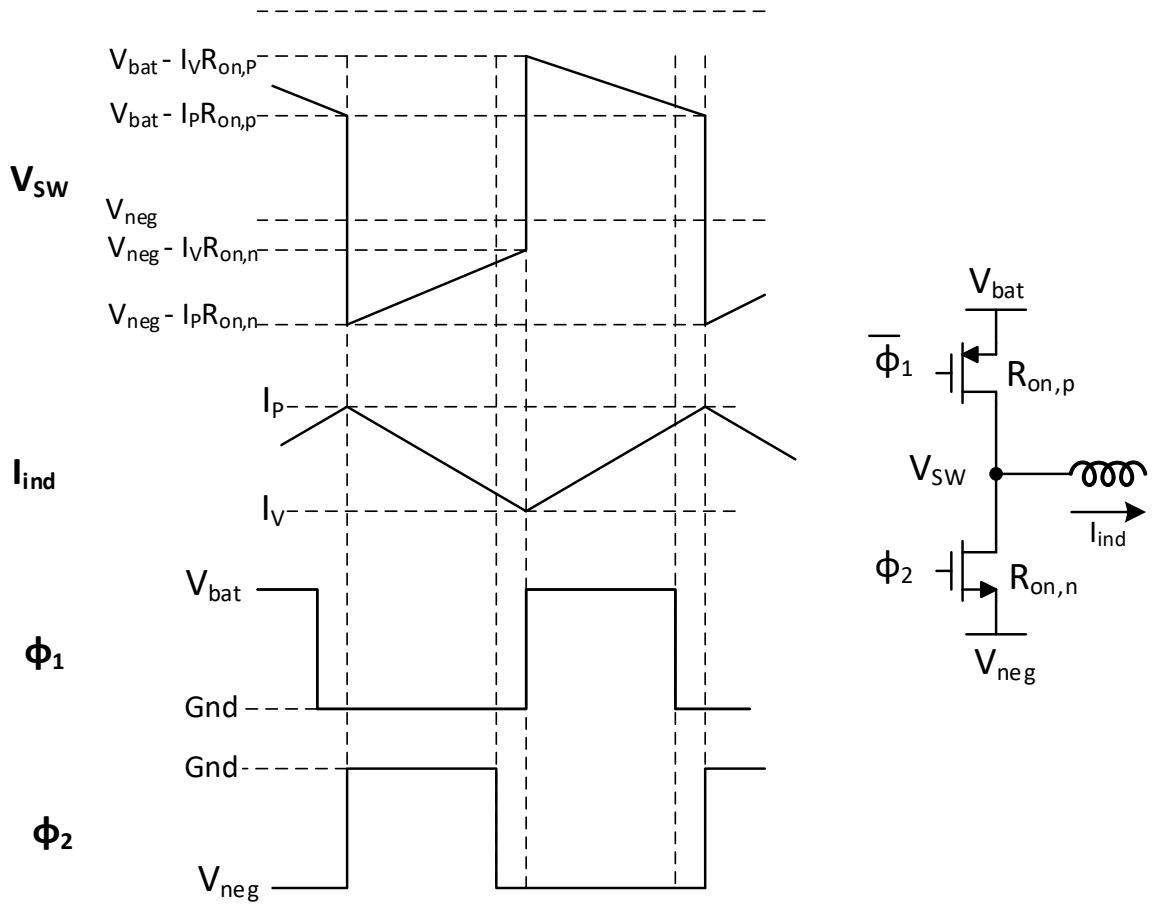


Figure 4.10 Timing waveforms to illustrate the current sensing technique

Since R_{on} for both the low side and high side varies over process, supply voltage and temperature, which affects the accuracy of the sensed current, the loop filter output needs to be scaled with R_{on} so that its effect is negligible when V_{SW} is compared to the loop filter output. This is illustrated in Figure 4.11, where the loop filter output (V_{LFp}-V_{FLn}) is converted into a differential current (I_{Gmp}-I_{Gmn}):

$$I_{Gmp} - I_{Gmn} = \frac{G_m}{K}\left(V_{LFp} - V_{LFn}\right) \tag{4.9}$$

This current is then scaled by K.$R_{on,p}$ to be compared against V_{SW} (= I_{ind}. $R_{on,p}$) by the peak comparator. Meanwhile the transconductance differential output current is scaled by K. $R_{on,n}$ when compared to V_{SW}(= I_{ind}. $R_{on,n}$) by the valley comparator, where

K represents the ratio between the on-resistance of the replica devices and the output stage on-resistance, and is typically a large ratio in order to: (1) reduce the area of replicas compared to the output stage, and (2)avoid consuming a large current in the transconductor. In addition, K scales the loop gain and its value has an impact on the loop stability. In this design the ratio K is set to 128,000. Similar scaling is applied to the constant ripple currents (ΔI), as shown in Figure 4.11 to keep the ripple currents constant.

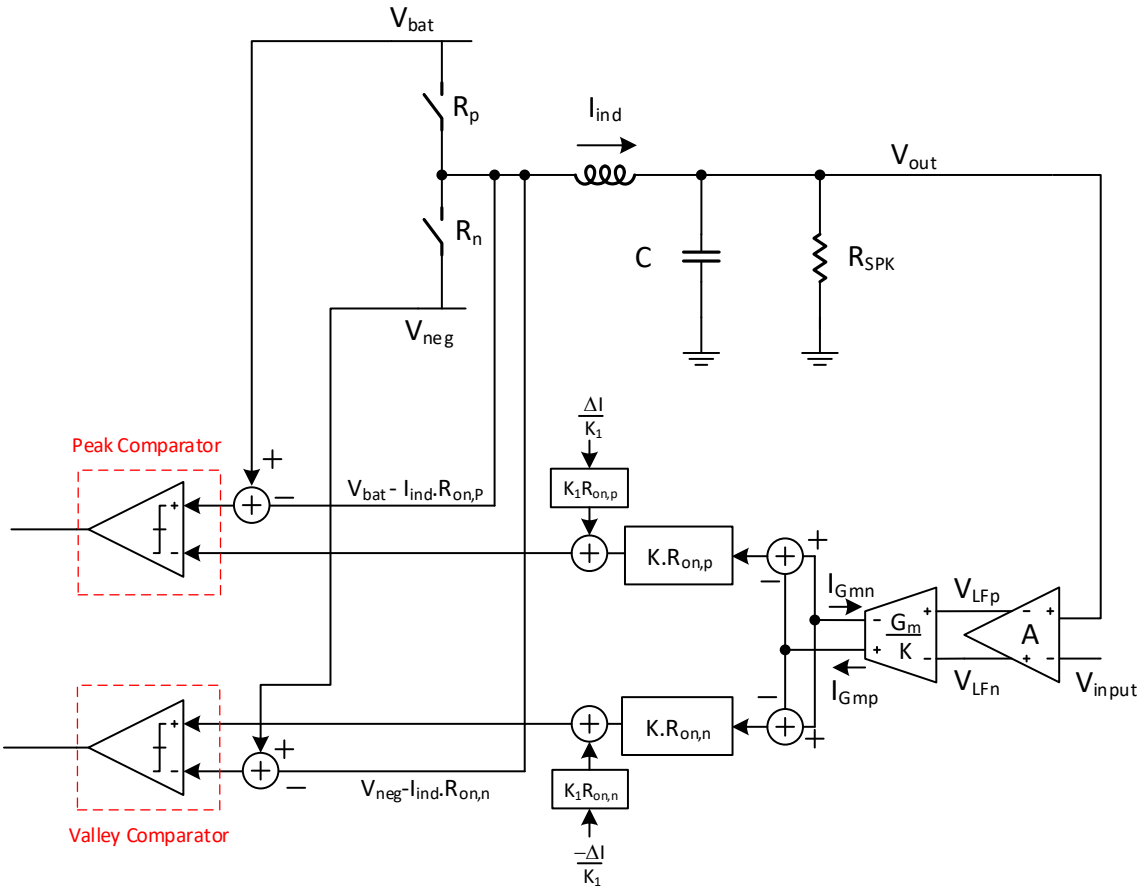


Figure 4.11 Scaling of loop filter output to cancel effect of switcher R_{on}

Equations (4.7) and (4.8) suggest that V_{SW} should be subtracted from V_{bat} and V_{neg} for peak and valley comparators respectively, which is necessary since the supply voltages are not constant due to their finite source impedance, and thus their instantaneous values depend on the inductor current. The supply subtraction is shown in Figure 4.11 as well. Inputs to the peak comparator ($V_{peak,p}$, $V_{peak,n}$) can be expressed as:

$$V_{peak,p} = R_{on,p}(I_{ind}) \tag{4.10}$$

$$V_{peak,n} = R_{on,p}\left(G_m\left(V_{LFp} - V_{LFn}\right) + \Delta I\right) \tag{4.11}$$

Equations (4.10), and (4.11) show that by comparing $V_{peak,p}$ and $V_{peak,n}$ the effect of V_{bat} is eliminated, and at the same time $R_{on,p}$ identically scales both inputs; thus, it does not affect the comparator decision. Similar expressions can be written for the valley comparator inputs as well to show that $R_{on,n}$ and V_{neg} do not affect the valley comparator decision.

Finally, it is worth mentioning that in the actual implementation the current is sensed using the cascode nodes (V_{CASN} and V_{CASP}) of Figure 4.8 and not V_{SW} as Figure 4.11 shows. This change does not affect any of the previous analysis and is needed to make sure that the high swing exercised by V_{SW} (V_{bat} -V_{neg}) does not affect the reliability of the switches used in summation/subtraction stage. On the other hand, similar to V_{SW}, V_{CASN} and V_{CASP} linearly change with the inductor current and can be used to sense the current without incurring the same large voltage swing. In fact, the swing for each of the cascode nodes is almost half of the V_{SW} swing as explained in Section 4.1.1.2.

The only caveat is that while V_{SW} could be used to sense the inductor current in both phases (Φ_1 and Φ_2), V_{CASP} can be only used during Φ_1, while V_{CASN} can be only used during Φ_2.

4.1.3 Summing/Subtracting Stage design

As explained in the previous section, a summer/subtractor is needed to linearly combine the scaled-transconductance output, and the scaled-ripple generator output on one side of the comparator and simultaneously combine the supply voltage with the switch node on the other side of the comparator.

Since some of these signals exercise relatively large swing, a switched-capacitor summer/subtractor is used to implement this function as shown in Figure 4.12 for the peak comparator.

Bottom-plate sampling using a two-phase operation is adopted. During ϕ_2, (V_{bat}-V_{CMI}) is sampled on all 4 capacitors. V_{CMI} is chosen to be at the middle of the comparator supply voltage.

During ϕ_1, the right sides of the capacitors are connected as follows:

a. C_1 is connected to V_{CASP}, which is given by:

$$V_{CASP} = V_{bat} - I_{ind}R_{on,p} \tag{4.12}$$

b. C_2 and C_3 is connected to V_{Gmn}, and V_{Gmp} given by:

$$V_{Gmn} = V_{bat} - KI_{Gmn}R_{on,p} \tag{4.13}$$

$$V_{Gmp} = V_{bat} + KI_{Gmp}R_{on,n} \tag{4.14}$$

c. C_4 is connected to V_{ripple} given by:

$$V_{ripple} = V_{bat} - \Delta I R_{on,p} \tag{4.15}$$

Since the capacitor terminals are not reset after ϕ_2, and only their right sides are connected to the above voltages, then the capacitors must maintain the same charge they acquired during ϕ_2, which forces the right sides of the capacitors to be equal to (V_{bat}-V_{CMI}) minus the voltages given by (4.12)-(4.15).

By end of ϕ_1, $V_{peak,p}$ and $V_{peak,n}$ can be expressed by:

$$V_{peak,p} = V_{CMI} + \frac{C_3}{C_3 + C_4}(V_{CASP} - V_{bat}) + \frac{C_4}{C_3 + C_4}(V_{Gmn} - V_{bat})$$

$$= V_{CMI} + \frac{C_3}{C_3 + C_4}\left(-I_{ind} R_{on,p}\right) + \frac{C_3}{C_3 + C_4}\left(-K I_{Gmn} R_{on,p}\right) \tag{4.16}$$

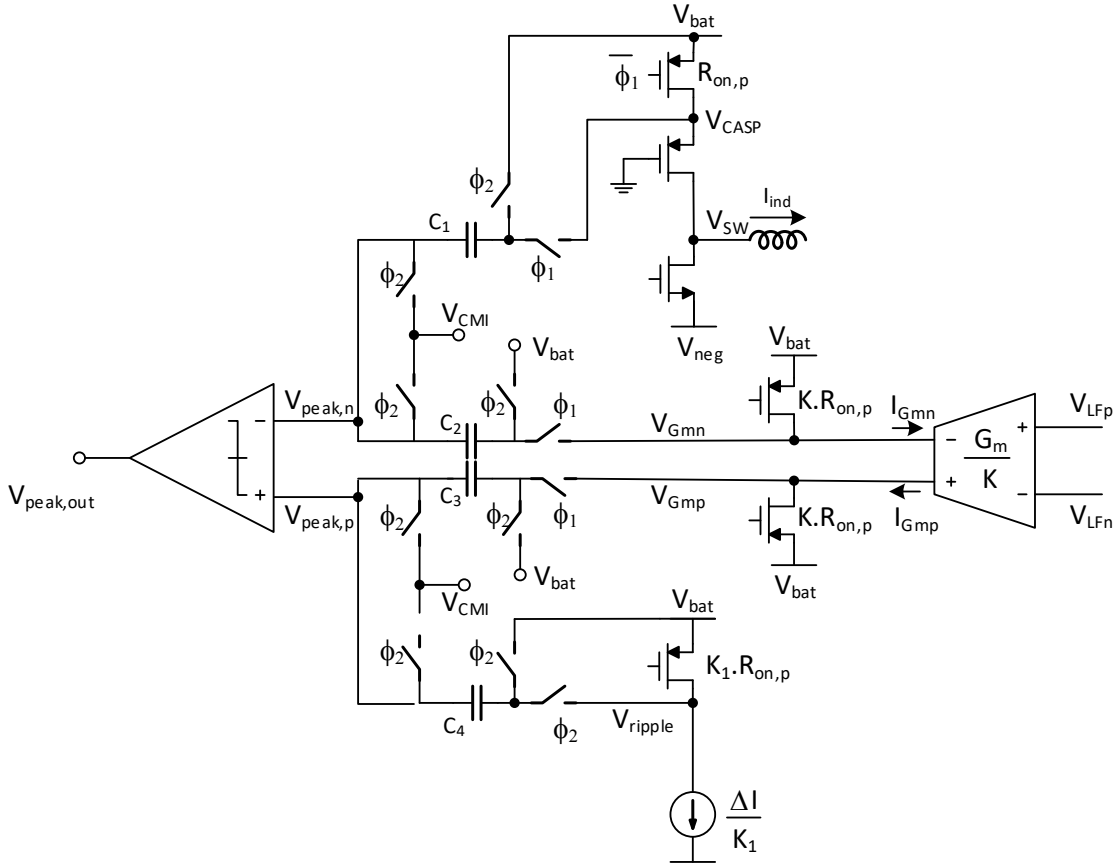


Figure 4.12 Capacitive summation/subtraction for peak comparator

Similarly,

$$V_{peak,n} = V_{CMI} + \frac{C_1}{C_1 + C_2}\left(V_{ripple} - V_{bat}\right) + \frac{C_2}{C_1 + C_2}\left(V_{Gmp} - V_{bat}\right)$$

$$= V_{CMI} + \frac{C_1}{C_1 + C_2}\left(-\Delta I R_{on,p}\right) + \frac{C_2}{C_1 + C_2}\left(-K I_{Gmp} R_{on,p}\right) \quad (4.17)$$

If C_1=C_3, and C_2=C_4, then the comparator triggers if this condition is satisfied:

$$I_{ind} > \Delta I + \frac{C_2}{C_1} K\left(I_{Gmp} - I_{Gmn}\right) \quad (4.18)$$

Similarly, the valley comparator triggers if this condition is satisfied:

$$I_{ind} < -\Delta I + \frac{C_2}{C_1} K\left(I_{Gmp} - I_{Gmn}\right) \quad (4.19)$$

Now, looking at the detailed implementation of each of these switched capacitor paths, Figure 4.13 shows the switches connected to C_1 of Figure 4.12. The sizes of the

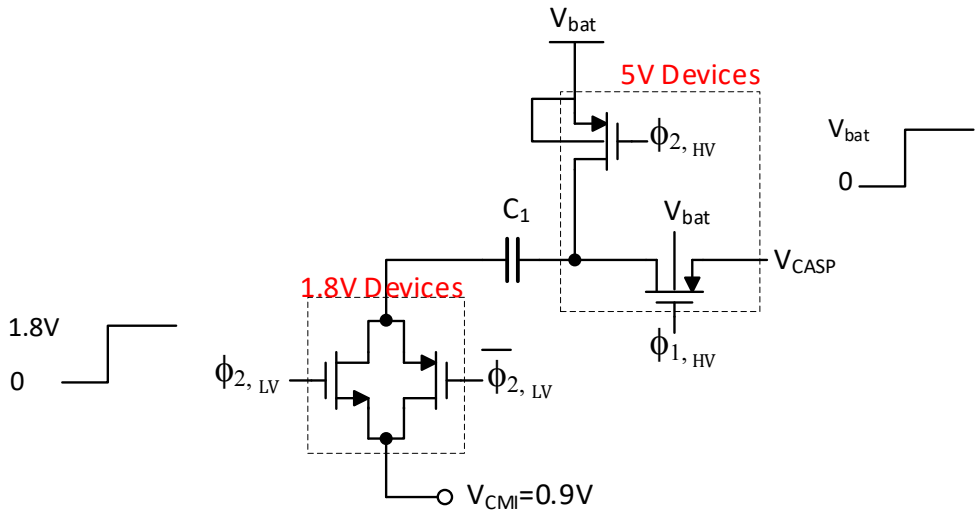


Figure 4.13 Switch implementation for C_1 path of Figure 4.12

switches are chosen to be close to minimum in order to minimize charge injection, which would corrupt the sampled data when the switches are turning off. Two types

of devices are used to realize the switches: (1) 5V devices, which can sustain a maximum of 5V across any pair of their terminals, to realize switches connected to the trans-conductor, output stage, and the ripple current generator, (2) 1.8V devices are used to realize switches connected to the comparator inputs and V_{CMI}.

Two voltage domains are needed to control the switches of Figure 4.13: (1) 1.8V domain for $\Phi_{2,\,LV}$ and (2) V_{bat} voltage domain for $\Phi_{2,\,HV}$ and $\Phi_{1,\,HV}$. In addition, a third voltage domain is needed to control the 5V devices used for the valley comparator, where the voltage swing of the clocks needs to be from 0 to V_{neg}.

The clock signals are generated in the 1.8-V domain and then level-shifted to both V_{bat} and V_{neg} domains.

Figure 4.14 shows the detailed implementation for the level shifter used for the peak comparator clocks. The input clock $\Phi_{1,\,LV}$ is inverted and used to control the input pair M_{N1} and M_{N2}. When $\Phi_{1,\,LV}$ goes from low to high, M_{N1} turns on and M_{N2} turns off, and initially, V_{O1} is at V_{bat} while V_{O2} is at Gnd_{clean}. In order for the LV to change

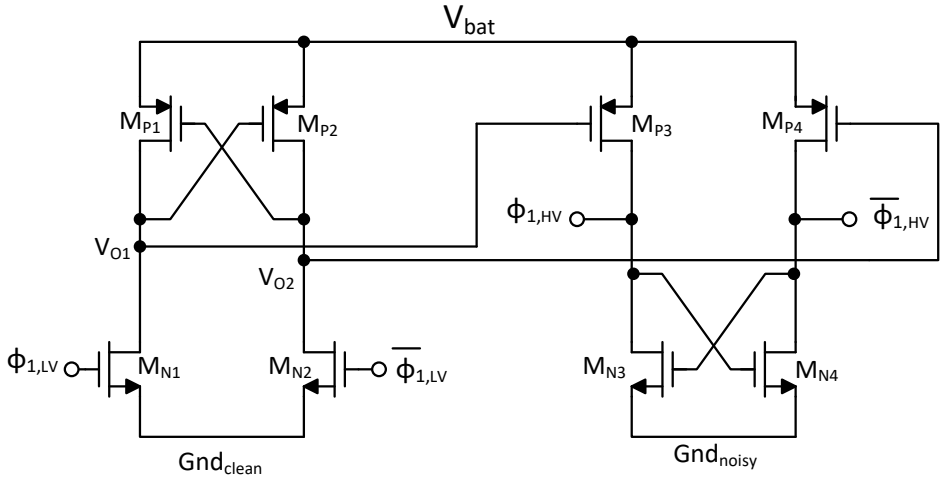


Figure 4.14 1.8V to V_{bat} level shifter

state, M_{N1} (with VGS = 1.8V) must overcome M_{P1} (with VGS = V_{bat}), which necessitates that aspect ratio of M_{N1} and M_{N2} must be designed to be large enough to allow the first stage of the LV to change state. Similar considerations are needed for sizing M_{P3} and M_{P4} so that the second stage is able to change state as well.

Two different ground signals are used on this chip: A clean analog ground (Gnd_{clean}) and a noisy ground for the switching modules (Gnd_noisy). The second stage of the level shifter of Figure 4.14, converts the clock reference from Gnd_{clean} to Gnd_{noisy} to interface with the summing stage.

4.1.4 Comparator design

Since the control loop is sliding-mode based, no clock source is available to strobe the peak and valley comparators or control the switched-capacitor phases. As

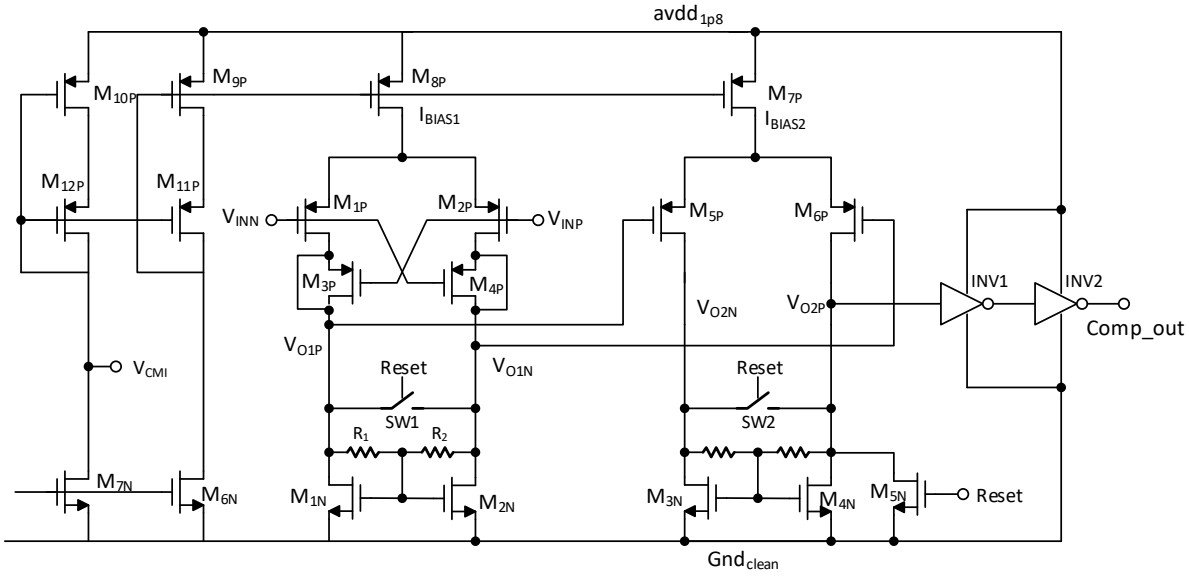


Figure 4.15 Peak/Valley comparator implementation

explained in Section 3.3.5, the loop-switching frequency is variable and is set by the peak and valley comparator decisions.

For this reason, the comparator itself is asynchronous and is implemented as a cascade of gain stages as shown in Figure 4.15. The input stage is biased by a 40uA current source M_{8P} to realize a delay of approximately 20ns, and the input devices are sized to limit the input-referred random offset to about 1.5mV (i.e. 1 sigma). A large random offset would result in false triggers before (or after) the inductor current reaches the target value, with may result in an increase for the inductor current ripples (±ΔI), which degrades the efficiency and distortion. The input-stage topology is selected to increase the differential gain, and therefore, minimize the offset contributions from the nmos load devices (M_{1N} and M_{2N}). A simple common-mode feedback mechanism is implemented by R_1 and R_2, which averages the output of the first stage (V_{O1P} and V_{O1N}), thereby rejecting the differential swing and feeding only the common-mode voltage back to the gates of M_{1N} and M_{2N}.

In response to the comparator differential input voltage, the first stage amplifies this difference, and the differential voltage V_{O1P}-V_{O1N} reacts. When V_{O1P} (or V_{O1N}) changes value, the C_{GD} of M_{1P} would need to charge (or discharge), and therefore, a current must be drawn from the circuit preceding the comparator (switched-capacitor summer/subtracting circuit in this case). If the output impedance of the preceding stage is not low enough, this current would result in "kickback" noise, which appears as an added dynamic offset at the input, and therefore, can result in false triggering. Capacitive neutralization [28] is implemented where a pair of devices (M_{4P} and M_{3P}) used as capacitances as shown in Figure 4.15.

The widths of M_{4P}/M_{3P} are sized to be half those of the input pair and therefore, has gate-source capacitance equal to the gate-to-drain capacitance of M_{1P}/M_{2P}. Because the voltage variations at the drains of M_{1P} and M_{2P} are complementary, the charge currents come now from capacitances (M_{4P} and M_{3P}) and not from the circuit preceding the comparator.

The second stage is a scaled-down version of the first stage with a bias current of 10uA. Two CMOS inverters follow the second stage to produce the final output. The branch consisting of M_{10P}, M_{12P}, and M_{7N} is used to generate the input common-mode voltage (V_{CMI}) used in Figure 4.12. M_{12P} has the same current density as the input pair and similarly as M_{10P} and M_{6P}. This ensures that V_{CMI} tracks with the input pair required headroom over process, supply voltage and temperature variation.

In the reset phase, when the inputs are shorted to V_{CMI}, the output of such an asynchronous comparator depends on the offset, which means that the following SR flip flop can be driven into unexpected states. To resolve this issue, the differential outputs of each gain stage are shorted by S_{W1} and S_{W2}, while V_{O2P} is pulled down to ground through M_{5N}. This ensures that the comparator output is defined throughout the reset state.

4.1.5 Comparator clock generation

As shown in Figure 4.16, during ϕ_1, the peak comparator is in the active mode waiting for the inductor current to cross the trigger level, while the valley comparator is idle and in the reset state. Once the peak comparator triggers, the following SR flip-flop is set, defining a new switching clock phase ϕ_2 where the peak comparator is reset, and the valley comparator is activated. At the same time, the new SR state turns

off the output pmos and turns on the output nmos device, thus forcing the inductor current waveform to change directions, so that it starts to ramp down towards the trigger level defined by the ripple (ΔI) and the transconductance output. Once the valley comparator triggers, the following SR FF is reset, defining a new switching phase ϕ_1 where the valley comparator is reset, and peak comparator is activated. At the same time, the new SR state turns off the output nmos and turns on the output pmos device, which forces the inductor current waveform to change directions again and the cycle repeats.

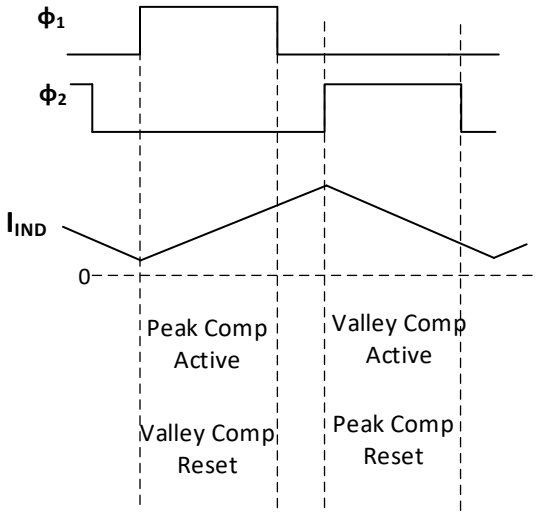


Figure 4.16 Comparator modes

Figure 4.17 shows the switched capacitor networks that are used to sum and subtract the inputs to both the peak and valley comparators with the respective clock phases. The figure also shows the interface to the SR flip-flop, which generates the clock phases back to the switched capacitor networks as well as for the final non-overlapping clock driver that switches the output stage.

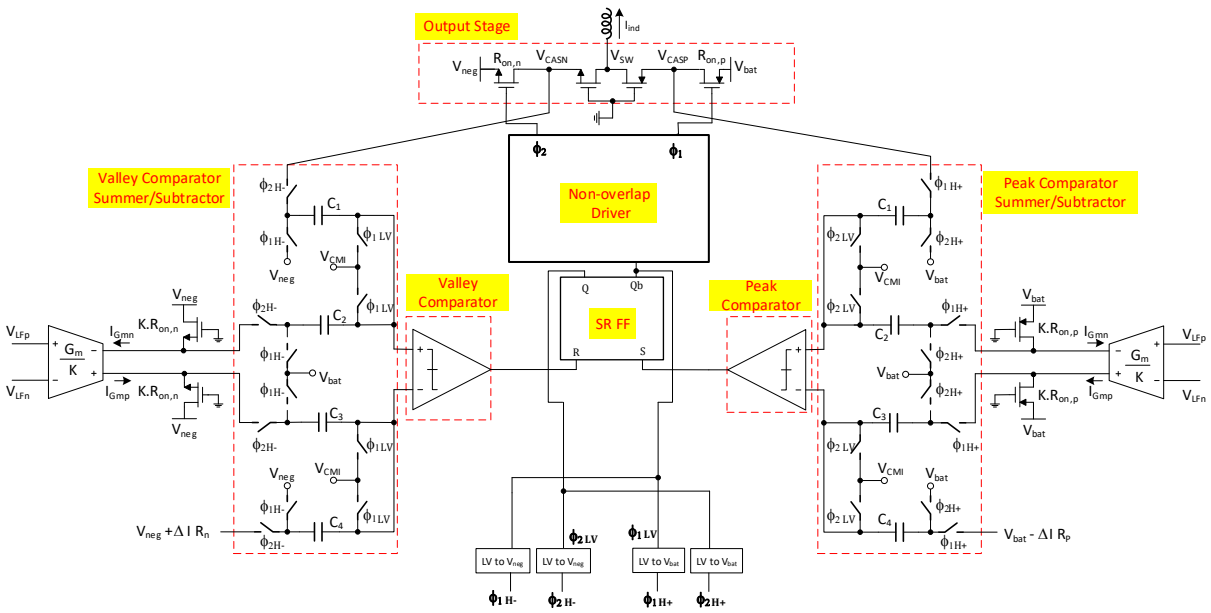


Figure 4.17 Switching clock generation

4.1.6 Blank time design

In Section 4.1.2.2, the use of cascode nodes (V_{CASP} and V_{CASN}) instead of V_{SW} to sense the current was discussed, and the transient of V_{SW} was simplified in Figure 4.10 to illustrate the concept. During most of the switching cycle, the transient behavior for the cascode nodes or the switching node is similar to what was illustrated earlier; however, the behavior is different during the non-overlapping time, when both the high-side and low-side switches (M_{POUT} and M_{NOUT}) are off, while the inductor current must then flow through parasitic diodes. In this work, the

polarity and amplitude of this inductor current depends on the output signal and its amplitude. As an example, shown in Figure 4.18, assuming that the output signal

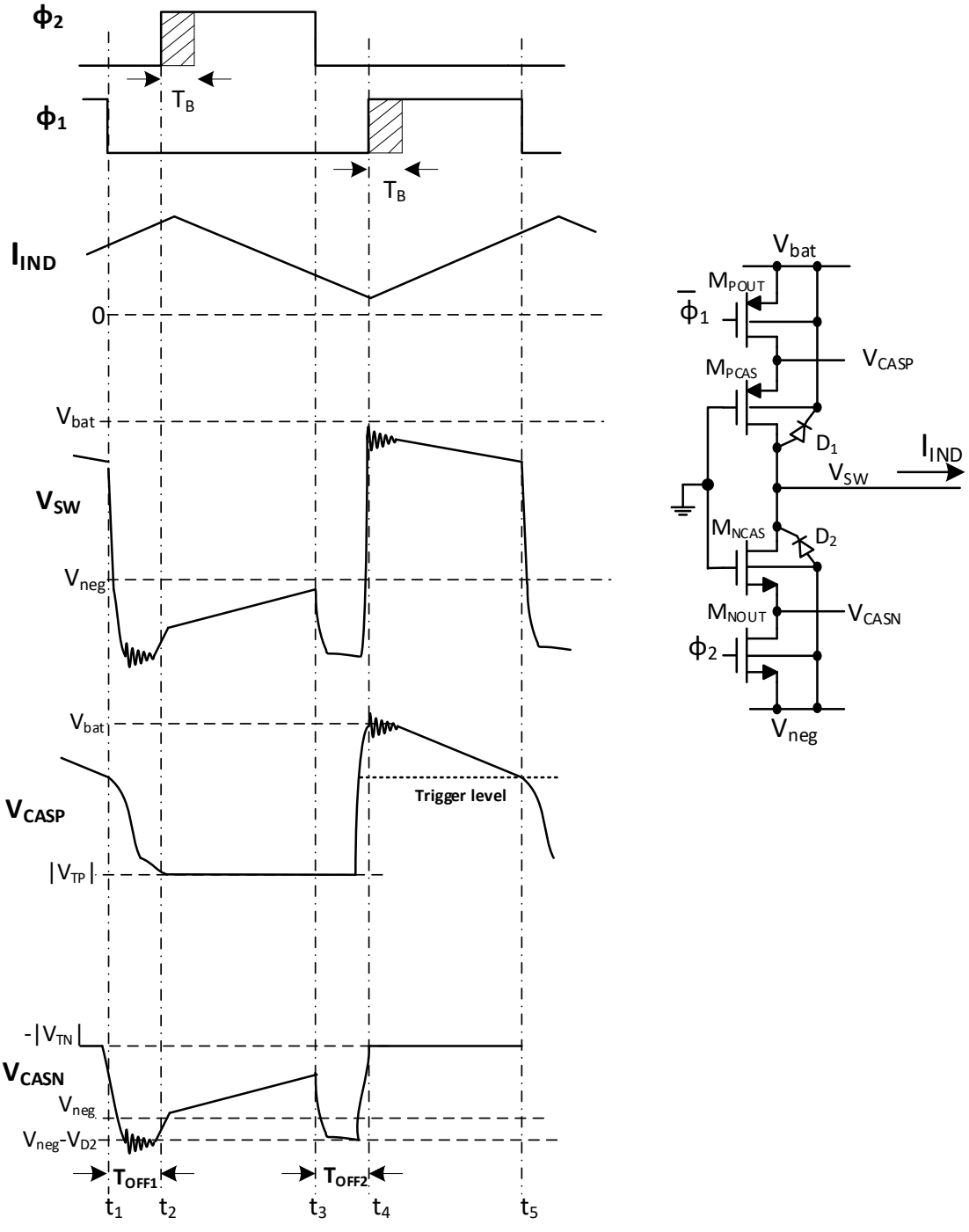


Figure 4.18 Transient waveforms for the output stage for a positive large inductor current

across the load is large and positive, which implies that the inductor current is large and positive (flowing out of the output stage). During the non-overlapping time T_{OFF2}, the inductor must continue to conduct current forcing the drain-to-bulk junction diode of M_{NCAS} (D_2) to turn on. As a result, both V_{SW} and V_{CASN} drops below V_{neg} by V_{D2}, which varies depending on how much current is flowing. Once ϕ_1 turns on, the inductor current is steered to M_{POUT}. This sudden change of the current path may result in damped oscillation on the internal V_{bat} due to the activation of the LC tank formed by the bondwire inductance and the internal parasitic supply capacitor. As a result, V_{CASP} experiences the same oscillation, which can lead to a false triggering to the current-controlled loop. Because of this transient behavior for both V_{CASP} and V_{CASN}, it is necessary that a blank time is introduced such any false triggering is masked out for a period of time after the rising edge of ϕ_1 and ϕ_2 (i.e. blank time T_B) until the internal nodes settle. T_B is nominally set to 40ns and can be programmed from 20n to 80ns in steps of 5ns. In addition, the comparators are kept in their reset state (as explained in Section 4.1.4) until the rising edge of either ϕ_1 (for the peak comparator) or ϕ_2 (for the valley comparator) occurs.

It is worth noting that this oscillation is usually minimized by intentionally increasing the rise/fall times of the gate drivers for ϕ_1 and ϕ_2 and/or using a damping resistor.

4.1.7 Loop filter design: G(s)

As explained in Chapter 3, a single-gain-stage second-order loop filter is designed to reduce the nonlinearities of the output stage and the disturbances on both V_{bat} and V_{neg}. The filter is designed to meet the following requirements:

a. At least 40 dB gain over the audio band
b. Drive the headphone load with 2Vrms signal, and therefore, a maximum of 10uV rms noise at the output meets 106dB target SNR
c. Minimum current consumption
d. Better than 45 degrees phase-margin for the outer voltage loop.
e. Less than 400kHz unity-gain bandwidth for the outer voltage loop in order to maintain at least a ratio of two between the smallest switching frequency (800kHz) and the unity-gain frequency. This guarantees a negligible delay in the current-control loop, which is the assumption used in Chapter 3 to perform the small-signal analysis of the voltage control loop and therefore, guarantees the large-signal stability of the system.

Figure 4.1 shows a block diagram of voltage feedback loop where the closed loop gain (A_{CL}) is given by:

$$A_{CL} = \frac{R_F}{R_{IN}} \tag{4.20}$$

The target maximum signal swing at the output is $2V_{rms}$ ($5.65V_{PP}$); the corresponding peak-peak input swing is given by ($V_{in,pp}$):

$$V_{in,pp} = V_{INP,pp} - V_{INN,pp} = \frac{5.65}{A_{CL}} \tag{4.21}$$

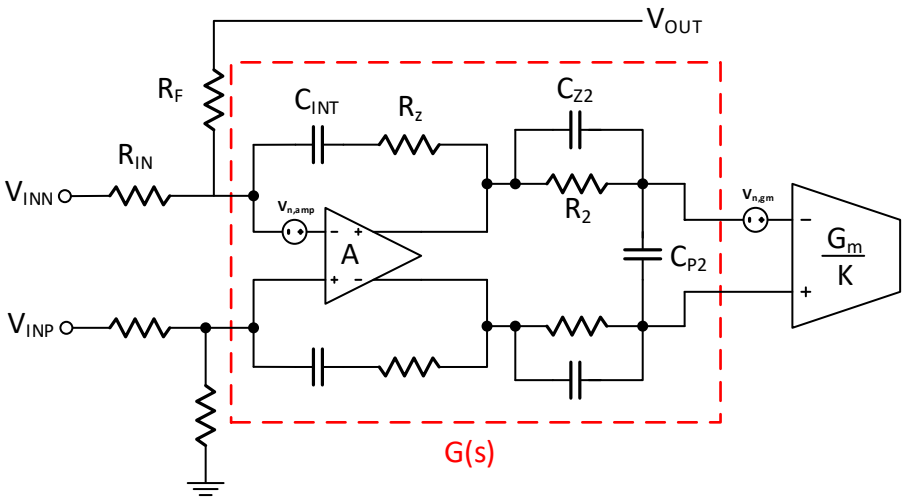


Figure 4.19 G(s) with input/output interface

The input stage is powered from a 1.8V supply, and therefore, A_{CL} is chosen to be 2 so that the signal-ended peak-peak input swing for V_{INP} (or V_{INN}) remains within the supply rail. Higher closed-loop gain results in lower unity-gain frequency and lower gain in the audio band, which results in worse THD.

The target output-referred noise can be referred to the input by dividing by A_{CL}; therefore, the target input-referred noise integrated within the audio band becomes 5μV. The main contributors for this noise are R_F, R_{IN}, and the input devices of the gain stage. The power density for the input-referred noise ($v^2_{n,\ input\_referred}$) can be calculated as:

$$v^2{}_{n,input\_referred} = \left(8kTR_{IN} + v^2{}_{n,amp}\left(1+\frac{R_{IN}}{R_F}\right)\right)\left(1+\frac{R_{IN}}{R_F}\right) + \frac{v^2{}_{n,gm}}{(|G(j\omega)|)^2} \qquad (4.22)$$

Where $v^2_{n,gm}$ is the input-referred noise power density for the transconductance stage and G(jω) is the loop filter gain as shown in Figure 4.19. Table 4.1 shows the relative contributions of the different noise sources.

Table 4.1 Noise contributions

Noise source	Noise (μV)	Contributions in %
R_{IN}	2.657	29.4
R_F	1.862	14.44
$V_{n,amp}$	2.8	32.86
G_m	2.35	23
Total	4.9	100

The choice for width and length of R_{IN} and R_F and their substrate connections, would not only impact the nominal resistor value, but could also affect the THD and noise performance of the driver. First, the resistor area (WL) needs to be large enough to reduce the effect of the flicker noise., and secondly, the length of R_{IN} and R_F should be large enough to reduce the effect of their voltage coefficients nonlinearity on the THD performance[29,30] and similarly, their substrate connection needs to be connected to the proper voltage to reduce the poly resistor conductivity modulation effect on THD [30].

The effects of the poly resistor voltage coefficient and conductivity modulation manifest themselves in a variation of the nominal resistor value as a function of the terminal voltages as given by:

$$R = R_0\left(1 + \alpha_1 V_{diff} + \alpha_2 {V_{diff}}^2\right)\left(1 + \beta(V_{comm} - V_{bulk})\right) \quad (4.23)$$

where R_0 is the nominal resistor value, and the terminal voltages are defined in Figure 4.20. The first term in the equation describes the variation of the resistor due to the voltage coefficients α_1 and α_2, whereas the second term shows the effect of the conductivity modulation coefficient β.

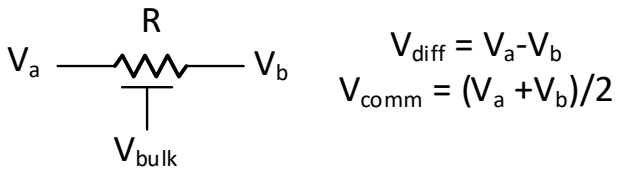
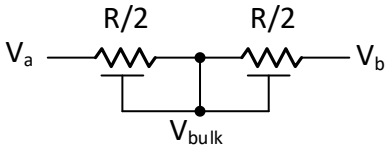


Figure 4.20 Resistor terminal definition

The coefficient α_1 is usually negligible compared to α_2, making this effect only a function of the squared of the differential voltage. Since both R_{IN} and R_F have unequal differential signal-dependent swing across them, then the closed-loop gain (A_{CL}) suffers from a second-order nonlinearity, which limits the maximum achievable THD+N. Since α_2 scales down with the length of the resistors, this effect can be reduced by increasing both the length and width of R_F and R_{IN} to reduce α_2, and thus, the second-order nonlinearity without altering the resistor value.

The second effect is the resistor conductivity modulation, which refers to the variation of the resistor value as a function of the difference between the common mode voltage across the resistor and its substrate voltage (V_{comm} - V_{bulk}).

Unfortunately, the coefficient β doesn't scale with any of the resistor dimensions, and therefore, a circuit technique is necessary to eliminate this effect. Figure 4.21 shows the technique used [30], --which is adopted in this work-- where a resistor R is decomposed into two equal parts in series, with the bulk of both resistors connected to the middle net. This ensures that V_{comm} is equal to V_{bulk}, thereby cancelling the second term in equation (4.23).



$$V_{comm} = V_{bulk} = (V_a + V_b)/2$$

Figure 4.21 Circuit technique to eliminate the conductivity modulation

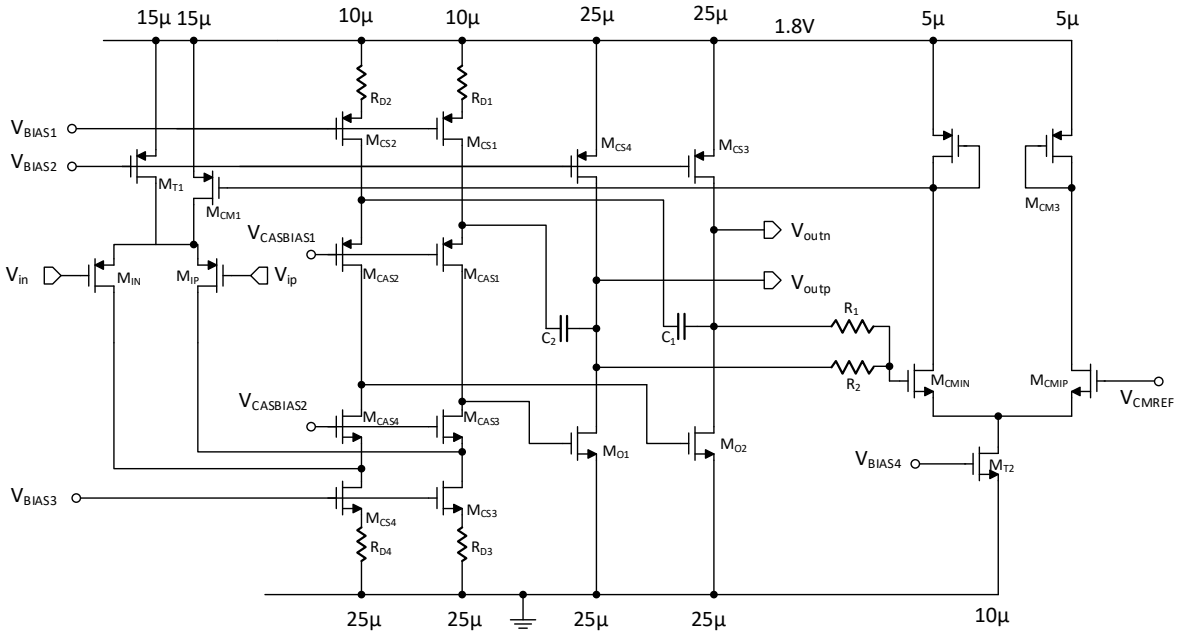


Figure 4.22 Amplifier implementation

Figure 4.22 shows the differential amplifier implementation, which consists of two stages: A folded-cascode first stage with a pmos input pair, and a common-source second stage. Cascode compensation, also known as Ahuja compensation [9], is used to stabilize the amplifier by ac-coupling the amplifier outputs to the source nodes of the cascode devices (M_{CAS1} and M_{CAS2}) of the first stage through C_1 and C_2. A pair of identical resistors (R_1 and R_2) is used to sense the output common mode, which is compared to a reference voltage V_{CMREF} by an error amplifier whose output is used to control a portion of the input stage tail current source in order to regulate the output common-mode voltage. In addition, source degeneration resistors (R_{D1}-R_{D4}) are used to lower the input referred noise of the amplifier as shown in the figure.

The amplifier is powered from a 1.8V supply, and uses all low-voltage devices, and consumes about 120μA of quiescent current. Its bandwidth is about 8MHz in order to have a small effect on the global loop stability.

4.1.8 Transconductance stage design

The transconductance stage shown in Figure 4.23, receives the loop filter G(s) output (V_{LFP} and V_{LFN}) and generates a linearly-proportional differential current. This current is then mirrored and then applied to a pair of series devices ($K.R_{on,N}$ and $K.R_{on,P}$), which are scaled-down replicas from the output stage devices as previously shown in Figure 4.11.

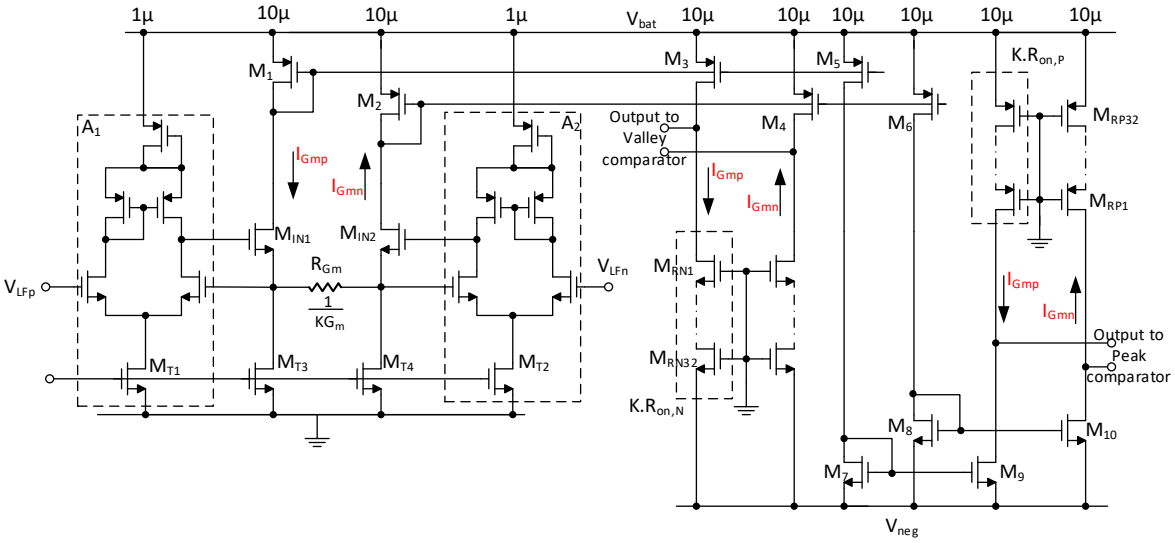


Figure 4.23 Transconductance implementation

The differential voltage across the $K.R_{on,N}$ switches is sensed by the valley comparator, while the differential voltage across the $K.R_{on,P}$ switches is sensed by the peak comparator. To enhance the linearity of the transconductor, two simple amplifiers A_1 and A_2 are used in conjunction with M_{IN1} and M_{IN2} to form a super source-follower configuration as shown in Figure 4.23. Using these amplifiers, the differential input voltages V_{LFp}-V_{LFn} is copied across R_{Gm}, and therefore; generates a differential current (I_{Gmp}-I_{Gmn}), which itself gets copied to generate the two

differential output voltages that go to the peak and the valley comparator as shown in Figure 4.23.

4.1.9 Negative charge-pump (NCP) design

Figure 4.24(a) shows the negative charge pump topology [30], which consists of four devices (M_1-M_4) and two external capacitors C_{fly} and C_{hold}. As shown in Figure 4.24(b), during ϕ_1, C_{fly} samples V_{bat} on the top plate with respect to ground. During ϕ_2, the top plate gets connected to ground while the bottom plate is connected to the hold cap (C_{hold}). This forces the bottom plate of C_{fly} to float towards $-V_{bat}$ while charge sharing with C_{hold}; eventually V_{neg} settles to $-V_{bat}$ in the steady state. The periodic action of charging C_{fly} and discharging it to C_{hold} can be modeled as a switched capacitor resistor with a value of (T_s/C_{fly}), where T_s is the switching period, and therefore, the settling time is characterized by a time constant (τ) expressed as:

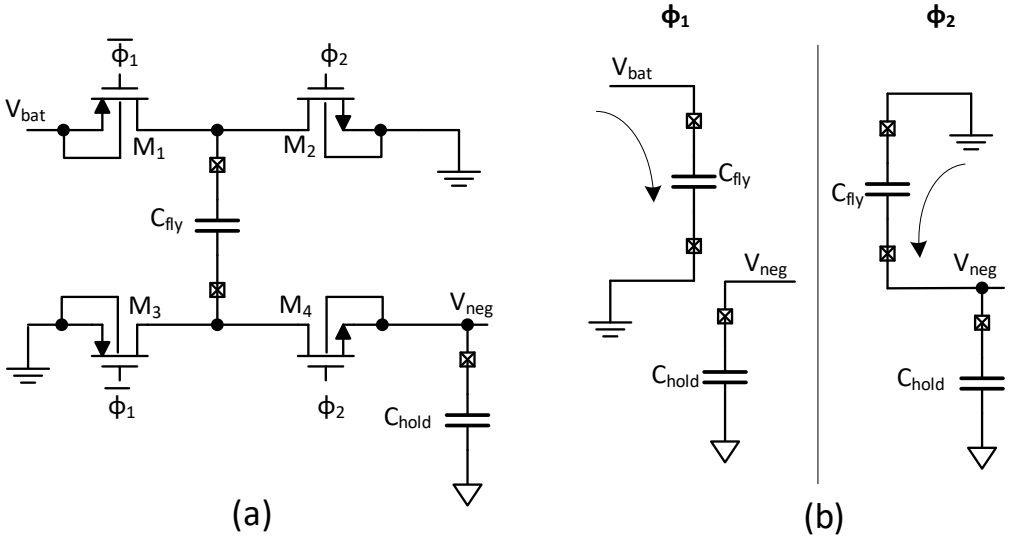


Figure 4.24 Negative charge-pump topology

$$\tau = T_s \frac{C_{hold}}{C_{fly}} \tag{4.24}$$

This time constant poses a constraint on the choice of the external capacitor values to obtain a reasonable settling time. In addition, the output stage continually loads the NCP as shown in Figure 4.25. This means that C_{hold} continues to provide charge for the output stage even when C_{fly} is connected to V_{bat} during ϕ_1. Depending on how much current is drawn from C_{hold} in ϕ_1, V_{neg} would increase, which limits the signal swing headroom.

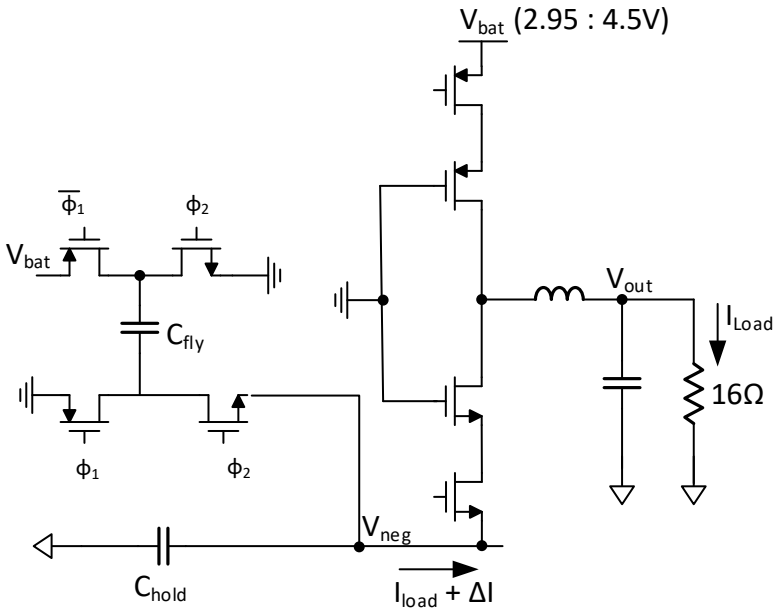


Figure 4.25 Charge-pump loaded by the output stage

To relieve this issue, C_{hold} and T_s must be chosen to allow only a maximum predefined drop in V_{neg}. The worst-case drop occurs when the output stage draws the maximum current from NCP during ϕ_2 as shown in Figure 4.25; this current is calculated by:

$$I_{max} = \frac{\max V_{peak}}{\min R_{load}} + \Delta I = \frac{2.82}{16} + 40mA = 216mA \tag{4.25}$$

Thus if the maximum charge pump output equals $V_{CP,\,MAX}$, then the minimum $C_{hold,min}$ can be calculated by:

$$C_{hold,min} = \frac{I_{max}}{V_{bat} - V_{CP,MAX}} \frac{T_s}{2} \tag{4.26}$$

If V_{bat}- $V_{CP,\,MAX}$ is limited to 150mV, and the NCP switching frequency is limited to 150kHz (to limit the dynamic power loss), then $C_{hold,min}$ equals 5μF.

The CP switch sizes are optimized to offer a balance between optimizing for power efficiency and quiescent current. To illustrate this optimization, the CP model is shown in Figure 4.26.

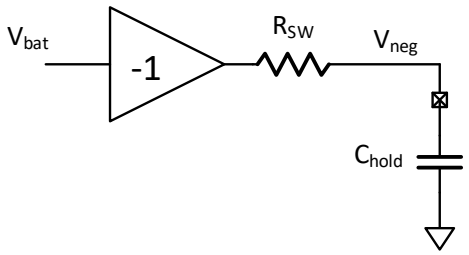


Figure 4.26 CP Model

If all switches have negligible on resistance, R_{SW} could be expressed as the known switched cap resistance: T_S/C_{fly}. However, if the switch's on resistance is not negligible, then R_{SW} can be derived more accurately by calculating the finite settling time for both phases [32]:

$$R_{SW} = \frac{T_S}{C_{fly}} \frac{1 - e^{-\frac{T_S}{2C_{fly}}\left(\frac{1}{(R_1+R_3)}+\frac{1}{(R_2+R_4)}\right)}}{\left(1 - e^{-\frac{T_S}{2C_{fly}}\left(\frac{1}{(R_1+R_3)}\right)}\right)\left(1 - e^{-\frac{T_S}{2C_{fly}}\left(\frac{1}{(R_2+R_4)}\right)}\right)} \tag{4.26}$$

Where R_1, R_2, R_3, and R_4 are the on-resistances for M1, M2, M3, and M4, respectively, shown in Figure 4.24. Using their values, shown in Table 4.2, results in an effective output resistance of 1.6Ω.

This value was chosen to be close to the on-resistance of the nmos switch of the output stage such that the efficiency conduction loss due of the CP would be similar to that of the nmos switch. Reducing this resistance even more in order to improve the efficiency can adversely affect the quiescent current since the larger the switch size or the switching frequency, the more dynamic power it consumes, thereby degrading the quiescent current. The target quiescent current of the charge pump for this design is about 100μA.

Table 4.2 Negative charge-pump switch sizes

	M_1	M_2	M_3	M_4
W/L	38400/0.5	20160/0.6	38400/0.5	20160/0.6
Ron @ 3.7V	200mΩ	119mΩ	200mΩ	119mΩ

Another issue that was addressed in this design is the surge current drawn from V_{bat} at startup, and this is because initially every time C_{fly} gets connected to V_{bat} during ϕ_1 a large charging current results to charge C_{fly} [33]. This initial current is simply V_{bat} divided by the sum of the on-resistances of M_1 and M_3, which would be close to almost 9A. This peak current will die out with time as the CP output settles to steady state; however, having such a high current flowing into the CP initially, can damage the switch devices as well as the metals routings connected to those devices.

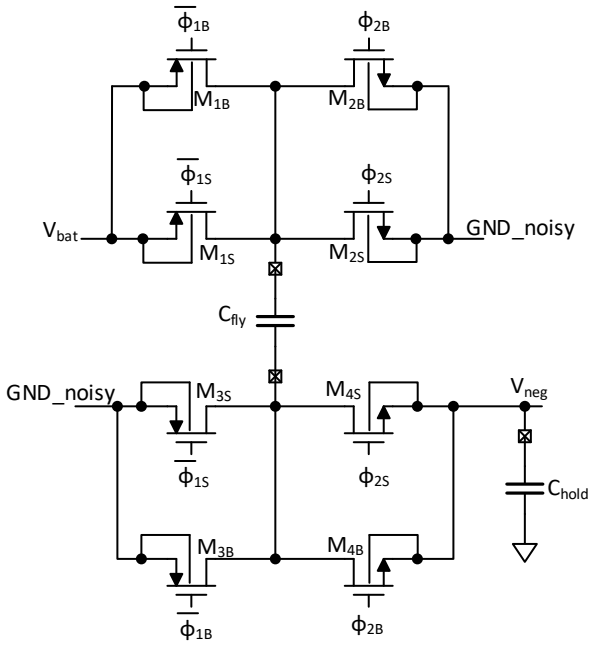


Figure 4.27 Charge-Pump Design

To resolve this issue, a soft start-up technique is adopted [33] where all CP switches are broken into two parallel devices, M_B and M_S, as shown in Figure 4.27; transistors M_s are simply one finger of the entire device, whereas transistors M_B have the rest of the fingers and constitute the bulk of the device. Therefore, the M_S on-resistances are 24 times larger than those of M_B. During the start-up, before the CP settles and reaches the steady state, only M_S is clocked while M_B remains off, and thus, the peak current flowing is reduced by a factor of approximately 24 times -- i.e., from 9A down to 375mA-- which can be sustained. Once CP has reached steady state, transistors M_B are activated in preparation for the overall loop to go out-of-reset and start driving the headphone load. This behavior is shown in Figure 4.28, where initially ϕ_{1s}, and ϕ_{2s} start toggling to control the small switches M_{1S}-M_{4S}, while ϕ_{1B},

and ϕ_{1B} are held idle until the CP goes to the final voltage $-V_{bat;}$ afterwards, ϕ_{1B}, and ϕ_{1B} start toggling indicating that the CP is up and ready to be used.

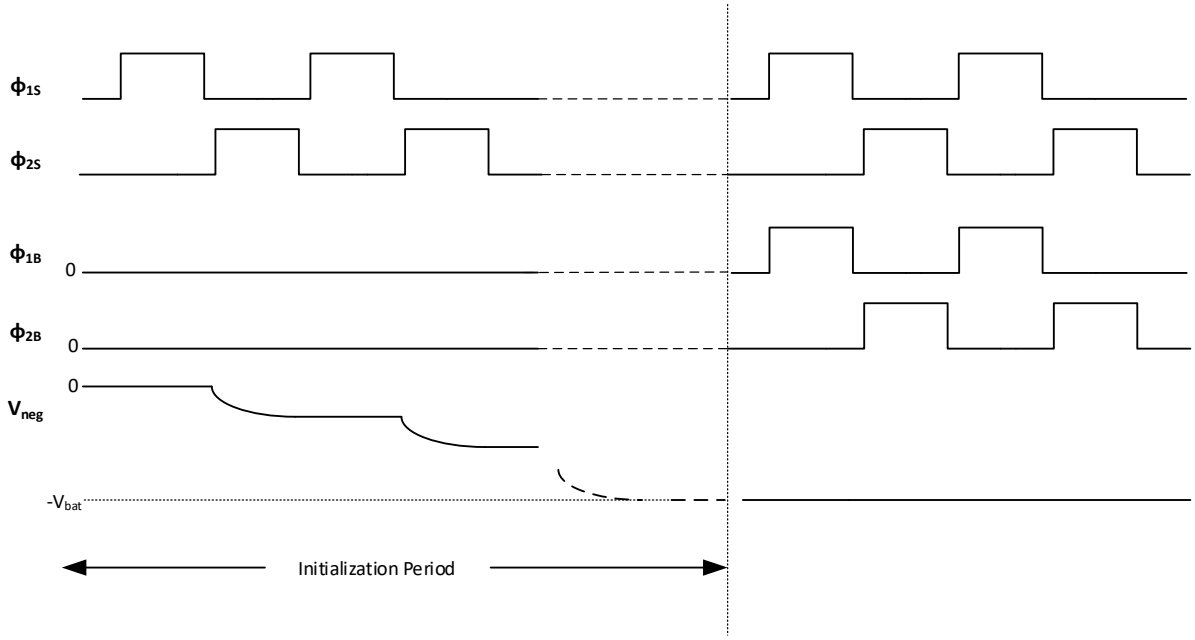


Figure 4.28 Relative timing of the different clock phases of the CP

CHAPTER 5 Experimental Results

A prototype chip was fabricated in TowerJazz 0.18µ PM technology, which supports 4 metal layers and 1 thick top metal. Devices in this technology come with two different oxide thicknesses: thin-oxide devices which has 1.8V maximum voltage across the device junctions, and thick-oxide devices that support up till 5.5V across any of the device junctions. In addition, LDMOS devices are offered but not used in this design.

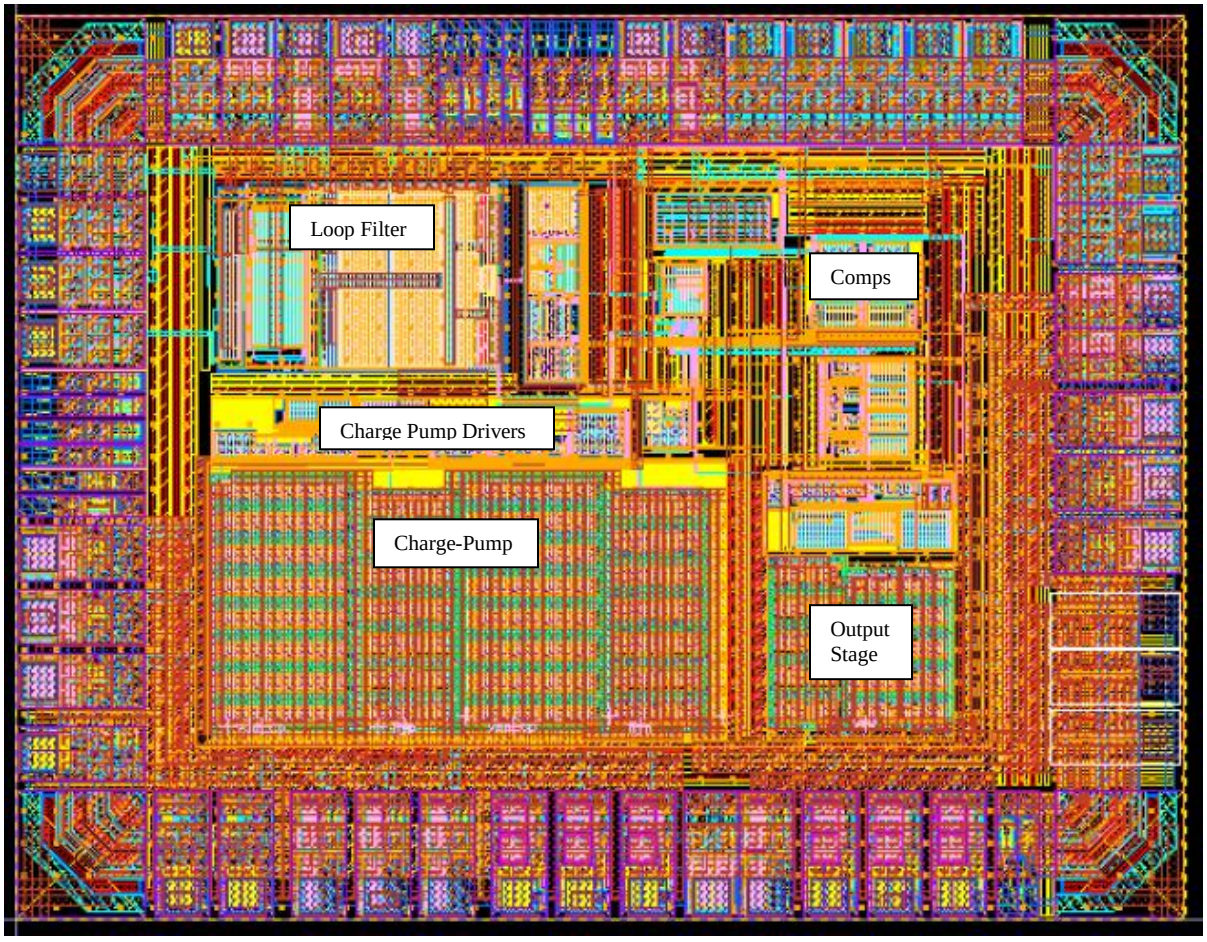


Figure 5.1 Chip Layout

The chip measures 2.46x1.9mm^2 and the layout is shown in Figure 5.1. Top Metal M5 has been extensively used to minimize the routing resistance between the output stage devices, charge-pump devices and the corresponding pads. It is also used for critical signal routings as well as the power supplies to minimize the parasitic routing resistances or the parasitic capacitances.

Figure 5.2 shows the test setup that is used to measure the chip performance, an APx555 audio analyzer is used to generate the analog signal and analyze the output.

Figure 5.2 Test Setup

Figure 5.3 shows the measured THD+N vs. the rms of the input signal for a 16 Ω load using a 3.7V battery supply. The measured gain from input to output is 1.917, which deviates slightly from a design value of 2. Therefore, from the figure, the peak non-A-weighted THD+N is about -96.3dB at an output level of 1.15Vrms. The output level that corresponds to 1% THD distortion (-40dB) is 1.93Vrms, which is equivalent to an output power of 232mW.

Similarly, Figure 5.4 shows the measured THD+N vs. the rms of the input signal for a 32 Ω load using a 3.7V battery supply. The peak non-A-weighted THD+N is about –98.5dB at an output level of 1.69Vrms. The output level corresponds to 1% THD distortion (-40dB) is 2.3Vrms which is equivalent to an output power of 165mW.

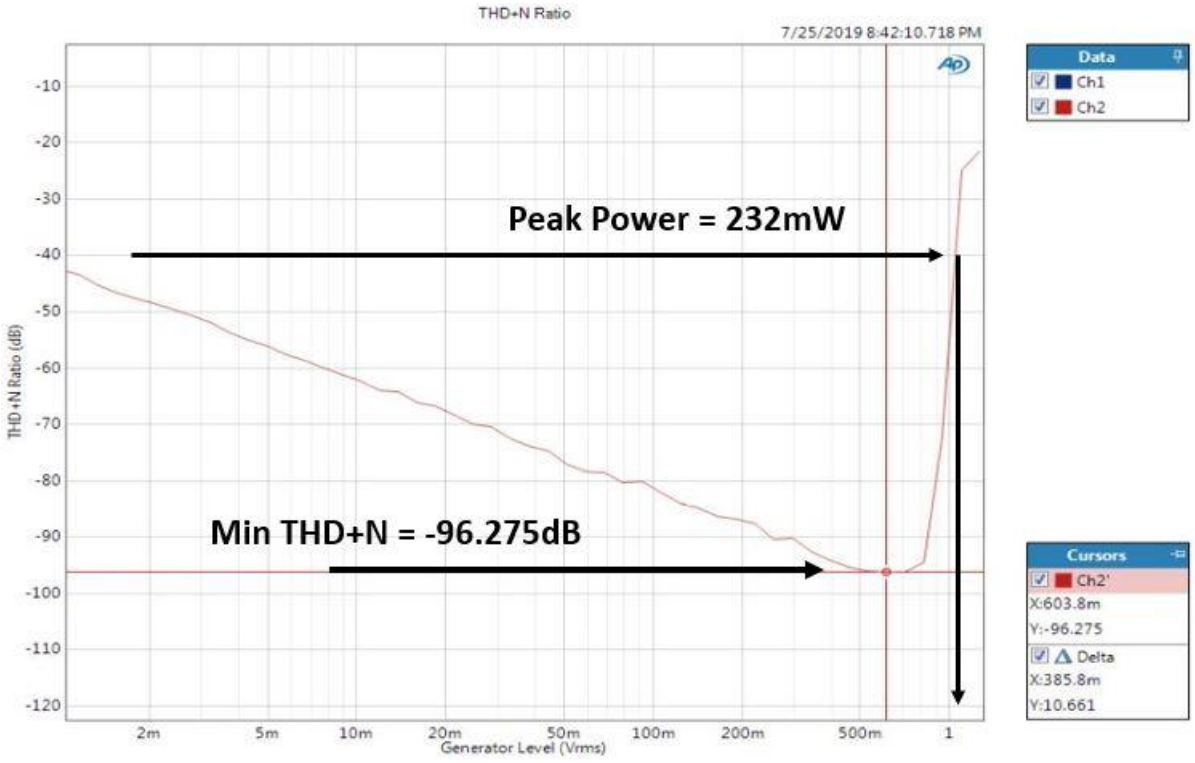


Figure 5.3 Measured THD+N vs. the rms of the input signal for a 16 Ω load

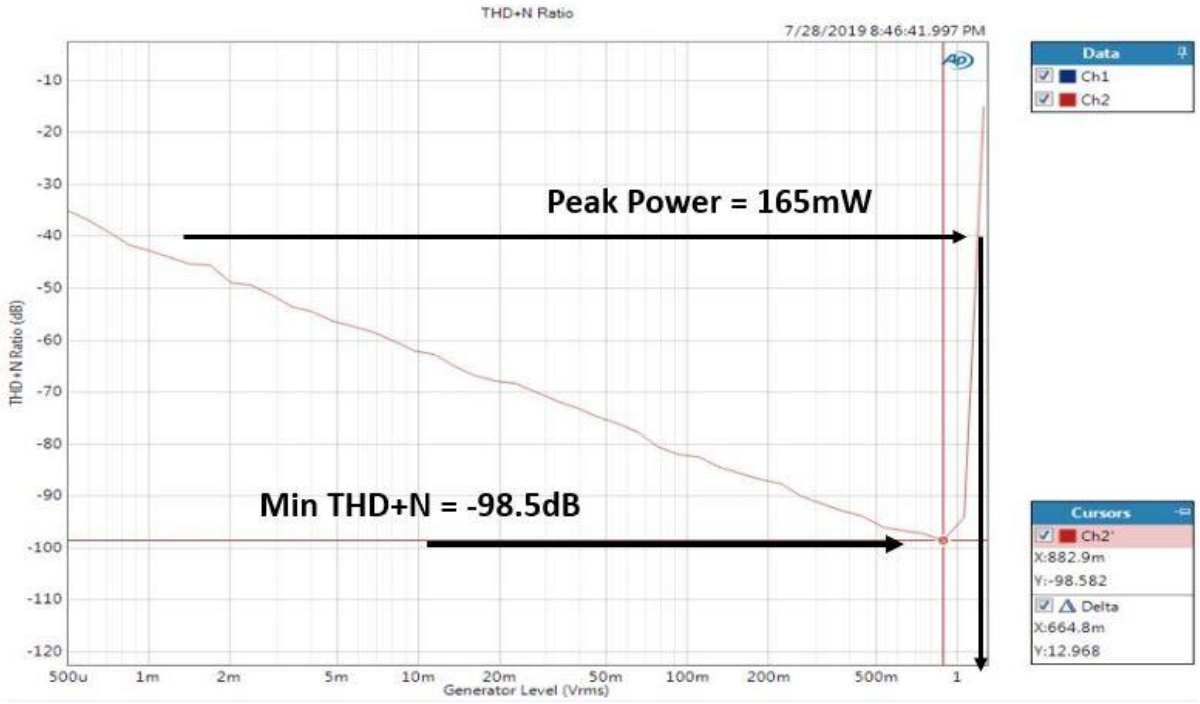


Figure 5.4 Measured THD+N vs. the rms of the input signal for a 32 Ω load

Figure 5.5 shows the measured THD+N vs the rms of the input signal for a 600 Ω load using a 3.7V battery supply. The peak non-A-weighted THD+N is about –98dB at an output level of 1.533Vrms.

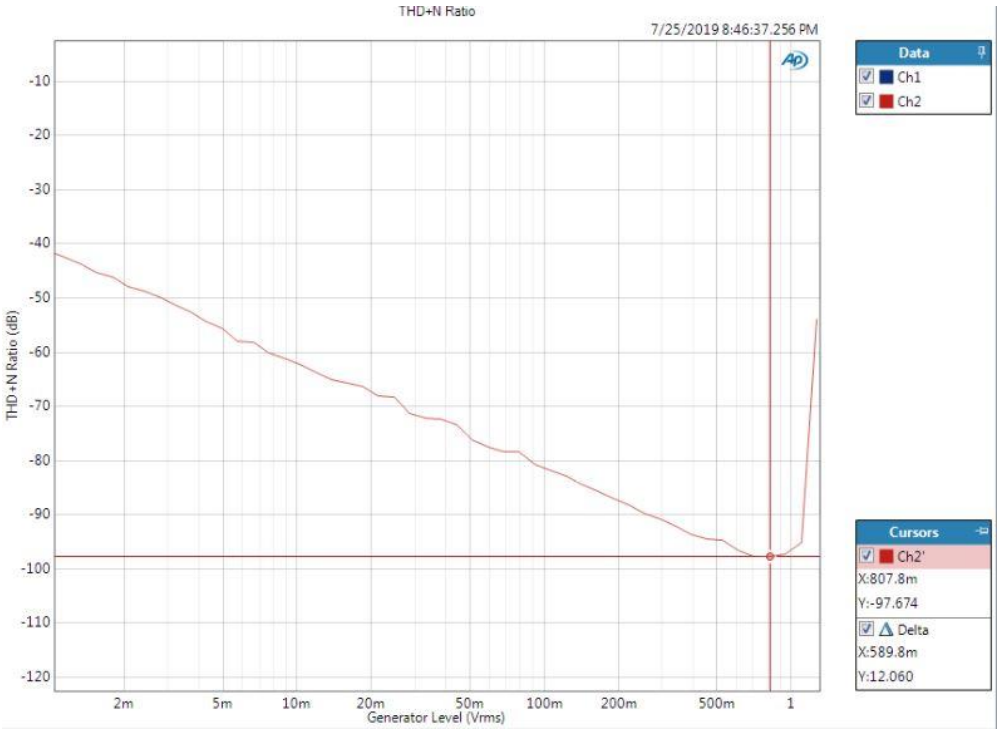


Figure 5.5 Measured THD+N vs. the rms of the input signal for a 600 Ω load

Figure 5.6 shows the FFT results for a 1kHz output tone with rms value of 1.533V using 48K FFT points. It can be observed that the spectrum is dominated by a third-order harmonic at about 105dB below the fundamental signal.

The A-weighted THD+N vs the rms of the input level sweep for a 32Ω load is shown in Figure 5.7. It can be observed that the THD+N for a -60dB input signal is -48.8dB which corresponds to a dynamic range of 108.8dB, this is very close match to the design value of 106dB. This result is consistent with a 10uV measured output-referred noise.

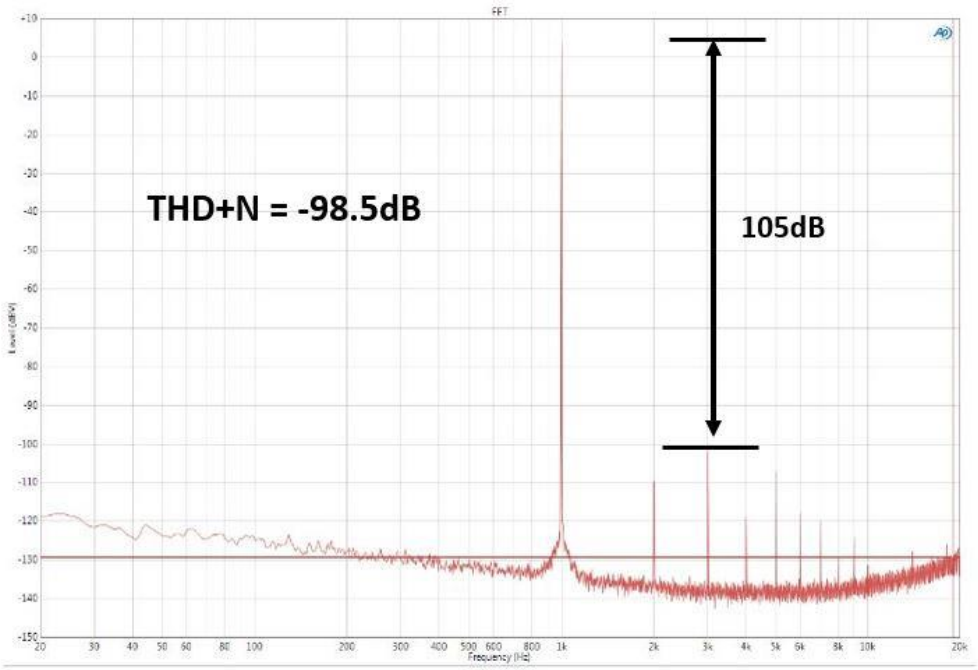


Figure 5.6 Output spectrum for 1.5Vrms 1kHz output with a 32 Ω load

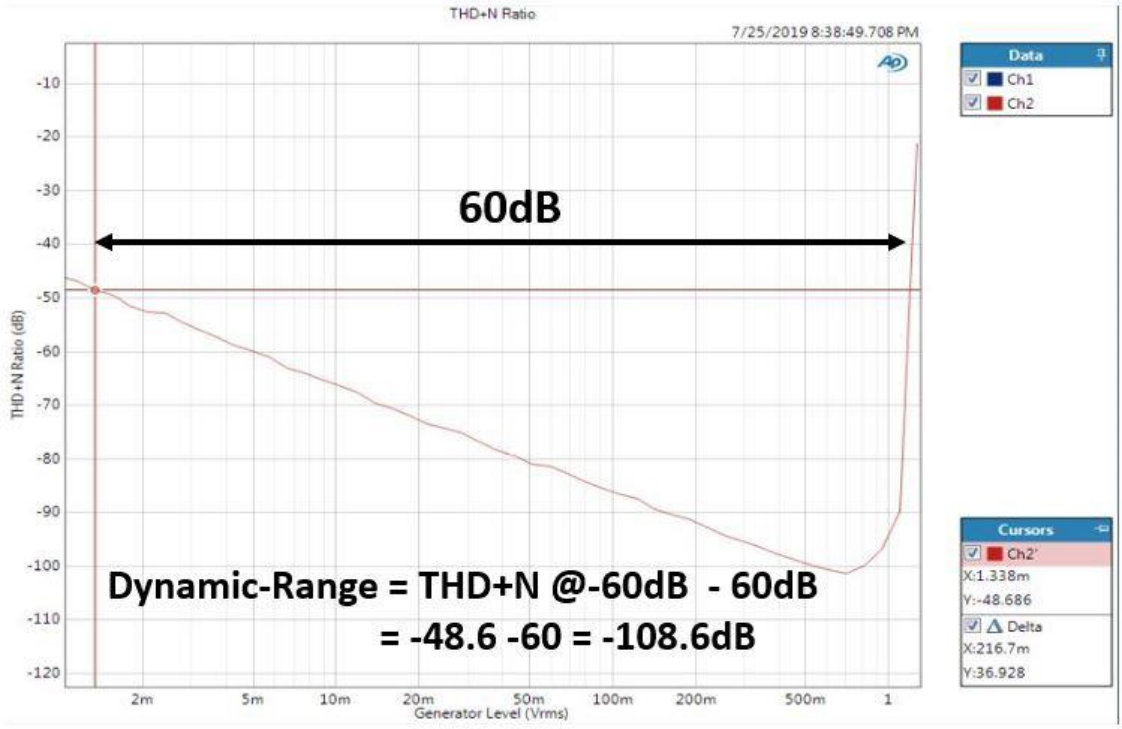


Figure 5.7 Measured A-weighted Dynamic Range for a 32 Ω load

The measured quiescent current is about 1.55mA, which is composed of 250uA from the 1.8V supply and 1.3mA from the 3.7V battery supply including the charge-pump current. The current consumed from the 1.8V supply is close to the simulated value of 280uA, while the current from 3.7V battery is higher than a schematic-only quiescent current simulation of 1mA. This difference can be attributed to conduction loss for all the layout routing resistances as well the PCB routing, and ESR of the external capacitors. Figure 5.8 shows the overall measured power efficiency for both 16 and 32Ω loads as a function of the normalized output power. The normalized output power is the driver output power divided by the maximum theoretical output power, as expressed in Equation (1.9).

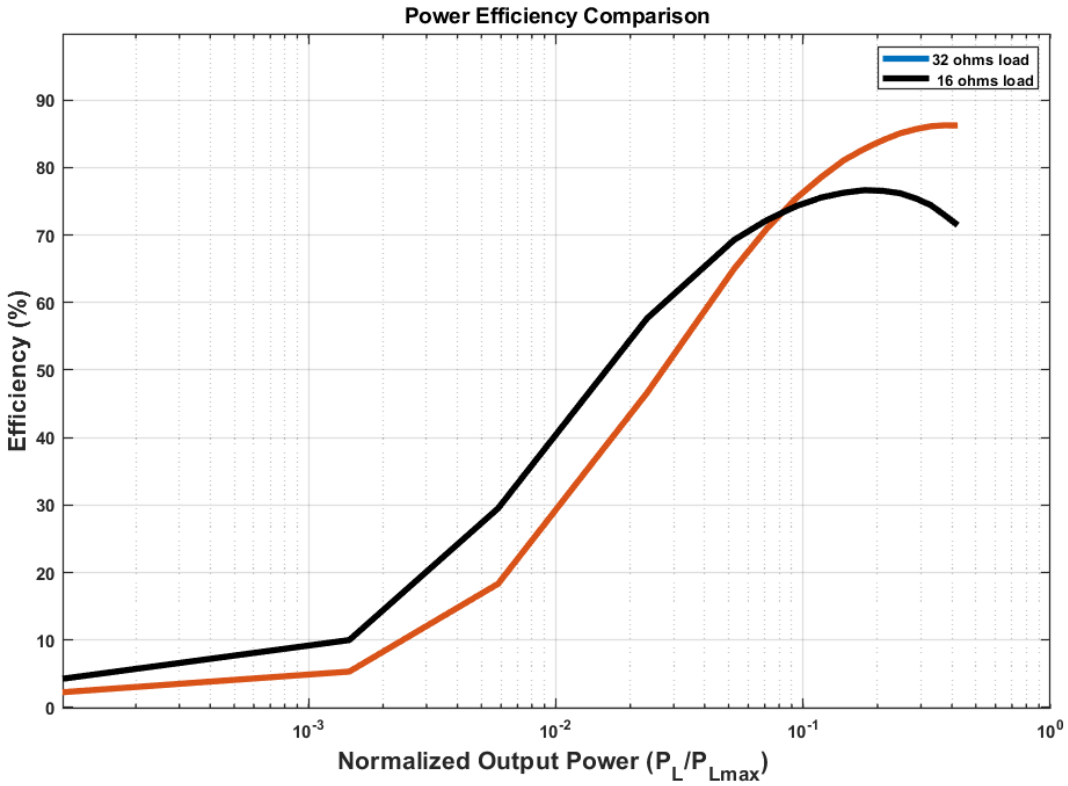


Figure 5.8 Measured power efficiency for 16 and 32 Ω loads

From the plot, it is observed that for the heavier load (i.e., 16Ω), the power efficiency becomes worse than that of the 32Ω load because conductivity losses dominate. The maximum efficiency realized for 32 Ω is about 86.22%.

Figure 5.9 demonstrates the power efficiency improvement by comparing the measurement results to an **ideal** power efficiency for Class-AB and Class-G (4 levels). The plot shows that the power efficiency of this work is superior, particularly for the mid-signal range.

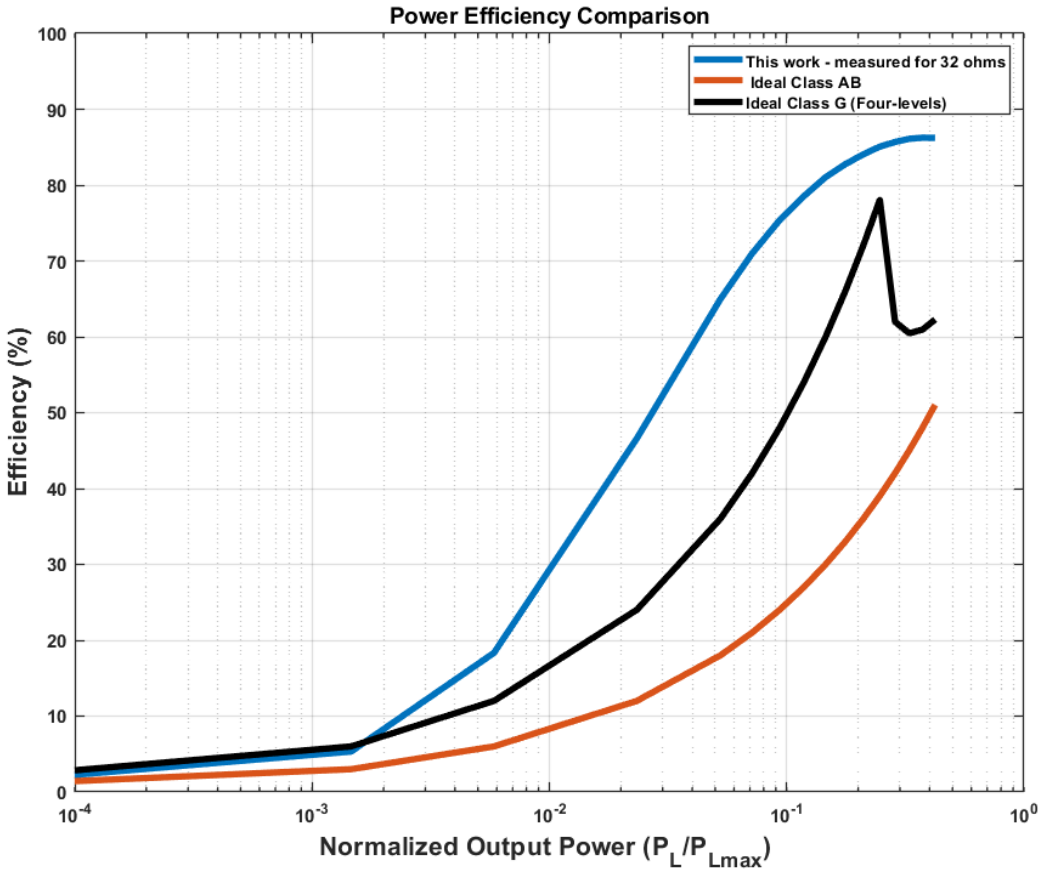


Figure 5.9 Power efficiency comparison

Figure 5.10 shows PSRR results for 500mV$_{PP}$ 217 Hz tone applied at the battery supply and the resulting output, PSRR is measured to be approximately 108dB, which is a little worse than the 110dB simulated value.

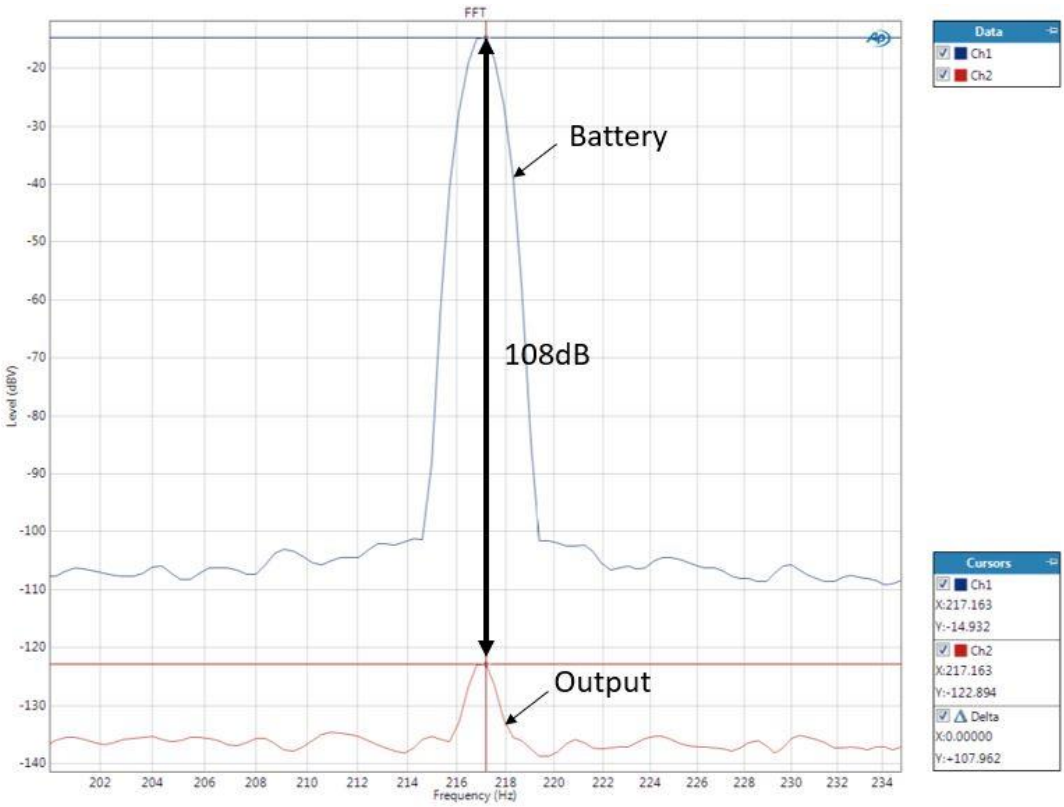


Figure 5.10 PSRR at 217Hz

Similarly, Figures 5.11 and 5.12 demonstrate the PSRR performance at frequency of 1kHz, and 19kHz, respectively. The PSRR degradation at the latter frequency is due to the finite loop bandwidth.

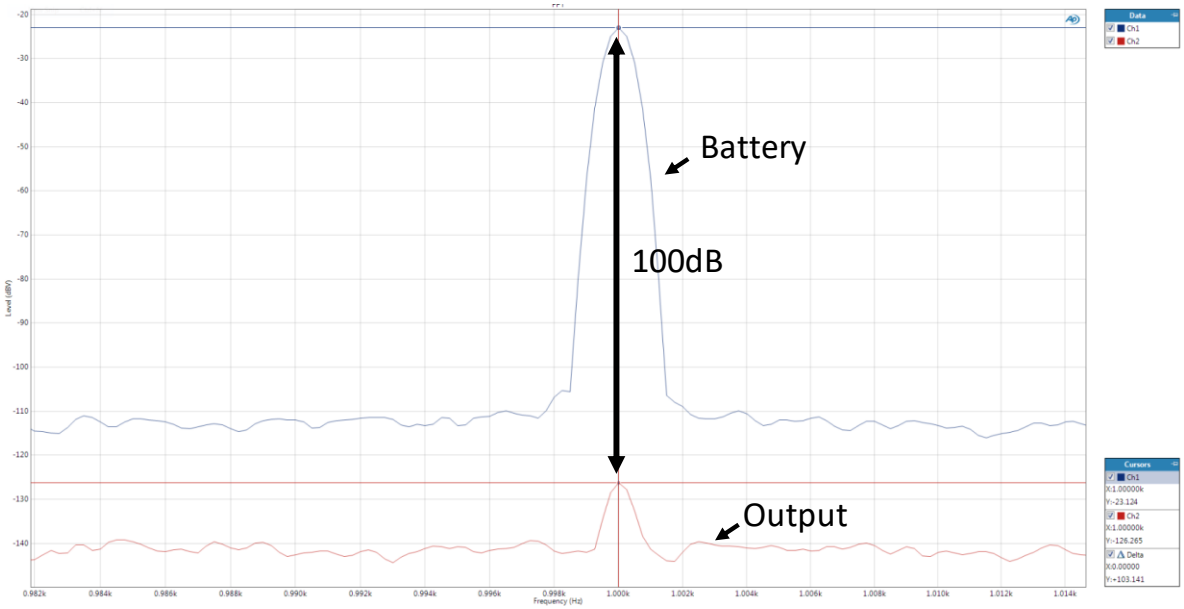


Figure 5.11 PSRR at 1kHz

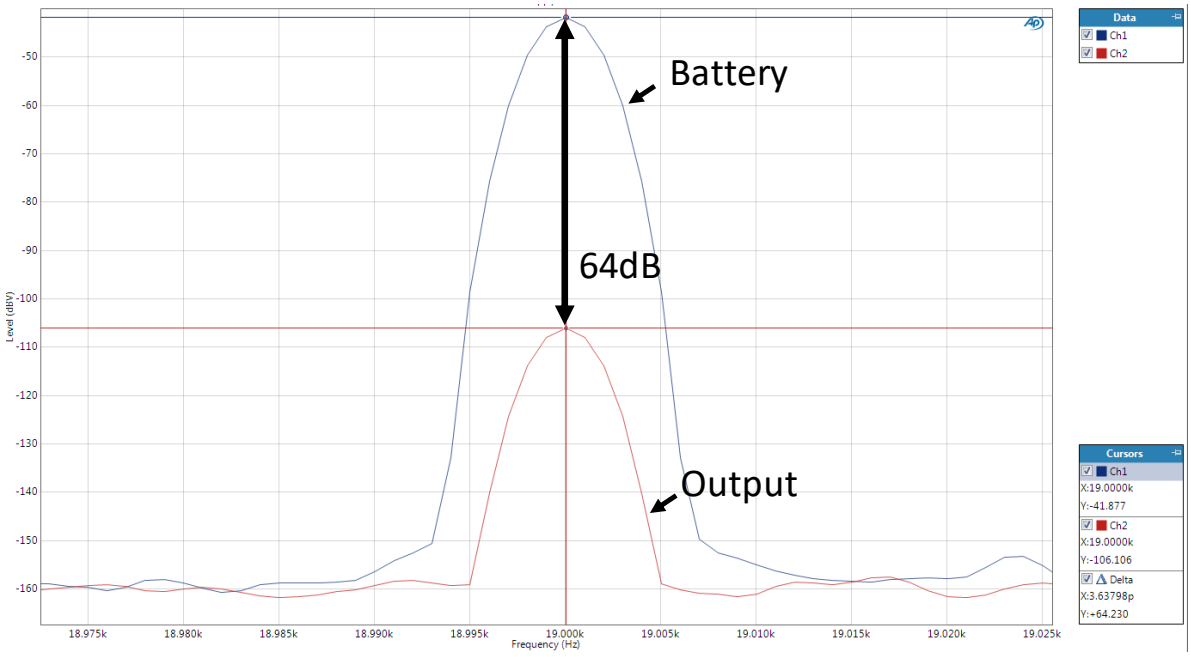


Figure 5.12 PSRR at 19kHz

Table 5.1 summarizes the measured performance as well as comparing with some of the state-of-the-art publications spanning all linear topologies as well switching topologies.

Table 5.1 Performance summary and comparison with the state-of-the-art publications

Parameter	This Work	[7]	[12]	[9]	[10]	[11]	[15]	[6]	[5]	[16]
Process	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	65nm CMOS	0.18µm CMOS	0.25µm CMOS	0.13µm CMOS	40nm CMOS	0.13µm CMOS
Supply [V]	2.95-4.5	2.95-4.5	1.2-3.3	2.65-4.5	±1.4, ±0.35	1.8V	3.6	±1, ±0.65	2.95-4.5	2.3-4.8
Quiescent Current/channel [mA]	1.5	0.6	1.7	1.15	NA	0.866	1.18	1.46	0.84	-
Output Power (16Ω) [mW] (@ 1% THD)	232 (3.7V)	62	210	60	45	62	-	20	82	-
Peak THD+N [dB]	-98.5	-88	-94 (THD only)	-95	-82	-95	-69 (5K, 47Ω)	-84	-84	-80
Dynamic Range (A-weighted) [dB]	108.5	108	-	111	101	108	-	92	100	96
FOM: Peak-to-Quiescent current	113 (3.7)	146	123	75	NA	101	-	34	120	
PSRR [dB]	109	-	-	120	-	130	84	-	110	70
Maximum Load Capacitance [nF]	100	-	-	-		-	-	22	-	
Class	D Current Mode	AB/B	H	G (r =2)	G (r=2)	G (r=2)	D	AB	AB	D
Comments			Sim, Diff out							

The comparison shows that this work achieves the highest output power for a 16Ω load. In addition, the fidelity achieved is better than all linear topologies in terms of the peak THD+N or the Dynamic Range while having very competitive PSRR results.

The quiescent current consumption is a bit higher than some of the previous publications, but it is still lower than that of the Class-H paper [7].

Thanks to the superior maximum output power, this work FOM is within the same range as the rest of the publications.

In summary, the results shown demonstrate superior fidelity, output power, and efficiency when compared to previous publications for both linear and switching topologies.

CHAPTER 6 Summary and Conclusions

This work presents a non-conventional way of realizing high-efficiency high-performance headphone amplifiers. A headphone amplifier is almost always realized using a linear amplifier to achieve superior performance such as THD+N, DR and PSRR, and several techniques are often used to maximize the power efficiency such as using Class-AB (or Class-AB/B) or by combining a linear topology with a supply modulation scheme such as Class-G or Class-H. While these techniques usually work for a low-frequency audio signal, their performance degrades at higher frequencies. In addition, these techniques require precise synchronization between the input signal and the supply-modulating signal to avoid distortion.

In this work, a Class-D topology is used to maximize the power efficiency beyond what linear topologies can achieve. At the same time, a current-sensing technique is used to employ a local feedback to enhance the THD+N and PSRR performance.

A prototype chip is fabricated in 0.18um TowerJazz technology and the measured performance proves a superior power efficiency, THD+N and dynamic range performance to the state-of-the-art publications. The maximum output power achieved is also much larger than any of the pervious publications. While the realized FOM is not as good as it was initially perceived in the design phase, it still stands very competitive compared to previous papers.

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