UNIVERSITY OF CALIFORNIA,
IRVINE

An Integrated Solution to Tinnitus Treatment

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

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2024

DEDICATION

To my parents.

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ACKNOWLEDGMENTS

I would like to express my deepest gratitude to those who have played a crucial role in the completion of this Ph.D. thesis. Their support, guidance, and encouragement have been invaluable throughout this challenging yet rewarding journey.

First and foremost, I extend my heartfelt thanks to my advisor, Michael Green for his unwavering support, expertise, and mentorship. His insightful feedback and encouragement have been instrumental in shaping the direction of this research.

I would like to acknowledge professor Hamid Djalilian and the donor for their financial support, which made this research possible. The funding provided not only facilitated the acquisition of essential resources but also allowed me the freedom to delve deeper into the subject matter.

I would like to acknowledge professor Fan-Gang Zeng, Rabih Nassif for their comments and suggestions during the numerous demo events, which guide this research toward the right direction.

I am grateful to the members of my dissertation committee, professor Ozdal Boyraz who offered me the chance worked as his teaching assistant during my second year of the Ph.D. study. Professor Hamidreza Aghasi who helped me several times with the Cadence, ADS license issues.

A special thanks to my Ph.D. colleagues Behnam Moradi Shahrbabak who worked on the supply chip design and all measurement setup, Pooya Khosravi who worked on the user interface design, Alireza Nikzamir who worked on the coil design. Hang Zhao who introduced me to professor Michael Green. Their shared enthusiasm have made this academic journey more enriching.

Last but not least, I owe a debt of gratitude to my family and friends. Their unwavering encouragement, understanding, and patience have been my pillars of strength. Their belief in me has been a constant motivation to persevere through the challenges.

In conclusion, the completion of this Ph.D. thesis would not have been possible without the support of these wonderful individuals and institutions. Thank you all for being an integral part of this academic endeavor.

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ABSTRACT OF THE DISSERTATION

An Integrated Solution to Tinnitus Treatment

By

Yaoyu Cao

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine, 2024

Professor Michael Green, Chair

This thesis focuses on the development of a novel approach for treating tinnitus, a prevalent condition marked by the perception of sound without an external source, affecting 10-15% of the global population. Traditional treatments are often ineffective for patients with severe tinnitus, prompting exploration into new methods such as electrical stimulation of inner ear tissue. The thesis presents the design and measurements of an miniaturized multi-chip module (MCM) solution intended for delivering well-defined, charge-balanced current stimuli directly to the inner ear. The MCM will be implemented in the inner-ear of patients with severe tinnitus.

Detailed descriptions of the MCM solution are provided, this solution contains four key elements: a laminate substrate, an antenna, a core chip and a supply chip. The most critical parts of this MCM solution are the two chips, the design of which is the main part of this thesis, both chips were designed and fabricated using the TSMC180nm BCD G2 process. This MCM solution is tailored to accommodate the high-impedance nature of inner ear tissue and to ensure safe and effective stimulation. Overall, this work represents a significant advancement in the development of innovative solutions for tinnitus treatment, offering potential benefits for patients suffering from this challenging condition.

The thesis concludes with measurements conducted to assess the performance of the chips

designed in generating current stimulation waveforms and maintaining charge balance. The measurements were conducted using two types of loads: a human inner-ear RC model circuit and pig-ear tissue. The results demonstrate the chip's ability to produce arbitrary current stimulation waveforms with tunable amplitudes, number of consecutive cycles, and charge-balance times.

Chapter 1

Introduction

1.1 What is tinnitus and tinnitus treatment methods

Tinnitus, a condition characterized by the perception of sound in the absence of an external source, affects 10-15% of the population worldwide [4] [5]. The major risk factors of tinnitus include hearing loss, abnormal plastic changes in the auditory network, and depression. Despite its prevalence, severe tinnitus can be very challenging to treat. A promising approach involves the use of electrical stimulation to the inner ear tissue with carefully defined current signals of varying frequencies, amplitudes, and wave shapes.

Research has shown that stimulation current amplitudes of up to 1.25 mA are required for effective tinnitus treatment [6], an example of treatment in the lab as shown in Fig. 1.1, where the patient sit on the exam chair with her right ear being stimulated. Currently, this treatment requires the use of large, commercially available equipment that is typically only found in hospitals or research institutes. A more practical solution would be the development of a fully implantable multi-chip module that can deliver well-defined, charge-balanced current stimulus directly to the inner-ear tissue, which is the research topic of the work described in this dissertation.

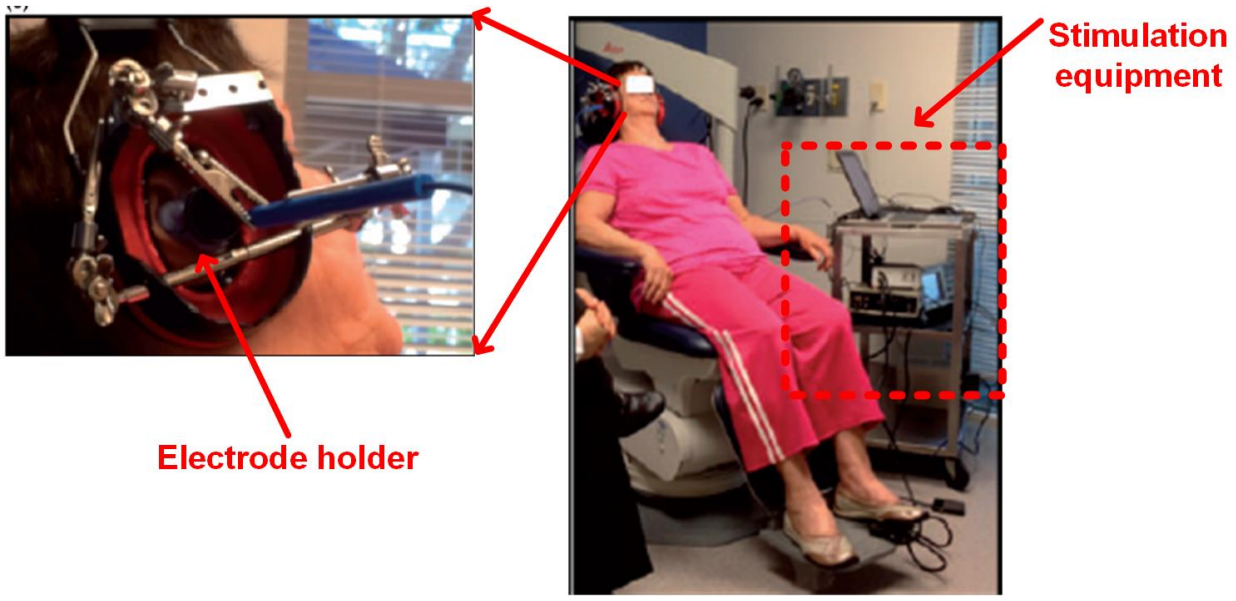


Figure 1.1: Example of treatment.

1.2 Cochlea implants and the state-of-art cochlea technology

A cochlear implant stands as a marvel of modern medical technology, meticulously engineered to provide a lifeline of sound to those navigating the challenges of profound deafness or severe hearing impairment. This sophisticated system is comprised of two integral components: an external device delicately positioned behind the ear, and a second device meticulously implanted beneath the skin, as shown in Fig. 1.2 [1]. These components work in tandem, harnessing cutting-edge electronics and surgical precision to restore a vital sense of sound to individuals who have long grappled with the silence of their world.

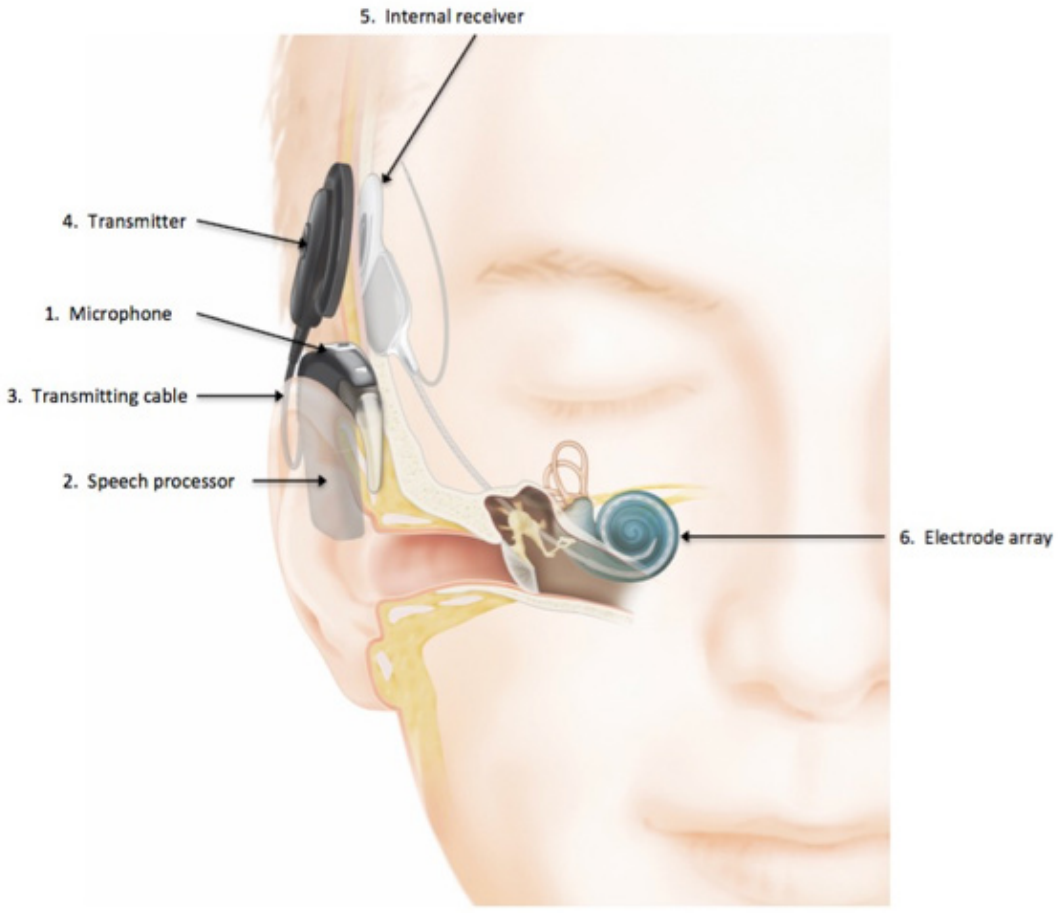


Figure 1.2: Cochlear implant. (Image courtesy of Cochlear[1])

A cochlear implant system is comprised of several key components, including a microphone designed to capture sound from the surroundings. A speech processor is then responsible for selecting and organizing the sounds acquired by the microphone, which is usually designed with digital-signal process techniques. The transmitter wirelessly transmits the signals generated from the speech processor to the implanted internal receiver. The internal receiver receives the signals and transforms them into electric impulses. An electrode array, consisting of a cluster of electrodes, gathers these impulses from the internal receiver and delivers them to various segments of the auditory nerve.

Figure 1.3: Off-ear external device. (Image courtesy of Cochlear [1])

The surgical procedure places the internal device permanently beneath the skin, ensuring that it remains in position. Subsequent to the surgery, the external device is tailored to the patient through programming. This external device is worn akin to a hearing aid, with the individual turning it on in the morning and turning it off before bedtime. Typically, the external device takes the form of a fitted module situated behind the ear. Alternatively, for very young children, a body-worn external device may be employed. Some modern external devices are designed to be entirely positioned on the head, eliminating the necessity for any

component on or in the ear as shown in Fig. 1.3 [1].

Fig. 1.4 shows a commercial cochlear product designed and manufactured by Cochlear. Ltd, where the internal device is the Nucleus implant as shown in the figure and the external device is either the Nucleus 8 sound processor behind-the-ear or the Nucleus Kanso 2 sound processor off-the-ear [1].

Figure 1.4: Nucleus system. (Image courtesy of Cochlear [1])

The dimensions of the internal device are shown in Fig. 1.5. Its insertion into the inner ear of the patient involves a series of steps: Initially, under general anesthesia, the surgeon makes a small incision behind the ear, through which the implant is positioned beneath the skin, and the electrode is introduced into the inner ear. Subsequently, the surgical team conducts tests to gauge the patient's response to the implant. Closure of the incision, often achieved with disposable stitches, concludes the procedure, which typically lasts around two hours per ear. Post-surgery, the patient is transported to the recovery area until the anesthesia subsides. Once the medical team is satisfied with the patient's recovery, the patient is allowed to return

home. Typically, three to four weeks after the surgery, the doctor informs the patient that the implant can be activated and synchronized with a sound processor [1].

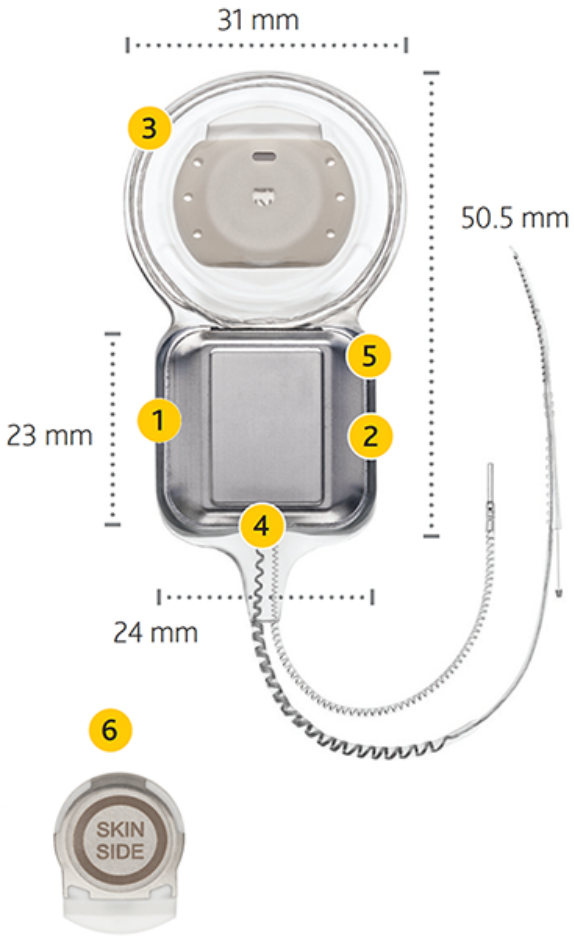


Figure 1.5: Implant size. (Image courtesy of Cochlear [1])

1.3 Drawbacks of cochlear implants and the proposed miniaturized MCM solution

Due to the relative large dimensions of the above mentioned cochlear implant, the internal device has to be implanted under the skull bone, which is considered highly invasive. Along with its side effects, such as the possibility of infection, the cochlear implant treatment is considered risky and not recommended for certain patients. Inspired by the cochlear implant, we present a inner-ear implantable device designed specifically for tinnitus treatment as shown in Fig. 1.6.

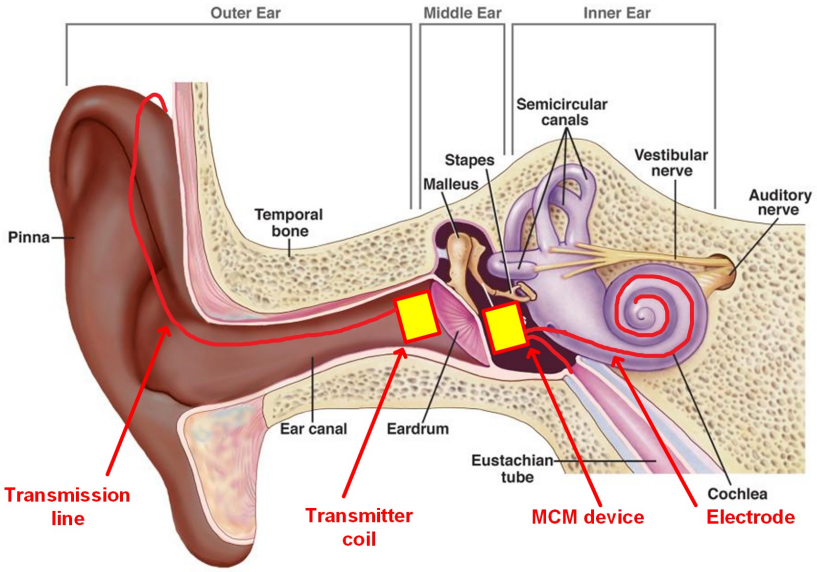


Figure 1.6: Proposed MCM. (Image courtesy of NIH/NIDCD [2])

Unlike the traditional cochlear implant that is placed under the skull bone, the proposed MCM internal device is placed in the tympanic cavity inside the inner ear. The surgery to implant the MCM internal device typically takes less than 25 minutes, which is low-cost, minimally invasive, and low risk for patients. The wearable transmitter coil is part of the external device, which sits in the outer ear.

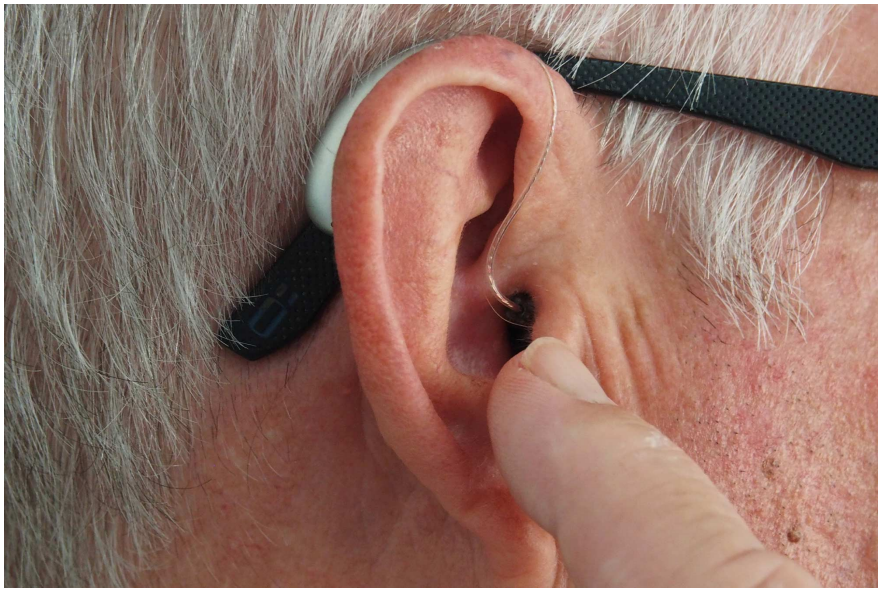


Figure 1.7: Behind-the-ear transmitter(Image courtesy of Tinnitus Hearing Experts [3])

The transmitter coil is connected to the behind-the-ear device through a thin transmission line as shown in Fig. 1.7. During treatment, the transmitter sends energy and modulated data to the transmitting coil through the transmission line, with another receiving coil built inside the MCM device wirelessly receiving the energy and data. The MCM device then generates stimulus that is delivered to the cochlea through the electrode.

Chapter 2

Proposed Miniaturized MCM Solution

2.1 Introduction of inner-ear tissue model under biphasic stimulation

In order to effectively and efficiently design the MCM device used to deliver the required electrical stimulation current into the inner-ear tissue, having an accurate but not overly complicated electrical model that can be used to represent the electrical properties of the inner-ear tissue is critical to success. However, this can be a complex task. A comprehensive study and summary of the effects of electrical stimulation on neural tissue is reported in [7].

The most basic and commonly used method to stimulate the inner-ear tissue is by utilizing biphasic pulse-shape current stimulation signals, as shown in Fig. 2.1, majority of the electrical models are derived based on this stimulation method. Each cycle of the stimulation consists of two phases: first a negative stimulation phase, followed by a positive stimulation phase. Ideally, the amplitude and duration of these two phases should be strictly matched to ensure there is no net charge delivered to the tissue. However, practical stimulation equipment often exhibits some mismatches in these two phases. The charge-balance period, as shown in Fig. 2.1, is used to eliminate the residual charge caused by these mismatches.

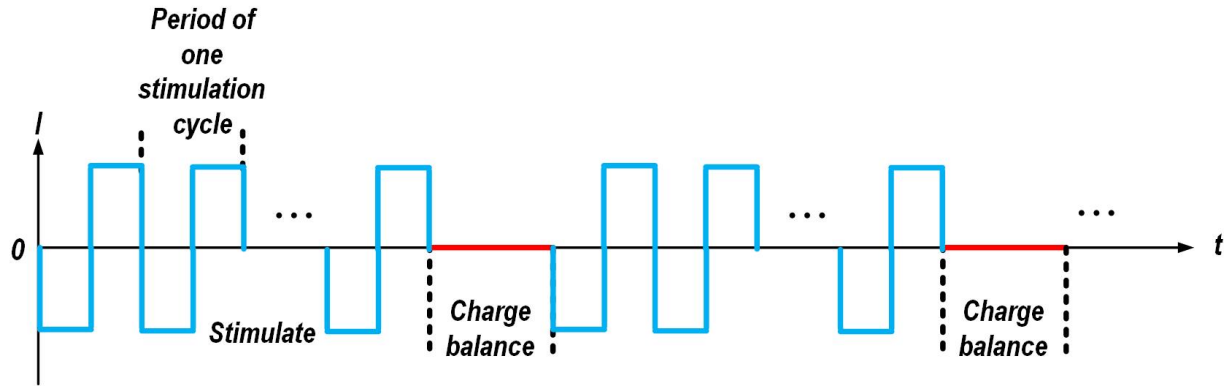


Figure 2.1: Biphasic current waveform

The current stimulation signals are delivered to the inner tissue through electrodes. When the electrodes are implanted inside the inner-ear tissue, the electrode/tissue interface forms a

capacitor, where the electrodes act as the two plates of the capacitor and the inner-ear tissue (electrolyte) serves as the dielectric material [8]. The resistance of the inner-ear tissue, along with resistance from wires and contacts of the electrodes, is modeled as spreading resistance, R_s. Current flow resulting from oxidation-reduction reactions at the electrode/electrolyte interface is represented by charge-transfer resistance, R_{ct}. The limitations of ion movement in the electrolyte are represented by the Warburg impedance [9]. Collectively, the charge-transfer resistance and Warburg impedance are combined as a Faradaic impedance which is represented by R_w [10]. These three components form an electrical model which is commonly referred to as the Randles R-C-R model as shown in Fig. 2.2 [7].

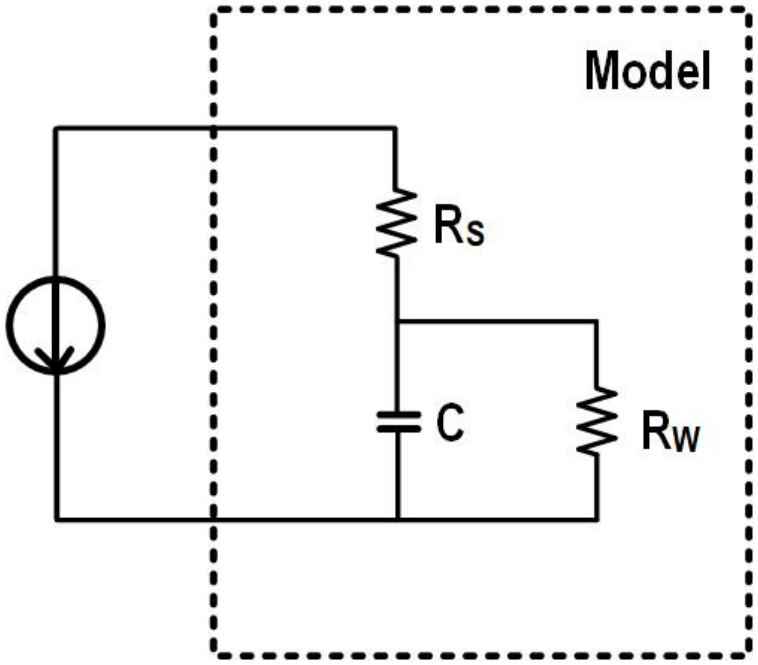


Figure 2.2: R-C-R model.

Another commonly used model for the electrode-tissue interface in a stimulator is the series R-C model, as depicted in Fig. 2.3 [11]. In contrast to the R-C-R model illustrated in Fig. 2.2, the collective impact of spreading resistance, R_s, charge-transfer resistance, R_{ct}, and the Warburg impedance is represented by a single resistor, R. The capacitance formed between the metal electrodes and the electrolyte of the inner-ear tissue is captured by a single capacitor, C. This simplified model, copmared to the R-C-R model shown in Fig. 2.2,

finds more frequent use in the circuit design stage. This preference stems from its ease of convergence and reduced simulation time during transient simulations when designing circuits using modern CAD software.

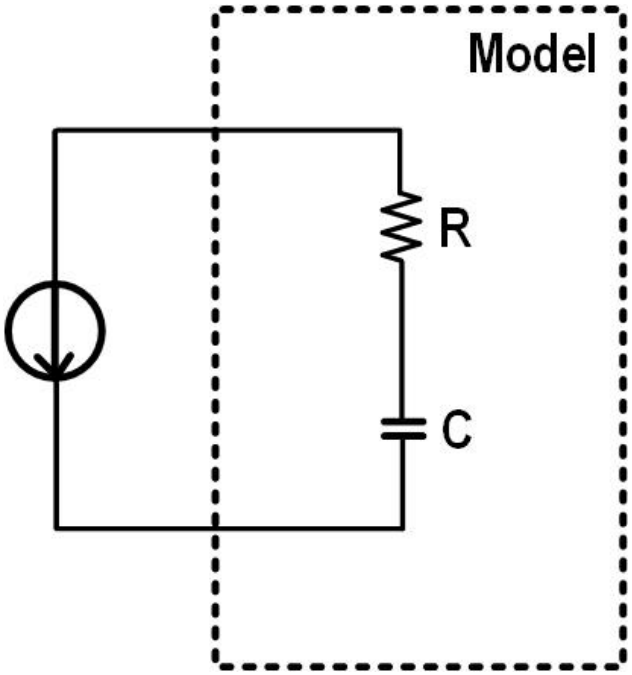


Figure 2.3: Series RC model.

2.2 Miniaturized MCM solution in detail

A transmitter that sends the waveform data to the module, which does not need to be implantable, can be realized using commercially available chips and development boards. On the other hand, an implantable multi-chip module must be powered wirelessly through an implantable receiving coil that is coupled with an external transmitting coil, where the receiving coil receives energy as well as modulated data that encodes the waveshape, frequency, and amplitude of the desired current stimulus.

In this thesis, we use the simplified inner-ear electrical model suitable for our application [11], as illustrated in Fig. 2.4, which consists of the series connection of a resistor and capacitor. The lowest audio frequency required for the stimulation current is 150Hz, at which, the impedance magnitude of this model is approximately 11kΩ.

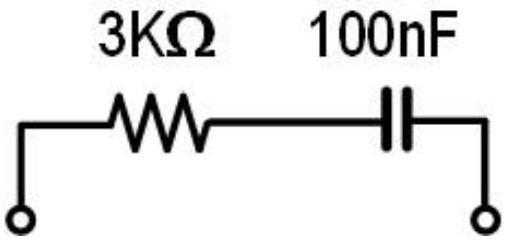


Figure 2.4: Inner ear RC model.

This requires a 20-V power supply to deliver the necessary net current amplitude of 1.25mA, while also allowing for some extra voltage headroom to ensure proper performance across process, voltage, and temperature (PVT) conditions. Therefore, an advanced high-voltage bipolar-CMOS-DMOS (BCD) process was selected for this work, the BCD process integrates the bipolar transistors for high-performance analog design, low-voltage CMOS transistors for digital deisng, as well as the high-voltage DMOS transistors for high-voltage circuit.

A visual representation of the multi-chip module is shown in Fig. 2.5. The module consists of a laminate on which is mounted a core chip, a dc-to-dc voltage converter chip, a rectifier, a

receiving coil, and some off-chip components such as capacitors used in conjunction with the dc-to-dc converter. In order to be implantable in the patient's inner ear, the entire module must have dimensions no greater than approximately 4.5 mm in each dimension.

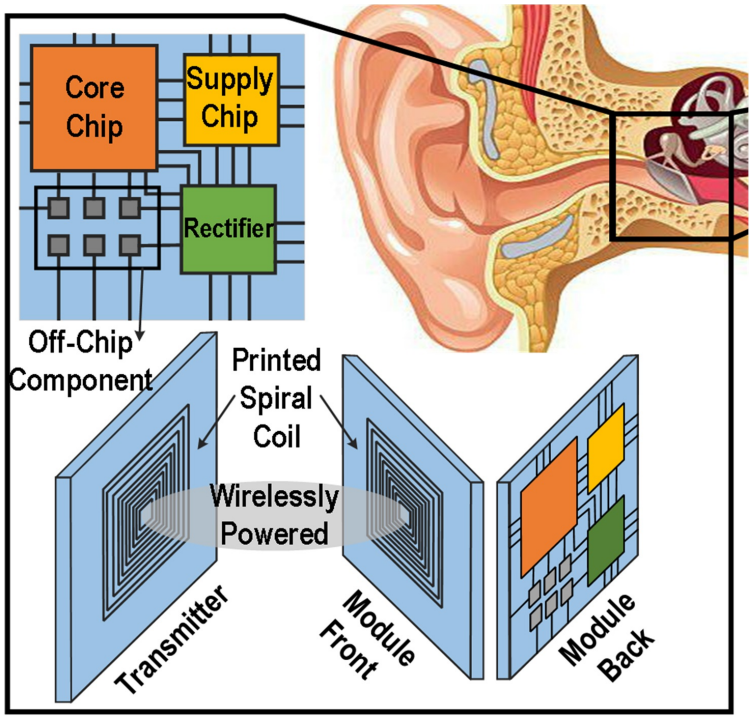


Figure 2.5: Multi chip module.

Due to the presence of random mismatches in any integrated circuit, the negative and positive cycles of the stimulation will never be perfectly symmetrical and there will be some net charge that slowly accumulates in the inner-ear tissue due to this imperfection. It is important to ensure that any such accumulated charge be kept balanced periodically to avoid damage to the inner ear. Several common charge-balance methods are employed in electronic stimulation circuits to manage charge imbalances effectively. One common method for charge balancing is to incorporate feedback control mechanisms to automatically monitor and adjust the delivered charge, where an adjustment in real time ensures that the system maintains charge balance during operation [12]; however, this method increases the system complexity significantly, which translates to higher total power consumption as well as larger chip area. In this thesis, we utilize one simple solution to balance the charge, which is il-

lustrated in Fig. 2.6, during the charge-balance operation, the two electrodes connected to the ear tissue are shorted together by the device in the chip, which will remove the residue charges stored in the tissue. A novel circuit is proposed to accomplish this charge-balance operation, this circuit can be implemented with the widely-used TSMC 180nm BCD process.

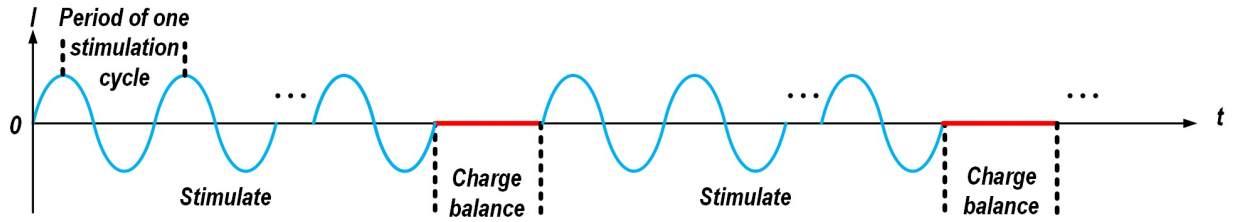


Figure 2.6: Charge balanced waveform.

To ensure that the device can be used to treat all patients with different severity levels of tinnitus, both the number of consecutive stimulation cycles and the duration of the charge balance time should be adjustable. The number of consecutive cycles can be set between 7 and 2047, the audio stimulation frequency can be set between 150 Hz and 20 kHz, and the duration of the charge balance time can be set between 16 ms and 1.28 s. These specifications are based on the unpublished data collected from the medical experiments done by a research group at University of California, Irvine.

2.3 System Diagram

The system block-level diagram is shown in Fig. 2.7, where the circuit blocks in the red box represent the circuit realization of the core chip and the circuit blocks in the green box represent the circuit realization of the supply chip.

The operation of the core chip is described as follows: A digital control sequence generated by the transmitter is modulated onto the 13.56-MHz ac signal that facilitates energy transfer between the two coils. The BPSK demodulator demodulates the signal from the coil, the

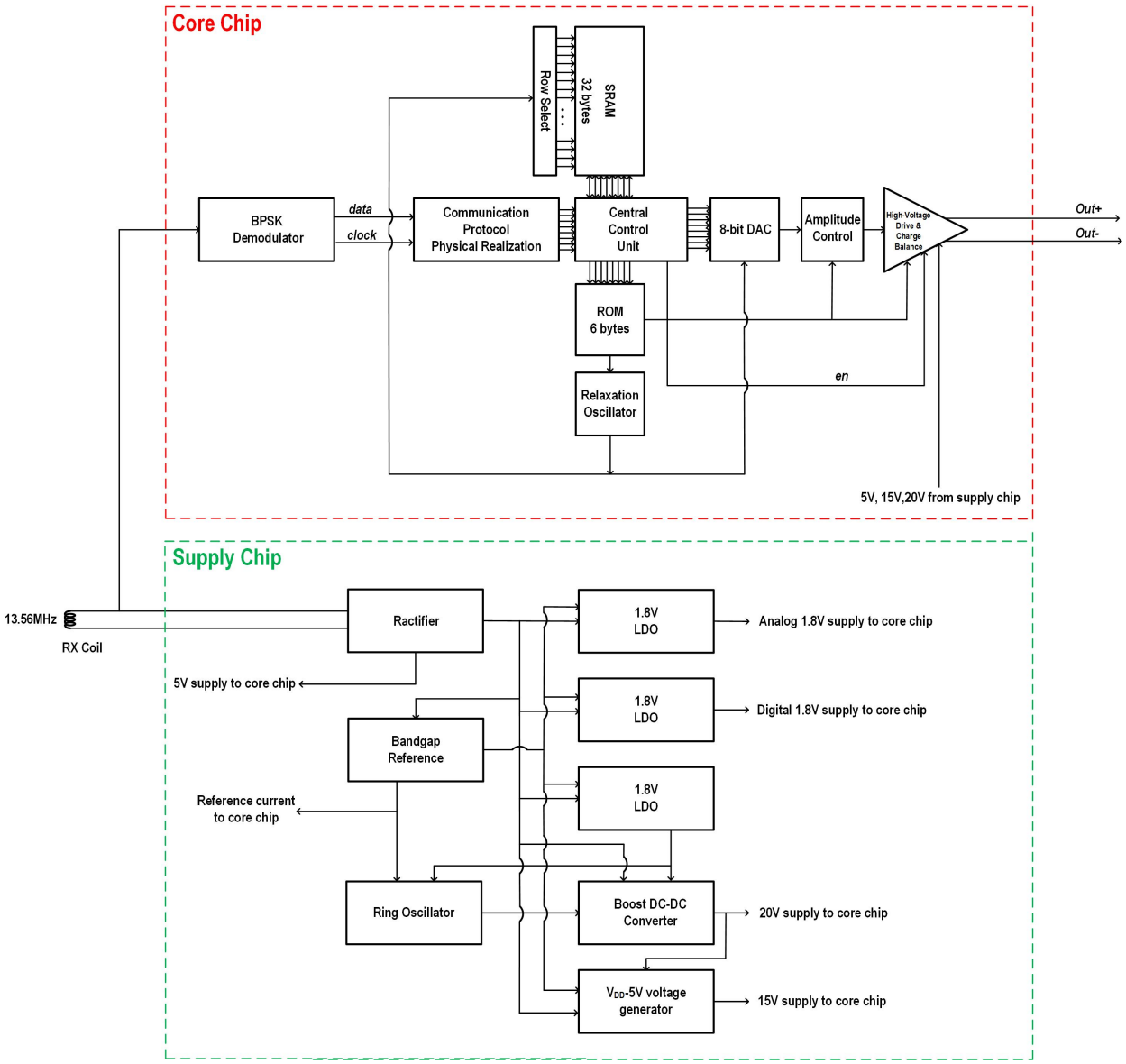


Figure 2.7: System diagram.

resulting digital data is then sent to the communication protocol physical realization block and the central control unit for further processing. Upon initiation of power transfer, a 12-bit start sequence is transmitted to initiate a handshake with the receiving core chip. Subsequently, the data specifying the signal parameters is transferred into the core chip's static random-access memory (SRAM) and read-only memory (ROM). The process is completed with the transmission of another 12-bit end sequence indicating the end of data transfer, after which the circuit begins conducting the current stimulus differentially to output nodes

out+ and *out-*, which are connected to the stimulation electrodes. During the surgery, one electrode is connected to the round window of the inner ear and the other is connected to the bone surface of the cochlea.

The nominal operation of the core chip requires two 1.8-V supplies - one for the digital circuits and the other for the analog circuits. The core chip also requires a 5-μA input reference current for the BPSK demodulator, relaxation oscillator, and digital-to-analog converter (DAC). The 5-V, 15-V, and 20-V high voltages are also required in the core chip by the high-voltage drive and charge balance block. The generation of these high voltages requires a separate supply chip, which contains several stages of noisy large-swing switch-capacitor circuits driven by high-amplitude clock signals. To isolate the switching noise from core chip, all these supply-generation blocks are built in the supply chip.

Chapter 3

Design of Core Chip

3.1 Core chip overview

This chapter describes the detailed circuit implementation of the key circuit blocks in the core chipas shown in Fig. 3.1. This chip is fabricated with the TSMC180nm BCD G2 process, which includes low-voltage transistors as well as high-voltage DMOS transistors to realize the high-voltage operation. The low-voltage 1.8V and 5V NMOS and PMOS transistors are used to design the low-voltage circuit blocks which include the BPSK demodulator, the communication protocol physical realization, the SRAM & ROM and the associated circuits, the relaxation oscillator, the digital-to analog converter, and the amplitude control circuit. The 20V high-voltage transistors are used to realize the high-voltage drive and charge-balance circuit.

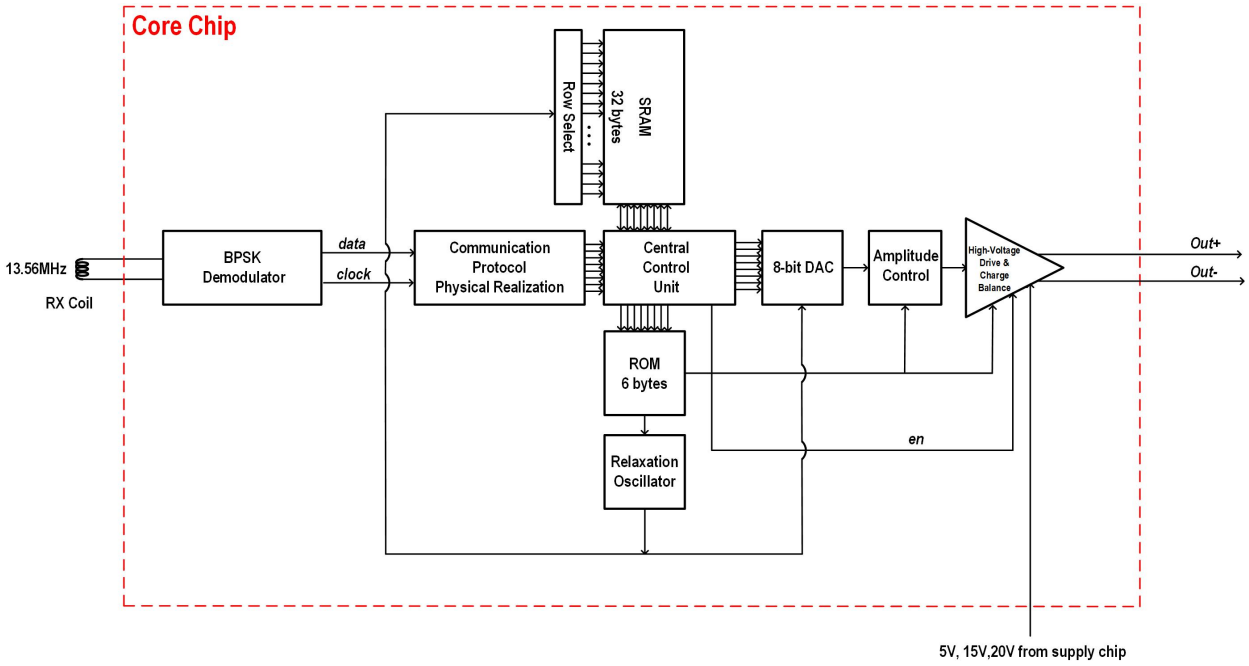


Figure 3.1: Block diagram of core chip.

3.2 Design of the BPSK de-modulator and clock recovery circuit

3.2.1 BPSK demodulator

As we explained in Chapter 1, the power and data must both be transferred wirelessly through a pair of magnetically coupled coils. We choose BPSK modulation for data transfer for the following two reasons: First, the coupling coefficient of the coupled coils can vary due to patients' body movements, which translates to amplitude variation; since, BPSK encoding is independent of amplitude, this modulation ensures data transfer reliability. Second, since both power and data must be transferred through the same coil, amplitude modulation may result in lower power transfer efficiency. Since BPSK modulation utilizes a constant RF amplitude, power transfer efficiency is maintained. Third, a narrow-band signal is desired because of the limited bandwidth of the wireless coupled coils due to its high quality factor. In this design, the carrier frequency is chosen to be 13.56MHz with the unit interval chosen to be 128 RF cycles, i.e., 9.44 μs, which corresponds to a data rate of 105.938 kb/s. The estimation of the bandwidth the BPSK signal takes can be calculated with Eq. 3.1 [13]. The fractional bandwidth is about 1.6%.

$$BW = \frac{2}{T_b} = 211.86\text{kHz} \tag{3.1}$$

The BPSK modulator (on the transmitter side) can be realized with a commercially available FPGA board. This section focuses on the most challenging part, namely, the on-chip BPSK demodulator. With the package form factor limitation, we cannot have a crystal oscillator generating a local reference clock; thus, the BPSK demodulator needs to be designed without

using any external clock reference. With the above mentioned considerations, a special topology of the on-chip BPSK demodulator is selected as shown in Fig. 3.2 [14].

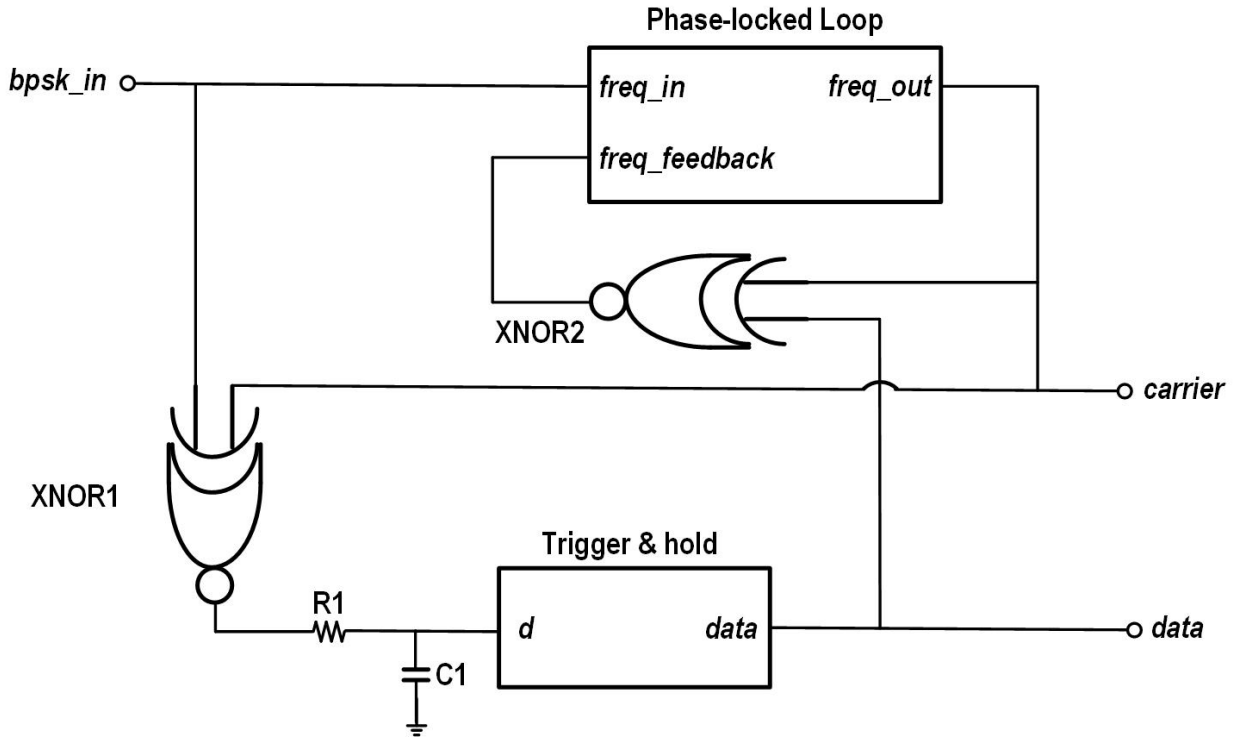


Figure 3.2: Block diagram of BPSK demodulator.

The working principle of this circuit is described as follows. In the absence of input data transitions, in steady state, the phase-locked loop (PLL) shown in Fig. 3.2 maintains lock between the *bpsk_in* and $freq\_feedback$ inputs. Under this condition the output of XNOR1 is fixed at either digital high or low. Whenever there is a sudden 180° phase shift in the input *bpsk_in* signal, at first the PLL output $freq\_out$ continues generating the previously locked carrier without any phase change, due to the long response time as designed in the phase-locked loop, the output of XNOR1 changes its state from either high to low, or low to high. This transition is then applied to the trigger & hold circuit, shown in detail in Fig. 3.3. The output of this trigger & hold circuit is the demodulated data.

In Fig. 3.3, the glitch generator generates a short positive pulse (about 20ns) in response to either a rising or falling edge at its input. The upper and lower threshold voltage of the

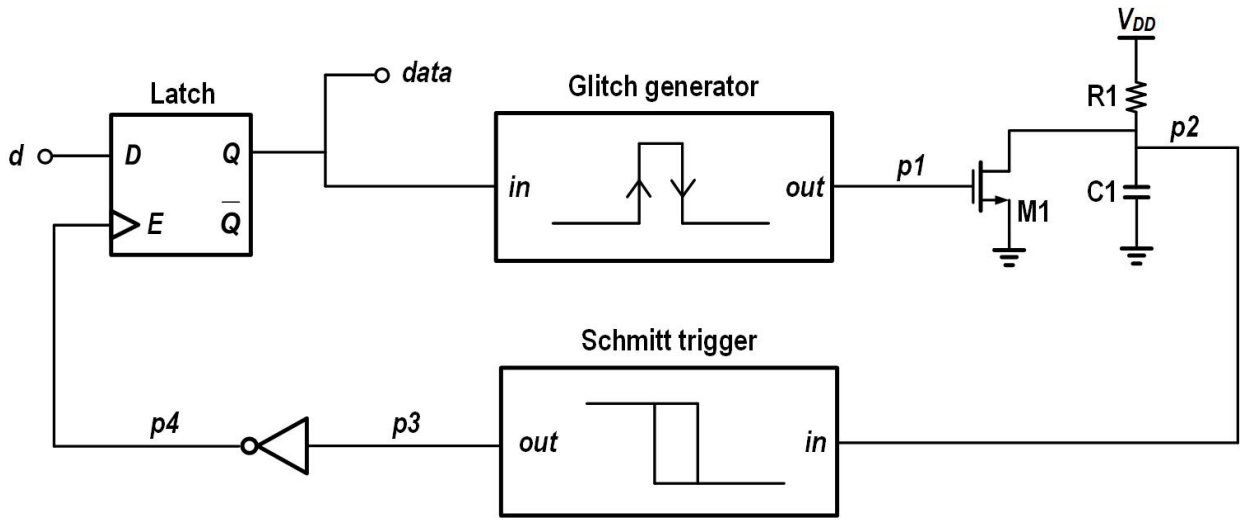


Figure 3.3: Trigger & hold.

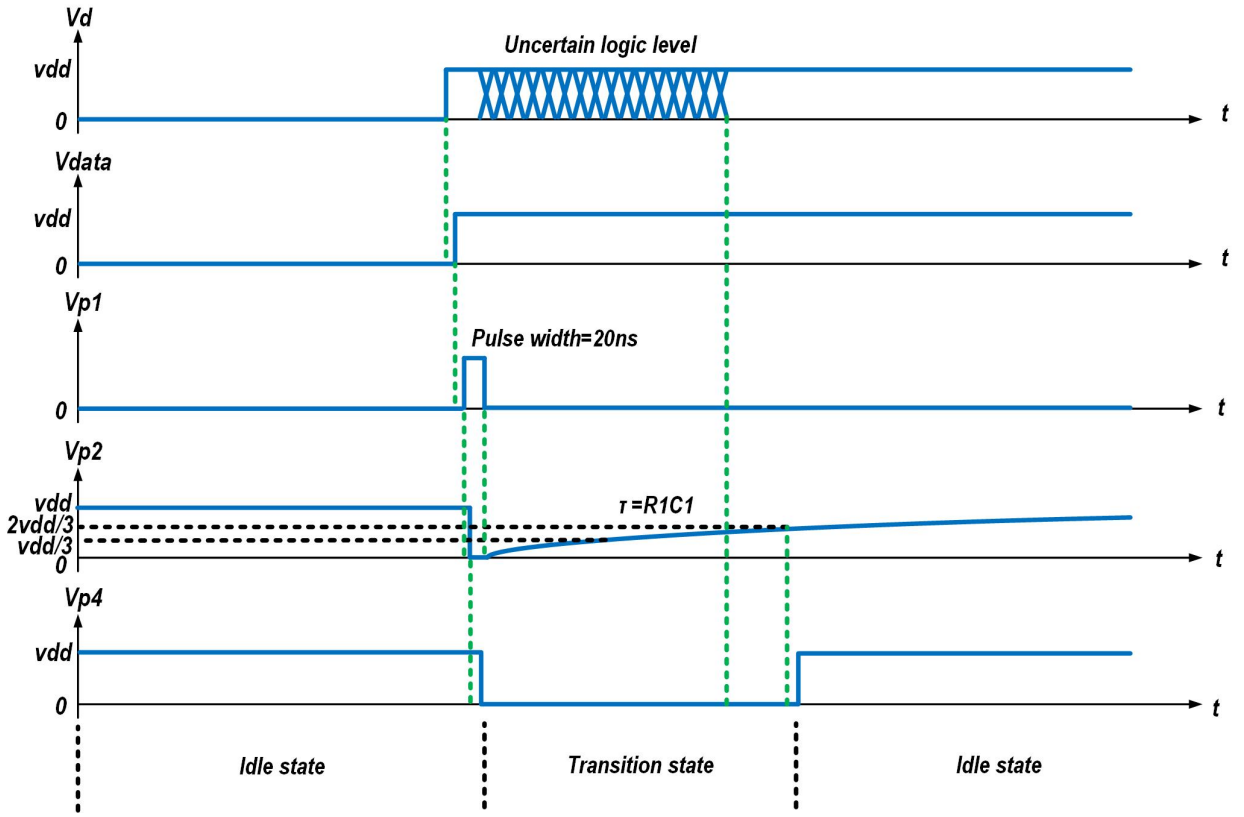


Figure 3.4: Trigger & hold waveform.

Schmitt trigger is $2V_{DD}/3$ and $V_{DD}/3$, respectively. In Fig. 3.2, when there is no 180° phase shift in the input *bpsk_in* signal (we define this condition as the idle state), the output of the glitch generator in Fig. 3.3 is low, transistor M1 is turned off, and signals $p2$ and $p4$ are both

high. Thus the latch D input is passed to its Q output at this idle state. For the opposite scenario, in Fig. 3.2, when there is a 180-degree phase shift in the input *bpsk_in* signal (we define this condition as the transition state), this phase shift (rising or falling edge of the signal) is passed to the input of the glitch generator in Fig. 3.3, the glitch generator generates a 20ns short pulse and momentarily turns on transistor M1 to fully discharge the capacitor C1. After this instant, capacitor C1 will be recharged through resistor R1 with a time constant equal to R1C1, and the voltage on node $p2$ is less than the threshold voltage of the Schmitt trigger for about 3.3 μs (duration of 45 RF cycles of the BPSK signal), during which, the PLL is in the re-acquire-lock process, the logic level of signal d is uncertain; however, the latch locks its Q output until the PLL once again reaches its steady-state locked condition. The voltage waveforms at each node of Fig. 3.3 are shown in Fig. 3.4.

The PLL shown in Fig. 3.5 is based on the classical Type II structure with a charge-pump. The purpose of this PLL is to lock the carrier signal at the 13.56MHz carrier frequency. The loop filter consisting of components R1, C1, C2 is designed such that this PLL is stable over all PVT conditions. In this design, the value of capacitor C1 is 1.67pF, the value of capacitor C2 is 100fF, the value of resistor R1 is 40kΩ. Based on the behavioral-model simulation, the PLL contains a real pole at -39.1MHz, a pair of complex poles at -416.8kHz$\pm$j399kHz, and a zero at -395.4kHz, and has jitter bandwidth of about 1.49MHz. The phase margin of this PLL is about 65°, which also ensures a sufficient delay between an input phase transition and the PLL output so that $freq\_out$ will maintain its previous phase after the sudden 180°phase shift in the $freq\_in$ signal.

Detailed schematics of the phase-frequency detector and charge pump are shown in Fig. 3.6 and Fig. 3.7, respectively. The reference current of the charge pump is set to 5μA, which is derived from the bandgap circuit of the supply chip.

The schematic of the current-starved ring oscillator is shown in Fig. 3.8. Transistor M1 converts its gate input voltage to current, Its frequency tuning range can cover 10MHz to

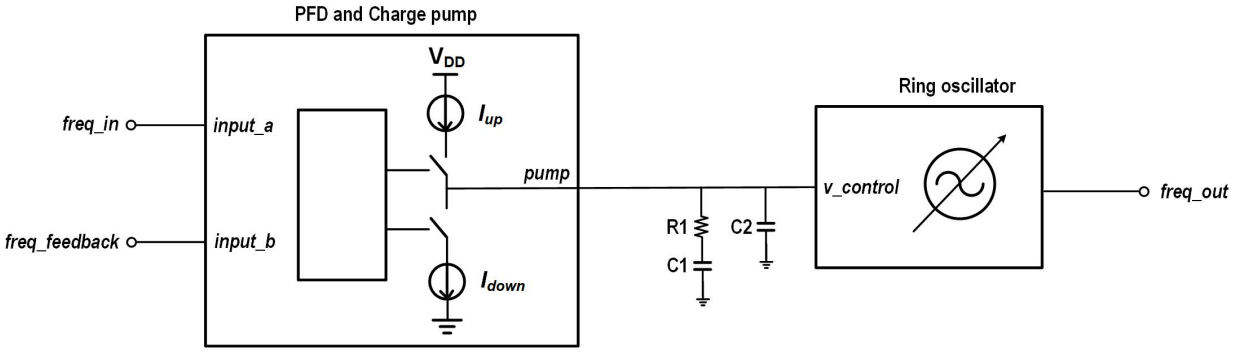


Figure 3.5: Phase-locked loop.

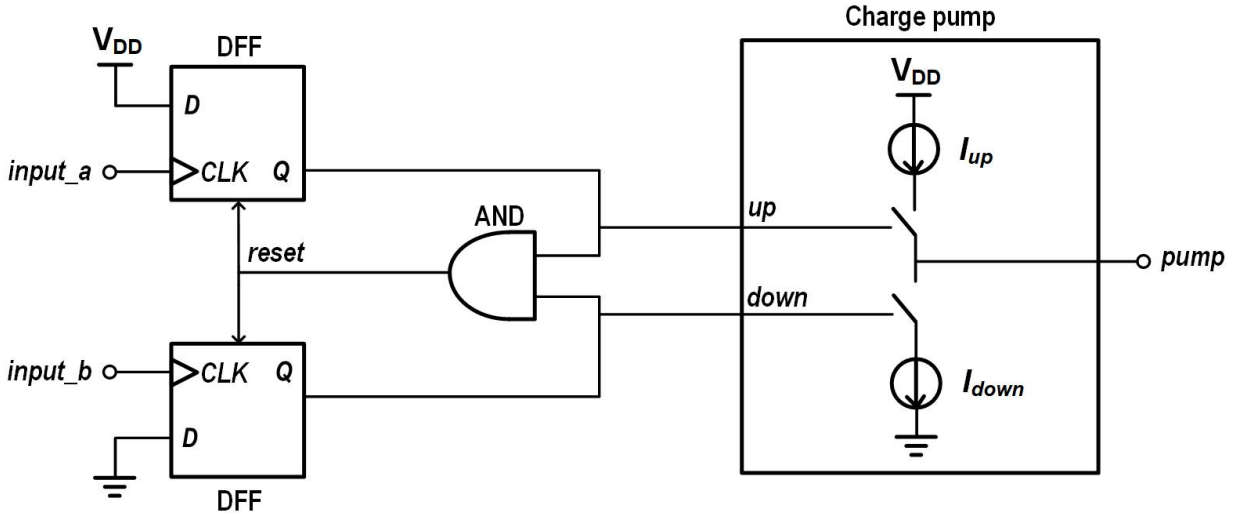


Figure 3.6: Phase-frequency detector.

16MHz over process, voltage, temperature (PVT) variations.

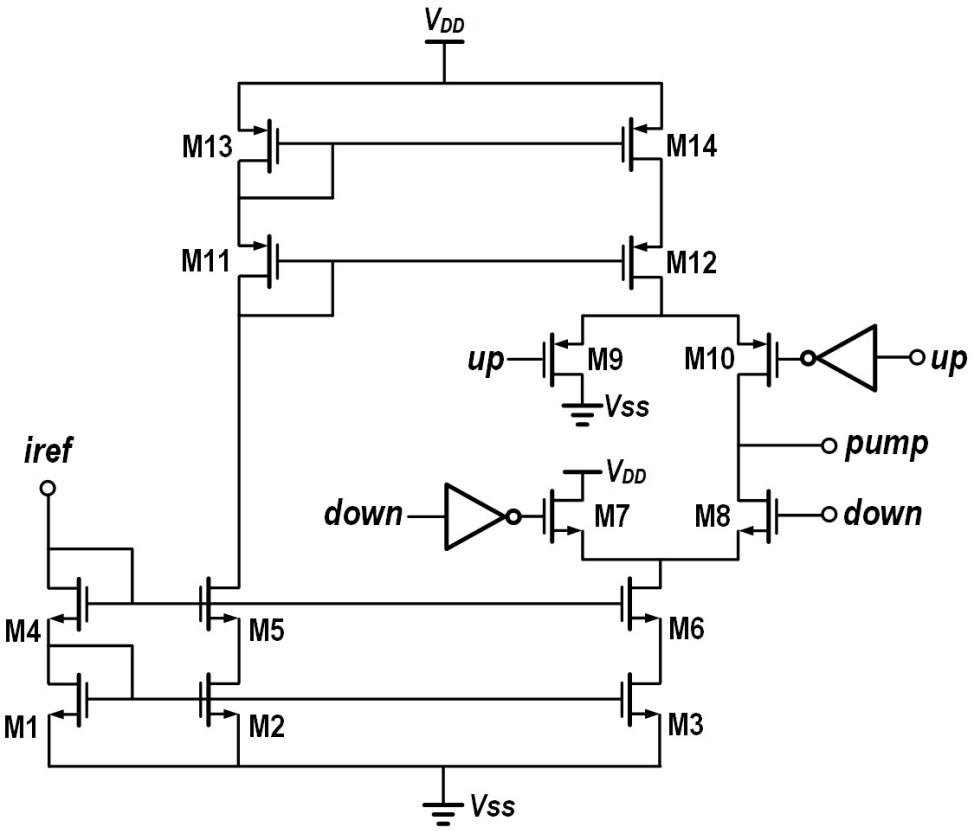


Figure 3.7: Charge pump transistor-level schematic.

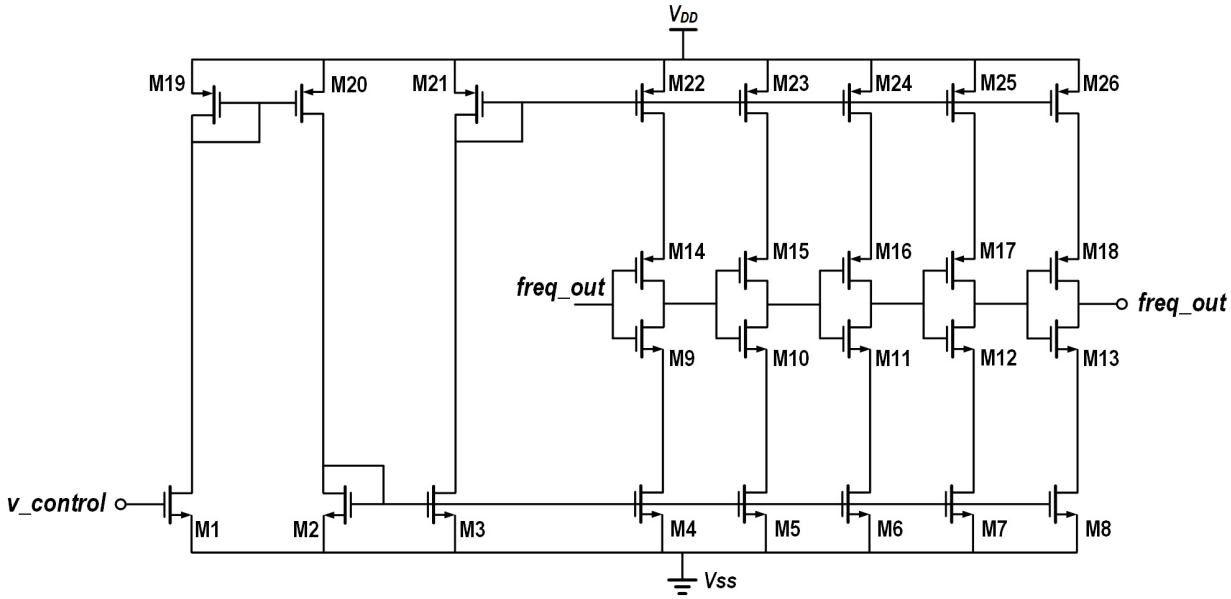


Figure 3.8: Ring oscillator.

3.2.2 Clock recovery circuit

The block diagrams of the BPSK demodulator and clock-recovery circuit are shown in Fig. 3.9. A simple clock divider is used to divide the 13.56MHz regenerated clock to generate the recovered clock. The schematic of the divide-by-128 frequency divider, which consists of seven divide-by two D flip-flops connected in tandem, is shown in Fig. 3.10.

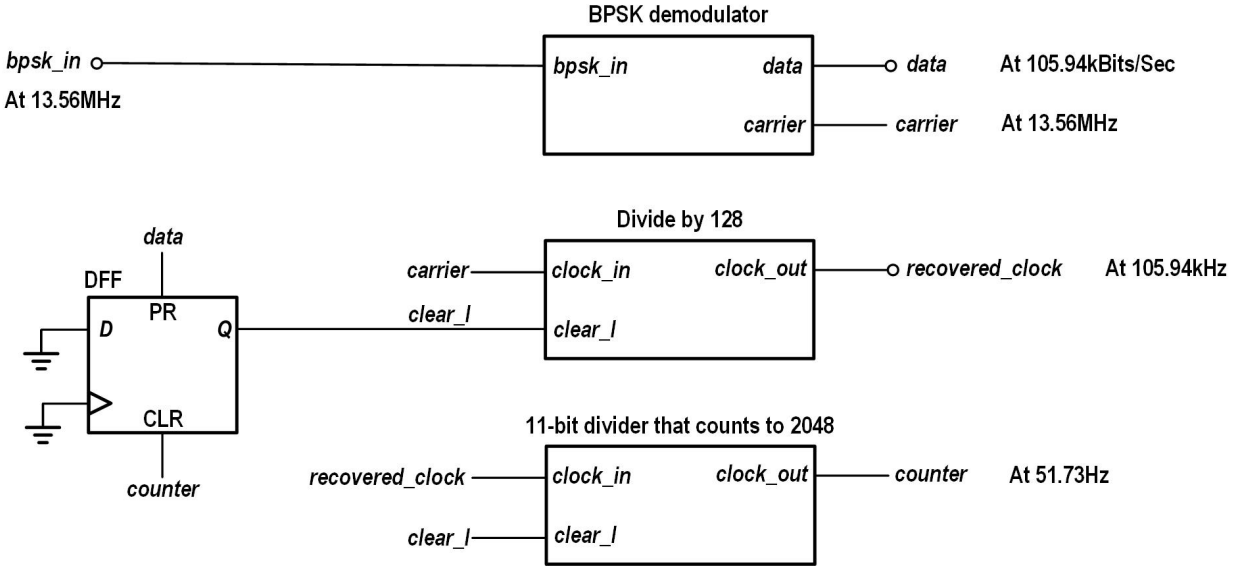


Figure 3.9: BPSK demodulator and clock recovery circuit.

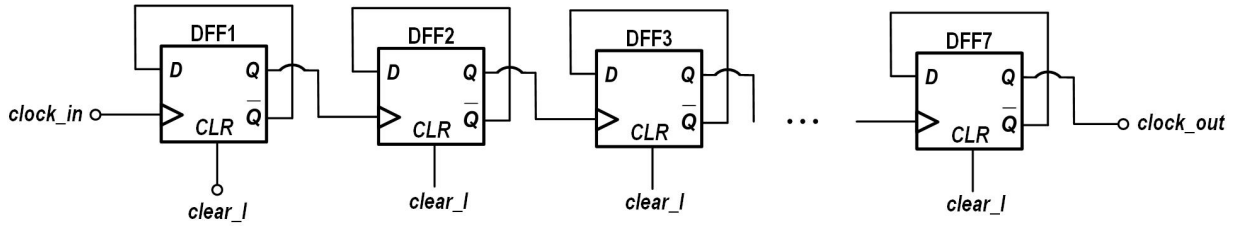


Figure 3.10: Divide by 128.

To ensure the rising edges of the recovered clock always sample the middle of the demodulated data, a counter is used to reset the divide-by-128 clock divider for every 2048 clock cycles of the recovered clock. The schematic of the 11-bit counter that counts 2048, which consists of 11 divide-by-two D flip-flops connected in tandem, is shown in Fig. 3.11.

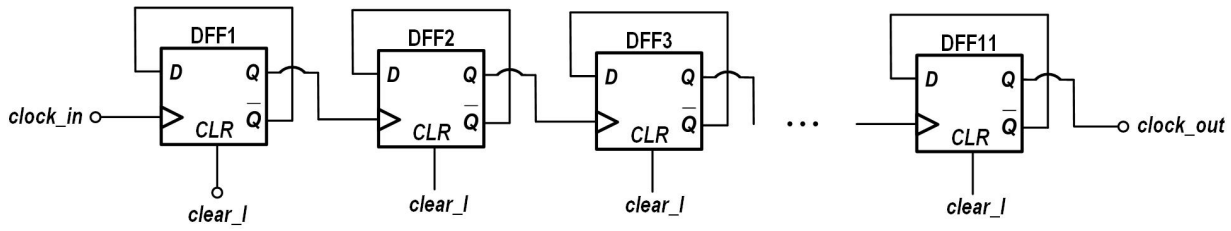


Figure 3.11: 11-bit divider that counts to 2048.

3.3 Design of the communication protocol and its circuit physical realization

3.3.1 Communication protocol

A communications protocol is a set of formal rules describing how to transmit or exchange data. For this project, the stimulation data must be transmitted wirelessly into the implanted MCM device; thus, a communication protocol needs to be specified. For the specific requirements of this medical device, a communication protocol facilitating uni-direction data transfer, low data rate and low power consumption is needed. The most commonly used wireless communication protocols are Wi-Fi, Bluetooth, Zigbee, SPI and so on; however, these wireless communication protocols are not suitable for this special application because of their implementation complexity and relatively high power consumption. A customized communication protocol has been designed and implemented for this communication system.

The communication system is shown in Fig. 3.12, where the BPSK demodulator is always on and its two outputs *data* and *clock* are fed to the communication protocol physical realization circuit block, whose outputs are the 8-bit parallel data $d7$ to $d0$, the associated clock signal $SRAM\_clock$, and the control signal $address\_reset$. The digital low of these two input signals is specified to be within -0.3V to 0.5V and the digital high of these two input signals is specified within 1.3V to 2.1V. The clock signal *clock* always samples the serial data signal *data* at its rising edges.

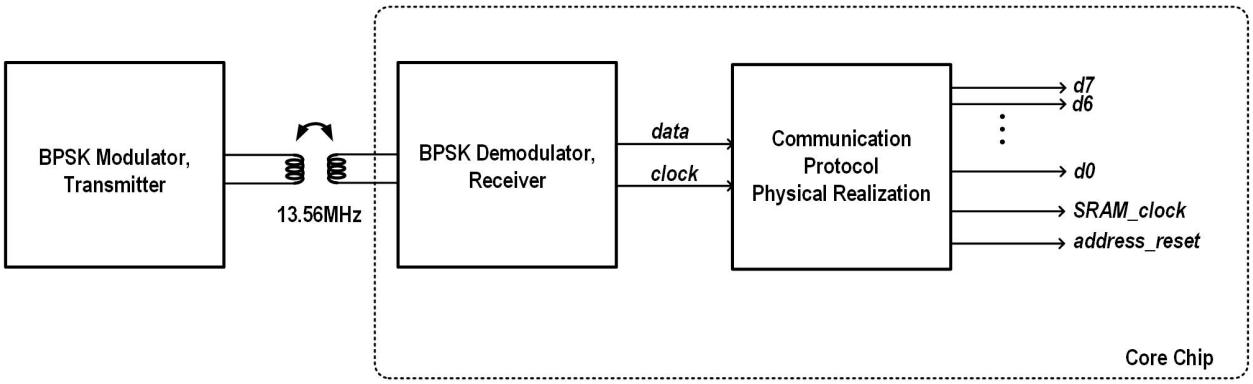


Figure 3.12: Communication system.

The terms used in this communication protocol are defined as follows.

Start sequence, a 12-bit long serial data sequence, which defines the start of transferring the serial data from the transmitter to the receiver. After the communication protocol physical realization circuit receives this 12-bit serial data, it sets the address of the SRAM and ROM to the first row, and controls the SRAM and ROM to start the data transfer process. In this design, the start sequence is designed to be 10101010101010, shown in Fig. 3.13.

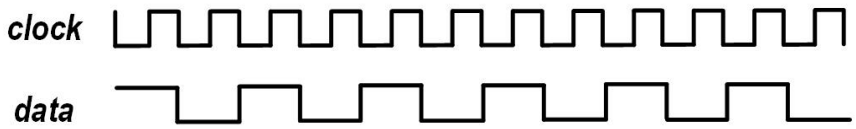


Figure 3.13: Start sequence.

End sequence, a 12-bit long serial data sequence, which defines the end of the data transfer. When the communication protocol physical realization circuit receives this 12-bit serial data, it recognizes that this is the end of the data transfer. In this design, the start sequence is designed to be 01011010101010, shown in Fig. 3.14.

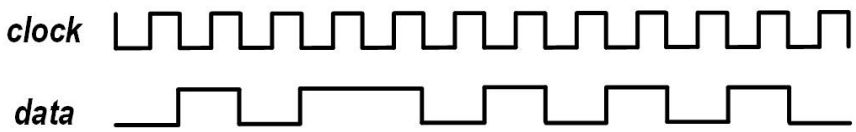


Figure 3.14: End sequence.

Data sequence, a 12-bit long serial data sequence, which defines each byte of data to be transferred. Starting from the MSB of one data sequence, the first 4 bits are the prefix bits, which are used to distinguish the data sequence from the start sequence or end sequence. In this design, the data sequence is designed to be 1111*ddddddddd*, as shown in Fig. 3.15. The first four 1*s* are the prefix bits, then each *d* represents one bit of data to be transferred. After executing this data sequence, the SRAM or ROM address increases by 1.

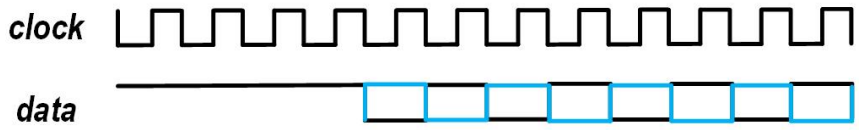


Figure 3.15: Data sequence.

There are 32 bytes of data in the SRAM and 6 bytes of data in the ROM. With each data sequence, we can transfer 1 byte of data into the core chip. Thus, in total we need to execute the data sequence 38 times to transfer all the required data into the core chip. The entire data transfer process contains 1 start sequence, 38 data sequences, 1 end sequence, as shown in Fig. 3.16.

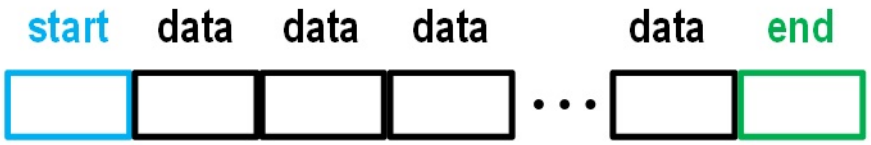


Figure 3.16: Entire data transfer process.

3.3.2 Communication protocol physical realization

The circuit realization of the communication protocol is shown in Fig. 3.17. The two outputs of the BPSK demodulator, *data* and *clock*, are fed to the inputs of this circuit. Its outputs consists of *d*7 to *d*0, *address_reset* and *SRAM_clock*, 10 signals in-total. Signals *d*7 to *d*0 are fed to the data inputs of the SRAM and ROM; *address_reset* and *SRAM_clock* are fed to the SRAM and ROM control circuit.

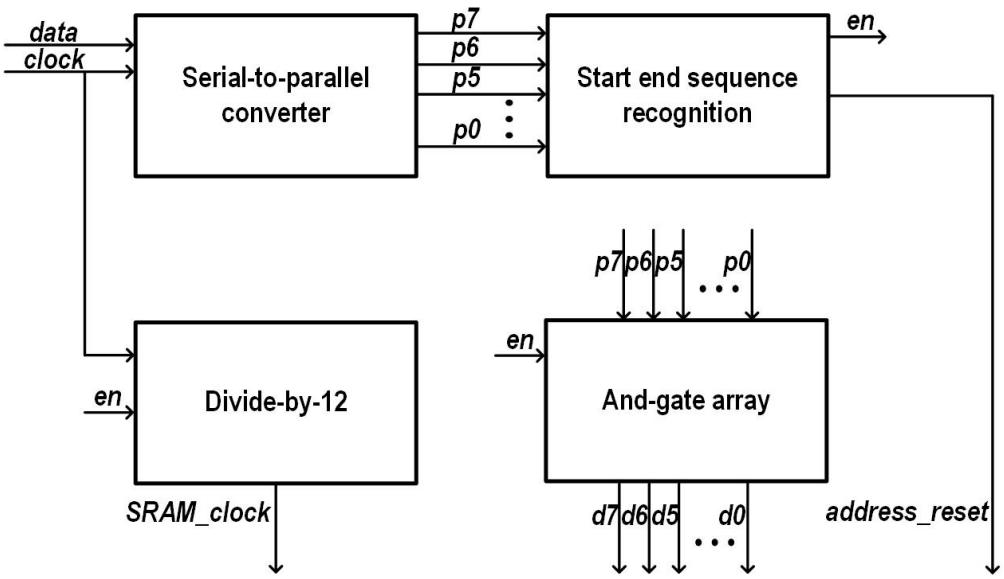


Figure 3.17: Communication protocol physical realization.

As shown in Fig. 3.17, this communication protocol physical realization circuit contains a serial-to-parallel converter which converts the incoming serial data stream into the corresponding parallel data. The start end sequence recognition block, built with combination logic, generates the corresponding *en* and *address_reset* signals. In data transfer mode, there are incoming data sequences on the *data* signal, the *en* signal is set to logic high, which enables the divide-by-12 circuit as well as the AND-gate array. The divide-by-12 circuit generates the $SRAM\_clock$ signal for the memory address decoding circuit while $d7$ to $d0$ signals are simply the buffered $p7$ to $p0$ signals. In stimulation mode, there is no data sequence on the *data* signal, the *en* signal is set to logic low, which disables the divide-by-12 circuit and the AND-gate array, and the $d7$ to $d0$ and $SRAM\_clock$ signals are set to digital low. The schematic of the serial-to-parallel converter circuit is shown in Fig. 3.18, where each DFF pair consists of two cascaded D-flip-flops. The schematic of the divide-by-12 circuit is shown in Fig. 3.19.

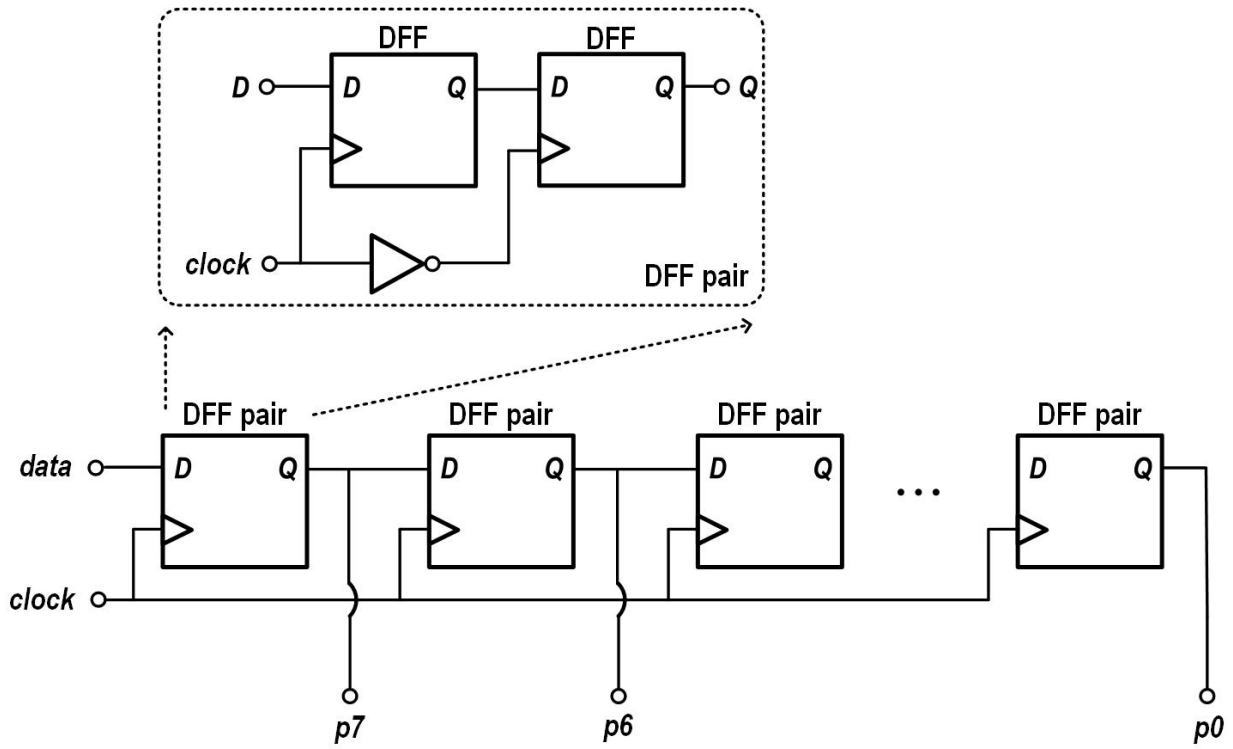


Figure 3.18: Serial to parallel converter.

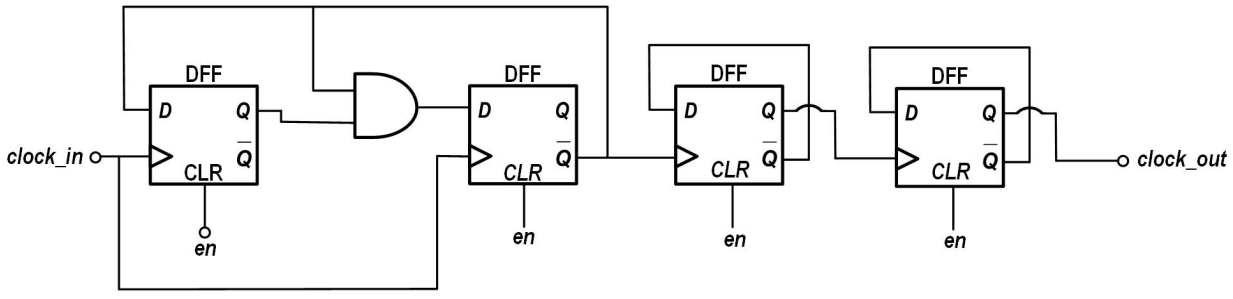


Figure 3.19: Divide by 12.

3.4 Design of SRAM and ROM and the associated address decoding circuit

3.4.1 SRAM

As described in the system block diagram, the data for the stimulation waveform is stored in the SRAM. To generate one cycle of the stimulation waveform, the DAC reads the SRAM data from the first row to the last row. Each cycle of the stimulation waveform contains 32 sampling points; thus, there should 32 rows in the SRAM. The DAC has 8-bit resolution, meaning that each row of the SRAM should contain 8 bits. Fig. 3.20 illustrates how one cycle is sampled.

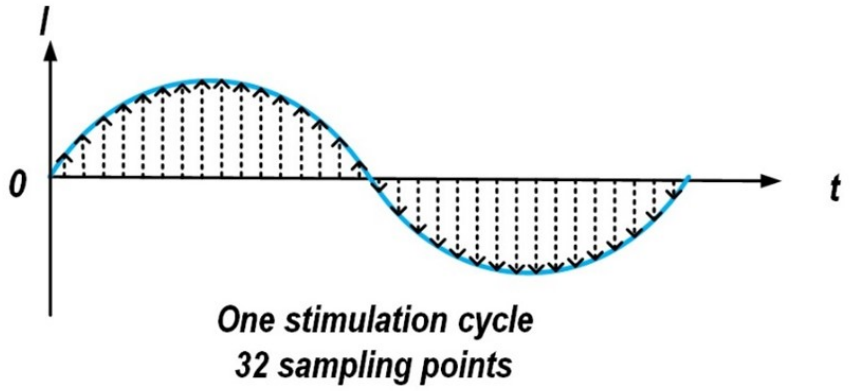


Figure 3.20: Sampling of one stimulation cycle.

Fig. 3.21 shows the SRAM structure mentioned above. It consists of 32 rows, with each row consisting of 8 bits of data. In total, 32*8=256 bits are stored in the SRAM in order to generate one cycle of the stimulation waveform.

Fig. 3.22 shows the schematic of each bit of the SRAM. The two inverters in this circuit form a standard 1-bit SRAM cell, with the two tri-state buffers being used to control the write or read operation. When *write_select* line is high, the input data can be written into this 1-bit SRAM cell; when it is low, the left tri-state buffer is in its high-output-impedance state;

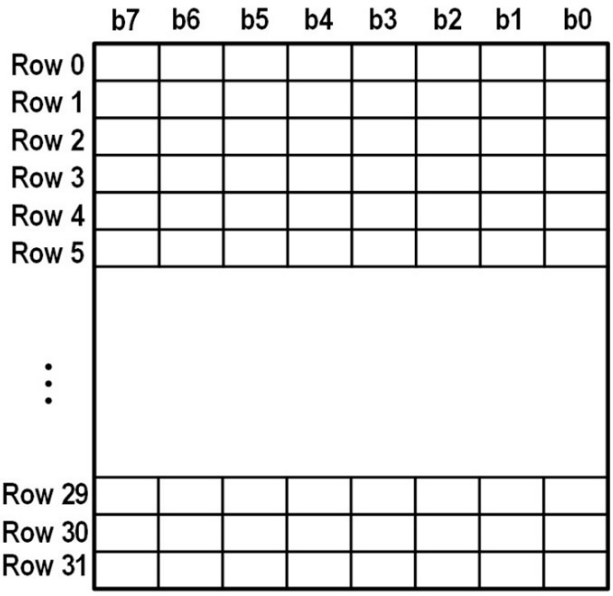


Figure 3.21: SRAM structure.

thus, the data in the SRAM cell is retained. The right tri-state buffer for read operation works in a similar manner. When *read_select* line is high, the data in this 1-bit SRAM cell is passed to *data_out*; when *read_select* line is low, the output of the right tri-state buffer is in its high-output-impedance state.

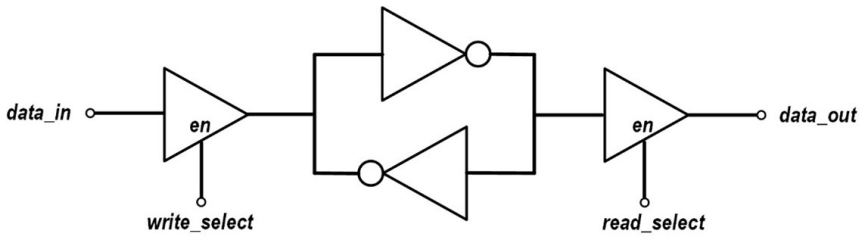


Figure 3.22: SRAM unit cell.

Each row in the SRAM contains 8 of the above described unit SRAM cells as shown in Fig. 3.23. All eight blocks share the same *write_select* and *read_select* signals.

There are 32 rows in total as shown in Fig. 3.24. All wires with a same net name are connected together. When writing or reading data into or from a specific row, the corresponding row is enabled, all other rows are disabled. The wires *b*7*_in* to *b*0*_in* are the shared write bus lines. Similarly, wires *b*7*_out* to *b*0*_out* are the shared read bus lines.

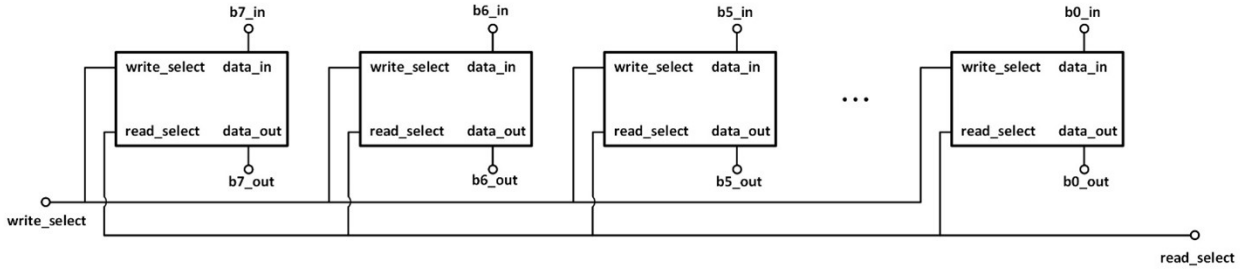


Figure 3.23: SRAM one byte.

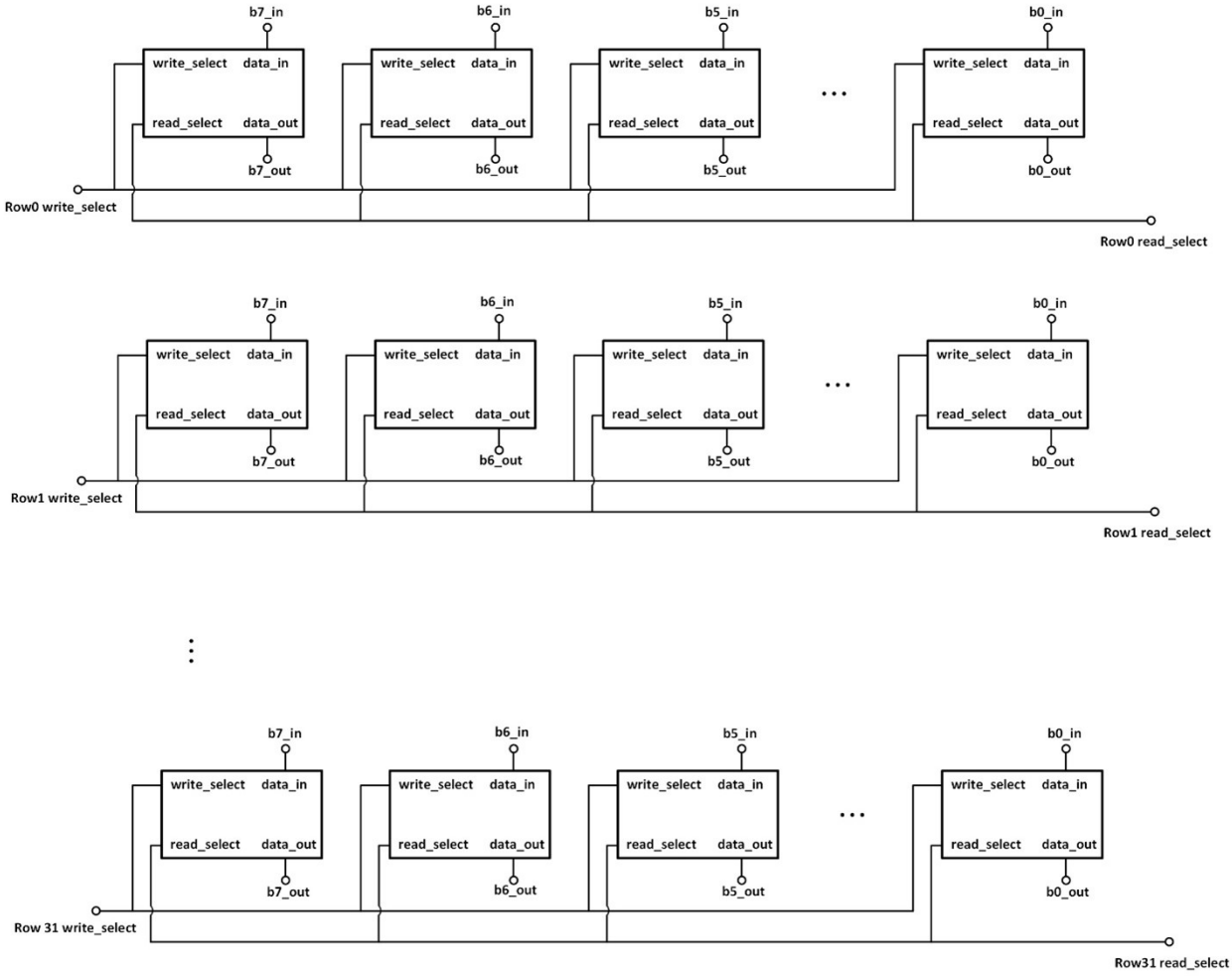


Figure 3.24: Entire SRAM block.

3.4.2 ROM

As mentioned in the SRAM section, the data specifying waveform shape is stored in the SRAM since these data need be accessed periodically in order to generate the stimulation waveform. Some other data, such as the control bits for the amplitude control block, that need be accessed constantly, are stored in the on-chip ROM. The ROM structure, which is shown in Fig. 3.25, consists of 6 rows, with each row consisting of 8 bits of data; thus, there is a total of 48 bits of data.

Row 0	b7	b6	b5	b4	b3	b2	b1	b0
Row 1	b15	b14	b13	b12	b11	b10	b9	b8
Row 2	b23	b22	b21	b20	b19	b18	b17	b16
Row 3	b31	b30	b29	b28	b27	b26	b25	b24
Row 4	b39	b38	b37	b36	b35	b34	b33	b32
Row 5	b47	b46	b45	b44	b43	b42	b41	b40

Figure 3.25: ROM structure.

Fig. 3.26 shows the schematic of the unit cell of the ROM. It is similar to the SRAM unit cell in Fig. 3.22, except that the ROM's output is always enabled to allow constant access to its data.

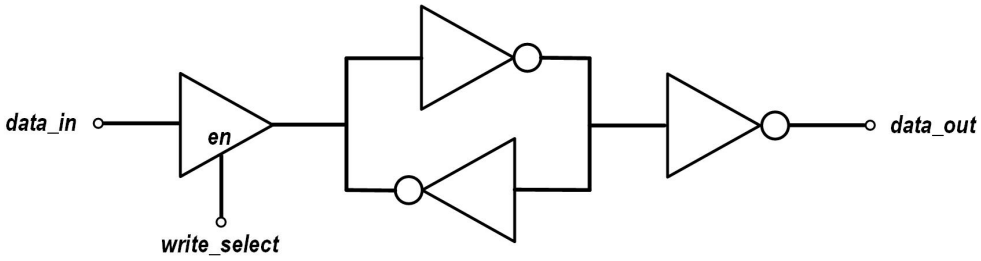


Figure 3.26: ROM unit cell.

Similar to the SRAM block, each row in the ROM contains 8 of the Fig. 3.26 unit ROM cells as shown in Fig. 3.27. All eight blocks share the same *write_select* and *read_select* signals.

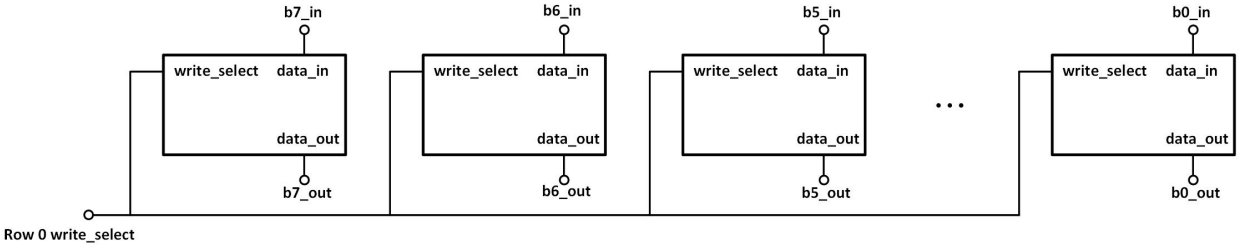


Figure 3.27: ROM one byte.

The ROM contains 6 rows in total as shown in Fig. 3.28, and works in a similar way as the Fig. 3.24 SRAM block.

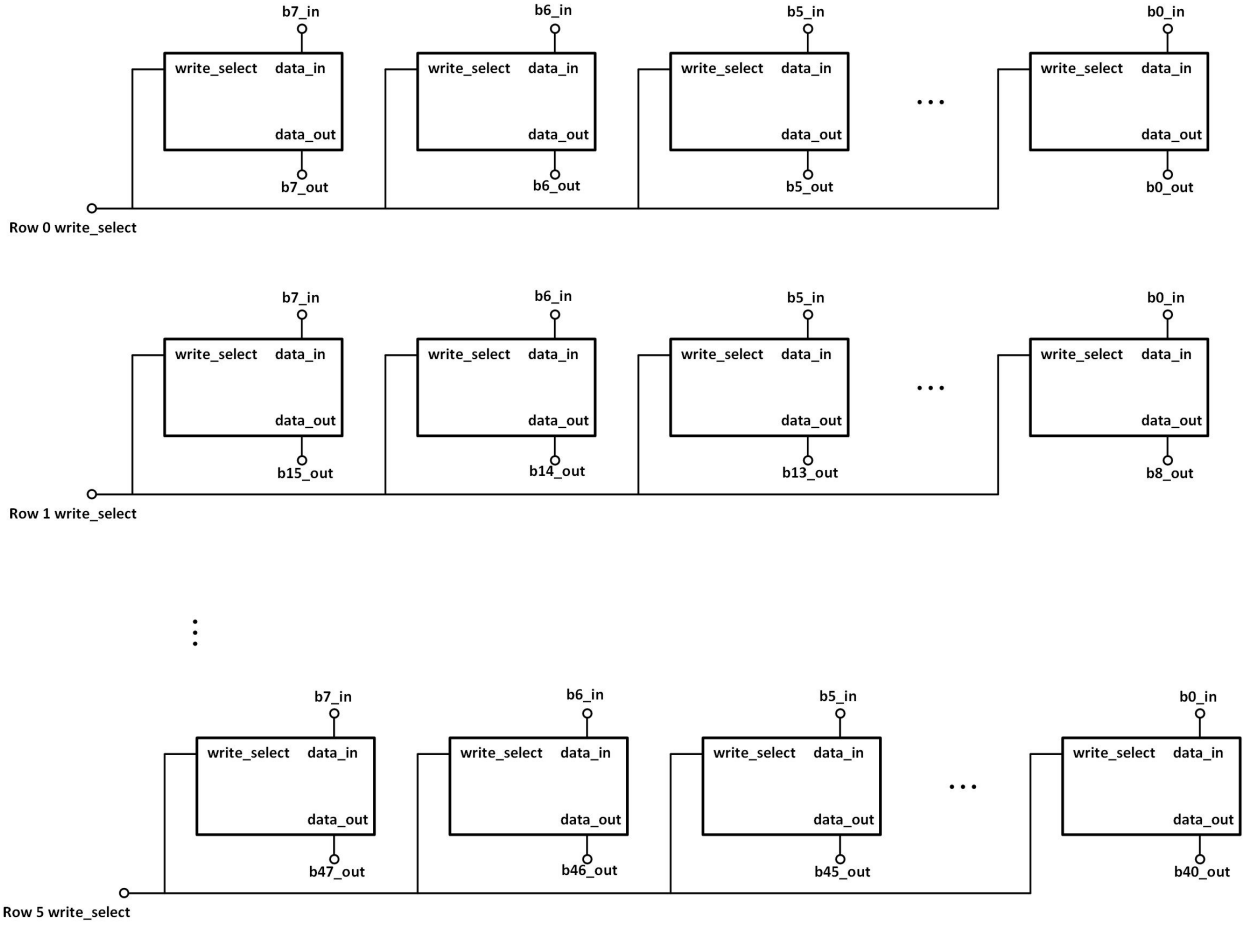


Figure 3.28: Entire ROM block.

3.4.3 Address decoder circuit

The write address decoder circuit is necessary for selecting a specific row of the SRAM and ROM for the write operation. The ROM is cascaded after the SRAM as shown in Fig. 3.29. Data is written into the SRAM and ROM, starting from row 0 and finishing at row37.

	b7	b6	b5	b4	b3	b2	b1	b0
Row 0	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 1	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 2	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 3	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 4	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 5	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
⋮								
Row 29	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 30	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 31	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
Row 32	ROM	ROM	ROM	ROM	ROM	ROM	ROM	ROM
Row 33	ROM	ROM	ROM	ROM	ROM	ROM	ROM	ROM
Row 34	ROM	ROM	ROM	ROM	ROM	ROM	ROM	ROM
Row 35	ROM	ROM	ROM	ROM	ROM	ROM	ROM	ROM
Row 36	ROM	ROM	ROM	ROM	ROM	ROM	ROM	ROM
Row 37	ROM	ROM	ROM	ROM	ROM	ROM	ROM	ROM

Figure 3.29: Write operation memory structure.

The address signal contains 6 bits $a5 - a0$, from which, the address decoder circuit decodes into the address selection signal. Address 000000 corresponds to row0 of the memory structure shown in Fig. 3.29; address 100101 corresponds to row37. The gate-level schematic of the write address decoder is shown in Fig. 3.30.

The read address decoder for the SRAM utilizes the exact same structure, the only difference is that the address signal contains 5 bits instead of 6 bits, also, there are 32 outputs instead

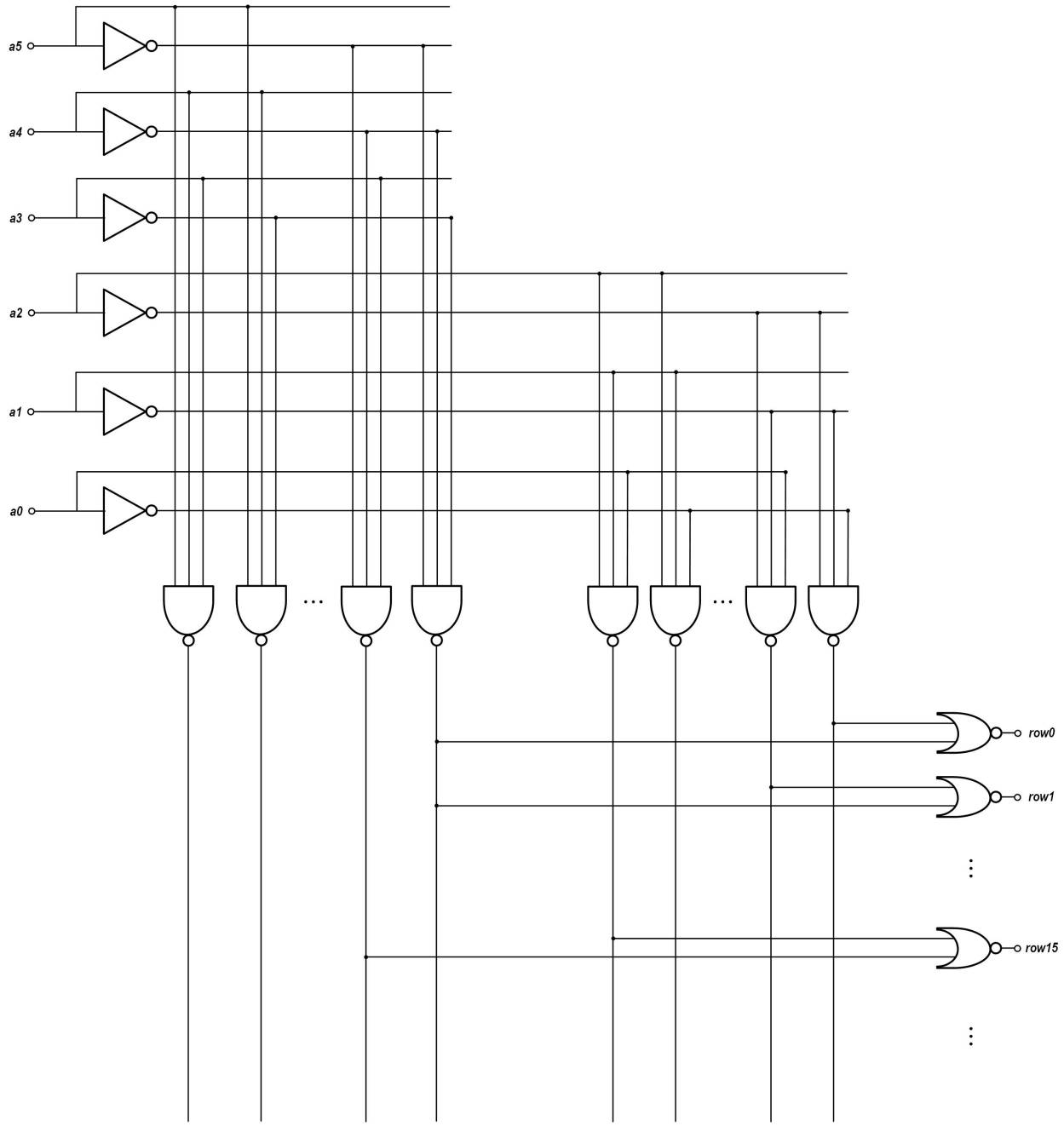


Figure 3.30: Write address decoder.

of 38.

3.5 Design of the relaxation oscillator

There are 32 sampling points taken within each cycle of the simulation waveform, with the frequency of stimulation waveform spanning across the audio frequency range, i.e., 150Hz - 20kHz. Thus, the clock frequency of the digital-to-analog converter that generates the stimulation waveform should span from 4.8kHz - 640kHz. This frequency range is too low to generate using a simple on-chip ring oscillator; however, a relaxation oscillator is specifically designed to oscillate at low frequencies; thus, the on-chip relaxation oscillator is designed and explained as follows.

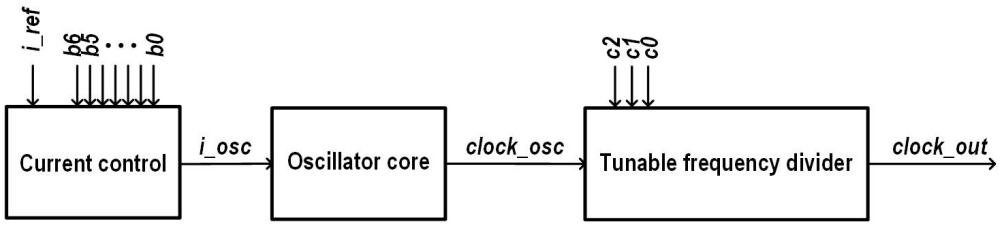


Figure 3.31: Clock generator.

Fig. 3.31 shows the block diagram of the entire clock generator, which consists of three major internal sub-blocks: the current control, the oscillator core, and the frequency divider. The current control block generates a tunable dc current *i_osc* for the oscillator core. The oscillator core block, whose detailed design is explained later in this chapter, generates the signal *clock_osc* with a frequency range of 65kHz - 3MHz. The tunable frequency divider block is then used to divide the *clock_osc* signal to generate the *clock_out* signal whose frequency can cover the desired 4.8kHz - 640kHz range.

Fig. 3.32 shows the schematic of the reference current control block. The bottom portion of this figure is a 7-bit current digital-to-analog converter (DAC), where the 5μA input reference current i_ref is derived from the bandgap reference. The top portion is a current mirror converting the current direction from flowing into the block to flowing out from the block. The output current *i_out* can be calculated using Eq. 3.2.

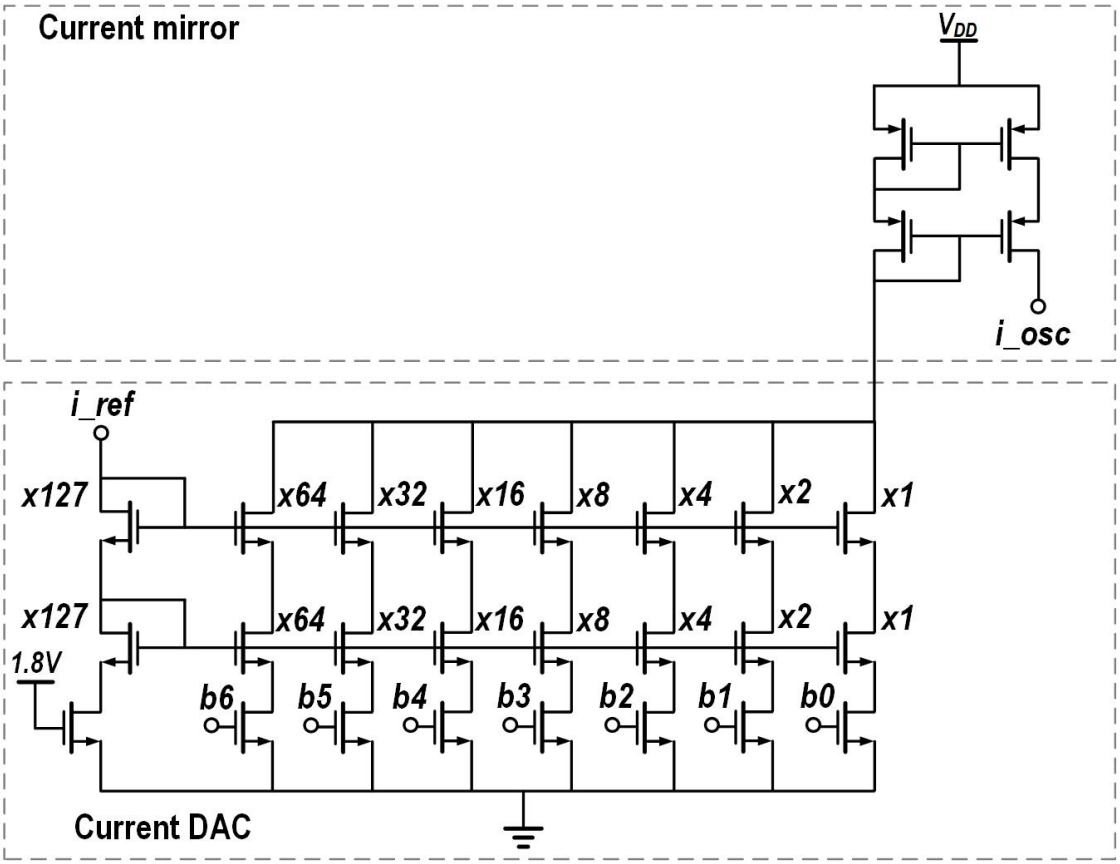


Figure 3.32: Current control.

$$i\_osc = \frac{i\_ref}{127} \sum_{k=0}^{6} 2^k \cdot a_k \tag{3.2}$$

This provides an output current that ranges from 39.4nA to 5μA.

Fig. 3.33 shows the schematic of the well-known relaxation oscillator, consisting of two comparators, a charge pump, and an S-R latch. The two reference voltages $Vhigh$ and $Vlow$ are generated by the resistor voltage divider, with the decoupling capacitors used to provide solid small-signal grounds for the reference voltages. The supply voltage of this block is derived from the output of a regulated LDO, whose value is set to 1.8V and insensitive to PVT variations. When powering up the chip, the initial charge in the capacitor C1 is

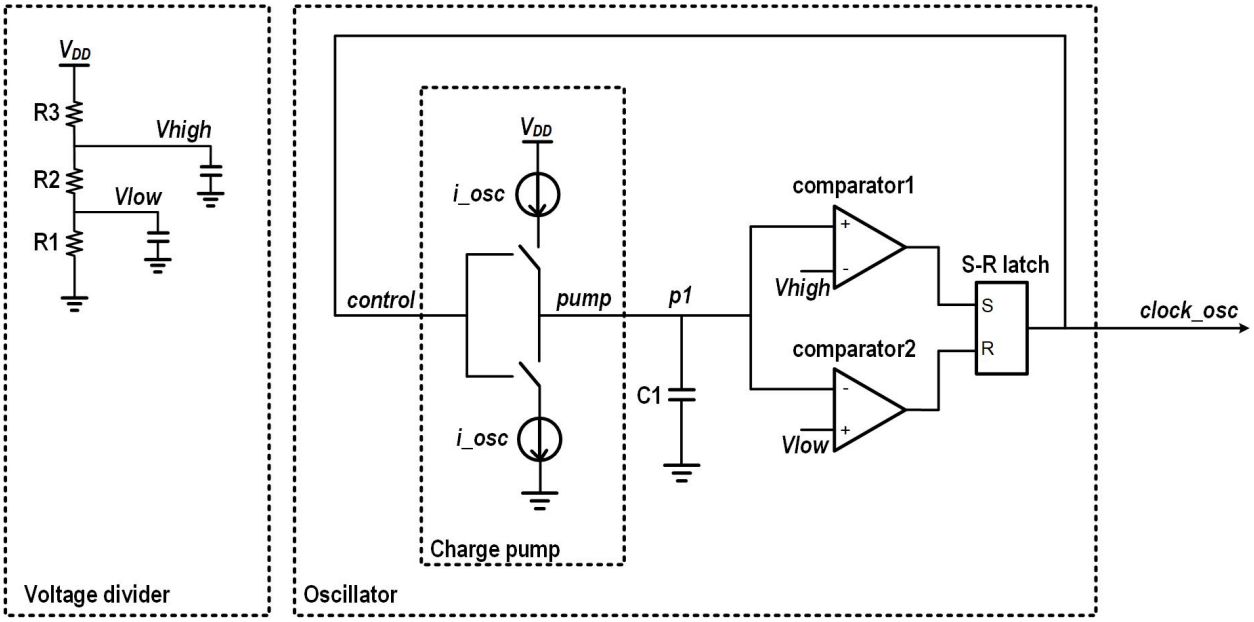


Figure 3.33: Oscillator core.

zero. The S-R latch generates a digital low control signal such that the top switch in the charge pump is turned on and the bottom switch is turned off. The top current source starts charging the capacitor and the voltage at p1 continuously rises until it reaches $Vhigh$; at this point, the S-R latch changes state and generates a digital high such that the top switch is turned off and the bottom switch is turned on. The bottom current source then starts discharging the capacitor and the voltage at p1 continuously decreases until it drops below $Vlow$, after which, the S-R latch changes state again. As this process continues, the circuit oscillates at a frequency given by Eq. 3.3.

$$clock\_out = \frac{i\_osc}{2 \cdot C1 \cdot (Vhigh - Vlow)} \tag{3.3}$$

In this design, the value of capacitor C1 is 0.45pF, $Vlow$ is 0.6V and $Vhigh$ is 1.2V. Due to parasitic capacitance and resistance, transistor non-linearity, the generated output frequency of this relaxation oscillator is 65kHz - 3MHz.

Fig. 3.34 shows the schematic of the charge pump, where all current mirrors are based on the cascode topology to ensure precision of the current mirror. When the *control* signal goes high, the circuit conducts current into the load; when the *control* signal goes low, the circuit conducts current from the load.

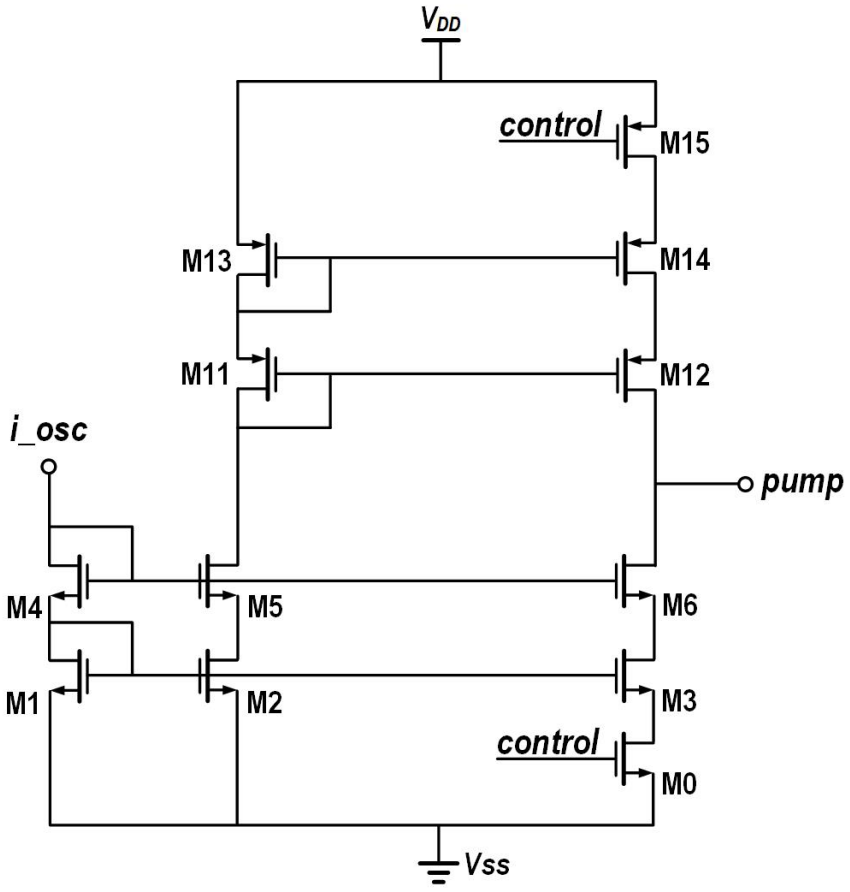


Figure 3.34: Charge pump.

Fig. 3.35 and Fig. 3.36 show the schematic of the NMOS-input and PMOS-input comparators respectively. The NMOS-input comparator functions best when comparing voltages higher than half of the supply voltage of the comparator while the PMOS-input comparator functions best when comparing voltages lower than half of the supply voltage of the comparator.

Designing an fully integrated on-chip relaxation oscillator that can cover the required three-decade frequency range is very challenging. A better solution is to use a frequency divider

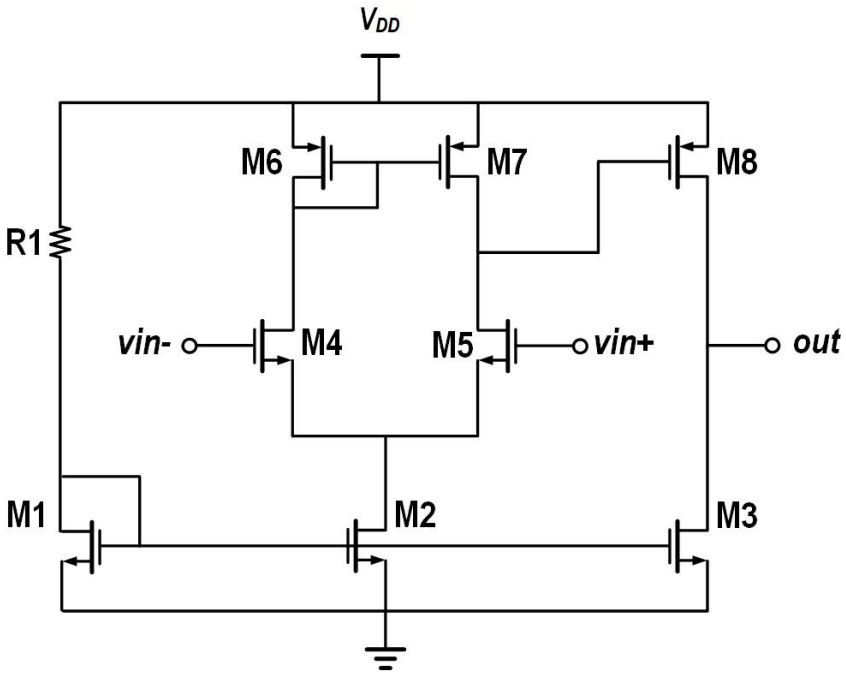


Figure 3.35: NMOS-input comparator.

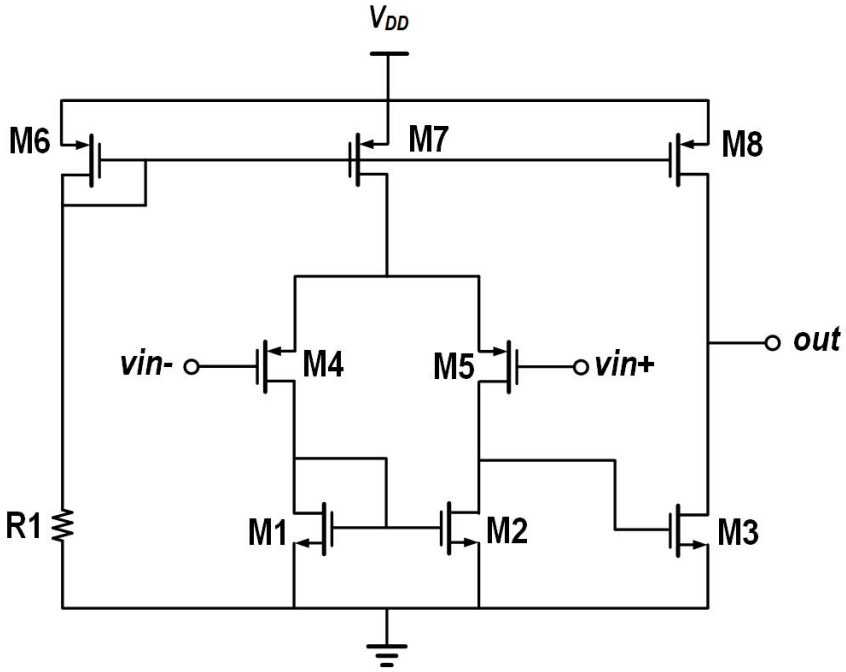


Figure 3.36: PMOS-input comparator.

following the relaxation oscillator. With this approach, the relaxation oscillator only needs to cover one decade of the frequency range. Fig. 3.37 shows the schematic of such a tunable

frequency divider.

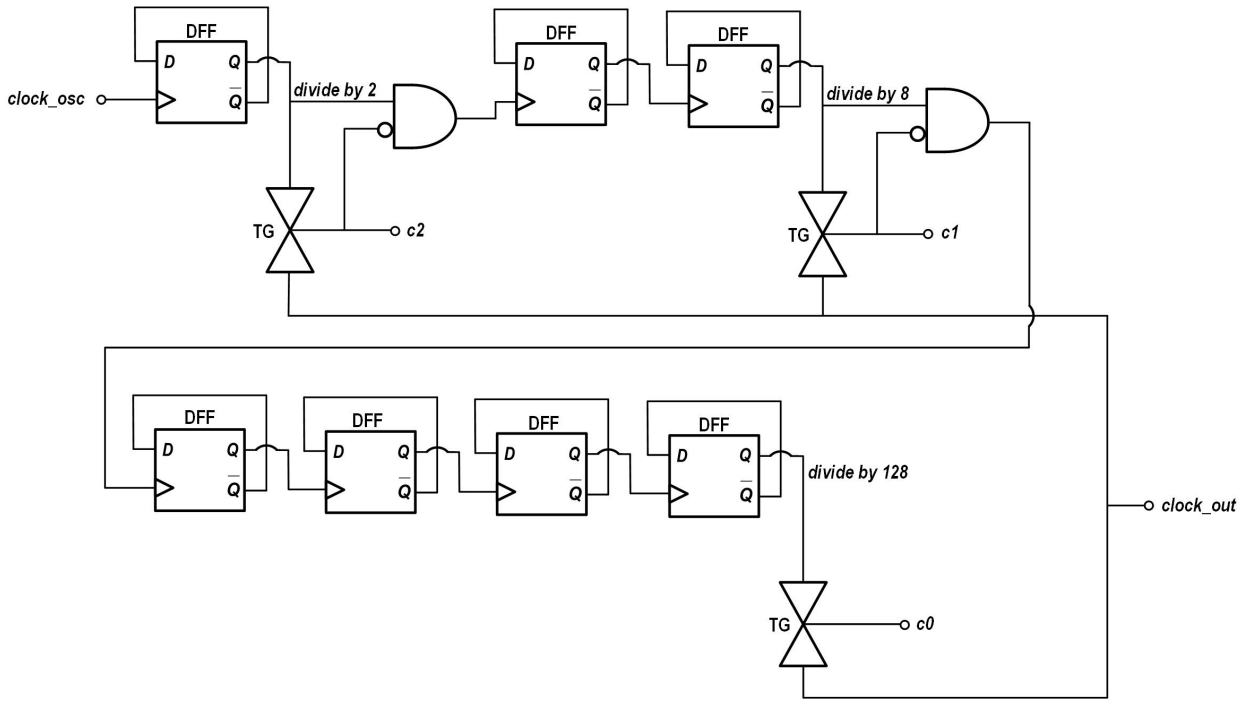


Figure 3.37: Tunable frequency divider.

There are three different dividing ratios of this frequency divider: divide by 2, 8, 128. This ratio is selected by the three-bit divider control signals $c2, c1, c0$ as shown in Table 3.1. The output frequency shown in this table covers the desired 4.8kHz - 640kHz range, where the three input frequency ranges are all within the relaxation oscillator 65kHz - 3MHz frequency generation capability.

Table 3.1: Divide ratio, output range, input range vs. control signal

Control bits c2,c1,c0	**Divide ratio**	**Output frequency range**	**Input frequency range**
001	128	4.8kHz - 20kHz	614.4kHz - 2560kHz
010	8	20kHz - 200kHz	160kHz - 1600kHz
100	2	200kHz - 640kHz	400kHz - 1280kHz

3.6 Design of digital-to-analog converter

The 8-bit current-steering DAC is implemented to generate the necessary arbitrary differential current stimulation signals. As illustrated in Fig. 3.38, the 2 most significant bits (MSBs) $bin7$ to $bin6$ are decoded into thermometer-code weighted control signals $t0$ to $t2$ by the binary to thermometer decoder, while bits $bin5$ to $bin0$ are still binary-weighted. The use of thermometer-code weighted bits for the MSBs in this DAC is crucial due to its ability to provide high resolution and linearity in the conversion process. For the thermometer-code weighted 3 control signals $t0$ to $t2$, each signal controls a unique current source, resulting in a linear relationship between the digital input and the analog output current. This approach ensures that each increment in the digital input results in a proportional change in the analog output, thus preserving precision [15].

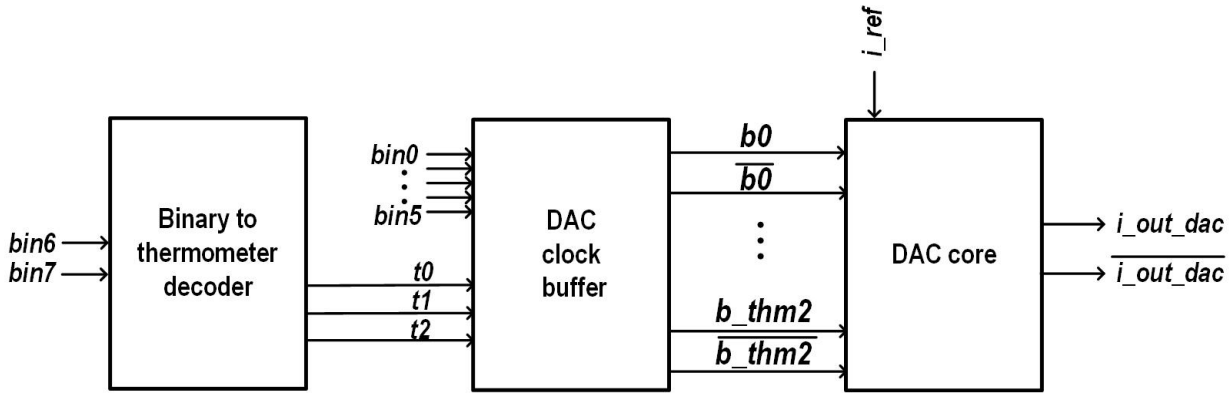
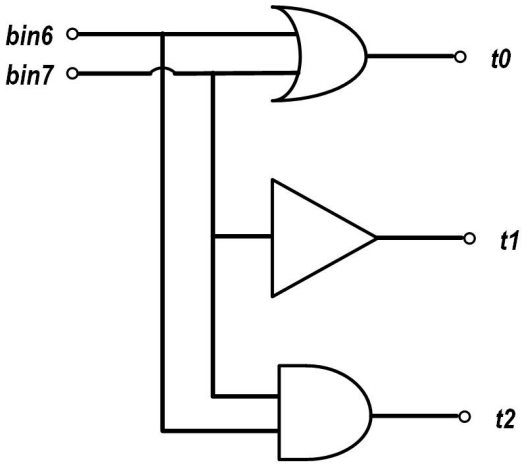


Figure 3.38: DAC top.

The schematic of the binary-to-thermometer decoder is depicted in Fig. 3.39, accompanied by the corresponding truth table showcased in the same figure. All digital gates utilized were sourced from the TSMC standardized 1.8-V digital library, which ensures consistency and reliability in the decoder's functionality.

For the DAC to operate with optimal precision and accuracy, it is imperative to ensure synchronized data transitions across all control bits simultaneously. This necessitates the



bin7, bin6	t2, t1, t0
00	000
01	001
10	011
11	111

Figure 3.39: Binary to thermometer decoder.

re-synchronization of all control bits with the *clock_in* signal. The schematic shown in Fig. 3.40 illustrates the methodology employed to achieve this synchronization, this circuit performs dual functions: converting the single-ended control signals into differential signals, also utilizing buffers to amplify the control signals, which ensures good signal strength when driving capacitive loads.

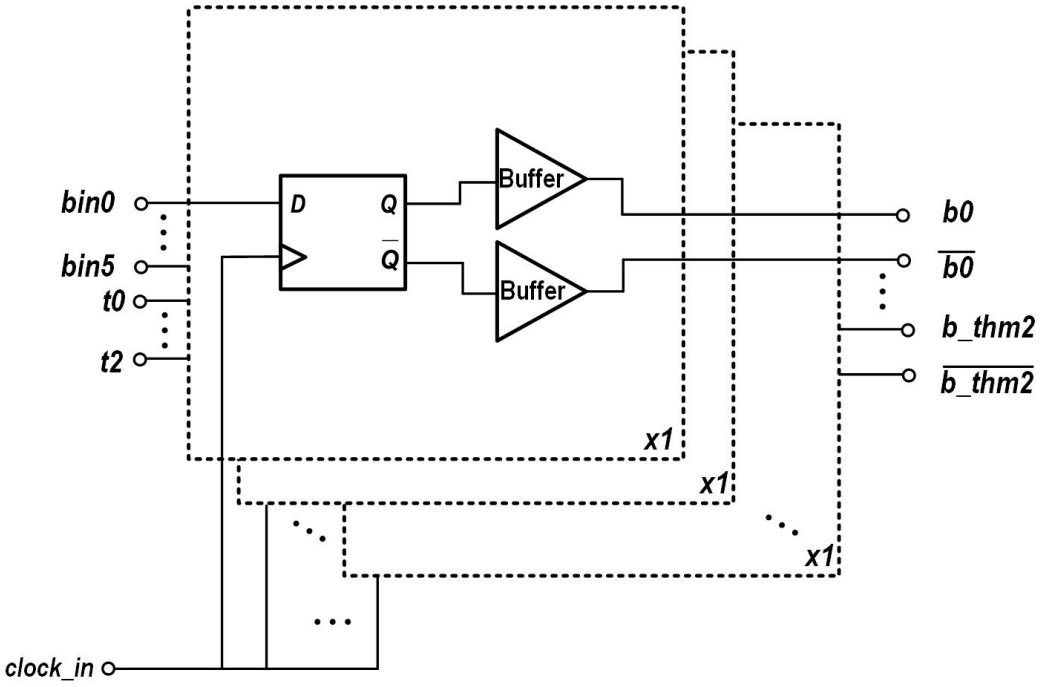


Figure 3.40: DAC clock buffer.

Fig. 3.41 illustrates the schematic of the DAC core, which comprises the reference, binary, and thermometer-code weighted branches. Specifically, the reference branch consists of 32 unit cells, while the binary branches consist of varying number of unit cells, ranging from 1 to 32 corresponding to $b0$ through $b5$ control signals, each thermometer-code weighted branch contains 64 unit cells. This DAC is carefully laid out using the common-centroid technique to reduce mismatches between unit cells.

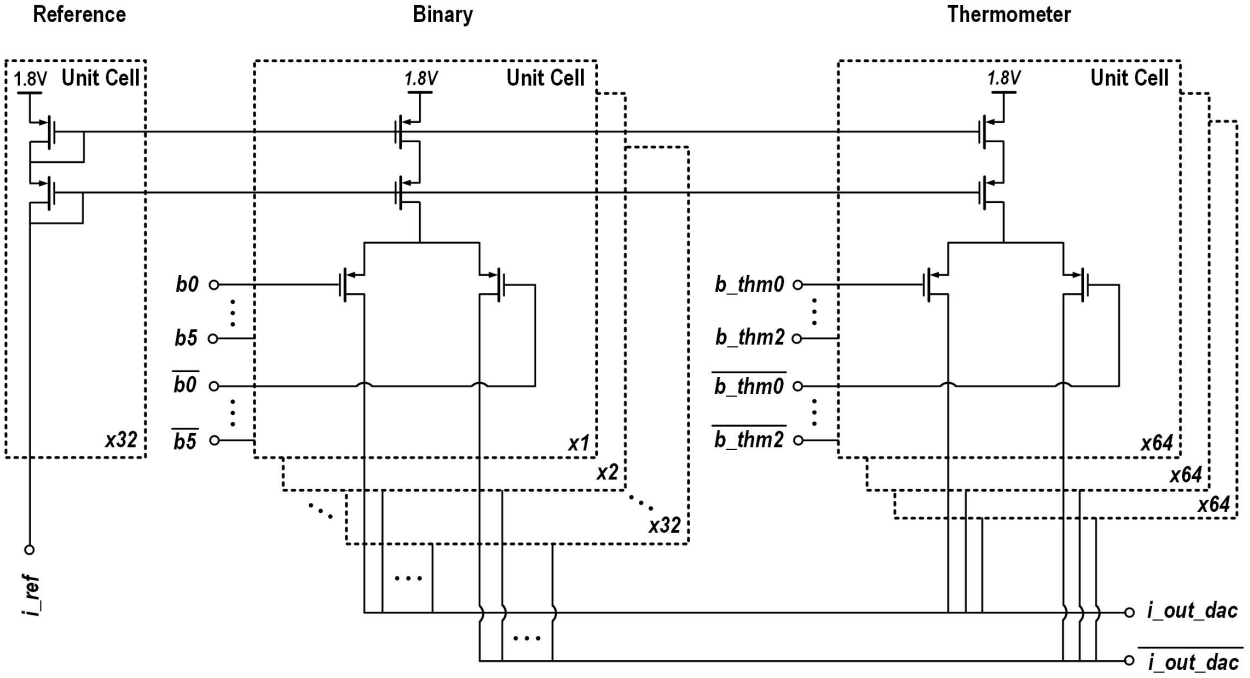


Figure 3.41: DAC core.

The reference current i_ref is set to 8μA, derived from the bandgap current reference on the supply chip. The following equations provide expressions for the output current i_out_dac and its complement $\overline{i\_out\_dac}$:

$$i\_out\_dac[n] = \frac{i\_ref}{32}\left[\sum_{k=0}^{5} 2^k \cdot b_k[n] + \sum_{k=0}^{2} 64 \cdot b\_thm_k[n]\right] \tag{3.4}$$

$$\overline{i\_out\_dac[n]} = \frac{i\_ref}{32}\left[\sum_{k=0}^{5} 2^k \cdot \overline{b_k[n]} + \sum_{k=0}^{2} 64 \cdot \overline{b\_thm_k[n]}\right] \tag{3.5}$$

The full-scale current available, measuring at $63.75\,\mu$A, represents the maximum current output capability of the DAC. This parameter is crucial as it dictates the range within which the DAC can accurately represent analog signals. With a resolution of 250 nA, the DAC can finely adjust its output current across this range.

For this inner-ear tissue stimulation application, this designed DAC operates within stimulation cycles in the stimulation mode, each cycle consists of 32 samples. The clock frequency of the DAC, which governs the rate at which these samples are processed and converted to analog signals, falls within the range of 4.8 kHz to 640 kHz.

Post-layout simulation indicates that this DAC operates properly with sampling frequencies up to 1 MHz. The Integral Nonlinearity (INL) of this DAC is less than ± 0.5 LSb, and the Differential Nonlinearity (DNL) is less than ± 1 LSb, suggesting it is sufficiently monotonic and linear for our application in inner-ear tissue stimulation.

3.7 Design of the amplitude control circuit

Since the DAC is designed to always operate with its full-scale amplitude, in order to generate differential current signals with tunable amplitudes, a 5-bit amplitude control block is designed as shown in Fig. 3.42. The output currents from the DAC, i_out_dac and $\overline{i\_out\_dac}$, are fed into this block. The generated signals are then mirrored to i_drive1, i_drive2, $\overline{i\_drive1}$, $\overline{i\_drive2}$ and subsequently fed into the high-voltage drive and charge balance block. The following equations give the expressions for these signals:

$$i\_drive1 = i\_drive2 = \frac{i\_out\_dac}{31} \sum_{k=0}^{4} 2^k \cdot a_k \tag{3.6}$$

$$\overline{i\_drive1} = \overline{i\_drive2} = \frac{\overline{i\_out\_dac}}{31} \sum_{k=0}^{4} 2^k \cdot a_k \tag{3.7}$$

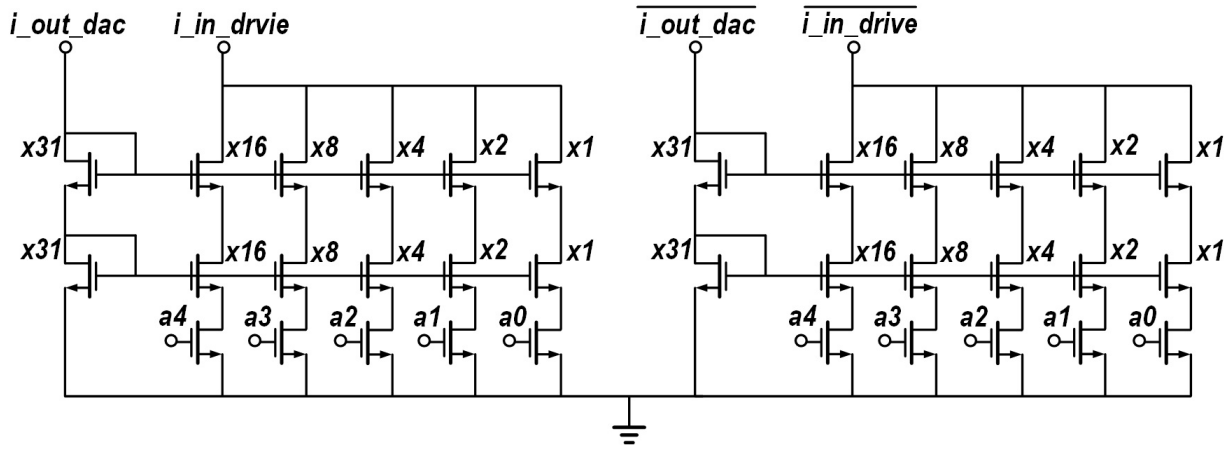


Figure 3.42: Amplitude control.

3.8 Design of the high-voltage drive and charge-balance circuit

Fig. 3.43 shows the detailed schematic of the high-voltage drive and charge balance blocks. Fig. 3.44 shows the level-shifting circuit that provides biasing voltages *control_5* and *control_15*.

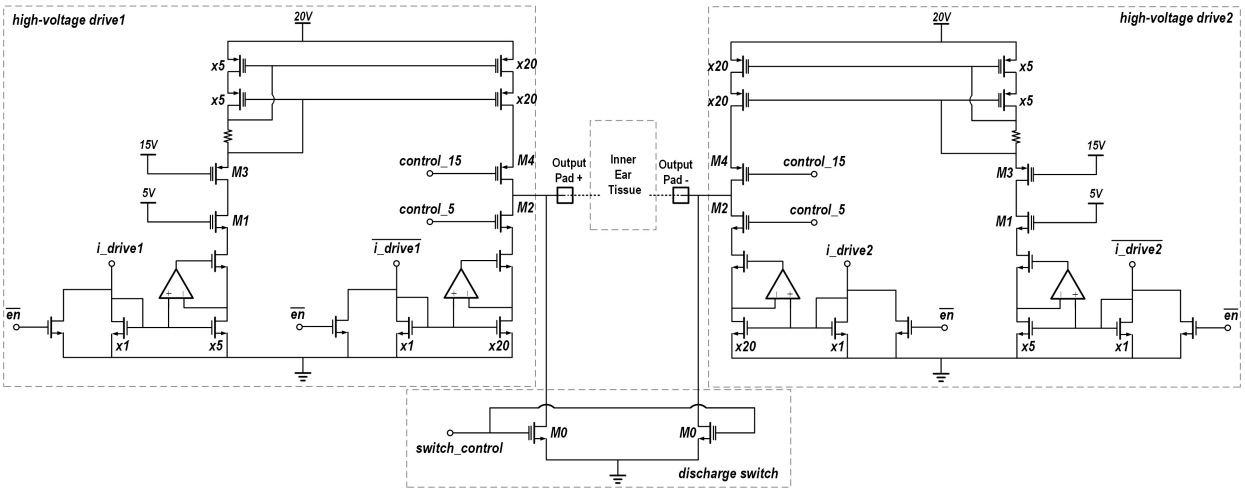


Figure 3.43: High voltage drive.

In these schematics, a double-gate symbol represents either a high-voltage transistor or a low-voltage transistor that is situated in a high-voltage well, while a single-gate symbol represents a standard 5-V transistor. Transistors M1-M4 in Fig. 3.43 are 20-V high-voltage LDMOS transistors; all other transistors in this schematic with double-gate symbols are 5-V transistors situated in high-voltage wells. The electrical rules for this process dictate that the maximum voltage magnitude between the gate and source of any high-voltage transistor must not exceed 5 V in order to prevent breakdown. For this reason the gates of M1 and M2 are biased to be no higher than 5 V, and the gates of M3 and M4 are biased to be no lower than 15 V.

To provide fully differential outputs, the two high-voltage drive circuits are designed to be identical with appropriate layout techniques to minimize random mismatches. However, even very small mismatches between the two drive circuits will result in charge accumulation;

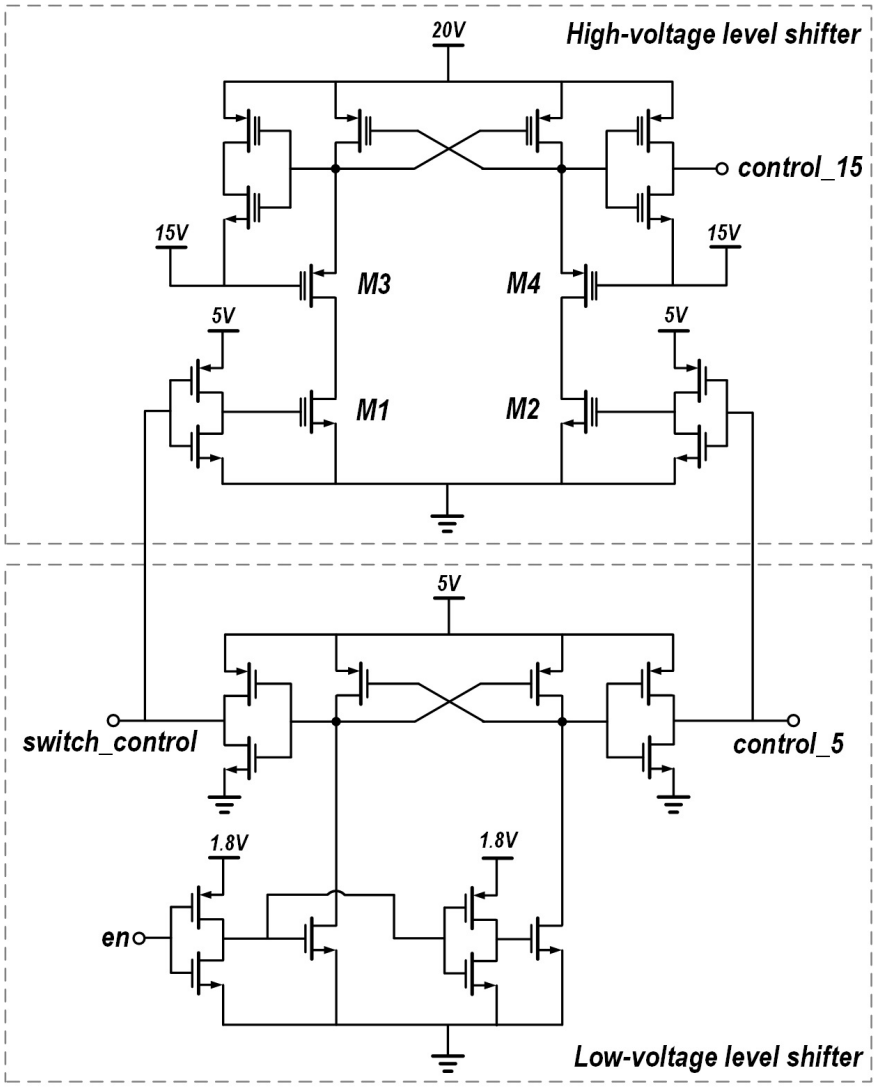


Figure 3.44: Level shifter.

therefore, charge balancing is required. A simple way to balance the residue charge that accumulates in the load would be turn on a transmission gate connected directly between the two outputs. However, designing a transmission gate that can sustain 20-V swing is not feasible in this process due to the limited 5-V breakdown voltage between gate-source junctions of high-voltage transistors. Instead, a high-voltage transistor M0 is connected between each output node and ground; these transistors can be switched on or off using 5-V or 0-V gate control voltages, respectively.

Input currents i_drive1, i_drive2, $\overline{i\_drive1}$, $\overline{i\_drive2}$ are supplied to this circuit from the

outputs of the Fig. 3.42 amplitude control circuit. When $\overline{en}$ is low the driver is in the stimulation mode, where M2 and M4 have the same gate bias as M1 and M3, respectively, and transistors M0 are turned off. In this mode a differential current, whose waveform is set by the control sequence described earlier, is applied between the two outputs.

When $\overline{en}$ goes high the driver is in the charge balance mode. In this mode transistors M2 and M4 are turned off by setting *control_5* to 0 V and *control_15* to 20 V. At the same time the *switch_control* node is set to 5 V, so that transistors M0 pull the outputs to ground.

The schematic of the operational amplifier used in is shown in Fig. 3.43. The supply voltage of this operational amplifier is 5V. PMOS transistor input stage is selected because the flicker noise of PMOS transistor is lower than that of the NMOS transistor [16], which can reduce the overall output noise of the stimulation current. The dimensions of the current mirrors realized by transistors M1-M4 and M7-M8 are set such that the current gains are all unity. The aspect ratio of M10 is 8 times of that of M9, and R1 is used to generate a 5μA reference current conducted in M9.

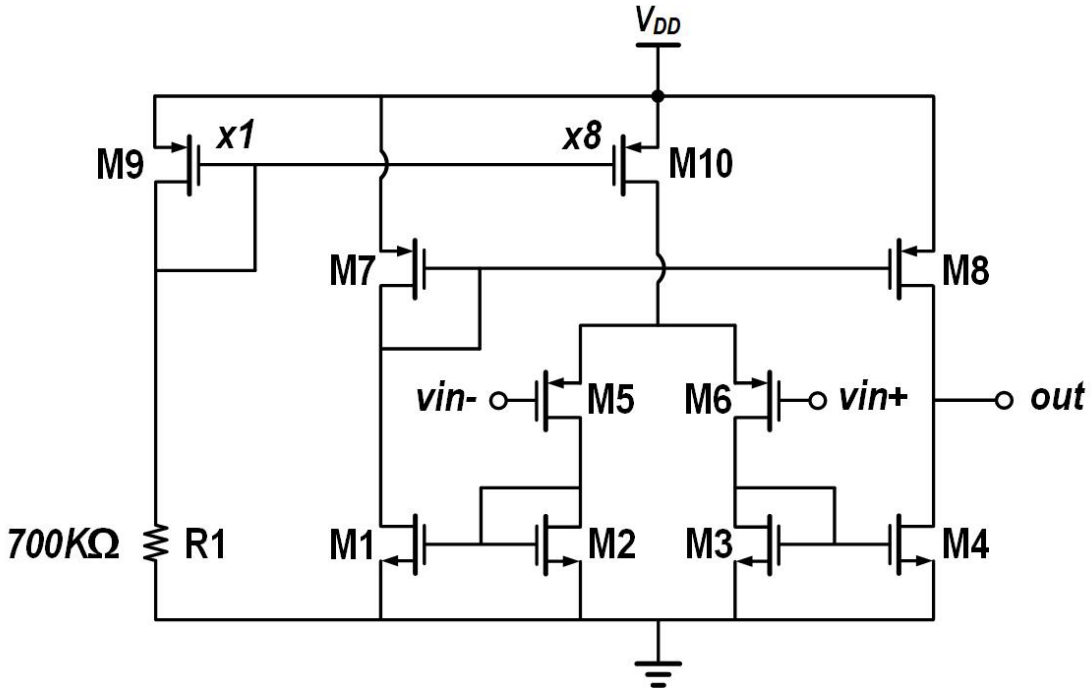


Figure 3.45: Operational amplifier in high-voltage drive.

3.9 Layout of the core chip

The entire core chip had been laid out manually using Cadenced Virtuoso layout editor tool as shown in Fig. 3.46. Compliance checks for design rules, layout vs. schematic, antenna rule, as well as parasitic extraction, were all performed using the Mentor Graphics Calibre tools. With parasitic resistors and capacitors been included, post-layout simulation shows the chip functions as expected.

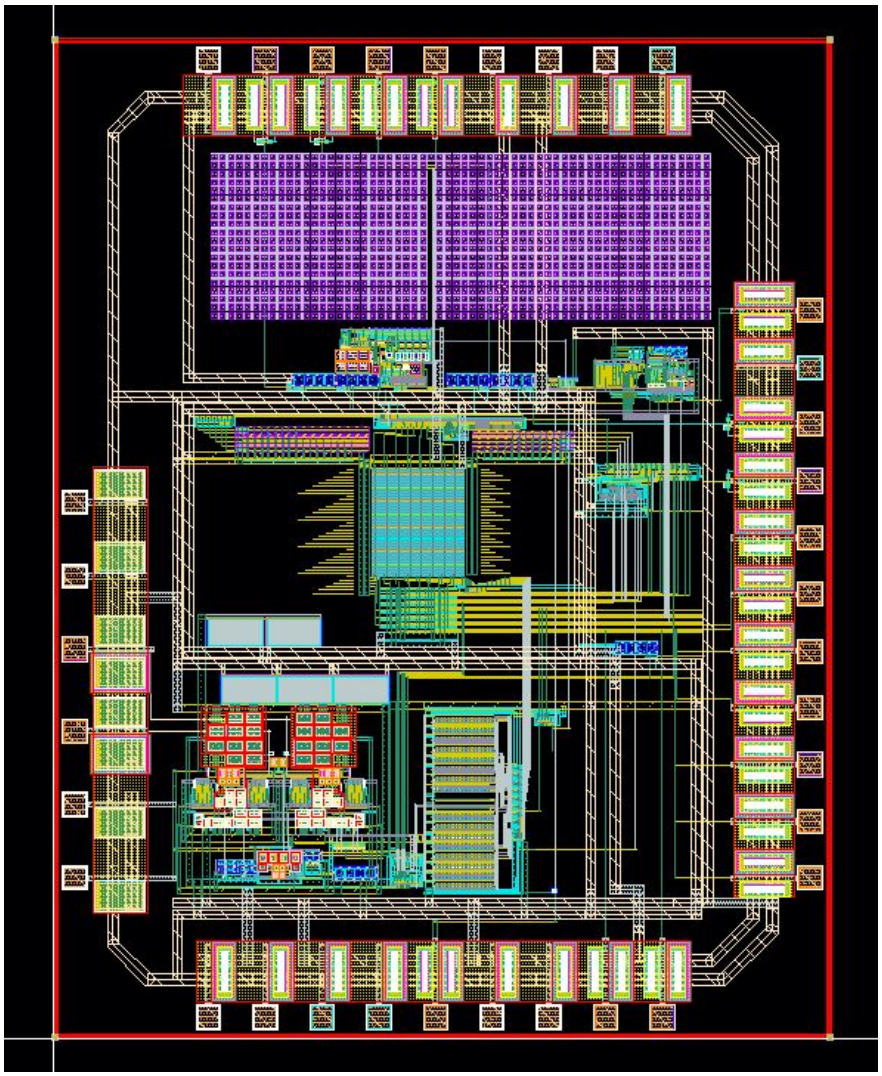


Figure 3.46: Layout of core chip.

Chapter 4

Design of Supply Chip

4.1 Supply chip overview

This chapter describes the design of the supply chip. The function of the supply chip is to generate five different supply voltages and one reference current to power the core chip. This chip is also designed and fabricated using the TSMC 180nm BCD G2 process.

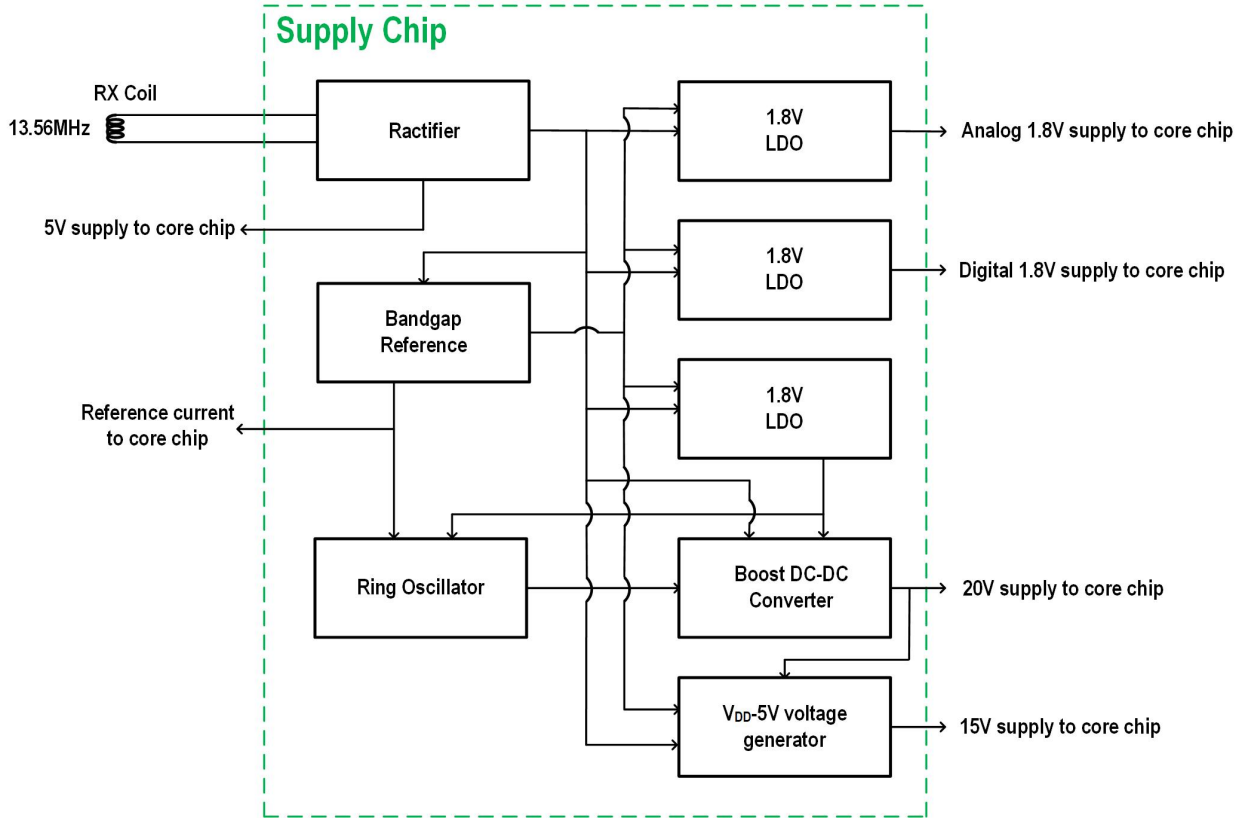


Figure 4.1: Block diagram of supply chip.

The block diagram of the supply chip shown in Fig. 4.1 contains 6 major building blocks: One rectifier, one bandgap reference, three low drop-out voltage regulators (LDOs), one ring oscillator, one boost boost dc-dc converter, and one V_{DD}-5V voltage generator. The ac power received wirelessly through the RX coil is rectified to about 5V dc, which is then applied to the LDOs to generate the 1.8-V low-voltage supply. This rectified voltage is also boosted to 20V to generate the 20-V high-voltage supply, with the 15-V power supply derived from the 20-V supply using the V_{DD}-5V voltage generator. The reference voltages and currents used

everywhere on the chip are generated by the on-chip bandgap reference.

The bandgap reference, LDO and V_{DD}-5V voltage generator blocks were designed by the author, with other blocks designed by another member of the research group. In this chapter, the three blocks designed by the author will be described in detail.

4.2 Design of the bandgap voltage reference

The supply chip includes an internal reference voltage for the LDOs and V_{DD}-5V voltage generator. This reference voltage should a maintain constant value across PVT conditions.

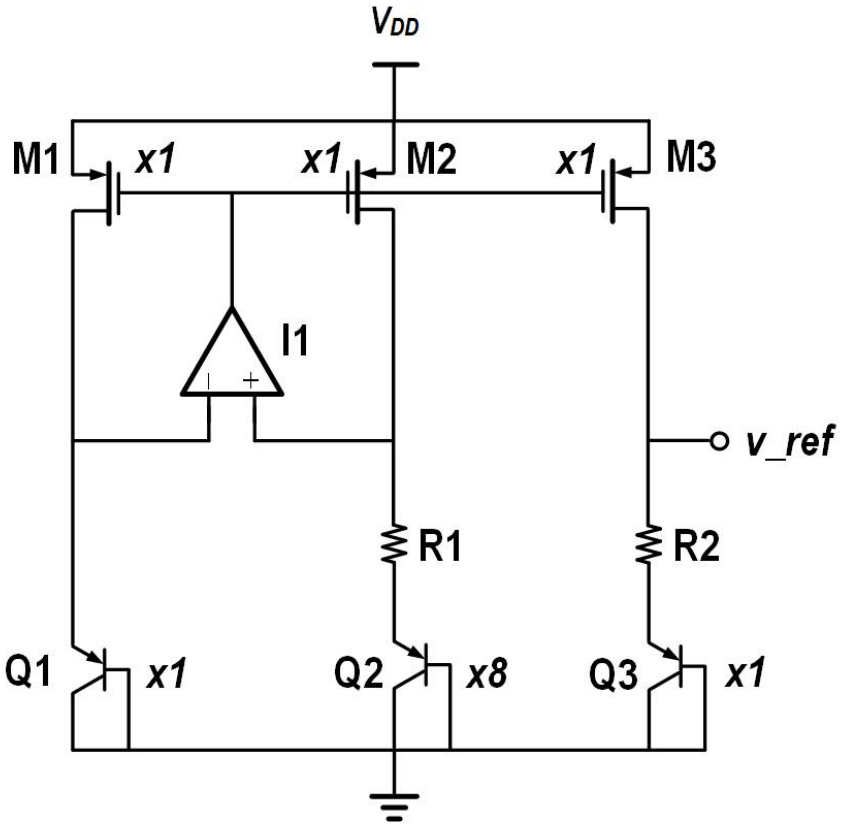


Figure 4.2: Bandgap voltage reference.

The schematic of the bandgap voltage reference circuit is shown in Fig. 4.2. This is the classical bipolar-junction transistor based bandgap voltage reference circuit. The bipolar-junction transistors are the low-voltage vertical PNP transistors available in the TSMC180nm BCD G2 process, where transistors Q1 and Q3 consist of one unit cell while transistor Q2 consists of 8 unit cells. The dimensions of M1, M2 and M3 are identical. This circuit itself includes a feedback network, with the dominant pole placed at the output of the operational amplifier, providing a phase margin of about 85° at the typical process corner. The layout of the bandgap reference circuit is critical to its performance, the transistors Q1, Q2 and

Q3 are laid out in a common-centroid manner as shown in Fig. 4.3, the cell QD represents a dummy transistor.

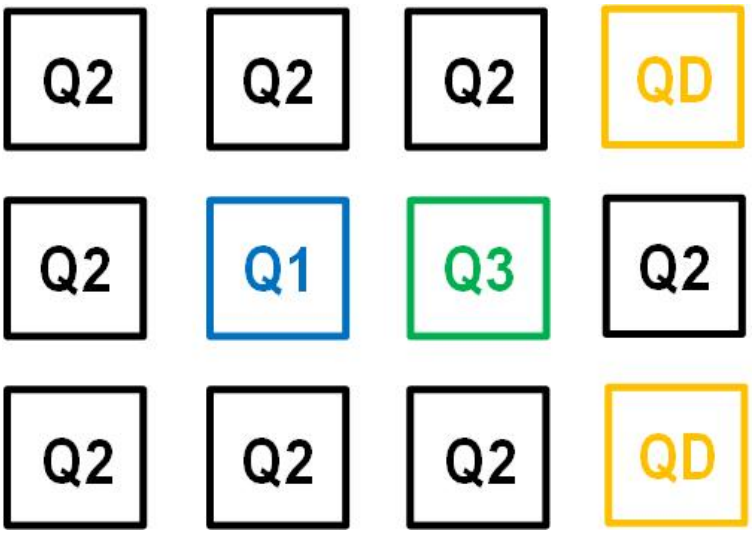


Figure 4.3: Bandgap voltage reference layout.

The expression for v_ref is shown in Eq. 4.1 [16], where V_{BE3} is the base-emitter voltage of transistor Q3, and this term has a negative temperature coefficient. V_T represents the thermal voltage, which has a positive temperature coefficient. With the resistance ratio of R_2/R_1 properly chosen, the temperature coefficient of v_ref can be set to approximately zero across the temperature range -20°C to 65°C. For this design, resistor values R_1 and R_2 are set to 6.13kΩ and 54.17kΩ, respectively, which gives $v_ref = 1.25$V at 36°C. Simulation result shows that the variation of this generated reference voltage over PVT conditions is within ±3%.

$$v\_ref = V_{BE3} + \frac{R_2}{R_1} V_T \ln 8 \tag{4.1}$$

4.3 Design of the bandgap current reference

In addition to the bandgap voltage reference, a bandgap current reference circuit, shown in Fig. 4.4 is also needed. Its purpose is to generate a reference current, used to bias the ring oscillator in the supply chip and also used in the core chip, that is insensitive to PVT variations.

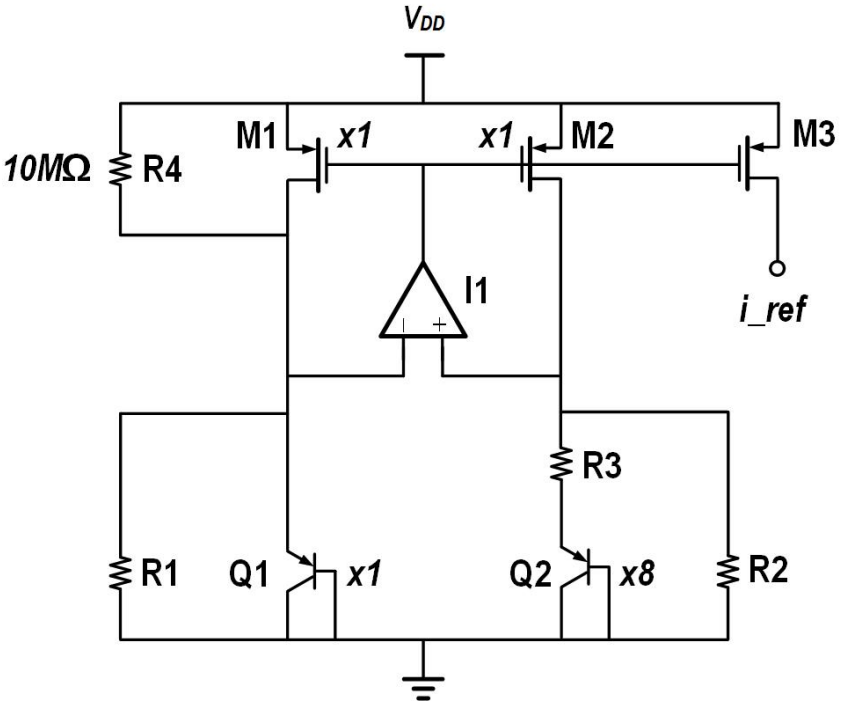


Figure 4.4: Bandgap current reference.

Similar to the Fig. 4.2 bandgap voltage reference, transistor Q1 consists of one unit cell while Q2 consists of 8 unit cells. Resistors R1 and R2 are identical and are placed in close proximity in layout for better matching. The value of resistor R4 is about 10MΩ; its purpose is to ensure start-up of this circuit over PVT conditions. The transistors of M1, M2 are identical, the length of transistor M3 is same as that of transistor M2, the width of transistor M3 is sized such that the output reference current i_ref is about 5μA. Similar to the Fig. 4.2 bandgap voltage reference, the dominant pole is placed at the output of the operational amplifier. Similar to the bandgap voltage reference circuit, the layout of the

bandgap reference circuit is also critical to its performance, the transistors Q1 and Q2 are laid out in a common-centroid manner as shown in Fig. 4.5.

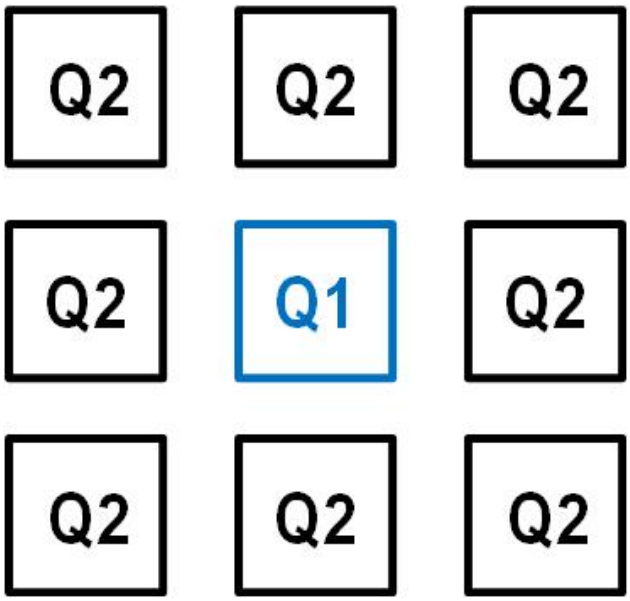


Figure 4.5: Bandgap current reference layout.

The expression for i_ref is shown in Eq. 4.2 [16], where V_{BE1} is the base-emitter voltage of transistor Q1, and this term has a negative temperature coefficient. V_T represents the thermal voltage, which has a positive temperature coefficient. The resistance terms R_2 and R_3 have negative temperature coefficient since p+ poly resistor were used in this design. W_2 and W_3 represent the width of transistor M2 and M3 respectively. With the resistance of R_2 and R_3 properly chosen, the temperature coefficient of i_ref can be set to approximately zero across the temperature range -20°C to 65°C. For this design, resistor values R_2 and R_3 are set to 45.3kΩ and 6.13kΩ, respectively, which gives $i_ref = 5\mu$A at 36°C. Simulation result shows that the variation of this generated reference voltage over PVT conditions is within ±5%.

$$i\_ref = \frac{W_3}{W_2}\left(\frac{V_{\mathrm{BE1}}}{R_2} + \frac{V_T \ln 8}{R_3}\right) \tag{4.2}$$

4.4 Design of the LDO regulator

Since the majority of the circuits in the core chip operate with stable 1.8-V power supplies, the best solution is to implement two LDOs - one for analog and one for digital on the supply chip. They are derived separately because it is critical to separate the digital switching noise in the digital circuits from the quiet analog circuits.

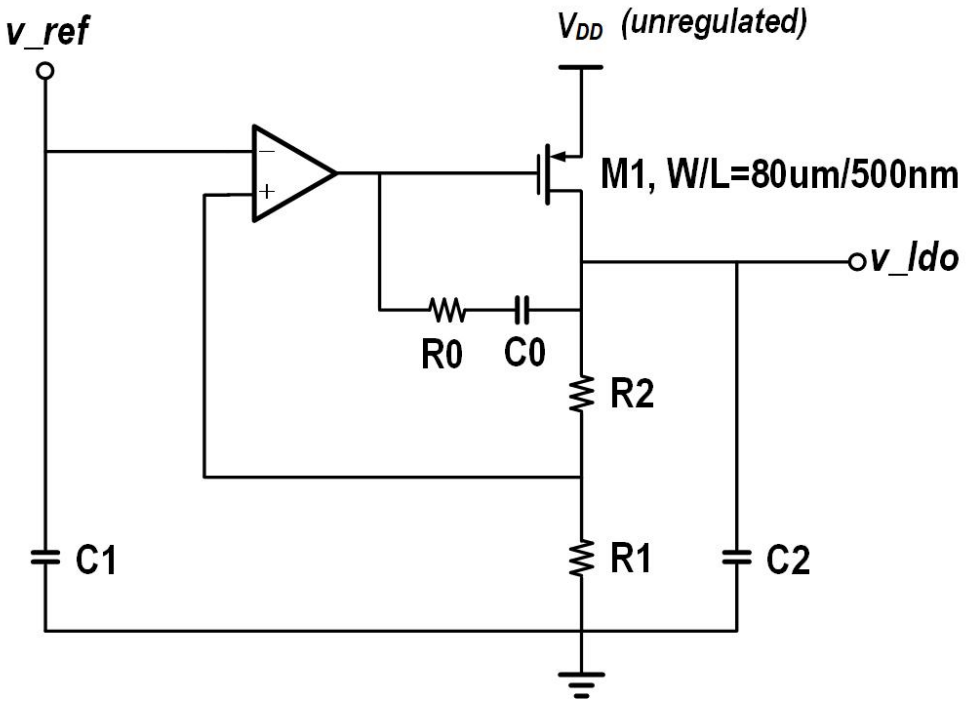


Figure 4.6: LDO.

Fig. 4.6 shows the schematic of the LDOs designed and used in the supply chip. The unregulated power supply V_{DD} comes directly from the output of the rectifier, and can vary between 3.5V and 5.5V depending on the coupling of the two wireless power transfer coils. Transistor M1 is the second stage of the LDO, it provides additional gain and is sized to provide a 10-mA dc output current. The design of the single-stage operational amplifier used in this schematic is explained in the last section of this chapter.

The LDO itself contains a feedback loop, components R0 and C0 form the Miller compensation circuit, after compensation, the dominant pole of this feedback loop is always at the

output node of the operational amplifier, its phase margin is greater than 60° under all PVT conditions. Capacitors C1 and C2 serves as decoupling capacitors, with capacitor C1 used to filter out high-frequency noise coupled to v_ref, and capacitor C2 used to filter out high-frequency noise coupled back to v_ldo during operation. The output voltage can be calculated with Eq. 4.3.

$$v\_ldo = v\_ref \frac{R_1 + R_2}{R_1} \tag{4.3}$$

Resistor values R_1 and R_2 are set to 35.8KΩ and 17.5KΩ respectively, which gives v_ldo=1.8V. The dc output resistance R_{out} can be calculated using Eq. 4.4.

$$R_{out} = \frac{1}{g_{m1}A} \| (R_1 + R_2) \| r_{o1} \tag{4.4}$$

where g_{m1} is the trans-conductance of the transistor M1, A is the small-signal gain of the operation amplifier at dc, based on the simulation results, when the output current is about 1.8mA, A is approximately equal to 57dB, R_{out} is about 0.8Ω.

4.5 Design of the V_{DD}-5V voltage generator

With the advancement of power electronics, monolithic implementations of power converters designed with high-voltage CMOS BCD process have become prevalent. However; due to the limited gate-to-source maximum operating voltage in this process, typically 5.5V. To fully turn on the high-voltage PMOS transistor used as a switch, it is always necessary to bias the gate of the high-voltage PMOS transistors at a voltage that is equal to the supply voltage (e.g. 20V for the core chip) minus a safe source-to-gate operating voltage (e.g. 5V which is slightly less than the maximum operating voltage). Since this bias voltage is supplied to the gate of the high-voltage transistors, the voltage source does not need to provide any dc current; however, this voltage needs to be accurate with minimal variation over PVT. This section elaborates on a circuit that can accurately generate this bias voltage for the core chip.

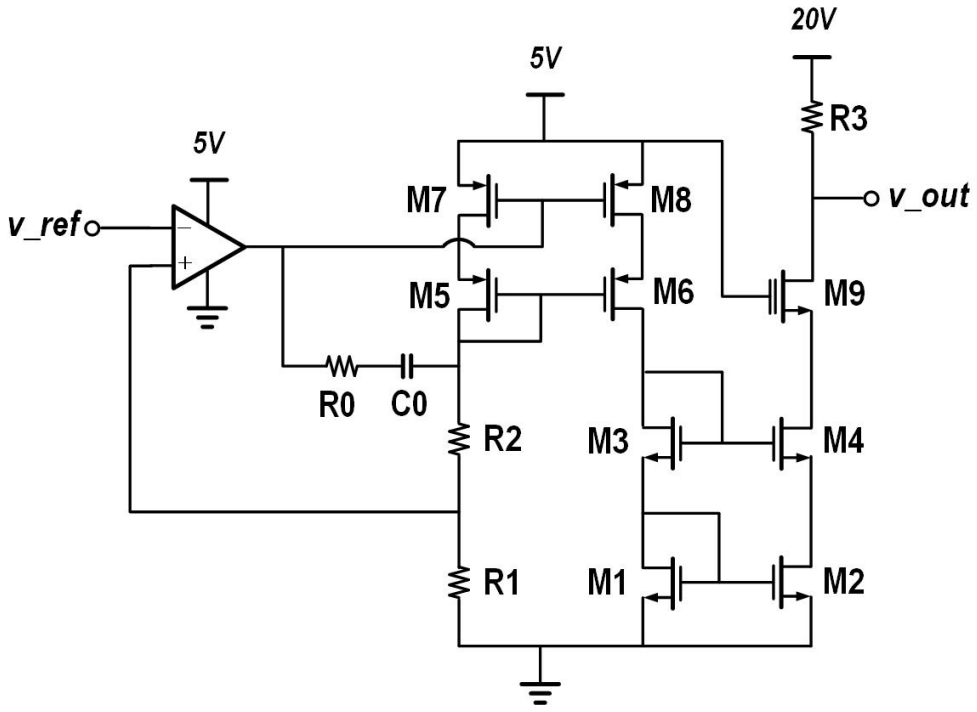


Figure 4.7: $V_{DD} - 5V$ generator.

The proposed circuit is shown in Fig. 4.7, where v_ref=1.25V is the reference voltage gen-

erated from the bandgap voltage reference circuit. The 5-V and 20-V supply voltages are derived from the outputs of the rectifier and boost dc-dc converter, respectively. As shown in the schematic, transistors M1 - M4 and M5 - M8 form a pair of unity-gain current mirrors. Transistor M9 is a high-voltage NMOS transistor, whose gate-to-source maximum operating voltage is limited to 5.5V while its drain-to-source maximum operating voltage is 28V. Components R0, C0 form the Miller compensation circuit used to ensure the stability of this feedback loop, with this compensation circuit, the dominant pole of this feedback loop is always at the output node of the operational amplifier and its phase margin is greater than 60° under all PVT conditions. The relationship between v_out and v_ref follows Eq. 4.5.

$$v\_out = 20V - v\_ref\frac{R_3}{R_1} \tag{4.5}$$

Assuming v_ref=1.25V, $R_3 = 4R_1$, then v_out=15V. If resistors R1 and R3 are placed in close proximity in the layout and the current mirrors are sufficiently accurate, then the voltage drop across R3 is always very close to 5V over PVT, thereby keeping v_out very close to 5V below the 20-V supply voltage.

4.6 Design of the operational amplifier

The schematic of the operational amplifier used in all circuits in this chapter is shown in Fig. 4.8, the maximum operating voltage of all transistors in the schematic is 5.5V. The input differential pair is constructed using transistors M5 and M6, with a layout meticulously designed for high symmetry. This careful arrangement serves to minimize the DC offset introduced by this stage. The dimensions of the current mirrors realized by transistors M1-M4 and M7-M8 are set such that the current gains are all unity. The aspect ratio of M10 is 8 times of that of M9, and R1 is used to generate a 3μA reference current conducted in M9. This is a single-stage operational amplifier whose dominant pole is placed at the output node. The output of this operational amplifier is rail-to-rail, which ensures that the circuits where this operational amplifier is used in can operate properly with the supply voltage varies from 3V to 5.5V.

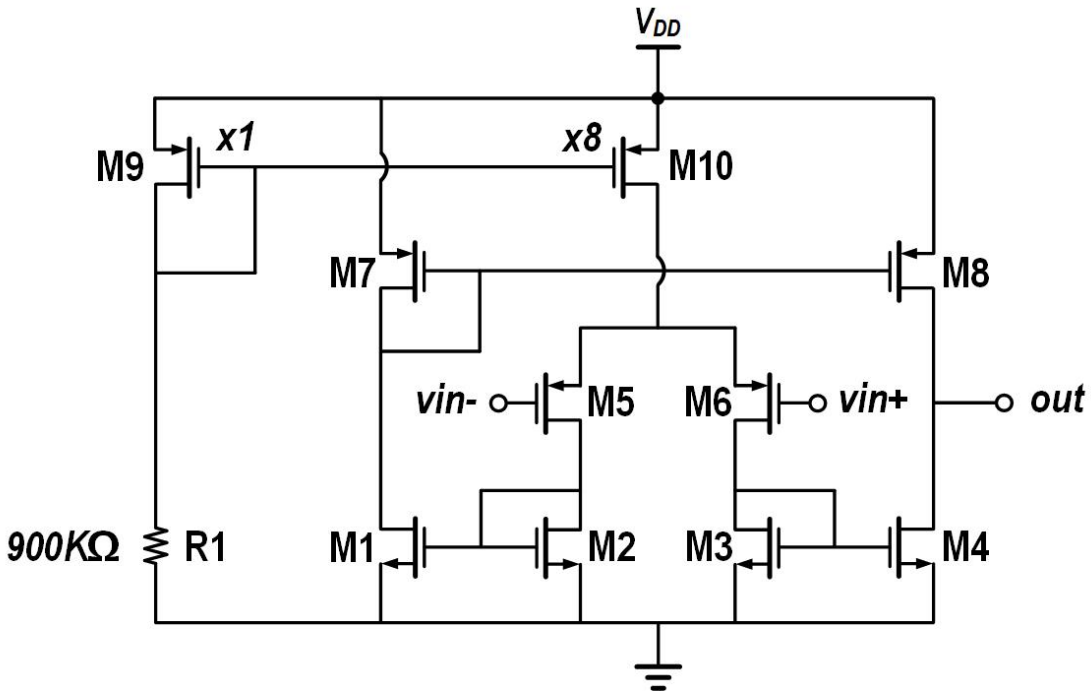


Figure 4.8: Operational amplifier for bandgap reference.

4.7 Layout of the supply chip

Similar to the core chip, the supply chip had also been laid out manually using the Cadenced Virtuoso layout editor tool as shown in Fig. 4.9, Compliance checks for design rules, layout vs. schematic, antenna rule, as well as parasitic extraction, were all performed using the Mentor Graphics Calibre tools. With parasitic resistors and capacitors been included, post-layout simulation shows the chip functions as expected.

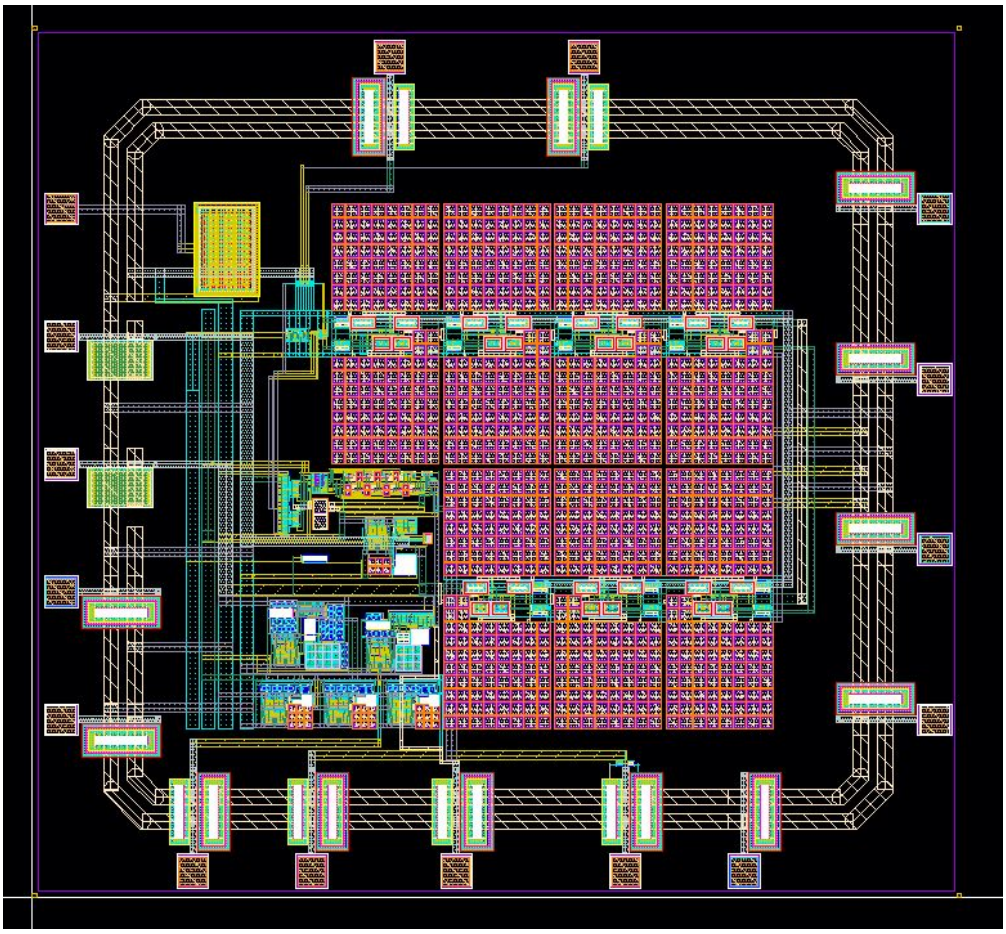


Figure 4.9: Layout of supply chip.

Chapter 5

Measurement

5.1 Measurement setup

The core chip was designed and fabricated using the TSMC 0.18um BCD G2 process. The die photo of this chip, measuring 2.34mm × 3mm, is shown in Fig. 5.1. There is an unused area near the top of the chip due to manufacturing requirements for the multi-project wafers. The digital part of the die photo encompasses the central control unit and the physical realization block for the communication protocol. Decoupling MOS capacitors are used to decouple the digital and analog 1.8-V power supplies.

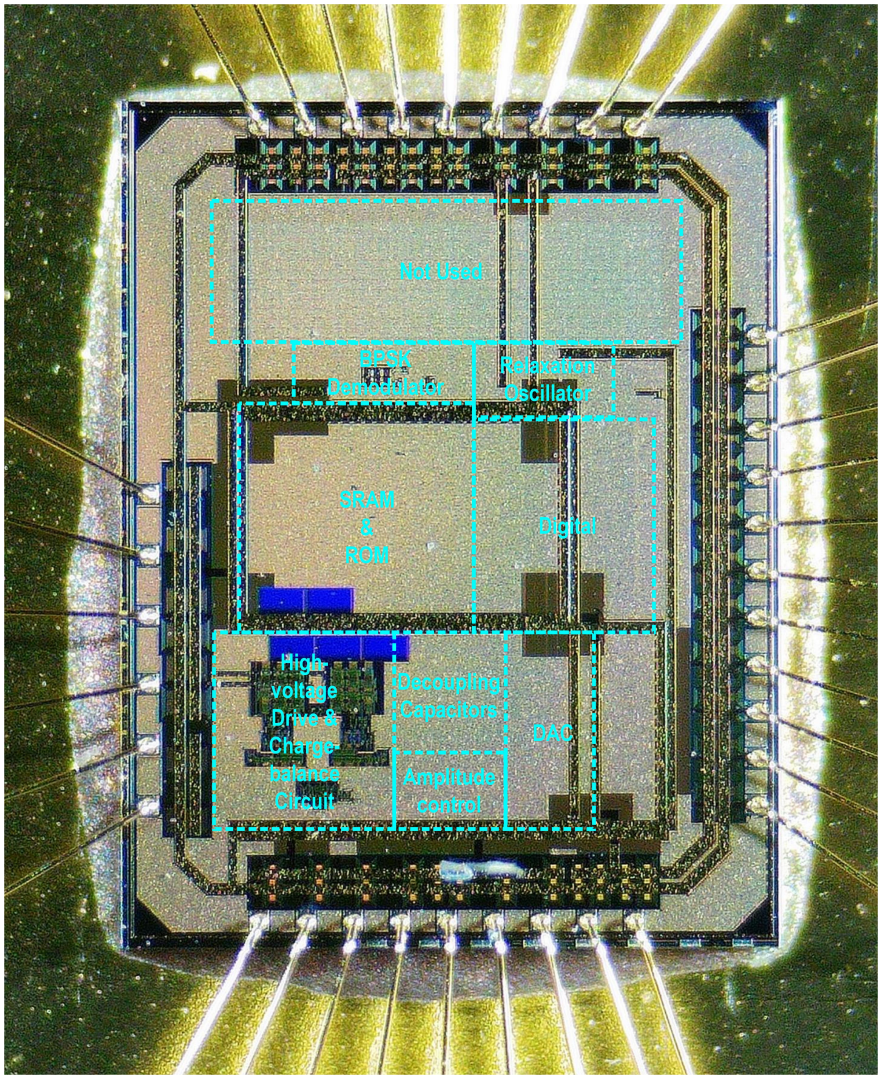


Figure 5.1: Core chip die photo.

The supply chip was also designed and fabricated using the TSMC 0.18um BCD G2 process. The die photo of this chip, measuring 2.13mm x 2mm, is shown in Fig. 5.2. Most of its chip area is taken by the metal-insulator-metal (MIM) capacitors in the dc-dc converter block.

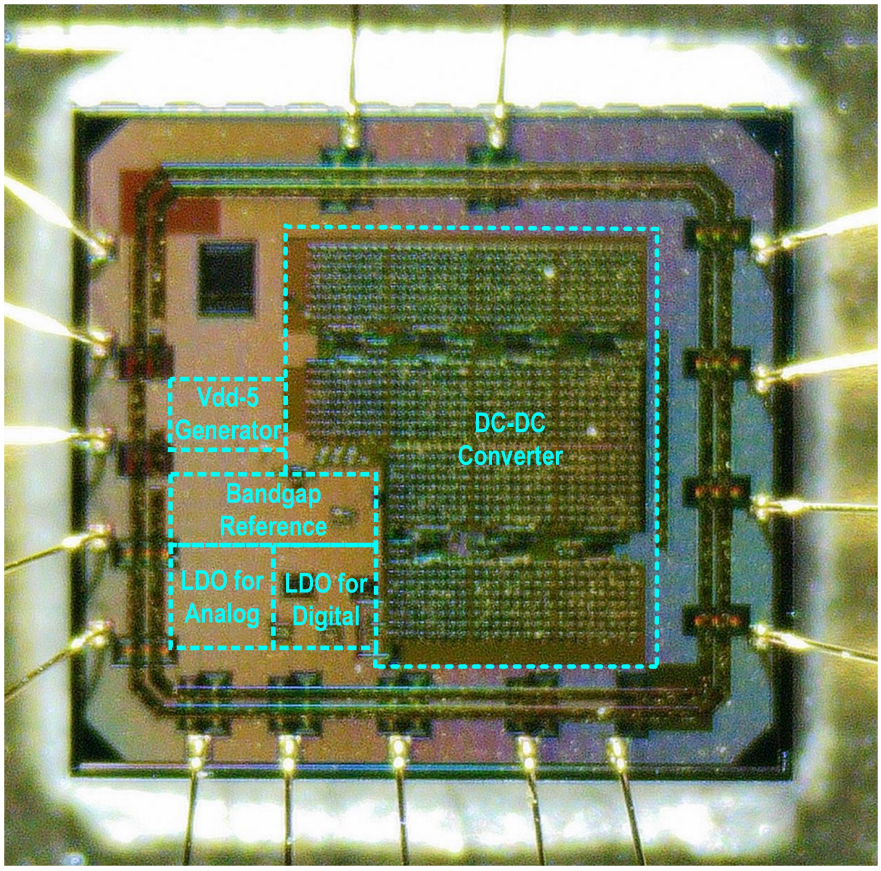


Figure 5.2: Supply chip die photo.

The two chips are directly mounted on two separate printed-circuit boards (PCB) as shown in Fig. 5.3. Wirebond packaging method was used to connect the dies to the outside world. The core chip and the supply chip boards are connected with some jump wires for measurement and probing. The supply chip provides the 5-V, 15-V, 20-V high-voltage supplies, the analog 1.8-V supply, the digital 1.8-V supply, the 5μA reference current to the core chip.

The entire measurement setup is depicted in Fig. 5.4. The Raspberry Pi device serves as the transmitter, transmitting the modulated signal to the core chip. A digital oscilloscope is utilized to probe the differential voltage waveform across the load. The measurements were

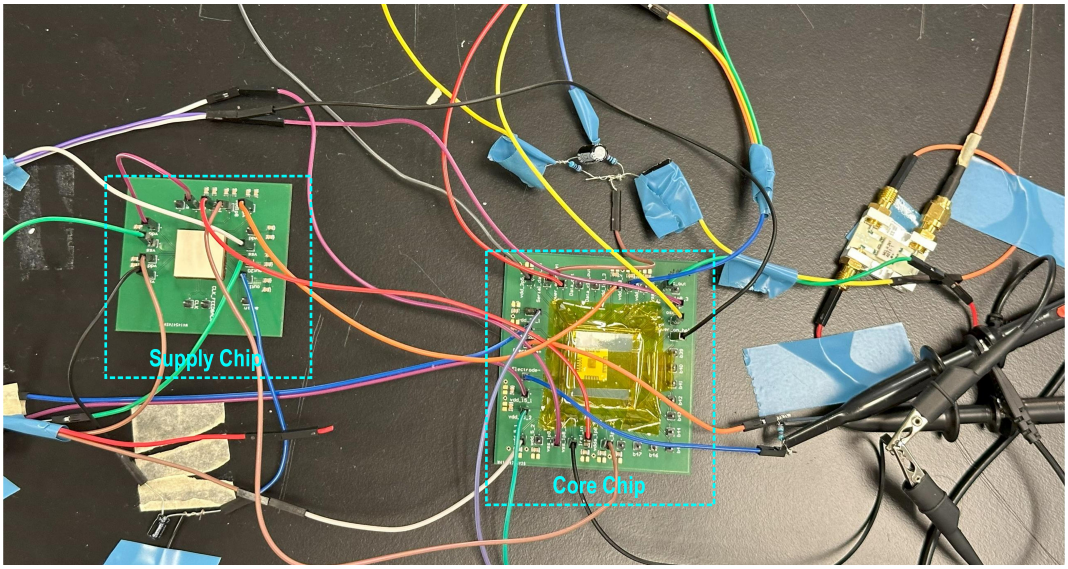


Figure 5.3: Core chip supply chip connected.

conducted using two types of loads designed to mimic human inner-ear tissue: The first load comprises a 3-kΩ resistor in series with a 100-nF capacitor, representing the human inner-ear model; the second load consists of a section of pig-ear tissue.

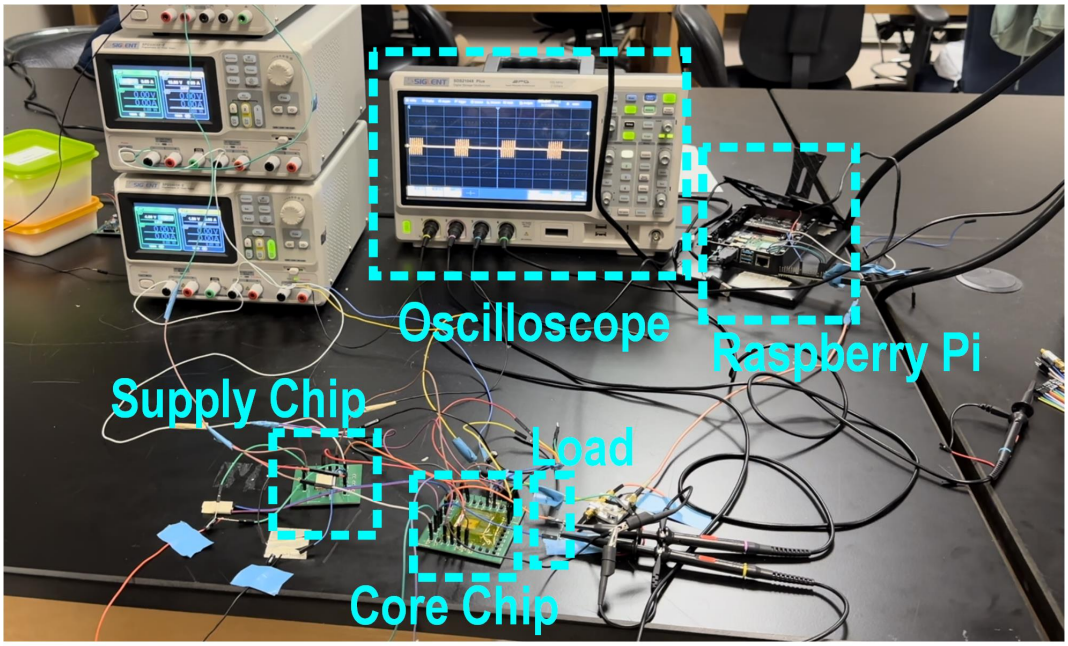


Figure 5.4: Entire measurement setup.

5.2 Measurement results

The total power consumption of the core chip at maximum stimulation mode is 33 mW, with the high-voltage drive and charge-balance block accounting for 99.5%, the DAC for 0.4%, and all digital circuits and other blocks for 0.1%. During the measurement of charge-balance precision, a 3-kΩ resistor in series with a 100-nF capacitor served as the load. The chip was switched from stimulation mode to charge-balance mode, and a multi-meter measured no more than 0.1 mV across the load.

To demonstrate the chip's ability to generate arbitrary current stimulation waveforms with tunable amplitudes, consecutive cycles, and duration of charge-balance time, several measurements were conducted. The oscilloscope captured the differential voltages across the loads.

For the results shown in Fig. 5.5, the load is the series-RC. The top digital signal waveform of each figure shows the associated input digital signals that encode the waveform parameters. The waveform specification is shown in the table associated with each figure. Observing Fig. 5.5 (a), (b), (c), we proved that a variety of wave shapes with different stimulation frequencies can be generated, including a sinusoidal waveform with 100Hz stimulation frequency, a triangular waveform with 1kHz stimulation frequency, and a square waveform with 20kHz stimulation frequency. The number of consecutive simulation cycles for all figures is 7 and the amplitude of all waveforms is 2.5mA. Comparing Fig. 5.5 (d) to Fig. 5.5 (a), the number of stimulation cycles is increased to 15 and the amplitude is reduced to 2mA. For stimulation waveform shown in Fig. 5.5 (e), its amplitude and stimulation frequency is same as that shown in Fig. 5.5 (b); however, its charge-balance duration is twice of that shown in Fig. 5.5 (b). Comparing Fig. 5.5 (f) to Fig. 5.5 (c), its number of cycles is increased to 15 and its amplitude is reduced to 2mA.

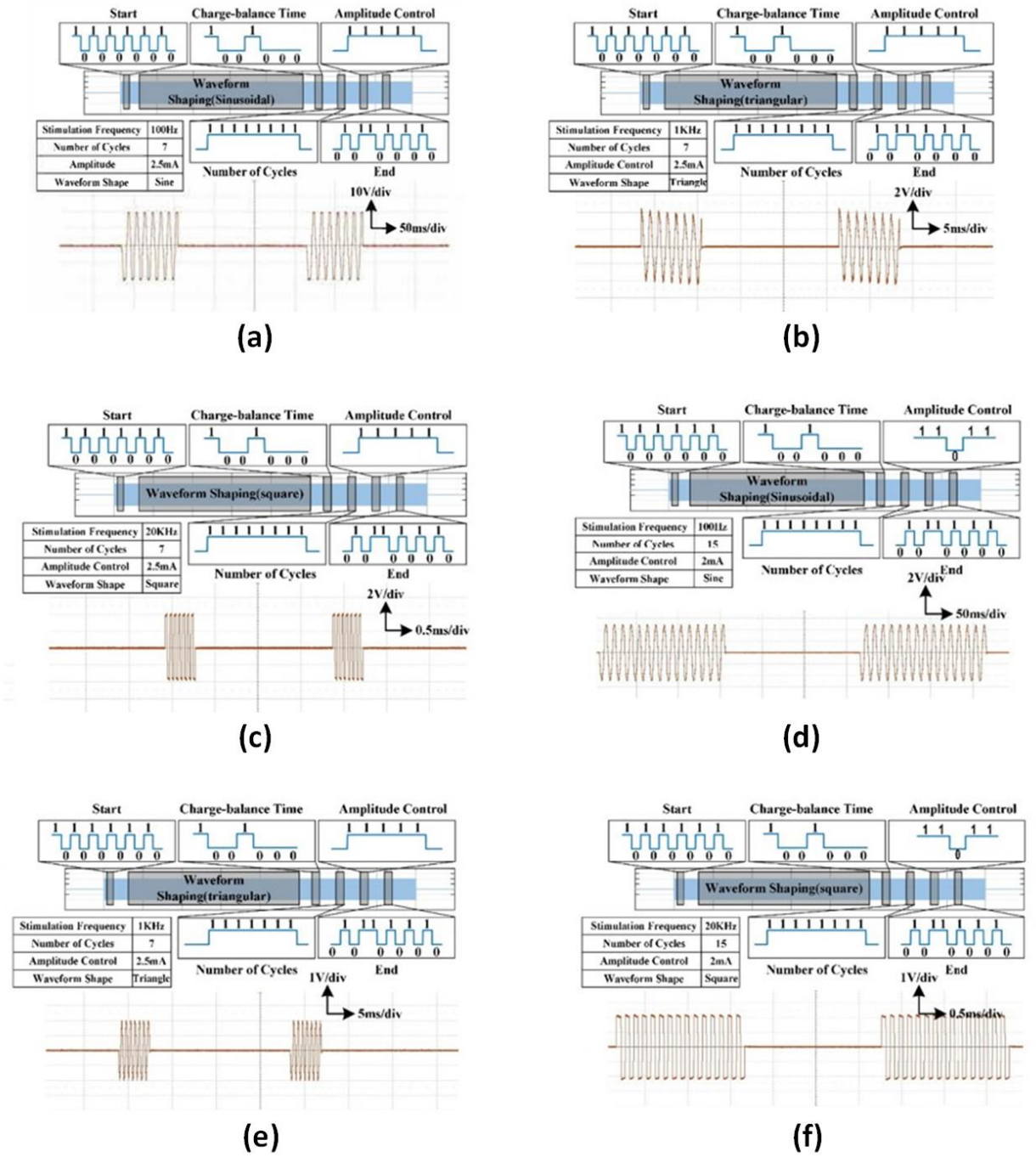


Figure 5.5: Measurement results with RC load.

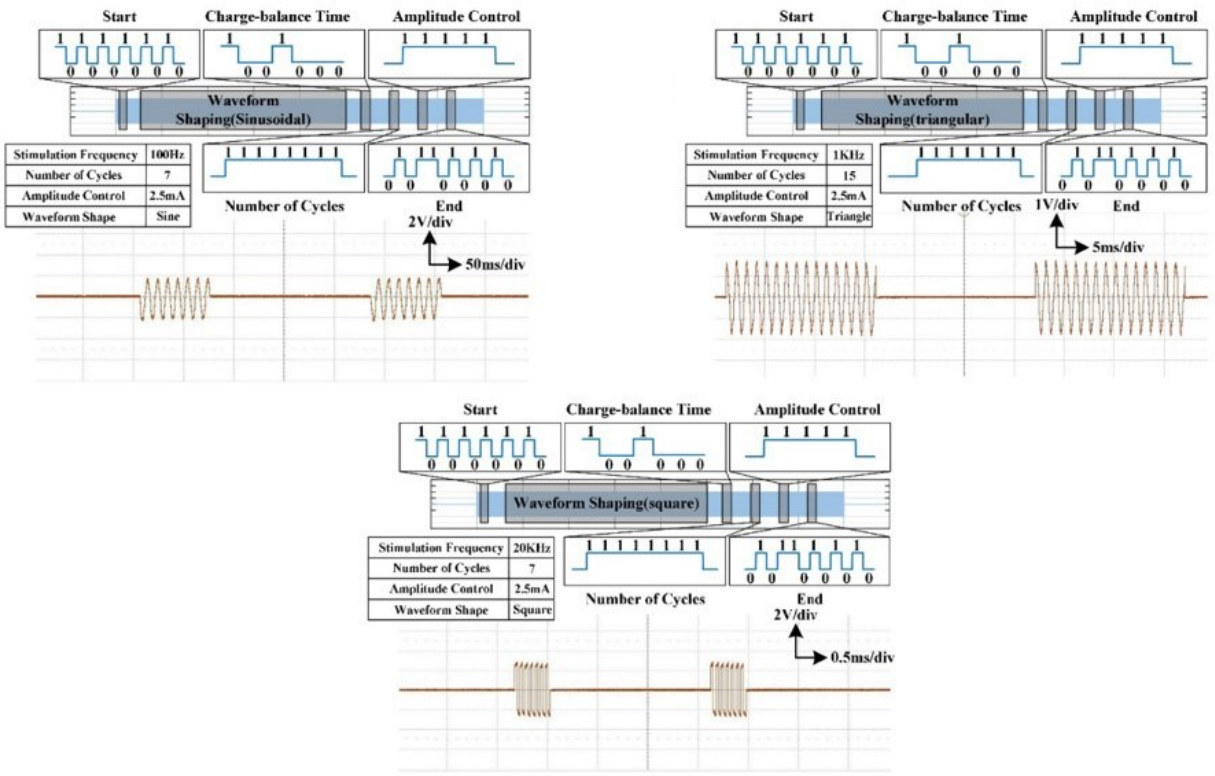


Figure 5.6: Measurement results with pig-ear load.

Fig. 5.6 shows the measurements with pig-ear tissue load. In this figure, three representative waveforms are shown, namely, sinusoidal, triangular, square. With these measurements, we proved that the chip has enough driving capability to the real pig-ear tissue. Comparing Fig. 5.5 to Fig. 5.6, it can be observed that the impedance of the pig-ear tissue is lower than that of the human inner-ear series-RC model. These measured waveforms confirm the effectiveness of the proposed design under varying loads, the ability to program the current stimulation waveform, and the charge balance period.

Comparison of this work with prior works is shown in Table 5.1. The chip performs extremely well considering the charge-balance precision when comparing with prior works; this is as expected thanks to the novel high-voltage drive and charge-balance circuit.

Table 5.1: Comparison of This Core Chip with Prior Works

Reference	Number of Channels (N)	Maximum Stimulation Current(mA)	DAC Resolution (bits)	Charge Balance Method	Charge Balance Precision(mV)	Voltage Compliance (V)	On-Chip Control Circuit	Implemented On-chip Memory
[17]	1	3	4	DCM+Passive	±9	12	No	No
[18]	6	10	9	OR	±20	49	No	Yes
[19]	1	5.12	9	IPCC+OR	±20	22	No	No
[20]	8	0.775	5	CPI	±50	4	Yes	No
[21]	1	0.2	-	No	-	1	No	No
[12]	16	12.75	8	TBCB	±2	40	No	No
This Work	1	1.25	8	Passive	±0.1	20	Yes	Yes

A standalone evaluation of the supply chip was conducted to assess its performance. Seven assembled chips were measured at room temperature. The measurement indicates that the bandgap voltage reference, bandgap current reference, LDOs, and the V_{DD}-5V voltage generator all operate as expected. Furthermore, the voltage and current accuracy of all seven chips fall within the designed ±3% variation.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

An integrated solution has been proposed for the treatment of tinnitus, which may revolutionize therapy options with its convenience and effectiveness. This innovative approach empowers clinicians to administer tinnitus treatment directly within their office settings, eliminating the requirement for cumbersome equipment and streamlining the therapeutic process for patients.

The comprehensive capabilities of this solution have been demonstrated through meticulous measurement and analysis, affirming its reliability and performance. Notably, the solution demonstrates the capacity to produce customizable arbitrary current stimulus waveforms with an impressive amplitude of up to 1.25 mA, providing clinicians with unparalleled flexibility in tailoring treatments to individual patient needs.

Furthermore, the incorporation of a cutting-edge charge-balance circuit represents a significant advancement in precision medicine for tinnitus treatment. This novel circuitry facilitates the precise removal of residual charge from the inner ear with an extraordinary precision level of ± 0.1 mV, ensuring optimal therapeutic outcomes while minimizing potential side effects.

By offering a seamless and efficient approach to tinnitus therapy, this integrated solution not only enhances the quality of patient care but also represents a significant leap forward in the field of auditory medicine. Its accessibility and effectiveness promise to alleviate the burden of tinnitus for countless individuals, marking a pivotal milestone in the ongoing pursuit of improved treatments for this prevalent condition.

6.2 Future work

The successful fabrication of our current chips, following the taping-out process, has validated our innovative concept. Looking ahead, our future endeavors are poised to elevate our project to new heights. We have outlined a comprehensive plan to enhance our chip design, leveraging flip-chip pads and employing the full-block type-out service. Additionally, we are incorporating specialized processes to manufacture the MCM board, which will serve as the foundation for integrating our chips.

Our vision includes mounting the two chips onto the MCM board, a critical step that will pave the way for seamless functionality and enhanced performance. To ensure the highest standards of safety and reliability, we are committed to packaging the entire module in a specialized medical-graded silicon package. This meticulous approach underscores our dedication to delivering a product that meets stringent quality standards and regulatory requirements.

As we progress toward clinical validation, we are embarking on a pivotal phase of our research journey. Live animal experiments, specifically conducted with pigs, will provide invaluable insights and data to validate the efficacy and safety of our device. These experiments will serve as a crucial precursor to human trials, guiding us in refining our approach and addressing any potential challenges.

With promising results from animal experiments, our ultimate goal is to advance to human trials and seek approval from the Food and Drug Administration (FDA). This pivotal milestone represents a culmination of years of dedication, research, and collaboration. By navigating the regulatory landscape and adhering to rigorous standards, we are poised to bring our transformative technology to market, ultimately improving the lives of patients suffering from the debilitating effects of our target condition.

In summary, our strategic roadmap encompasses a comprehensive approach to advancing our technology from concept to commercialization. Through meticulous planning, rigorous testing, and unwavering commitment to excellence, we are confident in our ability to revolutionize the field and make a meaningful impact on patient care.

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