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Athermal Laser Designs on Si and Heterogeneous III-V/Si_3N_4 Integration

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

Jock Trevor Bovington

Committee in Charge:

Professor John E. Bowers, Chair

Professor Daniel J. Blumenthal

Professor Larry A. Coldren

Dr. Richard Jones

September 2014

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Professor John E. Bowers, Committee Chairperson

September 2014

Athermal Laser Designs on Si and Heterogeneous III-V/Si_3N_4 Integration

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by

Jock Trevor Bovington

I dedicate this dissertation to all the
teachers of my life, most notably my family,
especially my wife Ana.

Acknowledgements

The life-long process of education is like a journey into the wilderness. You start at your home learning from those closest to you. Together you plan, discuss, and forecast. Eventually, you must leave with all of the supplies that your friends, family, and you can pull together. Supplies you all think would be helpful given the wisdom of your community's collective experience. If you're lucky, someone you meet will join you for a time, but in the end we all take our own path.

Some start with more, some with less. Most bring a map and a compass to guide their way, but the further you go the less value they have. Maps have borders and compasses mean little without a reference. In the wilderness, you must benefit from the guidance of your fellow travelers and your intuition. In the end, the attitude with which one undertakes their expedition matters more than the goods and skills they set out with.

Special thanks to my family, for providing such a wonderful home to grow up in; the town of Helena, for teaching me the meaning of community; my teachers, for challenging me; especially Prof. John Bowers, for providing a place for both my idealism and pragmatism; my committee as a whole, for all of their contributions in building the environment at UCSB and Intel where I could grow; my friends, for sharing their experiences and dreams with me; and most especially my wife, Ana, who joined me in my journey at the beginning of graduate school and has

been by my side the whole time. Even when we needed to explore our own paths and meet further down the road.

As I stand on the border of the last map I have in my possession, I would like to thank my fellow travelers and the intuition I have gained from their collective wisdom. It is time to draw my own map and build new relationships on this journey into the wilderness.

Curriculum Vitæ

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[1] J. F. Bauters, J. E. Bowers, **J. T. Bovington**, M. R. J. Heck, M. L. Davenport and D. J. Blumenthal, "Integration of Ultra-low loss and active silicon waveguide layers."

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Abstract

Athermal Laser Designs on Si and Heterogeneous III-V/Si_3N_4 Integration

Jock Trevor Bovington

This dissertation presents each component of and a path towards heterogeneously integrated GaAs type III-V lasers bonded to Si_3N_4 passive waveguides on silicon, targeting visible integrated photonics on silicon. A continuous-wave Fabry-Pérot laser, tapered mode converters from III-V to Si_3N_4, and Si_3N_4 sidewall distributed Bragg reflector elements, all made with an integrable process flow, are demonstrated to prove this principle. The goal of this integration is to combine electrically pumped InGaAs multiple quantum well (MQW) active material with low-loss, spectrally wide-bandwidth waveguides to enable compact, novel photonic integrated circuits.

An additional benefit with Si_3N_4 is its lower thermal drift relative to silicon. Additionally, demonstrations of TiO_2 based guides with $\sim pm/K$ thermal drift are presented to explore the possibilities of athermalized waveguides on silicon. Both TiO_2 core and clad waveguides are studied, and new materials information on amorphous sputtered TiO_2 are reported. As integration with such waveguides could open opportunities for novel athermal lasers, some passively athermal de-

signs and designs with integrated athermal wavelength references are presented which show the merit of an integrated approach.

As much process development was required to bring all of the device demonstrations presented in this dissertation to fruition, key process developments are highlighted and explained in detail to assist in any similar future developments.

Finally, the vision of heterogeneous integration as an enabler for ultra-broadband photonic integrated circuits beyond existing InP/Si photonic integrated circuits is presented as future work.

Professor John E. Bowers
Dissertation Committee Chair

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Chapter 1

Introduction

This thesis is focused on the heterogeneous integration of the best individual and combinations of photonic materials onto a single platform on silicon. This is a vision shared by many at UCSB, particularly in John Bowers' optoelectronics group, and elsewhere around the world, as evidenced by the large number of publications and conference presentations on the topic in recent years. More recently the funding and focus has shifted toward longer wavelengths in the research community for MIR applications related to molecular sensing and military applications thanks to the intrinsic properties of Si and Ge at these longer wavelengths [2, 3]. Unique to this work is a focus on wavelengths shorter than the bandgap of silicon. For this reason, the standard silicon waveguide designs no longer work below 1.1 μm and a wider bandgap material such as silicon-nitride (Si_3N_4) or titanium-dioxide (TiO_2) must be used for passive circuitry. For active

III-V materials, GaAs based semiconductors are used to demonstrate lasers as they are the key and in many ways most challenging of devices to integrate.

Beyond the discussion of shorter wavelength lasers on silicon, reductions in thermal sensitivity, or athermalization are covered. Applications at all wavelengths are sensitive to temperature, so all of the arguments and measurements presented for telecommunications also apply at short wavelengths and for sensing applications. So, a broader study was made of the reduced thermal sensitivity of TiO_2 waveguides. As III-V devices are not naturally paired with Si_3N_4 or TiO_2 waveguides, the method of integrating the two together requires integration. For this, we propose heterogeneous integration by wafer bonding. A schematic of this structure is shown in Fig. 1.1.

This dissertation specifically is an exploration into new possibilities of heterogeneous integration on silicon. Subjects explored include a path towards integration of GaAs type III-V lasers with Si_3N_4 planar lightwave circuits (PLCs), and the use of TIO_2, an athermalizing core or cladding material, for the purposes of athermal passive circuitry. As athermal waveguide circuits are of particular interest for passively athermalized circuits for optical communications, some tests were conducted at telecommunication bandwidths. Both of these waveguides are capable of higher energy densities and lower losses than silicon and are transparent to wavelengths below the silicon band gap, which is unique to this work. Prior

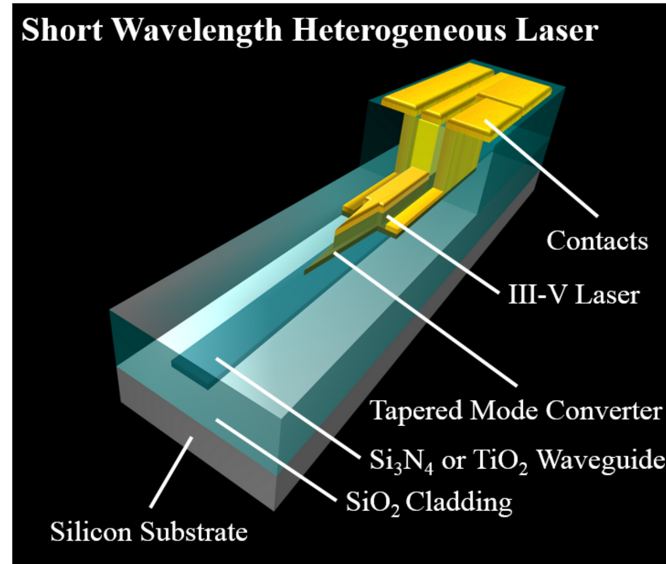


Figure 1.1: Schematic of heterogeneous integration of III-V laser with broadband Si_3N_4 or TiO_2 waveguide. (artwork courtesy of Martijn Heck)

art in heterogeneous integration of III-V and Si has focused on O and C-band [4] and some recent longer wavelength demonstrations [5].

Finally, in exploring both of the topics of III-V on silicon integration and athermalization together, some athermal laser designs are proposed theoretically with the intention of reducing the amount of feedback required in a conventional laser thermal stabilization approach. Unique to this approach, the stabilized wavelength references are integrated rather than relying on an external wavelength locker.

1.1 Background

This work was completed in the context of previous successful heterogeneous integrations which the reader should be aware of. In 2005, Hyundai Park, Alexander Fang and colleagues produced the world's first Hybrid Silicon Laser [6]. This was a heterogeneous integration of III-V InP based gain material on to partially processed silicon photonic circuits using die-scale 300°C O_2 plasma assisted molecular wafer bonding. The term hybrid in this case is different from, but may easily be mistaken with, prior work of photonic "hybridization." Prior hybridization of pre-processed lasers with photonics circuits was commercialized by companies like CIP Technologies (acquired by Hauwei in January 2012) and later by silicon photonics companies like Kotura (acquired by Mellanox in August 2013) and Oracle. These approaches use pre-fabricated III-V devices typically metal-bonded to host circuits similarly to flip-chip bonding. There is an understandable confusion that remains to this day as Intel Corporation, the most visible supporter and developer of III-V/Si technology, has taken on the Hybrid Silicon Laser name into it's marketing that at the time of this writing has gained a great deal of attention within the community. To avoid confusion, this dissertation adopts the nomenclature "heterogeneous" III-V/Si integration used by Aurrion, the company formed by Alexander Fang and Prof. John Bowers to move the technology out of the lab

and into the market. This refers to all technologies that bond III-V mid-process and then use wafer-scale lithographic processes to complete the III-V fabrication.

Heterogeneous, meaning simply "consisting of dissimilar or diverse ingredients or constituents" [7], is an appropriate term for the content of this work as the scope of this work covers a range of concepts and technologies which are made possible by the pairing of two or more different materials, platforms, or concepts.

Further context of this work is the broader and more longstanding emergence of Silicon Photonics, or more accurately the emergence of photonics on silicon whose distinction is made in Section 1.1.1. Briefly, the promise of photonics technology leveraging the investments in time, equipment, facilities, and human knowledge of the CMOS fabrication industrial revolution to make lower cost and higher quality components at previously unseen scales. Scale in terms of both higher volumes and in many cases smaller and simpler devices and packages.

It is through this lens that I have focused my efforts.

1.1.1 The value of photonics on silicon, not just in silicon

The tremendous amount of focus given to Silicon Photonics in the past decade as the platform promising to drive down costs and improve reliability while frequently providing more dense and complex integration. Technical conference presentation rooms have flooded out the doors with eager participants in this tech-

nological shift. The argument I wish to make here, simply stated, is that most of these advantages are not about Si device layers at all, but rather about the use of Si substrate in "CMOS" fabrication facilities with their years of development in equipment and personnel and substantial investment in the facilities themselves. I emphasize that these photonics processes need not necessarily be CMOS processes to leverage the advantages of CMOS.

The photonic technologies presented in this dissertation are not in Si at all, with the exception of TiO_2 clad Si results presented in 2.3, but rather on Si so as to achieve compatibility with Si fabrication facilities. I argue that this approach earns most merits of Silicon Photonics and potentially gains additional advantages by not using Si optical properties. Hence, I will refer to these technologies more broadly as Photonics on Silicon, focusing particularly on III-V Photonics on Silicon.

With regard to the oft-quoted merit of silicon photonics, cost reduction, Table 1.1 provides some economic perspective on the use of silicon-on-insulator (SOI) substrates, the backbone of Silicon Photonics.

Table 1.1: Approximate substrate minimum cost and maximum size [1]

	InAs	InP	GaAs	SOI	Si
Minimum Substrate Cost ($\$/cm^2$)	18.25	4.55	1.65	1.30	0.12
Maximum size (mm)	75	150	200	450	450

As is clear from Table 1.1, using SOI is an order of magnitude more expensive than directly using Si substrates, comparable in cost to a GaAs substrate, and a few times cheaper than InP, though InP and GaAs are not available at the larger sizes of Si and SOI. Therefore, passive elements in SOI, though compact, do not have an inherent cost advantage over conventional planar lightwave circuit (PLC) technology on Si.

Non-silicon waveguides using Si_3N_4 or TiO_2 have broader spectral bandwidth, lower thermal drift, and in many cases lower loss than Si waveguides. These waveguides can be implemented without SOI and therefore can be both lower cost and higher performance.

With regards to active component integration, again the cost of SOI is limiting in some cases. Simple heaters are available in PLCs for phase tuning and advanced circuits requiring lasers and high-speed modulation and detection need not be available in large areas of the PIC's passive elements, such as arrayed waveguide gratings (AWGs). The most-economic design would not be a completely monolithic III-V, nor would it be heterogeneous or hybrid integration of III-V on SOI, it would likely come from a heterogeneous or hybrid integration on bulk silicon that keeps passive elements in well established PLC technology on Si. This type of integration is where the line is drawn between Silicon Photonics and Photonics on Silicon.

1.2 Literature review

This section presents an overview of the prior art in the fields discussed in later chapters. Each subsection corresponds to the different Chapters 2, 3, and 4.

1.2.1 Athermal devices and designs

Managing temperature fluctuations in optical devices is not a new problem, it as old as the field itself and I could fill 100 pages with references on the topic. However, more recently the desire to develop uncooled circuits for silicon photonic devices has reinvigorated efforts to develop new solutions. I therefore focus mostly on silicon photonic efforts with an exception to circuit based schemes as those ideas would apply to many platforms. I will also refer to select non-silicon works as a potential inspiration for the solutions currently pursued on Si.

Packaging based athermal solutions: PLCs on Silicon offer superior passive components for most applications due to the highly reproducible fabrication and the tolerances of working with silica and silicon nitride compared to higher index difference waveguides. Additionally, fiber based gratings are implemented in a number of systems because of the maturity of that technology. Both in-plane and fiber-based solutions are typically dominated by material thermo-optical (TO) behavior in SiO_2. However, there is also a component of their drift with can be

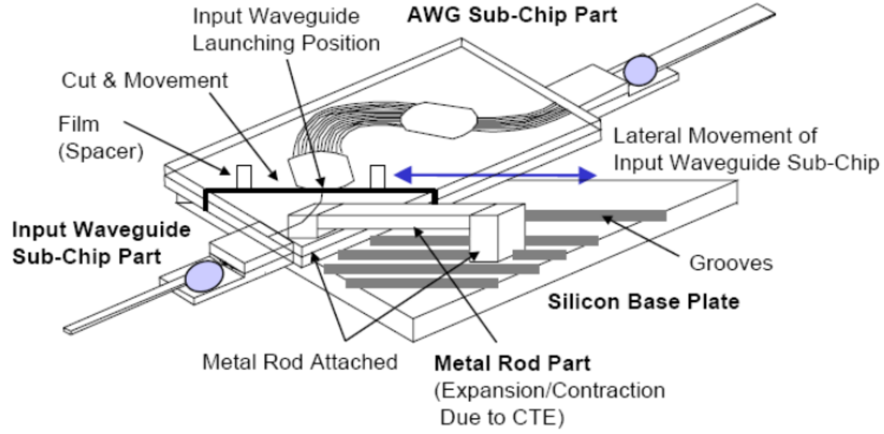


Figure 1.2: Schematic of athermal packaging solution for a conventional AWG. [8].

owed to thermal expansion of the actual optical path length. This is material specific and dominated by SiO_2 cladding in the case of fiber and Si in the case of in-plane devices fabricated on Si. To overcome both the material TO effects

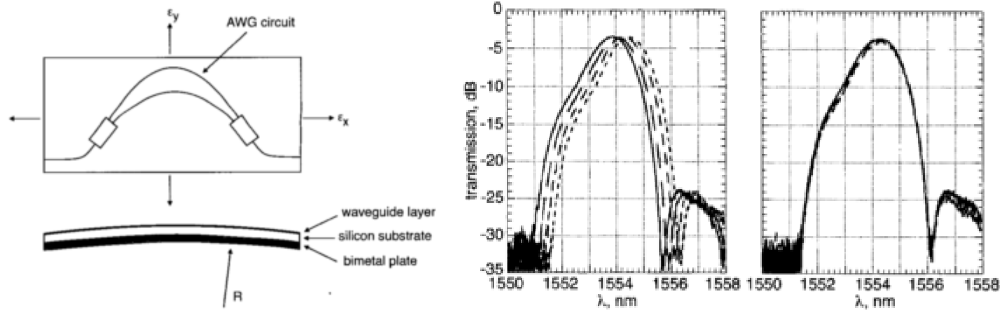


Figure 1.3: Schematic configuration of AWG multiplexer with bimetal plate and the corresponding change in temperature dependent spectral response. [9].

and thermal expansion, products and demonstrations have been made to force the optical path length to remain fixed or even shrink by means of an external

packaging solution shown in Fig. 1.2. In another example, a bimetal "stresser" attached to a conventional device can counteract the waveguide and substrate's natural inclination to both expand and bow, thereby compensating both material TO and path length effects of SiO_2 waveguides with stress as shown in Fig. 1.3.

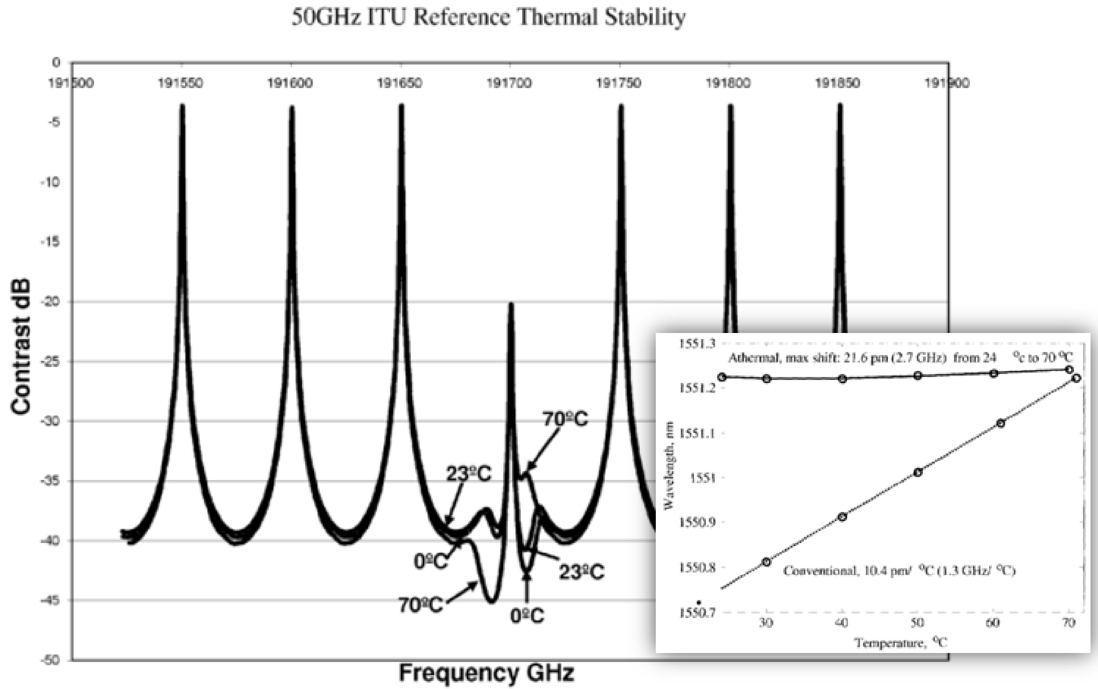


Figure 1.4: Spectral response and temperature dependent Bragg wavelength plots for athermally packaged fiber Bragg grating. [10].

For fiber Bragg gratings (FBGs), attaching the fiber to a single similar bimetal stack is not entirely sufficient, so methods of fixing the gratings to a structure that can be compressed or expanded from the two ends of the grating based on external structures of appropriately balanced thermal expansion coefficients have been implemented and achieve <0.5pm/K up to 70°C shown on Fig. 1.4. Metal

coatings have also been added to sections of fiber adjacent to the FBG and then pinned to a mount of lower thermal expansion than the metal coating. This acts to put strain on the FBG in opposition to it's natural inclination to expand and in opposition to the TOC of the waveguide of the fiber shown in Fig. 1.5.

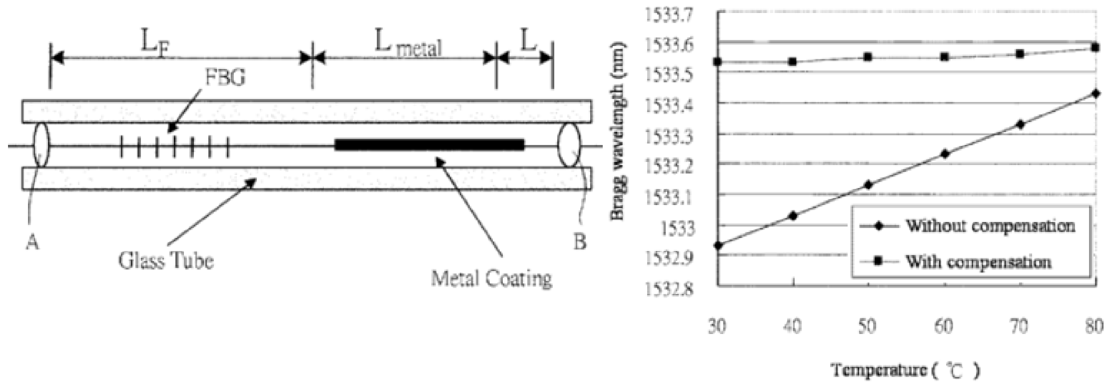


Figure 1.5: Schematic and temperature dependent wavelength response of an athermal packaging solution for a fiber Bragg grating [11].

In summary, there exist packaging solutions based on similar principles to counteract the thermal effects present in optical devices. However, most of these are for a single device and may not scale to a tightly packaged integrated circuit with devices placed in different orientations and locations on the die or consisting of different materials and or varied optical confinement within the same materials. In other words, one packaging solution does not fit all devices in a circuit.

Circuit based athermal solutions: A number of clever circuits based athermal solutions have been implemented, most notably that of an athermal, or temperature insensitive imbalanced Mach-Zehnder interferometer (MZI) filter [12] and

arrayed waveguide grating (AWG) [13]. These function by making the phase difference of the two paths temperature insensitive rather than the entire path itself as with the packaging solution. As these are interferometric devices, their transmission is based on this phase difference and therefore the transmission aptitude remains unchanged if the phase differences are locked over a wider temperature range.

This solution works for finite impulse response (FIR) filters and multiplexers but is not easily translated to infinite impulse response (IIR) rings and Bragg gratings or locking the cavity mode drift in a laser as is discussed more in depth in Sections 2.1.2 and 2.4. For this problem, there is a body of work on finding better materials to overcome thermal drift issues.

Organic materials based athermal solutions: Many polymers show very strong negative thermo-optical coefficients (TOCs) and can, therefore, be used to offset positive TOC materials like III-Vs, Si, and SiO_2. Polymers have been used for top claddings for surface Bragg gratings [14], low index claddings for SiO_2 cores [15], as the core material itself [16], and over cladding for high index SOI waveguides with and without slots ([17], [18], [19], [20]) to enhance confinement in the polymer and in AWGs [21] [22].

However, such polymers suffer from environmental sensitivity and degradation. They often change behavior within oxygen exposure, plasma treatment, UV ex-

posure, humidity and high temperature, and age more rapidly than other part of a product [23]. Understandably, this is not a fair generalization with all polymers for all applications, but it is a common counterpoint to consider when choosing them for your application. Finally, integration of such material into a CMOS facility can be met with resistance as they are not well established and therefore present a risk to existing processes that must be evaluated on a per facility basis.

Inorganic materials based athermal solutions: For this reason inorganic materials, such as TiO_2 discussed in Chapter 2, are under serious consideration for compensation of thermal drift on Si. Ta_2O_5 is another such candidate with a negative TOC [24]. Sputtered TiO_2 as an overcladding for silicon waveguides was first shown by Alipour to significantly reduce thermal drift of a ring [25]. Later demonstrations by [26] & [27] near 1550 nm showed additionally promising results with implementations in Si ring based modulators and for both polarizations.

Some demonstrations were made with TiO_2 as a core material, but they did not focus on the thermal characteristics of these guides [24] [28]. Therefore, no comparisons could be made with the thermal measurements of TiO_2 core waveguides presented in Section 2.2. However, earlier demonstrations of TiO_2 co-deposited with SiO_2 did target athermal behavior and achieved $<1\ pm/K$ [29].

Trimming: Interestingly few of the material based athermalization reports discussed trimming the devices post-fabrication, though nearly all used a ring

structure to characterize the athermal nature of their devices. The narrow resonances in rings, in particular, are very sensitive to fabrication variation. Therefore, a method of tuning to a resonance post-fabrication or as an intermediate fabrication step is vital. This is particularly an issue on silicon as a simple and common tuning mechanize, thermal tuning, would be useless in an off-resonance athermal ring. In silicon, implantation based index tuning has been demonstrated as a potential solution to this trimming problem. Once the index change caused by the defect of the implantation is made, the trimming process can be achieved by some form of local heating to reverse the index perturbation, for example by annealing [30], or locally with a focused laser, for example [31].

Alternatively, a Si_3N_4 top layer to a Si ring can be patterned and etched on a per ring basis in an automated process whereby the partially fabricated ring is tested at wafer level, and then a programmable lithographic step such as electron beam lithography is used as demonstrated in [32,33]. This is more appealing than the implantation process as the additional loss of implantation can be greater than the scattering loss due to surface roughness of the tuned Si_3N_4 over cladding.

In an alternative trimming process, a UV photosensitive As_2S_3 chalcogenide glass partial upper cladding has been deposited on a silicon waveguide. The effective index of the mode can then be trimmed by selective UV exposure of circuit elements. This has been further top clad with a negative TO polymer [34].

This is the ideal case, where a device can both be trimmed and made athermal. We have yet to demonstrate this, but As_2S_3 chalcogenide glass could be used as the upper cladding of the athermal revealed waveguides shown in 2.2. Assuming this proves reliable, this is an excellent future direction for this work.

Higher order effects: One topic also often overlooked by the literature on athermalization of structures in silicon is the higher order TOC of Si itself. Across the functional temperature range of Si for most applications dn/dT_{Si} has been measured to change from $1.85{\times}10^{-4}K^{-1}$ (at $300K$) to $>2.0{\times}10^{-4}K^{-1}$ (at $380K$) [35]. This may seem like a small shift, but athermalizing materials such as polymers also have higher order changes in dn/dT with temperature and in the same direction [22] & [36]. The result can be a strong quadratic resonance drift with temperature, perhaps hidden by the small temperature ranges of many publications. We too witnessed this effect in TiO_2 clad silicon rings tested near 1310 nm and a summary of this finding will be presented in Section 2.3.

1.2.2 GaAs-based devices on Si

Bonding of GaAs to Si: There were some early attempts to transfer InGaAs quantum well active material onto SiO_2 on silicon, similar to the work presented in this dissertation, but without the intention of photonic integration with PLC waveguides. Successful transfers and characterization of these films were made as

early as 1989 and showed that a high material quality could be retained following lift-off and film transfer by use of a hydrophilic van der Waals bond [37]. Later lasers were actually fabricated using spin-on-glass as an intermediate layer [38]. Similar spin on glass bonding was conducted as part of this work at UCSB. However, voids were more numerous and the curing temperature was higher which lead to an increase in bonding related defects, so this process was abandoned in favor of plasma assisted bonding.

The problem of defect migration from the bonding interface was identified early as an issued with all such bonding processes involving substrates with dissimilar coefficients of thermal expansion. It was proposed to add an intermediate layer near the bond interface to reduce this issues as early as 1998 [39]. The details of the most appropriate intermediate layer were not clearly defined at this point, however we discuss work in bonding superlattice structures which have been shown to be highly effective in InP heterogeneous devices in Section 4.2.2.

Electrical interfaces between Si and GaAs have also been pursued, with intermediate layers from metal/solder bonding interfaces [40] and [41], to InP [38] or Sn doped SeS_2 [42]. However, a potentially preferable direct bonding approach has been demonstrated for highly doped p-GaAs to p-Si interfaces and even fabricated into CW quantum dot lasers [43].

Growth of GaAs on Si: Many would argue that growth of III-V material on Si is the best approach and it is therefore an active area of research. Owing to the lattice mismatch of GaAs and Si intermediate layers are also required to achieve quality device material in the grown III-V. These layers either are full of defects themselves making them not desirable optically and/or electrically, or it is made of a narrow band gap material like Ge which would rapidly absorb the light passing through it. There may indeed be a path forward for direct growth of GaAs type material on Silicon Photonics circuits, as performance in this area is continuously improving with very promising QD on Si results coming out of several groups [44], [45]. However, I would argue that the benefit of such growth may first be realized as a low-cost growth substrate for material used in a selective area die bonding approach as discussed in [1]. Again, this need not be to SOI, but could be at shorter wavelengths with a bulk Si PLC carrier with small III-V device areas.

1.2.3 TiO_2 devices on Si

TiO_2 is a wide band semiconductor (>3 eV) which has previously been used for a high-k dielectric in Si transistors. Additional examples of TiO_2 in resistive switching memory devices [46] and as the gate for MOS capacitors [47] show that though it has since been eclipsed by HfO_2 as the gate oxide of choice, it still is a

CMOS compatible material making it a negative TOC material of least resistance for introduction to a CMOS facility.

A fairly detailed process flow for a TiO_2 top clad silicon modulator is provided in [26] including a nice presentation of process conditions for the sputtered TiO_2 and the resulting figures of merit n and dn/dT. Loss data was reported for these waveguides from 1-9dB/cm increasing with decreasing waveguide width. A more direct measurement of similar material was made using a coupled prism propagation loss measurement which found a propagation loss of 0.4dB/cm verifying TiO_2 as a low loss material [24]. These works also made an important observation about the thermal budget of TiO_2. Both attributed significant increases in loss to anatase crystal formation at temperatures as low as 350°C. This matches additional publications on the material characterization of TiO_2 which show first anatase, then rutile crystal transitions with increasing anneal temperatures [48].

1.3 Dissertation overview

The dissertation is broken into three main chapters followed by a conclusion and future work chapter. The following three chapters cover athermalization on silicon; a path towards heterogeneous integration of GaAs type lasers with Si_3N_4

core waveguides on silicon, and finally a chapter on key fabrication developments on this path.

The type of athermalization which this dissertation focuses on is materials-based waveguide athermalization explicitly with TiO_2, as it is semiconductor based CMOS compatible material, with both an index ~ 2.2 or greater at 1550, and a thermo-optic coefficient about as strong as Si, but negative. The type of heterogeneous integration which Chapter 3 focuses on is of InGaAs/GaAsP multiple quantum well lasers grown on GaAs transferred to the SiO_2 partial upper cladding of a Si_3N_4 strip waveguide by low-temperature O_2 plasma assisted bonding for laser integration. Chapter 4 has some details and rationale behind the processing used in this dissertation. Importantly, more than just a process follower both successes and failures, and the insights gained through the development are presented. The final chapter summarizes the findings of this dissertation and gives an outlook for the future.

Chapter 2

Athermal Devices and Designs on Silicon

Thermal stability is an important topic in integrated photonics research. The need for athermal structures is clear for photonics applications from low-cost communications links in data centers, passive optical networks, microwave photonic filters and sensors. The current solutions use either single channels, coarse wavelength division multiplexing (CWDM), temperature stabilizing feedback loops or a power hungry thermo-electric cooler (TEC).

This is an active research area with a number of solutions to address this challenge by designing intrinsically athermal structures. We would classify them into packaging solutions [8, 9, 49], circuit-based approaches [12, 13, 50], and materials solutions. Among the materials solutions, the overwhelming majority have used polymers [22]. Oft-quoted issues with these polymer-based solutions include process compatibility, performance degradation, long-term reliability, and narrowed

operating temperature conditions. Much work to address these concerns continues, and in the end such solutions may be useful. However, titania (TiO_2) has recently been suggested as a CMOS compatible alternative material to polymers for enabling athermal waveguides in photonic integrated circuits [51]. The reason for this is its strong negative material thermo-optic coefficient (TOC) dn/dT. Literature has quoted its TOC in a range of $-(1-6.5) \times 10^{-4}K^{-1}$ partially due to deposition method [26, 51, 52].

This chapter holds application examples, device demonstrations, numerical simulations, and theoretical explorations of using TiO_2 as a CMOS compatible athermalizing material on Si. This type of athermalization has not been demonstrated in other platforms such as InP to the author's knowledge because of the relatively high index of any type of (Al)InGaAs(P) lower cladding compared to negative TO materials. New materials data for TiO_2 are presented with a realistic projection of both the promise and pitfalls of the material. More generally, novel athermal laser designs are presented enabled by athermal waveguides in a heterogeneous III-V on Si platform.

This research is important because the future is moving towards highly integrated uncooled systems. Such integration will not scale or achieve cost targets without the simplicity of athermal design.

We project as much as a 100 fold improvement of spectral efficiency with the use of athermalized circuits over conventional CWDM solutions. Two approaches to achieve this are given. A novel TiO_2 core waveguide is presented with <3 pm/K thermal drift. A simple modification of a silicon rib waveguide by adding a TiO_2 cladding is demonstrated to reduce thermal drift of both gratings and rings at 1300 nm.

2.1 Applications and background for integrated athermal devices

There is a strong desire in a number of fields to develop photonic integrated circuits (PICs) that are *athermal*. What level of thermal insensitivity would be considered athermal is application specific, so the following examples should help illustrate what constitutes an athermal circuit. In general a wavelength selective element such as a multiplexer, ring, or grating is placed in the circuit to isolate one or more particular optical frequencies. Simply put, an athermal circuit should be able to maintain this filter response over a range of temperatures. The nature of conventional PICs is such that waveguides are comprised of dielectrics and semiconductors with positive thermo-optic coefficients on a substrate with a positive thermal expansion coefficient. This tends to cause a drift of all wavelength selec-

tive components to longer wavelengths with an increase in the temperature of the environment. Athermal circuits do not drift and therefore do not need to be held at a single temperature.

2.1.1 Application examples

In sensing applications that use filters targeting particular molecular resonances, a desire to limit or engineer this thermal drift is very clear. For example, when monitoring molecular resonances that shift only slightly with air temperature an athermal circuit would have to have a filter bandwidth equal to the resonance shift across this small range and no more. A conventional (III-V or Si) circuit may require a filter bandwidth of 10-20 nm to capture such a resonance from 0-80 $^{\circ}C$. Its ability to differentiate between molecules would suffer not withstanding the tremendous amount of noise such a wide filter could add to the signal. An SiO_2 based circuit could have as much as an order of magnitude less drift, but this could still be too much for many applications and you would lose the active component integration of III-V or Si. A preferred solution would passively maintain a narrow bandwidth no greater than the thermal drift of the resonance itself. In this chapter we present demonstrated thermal drift $\sim$2 pm/K, 40 times better than a Si filter and nearly an order of magnitude better

than SiO_2. This holds the potential for similar significant reductions in signal to noise or integrated circuit stabilization for such sensors.

Another application of athermal circuits is in communications. Athermal devices are needed as a method of increasing the single lane bandwidth of uncooled interconnects. Uncooled wavelength division multiplexing (WDM) interconnects are the clear choice for reasons of energy efficiency to address the exponential growth of demand for bandwidth. At this time, new solutions are required. Bandwidth demands for a given range of wavelengths, typically a single laser gain medium bandwidth, can be met by either an increase in the number of symbols per bit of a single channel or by increasing the channel spacing or some combination of the two. Figure 2.1 illustrates the trade-off as normalized to a 10Gbps non-return to zero (NRZ) signal. Usually the energy cost of digital signal processing for anything beyond the simplest of higher order modulation schemes would tend to bias a designer to pursue denser channel spacing before advanced modulation. However, this requires that one address the thermal drift challenge. Figure 2.1 assumes the spectral efficiency of higher order modulation signals scales linearly with channel spacing and modulation order as a first order approximation. A similar trade-off exists at higher baud rates.

In Section 2.4 we explore the concept of an athermal laser as part of the solution to this problem. Tunable lasers are also a potential solution, however the

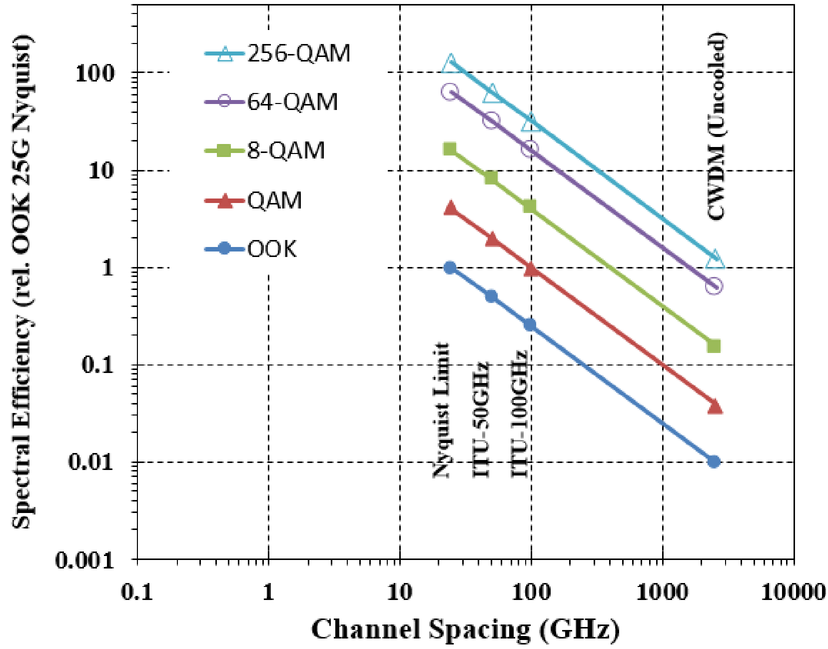


Figure 2.1: This plot compares two methods of improving spectral efficiency in a transmission link. Assuming the link is uncooled you are limited to coarse WDM (20 nm) spacing if you can not thermally stabilize your channels. If you can make a link with athermal components you gain a factor of 100 that makes on-off-keying comparable to the highest order modulation schemes.

feedback schemes required to stabilize them are more complicated than the approaches proposed here or require the additional complexity of an off-chip filter and monitor (wavelength locker) or on-chip temperature sensor and lookup table with associated memory and logic. The following sections include a brief background of the concepts and technologies that enable these novel designs and a few examples of designs that meet the requirements of uncooled WDM laser sources.

2.1.2 Circuit-based athermalization

The simplest athermal technology is the athermal waveguide, broken into athermal circuit-based guides and materials-based guides. Circuit-based guides have been used to create finite impulse response (FIR) filters where the temperature sensitivity of the center wavelength is reduced significantly [13, 53]. Some of the common FIR filters that can be made athermal are shown in Fig. 2.2. The main design methodology used in these structures is that the filter response depends only on the phase difference between the interfering waveguides and not the absolute phase shift. By co-integrating waveguides with different thermo-optic coefficients, and adjusting the length of each waveguide type, the phase difference between the neighboring waveguides can in principle be independent of temperature, over a range in excess of 50 °C [13, 53]. The same principle does not apply to the case of infinite impulse response (IIR) filters, such as ring resonators and Bragg gratings, as the filter response depends on the absolute phase shift. This significantly reduces the temperature range over which they can be compensated using the same technique. Also, the filter shape and insertion loss would vary thereby forming a limitation of circuit-based techniques to create IIR filters.

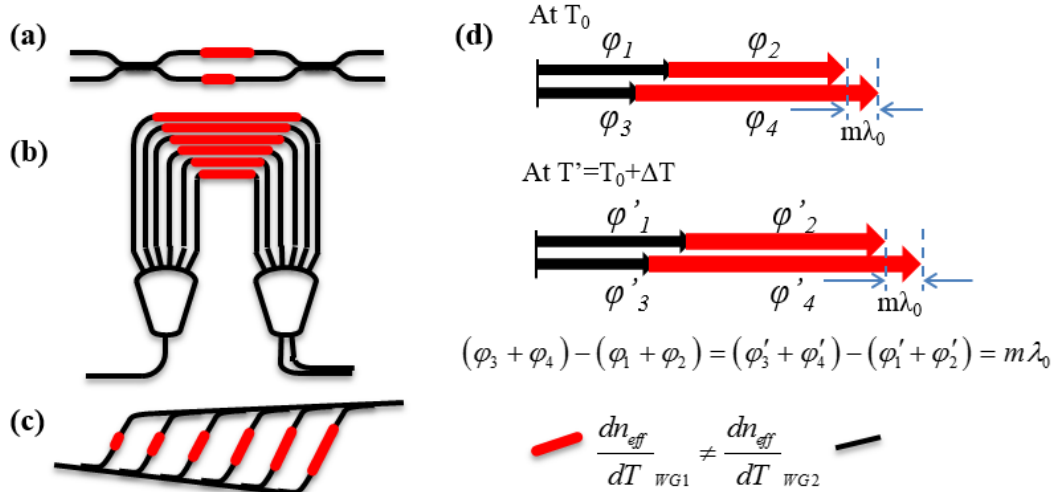


Figure 2.2: (a-c) Three FIR filters whose response can be made less sensitive to temperature variation by using two waveguide types (shown in red and black) each with a different thermo-optic coefficient. (d) Vector representation of effective path length for circuit (a) showing the principle whereby the phase difference of the paths is constant with temperature (T and T') [54].

2.1.3 Waveguide and grating athermalization

Starting with a simple waveguide defined by only the core and cladding material parameters, guided modes can be found by solving Maxwell's equations given the geometry and dielectric constants. The core typically has larger refractive index than the cladding. However, exceptions to this exist such as large low index core guides with a partial thin higher index cladding, slot type guides and photonic crystal waveguides. Regardless of the type, guided modes need different materials, and the mode is confined in both core and cladding(s).

So, how do we make such athermal waveguides? For a Fabry-Pérot (FP) etalon, the resonant wavelength shift with temperature, $d\lambda_r/dT$, can be shown to follow the equation,

$$\frac{d\lambda_r}{dT} \approx \frac{\lambda_r}{n_g}\left(n_{eff}\alpha_{sub} + \frac{dn_{eff}}{dT}\right) \tag{2.1}$$

where,

$$\frac{dn_{eff}}{dT} = \sum_k \Gamma_k \frac{dn_k}{dT} \tag{2.2}$$

This approximates the thermal expansion of the waveguide by that of the substrate, α_{sub}, and intentionally uses a partial derivative of the effective index, n_{eff}, with respect to temperature, T, such that this waveguide thermo-optic term can be expressed purely in terms of material thermo-optic coefficient, dn_k/dT, and confinement factor, Γ, for each material k [55].

$$\Gamma_{xy} = \frac{n}{n_{eff}} \frac{\int_{w_k}\int_{h_k} |U(x,y)|^2 dxdy}{\int_x \int_y |U(x,y)|^2 dxdy} \tag{2.3}$$

U(x,y) is the normalized transverse electric field profile. n is the index of refraction of the material for which the confinement is being calculated, and n_{eff} is the group index of the mode. For this cross-sectional representation, the extents of the integration are equal to the extents of the material w_k and h_k in the numerator and all of space x and y in the denominator.

To describe an athermal waveguide with the *confinement model* in Equation 2.1 alone is not a complete enough description. Generally, athermal waveguides

require a description of the layout and mechanical behavior of the waveguide including the substrate and packaging. As evidence of this assertion, I site publications on a commercialized technology to take a conventional AWG and package in a way to make it athermal. [8, 49] Nothing in the standard description of the core geometry, or core and cladding material parameters has changed, but the behavior of this phase sensitive interferometric device is completely altered with respect to a change in temperature. This can be explained by modifying the thermal expansion assumption and adding stress σ into the typical description of a waveguide thermo-optic term $dn_{eff}(\sigma, \lambda, T)/dT$. Note the full derivative rather than the prior partial notation. See Section **??** for a more complete derivation of each case.

Therefore either both core and cladding materials must be athermal or one must have a mix of positive and negative thermo-optic materials with correspondingly engineered confinement in each material to make an athermal waveguide. In order to understand the thermo-optic principle, let's start with the definition of refractive index in dense materials given by the Clausius-Mossotti relation [56]. This is similarly referred to as the Lorentz-Lorenz equation or Maxwell's formula. For this argument, I will use a derivation with explicit temperature dependence to make it clear what is happening [57].

$$\frac{n^2 - 1}{n^2 + 2} = \frac{\rho(T)\alpha(\rho, T)}{3\epsilon_0} \tag{2.4}$$

or

$$n = \sqrt{\frac{2\rho(T)\alpha(\rho,T) + 3}{3 - \rho(T)\alpha(\rho,T)}} \tag{2.5}$$

where

$$2\rho(T)\alpha(\rho,T) + 3 > 3 - \rho(T)\alpha(\rho,T) > 0 \tag{2.6}$$

For this expression ρ is the density of the material, α is the molecular polarizability, **T** is temperature, and **n** is the index of refraction. The derivative of this expression gets complicated and may cloud the discussion. However, it is clear from equation 2.5, if an increase in temperature causes the density-polarizability product to increase, the material will have a positive TOC. If it decreases with temperature, the material will have a negative TOC. With no external influence such a stress or pressure, and assuming the material is not undergoing a phase change, the density of a material will tend to decrease with increasing temperature, hence the term thermal expansion. Therefore without a compensating increase in the polarizability with temperature, all materials would tend to have negative TOCs. This is not true of most materials, in fact, of nearly all materials conventionally used in photonic integrated circuits, there is an increase in polarizability with temperature that more than makes up for the decrease in density with increasing temperature. There are, however, a group of materials with large coefficients of thermal expansion including alkali and thallium halides, and titania

that overcome the thermal variation in polarizability to achieve negative TOCs. This points out the impact of coefficient of thermal expansion (CTE) on the TOC.

Typical behavior of solid materials:

$$\uparrow T \implies \downarrow \rho(T), \uparrow \alpha(\rho, T) \tag{2.7}$$

Direct correlation of the CTE and TOC is an oversimplified description of the problem because as it is explicitly stated in Equation 2.4, the polarizability is a function of temperature and density and the complicated electron distribution of the material. For example studies on SiO_2 glasses including TiO_2 and other glasses have shown that adding TiO_2 not only doesn't increase the CTE of the glass, there is no correlation between the CTE and TOC of such mixed glasses [58]. However, barring changes to the molecular structure of the material, it is clear that mechanically enhancing or suppressing the expansion of the material will directly impact the TOC. Therefore, thermal stress induced by mismatches in thermal expansion of substrate, core, and cladding materials can be significant.

Each film has a CTE according to the manner in which it is deposited. However, this expansion is a three-dimensional process and will be pinned in the plane to the expansion of the substrate. For this reason, I have focused on values from materials deposited on silicon summarized in Table 2.1 below.

Table 2.1: Material properties used in CMOS compatible athermal waveguides

Material	CTE ($\times 10^{-6}$/K) [Ref.]	TOC ($\times 10^{-5}$/K) [Ref.]	n(1550nm)
Si	2.618 [59]	18.6 [60]	3.478
SiO_2	.55 [61]	1.19 [61]	1.445
Si_3N_4	2.5 [62]	2.4-4 [52, 63]	1.98
TiO_2	7.5 [62]	∼-(10-65) [26, 51, 52]	2.18

2.2 Athermalized TiO_2 core waveguides

Ring resonators with TiO_2 core confinement from 0.05 to 0.42 are fabricated and measured for thermal sensitivity achieving -2.9 pm/K thermal drift in the best case [64]. Materials used are CMOS compatible (TiO_2, SiO_2, and Si_3N_4) on a Si substrate. The under-discussed role of thermal stress in thermo-optic behavior is clearly observed when contrasting waveguides buried in SiO_2 to those with etched sidewalls revealed to air. Multiphysics simulations are conducted to provide a theoretical explanation of this phenomenon in contrast to the more widely reported theories on thermo-optic behavior dominated by confinement factor.

2.2.1 Background

In this section, we present some experiments with ring resonators offering a clean and repeating spectral signature that one can track even with only small

deviations in their resonance wavelengths. A resonator is also an important device for the proposed WDM systems and would, therefore, greatly benefit from thermal stabilization for uncooled systems. The rings presented use TiO_2 as a core material rather than a cladding layer, as previously demonstrated [26, 52].

Our measurements indicate that buried TiO_2 core waveguides clad by plasma enhanced chemical vapor deposition (PECVD) SiO_2 with core confinements ranging from 0.07 to 0.42 exhibit dn_{eff}/dT on the order of the published SiO_2 ($\sim 10^{-5}K^{-1}$) regardless of confinement. This implies a TOC of TiO_2 of ($-10^{-6}K^{-1}$), two orders of magnitude less than literature values. We argue that in such geometries the thermo-stress-optic (TSO) effect can dominate the TOC, which contradicts current literature on athermal waveguides which use a *confinement model* without dispersion, thermal path length expansion, and stress considerations [26, 27, 51, 52]. Given the results discussed in Section 2.2.3, we developed theory and conducted simulations to explain our experimental results.

2.2.2 Waveguide geometry and fabrication

A single lithography process with a chromium hard mask was used for all waveguides. 15 μm of thermal oxide was grown to eliminate potential substrate leakage for thin core geometries. Amorphous TiO_2 was DC sputtered at 2300 W in an Ar/O_2 (20/10 sccm) environment with a Ti target at room temperature in

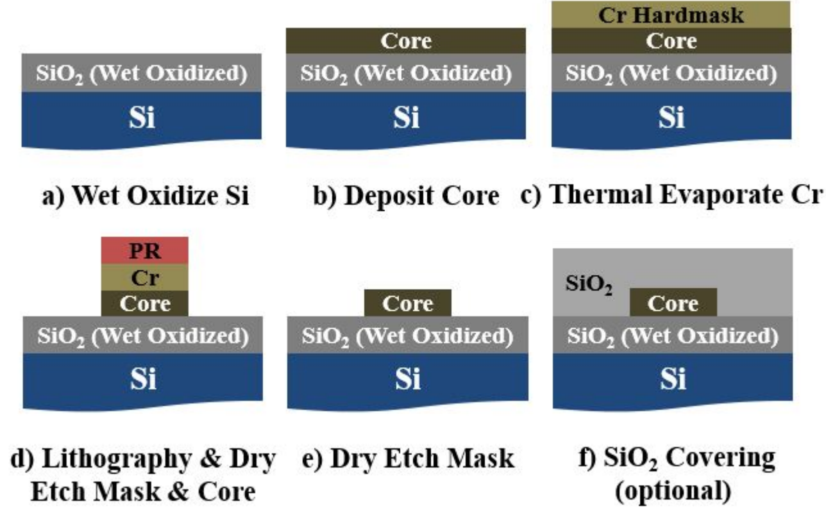


Figure 2.3: This is a process summary of the titania core waveguide process.

an Endeavor tool. The measured index is 2.18 at 1550 nm in a J.A. Woollam Co. Inc variable angle spectroscopic ellipsometer (VASE). Si_3N_4 is deposited using low-pressure chemical vapor deposition on both sides of the wafer using a stoichiometric process with a refractive index of 1.98 at 1550 nm as measured in the VASE. High-density PECVD SiO_2 films deposited at $300°C$ is used as cladding above the core.

Lithography was done using an ASML PAS 5500/300 deep ultra-violet photolithography tool. Dry etching was done with an inductively coupled plasma etcher for the Cr hardmask with a $Cl2/O_2$ chemistry, followed by a $CHF_3/CF_4/O_2$ dry-etch of the core. This core etch sufficiently removed the photoresist softmask such that only the Cr remained. The Cr was then dry-etched. The revealed core

was cleaned with O_2 plasma to remove the remaining polymer from the ICP etches. Buried waveguides had additional PECVD SiO_2 over cladding. The samples were then diced and tested as described below in Section 2.2.3.

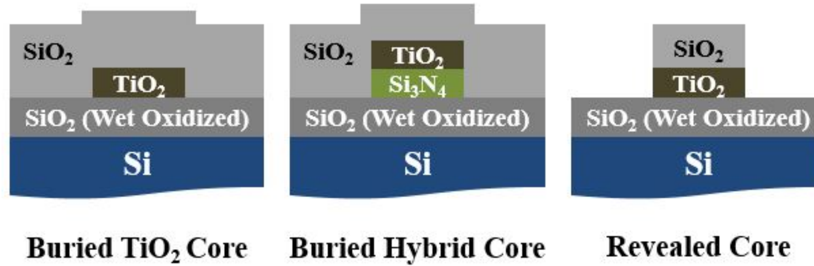


Figure 2.4: Cross section of waveguide designs with TiO_2 or hybrid cores.

Figure 2.4 shows the three waveguide cross sections reported in this work. Of note is the buried versus revealed designs.

2.2.3 Measurement setup and results

Using a tunable laser, polarization controller, lensed fiber facet coupling and a photodiode, we tracked the TE resonance of the through port of ring resonators with temperature (15-40°C) for a range of waveguide geometries (widths, thicknesses and radii) with 0.07 to 0.42 material confinement factors simulated in Fimmwave. This diverse set was used to span a large range of confinement factors. These measurements are plotted in Fig. 2.5(a) with simulations using a *confinement model* detailed in Section 2.2.4. Geometric details are provided in Table

2.2. Figure 2.5(b) adds measurements from two sources which reported a range of geometries [26, 27]. Our buried structures clearly stand out in these data sets as

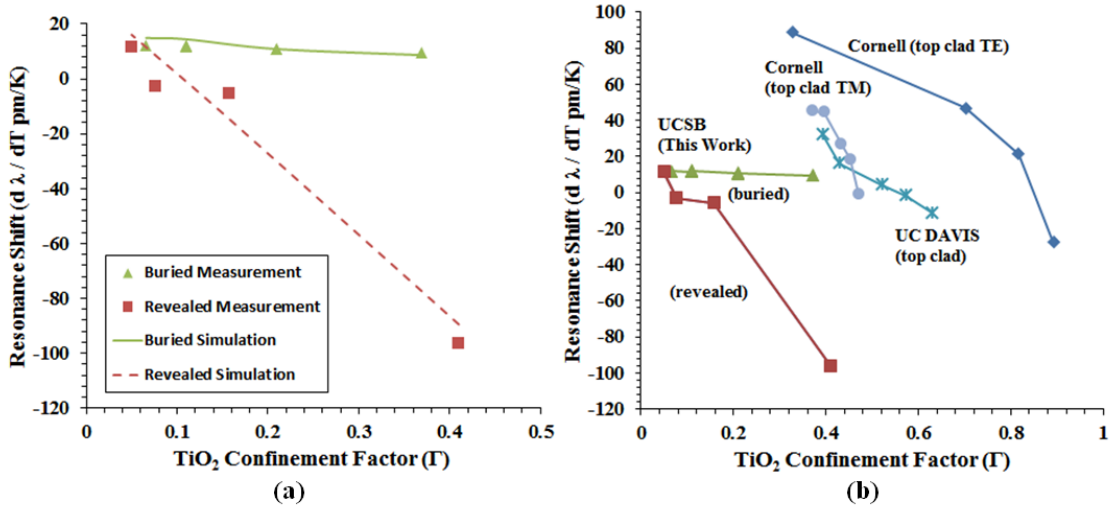


Figure 2.5: (a) Measured thermal drift with *confinement models* based on Eq. 2.9 with separately fitted TiO_2 TOC for buried (-$10^{-6}K^{-1}$) and revealed (-$2.5\times10^{-4}K^{-1}$) rings. (b) Measurements compared to other literature with TiO_2 cladding demonstrate a unique suppression of TOC in buried TiO_2.

having negligible change in thermal drift with increasing TiO_2 confinement. From this we conclude that the TiO_2 TOC is effectively suppressed to $\sim$ -$10^{-6}K^{-1}$ by burying these TiO_2 cores. This effect is released when the sidewall of the TiO_2 is revealed by co-etching the top cladding and the core as shown in Fig. 2.4(c). These revealed structures fit a *confinement model* described in Section 2.2.4 with a TOC of -$2.5\times10^{-4}K^{-1}$ which is more comparable to the UC Davis and Cornell results using TiO_2 as a top cladding which also lacks a thermal stress induced by full top SiO2 cladding.

Further evidence of the impact of burying the TiO_2 core with SiO_2 was found by top cladding revealed structures exhibiting the strongest negative TO behavior and seeing comparable suppression to those fabricated as buried structure initially.

2.2.4 Theory and simulations

The analysis in Section 2.2.3 results in two separate TOCs for the same TiO_2 material processed in nearly identical conditions, which is in contrast to an intuitive understanding of TOC as a geometrically independent parameter. Therefore, further exploration was conducted to converge on a model that explains these measurements.

The most typical model for thermal drift is a *confinement model*. Below is a derivation of this model for a ring resonator with resonance wavelength λ_r.

$$m\lambda_r = 2\pi R(T) n_{eff}(\lambda_r, T) \tag{2.8}$$

$$\frac{d\lambda_r}{dT} \approx \frac{\lambda_r}{n_g}\left(n_{eff}\alpha_{sub} + \frac{\partial n_{eff}}{\partial T}\right) \tag{2.9}$$

$$where, \frac{\partial n_{eff}}{\partial T} = \sum_k \Gamma_k \frac{\partial n_k}{\partial T} \tag{2.10}$$

The ring radius, R, and the effective index, n_{eff}, are explicitly a function of temperature, T, and m is the longitudinal mode number, m. The ring radius

canceled out and is not in the final Eq. 2.9. The use of partial derivative in $\partial n_k/\partial T$ implies the term is only a function of temperature. The material confinement factor, Γ, as define by Visser et al. in [65], quantifies the overlap of the optical mode with each material k. The resulting $\partial n_{eff}/\partial T$ is the sum over all k materials in which the light interacts. The final assumption is that the expansion of the actual waveguide path length is dominated by the linear thermal expansion of the 525 μm Si substrate α_{sub}.

Below is an alternative derivation for a *combined model* including stress terms similar to [9, 66]. Throughout this derivation, subscripts have been used as a shorthand for the stress tensor σ_{ij}, and a constant tensor β_{ij}.

$$m\lambda_r = 2\pi R(\sigma_{ij}, T) n_{eff}(\lambda_r, \sigma_{ij}, T) \tag{2.11}$$

$$\frac{d\lambda_r}{dT} \approx \frac{\lambda_r}{n_g}\left(n_{eff}\alpha_{sub} + \frac{dn_{eff}}{dT} + \beta_{ij}\frac{d\sigma_{ij}}{dT}\right) \tag{2.12}$$

$$where, \frac{dn_{eff}}{dT} \equiv \frac{\partial n_{eff}}{\partial \sigma_{ij}}\frac{\partial \sigma_{ij}}{\partial T} + \frac{\partial n_{eff}}{\partial T} \tag{2.13}$$

As a stress term is added to n_{eff} and R, the derivation of $d\lambda_r/dT$ has both a stress related term, and a subtle change in the confinement term $\partial n_{eff}/\partial T$ defined in Equation 2.9. In Equation 2.12, I have very intentionally used dn_{eff}/dT rather than $\partial n_{eff}/\partial T$, though the wavelength dispersion is all represented in the n_g as

before. For this reason Equation 2.13 includes both the original $\partial n_{eff}/\partial T$, from Equation 2.10, and a partial derivative with respect to the thermal stress tensor. There is also a stress induced path length change term with a device dependent constant tensor β_{ij}, which is significant when athermally packaging a device such as in [8, 9, 49]. For the purposes of devices in Table 2.2, this term is assumed to be negligible in comparison to the α_{sub} as the symmetric thermal oxide prevents bowing and none of the packaging methods discussed in Section 1.2.1 or similar methods are employed.

Three models are presented in Table 2.2 and plotted in Figure 2.6, the *confinement model*, the *stress model*, and the *combined model*. The *stress model* is the same as the *combined model*, however it assumes that $\partial n_{eff}/\partial T = 0$. To calculate the three models in Table 2.2 below, we use COMSOL finite element stress-optic simulations in two dimensions with a generalized plane strain model to solve for Eq. 2.13 and Fimmwave film mode matching model for accurate confinement factors, effective indices, and group indices for the fundamental TE mode. Unless otherwise stated, we used the material properties in Table 2.3.

To better visualize the simulation data in Table 2.2 the comparison of simulation results and measurement data is presented graphically in Figure 2.6.

Youngs modulus, E, Poissons ratio, ν, and linear thermal expansion coefficients, α, for all materials including the silicon substrate are shown in Table 2.3.

Table 2.2: Comparison of thermo-optic models and measured data

	Ring Geometries				Confinement					$d\lambda_r/dT$ (pm/K)			
	w (μm)	t_{TiO2} (nm)	t_{Si3N4} (nm)	R (μm)	TiO_2	SiO_2	Si_3N_4	n_g	n_{eff}	Meas.	Conf. Model	Stress Model	Comb. Model
Buried	4	30	90	1232	0.07	0.78	0.18	1.66	1.51	11.8	7.0	3.1	30.4
	4	45.6	90	1232	0.11	0.73	0.20	1.72	1.53	11.5	1.7	3.2	22.3
	4	90	0	1232	0.21	0.82	0	1.67	1.51	10.8	-14.2	3.2	2.3
	4	135	0	1232	0.37	0.67	0	1.84	1.58	9.48	-31.6	5.01	-4.2
Revealed	0.9	180	0	40	0.41	0.49	0	2.00	1.50	-96.3	-34.6	-39.7	-61.4
	4	75	0	1232	0.16	0.87	0	1.62	1.48	-5.60	-14.8	-12.8	-32.9
	4	50	0	1232	0.08	0.94	0	1.54	1.46	-2.93	3.1	-11.4	-5.2
	20	40	0	1530	0.05	0.96	0	1.51	1.46	11.7	6.9	-4.5	1.8
Fit Parameters										B_1 (10^{-12}/Pa) =	0	-1000	-100
										B_2 (10^{-12}/Pa) =	0	1000	0.5
										$dn_{TiO_2}(\times 10^{-5})/dT$ =	-13	0	-18

Refractive indices relate with the thermal stress as described by three stress-optic coefficients B_1 and B_2, and B_3. In the case of and isotropic material, as we have assumed SiO_2, Si_3N_4, and TiO_2 to be, $B_3 = B_1 - B_2$. In Equation 2.14 n_0 is the scalar index without stress, and dn_{ij}, and σ_{ij} are the stress induced index change and stress coefficients respectively. As n_{ij}, and σ_{ij} are functions of temperature, T, and we are interested in their derivatives the cross terms which relate to B_3 are not negligible, however σ_{xz} and σ_{yz} reduce to zero under the constraints of the

generalized plane strain model.

$$\begin{bmatrix} dn_{xx} \\ dn_{yy} \\ dn_{zz} \\ dn_{yz} \\ dn_{xz} \\ dn_{xy} \end{bmatrix} = \begin{bmatrix} n_{xx}-n_0 \\ n_{yy}-n_0 \\ n_{zz}-n_0 \\ n_{yz} \\ n_{xz} \\ n_{xy} \end{bmatrix} = \begin{bmatrix} B_1 & B_2 & B_2 & 0 & 0 & 0 \\ B_2 & B_1 & B_2 & 0 & 0 & 0 \\ B_2 & B_2 & B_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & B_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & B_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & B_3 \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} \tag{2.14}$$

Table 2.3: Material properties for simulation (λ_0=1550 nm)

	TiO_2	SiO_2	Si_3N_4	Si
n	2.18[b]	1.445[b]	1.98[b]	3.478
dn/dT (10^{-5}/K)	-(10-65)[a]	1	2.4 [63]	18 [51]
B_1 (10^{-12}/Pa)	[a]	0.65 [67]	∼0.65[d]	-11.35 [68][b],[c]
B_2 (10^{-12}/Pa)	[a]	4.2 [67]	∼4.2[d]	3.65 [68][c]
ν	0.2 [69]	0.42 [70]	0.2 [71]	0.19 [70]
E (GPa)	65 [69]	78 [70]	285 [71]	110 [70]
ρ (g/cm3)	3 [67]	2.203 [70]	3.1 [71]	2.33 [70]
α(10^{-6}/K)	7.5 [62]	0.38 [72]	3.0 [73]	2.6 [62]

[a)]Least squares fit, [b)]Measured, [c)]Full tensor is more accurate, [d)]Assumed

In addition to Table 2.2, $d\lambda_r/dT$ for all three models is plotted against confinement factor in Fig. 2.6. It is clear from this Fig. the difference in the models.

The *confinement model* in Fig 2.6(a) doesn't result in a different thermal drift behavior between buried and revealed waveguides as seen in measurements. The *stress model* in Fig. 2.6(b), fitting for B_1 and B_2, shows a split between the two waveguide types and fits the data better than the *confinement model* when compared using an F test (α=0.1) to rule out the addition of a fit parameter. However, the values B_1 and B_2 derived from the *stress model* fit are probably non-physical as they are quite large. In contrast the *combined model* which fits for B_1, B_2, and the TOC of TiO_2 has a better least squares fit, but doesn't quite

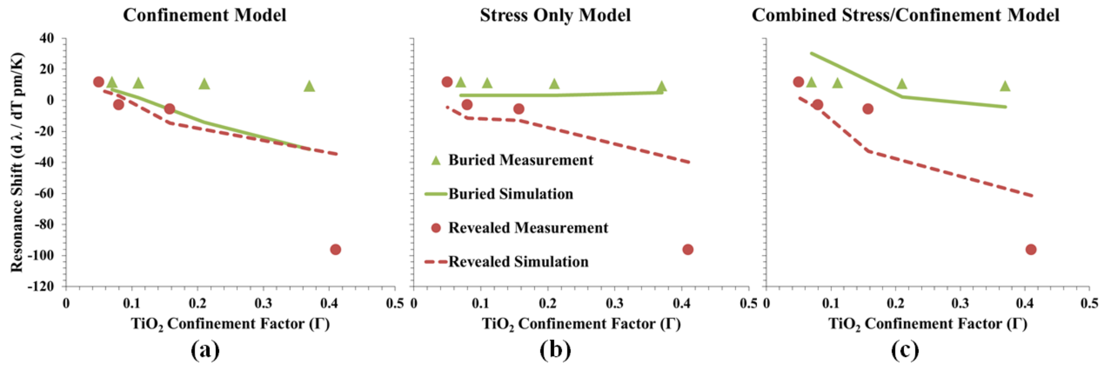


Figure 2.6: Comparison of the *confinement*, *stress*, and *combined stress/confinement model*.

pass the F test (α=0.1) as a superior model given it uses three fit parameters. However, this is backed by a clear physical model and has parameters that are reasonable. This comparison may also be confounded by the large variation in waveguide geometries that was required to span such a larger range of low confinements. By far and away the best model was a separate *confinement model* for

each type of waveguide as shown in Fig. 2.5(a). Given most analyses will only use waveguides of a similar stress profile and geometry, this may be a practical model, however we do emphasize that it lumps all of the underlying physics into a single non-generalizable parameter that cannot be fairly compared between a diverse set of literature, as is apparent in the range of TiO_2 TOCs already reported.

Figure 2.7 plots the thermally induced stress profiles of characteristic revealed and buried waveguides showing the contrast of those stresses applied to the core and adjacent cladding. As is clear from the plots, these waveguides have complex and drastically different thermal stress profiles; which cause the large difference in thermal drift uncorrelated to TiO_2 confinement.

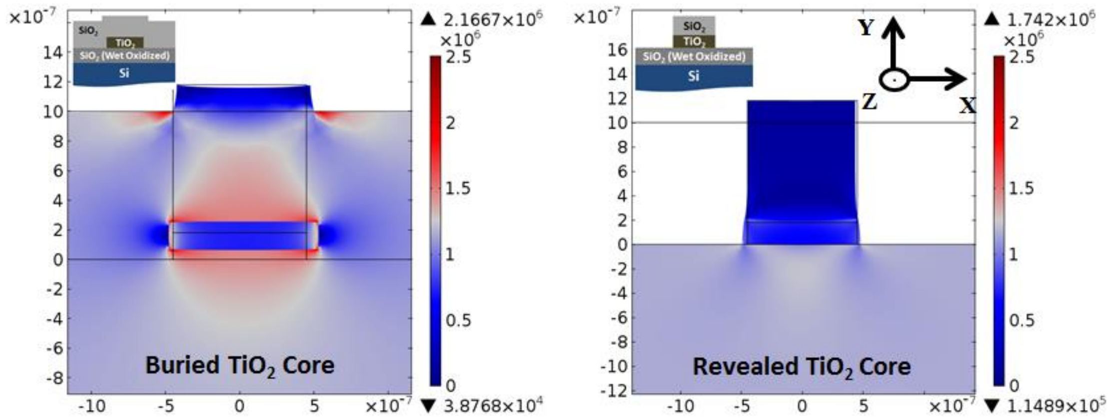


Figure 2.7: Comparison of the thermal stress profile of buried and revealed core waveguides.

Finally, a difference in loss was observed when comparing the buried and revealed waveguide structures. Using a fit to the ring spectra loss was calculated

assuming negligible loss in the coupler. Buried structures presented with 4 μm wide waveguides and 1232 μm ring radius typically had loss $\sim$0.5 dB/cm compared to $\sim$1-2 dB/cm in revealed structures. We believe both to be scattering loss limited and can therefore be improved with further process development.

2.2.5 Conclusions of athermalized TiO_2 core waveguides

We have shown that TSO effects are important to performance of TiO_2 core waveguides most strongly indicated by reduction of the material TOC by more than two orders of magnitude. Furthermore, we clarified the theoretical framework for this phenomenon with derivations of three models of ring resonator thermal drift. We believe that such buried channel waveguides show reduction in the thermal expansion of TiO_2, which is the likely cause of a stress-induced suppression of the negative TOC in TiO_2. Revealing the sidewalls to air releases that suppression. However, because of the complex nature of stress each waveguide type requires numerical analysis to understand the role stress will play. In many cases, this effect is at least as significant as non-stress related thermo-optic effects of the material and thus must be included to determine the correct TOC of TiO_2. To solve the thermal drift problem without polymers or active feedback further stress research into TiO_2 is required to enable CMOS compatible athermal photonic integrated circuits.

2.3 TiO_2 top clad athermal rings and gratings

In order to have a more compatible process with existing Silicon Hybrid technology, TiO_2 can be used as a top cladding layer on Si core waveguides. These designs require Si waveguides that are both thin and narrow.

Using SOI with a 200 nm thick Si device layer on 3 μm of SiO_2, a simple rib waveguide is formed by etching trenches on either side of the waveguide down to 190 nm using a SixNy hardmask. The 60 nm Si slab layer is then revealed while the top of the waveguide remains protected by SixNy. Then after stripping and cleaning the photoresist and other contaminants, the waveguide is oxidized to both smooth the sidewalls and shrink the width of the waveguide in a very controlled way to a slab thickness of 30 nm. This is important to push the waveguide width reliably below 200 nm, which is challenging for the ASML S500/300 DUV stepper with a 248 nm source used for the entire process. Following this waveguide formation, the hard mask is removed and the gratings are patterned 20-25 nm deep so as not to expose the buried oxide Fig. 2.8 shows a top-down SEM of this grating structure.

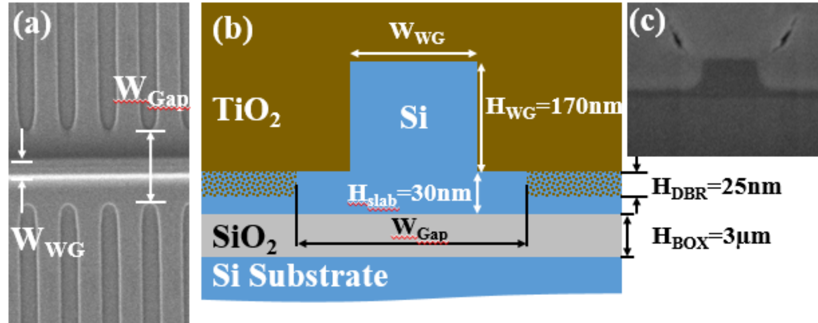


Figure 2.8: Waveguide geometries. (a) top down SEM image of DBR before TiO2 top cladding deposition, (b) cross-sectional diagram of DBR. (c) Cross-sectional SEM of TiO_2 clad Si waveguide with small voids visible in the TiO_2 [74].

2.3.1 TiO_2 top clad athermal gratings

The DBR gratings used were also limited by the stepper resolution to a 3rd order design for Bragg wavelength around 1300 nm. This design has higher loss and lower grating strength than a 1st order grating with the same grating gap width W_{Gap}. Following the waveguide formation a deep etch of the silicon facet is made and the TiO_2 was sputtered on as a top cladding of 1500 nm so that that mode has negligible interaction with the TiO_2 air boundary we exception to the small voids in Fig. 2.8(c). The grating has a waveguide width of 200 nm.

Reflection spectra of DBR gratings are measured using a broadband LED source, a fiber optic polarizer and polarization controllers, an optical circulator and an optical spectrum analyzer (OSA). Transmission measurements of the ring spectra used a similar setup but with a tunable laser and photodiode. Resonant

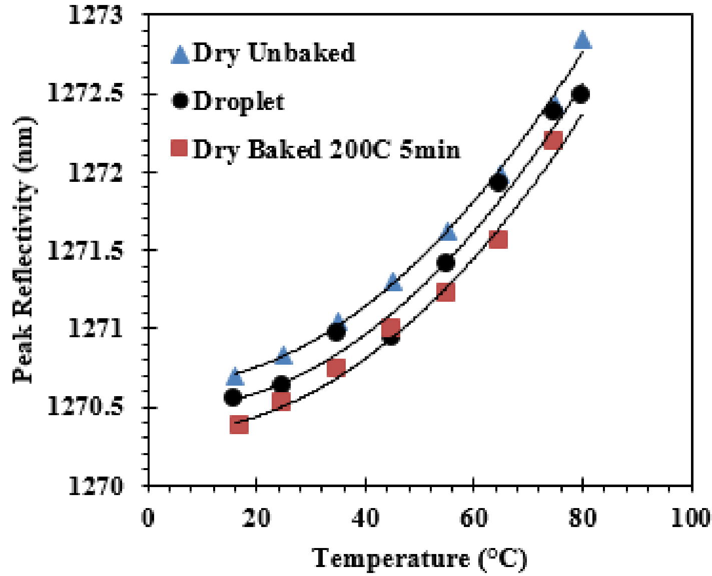


Figure 2.9: Peak reflectivity of 200 nm wide, 200 nm height third order DBR gratings as a function of temperature. Sample was tested following cleaning and N_2 drying, first without baking (typical), second with a water droplet on top (high humidity), and finally after a 5 min $200°C$ dehydration bake (low humidity) [74].

wavelengths of a ring resonator and a DBR grating are plotted in Fig. 2.9. They both show a distinctly quadratic relationship with temperature which has not been reported for similar devices near 1550 nm. Further discussion of this phenomenon is made in Section 2.3.3.

Figure 2.9 shows an environmental experiment to test the grating's sensitivity to humidity. Previous reports have been made which suggest that the negative TOC of TiO_2 deposited with atomic layer deposition (ALD) is due to evaporation of water molecules from the film. The findings from this test suggests that

the TOC of TiO_2 is not significantly impacted by the presence of water for our sputtered films.

One application of such athermalized gratings is in passively athermal DBR lasers. Design of such devices is discussed in greater detail in Section 2.4.

2.3.2 TiO_2 top clad athermal rings

Similar to the rings presented in [25], [26], & [27] near 1550 nm, UC Davis made passive rings for development towards our athermal transmitter project. SEM images of these rings with cross sections before and after TiO_2 cladding are shown in Fig. 2.11. The radius of the ring resonator is 25 μm with a 550 nm coupler gap to a 200 nm bus waveguide.

Using data collected by UC Davis for 25 μm radius ring Si rings clad with TiO_2, is shown in Fig. 2.11.

There are a few predictable trends in the data in Fig. 2.11 that were under discussed in prior literature. As the wavelength increases from 1270 nm to 1310 nm to 1340 nm the influence of the TiO_2 also increases resulting in a blue shift for the majority of the 20-50°C temperature range. This is predictable as waveguide dispersion causes the confinement factor in the TiO_2 to increase with increasing wavelength. Similarly, increases in the waveguide width cause a decrease in confinement and stronger red shift with temperature. This also was predicted and

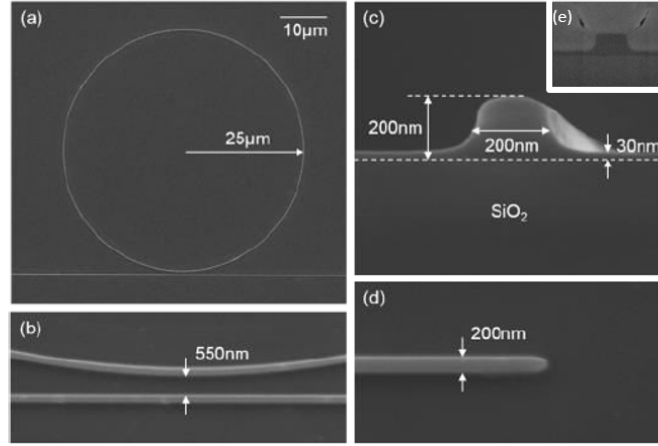


Figure 2.10: (a) Top-view SEM image of ring resonator before TiO2 cladding deposition; (b) Ring-to-bus waveguide coupling region; (c) Cross-sectional SEM image of waveguide before TiO2 cladding deposition; (d) Top-view SEM image of inverse taper. (e) Shows the waveguide following TiO_2 cladding with small voids in the deposited film [74].

reported in [26] & [27]. However, the quadratic nature of the resonant wavelength shift with temperature was neither predicted nor reported in previous work with TiO_2 on Si. A more detailed discussion of this observation follows in Section 2.3.3.

2.3.3 Discussion on second order effects

The majority of discussion in the athermal literature with TiO_2 assumes a constant dn/dT across temperature. Naturally this is not the whole truth, but quadratic (and other higher order) shifts in resonance wavelength with temperature are not observable over small ranges of temperature which many TiO_2 reports limited their data to [26, 27]. To treat this problem appropriately we found

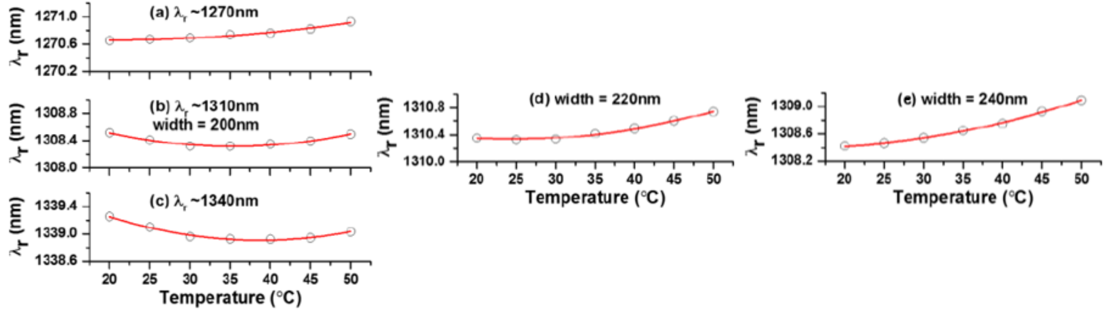


Figure 2.11: Measured (black circle) and quadratically fitted (red line) resonance wavelength as a function of temperature. The device with a waveguide width of 200 nm is measured at various spectral ranges around (a) 1270 nm, (b) 1310 nm and (c) 1340 nm and across different waveguide widths (b) 200 nm, (d) 220 nm, (e) 240 nm [74].

a discussion about polymer clad Si rings which also observed a strong quadratic change in resonance wavelength with temperature [22]. We have borrowed generously from their analysis but applied our data and assumptions based off of our knowledge of TiO_2 clad rings. As we concluded in Section 2.2, a confinement model is the best way to treat a group of waveguides of the same thermal stress profile. Restating Eq. 2.9

$$\frac{d\lambda_r}{dT} \approx \frac{\lambda_r}{n_g}\left(n_{eff}\alpha_{sub} + \frac{\partial n_{eff}}{\partial T}\right) \tag{2.15}$$

we simply must do an expansion of dn_{eff} to add second order effects

$$dn_{eff} = \sum_k \Gamma_k \frac{\partial n_k}{\partial T} dT + \frac{1}{2}\left(\Gamma_k \frac{\partial^2 n_k}{\partial T^2} + \frac{\partial \Gamma_k}{\partial n_k}\left(\frac{\partial n_k}{\partial T}\right)^2 + \dots\right) dT^2 \tag{2.16}$$

In Eq. 2.16 T is temperature, Γ_k is the confinement of the mode in a material k of index n_k and the change in effective index is the sum of contributions for

all k materials. This can be broken into three basic terms, the first order terms as used previously in Eq. 2.10, and second order terms that are due to material quadratic thermo-optic effects

$$\sum_k \frac{1}{2}\left(\Gamma_k \frac{\partial^2 n_k}{\partial T^2}\right) dT^2 \tag{2.17}$$

and those second order changes due to confinement factors change with temperature regardless of second order changes in the materials:

$$\sum_k \frac{1}{2}\left(\frac{\partial \Gamma_k}{\partial n_k}\left(\frac{\partial n_k}{\partial T}\right)^2 + \ldots\right) dT^2 \tag{2.18}$$

Here we have just used the $\ldots$ to represent all of the cross terms dependent on the number of materials in the waveguide. It turns out that the confinement factor terms in 2.18 when simulated for in the case of the TiO_2 clad rings are negligible by nearly two orders of magnitude when compared to material second order effects. With this knowledge it becomes simple to use the quadratic fit data to calculate second order material thermo-optic properties of TiO_2 with a subtle change to the *confinement model*:

$$\frac{dn_{eff}}{dT} = \sum_k \Gamma_k \frac{dn_k}{dT} \approx \sum_k \Gamma_k \left(\beta_k + \gamma_k T\right) \tag{2.19}$$

For this we assumed literature values for $dn_{Si}/dT = \beta_{Si} + \gamma_{Si} T = 1.834 \times 10^{-4} + 4.887 \times 10^{-7} T\ K^{-1}$ from [75]. For SiO_2 which has a much less significant role in this case $\beta_{SiO_2} = 10^{-5} K^{-1}$ and γ_{SiO_2} is assumed to be 0. A fit of the data

in Fig. 2.11 results in $dn_{TiO_2}/dT = \beta_{TiO_2} + \gamma_{TiO_2}T = -3.07 \times 10^{-4} + 4.45 \times 10^{-6}T$ K^{-1}.

2.3.4 TiO_2 clad Si rings and gratings conclusions

Though a materials solution for athermalization may indeed be the best for applications such as rings and gratings that have no circuit-based athermal equivalent, there are some finer details which will need to be considered. Section 2.2 highlights the importance of thermal stress as one such detail. In this section second order material thermo-optic effects limit the athermalizing range. However, on the whole, viable athermal solutions exist which can stabilize circuits and enable uncooled operation for low cost and energy efficient systems. The following Section 2.4 projects the use of such athermal technologies inside of integrated lasers.

2.4 Athermal laser design

This section discusses circuit-based and waveguide based athermalization schemes and provides some design examples of athermalized lasers utilizing fully integrated athermal components as an alternative to power hungry thermo-electric controllers

(TECs), off-chip wavelength lockers or monitors with lookup tables for tunable lasers. This class of solutions is important for uncooled transmitters on silicon.

In this section we explore the concept of an athermal laser as part of the solution to this problem. Tunable lasers are also a potential solution, however the feedback schemes required to stabilize them are more complicated than the approaches proposed here or require the additional complexity of an off-chip filter and monitor (wavelength locker) or on-chip temperature sensor and lookup table with associated memory and logic. The following sections include a brief background of the concepts and technologies that enable these novel designs and a few examples of designs that meet the requirements of uncooled WDM laser sources.

2.4.1 Thermal dependences of lasers

In order to athermalize a laser, one must carefully design for thermal drift of gain, loss, and cavity modes. Figure 2.12 shows a diagram of these three effects and provides typical values from thermal drift in semiconductor lasers with semiconductor mirrors. In general for an in-plane DBR, the thermal drift is represented by Eq. 2.20. This is an approximation for 50% duty cycle gratings and is similar to Eq. 2.9 utilizing the same definition in Eq. 2.10 for dneff/dT.

$$\frac{d\lambda_{Bragg}}{dT} = \frac{1}{m}\frac{\lambda_{Bragg}}{n_{g1}+n_{g2}}\Big((n_{eff1}+n_{eff2})\alpha_{sub}+\frac{dn_{eff1}}{dT}+\frac{dn_{eff2}}{dT}\Big) \tag{2.20}$$

In Eq. 2.20 λ_{Bragg} is the Bragg wavelength, or first order peak reflection wavelength, m is the order of the grating, $n_{g1,2}$ and $n_{eff1,2}$ are the group and effective indices corresponding to the two periodically repeating segments of the grating, and α_{sub} is the linear coefficient of thermal expansion for the substrate.

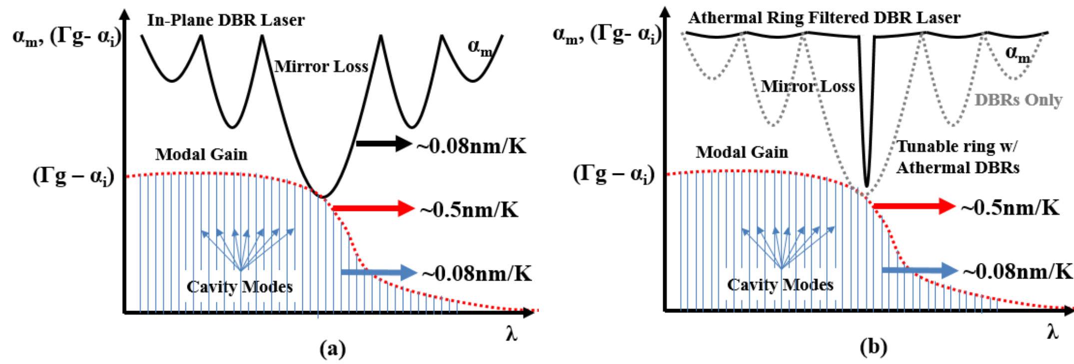


Figure 2.12: (a) Diagram of typical in-plane semiconductor laser with dense cavity modes where thermal drift is typically dominated by cavity loss. (b) A similar DBR laser design with and intra-cavity ring filter to achieve a narrower reflectivity bandwidth.

Thermal drift in gain is challenging to athermalize for because it is so fundamental to the change in band gap of the semiconductor gain material with respect to temperature. The two examples that perhaps have done the best job of overcoming this limitation are p-doping of quantum dots which can result in negligible change in threshold current with temperature or $T_0 = \infty$ at low temperatures and as much as 120K up to 85°C [45, 76], and the induction of hydrostatic pressure as a means to automatically counteract the typical thermal effect on the band gap and thus gain peak wavelength [77]. Thermal drift in loss is typically manifest in

the most spectrally sharp loss of the cavity, the mirror. For in-plane lasers with integrated DBR mirrors this drift, though it doesn't drift as rapidly as the gain peak, is the single most significant factor in laser wavelength drift. In contrast, in short cavity lasers such as vertical cavity surface emitting lasers (VCSELs) cavity mode drift is often the most significant. Athermalized VCSEL designs which modify the cavity with polymers and air gaps to compensate for cavity mode drift have already be proposed by Phillips et al. [78]. Our work focuses on in-plane devices and therefore athermalization must be made both in the mirror and the cavity.

2.4.2 Examples of integrated athermal lasers

One typical solution to temperature variations in uncooled WDM transmitter has been to use a tunable laser locked to an external wavelength locker, which varies only slightly with temperature or is itself regulated by a TEC. However, in this work we propose some designs which require no or only minimal laser feedback such that all lasers in an array can be easily integrated together with a channel spacing considerably less than the 20 nm specification of conventional uncooled coarse WDM.

Figure 2.13(a) shows a passively athermal DBR laser cavity, the simplest manifestation of an integrated athermal laser requiring no tuning or feedback. The

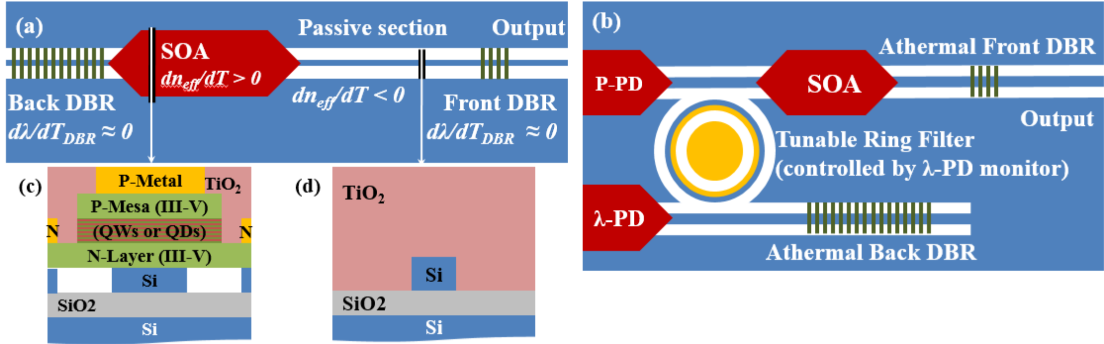


Figure 2.13: (a) Passively Athermal DBR Laser (b) Athermal Ring Filtered DBR (ARF-DBR) Laser (c) cross section of III-V/Si Hybrid SOA or PD with TiO_2 cladding. (d) cross section of Si waveguide clad with TiO_2 for a thermal compensator.

principle is that the cavity mode thermal drift is accomplished by cavity design following Eq. 2.22 and the mirror thermal drift is managed by creating an athermal DBR mirror design following Eq. 2.20. The gain drift is not compensated for, but rather the bandwidth of the gain can and must be wide enough to function across the entire temperature range of the application space. Thermal roll-off via self-heating can also be partially accounted for either by selection of a high T_0, defined in Eq. 2.21 by [79], material such as QDs or by simply aligning the low-temperature lasing wavelength on the long wavelength side of the gain peak, as shown in Fig. 2.12(a) such that heating will push the gain peak towards the minimum loss wavelength of the athermal mirror decreasing the threshold before it increases again at the high-temperature range of operation where the gain drops. This method of gain offset is a common technique utilized in current uncooled

VCSELs.

$$\frac{1}{T_0} = \frac{1}{J_{th}} \frac{\partial ln(J_{th})}{\partial T} \tag{2.21}$$

$$\frac{d\lambda_C}{dT} \approx \frac{\lambda_C}{\int\limits_{L_C} n_g dL} \Big(\alpha_{sub} \int\limits_{L_C} n_{eff} dL + \int\limits_{L_C} \frac{dn_{eff}}{dT} dL \Big) \tag{2.22}$$

Equation 2.22 represents cavity mode drift $d\lambda_C/dT$ for an FP laser or similar laser with broadband mirrors and multiple sections. The integrations are done over a single round trip laser path length, L_C, of the modal properties n_g, n_{eff}, and dn_{eff}/dT. Finding the criteria that upholds the condition $d\lambda_C/dT = 0$ is possible by use of a waveguide section with a negative TO coefficient if its length is appropriately weighted with the sections of the laser that have a positive TOC, such as the semiconductor gain region. Figure 2.14 plots the wavelength drift as an example. Assuming that any additional packaging required to offset the gain's bandgap change with hydrostatic pressure or other such methods are prohibitive, it is appropriate to use conventional semiconductor parameters. The platform selected for this example is the Hybrid Silicon Laser Platform [80] with a modification where TiO_2 cladding is added as an alternative to SU-8, a UV curing photoresist. Therefore, with a single lithography, the waveguide width of the passive section with $dn_{eff}/dT < 0$ and the DBR section with $d\lambda_{DBR}/dT \approx 0$ can be integrated. Using the model based on data collected by Guha et al. [27] at 1550 nm on 220 nm SOI, a 200 nm wide waveguide with 500 nm of TiO_2 shows a $d\lambda_C/dT =$

-20 pm/K, and a 270 nm waveguide guide is nearly athermal. The 200 nm guide results in a dn_{eff}/dT for the negative TO compensation guide of ~-4.3×$10^{-5}K^{-1}$. This is compared to dn_{eff}/dT for the gain section of ~2×$10^{-4}K^{-1}$ or a ratio of just under 5 in length for the gain to negative TO waveguide. Therefore, for short gain lengths possible on the Hybrid Silicon Laser Platform, the total cavity length need not be greater than 1mm provided a strong negative TO guide is available in the platform, as seen in Fig. 2.14. An issue does arise when using DBR lasers that are ~1mm long, which is that the FSR or the cavity is 0.4 nm, stipulating that to get a grating stop bandwidth on the order of the free spectral range of the cavity to avoid mode hopping requires a grating strength ~10 cm^{-1}.

$$\frac{dL_{eff}}{dT} \approx \frac{\alpha_{sub}L_g}{2} sech^2\Big(\frac{2\delta L_g}{\lambda_0}\Big) - \frac{L_g}{\delta}\frac{d\delta}{dT}\Big(1 - \frac{\lambda_0}{2\delta L_g} tanh\Big(\frac{2\delta L_g}{\lambda_0}\Big)\Big) \tag{2.23}$$

However, the length of the grating for appropriate reflectivity would then be such that the cavity length itself would grow considerably as the effective grating length, L_{eff}, would become significant to the total cavity length. This is important as dL_{eff}/dT is proportional to the grating length L_g as shown in Eq. 2.23 where δ is simply the difference in effective indices of the two periodic grating sections n_{eff1} and n_{eff2}. The $L_{eff} \to L_g$ case is not shown in Fig. 2.14, which has fixed grating lengths of 250 μm for all curves. This logical progression implies that ideally the platform best suited to this design is one that has not been created yet to utilize active III-V integration on waveguides both capable of highly negative

and athermal TO drift. For example TiO_2 core guides demonstrated with both ~-100 pm/K and <-3pm K^{-1} drift [81]. Or if narrow FSRs with these thermally compensated lasers are not avoidable, an intracavity filter should be used, as discussed below and shown in Fig. 2.13(b).

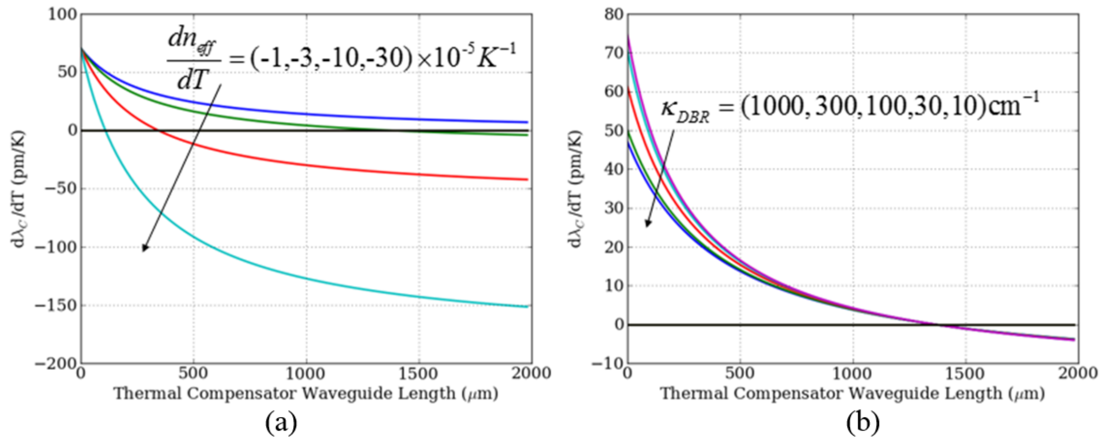


Figure 2.14: Athermal DBR laser drift in pm/K vs. the length of a thermal compensator waveguide as a function of (a) different passive compensator drifts dn_p/dT and (b) athermal grating strengths κ_{DBR}. Hybrid silicon gain region length assumed to be 200 μm with compensator made of a Si core with TiO_2 cladding, and 250 μm combined grating length for front and back. (a) assume κ_{DBR} = 300 cm^{-1}, (b) assumes dn_p/dT = -3$\times$10$^{-5}K^{-1}$.

Plotted in Fig. 2.14 is the trade-off of the athermal compensator waveguide length with the choice of compensator waveguide and grating design. When using a silicon waveguide compensator such as that in Fig 2.13(c) with a $dn_{eff}/dT \approx$ -3$\times$10^{-5} K^{-1} for waveguides around 200 nm wide and 1.5mm long. Alternatively, using a waveguide such as the TiO_2 core guide in Fig. 2.13(d) has been demonstrated with $dn_{eff}/dT \approx$ -17.5$\times$10^{-5} K^{-1}, which would reduce the required

compensator length to 300 μm for an athermal design. Figure 2.14(b) shows little impact of grating strength with selection of the compensator length.

Figure 2.13(b) shows an ARF-DBR utilizing a ring resonator as an intracavity filter. If the design of the passive straight waveguides of the laser is such that they compensate the positive TOC of the SOA as in the athermal DBR example, then this filter can be athermal as cavity modes will not drift out of the filter. However, as precisely aligning the cavity modes to the resonance of the ring may prove to be beyond fabrication tolerances, a simple feedback scheme can be utilized to maximize power to the wavelength monitor photo-diode, λ-PD, by tuning the intracavity ring filter so the lasing mode is centered about the rear athermal DBR. A number of feedback schemes would suffice here, for example a proportional-integral-derivative (PID) controller. The power monitor photodiode, P-PD, also is in a simple feedback with the SOA bias to regulate the output power of the laser out of the front facet without tapping the signal power at the output of the cavity. Of course, one can still tap the actual output with an additional monitor PD, but this utilizes an existing port in the architecture and will act as a fair and representative signal in most regimes of SOA operation, which is already constrained by the lasing condition.

A ring filter is needed as the cavity length of a standard DBR reduces the free-spectral range (FSR) to a point where it is not reasonable to integrate both

narrow band (low grating strength, kappa) and high reflectivity (longer length) mirrors. Therefore a ring filter is needed to prevent mode-hopping observed in previous implementations of DBR lasers. Figure 2.12(b) show such a filtered mirror response. The DBR bandwidth requirement is therefore loosened to the channel spacing less any fabrication variation inherent in the technology used to create the athermal grating rather than something as narrow as the laser FSR. Designing the ring filter for this cavity requires a ring with a bandwidth on the order of the FSR of the cavity and a tuning range on the order of the bandwidth of the DBR. The rings FSR can be smaller than the channel spacing and is ideally slightly less than the DBR bandwidth. The coupler designs can be made utilizing Fig. 2.15.

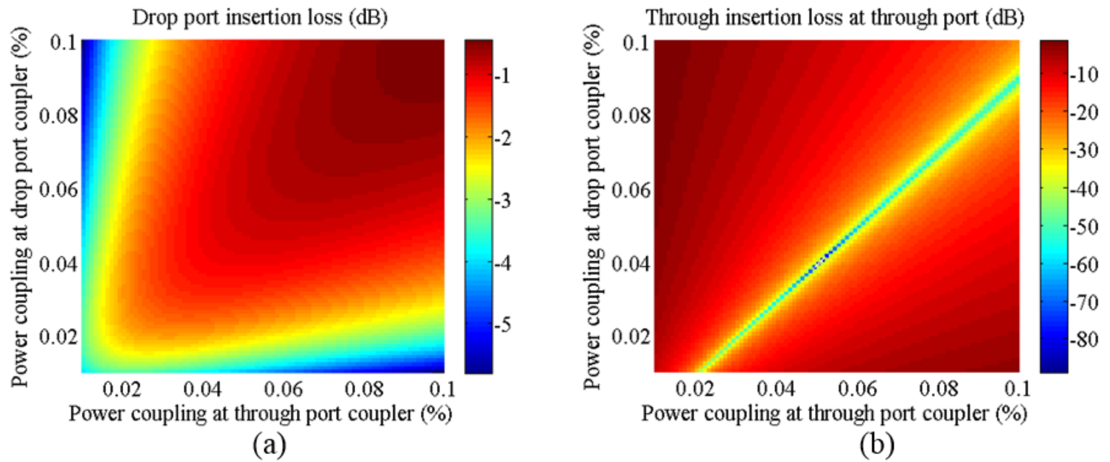


Figure 2.15: (a) Drop port insertion loss in dB of a ring filter (i.e. from the SOA to the rear mirror in Fig. 2.13(a). (b) Through port insertion loss in dB (i.e. from the SOA to the P-PD in Fig 2.13(a). Assumes 1dB/cm propagation loss, 25 μm ring radius.

Shown in Fig. 2.15(a), a symmetric design where both through and drop couplers are identical is preferred for lowest total laser loss with the ring as an intracavity element, as in Fig. 2.13(a). There is a little bit of flexibility in adding an asymmetry in the ring coupler design without a large variation in drop port insertion loss, however you can stumble into (or near) the quasi-critical coupling region denoted by the sharp increase in through port insertion loss in Fig. 2.15(b), which will block the through port transmission to a monitor PD. As is clear from Fig. 2.15(a), this through port critical coupling regime doesn't significantly change the intracavity laser loss, just the ratio of power out of the multiple outputs of the laser cavity. Therefore, the additional energy is lost in radiation out of the ring.

Finally, an additional example is shown in Fig. 2.16 with an integrated wavelength locker. This wavelength locker uses a quarter wavelength shifted DBR as a filter to the input of the integrated wavelength monitor photo-diode. Utilizing either a wavelength operation point on the steep section of the high transmission notch or the maxima of this notch to reduce back-reflections into the laser, a dither can be added to a phase section of the tunable laser to make a signal for the monitor diode which can be interpreted through the PID controller on the co-packaged Tx driver board. An athermal grating is used for this filter because it has a higher fabrication tolerance to hit a precise wavelength than a ring to eliminate tuning.

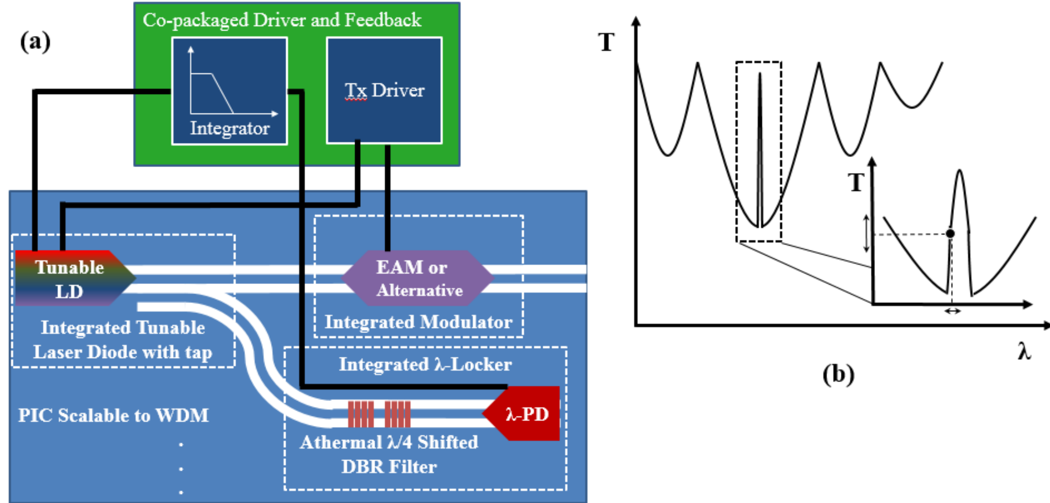


Figure 2.16: (a) Schematic of an integrated transmitter with on-chip wavelength locker utilizing a quarter wavelength shifted DBR as a filter to an integrated monitor photodiode. This is co-packed with the control electronics. (b) the transmission of the wavelength locker filter concept is plotted with a slight wavelength dither on the high slope region of the transmission notch caused by the $\lambda/4$ shift.

2.4.3 Athermal laser design summary and conclusions

An argument for targeting denser uncooled channel spacing was made followed by a review of how to achieve this with athermal designs. A simple athermal circuit concept implementable in MZIs and AWGs on most platforms is reviewed and shown to be limited for IIR filters, such as rings and DBRs. Therefore, materials based athermal waveguides are presented as an alternative to overcome such limitations with a brief theoretical description. The presence of SiO_2 lower cladding in SOI enables increased confinement in a negative TOC material top cladding of a Si core waveguide, making it possible to achieve both zero and negative waveguide

TOCs. Therefore, athermal laser designs based on a modification of the Hybrid Silicon Laser are proposed to utilize such athermal waveguides without the use of external wavelength lockers required for conventional tunable lasers solutions. These proposed designs encompass entirely passive athermalization, and simple feedback loops with passively athermalized integrated reference filters using athermal DBR gratings. We project that such designs will provide the basis for a new class of uncooled lasers for photonic integrated transmitters.

2.5 Conclusions

This chapter on athermal devices and designs for integration on Si covered some background for current solutions to athermalized circuits with a key point that circuit-based athermalization without sections of negative TOC material can only create FIR filters such as MZIs and AWGs. IIR filters such as gratings and rings require material based athermalization. Fabricated, tested and analyzed waveguides using TiO_2 as the negative TOC material were demonstrated in rings and gratings. Through deeper analysis of the actual devices, the key topics of thermal stress and second order material TO behavior were discovered and quantified.

The need for athermal PIC circuit design will increase as more uncooled solutions are implemented. If this work is done on Si, we recommend TiO_2 as a compatible material with more tolerance to environmental degradation than polymer alternative. However, further exploration in this area should consider the effects reported here as important details to consider in future designs.

Chapter 3

III-V/Si_3N_4 Heterogeneous Laser Integration

3.1 Introduction

Traction has been made in recent years in development of III-V/Si heterogeneous lasers using wafer bonding of III-V InP based material to silicon-on-insulator (SOI) in order to leverage Si fabrication facilities, diagnostics and process controls [80, 82]. The emergence of high volume datacom products using this technology will open these facilities to other products, including using multi-project wafers with different bandgap materials [83]. In this work we utilize bonding technology to enable integration of new components at shorter wavelengths, starting with an InGaAs/GaAsP MQW laser operating near 1060 nm. This wavelength is absorbed in a silicon waveguide, so we use a SiO_2 clad Si_3N_4 waveguide, which is coupled to III-V via a tapered mode converter. Figure 3.1 shows our concept of

a directly bonded III-V laser onto Si_3N_4 waveguides and processed post-bond to achieve lithographic alignments and resolution for III-V device fabrication. This approach can be used at wavelengths from the visible to the infrared to integrate lasers and other active components to low-loss Si_3N_4 waveguides and devices such as arrayed waveguide gratings (AWGs).

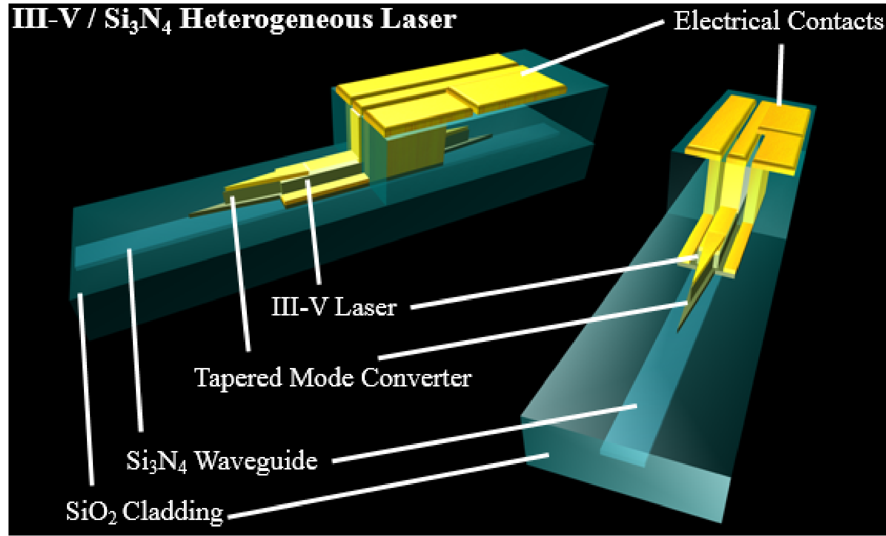


Figure 3.1: Schematic of III-V/Si_3N_4 heterogeneous laser directly coupled via III-V tapers through the III-V/SiO_2 cladding bonding interface. (artwork courtesy of Martijn Heck)

Because of its low water absorption, 1060 *nm* is great for applications in sensing, free space communications, medical applications, LiDAR, high power low divergence lasers [84], and seed sources to fiber lasers [85]. Integration at these wavelengths can enable novel systems for high power beam combining, mode converters for lower divergence beams, lithographically defined interferometric tech-

nologies such as balanced photodetection and so much more. Utilizing Si_3N_4 passive waveguides is desirable for integrating devices across a broader spectral range than anything previously demonstrated [3] or for circuits requiring low loss, less than 0.1 dB/m at 1.58 μm [86], or the order of magnitude lower thermal drift compared to Si. Finally, the cost of such circuits built on bulk Si can be lower than SOI based designs.

3.2 InGaAs/GaAsP multiple quantum well lasers on Si

InGaAs multiple quantum well (MQW) lasers were grown on GaAs and bonded to Si_3N_4 planar lightwave circuits (PLCs) fabricated on a silicon substrate. The argument for such a marriage of materials is made in Section 1.1.1.

3.2.1 Fabry-Pérot lasers

Figure 3.3 details the process flow for both the lasers and tapered mode converters. Note that no Si_3N_4 waveguide is present under the Fabry-Pérot lasers as the mode is confined by the III-V and AlGaAs oxidation aperture in Fig. 3.2. Also, the tapered test structures do not have metallization or a p-mesa as the MQW material would absorb the transmission. 200 nm of stoichiometric LPCVD Si_3N_4

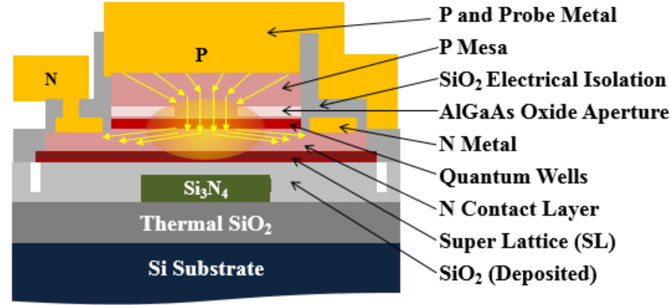


Figure 3.2: Laser cross-section. In bulk of the gain region, mode is entirely in III-V so Si3N4 waveguide width reduces to zero over the course of the tapered mode converter and the mode is guided by the AlO_x aperture

is deposited on thermally oxidized Si wafers, annealed at anneal at 1050°C for 7 hours to drive out any residual hydrogen and then patterned using DUV 248 *nm* lithography on an ASML S500/300 DUV stepper and a CHF_3:CF_4:O_2 inductively coupled plasma (ICP) dry etch. Patterned wafers are then clad with a PECVD SiO_2 partial upper cladding and chemically mechanically polished on a Logitech Orbis tool to planarize and achieve ∼0.5 *nm* RMS roughness. A gap from the Si_3N_4 waveguide to the bonding surface was targeted at 200 *nm* with a ±50 *nm* deviation measured across the 70 mm center of the 100 mm wafer. Vertical channels were etched into the SiO_2 to improve bonding [87]. InGaAs / GaAs MQW laser material grown by metal-organic chemical vapor deposition (MOCVD) is bonded to SiO_2 on Si following an O_2 plasma treatment and anneal at 300°C. The GaAs growth substrate is lapped to ∼100 μm and then selectively etched using a NH_4OH:H_2O_2 (1:30) solution sprayed by a Venturi spray head which draws the

solution and aggressively sprays it with N_2 gas onto the GaAs substrate. The solution is recycled for the 30-60min duration of the etch (depending on the final lapped substrate thickness) without noticeable change in selectivity relative to the 10-200 nm InGaP etch stop layer. 500-200 nm of $Al_{0.8}Ga_{0.2}As$ has also been observed to act as a sufficient etch stop, though the selectivity is less and the etch stop is prone to oxidation post substrate removal, so it should be removed with buffered hydrofluoric acid directly following substrate removal.

Laser p-mesas were then patterned and dry etched using a Cl_2:N_2:H_2 ICP etch with a SiO_2 hardmask and stopped in the lower n-GaAs contact layer using a laser monitor. The vertical channel mask was reused to open all vertical channels (VCs) before an AlGaAs wet oxidation was performed at 365°C in a 50 mm Lindberg furnace with 10sccm of N_2 carrier gas bubbled through an 80°C deionized wafer beaker. The VCs must be reopened, because pressure in covered VCs causes them to burst and redeposit III-V onto the sample during the anneal. The oxidation aperture forms both a current and optical guide, as shown in Fig 3.3. Two additional tapers were formed by dry etching and selective wet etching to stop cleanly on the top of an InGaAs/GaAsP superlattice and the bonding surface. AuGe/Ni/Au (70/15/500 nm) n-metal was e-beam evaporated onto $2{\times}10^{18}cm^{-1}$ n-GaAs and lifted-off, rapid annealed at 420°C for 30s, then covered in a PECVD SiO_2 electrical isolation layer. Vias were made in the isolation and then a Ti/P-

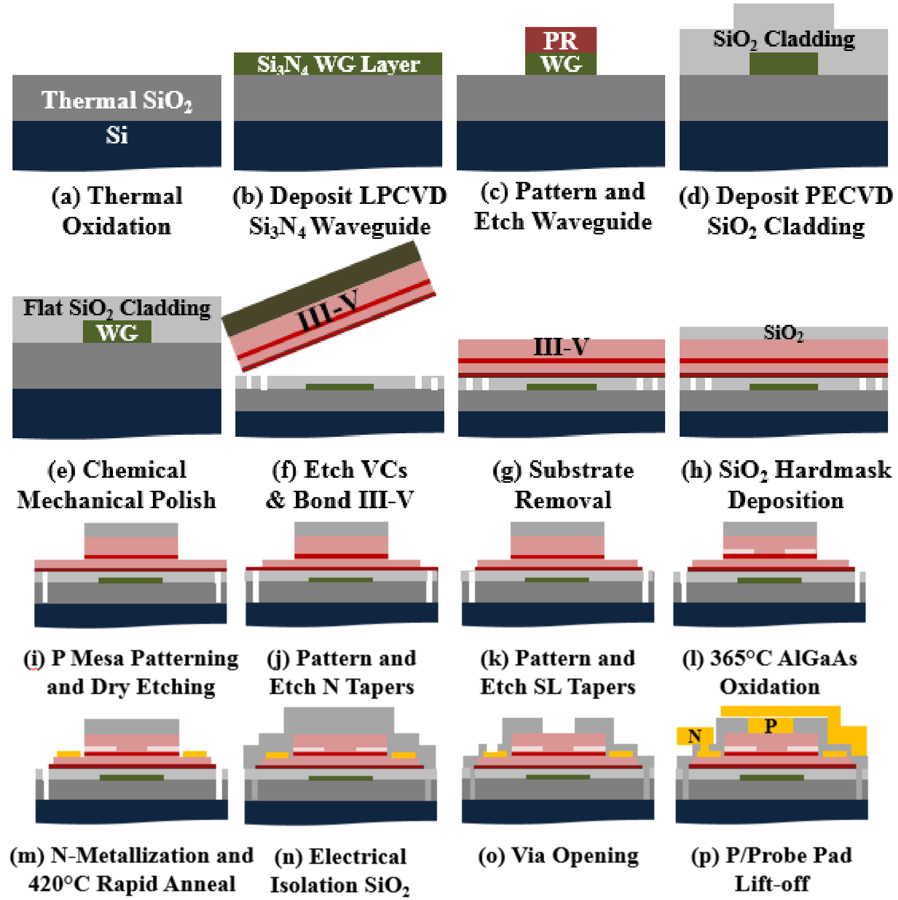


Figure 3.3: Process flow for Fabry-Pérot lasers and tapered mode converters.

t/Au (5/30/1500 nm) e-beam evaporation was made to $1{\times}10^{18}cm^{-1}$ p-GaAs and lifted-off to form probe pads to the n-contacts. Two types of experiments were done to prove the feasibility of the concept. First, we fabricated lasers on a thermal oxide layer. Secondly, we fabricated passive III-V to Si_3N_4 taper loss test structures.

A cross-section of these devices is shown in Fig. 3.2. The key dimensions that were varied in this run were the mesa width and length. The mesa width varied the width of the oxidation aperture as all of the devices were oxidized at the same time. P-mesa widths were varied from 11-13 μm. resulting in oxidation apertures from 3-5 μm following the AlGaAs oxidation. Additional splits were made for the p-contact width from 1.5-11 μm resulting in insignificant variation.

Table 3.1: Epitaxial layer design for Fabry-Pérot lasers

Function	Material	(%) Al	t (nm)	Doping	Type
Bonding SL	InGaAs/GaAsP	-	72	2.7E+18	n-Si
n-Contact	GaAs	-	200	2.7E+18	n-Si
n-GRINSCH	AlGaAs	10→30	48	2.7E+18	n-Si
Barrier	GaAs	-	10		UID
(3x/2x)QW/Barrier	InGaAs/GaAsP	-	8/8		UID
Barrier	GaAs	-	10		UID
p-SCH	AlGaAs	30→80	88	7.5E+17	p-C
AlO_x aperture	AlGaAs	98	50	7.5E+17	p-C
p-Cladding	AlGaAs	80	1500	7.5E+17	p-C
Grade	AlGaAs	80→10	200	7.5E+17	p-C
p-Contact	GaAs	-	100	1.0E+18	p-C
Etch stop	InGaP	-	200	1.0E+18	p-C
Buffer	GaAs	-	500	1.0E+18	p-C
Substrate	GaAs	-	625000	>1E+18	n-Si

Electrically pumped Fabry-Pérot lasers were made by dicing III-V on SiO_2 on Si bars into different lengths, and polishing these to create facets. Multiple mesa widths were fabricated to vary the width of the current channel. Confinement factor in the quantum wells was simulated to be 0.09 regardless of aperture width.

A p-mesa width of 12 μm with 4 μm wide current apertures had the best results with the most working lasers, resulting in the cleanest analysis, and these data are, therefore, presented below unless otherwise specified. Table 3.1 shows the layers of the MQW InGaAs/GaAsP MOCVD epitaxial material pre-bonding.

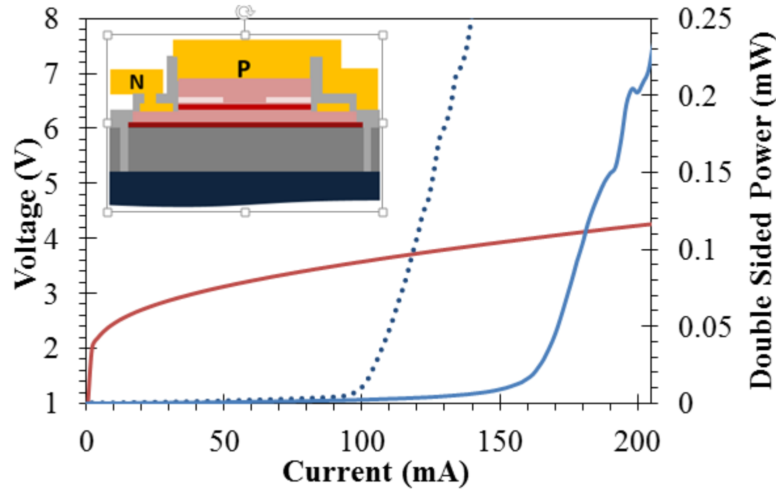


Figure 3.4: CW (red) IV and (blue) LI curves of a 2400 μm long Fabry-Pérot laser. Inset shows a cross-sectional schematic.

Continuous-wave (CW) operation was observed at 12.3°C in a 2400 μm long laser whose optical power-current-voltage (LIV) curves are shown in Fig. 3.4. These devices suffer from high p-contact resistivity ($>13\Omega \cdot mm$ at 200 mA in 4×2400 μm laser shown) and turn-on voltage (>2 V) both believed to be due to residual InGaP between the p-GaAs and p-metal. Additional material degradation may be caused by the oxidation anneal evidenced by a decrease in the measured PL intensity of bonded material before and after this anneal step.

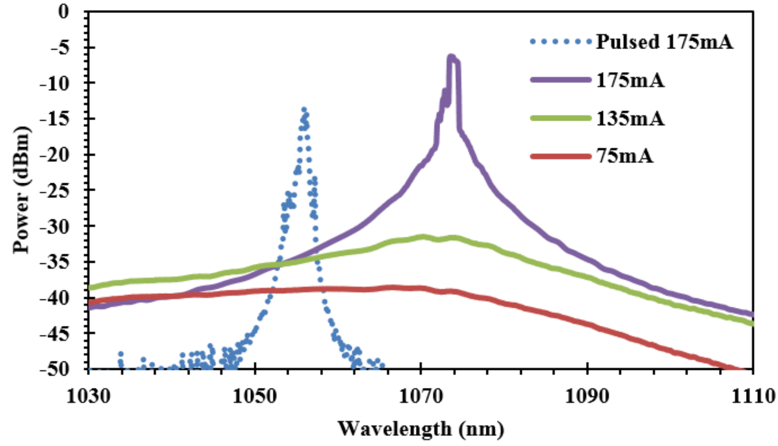


Figure 3.5: CW spectral output below and above the lasing threshold.

Additionally, the thermal impedance is higher in these designs than those on a native substrate owing to the 5 μm of lower SiO_2 cladding selected for better compatibility with thin Si_3N_4 cores for low-loss [86]. This is shown in the inset in Fig. 3.4.

Spectral measurements were made on the CW laser confirming the lasing peak to be at 1073 nm, as shown in Fig. 3.6. This can be compared to a 1030 nm photoluminescence peak at room temperature before bonding and the 1056 nm lasing peak of the same laser under pulsed operation. From this the increase in temperature at the junction is approximated to be 42°C, assuming 0.5 nm/K change in the quantum well bandgap. This puts the calculation for the thermal impedance at 49°C/W for this 2.4mm device. This is expectedly higher than that reported on InP type Hybrid Silicon Lasers with 1 μm buried oxide [88].

This is in reasonable agreement with simulations of similar laser structures in COMSOL with 5 μm lower SiO2 cladding from Section 3.5 when you account for mesa width and length. As a result of this self-heating, the threshold current was seen to increase from 100mA to 163mA for pulsed and CW respectively as shown in Fig. 3.4. Ideally, such devices would be flip-chip bonded to AlN or other high thermal conductivity electrical interconnection boards to improve the thermal performance, as discussed in Section 3.5.

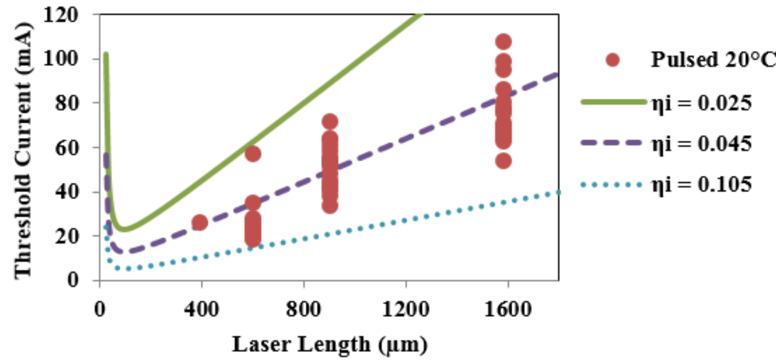


Figure 3.6: 20°C pulsed threshold current data for 12 μm mesas with 4 μm wide current apertures 300°C O_2 plasma assisted bonded to 5 μm of SiO_2 on Si.

Different length lasers were tested pulsed with 600ns pulses at 1 kHz repetition rates at 20°C to avoid device self-heating. Threshold currents below 20mA for 600 μm long lasers are shown in Fig 3.6. The internal loss was calculated by cutback measurements for devices with 12 μm mesas and 4 μm wide current apertures to be 6.2 cm^{-1}. The analysis used Eq. 3.1 and the curve fit to the best devices of each length in terms of inverse differential quantum efficiency, $1/\eta_d$, plotted in

Fig. 3.7 [55].

$$\frac{1}{\eta_d} = \frac{\alpha_i}{\eta_i ln(1/R)} + \frac{1}{\eta_i} \tag{3.1}$$

The internal quantum efficiency, η_i, was calculated to be 4.5% from the cutback analysis shown in Fig 3.7. Fig. 3.6 plots with higher and lower bounds of the data using fitted curves assuming internal loss, α_i, of 6.2cm^{-1} and facet reflectivity R = 0.32 used in Fig. 3.6 . This performance may be partially owed to poor IV characteristics. These devices suffer from high p-contact resistance.

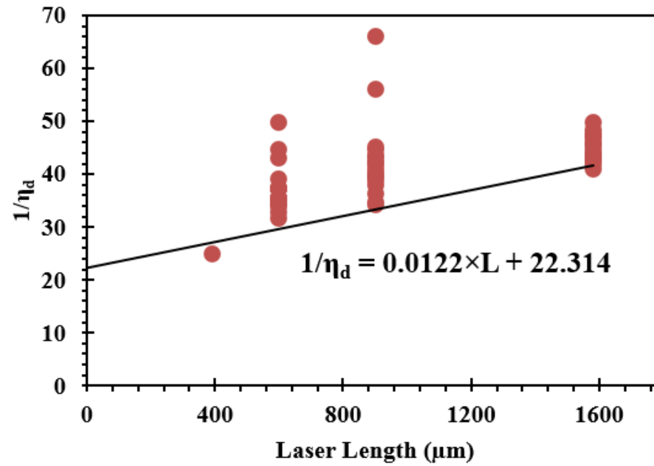


Figure 3.7: $1/\eta_d$ plotted v. laser length with a linear fit to best devices of each length to extract internal parameters using Eq. 3.1.

Finally, a series of aperture widths were explored to get some understanding of the best overlap of the injected carriers and the mode. As the width of the aperture increases so does the mode and so do the carrier profiles. Because this is a top contact device, it is not fair to think of the pumping as a uniform profile

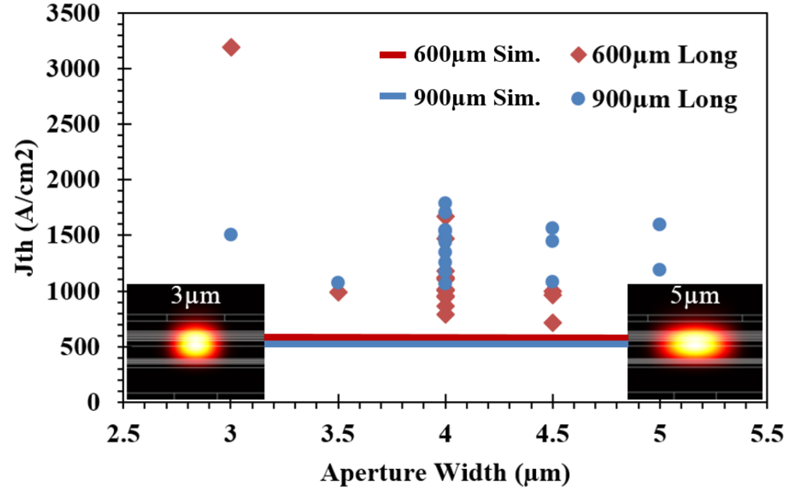


Figure 3.8: Threshold current densities of pulsed laser as a function of their aperture width.

through the aperture so simple models do not explain the relationship of threshold current density and aperture width. Once the current passes to the n side of the aperture, it spreads to either side of the mesa taking the path of least resistance. In narrow aperture devices this means that the mode is not as wide as the carrier distribution, in wider apertures, the mode may be too wide and overlay well with the bi-modal distribution of carriers crowding both edges of the aperture. Figure 3.8 shows the current density of pulsed results for two lasers lengths, 600 and 900 μm, v. aperture widths from 3-5 μm.

3.3 III-V to Si_3N_4 tapers

Device structures were measured to quantify the taper loss of adiabatic mode converters from the low-index Si_3N_4 waveguide to the high index III-V device layers. These structures were designed with a series of tapers in the III-V while the Si_3N_4 maintained a constant width.

Table 3.2: Epitaxial layer designs for III-V to Si_3N_4 taper structures

Taper	Layer	Material	t (nm)	Index(1030nm)
N	Sacrificial Layer	InGaP	50	3.215
N	Contact layer	GaAs	250	3.503
—	Taper interface	—	—	—
SL	SL Etch Stop	InGaP	20	3.215
SL	Bonding SL	InGaAs/GaAsP	62	3.503

Simple passive structures without a quantum well mesa were made in serially repeating test structures to isolate taper loss. A section of the layout and a zoom in of a single device is shown in Fig. 3.9.

The 100 μm straight section was selected to match the intersection with the quantum well mesa of a linear in-plane laser that has an oxidation aperture index guide down the center to make the structure single mode. These test structures however, have a multi-mode straight segment, that showed some spectral dependence for some taper design splits, but only for straight lengths greater than 100 μm. Repeated test structures only showed periodic oscillations with wavelength that are attributable to reflections cause from the III-V to Si_3N_4, but nothing to

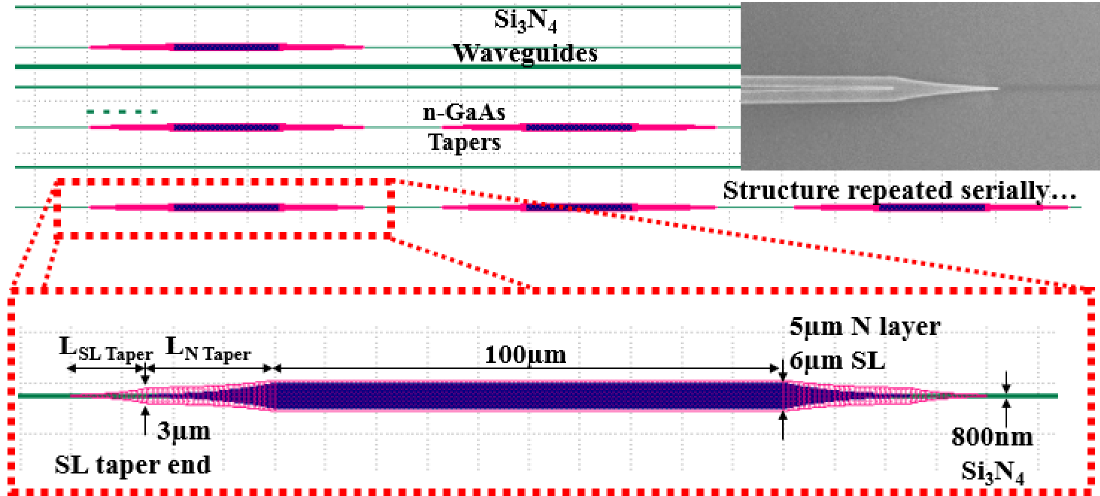


Figure 3.9: Layout of repeated taper structures with labels on key geometries. Mask splits included length of SL taper, and length of N Taper. Taper tips ~200 *nm*. Structures do not include active quantum well mesa.

suggest that the multi-mode behavior impacted the measurement. Because of the oscillations, transmission spectra were captured over a range of wavelengths from 990-1090 *nm*, normalized to a transmission though a straight waveguide without III-V and then averaged. The error in this method along with the error found from variations in repeated measurements of identical reference waveguides without III-V are represented by the error bars in the graphs and taken to be the sum of the standard deviations of these two sources of error and are plotted in Fig. 3.10.

The measurement results indicate that the shorter n-taper lengths are preferred to long tapers. That does not agree well with the simulations used to design this

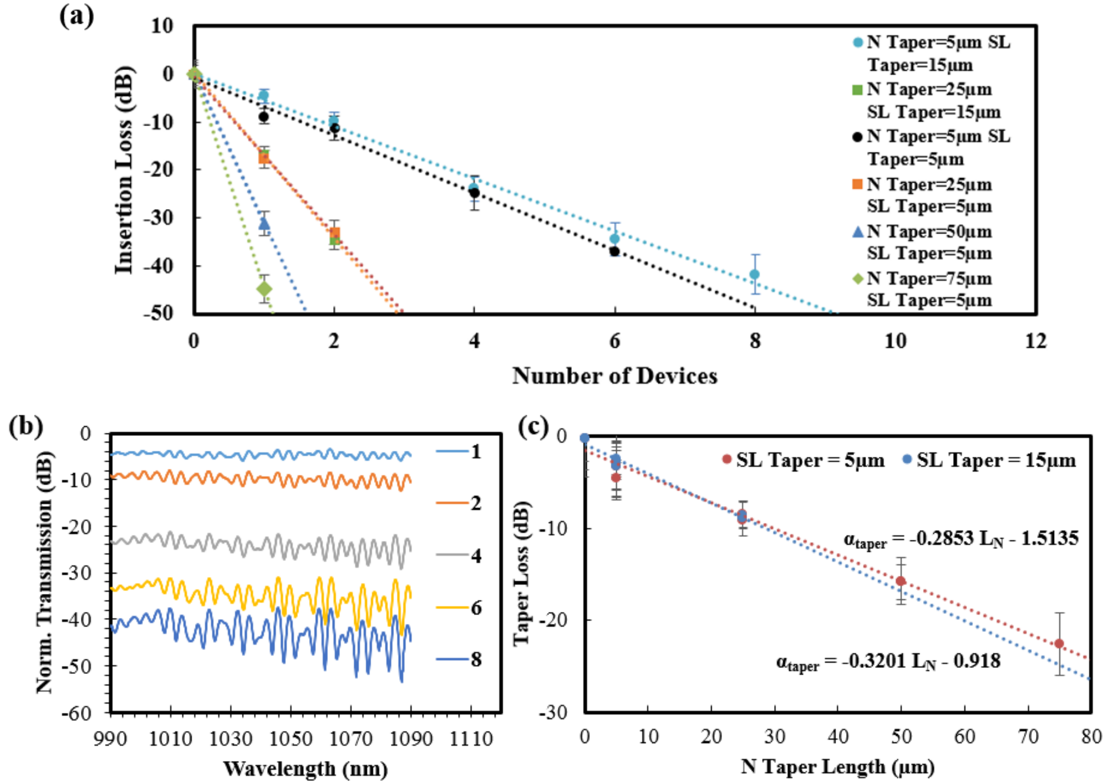


Figure 3.10: (a) Measured insertion loss for repeated passive III-V to Si_3N_4 tapers plotted by number of serial repeats of a single device. (b) Normalized transmission spectra for (1, 2, 4, 6 & 8) repeats of lowest loss taper. (c) Taper loss is plotted from the repeated taper data in (a) after removing bulk loss.

mask split. There is little or no measurable difference between the two SL taper lengths selected of 5 μm and 15 μm. Additional structures with different lengths of straight III-V sections were tested to measure the propagation loss of this segment and remove it from the insertion loss to yield a loss of each taper plotted in Fig. 3.10(b). This propagation loss was found to be 44.5 dB/cm. Therefore, the lowest loss taper design of 2.5±0.75 dB/taper was measured with a SL taper length of 15

μm and an n-taper length of 5 μm. Two limits have been identified to improve this design. First, the width of the SL taper at the start of the n-taper tip is simulated to be more significant than previously anticipated. The selection on the mask was 3 μm with the intention of ashing back the tapers to reduce the actual device width, however inspection post ashing was only a couple hundred nm reduced as seen in Fig. 3.9. This parameter should be reduced in future similar designs to improve the coupling loss. A simulated optimum value would be closer to 700 nm. Secondly, there is a loss mechanism that clearly scales strongly with length. Future focus should be given to shorter taper designs.

3.4 Integrated DBR mirrors in Si_3N_4 waveguides

To make an integrated laser, there are a few options for mirrors that can be explored. A very common choice is a distributed Bragg reflector (DBR) because of the wavelength selection function that it adds, eliminating the need for an intra-cavity filter. This type of mirror functions by a simple periodic perturbation of the waveguide mode that in a first order grating has a periodicity of half a wavelength, and scales with order such that the period is a full wavelength for second order, 1.5 wavelengths for third order etc. as detailed in Eq. 3.2, where m is the order λ_{Bragg}, is the Bragg wavelength, n_{eff} is the effective index of the

grating and Λ is the period of the grating.

$$\Lambda \approx \frac{m\lambda_{Bragg}}{2n_{eff}} \tag{3.2}$$

These repeated perturbations scatter incoming light with a strong wavelength selective in-phase reflection back into the waveguide from which the light came. An accurate theoretical analysis of DBR gratings can be made using coupled mode theory between the forward and backward modes. This is well documented in a number of textbooks including [55] so I will not repeat it here. I will however include formulas from this method of derivation to be used in the analysis of the devices measured.

Integrated DBR mirrors for heterogeneous lasers can either be placed into the III-V by etching the III-V before conducting an aligned bond [89], etched into the passive waveguide directly underneath the III-V [90], or outside the III-V [91]. Of theses approaches, etched III-V devices require accurate alignment during bonding, and gratings directly underneath the III-V are sensitive to the bonding oxide thickness, so the most repeatable results arguably can be achieved in placing the mirrors outside the III-V region in the passive waveguide. Additionally, in this case the mirror thermal drift will be that of the passive waveguide materials and not III-V, an attribute utilized for non-silicon waveguides in Section 2.4 to reduce laser thermal drift. However, with passive DBRs additional loss will be added in the laser cavity transitioning from the III-V gain to the passive waveguide.

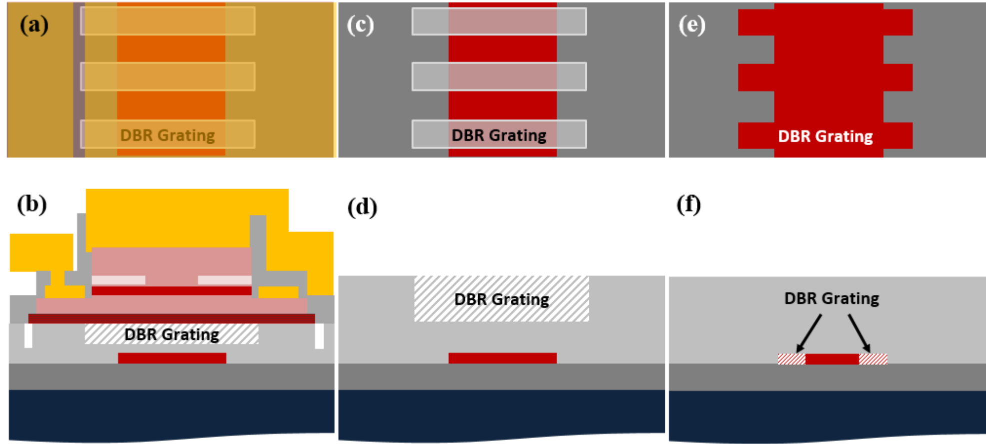


Figure 3.11: (a-b) Top and cross-section of surface corrugated gratings underneath bonded III-V lasers (c-d) Top and cross-section of surface corrugated gratings into top cladding of passive waveguide. (e-f) Top and cross-section of sidewall passive gratings.

Three potential grating configurations are diagrammed in Fig 3.11. The first two use surface corrugated gratings etched into the upper SiO_2 cladding. For III-V lasers bonded on top of these gratings, air gaps can be quite a fabrication tolerant modal perturbation for a mode in the III-V and even if the etch is deeper than intended and punctures the Si_3N_4 core, the grating strength of the III-V mode is not detrimentally impacted. This is because as the mode is strongly confined to the III-V, the perturbation of the air compared to the SiO_2 only occurs within the first 10s of nm from the III-V surface. Also, as the gratings can be patterned on the waveguide surface prior to bonding, no precise bonding alignment is required.

However, surface gratings are not ideal for passive gratings (outside of III-V regions) for two reasons that came up when developing processes for their use in heterogeneous laser integrations. Firstly, the gratings should be placed in the final cladding layer or they will be filled during subsequent cladding depositions. Unfortunately, this puts this process step near the end of the entire process flow on a wafer with high morphology and restricts the implementation of probe pad or thermal heaters on top of the grating for tuning as the metal would fill the corrugations. Secondly, if the etch actually does penetrate the core, the grating strength sees a rapid increase with etch depth into the core and the Bragg wavelength also shifts rapidly with the change in effective index cause by this strong perturbation. This unintentional core etch becomes very possible if the target depth is close to the core. Especially as CMP of the partial upper cladding before bonding adds uncertainty to total cladding thickness and resulting etch end point. This example of an etched core was measured to have extremely high grating strength and loss in some test structures when first exploring these surface corrugated structures. This is one reason we moved away from surface corrugations in favor of sidewall gratings.

The second type of DBR mirror are sidewall gratings as shown in Fig. 3.11(e-f). I must credit co-authors Michael Belt and Martijn Heck for the testing and layout of the first of these structures at UCSB with 100 nm thin Si_3N_4 strips

[92]. I provided testing advice, analytical support, and SEM characterization to understand the data. I have also designed, fabricated and demonstrated such gratings near 1 μm in 200 nm thick strip geometries but have chosen to present the larger data set and cleaner analysis from our shared paper [92].

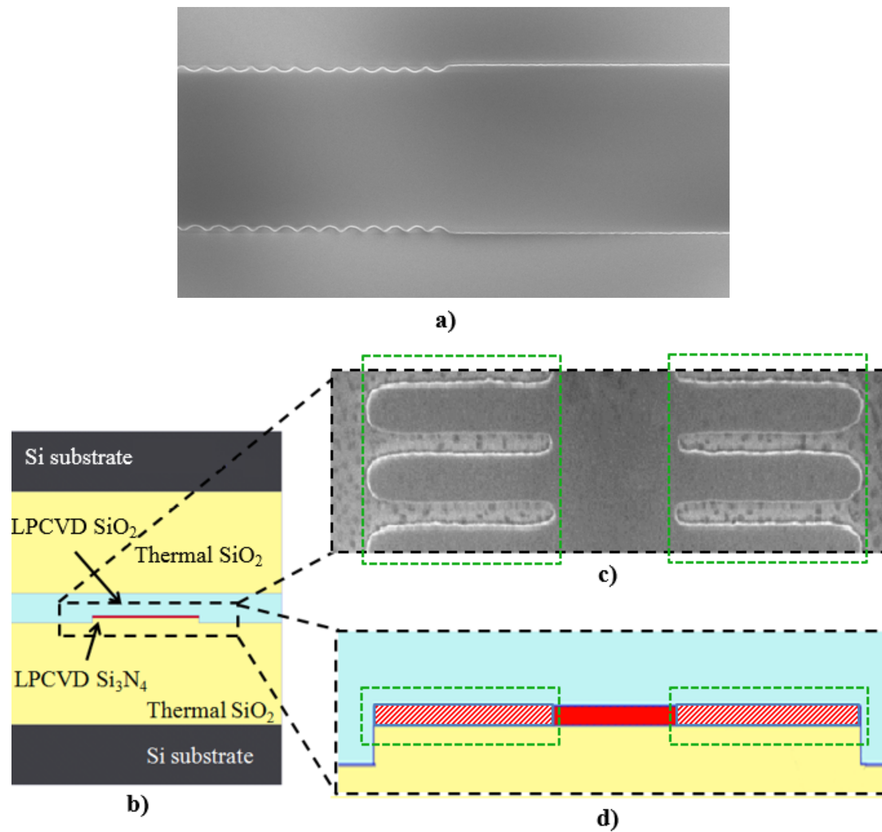


Figure 3.12: (a) SEM image of sidewall DBR in LPCVD Si_3N_4 strip with subtle perturbation. (b) Waveguide cross-section for C-band ultra-low loss waveguide. (c) SEM image of strong perturbation for reference to (d) a zoomed in cross-section with shaded grating areas.

Sidewall gratings hold the advantage of being defined in the actual waveguide layer, so they are the first lithography step performed on a planar wafer for the highest resolution. As the gratings are also entirely in Si_3N_4 and SiO_2 even for 200 nm thick cores at 1 μm wavelength the first order period is in excess of 300 nm. Therefore, it can be exposed using DUV stepper lithography. The practical limit we have found with UCSB's AMSL S500/300 DUV stepper (a 248 nm stepper) is around 300 nm for a NA of 0.63. In contrast, gratings in the III-V or under as in Fig. 3.11(a) must be exposed using holography or electron beam lithography (EBL) as their periods fall below 300 nm.

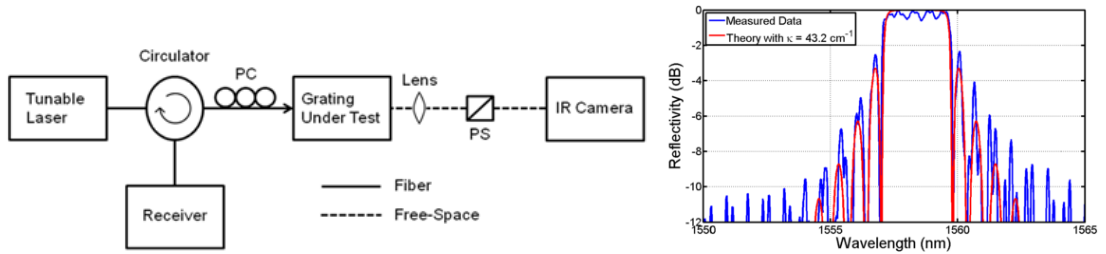


Figure 3.13: Reflection mode test setup and corresponding characteristic spectra for a 1mm DBR measured TE with $\kappa = 43.2\text{cm}^{-1}$.

These devices, shown in Fig. 3.12, were measured in reflection as shown in Fig. 3.13 and were found to have Bragg wavelengths and grating strengths that conform well to theory so long as you account for the increased duty cycle caused by the reflow of developed photoresist. Duty cycle is defined as the percentage of the grating period occupied by the widest waveguide section. The reflow was

performed to reduce total waveguide loss due to sidewall roughness. These gratings presented were all first order and many of them exhibited a very large change with width from the widest to the narrowest waveguide section. Rounding at the end of wide sections was not a significant portion of the total waveguide width as observed in Fig. 3.12(c). Therefore, a simple single cross-sectional mode simulation was made to quantify the change in grating strength, κ. The cross-section shown in Fig. 3.12(d) was simulated in Fimmwave with a finite element method (FEM) model with the index of the grating region (n_{gr}) (shaded in red and white and highlighted by the green boxes) defined by a weighted geometric mean of the core and cladding indices (n_{core}, n_{clad}) and shown in Eq 3.3.

$$n_{gr} = \sqrt{\left(\frac{DC}{2}\right) n_{core}^2 + \left(\frac{1-DC}{2}\right) n_{clad}^2} \tag{3.3}$$

Using this simulation technique and the index measurements from the ellipsometer at 1550 nm ($n_{core} = 1.988, n_{clad} = 1.445$) I was able to show duty cycle as the primary factor causing the raise of n_{eff} with increase in waveguide width difference, or perturbation in from the nominal waveguide width of 2.8 μm in Fig. 3.14.

Using this the effective index of this single simulation n_{eff} and the confinement factor of the grating region, Γ_{gr}, the grating strength kappa can be expressed as

$$\kappa = \frac{4}{\lambda}\left(\frac{n_{gr}}{n_{eff}}\right)^2 sin(\pi DC)\Gamma_{gr}(n_{core} - n_{clad}). \tag{3.4}$$

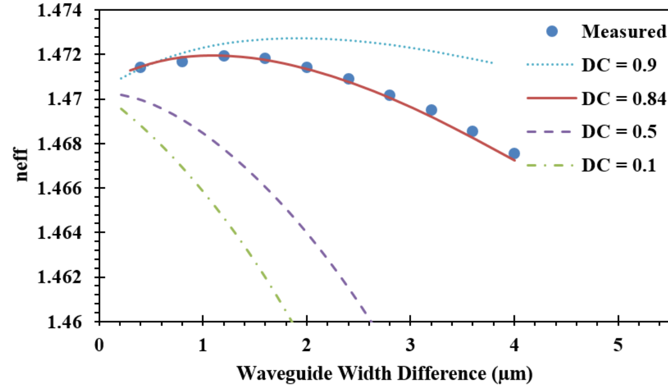


Figure 3.14: Measured and predicted grating n_{eff} for different narrow waveguide widths (or width differences from narrow to wide). The widest waveguide width is always 2.8 μm.

Using the values of Γ_{gr} and n_{eff} from a 2-D Fimmwave simulation the grating strength was found also to agree very well with measurement. The relationship of κ and stop bandwidth, BW, is expressed in Eq. 3.5.

$$\kappa = \frac{2n_{eff}\pi BW}{\lambda^2} \tag{3.5}$$

Figure 3.15 is a plot of these Fimmwave simulation results compared to values derived from measurements of the reflection spectrum bandwidth. The bandwidth was measured at the first null of the reflection spectrum.

3.4.1 Summary of integrated DBR mirrors in Si_3N_4

We demonstrated for the first time sidewall gratings in 100 nm thick Si_3N_4 planar waveguides with unperturbed loss below 5.5 dB/m over the range of 1540 to

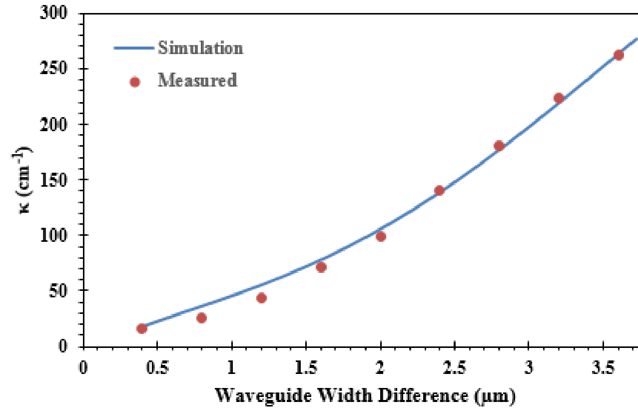


Figure 3.15: Measured and simulated grating strength for 1000 μm long gratings under TE excitation. The widest waveguide width is always 2.8 μm. The plot also gives fitted and simulated coupling constant values for the same set of gratings.

1570 nm. By this design it is possible to appodize gratings with a single etch with coupling constants, κ, that range from 13 cm^{-1} to 310 cm^{-1} enabling lithographically tailored filter functions. These have been shown to be well simulated using a single 2-D numerical mode solution and measured indices without additional parameter fitting.

3.5 Limiting self-heating in heterogeneous lasers with thick SiO_2 lower cladding

There are a number of approaches to limiting self-heating of lasers with thick SiO_2 lower cladding. This section discusses a few of them, including Au thermal

shunts in various locations and flip-chip bonding to a AlN carrier. These approaches are examined in the domain of very thick lower SiO_2 claddings required for integration with ultra-low loss Si_3N_4 strip waveguides, currently demonstrated with thermal SiO_2 claddings as thick as 15 μm. This analysis was conducted using 2-D COMSOL thermal heat transfer simulations.

3.5.1 Thermal impedance modeling in COMSOL

COMSOL is a finite element method (FEM) simulation tool that can perform any number of multi-physics simulations. For the purpose of this analysis a 2-D simulation was selected. The direction of propagation of light is assumed to vary insignificantly. This is not strictly true for structures with tapered mode couplers, but is a reasonable assumption for the bulk (untapered) section of the laser and is very reasonable for a Fabry-Pérot design.

The heat generation is assumed to occur in the center of the intrinsic region of the junction, that has the highest optical intensity and thermal effects due to absorption, highest resistance as it is intrinsic, and the most significant heterojunction interfaces, an additional source of photon production. This is a conservative assumption as the heat generation is actually more distributed. This is also nearly the furthest point from heat sinks such as the contacts. Addition heat sources such as contact resistance are ignored as their thermal energy is more readily diffused

into the contact itself than propagate toward the junction. Therefore, simulation results should fall on the high side of actual measurements but are believed to be an accurate representation for the purposes of selecting an appropriate thermal mitigation strategy.

Table 3.3: Material properties used in COMSOL thermal simulations

Material	k (W/m·K)	ρ (kg/m^3)	C_p (J/kg·K)
Au	317	19300	129
Si	130	2329	700
SiO_2	1.38	2203	703
GaAs	44	5316	550
$Al_xGa_{1-x}As$ [93]	$(.0227+.2883x-.30x^2)^{-1}$	8700	385
$In_{0.484}Ga_{0.516}P$ [93]	14.4	4460	376

The parameters used in this model have been selected from the COMSOL 4.3a MEMS materials library with the exception of ternaries referenced from other sources. All are listed in Table 3.3.

All lasers thermal impedances are assumed for 1mm long in-plane devices. Shorter lasers will have higher impedance inversely proportional to their length. In other words results quoted in K/W could just as easily be quoted in $K/(W{\cdot}mm)$ and then multiplied by device length.

3.5.2 Thermal impedance of heterogeneous lasers with thick SiO_2 lower cladding

Unlike a conventional PIC, heterogeneous lasers with thick SiO_2 lower cladding do not work well with a simple substrate thermal sink. The thermal impedance of the oxide layer becomes increasingly detrimental to the laser performance because it blocks the laser from draining heat through the substrate. As the simulation in Fig. 3.16 shows, the heat tends to escape out the top contact to the air.

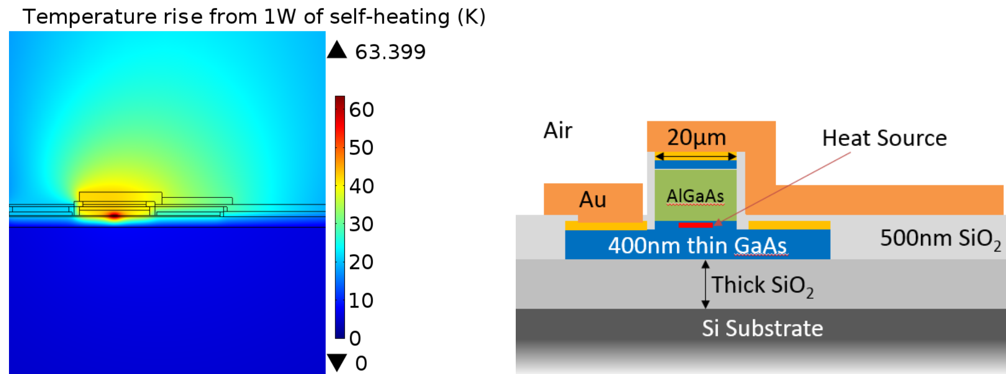


Figure 3.16: 5 μm wide Au shunts positioned directly under the sides of a 20 μm mesa result in a thermal impedance of 63.4 K/W.

To mitigate this in prior heterogeneous integrated lasers thermal shunts have been proposed [94]. These have shown some improvements in very small devices like micro-ring lasers but don't show nearly as significant improvements in longer in-plane lasers for buried oxide layers of 1 μm. This all changes though as you increase the lower cladding oxide thickness beyond 1 μm

The thermal impedance in Fig. 3.21 shows a slight sub-linear power relationship of thermal impedance with increase in lower cladding thickness. The significance of the thermal shunt becomes very clear for thick lower claddings.

3.5.3 Thermal shunts

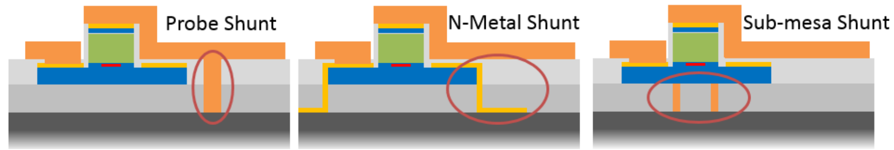


Figure 3.17: Different thermal shunt designs.

In order to simply use the metal already part of the unshunted laser process, thermal vias can be used as part of the vertical channel layer and then later covered with either probe metal or n-metal. These shunts would thus be added post bonding and are considered a lower risk change of the process.

A comparison of the probe and n-metal shunts is provided in Fig. 3.18 some improvement is seen in this example with a 3 μm thick lower cladding. The unshunted thermal impedance of 63.4 K/W shown in Fig. 3.16 is reduced with a probe shunt to 55.2 K/W. This was further improved by the use of n-metal shunts, however the improvement over probe shunting was only seen when the n-layer was reduced such that the n-metal shunt could be within 25 μm from the center of the 20 μm mesa.

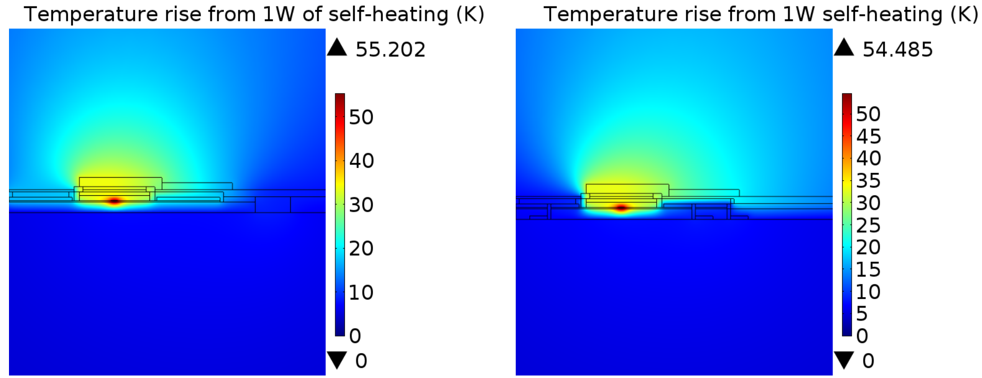


Figure 3.18: Comparison of probe and n-metal shunts. N-metal shunts 1.5 μm wide were added 25 μm from the center of the 20 μm mesa. A single 10 μm wide probe shunt is added to the 2 μm thick p-probe and shunted 40 μm from the mesa.

Alternatively, shunts can be added before bonding so that they may be aligned directly under the mesa as shown in Fig. 3.19. These can be added by electoplating following a deep etch of the thermal via so as to fill a significant portion of the via within limited time and without an unreasonable amount of metal compared to evaporation. These sub-mesa shunts can be designed to have the Au touching the III-V at the bonding interface as shown in Fig. 3.19, or a small buffer can be added by either etching back the metal from the polished interface or covering it with a thin layer of additional oxide that can then be CMPed and bonded. Figure 3.20 shows a comparison of the impact of these two surface preparations on the thermal impedance of the laser.

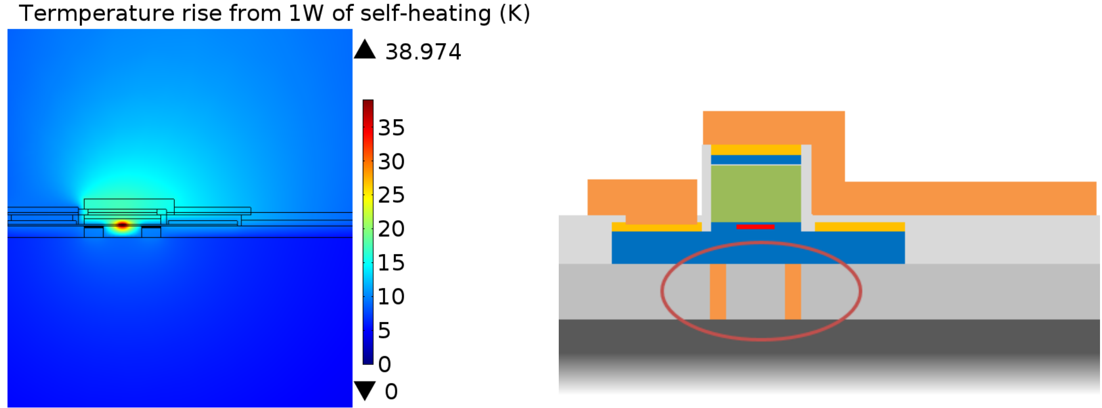


Figure 3.19: 5 μm wide Au shunts positioned directly under the sides of a 20 μm mesa result in a thermal impedance of 39 K/W.

As there is an improvement over an air void by using a thin oxide layer between the shunt and the III-V and it does not require a change to the actual bonding interface, a reasonable thickness of 200 nm was selected to compare sub-mesa shunts with unshunted devices. 200 nm can be achieved with CMP within a tolerance of a few 10s of nm across the wafer. Significant improvements are seen with this 200 nm buffer as the thickness of the lower cladding increases. A factor of nearly 2.5× improvement in thermal impedance, Z_t, over unshunted devices at 15 μm cladding as shown in Fig. 3.21.

In conclusion, thermal shunting is a viable method of reducing the thermal impedance of devices with thick SiO_2 cladding. It improves devices most significantly when used beneath the mesa, however such shunts must be offset from the actual guided mode so as to not add to the optical loss. However for short lasers,

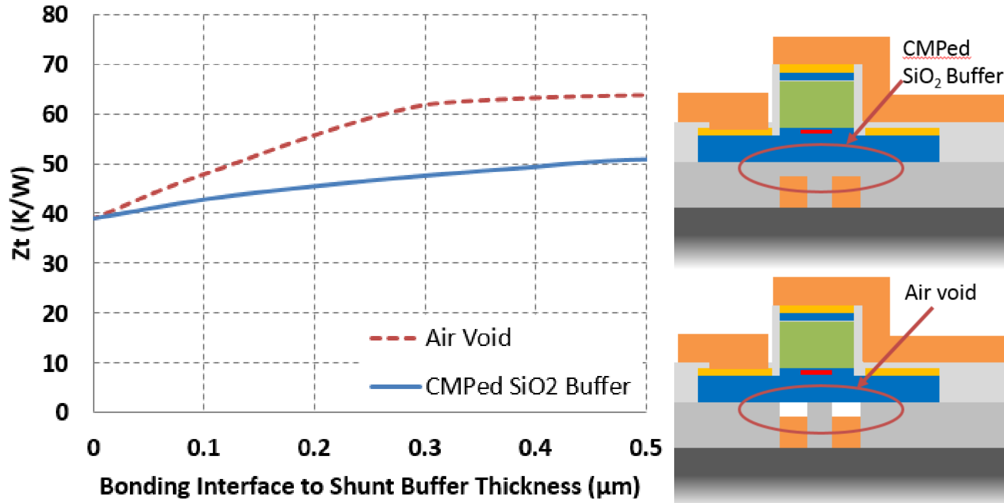


Figure 3.20: Two buffers between the shunt and the bonding interface are compared, an air void and CMPed SiO_2.

such as directly modulated distributed feedback lasers (DFBs) or micro-ring lasers, this may not be enough.

3.5.4 Flip-chip bonding

One well developed process that can also be designed to improve the thermal impedance of heterogeneous devices with thick lower cladding is flip-chip bonding. The process uses a high thermal conductivity electrical interposer layer, typically AlN with electrical leads to the device contacts. Au bumps, Au pillars, or other solder balls have been used for this purpose. If the problem is examine in the limit where the oxide thickness provides an infinite thermal barrier, the most logical place to take the heat off is the top.

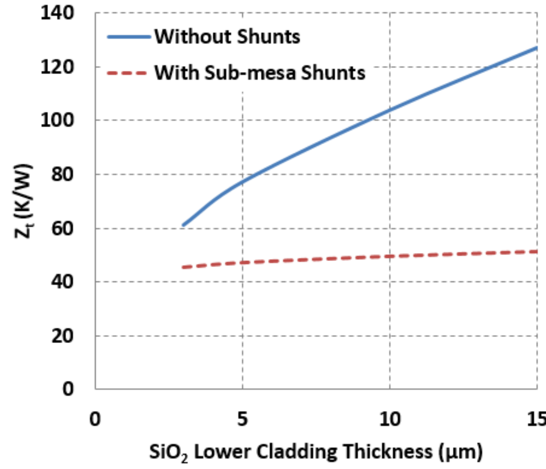


Figure 3.21: Comparison of thermal impedance Z_t v. SiO_2 lower cladding thickness for unshunted and shunted lasers. Two 5 μm wide Au shunts are placed on either side of the 20 μm mesa. There is a 200 nm buffer of SiO_2 between the shunt and the bonding interface.

Figure 3.22 shows how taking the heat up and out of the mesa can be a viable alternative to thermal shunting even for thick oxide layers. In this case the mesa upper cladding ($Al_{0.8}Ga_{0.2}As$) dominates the thermal impedance of the device. This ternary has significantly worse thermal conductivity than GaAs or AlAs as shown in Table 3.3. 80% AlGaAs sees a reduction from 44 $W/m \cdot K$ with GaAs to 16.3 $W/m \cdot K$. This is very poor only gets worse when using InGaP cladding or lower Al content material.

Restricting the design to geometric improvements wider and taller mesas can help. Wider mesas will have increased series resistance on the n-side, which is not appropriately captured in this thermal model. At the operating wavelength of

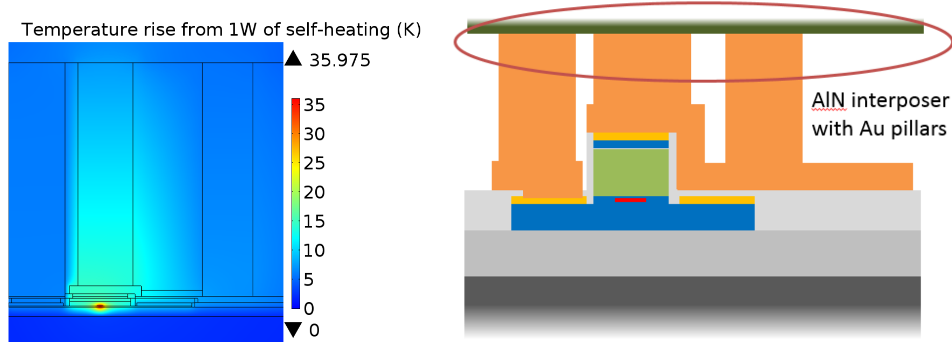


Figure 3.22: Thermal simulation showing the release of thermal energy primarily out of the mesa. Mesa is 20 μm wide with 1.520 μm tall mesa and made of $Al_{0.8}Ga_{0.2}As$.

the lasers discussed in this dissertation ∼1 μm the cladding thickness could safely be reduced to slightly less than ∼1 μm, but further reduction will increase the optical loss detrimentally. This shortened mesa reduces the thermal impedance from 36 K/W to 32 K/W. This represents the lower thermal impedance of the designs presented.

3.5.5 Summary of thermal design

Thermal impedance simulations were conducted on 1 mm lasers in 2-D to determine the best way to improve laser performance in heterogeneously integrated GaAs type lasers with thick SiO_2 lower cladding. Different types of thermal shunts were shown using Au as the high thermal conductivity shunt material. Of these, shunts placed under the laser mesa were found to be most effective but can not be

placed directly under the center of the mesa or optical loss would detrimentally impact laser performance. As an alternative to thermal shunting, flip-chip bonding was simulated and showed excellent results when wide and short mesas were used. Thermal impedance in these device approached half those with only bottom substrate thermal sinking through 3 μm SiO_2 lower cladding and were about a third those with 15 μm SiO_2 lower cladding. It is therefore suggested that future work on lasers with thick SiO_2 lower cladding include the use of flip-chip bonding as a viable back-end thermal solution.

3.6 Conclusions of III-V/Si_3N_4 laser integration

A new heterogeneous integration concept of directly bonded III-V epitaxial layers to SiO_2 clad Si_3N_4 waveguides is presented. Continuous-wave lasing was observed with output power of nearly 0.25 mW on InGaAs/GaAsP multiple quantum well epi bonded to 5 μm of SiO_2 and processed on Si as a proof of principle towards this concept. Si_3N_4 waveguides were coupled to n-layer III-V taper structures to quantify the expected loss of these tapers. 2.5$\pm$0.75dB coupling efficiency was measured. Sidewall DBR grating mirrors were also demonstrated in Si_3N_4 waveguides. Analysis showed good agreement with numerical simulations of these structures. Finally, heat transfer simulations were conducted to understand the

best ways to mitigate the high thermal impedance of thick lower SiO_2 cladding. Flip-chip bonding was determined to be the best solution when compared to using metal thermal shunts which can not be placed too close to the optical mode and require challenging modifications to the current working process.

Progress on many fronts towards achieving a new heterogeneous integration platform has been demonstrated, but there is still much more to do. Additional efforts should be focused in the domain of shorter tapers <20 μm. This was an empirical observation which was not in good agreement with simulations of theses structure and is perhaps one of the more valuable contributions of this experimental exploration. A process compatible with both tapered and straight III-V mesa needs further development. The demonstrated AlGaAs oxidation process used in this chapter was deemed not feasible as the oxidation close the tapers from passing current and closed the guided index channel provided by the oxidized aperture. Further details of these process pitfalls are provided in Chapter 4. The most clear take aways from this chapter are, 1) a path toward visible and NIR lasers integrated with Si_3N_4 waveguide is given, 2) a simple and accurate method of predicting sidewall grating performance is shown, and 3) a clear direction to focus development for lower thermal impedance. Further detailed suggestions will be covered in the Section 5.2, Future Work.

Chapter 4

Fabrication of Heterogeneous $GaAs/Si_3N_4$ Lasers

4.1 Heterogeneous laser process

A simplified heterogeneous laser process flow is shown in Fig. 4.1. This is referred to throughout this chapter in more detail. This section is simply to provide the context for the process development presented.

Figure 4.1(a) shows the thermal oxidation of a bulk silicon wafer. One could envision using a pure glass substrate in place of this oxidation, however the optical quality of thermal oxide has been shown to be at least as sufficient as a pure SiO_2 substrate and Si has superior thermal properties to act as a substrate thermal sink. Starting with a silicon substrate also gives the process more access to fabrication facilities and is lower cost.

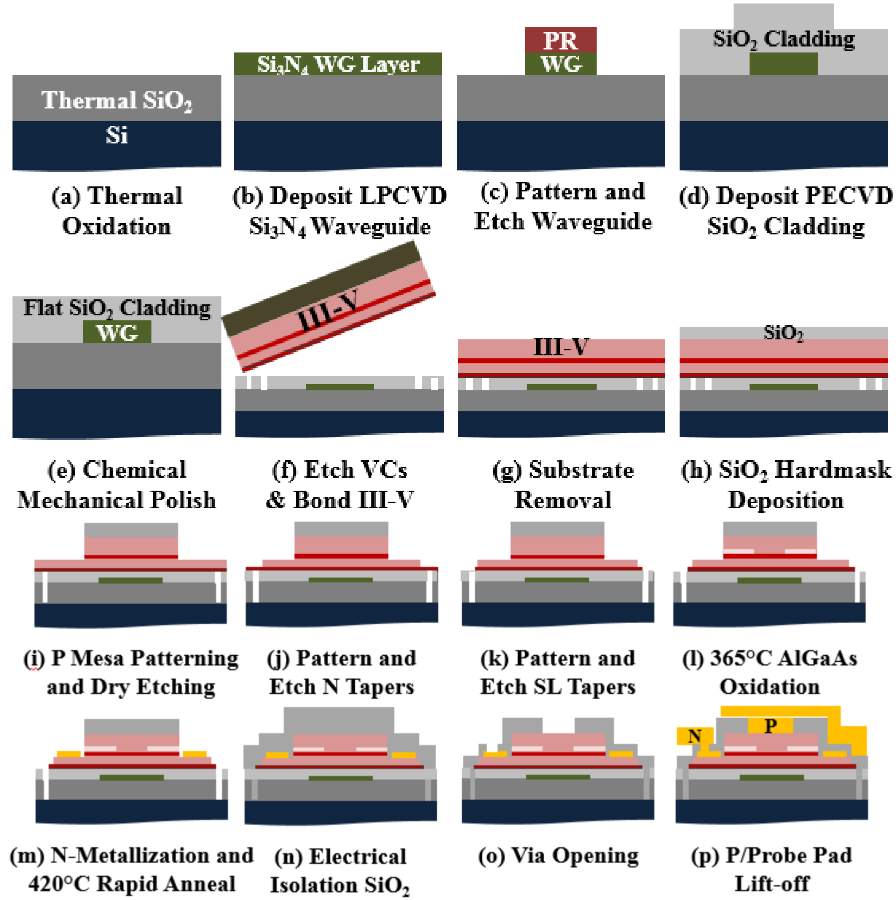


Figure 4.1: Process flow for Fabry-Pérot lasers and tapered mode converters.

Figure 4.1(b) is the Si_3N_4 core deposition. For this process we selected stoichiometric Si_3N_4 deposited via low pressure chemical vapor deposition (LPCVD), which is tube furnace batch process that we must order from outside UCSB. This was found in a through literature survey of low loss waveguides to be the preferred choice [95]. The lowest loss waveguides from this review also use thermally oxi-

dized SiO_2, further supporting this decision. This waveguide layer was annealed at 1050°C for 7 hours to drive out any residual hydrogen.

In order to lithographically form first order DBR gratings and lower sidewall roughness than contact lithography, the ASML PAS 5500/300 deep ultra-violet (DUV) stepper photo-lithography tool was selected with a positive process in (c). The waveguide was etched using a $CHF_3/CF_4/O_2$ inductively coupled plasma (ICP) dry-etch of the core.

Figure 4.1(d) partial upper cladding deposition was performed using PECVD at 250°C followed by an anneal at 1050°C for 7 hours to drive out any residual hydrogen. Following this a chemical mechanical polishing (CMP) process planarizes and smooths the surface in (e). The SiO_2 surface is then etched to form vertical channels (VCs) pre-bond and bonded to the III-V layer with a thin SiO_2 layer by a 300°C plasma assisted bond in (f).

Substrate removal of the GaAs is conducted by a spray etch from [96] diagrammed in (g). A PECVD SiO_2 hardmask deposited in (h) is used for the mesa etch in (i). $Cl_2/N_2/(H_2)$ ICP etching with a laser monitor defines the mesa and is used to reopen the vertical channels (VCs) in (j). This step may also be performed by etching n-tapers and the bonding superlattice (SL) layers into tapers.

Once the VCs have been opened they will not explode from the pressure increase on the thin III-V during the 365°C AlGaAs oxidation used to form the

current aperture in (k). The n-metalization (AuGe/Ni/Au) and rapid thermal anneal (420°C) to alloy this contact, (l), were placed after the oxidation to avoid any impact of the water vapor and high temperature on the metal.

The process is concluded by simply depositing a SiO_2 electrical isolation, (m), and opening vias, (n), in it to make contact with the both sides of the diode with a thick p/probe metalization in (o).

The following sections highlight some of the sticking points in this process flow, and the learning that was achieved in working towards heterogeneous integration of GaAs type lasers directly on top of a Si_3N_4 PLC.

4.2 Bonding

> "The friction of surfaces decreases with decreasing surface roughness up to a point where the surfaces are so well polished that they stick together with dramatically increased friction." -Desauliers 1734

4.2.1 Background and context

Direct bonding is a very old technology that seems only recently to have been rediscovered by the photonics industry as a viable means for heterogeneous integration. Bonding of III-V semiconductors to silicon have been previously demonstrated by UCSB using low temperature plasma assisted bonding [87]. Additional considerable efforts have been made in by UGhent/IMEC, Einhowen, Intel Cor-

poration, CEA-DRT/LETI, Hewlett Packard, and others [97], [98]. There have also been efforts by A*STAR and Northwestern University to directly bond InP to Si_3N_4 using a low temperature process similar to the UCSB plasma assisted bonding process [99]. To date the main focus of these efforts has been on InP based materials.

This work focuses on GaAs based materials and integration with waveguides clad by SiO_2. I will summarize the methods used and why they apply to applications in heterogeneous integration of GaAs type lasers to SiO_2 clad waveguides. Then I will give an overview of the key experimental results I have made in applying the technique to GaAs type laser epitaxy bonding.

Table 4.1: Coefficients of thermal expansion (CTE) of substrate materials

Material	linear CTE ($\times 10^{-6}$/K) [Ref.]
SiO_2	.55 [61]
Si	2.618 [59]
InP	4.6 [100]
GaAs	6.4 [100]
GaP	5.9 [100]
InAs	5.2 [100]

The great majority of bonding processes either require an anneal post contact or see a greatly increased bonding strength post-anneal. For this reason, it is ideal to match the coefficients of thermal expansion (CTE) of the two substrates so that the anneal does not put unnecessary thermal stress on the bonding interface as the

bonded sample is cycled in temperature. However, the very aspect which makes heterogeneous integration appealing is the marriage of different materials. So you can't have both a matched CTE and two material systems integrated together. Table 4.1 shows the linear CTE of some common substrates for PLCs and III-V photonics. From this table two things are clear. If we would like to integrate a SiO_2 clad waveguide with a GaAs type laser, it is preferred that the SiO_2 be grown first on Si to get the higher CTE, and that there will be more than a factor of 2 difference in thermal expansion between the two substrate. Comparing this with the InP/Si mismatch we see an increase of nearly 40%.

This difference has not been shown to be prohibitive as demonstrations of bonded GaAs to Si using spin-on-glass, an intermediate layer cured by a 200°C anneal, have been made by Alexe et al. [101] and Dragoi et al. [102]. Similar results have even been reported with fabricated lasers on SOG on Si [38]. These showed similar bonded and unbonded laser threshold current and slope efficiencies. Direct bonding to SiO_2 on Si was also demonstrated followed by a SmartCut style He implantation and GaAs substrate removal [103]. Most recently GaAs bonding directly to Si has even been shown to form an ohmic electrical junction [104].

Emboldened by these past successes we designed a first epitaxial layer stack to test our bond and substrate removal process steps.

4.2.2 Design decisions

Laser material with InGaAs quantum wells was grown using MOCVD. Aspects of this design which are important to bonding are the selection of a substrate removal etch stop layer, superlattice (SL), and bonding interface material. The SL blocks dislocations generated near the bonding interface from propagating to the quantum wells. The thermal expansion and lattice mismatch of the bonded epitaxy and host substrate are the source of these dislocations. The bonding interface material is important to the chemical bond formed. However, perhaps more important than what material, is it's roughness.

MOCVD growth was selected for its affordability and quality. Commercial growth of InGaAs quantum wells is well established and the defect density, particularly large defects which impact bonding, was found to be low enough so as to achieve sufficient yield for demonstration of hundreds of devices per bond. In designing the layers for these structures, the etch stop layer was a critical decision. Multiple layers where used successfully including $Al_{0.8}Ga_{0.2}As$ (thickness = 500 *nm*) and lattice matched InGaP (with thicknesses ranging from 200-10 *nm*). In both instances a spray etch [96] of NH_4OH:H_2O_2 (1:30) was used with selectivities reported greater than 1,000:1 for GaAs from the etch stop layer. Etch rates of the substrate ranged from 1-3 μm/min. Given that the InGaP etch stop in some cases was 10 *nm*, and that it often took many minutes to remove the most stubborn

and non-uniform remnants of GaAs from the etch stop layer, there was nothing to suggest that for InGaP the selectivity was not nearly infinite.

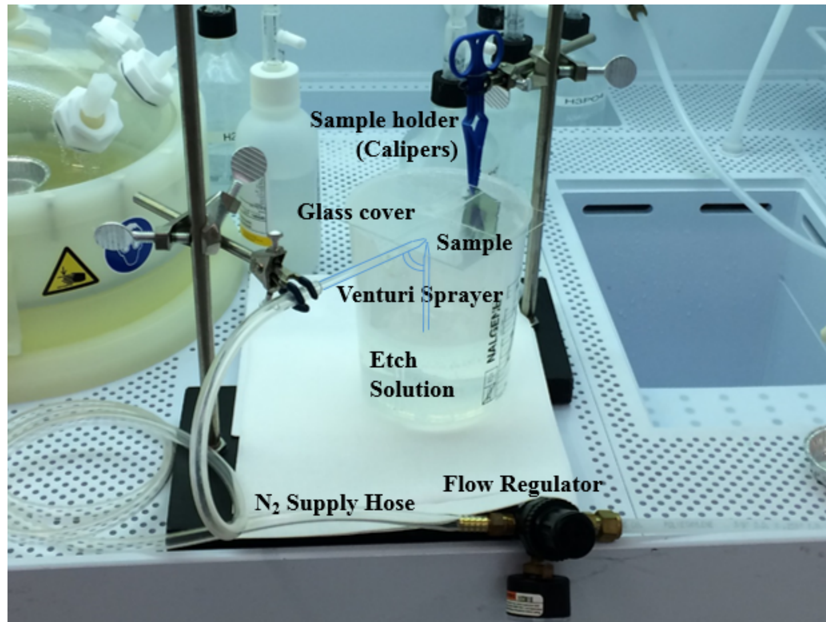


Figure 4.2: Photograph of spray etch setup as adapted from the setup in [96].

The bonding superlattice (SL) was an important element in the epitaxial design. Firstly, a strained SL has been proven to improve performance in photodetectors (PDs) by reducing dark current attributable to bonding induced defects [105]. Secondly, the surface roughness of our samples was found to be related to the selection of SL. Strained SLs made by an alternate stack of 7.5 nm InGaP ($\pm 1\%$ strain) were grown. The surface roughness of these highly strained designs was measured to be 2.8 nm by atomic force microscopy (AFM). To determine the source of the roughness, the SL was removed by selective wet etching and remea-

sured. The n-GaAs contact layer beneath the SL was found to have roughness less than 1 *nm*. This proves that the origin of the roughness was the strained InGaP material. Figure 4.3(a) show the AFM scan of this sample before bonding.

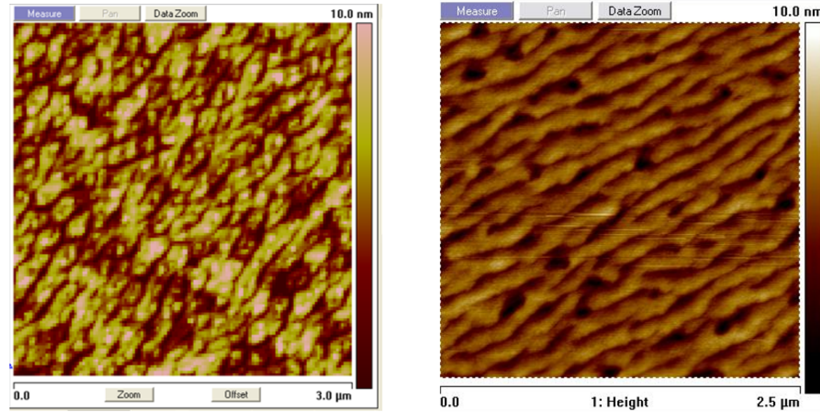


Figure 4.3: AFM scans of SL surface before bonding; (a) initial growth with InGaP SL (2.8 *nm* RMS) resulted in unsuccessful bonding; (b) second growth substituting the InGaP SL with InGaAs/GaAsP (1.1 *nm* RMS) resulted in successful bonding.

The roughness of the strained InGaP is attributable to a bifurcation of the InP and GaP binaries that is often observed in MOCVD growth of InGaP. In contrast to the ±1% InGaP SL, a strained ±0.5% SL of InGaAs/GsAsP was selected for the next epitaxial layer design. This was also two repeats of 7.5 *nm* layer pairs. A reduced surface roughness on the order of 1 *nm*, or comparable to the surface roughness of the layer grown directly before the SL, was measured and is shown in Fig. 4.3(b).

InGaAs/GaAsP growth was done on 10° offcut [100] GaAs wafer, which was also shown to have a slight improvement on roughness when compared to samples with 2° and no offcut from the same vendor. Both the higher strain and material choice were critical to decreasing surface roughness, therefore a ±0.5% strained InGaAs/GsAsP SL is suggested for future development as it resulted not only in lower surface roughness, but superior bonding yield.

Bonding yield after substrate removal went from on the order of 10-20 percent with ±1% strained InGaP SL to more than 90 percent with clean ±0.5% strained SLs of InGaAs/GsAsP. In all cases, the selection of pieces of epi had low bond yield. The rounded edge of the wafer failed to bond due to a combination of increased surface roughness as measured by AFM higher defect density and the unlevelness to the rest of the wafer. Wafer levelness is critical to uniform contact. Even under a pressure of 3 MPa, a large area of unbonded material occurs repeatably at the very edge of die which still has a rounded edge from the original wafer they were diced out of.

The actual selection of the bonding interface and its preparation are very important. We tried epitaxial samples with GaAs directly bonded to thermal and PECVD SiO_2 and GaAs with PECVD SiO_2 directly bonded to thermal and PECVD SiO_2. All bonding was done using the same plasma assisted bonding technique outlined in [87]. GaAs directly bonded to both thermal SiO_2 and PECVD

SiO_2 often failed even to achieve a spontaneous bond, sliding off the bonding surface post anneal. Results of the GaAs/SiO_2-SiO_2/Si were far superior and comparable to those found on GaAs/SiO_2-Si. These oxide-to-oxide bonds agreed with prior published results in [106] suggesting that no significant contribution due to thermal expansion mismatch exists for GaAs-Si compared to InP-Si low temperature plasma assisted bonding. Therefore, oxide-to-oxide bonding was the preferred choice.

PECVD SiO_2 on the Si side is one method for heterogeneous integration with Si_3N_4 strip waveguides, as is the case with partial upper claddings of waveguides fabricated on Si.

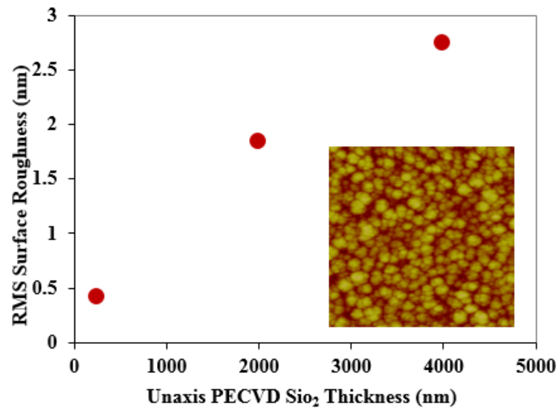


Figure 4.4: Roughness from AFM scans of Si with different thicknesses of SiO_2 deposited with the Unaxis PECVD 100°C UCSB standard recipe. Inset shows typical topology of SiO_2 on Si.

As seen on Fig. 4.4, surfaces prepared with thick PECVD SiO_2 were found to have roughness in excess of 1 nm, a reasonable target for surface roughness with high-quality bonding. Additional deposition enlarges existing grains of SiO_2 increasing roughness, rather than filling in-between existing grains and maintaining or decreasing roughness. The rate at which the roughness increased depends on the PECVD system used. This is not an issue for the film deposited on the III-V epitaxy which is 50 nm or less, so long as the initial roughness of the epitaxy was small. In the instance of the $\pm1\%$ strained InGaP SL where the roughness exceeded 1 nm additional PECVD SiO_2 only increased the problem.

However, an entire 75mm wafer of $\pm1\%$ strained InGaP SL epitaxy was deposited with 200 nm of PECVD SiO_2 and then chemical mechanical polished (CMPed) to 0.5 nm RMS roughness. This method was able to reclaim some of this material previously thought to be worthless because of high roughness.

To achieve planarization via a CMP process, Fig. 4.5(e), the density of features on the mask is critical. There are two basic approaches to device layout for the waveguide layer, dense layout and sparse layout. A common approach for dense layout is to increase the density of open areas with dummy patterns as proposed in [107]. This works well for electronics where the interaction distance between devices is small, but for photonics, particularly for PLCs with large optical modes that interact even with many μm of separation, such as the ultra-low loss Si_3N_4

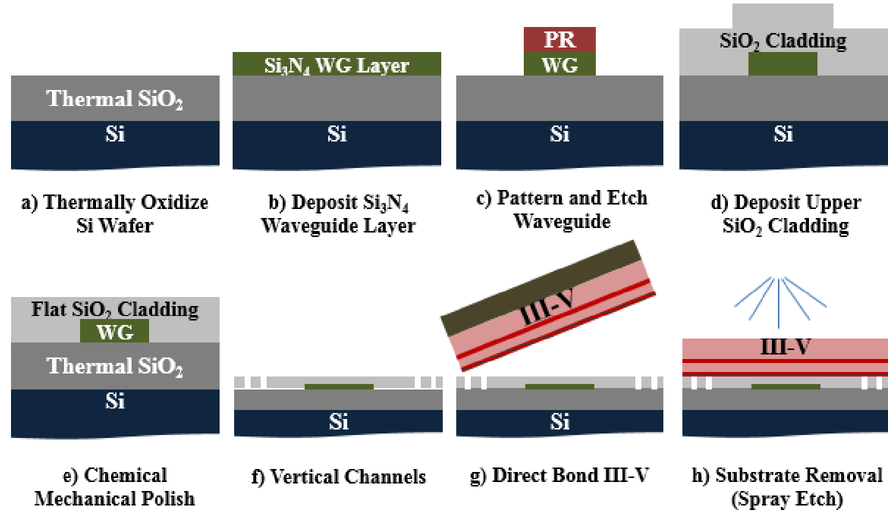


Figure 4.5: Simplified process flow diagram from bulk Si oxidation through bonding and substrate removal.

platform [86], this is not an option. For the buried channel Si_3N_4 waveguides used in Chapter 3, we selected a sparse approach and reduced the size and proximity of features as much as possible. The planarity of the sample was compromised by the height of the waveguide (nominally 200 nm in reports from this work). Therefore the SiO_2 partial upper cladding was CMPed to produce both a planer and smooth surface for bonding. This process requires the use of two polishing pads on the Logitech Orbis CMP tool. The first pad (IC1000) is a self-adhesive hard polyurethane impregnated polyester felt pad with concentric trenches patterned into it mounted to the tool's iron platen. This pad provides efficient planarity of SiO_2 without removing an excessive amount of material. From empirical observations, a factor of 3-4 times more SiO_2 than the waveguide etch step should

be deposited as partial upper cladding to planarize features as diverse as 500 nm narrow waveguides and 20 μm profilometer test mesas. As the majority of the waveguide layer was etched, problem areas of planarization were limited to areas of dense features, such as spiral 800 nm waveguides with more than ten guides spaced 4 μm between adjacent guides, and wide features such as alignment marks and the 20x60 μm rectangular profilometer mesas spaced by 20 μm. Once the planarization polish is completed and the slurry is thoroughly rinsed from the sample, a profilometer scan across a dense features is done to determine if the planarization is complete. Empirically, we settled on 15 nm as the step height that must be achieved before the second polishing step could be initiated.

The surface roughness following the planarization polish typically was measured in AFM to be >2 nm RMS. A second soft black pad was used to reduce this. The soft black OCON-357 Chemcloth polishing cloth is also self-adhesive to a large iron platen and was measured to smooth SiO_2 from up to 5 nm RMS to less than 0.4 nm RMS as measured in the AFM. It also planarizes but has worse uniformity and consumes more material than the IC1000 pad.

Finally, following the CMP surface preparation, vertical channels (VCs) are etched into the oxide surface, Fig. 4.5(f). These channels were and empirical discovery at UCSB by John Bowers' group. Dubravko Babic made initial observations of the impact of long waveguide channels on bonding quality of InP. Later

Di Liang showed smaller "vertical channels" to improve bonding performance of plasma-assisted InP to Si bonding [87]. In this work GaAs/SiO_2-SiO_2/Si bonds also improved with the addition of vertical channels into the SiO_2 surface implying that the void is more fundamental than any outgassing into SiO_2.

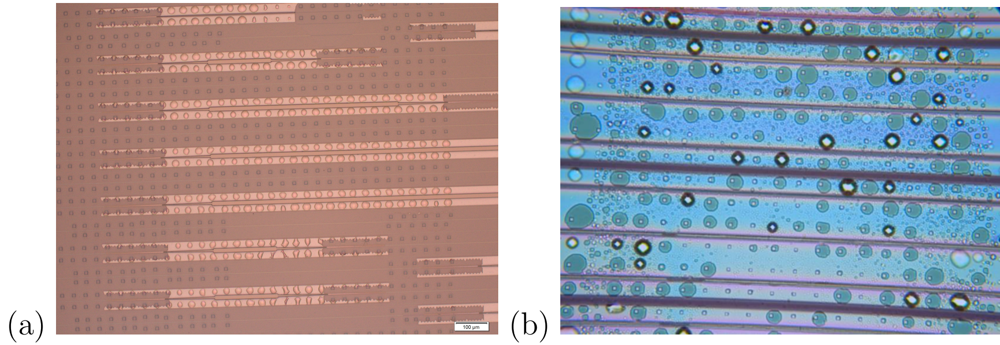


Figure 4.6: (a)Microscope image of the original placement of VCs under thin n-contact material. (b) Microscope image following a high-temperature process with a full thin n-layer. Most VCs burst and redeposited material onto the sample.

One observation in working with VCs was that there is a risk placing them underneath III-V regions that are less than a few hundred *nm* thick. The thin III-V layer will be fragile suspended membranes. It was observed in processing AlGaAs type material that significant bubbles would form as shown in 4.6(a) under the III-V containing the n-contact layer. If these bubbles are subsequently placed into a high-temperature process such as the AlGaAs oxidation furnace, they will likely burst and redeposit on the sample in another location. Therefore, though subsequent processes used VCs, their size was reduced and density increased to

provide a similar volume of void and proximity, without placing them directly underneath the devices. Furthermore, processes order was adjusted to place the higher temperature processing after the devices were reduced to small islands of material on SiO_2 as shown in Fig. 4.7.

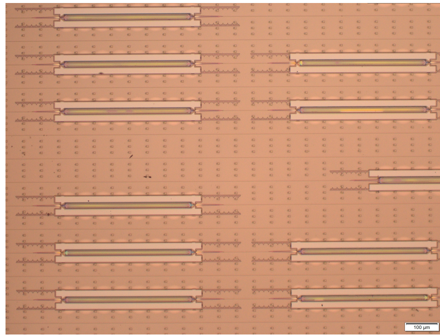


Figure 4.7: Selective placement of vertical channels was made to prevent them from expanding into bubbles and possibly exploding during high-temperature oxidation or contact anneal processes.

4.2.3 Bonding results and conclusions

Bonding tests were conducted on GaAs(epi)/SiO_2-SiO_2/Si and GaAs(epi)-SiO_2/Si using the process described in 4.2. Both bonds worked after substrate removal with high yield and limited bonding failure either attributable to localized growth defects, particles or edge effects from the edge of the epitaxial wafer. However, perhaps the best test of all, continued device processing revealed that the GaAs(epi)/SiO_2-SiO_2/Si had substantially less flaking and epitaxial redepo-

sition than GaAs(epi)-SiO_2/Si. This is a small statistics observation, however given that the SiO_2 can be also used to smooth rough epitaxial surfaces, direct GaAs(epi)/SiO_2-SiO_2/Si bonding was selected as the process of choice.

4.3 AlGaAs mesa etch development

Very critical to the development of an in-plane laser is an etch of the semiconductor mesa. In the case of the heterogeneous lasers tapered mode converters are required, so a dry etch is necessary given the thickness of the top cladding. Dry etching using an inductively coupled plasma (ICP) system enables tailoring the etch to achieve smooth etched surface, vertical sidewalls, and uniform etching rate, both locally by avoiding "trenching", a sharp increase in etch rate at the side wall of an etched feature caused by charge build up on the walls of the etched surface and mask, and globally so as to maintain a consistent end point for future process. This end point detection was conducted using a laser monitor. Development was conducted on multiple ICP tools in the UCSB nanofab.

4.3.1 AlGaAs ICP etching in the Unaxis VLR system

As the standard in-house process had strong trenching and poor verticality, a process on the Unaxis ICP etch tool was developed first. Extensive develop-

ment was done on a $Cl_2/N_2/H_2$ etch which resulted in 150 nm/min, vertical etch without trenching as shown in 4.8(a). The hydrogen was added to passivate the charging that caused the trenching.

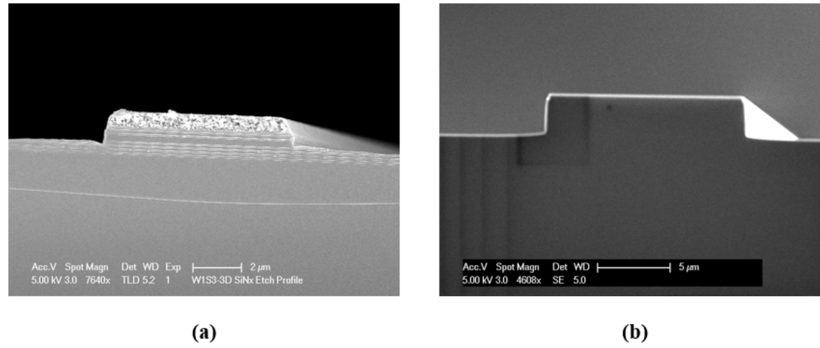


Figure 4.8: SEM cross sections of Unaxis ICP AlGaAs etches. (a) Initial house Cl_2/N_2 recipe. (b) Developed $Cl_2/N_2/H_2$ recipe.

Additional parameters were optimized to improve selectivity of the PECVD SiO_2 hardmask. The final selectivity was 50:1.

This process worked very well for the first batch of InGaAs/GaAs quantum well FP lasers discussed in 3.2.1. Unfortunately, over the course of this work issues with this etch chamber required it to undergo repair to remove the Al heating element that maintained a constant temperature on the top electrode. The replacement was a mechanical dummy piece which left the tool no longer able to regulate the temperature of the top electrode. The unfortunate result from this was that the etch development was lost as the $Cl_2/N_2/H_2$ process grassed profusely with the new lower steady state top electrode temperature. Attempts were made to

resolve this with a long oxygen clean pre-process which raised the temperature of the top electrode back up closer to the original 80 °C removed the grass, but lost both the selectivity and verticality of the etch. After extensive recalibration, the grassing was eliminated, however the selectivity never recovered, and the tool was abandoned for this process.

4.3.2 AlGaAs ICP etching in the Panasonic ICP system

In early 2014, a laser monitor was added to the Panasonic E626I (ICP#1) etching tool. This enabled endpoint detection that is a requirement for good etch control. The existing etch for this tool is Cl_2/N_2, only subtle adjustments were made to this process to bring the selectivities and verticality into spec. The final process is Cl_2/N_2 (20/10sccm) P_{ICP}=500W, P_{CCP}=35W, 0.25Pa.

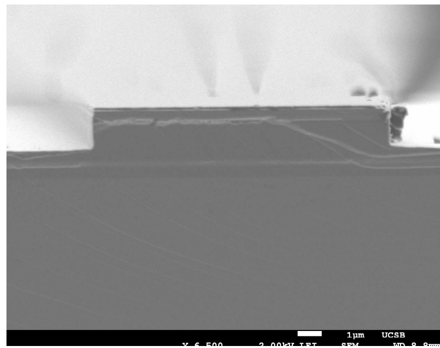


Figure 4.9: SEM images of Panasonic E626I ICP AlGaAs etches in cross section.

The ICP#1 Cl_2/N_2 etch was also selective to InGaP lattice matched to GaAs by a ratio of ~7:1 which makes InGaP a convenient etch stop indicator as well as selectively removable from GaAs with HCl based wet etches.

4.3.3 AlGaAs mesa etching results and conclusion

Small variations in the dry etch rate across both a single die and multiple bonded die on a wafer required that a well controlled highly selective wet etch be used. H_3PO_4:H_2O_2:H_2O (3:1:50) was used for this purpose. With an etch rate of ~100 nm/min for GaAs and similar though not well quantified rates for InGaAs, GaAsP, and AlGaAs. This etch was found not to detrimentally undercut critically sharp tapers with tips <200 nm.

In conclusion, a process of dry followed by wet etching was developed which provides a uniform etched surface with vertical sidewalls for critical features such as tapers without significantly distorting the intended pattern by undercutting or flaring out the base of the mesa on critical features. Additionally, only a slight 10 nm/min etch rate of SiO_2 was observed during dry etching that is manageable for unprotected waveguides in unbonded areas if there is a few hundred nm of SiO_2 partial upper cladding above the core.

4.4 Oxidation of bonded AlGaAs epi

During the development of this process, numerous patent applications have been filed for VCSELs heterogeneously bonded to silicon [108–111]. These often overlook the fact that a high temperature AlGaAs oxidation process is fundamental to successful AlGaAs VCSEL current apertures and is typically done at temperatures in excess of 400 °C. In this work we have developed a process for oxidation at 365 °C without observing mechanical damage to the bonding interface so long as VCs containing pockets of gas are uncovered before this process as discussed in 4.6.

4.4.1 Oxidation results of bonded AlGaAs

AlGaAs oxidation apertures are used both for current guiding and index guiding in heterogeneously bonded InGaAs multiple quantum well lasers. This also enables the guided mode of the laser to be offset from high surface recombination of the etched p-mesa sidewall while maintaining a wide mesa for improved thermal dissipation compared to a narrow p-mesa structure as the mesa is the ideal place to dissipate heat in a packaged device, detailed further in Section 3.5.4. The aperture is formed by hydrolysis, or thermal wet oxidation, of high Al content $Al_{0.98}Ga_{0.02}As$ to form a layer of Al_2O_3.

Al_2O_3 both has a substantially lower refractive index than AlGaAs, 1.6 [112], and is a sufficiently wide bandgap to act as a current block in the p side of the AlGaAs cladding. This style of thin current and optical aperture is well known in vertical cavity lasers but is less used for in-plane devices though the first observations of the effect reported by Dallesasse and Holonyak [113] were of in-plane devices. The reason for this is that exposed facets of $Al_{0.98}Ga_{0.02}As$ are not stable over time. However, the objective of this design, similar to the Silicon Hybrid Laser is to have no exposed facets to avoid this issue.

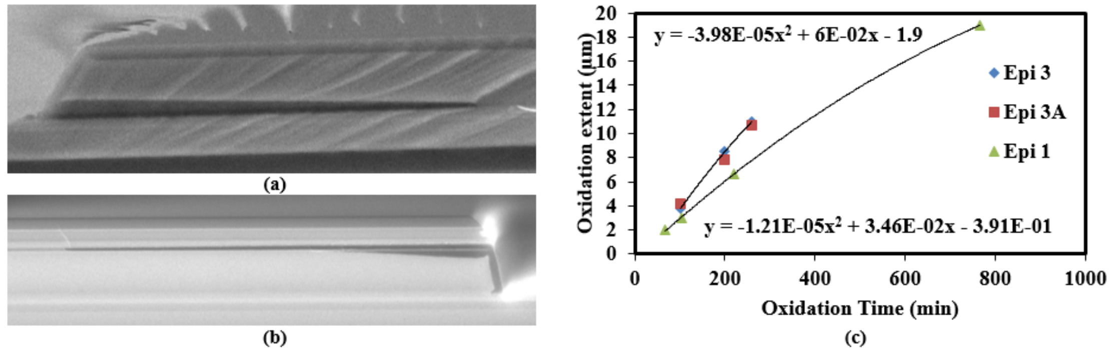


Figure 4.10: (a) SEM image of bonded (cladding on top) mesa oxidation profile from Epi 1. (b) SEM image of unbonded (cladding on bottom) test mesa oxidation profile from Epi 3. (c) Measured AlGaAs oxidation extents over a range of times for 3 epi with two different aperture layer designs.

Oxidation was performed at the relatively low temperature of 365 °C by loading onto a quartz boat freshly removed from a three zone 50mm Lindberg tube furnace fed with 10 sccm of nitrogen. The samples are measured on unbonded freshly Cl_2/N_2 dry etched pieces rinsed in water, stripped in 1165(80 °C), and rinsed

again in isopropanol. Data is plotted over a range of times initiated after the boat is slowly placed into the center of the furnace over the course of 1 minute and the nitrogen carrier gas is diverted through a bubbler system in an 80 °C deionized water beaker. This forces steam into the tube. The steam activates the process so the end time is declared when diverting the flow of nitrogen back to bypass the bubbler and flow freely into the tube. The sample is then unloaded over the course of 1 minute and let cool in ambient. Results are shown in Fig. 4.10. Any differences between the oxidation rate of unbonded calibration samples and the bonded actual samples fell within the noise of the data collected.

Table 4.2: Epitaxial layer designs for oxidation apertures

Layer	Material	Epi 3 & 3A Thickness (nm)	Epi 1 Thickness (nm)
Cladding	$Al_{0.8}Ga_{0.2}As$	1000	1000
Graded transition	$Al_{0.1}Ga_{0.9}As$ ⇓ $Al_{0.9}Ga_{0.1}As$	50	NA
Oxidation buffer	$Al_{0.9}Ga_{0.1}As$	10	NA
Oxidation layer	$Al_{0.98}Ga_{0.02}As$	50	50
Oxidation buffer	$Al_{0.9}Ga_{0.1}As$	10	NA
Graded transition	$Al_{0.8}Ga_{0.1}As$ ⇓ $Al_{0.3}Ga_{0.7}As$	80	80

The process appears to be diffusion limited rather than reaction limited judging from the quadratic relationship of extent with temperature most clearly visible

in the Epi 1 data in Fig 4.10(c) [114]. A more rapid oxidation in Epi 3 and 3A is due to a modification in design detailed in Table 4.2. The intent of the design change in Epi 3 and Epi 3A is to provide a thicker more well defined aperture with a square cross section. This was achieved and can be seen by comparing Epi 1 Fig. 4.10(a) to Epi 3 Fig. 4.10(b). There is a triangular profile of Al_2O_3 in Epi 1 which is due to the oxidation of the 80% Al cladding layer along with the 98% Al front. This occurs in Epi 3 however the triangular profile forms more slowly and is, therefore, offset from the oxidation front forming the aperture because of the addition of the graded transition between the cladding and oxidation layer detailed in Table 4.2.

The oxidation front can also be viewed in Nomarski mode of a microscope, as in Fig. 4.11. This is visible though the cladding remains opaque due to an increase in volume of Al_2O_3 replacing $Al_{0.98}Ga_{0.02}As$. This pushes the surface to form a subtle step. Measurements done in the microscope were confirmed to agree with measurements done by SEM.

4.4.2 Selective area AlGaAs oxidation

The oxidation studies presented in the literature have typical of developed for VCSELs and perhaps only unique in that the oxidation was applied to bonded epitaxy on SiO_2 on Si. However, in order to use oxidation with a linear in-plane

device a requirement for a tapered mesa structure is the appropriate termination of the oxidation aperture. The issue is diagrammed in Fig. 4.11.

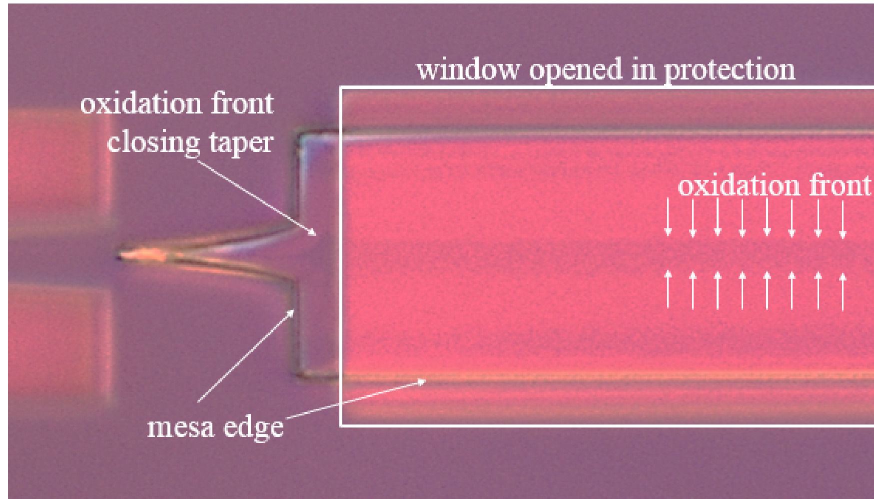


Figure 4.11: Example of selective area oxidation of a wide mesa device with unwanted oxidation observed in the tapered section which is covered with a protection dielectric.

As shown in Fig. 4.11 the taper can easily oxidize closed preventing electrical pumping of the quantum wells in the taper tip furthest away from any diffused carriers which enter the wells at the aperture. Some literature has been published showing that oxidation is inhibited by adding a diffusion blocking layer to limit the steam and other reactants from reaching the $Al_{0.98}Ga_{0.02}$ and form an oxidation front into the semiconductor [115]. This is commonly done to the top DBR stack of Al(Ga)As/GaAs DBRs by a complete encapsulation of the etched DBR. However, when part of the mesa is exposed as in Fig. 4.11, an interesting and vexing

phenomenon was observed. When part of the sealed mesa is opened to define the origin of the oxidation front, and part of the mesa remains sealed to prevent oxidation, as the front reaches a section that is protected an accelerated oxidation occurs along the edge that is protected. This causes devices to appear as if it is wholly unprotected as shown in the half protected mesa in Figure 4.12.

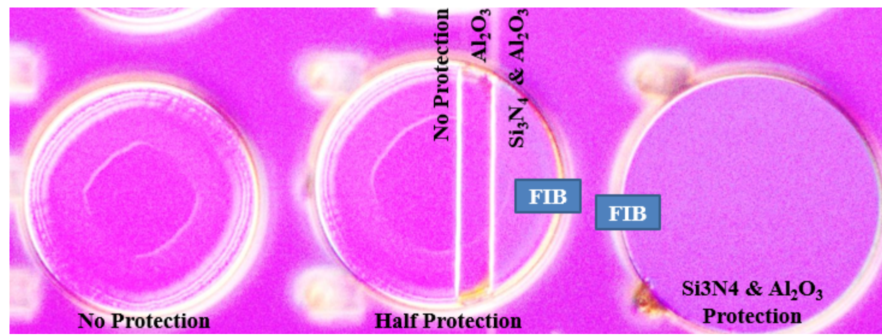
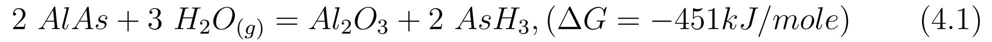


Figure 4.12: Nomarski mode image of round test structure mesas including one with no protection, one with half protection and one that is fully protected of 90 *nm* PECVD silicon nitride and 30 *nm* ALD Al_2O_3

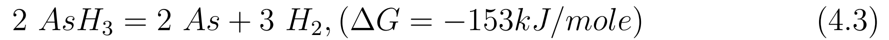
The source of oxidation in protected regions on a partially exposed mesa has been found to be a one of two things depending on the condition of the sample during oxidation. 1) Voids or edge effects which enable enhanced transport of gases along the edges. 2) Diffusion through the protection layer of byproduct and/or reactant gases such as hydrogen that interact with the oxidation front. A

number of molecules could be involved. Below is a list of the molecular analogs for the hydrolysis process and their respective Gibbs free energies, ΔG.

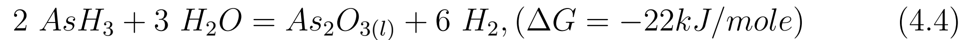


$$2\ AlAs + 3\ H_2O_{(g)} = Al_2O_3 + 2\ AsH_3, (\Delta G = -451kJ/mole) \tag{4.1}$$

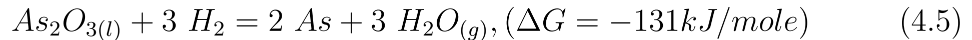
$$2\ AlAs + 4\ H_2O_{(g)} = AlO(OH) + 2\ AsH_3, (\Delta G = -404kJ/mole) \tag{4.2}$$



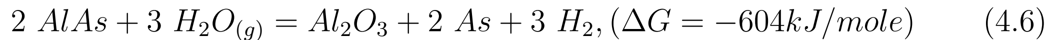
$$2\ AsH_3 = 2\ As + 3\ H_2, (\Delta G = -153kJ/mole) \tag{4.3}$$



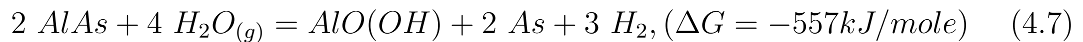
$$2\ AsH_3 + 3\ H_2O = As_2O_{3(l)} + 6\ H_2, (\Delta G = -22kJ/mole) \tag{4.4}$$



$$As_2O_{3(l)} + 3\ H_2 = 2\ As + 3\ H_2O_{(g)}, (\Delta G = -131kJ/mole) \tag{4.5}$$



$$2\ AlAs + 3\ H_2O_{(g)} = Al_2O_3 + 2\ As + 3\ H_2, (\Delta G = -604kJ/mole) \tag{4.6}$$



$$2\ AlAs + 4\ H_2O_{(g)} = AlO(OH) + 2\ As + 3\ H_2, (\Delta G = -557kJ/mole) \tag{4.7}$$

In the case of the half protected mesa in the middle of Fig. 4.12 a large void that ran along seemingly the entire mesa edge was found. This void is shown in

the focus ion beam (FIB) cross section in Fig. 4.13(a). FIB cross sections are courtesy of Daryl Spencer.

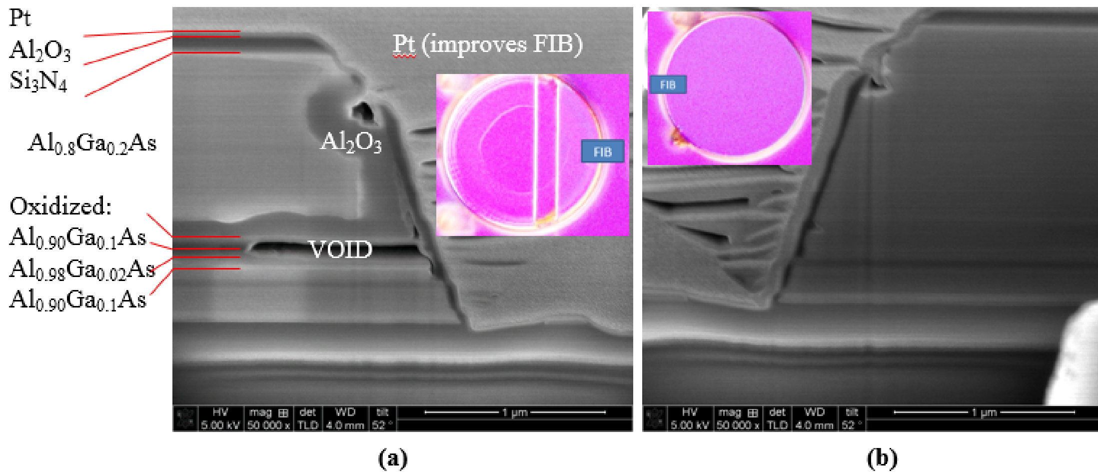


Figure 4.13: Comparison of FIB cross sections in adjacent mesas labeled in Fig. 4.12 and placed in the inset of each SEM image. (a) Shows oxidized area of protected feature of mesa and a 1 μm void at the oxidation layer. (b) Shows an entirely protected mesa with no signs of oxidation at all and no void.

The void is believed to have developed during wet processing of the oxidation window revealing the Al_2O_3 etchant which is AZ 300 MIF developer, containing 2.38% tetra-methyl ammonium hydroxide (TMAH) an etchant of Al containing materials.

The second reason for unwanted oxidation in protected regions is believed to be either the diffusion of gases through the protection layer which interact with the oxidation front to cause an accelerated oxidation process which is localized along the edge of the mesa, or simply an accelerated transport of reactants (to

and/or from the oxidation from) along the side-wall. To illustrate this Fig. 4.14 shows two simple geometries which have been partially protected with 30 *nm* ALD Al_2O_3 and 90 *nm* of PECVD Si_3N_4 with 30 *nm* ALD Al_2O_3 on top in the round structure and just 120 *nm* ALD Al_2O_3 in the rectangular mesa. In both cases with 120 *nm* of dielectric protection, there is are sections of protected mesa that show no oxidation however the extent to which oxidation occurs relative to the closest unprotected edge is greater than the extent perpendicular to the unprotected edge. This is clearest in Fig. 4.13(b) where the extent of oxidation along the side wall is five times that in towards the mesa center.

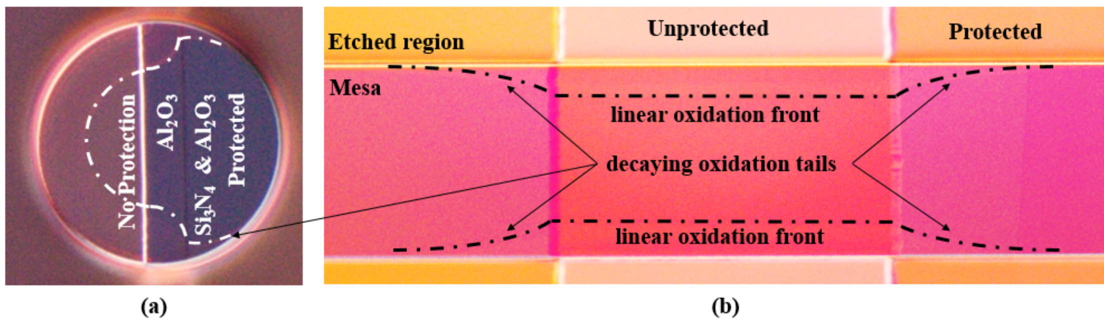


Figure 4.14: Exponential oxidation tails are observed in protected mesa sections

The use of different sized windows in the oxidation protection layer, as shown in Fig. 4.11, were not able to both prevent oxidation of the taper tip and make a clean transition from the linear current channel to a pumped taper, so an alternative was attempted. In Fig 4.15, fully protected mesas have deeply etched trenches added to them to provide an exposed sidewall for oxidation. The purpose of these

trenches is to reduce the time of the oxidation and thus capacity for accelerated oxidation on the edges to close the taper tips.

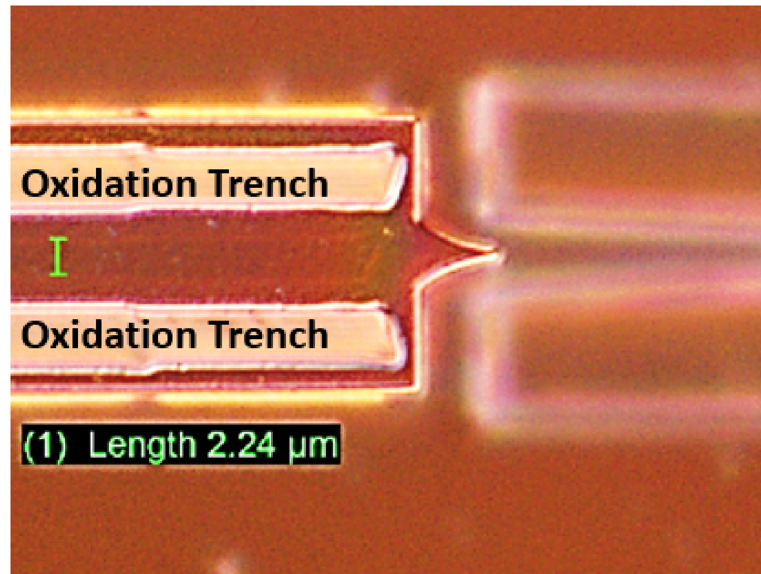


Figure 4.15: Oxidation trenches are shown not to prevent oxidation of taper tips.

Figure 4.15 not only shows the failure of these oxidation trenches to prevent the taper from closing but that the oxidation extent measured from any point on the taper is more than twice that measured from any point on the oxidation trench.

4.4.3 Conclusion of oxidation of bonded AlGaAs epi

It was reasoned that accelerated oxidation on mesa edge prevents both a clean linear current aperture down the center of the mesa and a smooth transition

from that mesa to a pumped taper. From the empirical observations over numerous attempts to achieve this goal by means of oxidation windows and oxidation trenches, it was concluded that alternative means of current and index guiding, such as shallowly etched III-V mesas, should be pursued.

4.5 Taper tip reduction

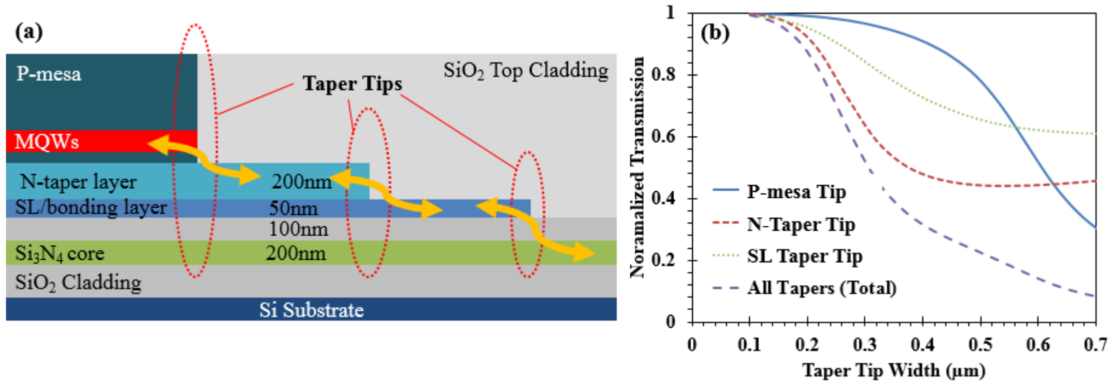


Figure 4.16: Analysis of transmission through tips in 3 layer taper from III-V to Si_3N_4. (a) Side view of each tip and the simulated layer thicknesses. Indices can be found in Table 3.2. (b) Transmission for each taper and the product of all of them plotted vs. the taper tip width.

Figure 4.16 provides a convincing argument for pursuing very fine tapers to overcome the large effective index mismatch between the Si_3N_4 passive waveguide and III-V components. Parameters that are not swept here which are worth noting are the selection of each of the layer thicknesses. A thin SL/bonding layer is very significant for the first transition. However, the thinner this becomes the thinner

the n-contact layer above it should be to prevent the second taper transition, the n-taper tip, from dominating the transmission loss. The contact layer thickness is also selected for low series resistance, so the sum of N and SL layers should be greater than $\sim>$200-300 *nm* assuming reasonable dopant levels for low optical loss. At these thicknesses, the final taper from the p-mesa to the n-layers is typically not the dominate transmission loss point as in Fig. 4.16(b).

The sub-200 *nm* taper tips suggested by this simulation study are much less than those we have used in prior Hybrid Silicon Lasers, so additional development efforts were required. The most promising of these are presented in this section. The first uses the GCA 6300 i-line Autostepper which is capable of 500 *nm* taper tips with sub-200 *nm* alignment accuracy on well leveled samples.

4.5.1 I-line bi-layer process

In order to reduce the feature size of tapered patterns using the GCA 6300 i-line Autostepper an adaptation was made from the bi-layer lift-off process which utilizes the difference in exposure and development properties of a PMGI (SF-11, or SF-15) underlayer with i-line photoresist (PR) (SPR955-0.9, etc.). Figure 4.17 shows the process flow by which a hardmask and epitaxial layer structure are patterned using this bi-layer pattern reduction.

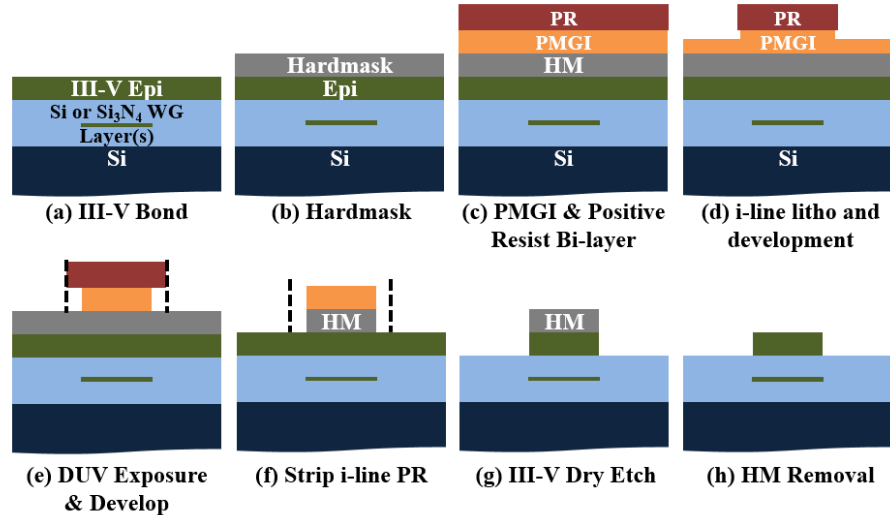


Figure 4.17: Process flow to reduce feature sizes by over developing a PMGI under layer.

In Fig 4.17(d) a standard i-line photolithography and development is made. This only partially develops the PMGI underlayer. In order to make a controlled undercut the rest of the PMGI is DUV flood exposed, masked by the i-line PR, and developed with a second developer which will not dissolve the i-line PR. This process may take a few cycles and I found that fewer, longer cycles gave slightly more control and a better result as characterized in the microscope.

For example, in Fig. 4.18, two samples with initial patterns in SPR955-0.9 i-line PR similar to Fig. 4.18(a) were undercut and then stripped to leave only the PMGI below shown in Fig. 4.18(b-c). These represent a split in repeated flood exposure development cycles. Figure 4.18(b) had six PMGI DUV flood exposure development cycles, while (c) had only three 4min flood exposures. The resulting

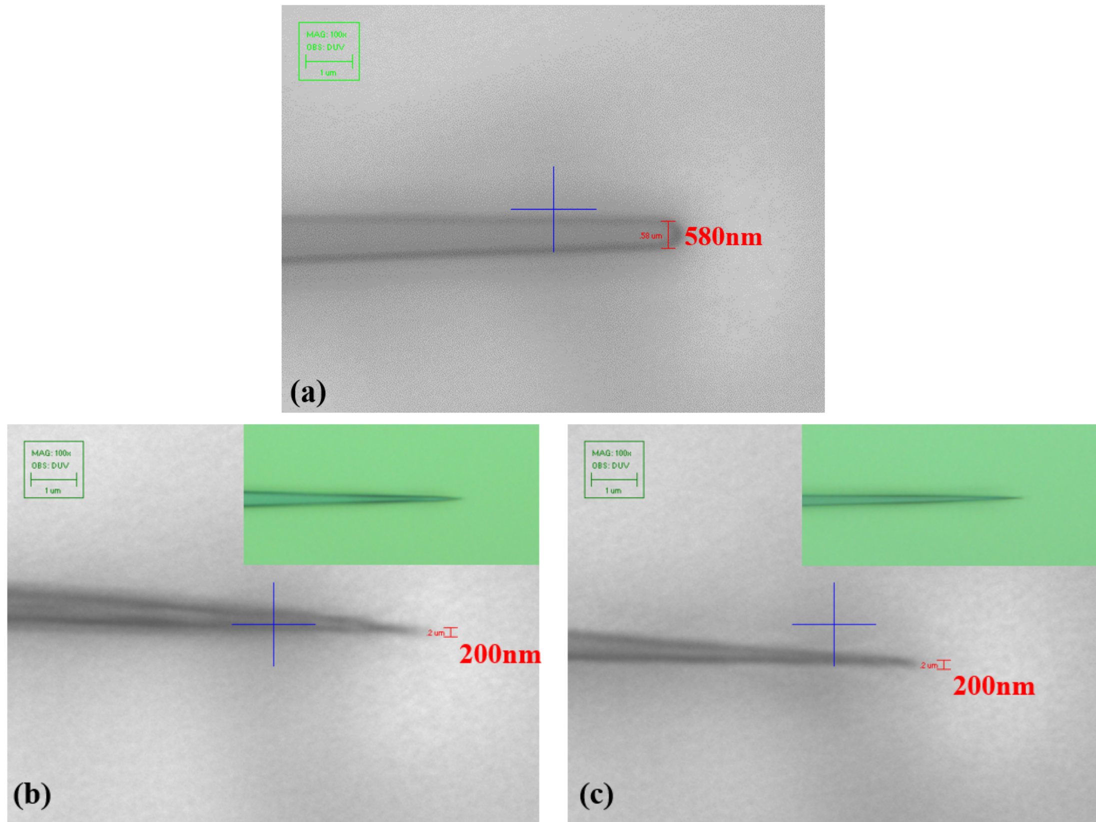


Figure 4.18: (a) Initial taper tip width from SPR955-0.9. (b-c) CUV microscope images of the split in final tapered PMGI patterns post-process. (b) 6x2min exposure, 3x60s develop (c) 3x4min exposure, 3x60s develop. Figure insets are visible microscope images.

pattern in (b) shows a slightly wispier tip than (c), but both (b) and (c) have significantly reduced taper tip widths from the original pattern (a).

In summary, a taper tip reduction process is shown using a bi-layer PR process in which the top (i-line) layer is selectively stripped following development of the (PMGI) underlayer. This enables i-line lithography, previously resolution limited to 500 nm, to achieve taper tips $<$200 nm.

Detailed Bi-layer Taper Tip Reduction Process

1. ACE,ISO,DI,PEII(O_2 Plasma)
2. Deposit oxide hardmask in PlamsaTherm PECVD 200 nm
3. ACE,ISO,DI,PEII(O_2 Plasma)
4. Dehydration bake 110 1min
5. Spin SF-11 (4krpm, 30sec)
6. Hotplate Bake (200C, 2min)
7. Spin SPR955.9 (3krpm, 30sec)
8. Pre-exposure bake 95C, 90s
9. Autostepper Exposure = 0.42s, Focus = +10
10. Post-exposure bake 110C, 90s
11. 40s Develop in MIF726
12. (repeat)DUV flood expose (2-5min), Develop (SAL-101A, 1-2min)
13. ACE soak 5min - to strip SPR955.9 from PMGI
14. 30s (100W,300mT) PEII O_2 descum

4.5.2 DUV ash-back taper process

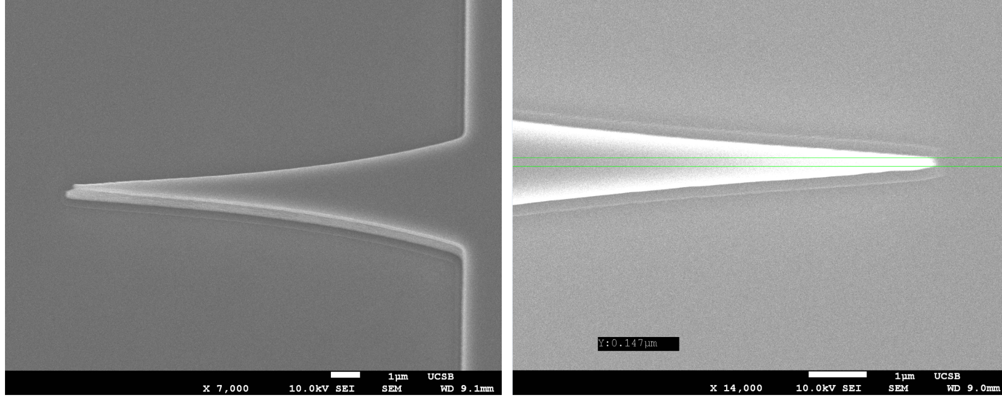


Figure 4.19: Characteristic p-mesa tapers following Cl_2/N_2 dry etch with SiO_2 hardmask and H_2SO_4:H_2O_2:H_2O (1:1:10) wet etch. (right) measurement of hard-mask taper tip width is 147 *nm*.

As taper tip widths decrease, alignment becomes more critical. The ASML PAS 5500/300 DUV stepper both has finer feature sizes and tighter alignment tolerance than the GCA 6300 i-line stepper. Alignment on the ASML tool is specified at 50 *nm* compared to 200 *nm* on the GCA. As the first taper is applied post-bond, and the epitaxial III-V membranes add >2 μm steps to the surface of the wafer, UV-6 DUV PR spun on at 1.5krpm (1 μm) without additional anti-reflective coating (ARC) layer is required to obtain sufficient coverage. Using this thick resist, we have reliably been able to achieve taper tip widths ~300 *nm* with the same sized mask feature. Narrower tip patterns are more sensitive to leveling and focus, and are not achievable without thinner resist.

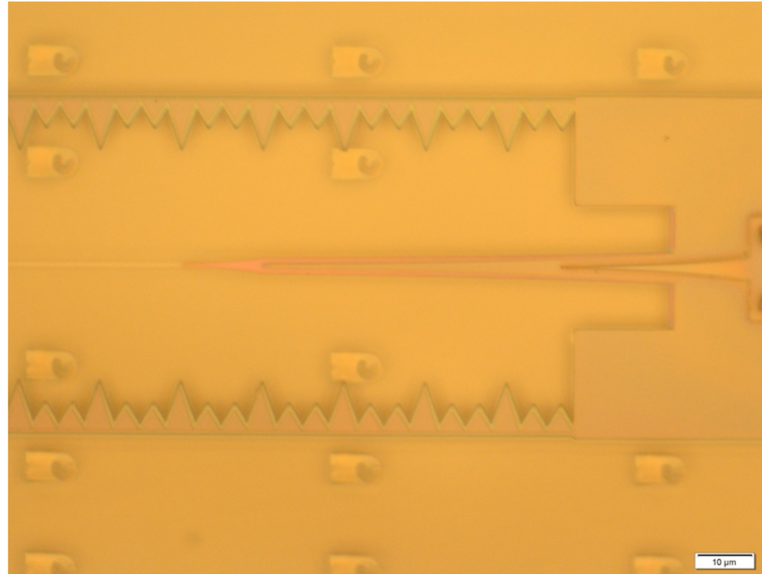


Figure 4.20: Microscope image of fabricated three layer taper with fine well-aligned taper tips using the DUV ash-back taper process

However, PEII (100W, 300mT) O_2 plasma applied post-development for 90s was shown to reduce the taper tip widths repeatably below 200 nm. This pattern is easily transferable to a SiO_2 hardmask and the p-mesa with subsequent dry etching as shown in Fig. 4.19.

This simpler ash back process was implemented for the results presented in Chapter 3 for its higher alignment precision and repeatability. The same process applied to p-mesa, n-taper, and SL-taper achieved similar results. Figure 4.20 show one result from a series of three layers formed with this process.

Chapter 5

Summary and Future Work

5.1 Summary and conclusions

This dissertation presented an argument for heterogeneous integration on bulk Si rather that with SOI by use of non-silicon waveguides and active semiconductor components placed by selective area bonding. Appropriate selection of waveguide materials, such as TiO_2 can even make it possible for these circuits to be athermalized well beyond conventional circuit designs. This integration will enable uncooled operation in compact packages for lower life-cycle cost and the performance enhancements of integration. A path towards this vision was provided by demonstrations of a series of components including, bonded lasers at 1060nm, taper transitions from GaAs to Si_3N_4, sidewall DBR gratings in Si_3N_4, and thermally insensitive passive ring structures using TiO_2 with $\sim$pm/K thermal drift.

5.1.1 Athermal devices and designs on Si

Following a review of the literature it was concluded that athermal packaging solutions do not exist for PICs with diverse and dispersed components and that individual athermal device designs are preferred. For these individual device designs, circuit based and material based approaches are considered. Circuit based solutions are an excellent selection for FIR filter functions such as MZIs and AWGs. The underlying principle of maintaining constant phase differences in these interferometric devices is well-explained in the literature, and specific device designs would be platform specific. Therefore, much of the Chapter 2 was devoted to materials based approaches, specifically with TiO_2, an inorganic CMOS compatible negative TOC material. Details such as sensitivity of this material to thermo-stress-optic effects and higher order TOC behavior which will be the ultimate boundaries confining future design of these structures were covered. These details should be considered in future work with this material.

It was concluded that TiO_2 core devices are much more fabrication tolerant and exhibit less performance degradation due to higher order TOC properties than TiO_2 clad structures. However, for integration with athermal laser structures, the simplest modification to the Hybrid Silicon Platform would be as a TiO_2 cladding. Given this fact, novel athermal laser designs were presented to passively

or with simple feedback schemes maintain wavelength stability over temperature and monitor power levels to stay within application limits.

Models and material data contributions were presented that should be of benefit for future explorations in this topic.

5.1.2 III-V/Si_3N_4 heterogeneous laser integration

A clear path toward heterogeneous laser integration of GaAs type lasers with Si_3N_4 waveguides was given with laser, mode converter, and DBR mirror demonstrations in Chapter 3. Additionally, an exploration of best approaches to reduce thermal impedance of these devices was given through heat transfer simulations.

Conclusions were that additional focus for tapers should be given to shorter designs, and that lasers with oxidation apertures have not proven to easily integrate with tapered mode converters due to oxidation of the tapers themselves. Therefore, shallowly etched narrow ridge designs should be considered as an alternative for index and current guiding and such lasers should be packaged with a flip-chip bonded approach to compensate the higher thermal impedance of these narrower devices.

5.1.3 Fabrication of heterogeneous GaAs/Si_3N_4 lasers

A detailed discussion of the heterogeneous laser process flow was given in Chapter 4. Observations and outcomes from process development into bonding GaAs type devices to SiO_2 on Si, etching the (Al)GaAs material with various ICP tools, oxidation of the high Al oxidation aperture layer post bond, and the best methods of reducing taper tip width are all detailed.

Key processing steps not included in prior laser process flows at UCSB included bonding using CMP planarization and surface roughness reduction, DUV stepper lithography of heterogeneous devices, improved ICP dry etch processing of (Al)GaAs, and AlGaAs oxidation of bonded lasers. Each of these required considerable time to develop and as much as possible the details of each process and, more importantly in many cases, the rationale for process decisions was included.

5.2 Future work

It is clear that much more work can be done in both the areas of athermal devices and heterogeneous integration of III-Vs on non-silicon PLCs. From my perspective, a few projects should be considered as direct continuations from this work.

First, a highly temperature stable DBR with a Si core would be advantageous for realization of the athermal laser designs presented in Section 2.4. The DBR presented in Section 2.3.1 both shows poor athermal performance and a strong impact of higher order TO effects from Si and TiO_2. Also, by making the grating in Si, the effective index is so high as to make the achievable Bragg wavelengths too long for our current lithography tools. It would be interesting to see the integration of the TiO_2 core type waveguide with a lower index for such an athermal grating. This would both be more athermalized and more fabrication tolerant, one example of a performance enhancement of using non-si waveguides.

Second, shallow ridge GaAs type lasers could be used rather than those confined by an oxidation aperture. These would not have an issue with electrically pumping the tapers that those with oxidized tapers would have. They would also not observe as much surface recombination as a deeply etched structure as you could design the distance to the QW sidewall to be wall away from the shallow ridge.

Finally, one of the visions we hope will come out of this type of heterogeneous integration is an ultra-broadband source from the ultra-violet (UV), visible (VIS), near infra-red (NIR), short-wave IR (SWIR), mid-IR (MIR), out even to long-wave-IR (LWIR). In order to span such a massive range, it necessary to have a broadband waveguide and a heterogeneous integration of all of the material

systems required to provide light across these wavelengths. Figure 5.1 gives the vision of this multiple-band integration.

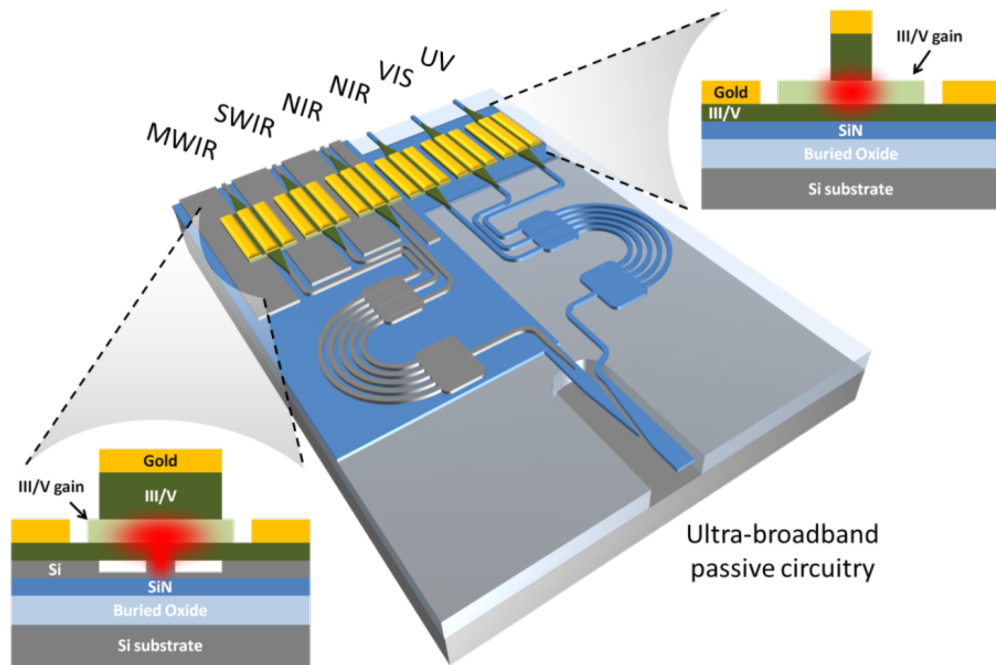


Figure 5.1: Schematic of a fully-integrated UV-MIR (6-bands shown) single-chip emitter concept, showing the two regions of the wafer with Si-on-Si_3N_4-on-SiO_2-on-Si and more standard Si and Si_3N_4 waveguides. (Artwork courtesy of Martijn Heck.)

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