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Semiconductor Nanowires for Optoelectronic, Renewable Energy and Retinal Prosthetic Applications

A dissertation submitted in partial satisfaction of the requirements
for the degree Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

Yi Jing

Committee in charge:

Professor Deli Wang, Chair
Professor Prabhakar R. Bandaru
Professor Andrew C. Kummel
Professor Jie Xiang
Professor Paul K.L. Yu

2013

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Chair

University of California, San Diego

2013

Dedication

To my family

Table of Contents

Signature Page ... iii
Dedication ... iv
Table of Contents ... v
List of Figures ... vii
List of Tables ... xi
Acknowledgements ... xii
Vita ... xv
Abstract of The Dissertation ... xviii
Chapter 1 : Introduction ... 1
1.1 Semiconductor Nanowires ... 1
1.2 Surface States and Surface Recombination ... 3
1.3 Light Absorption in Nanowires ... 6
1.4 Top-down Nanofabrication of Si Nanowires ... 9
1.4.1 E-beam lithography and nanoimprint lithography ... 9
1.4.2 Dry Etching of Si Nanowires ... 10
1.4.3 Metal Assisted Wet Chemical Etching of Si Nanowires ... 13
1.5 Bottom-up growth of nanowires ... 14
1.6 Scope of This Dissertation ... 15
Chapter 2 : Si Nanowire Photodetector Arrays for Image Sensing and Retinal Prosthesis Applications ... 18
2.1 Introduction—Nanowire Photodetectors ... 18
2.2 Single Nanowire Photoconductors ... 20
2.2.1 Fabrication of Individual Addressable Si Nanowire Photodetector Array ... 20
2.2.2 Single Si Nanowire Photodetector Characterization ... 23
2.2.3 Integration to CMOS for Image Sensor Applications ... 24
2.3 Axial P-N Junction Si Nanowire Photodetectors ... 27
2.3.1 Device Fabrication ... 27
2.3.2 Device Characterization ... 30

2.4 Radial Junction Si Nanowire Photodetectors ... 34
2.5 Integration with Nanowire Solar Cell and Self-powered System ... 38
2.6 Si Nanowire Photodetectors for Retinal Prosthesis ... 41
2.7 Conclusion ... 45
Chapter 3 : Si Nanowires for Photovoltaic Applications ... 47
3.1 Introduction ... 47
3.2 Planar Si Solar Cells with Si Nanowire Light Absorber ... 48
3.2.1 Introduction ... 48
3.2.2 Solution Etching of Si Nanowires ... 49
3.2.3 Device Fabrication and Characterization ... 51
3.2.4 Conclusion ... 54
3.3 Si Nanowire Radial Junction Solar Cells ... 54
3.3.1 Introduction ... 54
3.3.2 Nanoscale Doping ... 56
3.3.3 Device Fabrication ... 62
3.3.4 Effects of Doping Concentration of Nanowire Core ... 63
3.3.5 Auger Recombination ... 68
3.3.6 Effects of Surface Passivation ... 72
3.3.7 Conclusion ... 82
Chapter 4 : III-V Nanowire Solar Cells ... 84
4.1 Introduction ... 84
4.2 Catalyst-free Growth of InAs Nanowires ... 86
4.3 Catalyst-free Growth of InAs based Core/multi-shell Nanowires ... 103
4.4 Transport Properties of Single InAs Nanowire ... 111
4.5 III-V Core/multi-shell Nanowire Solar Cells ... 113
4.6 Conclusion ... 116
Chapter 5 : Conclusion ... 118
5.1 Conclusion ... 118
5.2 Future work ... 120
Bibliography ... 122

List of Figures

Figure 2.1: Process flow for fabrication of individually addressable vertical Si nanowire photoconductor array...21

Figure 2.2: (a) A SEM image (75 ° tilted view) of Si nanowires array. (b) A magnification of SEM image (45 ° tilted view) of Si nanowires. (c) A SEM image of Si nanowire photoconductor array. (d) Optical microscope image (top view) of Si nanowire photoconductor array..........................22

Figure 2.3: (a) Schematics of a single Si nanowire photodetector. (b) I-V curves of a representative Si nanowire device under dark and illumination with varying light intensities. (c) Curves of photocurrent as a function of incident light intensity at different applied biases...................................23

Figure 2.4: (a) Measured photocurrents of each Si nanowire photodetector in the array. (b) A simple demonstration of the response of the photodetector array as an image sensor to uniform white light illumination with each device representing one pixel.. 26

Figure 2.5: Schematics of fabrication process of Si axial p-n junction photodetectors.... 28

Figure 2.6: (a) SEM images of Ni dot array. (b) SEM images of vertical Si nanowire array. (c) A SEM image of Si nanowires embedded in PMGI with expose nanowire tips. (d) A SEM image of Si nanowire device with sputtered ITO top contact at 45^0 tilted view. 29

Figure 2.7: (a) Schematic of a Si axial junction nanowire photodiode. (b) Semi-log I-V curves of a typical photodiode under dark and with white light illumination (100 mW/cm^2). (c) Spectra photoresponsivity and specific detectivity of the photodiode under zero bias. 31

Figure 2.8: Fabrication Process of Si radial junction nanowire photodiodes. 34

Figure 2.9: Representative I-V curves of the Si radial junction nanowire photodiode measured under dark and illumination with a white light source (Xe arc lamp, 100 mW/cm^2). 36

Figure 2.10: Spectra responsivity of Si radial junction nanowire with Al_2O_3 passivation...37

Figure 2.11: Illustration of the Si axial junction nanowire photodetector driven by a Si

axial junction nanowire solar cell and the equivalent circuit. 38

Figure 2.12: I-V curve of a representative Si nanowire axial p-n junction solar cell measured with AM 1.5G illumination (100 mW/cm^2)............................ 39

Figure 2.13: (a) Spectra responsivity of the nanowire photodetector driven by a nanowire solar cell (▲). The (●) curve is the responsivity at zero voltage bias for comparison. (b) Enhancement factor of the responsivity.. 40

Figure 2.14: Illustration of a Si axial p-n junction nanowire photodetector served as photoreceptor to generate charges for retinal neuron stimulation. 44

Figure 2.15: Time-resolved photocurrent measured by switching white light illumination at a frequency of 1000 Hz.. 45

Figure 3.1: SEM images of Si wafers etched for different amounts of times (a) 1 min; (b) 5 min; (d) 10 min; (d) 15 min. (e) Plot of nanowire length vs. etch time. (f) Optical image of a large-area Si nanowire array created on a 2-inch Si wafer with 20 min etching. 49

Figure 3.2: Illustration of fabrication process of planar Si solar cell with nanowire absorber. 51

Figure 3.3: SEM images of Si nanowire based solar cell with ITO front contact at (a) 45 °tilted view, and (b) 75 °tilted view. 52

Figure 3.4: (a) I-V characteristics of a typical Si nanowire based solar cell measured under dark condition. (b) I-V characteristics of a typical Si nanowire based solar cell (blue) and a planar device (red) with AM 1.5G illumination (100 mW/cm^2). 53

Figure 3.5: Illustration of the radial junction nanowire solar cell. 54

Figure 3.6: Schematic of boron diffusion using SOD in RTA. 57

Figure 3.7: I-V curve of doped Si p-n junction. One-step diffusion was carried out at 800 ℃ for 20 s. The inset is the schematic of the p-n diode. 58

Figure 3.8: SIMS analysis of boron distribution profile in planar Si. The Si was doped using one-step diffusion at 820 ℃ for 20 s, 40 s and 60 s, respectively. The doping concentration of n-type Si wafer is 6.5×10^{17} cm^{-3}. 59

Figure 3.9: Silvaco Athena simulations of boron profiles in Si diffused at 820 ℃ for 20 s in (a) planar geometry and (b) cylindrical geometry. N-type Si with an arsenic concentration of 6.5×10^{17} cm^{-3} is considered. 61

Figure 3.10: The fabrication process of Si nanowire radial junction solar cells. 62

Figure 3.11: SEM images of (a) as-etched Si nanowires, (b) Si nanowires embedded in PMGI, and (c) Si nanowires with 300 nm ITO top contact. 63

Figure 3.12: (a) Schematic of Si radial junction nanowire solar cell. I-V characteristics of Si nanowire radial junction nanowire solar cells with a core doping concentration of (b) 1×10^{15} cm^{-3}, and (c) 6.5×10^{17} cm^{-3}. 64

Figure 3.13: Simulated band diagrams of Si nanowires under zero bias. The arsenic doping concentrations of Si nanowire cores are (a) 1×10^{15} cm^{-3}, and (b) 6.5×10^{17} cm^{-3}. The nanowires were doped using boron diffusion at 820 ℃ for 20 s. 66

Figure 3.14: Silvaco Athena Simulation of doing profile of Si radial p-n junction nanowire. The radial p-n junction was created using two-step boron diffusion. The pre-deposition step was first carried out at 800 ℃ for 10 s, followed by a drive-in process at 800 ℃ for 3 hrs. 70

Figure 3.15: I-V curves of Si nanowire radial junction solar cells measured under AM 1.5G illumination (100 mW/cm^2). 71

Figure 3.16: SEM images of Si radial junction nanowires with a layer of passivation material as shell: (a) PECVD Si_3N_4, (b) ITO, and (c) ALD Al_2O_3. 76

Figure 3.17: I-V curves of Si radial junction nanowire solar cells with various diffusion conditions and passivation layer measured under AM 1.5G illumination (100 mW/cm^2).. 77

Figure 4.1: SEM Images of InAs growth on Si (111) at 45° tilted view. The growth were done at 550 ℃ for 5 min. The surface of Si substrates were treated differently before growth. 88

Figure 4.2: SEM Images of InAs growth on Si (111) with 45° viewing angle. The growth was done at 550 ℃ for 5 min with substrate baking in H_2 at 635 ℃ for 10 min prior to growth. The surface of Si substrates were treated differently before growth. Scale bars are 1 μm.. 92

Figure 4.3: (a), (b) and (c) are SEM images of InAs nanowires grown for 5 min on Si(111) substrate. Si was treated with BOE etch for 30 s and rinsed in running DIW for 8 min. (d) Column graph showing distribution of nanowire diameters. 95

Figure 4.4: TEM micrographs of InAs nanowires. (a) Low resolution image of InAs nanowires. The corresponding electron diffraction pattern is shown in the inset. (b) High resolution TEM image of bottom portion of a nanowire. (c) High resolution TEM image of the top portion of a nanowire................ 97

Figure 4.5: Cross sectional TEM images of InAs nanowires grown for 5 min on Si (111). (a) Low resolution TEM showing InAs nanowires embedded in PMGI. (b) and (c) HRTEM of InAs/Si interface. Fast Fourier transforms of (d) region I, (e) region II, (f) region III, and (g) region IV. 101

Figure 4.6: SEM images of InAs/InGaAs core-shell nanowires grown on Si (111) substrate (45 ° tilted view). (b) and (c) are higher magnification images of InAs/InGaAs core/shell nanowires (75 ° tilted view). 104

Figure 4.7: SEM images of InAs/InGaAs/GaAs core/multi-shell nanowires (45 ° tilted view). 106

Figure 4.8: (a) and (b) are SEM images of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires at 45 ° tilted view. Inset shows the top-view image. 107

Figure 4.9: TEM images of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires.. 108

Figure 4.10: Ids-Vds measurements of a single InAs nanowire FET using a bottom-gate structure; inset is the Ids-Vgs curve and a SEM image of the device. 112

Figure 4.11: I-V measurement of a single InAs(n)/InGaAs/GaAs/InGaP(p) core/multi-shell nanowire diode. Inset is a SEM image of the single nanowire device. 114

Figure 4.12: (a) Schematic of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowire solar cell. (b) A SEM image of front surface of device with ITO front contact. I-V measurement of InAs(n)/InGaAs/GaAs/InGaP(p) nanowire solar cell (c) under dark, and (d) with AM 1.5G illumination... 114

Figure 5.1: (a) Schematic of PDMS transfer process. SEM images of (b) as-etched Si nanowire array, (c) Si substrate after peeling off the PDMS film, (d) Si nanowires embedded in PDMS film. Optical images of PDMS films with embedded (e) Si and (f) InAs nanowires... 120

List of Tables

Table 3.1: Comparison of Si solar cells with and without nanowire as light absorber.. 53

Table 3.2: Summery of performance of solar cells with different n-type core doping concentrations. 64

Table 3.3: Comparison of Si nanowire radial junction solar cells with different shell doping concentrations. The surface states of nanowires were passivated using a layer of ITO shell. 72

Table 3.4: A list of samples with different diffusion conditions and passivation materials. 75

Table 3.5: Summary of performance of solar cells with different p shell doping and passivation materials. 78

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Publications

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ABSTRACT OF THE DISSERTATION

Semiconductor Nanowires for Optoelectronic, Renewable Energy and Retina Prosthetic Applications

by

Yi Jing

Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California, San Diego, 2013

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This dissertation presents works on two significant application areas of semiconductor nanowire. The first is nanowire photodetectors and their applications for image sensing and retinal prosthesis. The second is nanowire solar cells for renewable energy application and both Si and III-V nanowire devices are extensively discussed.

Three structures of Si nanowire photodetectors are presented, including nanowire photoconductor, axial and radial junction nanowire photodiodes. Using the design of a crossbar structure, an individually addressable vertical Si nanowire

photoconductor array was presented, followed by discussion on integration to CMOS for image sensing applications. In addition, the Si axial junction nanowire photodiodes were also demonstrated, which showed excellent detectivities in visible spectrum at zero bias, with a peak value of 2.14×10^{13} Jones at wavelength of 636 nm. Furthermore, the radial junction nanowire photodiodes were discussed as well, which exhibited enhanced photo responsivity due to shorter carrier separation and collection paths. These nanowire photodiode arrays promises potential application for retinal prosthesis by replacing the dysfunctional photo receptors in human retina.

In addition to photodetectors, I also demonstrated Si nanowire solar cells including both planar Si solar cells with nanowire absorber and Si radial junction nanowire solar cells. A low-cost chemical etching method was introduced to fabricate large-scale Si nanowire array as light absorber to improve the light absorption of planar Si solar cells. The efficiency of this device is over one order of magnitude higher than the one without nanowires. In addition, the Si radial junction nanowire solar cells were studied. A systematic study on design parameters, including nanowire core and shell doping concentrations, band structures and surface passivation methods, were discussed to achieve optimal device performance. With optimal design, a power conversion efficiency of 8% was demonstrated.

InAs based nanowire core/multi-shell heterojunction solar cells were investigated as well. A systematic study of catalyst-free MOCVD growth of InAs

nanowires on Si substrates was performed. Various growth parameters and surface treatment methods were studies to achieve optimal nanowire growth and reveal the growth mechanism. Based on the InAs nanowire growth, the III-V core/multi-shell nanowires were successfully fabricated and solar cells have been demonstrated.

Chapter 1: Introduction

1.1 Semiconductor Nanowires

A nanowire is a one dimensional (1D) nanostructure, with a diameter constrained to the nanometer scale, typically around from a few nm to a few hundred nm, and an unconstrained length on the order of several μm to tens of μm. The first semiconductor nanowire, or so called whisker, was experimentally demonstrated by Wagner and Ellis in 1964.[1] Nowadays, study of semiconductor nanowires has been one of the most active fields of research. Owing to their unique properties resulting from one dimensionality and large surface-to-volume ratio, nanowire structures are not only utilized for exploring phenomena at the nanoscale but also expected to play a critical role for future applications in electronics,[2] photonics,[3] thermoelectrics,[4, 5] chemical/bio-sensing,[6] optoelectronics[7, 8] and renewable energy.[9, 10] From a perspective of fundamental physics, the 1D nanowire structure is an ideal platform to study the properties which may be inaccessible or difficult to achieve in conventional bulk materials. In addition, the properties of nanowire devices can be enhanced as a result of combination of shape, density and strong confinement of photon, phonon and electrons. For example, vertical nanowire arrays can exhibit absorption of light close to the Lambertian limit with properly designed geometry.[11] On the other hand,

insignificant parameters of materials in conventional devices may greatly influence the device performance as the size enters into nanoscale. For instance, because of the high surface-to-volume ratio, trapping of carriers at the surface states drastically affects the transport and optical properties of nanowires. The presence of surface states could significantly enhance the photoconductive gain by trapping one type of photo-generated carrier while leaving behind the other unpaired carriers,[8] or increase surface combinations thus reduce the solar cells efficiency. Therefore, it is essential to understand the electrical and optical properties of nanowire structures in order to provide design guidance for high-performance nanoscale devices for future applications.

A large variety of preparation methods have been developed to fabricate nanowire structures and from a broad range of materials. The fabrication methods mainly can be categorized into two groups: top-down and bottom-up. Fabrication of nanowires with well controlled size, shape, position and doping has been achieved using both top-down and bottom-up approaches. Each approach has its pros and cons. The top-down approach utilized lithographic or self-assembled patterning of nanoscale mask structures on the substrate; then selectively etches the materials away from the substrate to form nanowire structures. Both planar and vertical nanowire structures have been demonstrated using top-down approach. On the contrary, bottom-up approach uses gases comprising of the constituent materials to epitaxially grow

nanowires, either with the assistant of metal catalysts or catalyst-free methods. With the rapid progress of fabrication technologies, various novel nanowire structures have been demonstrated, including radial (core-shell) homo- and heterojunctions, axial structures and 3D branched nanowire configurations.[10, 12-17] The enriched versatile nanowire structures greatly enhance the device functionality for practical applications.

1.2 Surface States and Surface Recombination

Due to the high surface-to-volume ratio, surface states, such as dangling bonds, defects, and adsorbates, play a much more dominant role in electrical, carrier transport and photoconduction properties of nanostructures than that in thin films and bulk crystals. As a result, the performance and function of nanowire devices are expected to be strongly influenced by surfaces states. Such high surface sensitivity, although beneficial for some device applications, presents challenge to device fabrication as it leads to difficulty in the reproducibility and controllability of device performance. Thus, it raises the importance of understanding mechanism and careful engineering of the surface states so that we can fully use the benefits of surface states while keep the deleterious impacts to the minimum.

The electrical properties of nanowires, such as conductivity and doping type, strongly depend on the effects of surface states and may be surface-dominated with increasing of the surface-to-volume ratio. For example, the transport properties of Si

nanowires are strongly influenced by the surrounding ambient and surface conditions.[18, 19] In air, gas molecules (mainly water molecules) get absorbed on Si nanowires due to the large number of dangling bonds and defects present on the surfaces. The absorbed water molecules would trap electrons from Si nanowires, forming OH^- ions. The negative charges on the surfaces of Si nanowires would cause surface band bending, and lead to accumulation of excess holes in the valence band. In the case of p-type Si nanowire, the excess holes contribute to the electrical transport and enhance conductance. For n-type Si nanowire, however, the excess holes from surface adsorption may fully compensate the electrons in nanowire and convert the nanowire to p-type.[20] This phenomenon is more pronounced for nanowires with smaller diameter, owing to the larger surface-to-volume ratio.

The effects of surface states also influence the photoconductive properties of nanowires. It has been recently observed and discussed that modification of surface states leads to high gain in photoconductive.[8, 18, 19, 21-26] For example, in ZnO nanowire UV photodetectors,[8] oxygen molecules are absorbed on the oxide surface and capture the free electrons present in the n-type semiconductor. Due to the Fermi-level pinning at the surface of nanowires, a low conductivity depletion layer is formed near the surface. Depending on the diameter and doping profile of nanowire, it is possible to obtain completely depleted nanowire or nanowire with thin conducting channels, which leads to low dark current.[21] When photons with energy above bandgap E_g impinge on the

nanowire surface, electron-hole pairs are generated. Holes migrate to the surface along the potential slope produced by band bending and discharge negatively charged adsorbed oxygen ions, while unpaired electrons prefer the inner part of the nanowire, increasing the conductivity and passing through the nanowire multiple times before recombination, which leads to photoconductive gain as high as 10^8.[8]

Besides the benefits resulting from the high surface-to-volume ratio, the nanowire device may also suffer from deleterious effects caused by large surface area if not well designed. One of the most important factor need to be considered is the surface recombination for solar cells. In the surface recombination process, an electron from the conduction band recombines with a hole in the valence band via defect level within the band gap. The increased recombination of photo-generated carriers at the dramatically increased surface area of the nanowire solar cells decreases the efficiency by reducing device short-circuit current and open-circuit voltage. For solar cells, implementation of passivation techniques is essential in order to achieve minimum surface recombination.[27]

From the above examples, we conclude that surface states can dominate the transport, photoconductive and recombination properties of nanowire devices. These surface-related phenomena should be generic to any nanowire systems with different materials and diverse architectures, of which surface constitutes a significant portion.

1.3 Light Absorption in Nanowires

The light absorption is one of the most important processes that determine the performance of nanowire photodetectors and solar cells. Due to the unique one-dimensionality and small size, there are many fundamental advantages of nanowire structures for light absorption, such as suppressed reflection, reduced transmission and weak angular dependence. Optimal design of nanowire structures with enhanced absorption is of great importance to achieve high performance nanowire devices. In the following, we will start our discussion with photon management of individual nanowires, which are basic building blocks of devices.

For conventional thin film or bulk devices, light absorption mainly relies on the intrinsic optical properties of the materials. However, with the emerging of nanowire devices, engineering of light absorption through control over the size, dimension and orientation of the nanowires becomes important. Cao et al proposed and demonstrated a novel method, called leak-mode resonances, for optimal design of light absorption.[28] When illumination wavelength matches one of its leaky-modes, strong resonances occur inside a single nanowire, resulting in trapped light in circulating orbits by multiple total internal reflections from the periphery, leading to enhanced absorption.[29] Owing to the coupling to different transverse electric (TE) and transverse magnetic (TM) leak-mode resonances of the nanowire, distinct peaks occur at matched wavelengths. At the resonance wavelengths, the external quantum efficiency of nanowire is substantially

larger than that of the thin film. Of particular importance is that subbanggap photoresponse can also be dramatically improved (>25-fold) using leak-mode resonance. Theoretical simulation using full-field finite difference frequency domain (FDTD) further confirms that absorption enhancement results from the leak-mode resonances. Optimal wavelength selectivity of single nanowire photodetectors can be achieved through careful design of diameters. Due to the dependence of resonances on size parameter, the absorption peaks increase monotonically with increasing nanowire diameters.[30]

In addition to single nanowire, vertical nanowire arrays also show enhanced light absorption.[31] By embedding the vertical nanowires into low refractive index materials, nanowires with diameter comparable to or smaller than the wavelength of incident light can absorb not only the portion of the wave directly on it, but also the surrounding wave. Numerical simulation shows that the coupling of light results in significantly larger percentage of photon energy within the nanowire volume than the physical fill factor, especially at larger pitch size.[31]

Total absorption is determined by both reflection and transmission. For many thin film devices, surface reflection is one of the main mechanisms responsible for the loss of quantum efficiency and usually an antireflection coating is required.[32-34] On the contrary, numerical analysis have shown that the reflectance of nanowires is significantly lower than that of the thin film in the entire spectral range due to the

reduced density of the nanowire structure.[35] Experimental measurements on optical properties of Ge nanowires further indicate a monotonic reduction of reflectance with decreasing diameter of nanowire.[36] This phenomenon can be attributed to the enhanced light scattering when the diameter of nanowires becomes comparable to or smaller than the wavelength of incident light.[37]

Furthermore, both numerical simulations and optical measurements of Si and Ge nanowire arrays show negligible transmission at small wavelengths.[35, 36, 38] However, at long wavelengths, nanowire structures exhibit higher transmittance than thin film. As the nanowire diameter is reduced, a blue shift in wavelength corresponding to the onset of measurable transmittance is observed.[36] The higher transmittance cannot be compensated by the low reflectance, resulting in reduced absorption of long wavelength light in the nanowires. The absorption of low energy photons can be improved by careful design of physical fill factor. Although the nanowire arrays with smaller fill factor have shown better absorption of small wavelength light, calculations show that nanowires with larger physical fill factor has higher absorption in the long wavelength regime. By changing physical fill factor, the overall absorption of nanowire structure can be increased close to its thin film counterpart at long wavelengths. Further enhancement of light absorption at long wavelengths can be achieved using dual-diameter nanowire arrays.[36] In this design, the light reflection can be suppressed by

small diameter nanowire tips; while the light transmitted to the larger diameter base can be efficiently absorbed due to larger physical fill factor.

1.4 Top-down Nanofabrication of Si Nanowires

In general, there are two approaches to fabricate Si nanowires using top-down process: ICP/RIE dry etching (a combination of inductively coupled plasma and reactive ion etching) and chemical wet etching. The dry etching of Si nanowires usually requires patterning of Si wafers to form nanoscale dots array as etch mask; then the nanowires are created by selectively etching away of Si using ICP/RIE process. On the other hand, Si nanowires can also be formed by chemical etching either using a mask or by a maskless approach. In the following sections, we will discuss the two approaches in details.

1.4.1 E-beam lithography and nanoimprint lithography

For fabrication of position-controlled nanowire array, the top-down process usually starts with pattern definition of the substrate. Traditionally, the nanoscale patterns are created using E-beam lithography and more recently nanoimprint lithography was also developed to fabricate large area arrays of nanoscale pattern.

By using a beam of electrons to expose the resist, E-beam lithography can beat the diffraction limit of light and make nanoscale structures with precisely controlled position, shape and size. However, the main disadvantage of the E-beam lithography is

the long processing time, which dramatically increases the manufacturing cost. Also, the long exposure time leaves the users vulnerable to beam drift or instability which may occur during the exposure. Thus, the application of this technique is limited to pattern small area structures.

On the contrary, nanoimprint lithography provides an alternative way to define nanoscale patterns with low cost and high throughput. In a nanoimprint lithography process, a thin layer of imprint resist is spin-coated onto the substrate; then a mold, which has predefined patterns, is brought into contact with the sample and they are pressed together under certain pressure. The resist is then either thermally or UV cured and becomes solid. After mold separation, the pattern is transferred from mold to the resist. A similar pattern transfer process can be used to further transfer the pattern from the resist to the underneath substrate using dry etch.[39] Due to the quick processing and high throughput, nanoimprint lithography technology has been used to fabricate devices in electrical, optical, photonic and biological applications.[40-44]

1.4.2 Dry Etching of Si Nanowires

Reactive ion etcher (RIE) has been widely used in industry for fabrication of integrated circuits and microeletromechanical (MEMS) systems. It uses chemically reactive ions to remove materials deposited on wafers. By independently controlling the ion density and the momentum imparted to the ions, various highly fined Si structures can be achieved, such as high aspect ratio Si nanowires.

Generally speaking, there are two types of configurations of RIE systems: the parallel plate RIE system and inductively coupled plasma (ICP) RIE system. A typical parallel plate system consists of a cylindrical vacuum chamber with two parallel plates (which form a capacitor) sitting at the top and bottom of the chamber respectively, and a wafer platter situated in the bottom portion of the chamber. The wafer platter is electrically isolated with the rest of chamber. Gases enter through the small inlets in the top portion of the chamber and exit to the vacuum system through the bottom. When a radio frequency (RF) voltage, typically set at a frequency of 13.56 megahertz, is applied to the plates, plasma is generated in the chamber owing to the strong RF electric field. In each cycle of the field, electrons are accelerated up and down in the chamber. However, the much more massive ions cannot track the rapidly oscillating electric field changes and moves relatively little in response to the RF electric field. Accumulation of negative charges on the platter builds up a negative voltage, which forms electric field between the parallel plates. The resulting electric filed caused by this voltage drives the negative ions in plasma towards the wafer platter, where they collide with the sample to be etched.

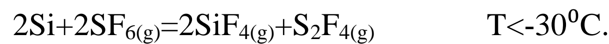
In an ICP process, the excitation of plasma is similar to the parallel plate system, except that instead of RF electric field, the plasma is generated by an RF magnetic field, which is delivered inductively, via a coil wrapped around RIE plasma discharge region. The changing magnetic field induces an electric field that tends to

circulate the plasma in the plane parallel to the plates. With ICP process, very high plasma densities can be achieved, although the etch profile tends to be more isotropic.

Usually, the ICP/RIE process, which combines the parallel plate and ICP RIE, is employed to etch Si. In this process, the ICP is utilized as a high density source of ions which increases the etch rate, whereas a separate RF bias is applied to the Si substrate to create directional electric fields near the substrate to achieve more anisotropic etch profiles. In other words, the ICP controls the number of ions reaching the substrate to chemically etch while the parallel plate RIE controls the momentum of the ions reaching the substrate to mechanically etch.

In this work, the ICP/RIE process (gases: CF_4 and SF_6) is employed to etch Si nanowires using Oxford Plasmalab 100 system. The Si etching mainly relies on SF_6 gas. When Si is etched by SF_6 gas, the following two spontaneous etching reactions may occur:[45]

$$Si+2SF_{6(g)}=SiF_{4(g)}+2SF_{4(g)} \qquad T>100^{0}C,$$



$$2Si+2SF_{6(g)}=2SiF_{4(g)}+S_2F_{4(g)} \qquad T<-30^{0}C.$$

It can be seen that the all byproducts are volatile. The silicon-containing product is SiF_4 gas while the sulfur-containing product depends on temperature. The equilibrium product is either SF_4 gas for temperatures above 100^{0}C, or Si_2F_2 for temperatures below -30^{0}C. Both products can exist when temperature is between -30^{0}C to 100^{0}C.

To achieve high aspect ratio Si structures, passivating the sidewalls by

dissociating gas reactants in a plasma environment is a common strategy. The passivation layer protects sidewall from lateral etching and improves anisotropy. There are several gases can function as passivating agents, such as O_2 and C_4F_8. C_4F_8 is the most common one and used in this work. During sidewall passivation, C_4F_8 breaks down in the plasma to produce CF_2 and longer chain radicals. Then CF_2 is adsorbed to from a teflon-like polymer, i.e. the passivation layer, on the sidewall and base surfaces.[46]

In summary, with a combination of SF_6 and C_4F_8 gases, the etch gas SF_6 is injected and ionized in the chamber to provide fluorine ions and radicals to etch Si, while simultaneously passivation gas C_4F_8 is injected and ionized to create a passivation layer to protects sidewall and base surfaces of Si from chemical etching. However, the passivation layer on the base surface is etched away faster by the milling of fluorine ions than re-deposition. Thus, sidewall of Si is protected by the passivation layer while base surface is free to etch, leading to formation of high aspect ratio Si nanowires.

1.4.3 Metal Assisted Wet Chemical Etching of Si Nanowires

Metal assisted wet chemical etching is a rapid and low-cost technique to fabricate large-scale Si nanowire arrays.[47-51] This simple technique involves only wet chemical processing under the near ambient conditions and is easy to scale up to wafer size, leading to a low-cost operation. The etching of Si is usually catalyzed by metal

particles formed on Si surface via either electroless deposition or physical vapor deposition, such as sputtering. The Si surface that comes in contact with the metal is selectively etched in hydrofluoric acid (HF) based aqueous solution, leaving behind arrays of Si nanowires.[48] For instance, by immersing the Si wafers in HF aqueous solution containing silver nitrate ($AgNO_3$), the Si etching and silver deposition start to occur simultaneously at the surface. The deposited silver nanoclusters act as local cathodes while the surrounding areas serve as anodes. Thus the Si underneath the silver nanocluster is oxidized into SiO_2. Subsequently, SiO_2 is dissolved by HF, leaving a pit underneath the Ag nanocluster. As a result, successive deposition of silver produces a dendrite layer covering Si substrate and vertically aligned Si nanowires are created.[47]

1.5 Bottom-up growth of nanowires

The bottom-up growth has been widely used to synthesis various semiconductor nanowires, including Si,[1] Ge,[52] III-V compounds[53-55] and so on. The mostly used method for nanowire growth is the vapor-liquid-solid (VLS) process, which was firstly proposed by Wagner and Ellis to grow Si nanowires in 1964.[1] By introducing a catalytic metal nanoparticle, which can absorb reactants in vapor phase to form supersaturated liquid alloy inside the nanoparticle, the single crystal nanowires can grow from the nucleated seeds at the liquid-solid interface.[53] Through control of

the growth conditions, one could control the length, location, morphology and doping of the nanowires. Au is the most commonly used catalyst for single crystalline nanowire growth. However, it forms unwanted deep level traps in semiconductor nanowires during growth, which is notoriously deleterious to the performance of nanowire devices.[56-58] To circumvent this issue, research efforts have been devoted to develop growth method without assist of Au particles, such as self-catalyzed growth[59-65] and catalyst-free growth. The self-catalyzed growth is also categorized as VLS growth since one or more nanowire elements, usually In[61] or Ga[62] droplets, are used as the seed nanoparticles. On the other hand, no catalyst is used during the nucleation and growth for the catalyst-free method. For example, selective-area growth uses partially masked substrate, usually by an oxide or nitride layer, with lithographically defined opening pattern. Subsequently, semiconductor materials nucleate and initiate nanowire growth in the openings after increasing the temperature and introducing the reactant gases.

1.6 Scope of This Dissertation

The scope of this dissertation is as follows:

Chapter 2 presents Si nanowire photodetectors and their applications for image sensing and retinal prosthesis. We discuss three structures of nanowire photodetectors: nanowire photoconductor, nanowire axial junction photodiode and nanowire radial

junction photodiode. Firstly, fabrication and understanding of a single Si nanowire photoconductor is provided. Using the design of a crossbar structure, an individually addressable vertical Si nanowire photoconductor array is presented, followed by discussion on integration to CMOS for image sensing applications. Secondly, Si nanowire axial and radial junction photodiodes are discussed. Both photodiodes exhibit good photo responsivity at zero bias. These nanowire photodiode arrays could be used to replace dysfunctional photo receptors in human retina, promising potential application for retinal prosthesis.

Chapter 3 discusses the Si nanowire based photovoltaic devices, including planar Si solar cells with nanowire absorber and Si nanowire radial junction solar cells. First a planar Si solar cell with nanowire absorber is introduced. A low-cost chemical etching method is used to fabricate large-scale vertically aligned Si nanowire array. The Si nanowire array is utilized as light absorber to improve the light absorption of the planar solar cell. Then Si nanowire radial junction solar cells are presented. The fabrication process and key factors that contribute to achieving optimal device performance are discussed.

In chapter 4, we discuss III-V nanowire core/multi-shell heterostructure based photovoltaic devices. First a simple catalyst-free MOCVD method is studied to growth vertical InAs nanowires on low-cost Si substrates. Several aspects of the growth method are investigated to achieve optimal nanowire growth and elucidate the growth

mechanism. Then this method is extended to growth InAs based nanowire core/multi-shell heterostructures. The morphology and structure properties of nanowire heterostructures are characterized by scanning electron microscope (SEM) and transmission electron microscopy (TEM). Photovoltaic devices are fabricated and characterized, demonstrating a III-V nanowire tandem cell on low-cost Si substrate.

In chapter 5, a summary of the dissertation and possible areas for future work are discussed.

Chapter 2: Si Nanowire Photodetector Arrays for Image Sensing and Retinal Prosthesis Applications

2.1 Introduction—Nanowire Photodetectors

Semiconductor nanowires have been extensively investigated as building blocks for nanoscale electronics[2] and optoelectronics[7, 66-68] due to their unique properties. In particular, nanowire photodetectors have attracted significant interest because of promising applications for single photon detection, image sensing, medical imaging and diagnosis. Due to the unique one-dimensionality and large surface-to-volume ratio, semiconductor nanowires exhibit high internal gain and high sensitivity.[8, 31] With rapid progress of the fabrication technology, numerous nanowire structures have been realized without constraint of lattice mismatch using either top-down or bottom-up processes with precisely controlled doping, size, shape and position, including structures which are traditionally inaccessible. The enriched versatile nanowire structures further enhance nanowire photodetection applications. Therefore, a deep understanding of the physical mechanism and versatile design of the nanowire structures is crucial to obtain optimized nanowire photodetectors and consequently achieve higher performance devices for practical applications.

Photodetectors are semiconductor devices that convert incident light to

electrical signal. There are different types of photodetectors, such as photoconductors and photodiodes, but the general physical mechanism of photodetectors is the same. Basically, the performance of a photodetector depends on three processes: (1) carrier generation by incident light; (2) carrier transport; and (3) extraction of carriers as terminal current to provide the output signal.[69]

Photoconductors conduct a single carrier type, whereas photodiodes extract carriers of each type.[69] In a photoconductor, one type of carrier is trapped while the other circulates under the influence of an electric field. The ratio of τ_n/τ_t (here τ_n is the carrier lifetime; τ_t is the transit time) gives the photoconductive gain, which is determined by how fast the electrons transit across the electrodes and contribute to the photocurrent in the circuit before they recombine with holes. Photoconductors are capable of high gain because of traps, which delay band-to-band recombination and impede the extraction of trapped carriers. In nanowire structures, the effect of traps is much more influential on the performance of photodetectors.

Photodiodes consist of two materials, with at least one being a semiconductor, where a large difference in the materials' work functions produces a built-in potential. An internal electrical field in the semiconductor depletion region near the junction propels electrons and holes in opposite directions. Response times of photodiodes are typically microseconds or less for direct-gap semiconductors, and can be shorter than electron-hole recombination times. Nanowires offer a variety of opportunities to design

photodiode architectures, including homo- or hetero-junction devices formed either axially along the nanowire[70] or radially by core-shell junctions.[15, 71]

2.2 Single Nanowire Photoconductors

In this section, we present fabrication of a vertical Si nanowire photoconductor array with individual addressability using E-beam lithography and an ICP/RIE process. The electrical properties of devices are determined by I-V measurements. Using a design of crossbar structure, the photoconductor array can be individually addressed and function as an image sensor. This reliable and repeatable fabrication process results in high yield (100%) functional devices in the array. The uniformity of the device performance was also discussed. A preliminary result of the small pixel image sensor array was demonstrated under uniform white light illumination, leading to the potential application of fabricating miniaturized high-detectivity image sensors.

2.2.1 Fabrication of Individual Addressable Si Nanowire Photodetector Array

The fabrication started from a p-type (100) silicon-on-insulator (SOI) wafer with a device layer thickness of 5 μm and a doping concentration of ~10^{15} cm^{-3}. Firstly, E-beam lithography was used to pattern stripes and connecting electrodes onto poly(methyl methacrylate) (PMMA) resist. Then Ni was deposited using E-beam evaporation and lift-off. The ICP/RIE process (Gases: C4F8 and SF6) was carried out to anisotropically etch Si, resulting a pattern of Si stripes in the central region and Si

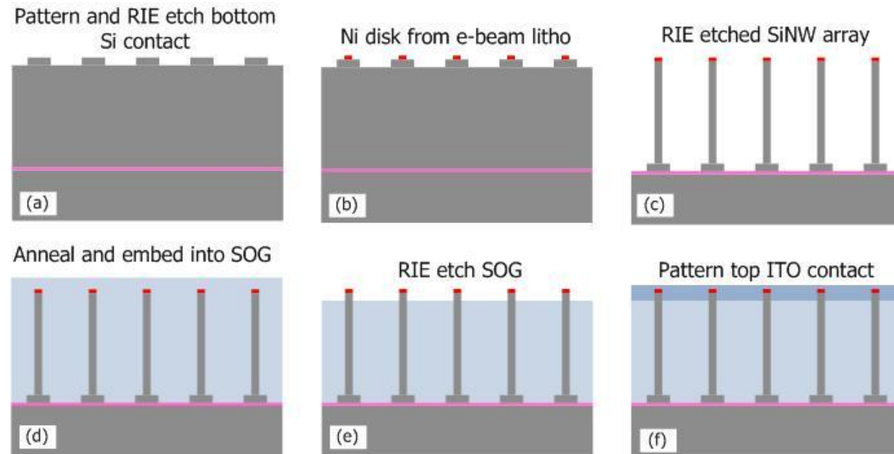


Figure 2.1: Process flow for fabrication of individually addressable vertical Si nanowire photoconductor array.

lines connecting to electrode pads in the outer region (Figure 2.1 (a)). After etching off Ni mask by Ni etchant, another E-beam lithography process with alignment was used to pattern nanoscale Ni disks onto the Si stripes (Figure 2.1 (b)). Similar to the first etching, Si was dry etched down the SiO_2 layer to create a Si nanowire array sitting on the stripes. Then the SOI substrate with Si nanowires was annealed at 650 ℃ for 60 s in forming gas (5% H_2, 95% N_2) to form nickel monosilicide (NiSi) between the Ni disks and nanowire tips to ensure an ohmic top contact. Al was patterned and evaporated onto the Si stripes and contact pads by E-beam lithography, and annealed at 400 ℃ for 60 s in N_2 to form an ohmic bottom contact. Transparent spin-on glass (SOG, Futurrex, Inc) was spin-coated to fill the spacing between nanowires as an insulating layer (Figure 2.1 (d)). Excess spin-on glass was removed using O_2 RIE etching to expose the nanowire tips (Figure 2.1(e)). A patterned layer of transparent indium tin oxide (ITO) was sputtered and lift-off to form top contact.

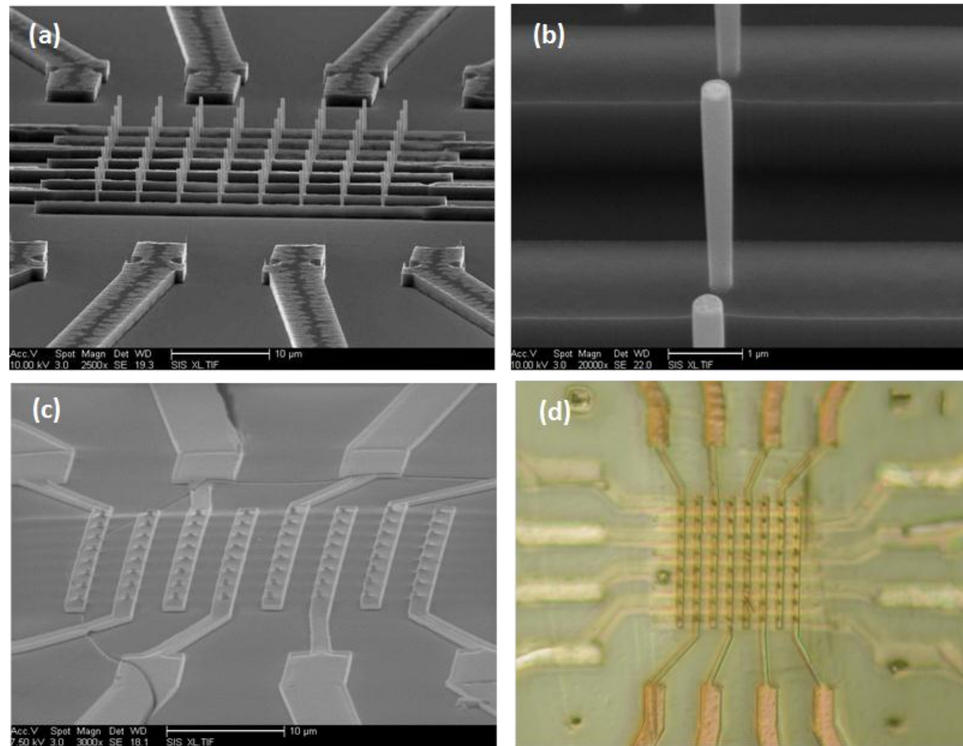


Figure 2.2: (a) A SEM image (75 ° tilted view) of Si nanowires array. (b) A magnification of SEM image (45 °tilted view) of Si nanowires. (c) A SEM image of Si nanowire photoconductor array. (d) Optical microscope image (top view) of Si nanowire photoconductor array.

The morphology of Si nanowire array was characterized by SEM and optical microscope. Figure 2.2 (a) shows a SEM image of fabricated 8×8 Si nanowire array. The diameters, length and pitch size of nanowire array are ~~200-240 nm, 3.7 μm and 4 μm, respectively. The Si nanowires sit on 1.5 μm wide and 1.3 μm thick electrically insulating Si stripes. Figure 2.2 (c) illustrates the patterned ITO electrodes on top of the Si nanowires embedded in SOG. The crossbar contact structure enables the individual addressability of Si nanowire photodetector array, as shown in Figure 2.2 (d).

2.2.2 Single Si Nanowire Photodetector Characterization

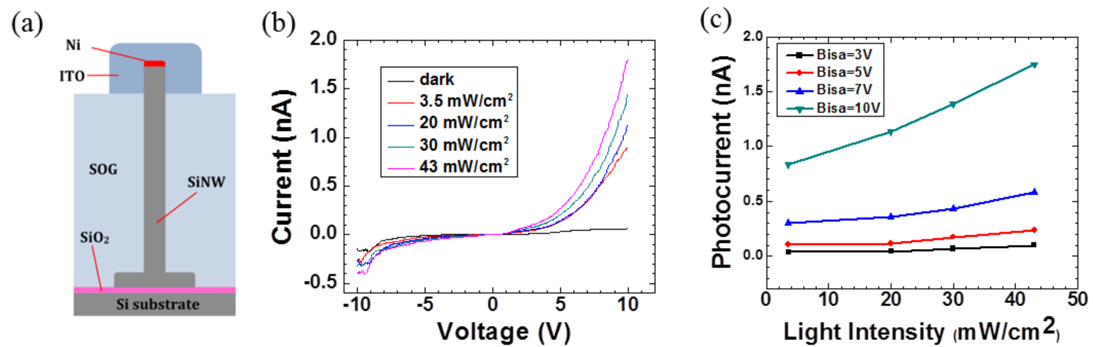


Figure 2.3: (a) Schematics of a single Si nanowire photodetector. (b) I-V curves of a representative Si nanowire device under dark and illumination with varying light intensities. (c) Curves of photocurrent as a function of incident light intensity at different applied biases.

The electrical properties of a single Si nanowire photodetector were characterized by current-voltage (I-V) measurements using a semiconductor parameter analyzer (Agilent B1500). The light source used in this experiment was a while light lamp. Figure 2.3 (a) shows typical I-V curves of a single Si nanowire device from the array under dark and varying light illumination levels at room temperature. Under dark, rectifying I-V curve was observed owing to the Schottky contact between Si and nickel silicide. Upon illuminated, the device shows very small photo response under reverse bias. When the device is forward biased, the measured current increases significantly. It shows that the current is increased by 2 orders of magnitude with a light intensity of 43 mW/cm^2 at 10 V bias. With increasing illumination light intensity, the photocurrent increases proximately linearly (Figure 2.3 (b)). The photoconduction of the Si nanowire devices mainly arise from two factors: (1) the enhancement of the

carrier lifetime caused by the trapping of carriers in the surface states; (2) decrease of the carrier transit time due to small dimension of nanowire devices.[8] Because of the high surface-to-volume ratio, surface states have been reported to play an important role in photoconductive and carrier transport behaviors for various nanostructures, such as ZnO nanowires, boron nanobelts,[72] Ge nanowires,[73] CdS nanoribbons.[22] In the case of p type Si nanowires, due to the presence of large number of dangling bonds and defects, water molecules adsorb on the nanowire surface when exposed to humid ambient.[20] The adsorption effect is especially important in etched nanowires due to the rough surface. The adsorbed molecules can trap electrons to form OH^- ions. The existence of the negative charges on the surface causes band bending. Upon illumination with photon energy higher than the band gap, electron-hole pairs are generated. The photo-generated electrons migrate to the surface and are captured by the surface traps, resulting in accumulation of excess holes in valence band inside the nanowire. The excess holes contribute to the electrical transport and induce photoconduction.

2.2.3 Integration to CMOS for Image Sensor Applications

An image sensor is a device that converts an optical image to an electrical signal. Image sensors have been widely used in cameras, camcorders, scanners, fax machine, and other camera modules. The two main Si based image sensor technologies are charge-coupled devices (CCDs) and CMOS image sensors. A CCD

image sensor is an analog device, which converts the incident light into small electrical charge in each photo sensor. The charges are subsequently converted to voltage one pixel at a time as they are read from the chip. CCD is a more mature technology. Ever since it was first reported by Bell lab in 1970, significant research advances have been achieved on CCD image sensors, leading to a very high level of performance with low readout noise, high dynamic range and excellent responsivity. However, CCD based camera system requires not only one image sensor chip but also a set of ancillary chips, such as signal processors and analog-to-digital converters, which greatly increases the fabrication cost, power consumption and hampers miniaturization of cameras. On the other hand, the CMOS imaging chip is a type of active pixel sensor made using the CMOS semiconductor process, which offers lower fabrication cost, lower power consumption, high miniaturization and increased functionality.

However, miniaturization of CMOS technology does not always lead to enhanced image sensor performance. The main obstacles of the conventional CMOS image sensor systems are the poor scalability and low responsivity of the photodetector.[74] To overcome the limitations of conventional devices and meet the need for scaling down, high-sensitive nanoscale photodetectors are highly desirable. Semiconductor nanowire photodetector, which promises high responsivity and small size, is an attractive candidate for applications in integration with CMOS image

sensors. Recently, extensive research efforts have been devoted to develop large-area nanowire based image sensing devices.[75-77]

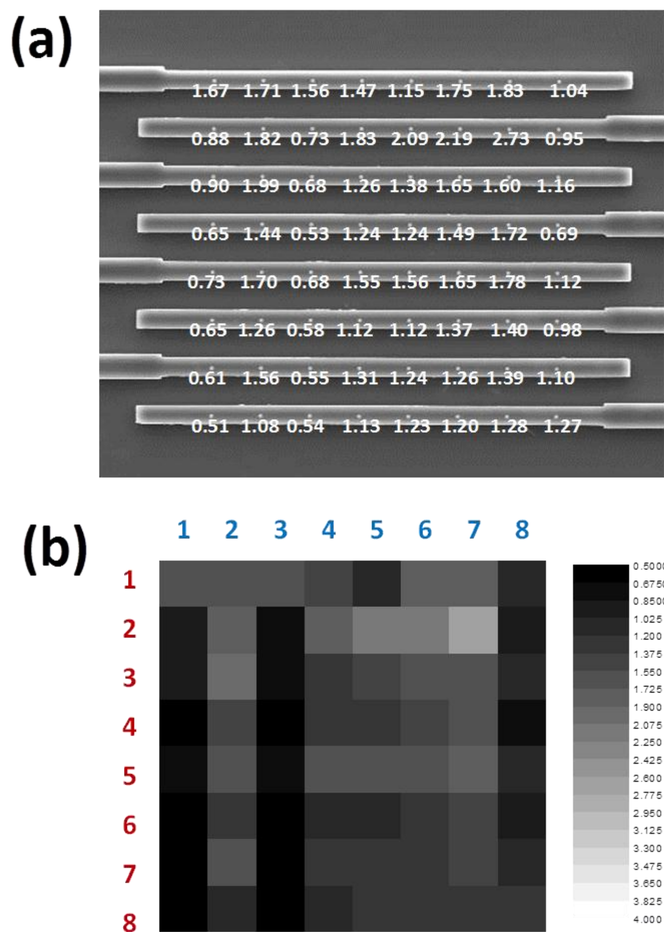


Figure 2.4: (a) Measured photocurrents of each Si nanowire photodetector in the array. The SEM image is a top view of Si stripes with Ni dots on top. The array is illuminated by a uniform white light lamp (3.5mW/cm^2). (b) A simple demonstration of the response of the photodetector array as an image sensor to uniform white light illumination with each device representing one pixel. The contrast map corresponds to the photocurrent map.

To demonstrate the concept that the vertical Si nanowire photodetector array can function as an image sensor, the photocurrent (the current with illumination

subtracts dark current) of the individual nanowire photodetector in the 8×8 Si nanowire array was measured under uniform white light illumination with a power density of 3.5 mW/cm^2. Figure 2.4 (a) shows the mapping of measured photocurrents. The results show 100% yield functional nanowire devices and a nonuniform distribution of photocurrents (I_{ph0}), ranging from 0.53 nA to 2.73 nA (see Figure 2.4 (a)). A 2D contrast map of the photocurrent was plotted considering each nanowire device as a pixel (see Figure 2.4 (b)). The map shows relative small spatial variation of the light intensity, which is consistent with the uniform illumination. To further enhance the device uniformity, the relative intensity, which is defined as measured current of imaging an object divided by photocurrent with uniform illumination, can be used to plot contrast map. Thus, potential application as functional, small pixel and high resolution image sensor of the Si nanowire photodetector array has been demonstrated.

2.3 Axial P-N Junction Si Nanowire Photodetectors

2.3.1 Device Fabrication

The fabrication process of Si axial p-n junction nanowire photodiode array is illustrated in Figure 2.5. The substrates used in this study were p-type Si (100) wafers with a boron doping concentration of 1×15 cm^{-3}. Firstly, the Si surface was inverted to form an n-type top layer via phosphorus diffusion using spin-on-dopant (SOD) (Figure

2.5 (a)). The junction depth was found to be ~1.6 μm using ICP/RIE etch and four point probe method. Secondly, nanoimprint lithography and ICP/RIE etching were used to pattern the Si substrates and fabricate large-area Si nanowire arrays. Ni dots array with an area of 2×2 cm^2 was patterned on Si wafers as the etch mask by nanoimprint lithography (Figure 2.5 (b)), followed by evaporation of 40 nm thick Ni and lift-off processes. Thirdly, the vertically aligned Si nanowires with an axial p-n

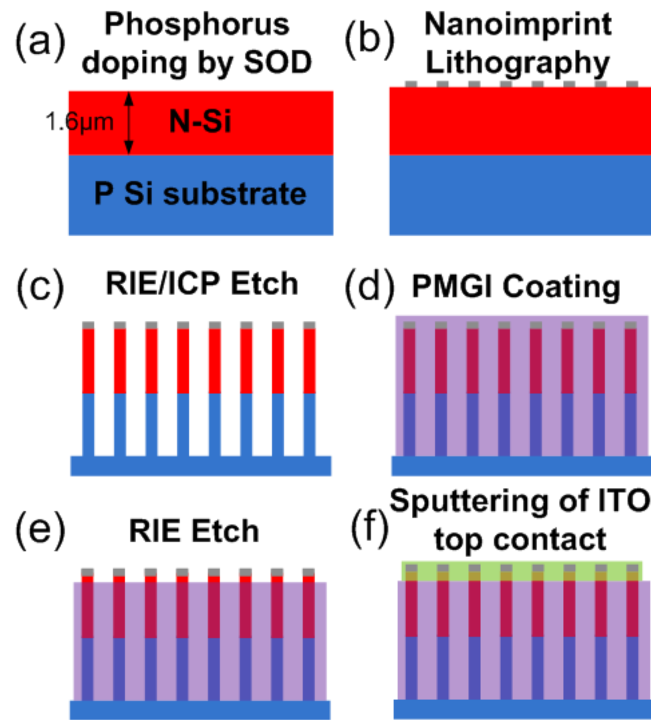


Figure 2.5: Schematics of fabrication process of Si axial p-n junction photodetectors. (a) Phosphorus diffusion of Si wafers using spin-on dopant to form a planar p-n junction. (b) Nanoimprint lithography and E-beam evaporation to pattern Ni dots array on Si wafers. (c) ICP/RIE dry etch of Si nanowire array. (d) Spin-coating of PMGI polymer as an insulating filling material. (e) Removal of excess PGMI by O_2 RIE to expose nanowire tips. (f) Sputtering of ITO as transparent top contact.

junction were created by ICP/RIE process with C_4F_8 and SF_6 gases (Figure 2.5 (c)). Upon a rapid thermal annealing process at 650 ℃ for 60 s in N_2, a NiSi layer was formed on top of Si nanowires to ensure a good electrical contact. Subsequently, the Si nanowire array was embedded in a poly(methylglutarimide) (PMGI, Microchem) insulating layer by spin-coating (Figure 2.5 (d)). The tips of Si nanowires were then exposed by removing excess PMGI with O_2 RIE etching. Finally, 300 nm transparent indium tin oxide (ITO) was sputtered as a top electrode to the nanowires (Figure 2.5 (f)); and a layer of indium was formed on the backside of the substrates as back electrode using soldering iron.

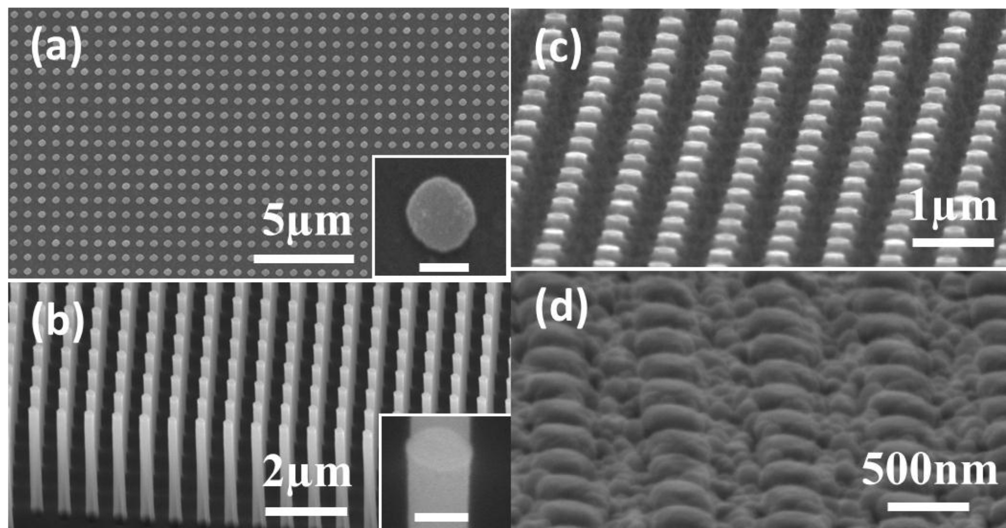


Figure 2.6: (a) SEM images of Ni dot array patterned by nanoimprint lithography. Inset shows magnified image of a Ni dot. Scale bar is 200 nm in the inset. (b) SEM images of vertical Si nanowire array at 45^0 tilted view. Nanowire length ~ 4 µm and scale bar in the inset is 200 nm. (c) A SEM image of Si nanowires embedded in PMGI with expose nanowire tips at 45^0 tilted view. (d) A SEM image of Si nanowire device with sputtered ITO top contact at 45^0 tilted view.

The nanoimprint lithography allows a high-throughput fabrication of large-area nanowire arrays with precise control of position and diameter in a cost-effective way. As shown in Figure 2.6 (a), SEM characterization indicates a uniform, well-ordered, nearly defect-free array of Ni dots with diameters of ~ 200-250 nm. Figure 2.6 (b) illustrates the as-etched Si nanowire array. The Si nanowire array is 600 nm in pitch size and 4 μm in length. The nanowire length can be easily turned by varying etching time. Figures 2.6 (c) shows the Si nanowire array embedded in PMGI, with an exposed length of ~200 nm. A good coverage of ITO on top of Si nanowires was reached as top electrode with a thickness of 300 nm, as shown in Figure 2.6 (d).

2.3.2 Device Characterization

I-V characteristics were investigated at room temperature under dark and with illumination on top of the device using a semiconductor device analyzer. Under dark, a clearly rectifying I-V curve was observed (inset of Figure 2.7 (b)), with a rectification ratio of 151 at ±1 V, implying a successful doping of p-n diode using SOD. At zero voltage bias, the dark current density is smaller than 0.16 $\mu A/cm^2$. Upon illuminated with a white light source (xenon lamp, 100 mW/cm^2), the current density suddenly increases to 4.04 mA/cm^2. The photosensitivity, which is defined as $(I_{photo}-I_{dark})/I_{dark}$,[78] is calculated to be 2.5×10^5 under zero bias. This high photosensitivity is attributed to the superior light absorption of nanowire structure.

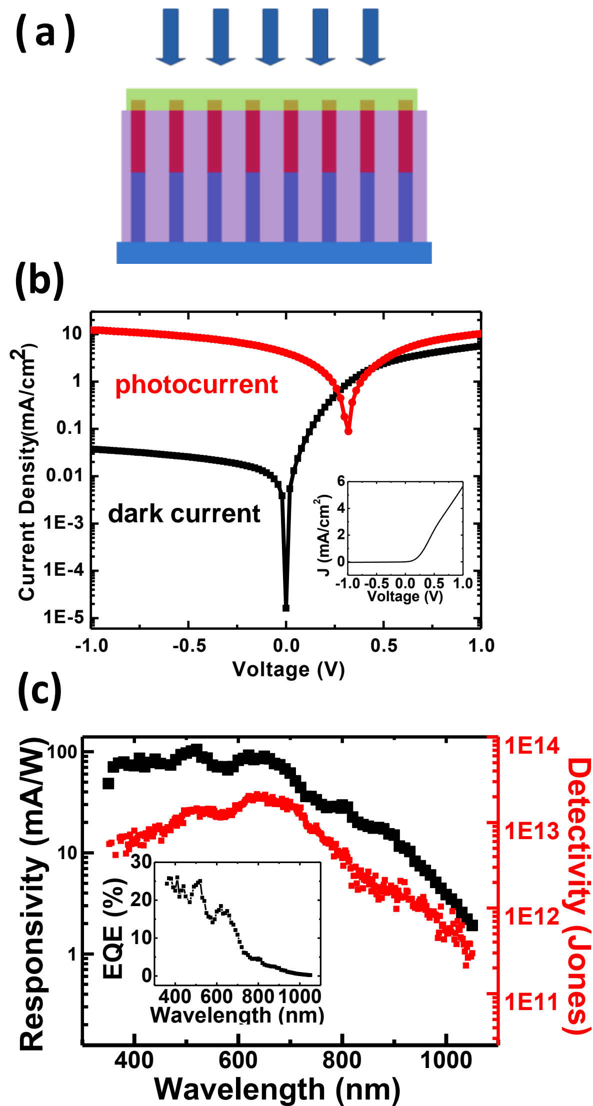


Figure 2.7: (a) Schematic of a Si axial junction nanowire photodiode. (b) Semi-log I-V curves of a typical photodiode under dark and with white light illumination (100 mW/cm^2). Inset is the I-V curve under dark in linear scale. (c) Spectra photoresponsivity and specific detectivity of the photodiode under zero bias. Inset is the corresponding external quantum efficiency.

To further investigate the photo response properties of the Si nanowire photodetector, the room temperature spectra response was measured using a monochromator (Horiba Jobin Yvon iHR-550). A 100 W halogen lamp was used as

the light source to measure spectra response. The monochromator tuned white light emitted by the halogen lamp into monochromatic light and the beam was focused onto the device surface. The photocurrent was measured by a commercial Si p-i-n photodiode (Newport, Si-818UV) connected to a lock-in amplifier (Stanford Research SR520). The responsivity of Si nanowire photodiodes was calculated based on the equation below,

$$R_{\lambda}= I_{ph}/P_{inc} =R_{\lambda pin}I_{ph}/I_{pin},$$

where R_{λ} and $R_{\lambda pin}$ are responsivities of Si nanowire devices and the commercial Si p-i-n device, respectively; I_{ph} is the measured current density of Si nanowire device and I_{pin} is that of Si p-i-n photodiode; P_{inc} is incident light power. Accordingly, the external quantum efficiency (EQE) can be obtained from responsivity (R_{λ} in A/W) using,

$$EQE=(R_{\lambda}/\lambda)\times(hc/e)\approx (R_{\lambda}/\lambda) \times(1240W\cdot nm/A),$$

where λ is the wavelength in nm, h is the Planck constant, c is the speed of light in vacuum, and e is the elementary charge. Thus, the responsivity and EQE of the Si nanowire photodetector were measured without external power supply. In the visible wavelengths ranging from 350 nm to 680 nm, as presented in Figure 2.7 (c), the Si nanowire photodetector exhibits a quite constant responsivity of around 70-105 mA/W. When wavelength is above 680 nm, responsivity starts to decrease gradually. The peak

responsivity occurs at λ=520 nm, with a value of 105 mA/W. Accordingly, the EQE is calculated to be 25% electron per photon.

The noise equivalent power (NEP), which is the minimum incident light power that a detector can distinguish from the noise, is an important figure of merit for evaluation of photodetector performance. The NEP can be given by

$$NEP=(A\Delta f)^{1/2}/D^*,$$

where A is the effective area of the detector in cm^2, Δf is the electrical bandwidth in Hz, and D* is the specific detectivity measured in Jones (cm $Hz^{1/2}$/W). The specific detectivity is another important photodetector figure of merit that is independent of the measurement system. Thus, the specific detectivity can be expressed as

$$D^*=(A\Delta f)^{1/2}/NEP= R(A\Delta f)^{1/2}/I_n,$$

where I_n is the noise current in A and R is the responsivity in A/W. There are three kinds of noise limiting D*: shot noise from dark current, Johnson noise, and flicker noise from thermal fluctuation.[79, 80] Assuming the detectivity is limited by the shot noise from dark current, it can be written as

$$D^*=R/(2qJ_d)^{1/2},$$

where J_d is the dark current density. Thus, the specific detectivity in the spectrum from 350-1050 nm can be calculated based on the measured spectra responsivity and dark current. At zero bias, the specific detectivity of Si axial junction nanowire photodiode as a function of wavelength is illustrated in Figure 2.7 (c). The device shows optimal

specific detectivities in the visible range, with a value greater than 5×10^{12} Jones across the entire visible spectrum (380-750 nm). And it reaches a maximum of 2.14×10^{13} Jones at 636 nm wavelength. For comparison, the commercial Si photodiode (Newport, Si-818UV) has a specific detectivity typically around 2.22×10^{12} Jones in visible spectrum. From the above equation, we can see that it requires not only high responsivity but also low dark current to achieve high detectivity. This photodetector achieves excellent detectivity owing to its low dark current, although it exhibits a lower responsivity than the commercial Si photodiode. This observation reveals an excellent ability of the Si nanowire axial p-n junction photodetector to distinguish signal from noise.

2.4 Radial Junction Si Nanowire Photodetectors

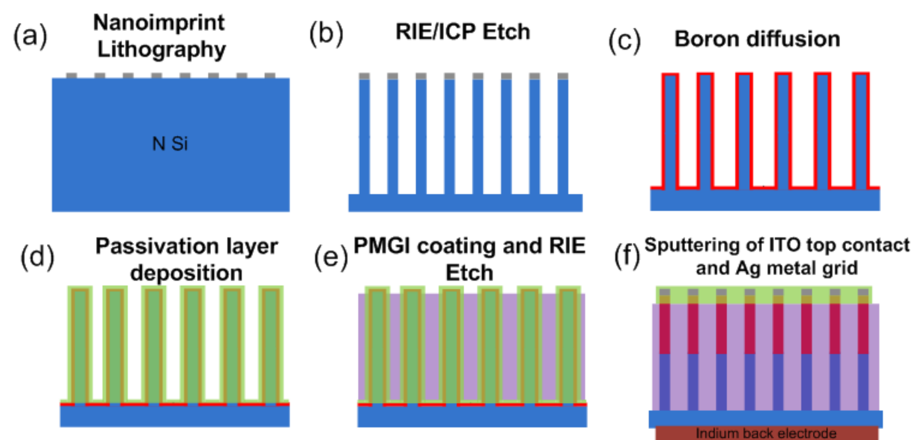


Figure 2.8: Fabrication Process of Si radial junction nanowire photodiodes.

Radial junction nanowire, consisting of an n-type core and a p-type shell or the

vice versa, is an attractive structure for photodetection. The large difference of work functions between core and shell creates a build-in potential along the radial direction of nanowire. When the nanowire absorbs a photon with energy higher than the band gap of the material, an electron-hole pair is generated. The internal electric field caused by the build-in potential in the depletion region near the junction propels the electrons and holes in opposite directions. In our case, the electrons move to the n-type core while holes migrate to the p-type shell. A photocurrent forms as the carriers are collected by the electrodes. Owing to the short carrier separation/collection length of radial junction nanowire, the carrier collection efficiency is significantly enhanced, especially for materials with small minority carrier diffusion length.

In this section, we present the fabrication and characterization of Si radial p-n junction nanowire photodiodes. The fabrication process is illustrated in Figure 2.8. The vertically aligned Si nanowire arrays were created using nanoimprint lithography and ICP/RIE etching. An array of Ni dots was patterned onto n-type Si substrate (6.5×10^{17} cm^{-3}) as etch mask and ICP/RIE process was carried out to etch Si nanowires. The diameter, length and pitch size of the nanowire array is ~200 nm, 4 μm and 1 μm, respectively. After etching off the Ni mask, the Si sample was cut into ~ 8 mm × 8 mm pieces. The radial p-n junction was formed by boron diffusion (pre-deposition at 800 ℃ for 10 s; drive-in at 800 ℃ for 3 hours) using boron spin-on dopant (SOD, B155, Filmtronics) as the dopant source. The SOD diffusion process

will be discussed in details in Section 3.3.2. Subsequently, a layer of Al_2O_3 was deposited onto the surface of Si nanowires to passivate the surface states. Following surface passivation, the Si nanowire array was embedded in transparent Polymethylglutarimide (PMGI) polymer. Oxygen RIE was employed to remove excess polymer to expose the nanowire tips. The Al_2O_3 on the nanowire tips was removed by BOE etching, followed by sputtering of ITO as front contact. Then Ag grid front electrode was patterned using photolithography and lift-off. ITO layer was annealed at 300 ℃ for 1 min on a hotplate to improve the conductivity and transmittance. Indium was soldered on the backside of Si substrates as ohmic back electrode.

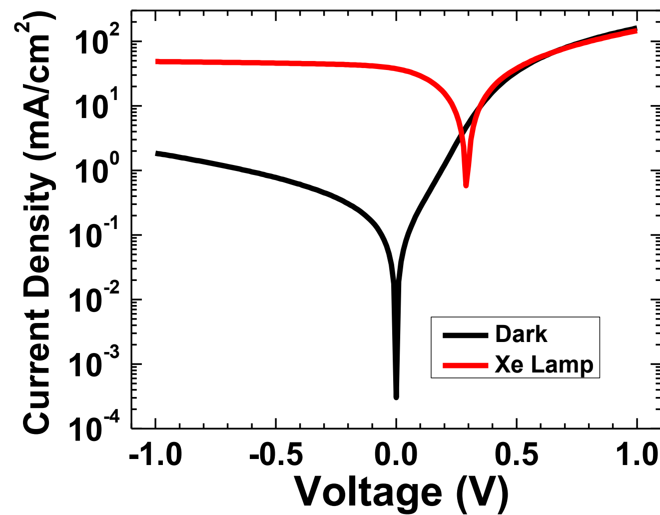


Figure 2.9: Representative I-V curves of the Si radial junction nanowire photodiode measured under dark and illumination with a white light source (Xe arc lamp, 100 mW/cm^2).

The Si radial junction nanowire photodiode was characterized using I-V measurements under dark and illumination with a xenon arch lamp (100 mW/cm^2), and the results are shown in Figure 2.9. The device shows a high photosensitivity of 1.24×10^6 at zero bias to white light illumination, which is 5 times higher than that of the Si axial junction nanowire photodiode. The remarkable enhancement of the photosensitivity is due to the shorter carrier collection path of radial junction nanowire structure. Furthermore, the spectral responsivity of the radial junction nanowire device was characterized at zero bias, as shown in Figure 2.10. Comparing the Si axial junction device, the radial junction device shows higher responsivity over the measured wavelengths ranging from 350 nm to 1100 nm, as a result of the improved carrier collection. The peak responsivity of the device is 235 mA/W at 672 nm wavelength.

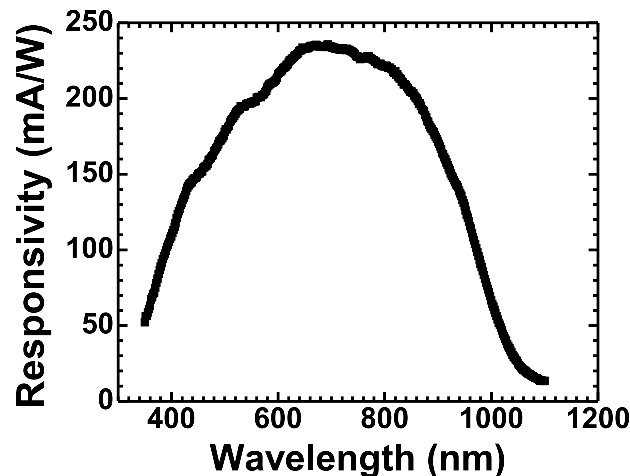


Figure 2.10: Spectra responsivity of Si radial junction nanowire with Al_2O_3 passivation.

2.5 Integration with Nanowire Solar Cell and Self-powered System

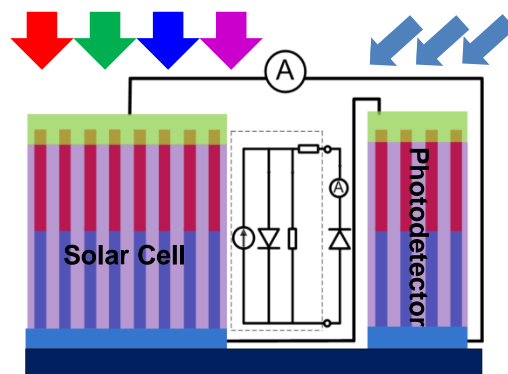


Figure 2.11: Illustration of the Si axial junction nanowire photodetector driven by a Si axial junction nanowire solar cell and the equivalent circuit.

Currently, most of the highly sensitive photodetectors require an external power source, which limits the mobility and independence of the system owing to increased size and weight. The self-powered photodetector, which could operate without external bias, is highly desirable for medical applications. In the preceding sections, we have shown that the Si nanowire photodiodes exhibited high photo responsivity and detectivity at visible wavelengths under zero bias. To further demonstrate the self-powered properties of the Si nanowire axial p-n junction photodiode, two identical Si axial p-n junction nanowire arrays were integrated together: one served as a photodetector and the other as a solar cell to drive the photodetector. Fabrication of the solar cell went through similar processes as illustrated in Figure 2.5, except that a layer of Ag grid electrode was deposited on top of ITO contact to improve the solar cell performance. Figure 2.11 illustrates the schematics of the integrated devices and the equivalent circuitry.

The Si axial junction nanowire solar cell was first characterized using I-V measurements. A representative I-V curve of the device with AM 1.5G illumination (100 mW/cm^2) is illustrated in Figure 2.12. The solar cell exhibits a short-circuit current density of 4.92 mA/cm^2, an open circuit voltage of 0.21 V, a power conversion efficiency of 1.2% and a maximum output power of 0.275 mW/cm^2. Then the spectral photo responsivity of the Si nanowire photodetector driven by the Si nanowire solar cell was measured. As illustrated in Figure 2.12, the solar cell was impinged with AM

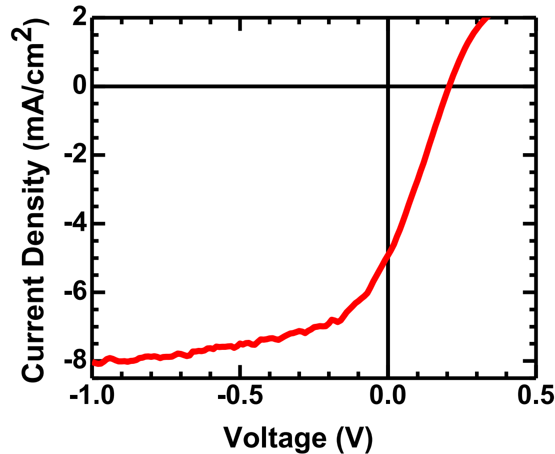


Figure 2.12: I-V curve of a representative Si nanowire axial p-n junction solar cell measured with AM 1.5G illumination (100 mW/cm^2).

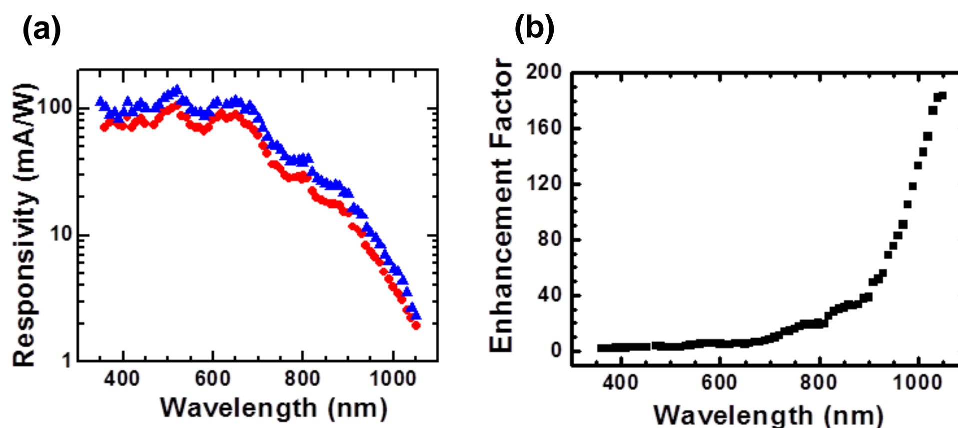


Figure 2.13: (a) Spectra responsivity of the nanowire photodetector driven by a nanowire solar cell (▲). The (●) curve is the responsivity at zero voltage bias for comparison. (b) Enhancement factor of the responsivity, which is defined as the ratio of responsivity of the nanowire photodetector driven by a nanowire solar cell to that under zero bias.

1.5G illumination while the photodetector was illuminated with monochromatic light from the monochromator. As seen in Figure 2.13 (a), there is a significant enhancement of responsivity when the Si nanowire photodetector is driven by the Si nanowire solar cell, compared to that without bias. Figure 2.13 (b) shows the enhancement factor of photo responsivity (i.e. the ratio of responsivity of the nanowire photodetector driven by the nanowire solar cell to that at zero voltage bias) as a function of wavelength. The enhancement factor increases monotonically with the wavelengths. At visible wavelengths, the enhancement factor is in the range of 2 to 19. In the IR region, the enhancement factor increases more rapidly, reaching a value of 183 at a wavelength of 1050 nm.

2.6 Si Nanowire Photodetectors for Retinal Prosthesis

Si photodetectors have been attracting extensive research for imaging applications in the visible and near-infrared wavelengths, such as image sensor and artificial Si retinal prosthesis. Especially, through implantation of a Si photodetector array between the inner and outer retina layers, the optical signals can be converted into electrical signals. Consequently, the inner retinal neurons are electrically stimulated to elicit visual sensation known as phosphenes in healthy subjects[81-83] and patients suffering from retinal degenerative diseases such as retinitis pigmentosa[84] and age-related macular degeneration.[85] Therefore, it provides an alternative route to improve vision or even restore sight for the blinds by replacing the dysfunctional photoreceptors in retina with Si photodetectors.[86, 87] However, most highly sensitive photodetectors require external power sources delivered, for example, via cable connection[88, 89] or inductive radio frequency coils,[90] which greatly increase the system size and require complex surgical methods. The bulky photodetector system makes the implantation surgery more complex and increases the possibility of undesirable side effects.[89] Thus, it is highly desirable to develop a self-powered visible photodetector without the need of external power supply. This will greatly enhance the adaptability and mobility of the devices. Recently, research efforts have been devoted the study self-powered devices based on photoelectrochemical cells,[91] microbial fuel cells,[92] piezoelectric nanowire-based nanogenerators[93-95] and photovoltaic cells.[96] The

self-powered photodetectors based on photoelectrochemical and microbial fuel cells are bulky and incompatible with retinal prosthesis. Nanogenerators, which harvest mechanical energy and convert it into electrical energy, rely on the piezoelectric potential created in ZnO nanowires by an external strain.[95] It requires mechanical bending and/or deformation for energy generation in nanogenerators;[97] thus makes it unfeasible for retinal prosthesis. In contrast, photovoltaic cells are photodetectors that can be driven by the photo voltage generated from absorption of incident light and operate as photodetectors without external power source simultaneously. As discussed in the preceding sections, the Si axial junction nanowire photodiode have high photosensitivity under zero bias. By integrating with an identical nanowire array which served as a solar cell, the photo response of the photodetector can be further enhanced. The self-powered properties of Si nanowire photodiodes makes them perfect candidates for retinal prosthesis.

In order to achieve restoration of useful vision by retinal implantation, fabrication of high-resolution, high-responsivity and fast response visible photodetector arrays is critical. The human eye has about 100 millions of photoreceptors. Zrenner *et al* have demonstrated restoration of vision with a visual acuity up to 20/1000 by subretinal implant of an array containing 1500 active microphotodiodes with pixel size of 72×72 μm, each consisting of a photodiode, its own amplifier and local stimulation electrode.[88] It is an important proof of concept,

but the visual acuity is low due to the insufficient active pixels. It is vital to scale down the pixel size in order to integrate a large number (i.e. 1.2×10^5 pixels required to obtain 20/40 visual acuity for 10 field of view with 10 μm pixel size) of active pixels in a small area (a few mm^2). The pixel size of conventional CMOS image sensors is limited by the non-photosensitive regions, including electronic transistors and optically active element, which typically reduce the fill factor to 30%.[98] On the contrary, due to the reduced dimensionality, semiconductor nanowires are ideal candidates to realize high-resolution photodetector arrays with small pixel size. In addition, semiconductor nanowires exhibit superior optical and electrical properties for photodetection owing to their unique one dimensional structure and large surface-to-volume ratio, such as enhanced optical absorption from light trapping[35, 38] and shorter path length for carrier transport.

Figure 2.14 illustrates the mechanism of semiconductor photodiodes function as photoreceptors. In a healthy retina, the photoreceptors capture incident light and generate an electrical signal, which is transmitted through bipolar cells to the retinal ganglion cells.[99] Then the ganglion cells with axonal extensions transmit the signal all the way to the visual cortex of brain. The function of the degenerated photoreceptors can be replaced by subretinal implantation of Si nanowire photodiode arrays. When photons with energy higher than the Si band gap impinge on the Si nanowire surface, the electron-hole pairs are generated in the depletion region and separated by the

built-in electric field. The generated electric current is then transferred to the neuronal network in the retina to electrically stimulate bipolar cells.

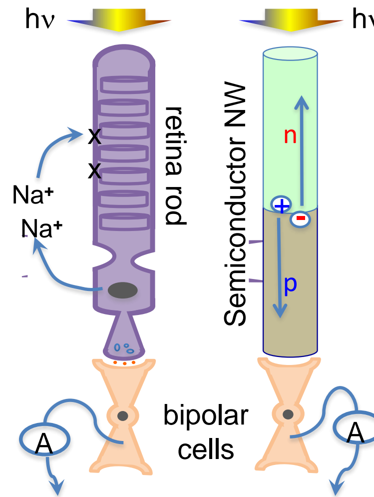


Figure 2.14: Illustration of a Si axial p-n junction nanowire photodetector served as photoreceptor to generate charges for retinal neuron stimulation.

Electrical stimulation of neurons requires sufficiently large current. The minimum charge required to stimulate retina neurons is 1 μC, delivered over 5 ms with a charge density of 1 μC/cm^2. To determine the charge density delivered by Si nanowire photodetector, time-resolved photocurrent measurements were carried out without external bias. A white light source (xenon-arc lamp) with 100 mW/cm^2 intensity was used to illuminate the Si nanowire photodetector array, while a mechanical chopper working at 1000 Hz was employed to create light pulses. As calculated from Figure 2.15, the Si nanowire axial p-n junction photodiode was capable of delivering a charge density of 0.42 μC/cm^2, which was very close to the required charge density for neuron stimulation.

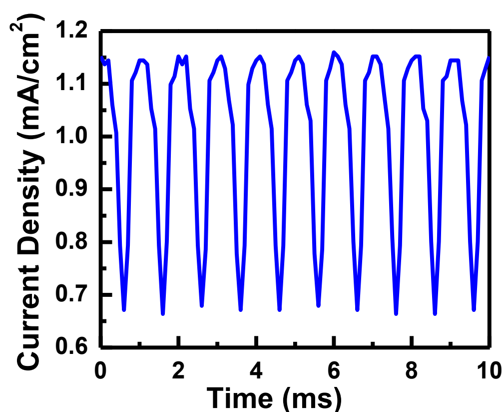


Figure 2.15: Time-resolved photocurrent measured by switching white light illumination at a frequency of 1000 Hz.

In addition, the Si nanowire photodetectors exhibited fast photo response time. From the time-resolved response curve of photocurrent with switching illumination (Figure 2.15), we obtained a response time of <0.5 ms. In comparison, the response time of retinal photoreceptors (rods and cones) is in the range of 70-120 ms depending on the background illumination.[100] This demonstrates that photo response of the Si nanowire photodetectors is sufficiently fast to replace the function of photoreceptors.

2.7 Conclusion

In conclusion, we have demonstrated Si nanowire based photoconductor, axial junction photodiode and radial junction photodiode. Through patterning of Si wafers using either E-beam lithography or nanoimprint lithography, followed by ICP/RIE dry etch, vertical Si nanowire arrays are fabricated. Using a crossbar electrode structure, individually addressable photoconductor array is achieved, showing potential

application in small pixel image sensors. In addition, a self-powered, visible photodetectors based on vertically aligned Si axial p-n junction nanowire array is also demonstrated. Without external power supply, the nanowire photodetectors exhibit high detectivities (>5×10^{12} Jones) at visible spectrum, with a peak detectivity of 2.14×10^{13} Jones at wavelength of 636 nm. Furthermore, the Si nanowire photodetector array shows enhanced responsivity when powered by another Si nanowire array which serves as a solar cell. Measurements of time-resolved photocurrent generation with illumination toggling between "on" and "off" revealed the charges delivered by the Si nanowire photodetectors is close to the minimum charges required to stimulate retina neurons, which makes it a promising candidate for applications in retinal prosthesis. Furthermore, the photo responsivity of Si nanowire photodiode can be improved by using a radial junction structure, which shortens the separation and transport distances of photo-generated carriers and enhance the carrier collection efficiency.

Chapter 2, in part, has been submitted for publication of the material as it may appear in Nano Letters 2013. Yi Jing, Huisu Jeong, Ke Sun, Muchuan Yang, Gun Young Jung, and Deli Wang, "High-detectivity vertical Si nanowire artificial photoreceptors for retinal prosthesis applications". The dissertation author was the primary investigator and author of this paper.

Chapter 3: Si Nanowires for Photovoltaic Applications

3.1 Introduction

Solar energy conversion is one of the most attractive process for applications in clean and renewable energy, since it promises an abundant, almost zero carbon-emission power source.[101] In recently years, the production of solar cell units has seen double-digit growth. Today, single- and multi-crystalline Si solar cells still dominate the commercial photovoltaic (PV) market. However, because of high production cost, solar electricity from PVs still cannot compete with fossil-derived electricity. Thus, the need for high-efficiency solar cells at low production cost is critical.

Crystal Si is an attractive material for photovoltaic application because of its natural abundance, favorable band gap and compatibility with current semiconductor wafer manufacturing technology. However, As an indirect band gap semiconductor material, the absorption coefficient of Si is low, especially at long wavelengths.[102] To absorb fully incident sunlight, 100 μm of Si is required, which is much larger than collection length (limited by the minority carrier diffusion length). Although increase of Si thickness improves the light absorption, it does not necessarily enhance the device performance because the minority carriers generated at the point more than one

diffusion length away from the p-n junction space charge region have an extremely low possibility to be collected due to recombination.[103, 104]

The 1D nanowire structure provides potential advantages over planar wafer-based or thin-film solar cells. Si nanowire based solar cells have been attracting extensive research interests in recently years. A ~24% ultimate efficiency limit of vertical Si nanowire arrays has been proposed by Lin *et al* using transfer matrix method, which is 72.4% higher than a thin film device with the same height (2.33 μm).[105] Solar cells has been demonstrated experimentally to have efficiencies as high as 9.31% on Si nanowire arrays[51] and 7.9-11% on Si microwire arrays.[106, 107] In order to realize higher efficiency devices, it requires substantial research efforts on the design and optimization of optical and electrical properties of Si nanowires. Herein, from design point of view, I present a thorough discussion on the impacts of device structures and parameters on the device performance, providing a guidance to achieve high-efficiency Si nanowire based solar cells.

3.2 Planar Si Solar Cells with Si Nanowire Light Absorber

3.2.1 Introduction

In chapter 1, I have discussed that the nanowire structure exhibit enhanced light absorption due to light trapping effects[35, 37, 38, 105, 108] which dramatically reduce the portions of reflected and transmitted photons. In the section, I present a Si planar

solar cell with vertical nanowires as light absorber. The device was fabricated using a low-cost wet chemical etching method and the photovoltaic cell was characterized using I-V measurements.

3.2.2 Solution Etching of Si Nanowires

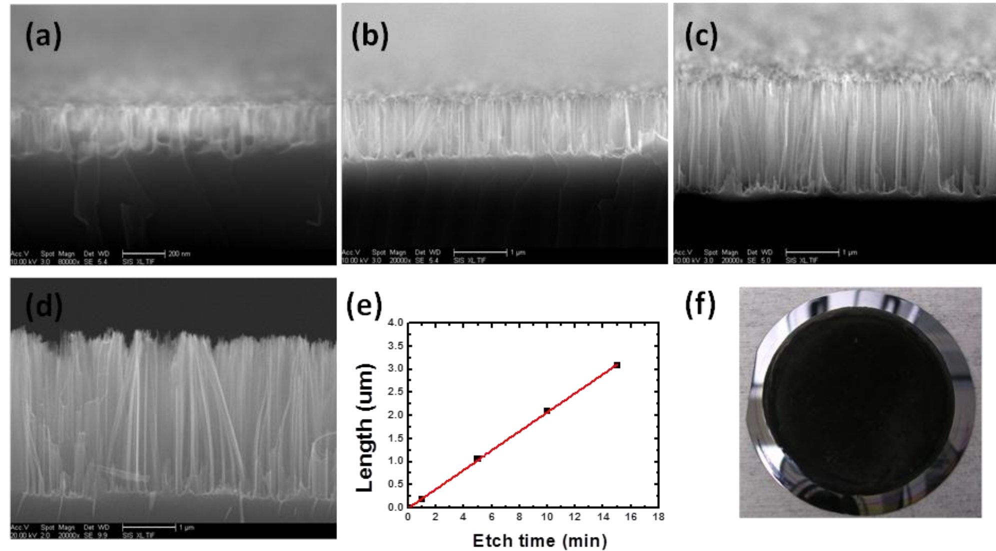


Figure 3.1: SEM images of Si wafers etched for different amounts of times (a) 1 min; (b) 5 min; (d) 10 min; (d) 15 min. (e) Plot of nanowire length vs. etch time. (f) Optical image of a large-area Si nanowire array created on a 2-inch Si wafer with 20 min etching.

Instead of conventional VLS growth or dry etch, metal-assisted chemical etching was employed to etch vertical aligned Si nanowire array with desired doping and crystalline orientation.[50] This hydrofluoric acid (HF) based aqueous solution method is simple and cost-effective. Without size limitation, multiples Si wafers can be etched together to produce wafer-scale nanowire arrays. The size of nanowire array is only limited by the size of vessels and can be scaled up as large as needed. In this

study, test-grade 2-inch n-type (100) Si wafers were used for etching of nanowires. After standard solvents cleaning and deionized water (DIW) rinsing, Si wafers were immersed into an aqueous solution of HF and silver nitrate ($AgNO_3$) with a concentration of 0.02 M and 4.6 M, respectively. The etching was performed at 50 ℃ for varying lengths of time, followed by rinsing with running DIW for 5 min immediately after removal from etching solution. The as-etched Si nanowires were usually coated with a thick layer of chemically reduced Ag, which can be removed by etching in diluted nitric acid (HNO_3, 10%). Figure 3.1 (a)-(d) illustrates a series of SEM images of Si nanowires etched for different lengths of time. As can be seen, the Si nanowires are well aligned perpendicularly to substrate surface. The length of the nanowires increases linearly with etching time, as shown in Figure 3.1 (e). A constant etching rate of ~208 nm/min was obtained by linearly fitting the curve of nanowire lengths vs. etching time. An optical image of the Si nanowire array etched for 20 min on a 2-inch wafer exhibited very dark color, in contrast with shiny gray color of the surrounding area without nanowires, indicating superior light absorption owing to the light trapping effect.

This etching method shows little dependence on the orientation or doping type of the original Si wafers. Si nanowires with desirable doping characteristics and orientation could be readily obtained. The length of nanowires can be easily tuned by varying etching time. This aqueous solution based method is a cost effective way to

synthesis large scale Si nanowires. The resulting nanowire arrays have been proven to show superior light absorption properties,[51] which is very attractive for photovoltaic applications, such as solar cells[109] and photoelectrochemical cells.[10]

3.2.3 Device Fabrication and Characterization

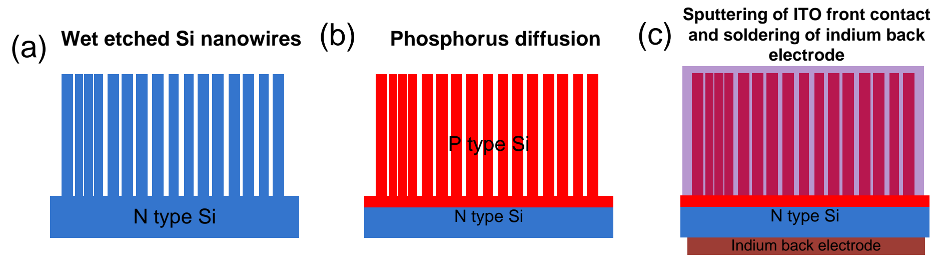


Figure 3.2: Illustration of fabrication process of planar Si solar cell with nanowire absorber.

Figure 3.2 illustrates the fabrication process of the Si nanowire based solar cell. The vertical Si nanowire array was created by metal-assisted chemical etching, followed by HNO_3 etching to remove the produced Ag film (Figure 3.2 (a)). Then the etched Si nanowire wafers were cut into ~1×1 cm^2 pieces for fabrication of solar cells. After standard RCA cleaning to remove contaminations adhering to the Si nanowires,[110, 111] boron diffusion process was carried out in a furnace using boron nitride wafer as dopant source. The diffusion was performed at 1100 ^{0}C for 15 min in N_2 to convert the nanowires into p-type as well as to form a planar p-n junction underneath the nanowire array (Figure 3.2 (b)). Afterwards, 500 nm ITO was sputtered onto the surface of the nanowires as transparent front contact and indium back electrode was formed using soldering iron (Figure 3.2 (c)). Figure 3.3 illustrates the

SEM images of nanowire device with front ITO contact. For comparison, a planar Si solar cell without nanowire absorber was also fabricated under identical conditions.

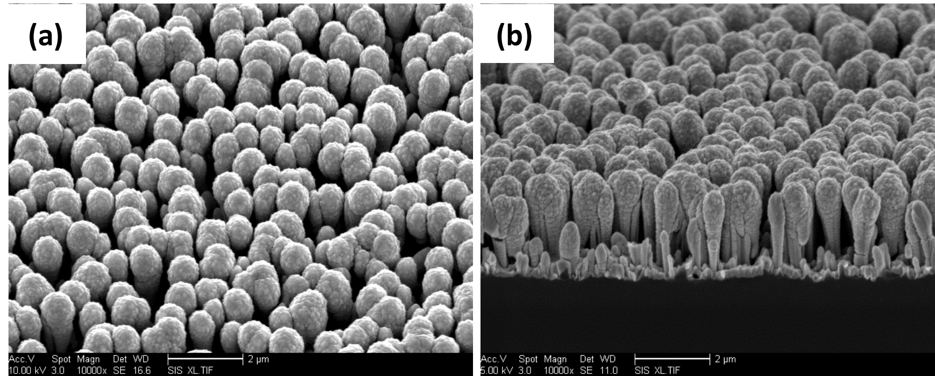


Figure 3.3: SEM images of Si nanowire based solar cell with ITO front contact at (a) 45 °tilted view, and (b) 75 °tilted view.

I-V measurements were carried out to characterize the electrical properties of the solar cells. As shown in Figure 3.4 (a), the fabricated nanowire device exhibited clearly rectifying I-V characteristics under dark, indicating successful formation of a p-n junction by boron diffusion. The operation of the solar cells was investigated under AM 1.5G (100 mW/cm^2) solar simulator illumination. Figure 3.4 (b) shows the I-V curves of the nanowire and planar Si solar cells under illumination. The photocurrent of Si nanowire based device is significantly higher than that of the Si planar device. By extracting data from I-V curves, as illustrated in Table 3.1, an open-circuit voltage (V_{oc}) of 0.51 V, a short-circuit current density (J_{sc}) of 24.4 mA/cm^2 and a power conversion efficiency (η) of 3.1% were obtained for the Si device with nanowire absorber. As a comparison, the V_{oc}, J_{sc} and η of the planar Si

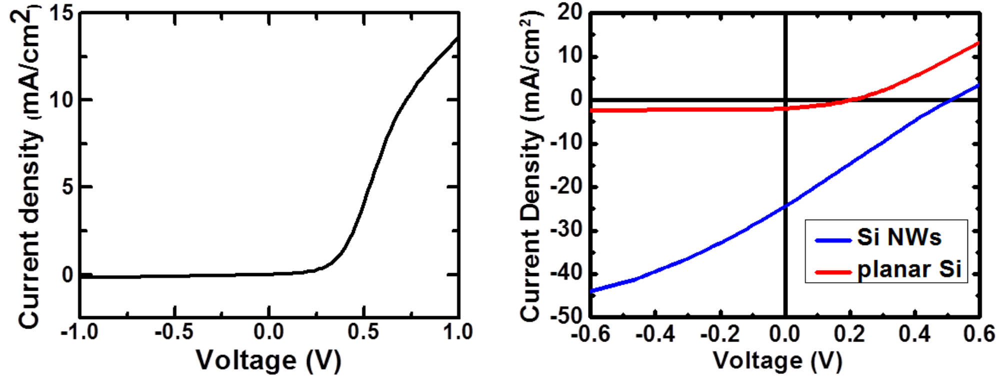


Figure 3.4: (a) I-V characteristics of a typical Si nanowire based solar cell measured under dark condition. (b) I-V characteristics of a typical Si nanowire based solar cell (blue) and a planar device (red) with AM 1.5G illumination (100 mW/cm^2).

Table 3.1: Comparison of Si solar cells with and without nanowire as light absorber.

	Planar Si device	**Si nanowire based device**
Open-Circuit Voltage (V)	**0.21**	**0.51**
Short-Circuit Current (mA/cm^2)	**1.91**	**24.4**
Power Conversion Efficiency	**0.13%**	**3.1%**
Fill Factor	**0.33**	**0.25**

without nanowires are 0.21 V, 1.92 mA/cm^2 and 0.13%, respectively. From the above results, we can see that with nanowire absorber, the device performance is dramatically improved. With nanowire absorber, the open-circuit voltage increases remarkably by a factor of two; the short-circuit current and power conversion efficiency are over one order of magnitude higher compared to the planar Si device. The dramatic improvement of device performance is attributed to the superior light

absorption of vertical nanowire array. As discussed in chapter 1, owing to the light trapping effect of nanowire array, more photons are absorbed by the nanowire device, generating more electron-hole pairs, which contribute to the photocurrent.

3.2.4 Conclusion

In conclusion, the Si planar solar cells with nanowire absorber were demonstrated. The nanowire array, prepared by a simple chemical etching method, shows superior light absorption properties; thus no antireflection coating layer is required. With nanowire absorber, the device shows a power conversion efficiency one order of magnitude higher than that without nanowires.

3.3 Si Nanowire Radial Junction Solar Cells

3.3.1 Introduction

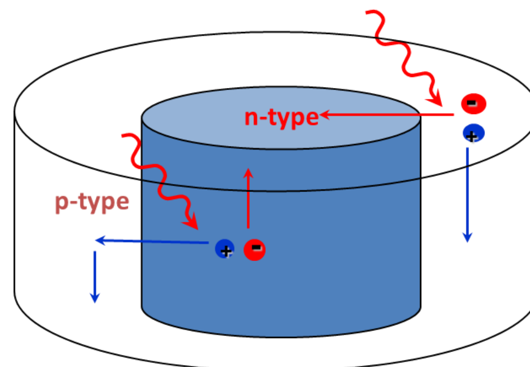


Figure 3.5: Illustration of the radial junction nanowire solar cell.

The nanowire radial p-n junction structure consists of an n-type core and a p-type shell or vice versa. The large difference of work functions between core and

shell creates a build-in potential along the radial direction of nanowire. When a photon with energy higher than the band gap of the material is absorbed by the nanowire, an electron-hole pair is generated. The internal electric field in the depletion region near the junction propels the electrons and holes in opposite directions. In our case, the electrons move to the n-type core while holes migrate to the p-type shell (Figure 3.5). A photocurrent forms as the carriers are collected by the electrodes. The photo-generated carriers which recombine before travelling to the electrodes don't contribute the photocurrent.

There are many advantages using radial junction nanowire structure for photovoltaic applications. In addition to the enhanced light absorption as discussed in Chapter 1, the radial junction nanowire structure also provides a solution to resolve the dilemma arising in the conventional solar cell configuration for materials with absorption length >collection length. By orthogonalizing the directions of light absorption and carrier collection, the carrier separation/collection lengths of radial junction nanowire structure are dramatically reduced while still maintaining long enough nanowires for light absorption. Due to the short carrier separation/collection length, the carrier collection efficiency is significantly enhanced, especially for materials with small minority carrier diffusion length. In addition, the high surface-to-volume ratio increases photoactive junction area, leading to enhanced generation of photo carriers. The reduced dimensionality of nanowire structure also

improves the carrier transport and collection, because the minority carrier diffusion length need only be comparable to the dimension of the sub-units of the nanowire device, which is typically on the order of a few tens of nanometers.

Furthermore, the Si nanowire radial junction structure also promises low-cost solar cells. A major factor of production cost of conventional Si-based solar cells is the purification and fabrication of relative pure single-crystal and polycrystalline Si from raw materials. By using radial junction nanowire structure, relative impure, therefore inexpensive materials can be used to achieve high-efficiency photovoltaics. Thus, radial junction Si nanowire array provides a promising alternative to achieve high-efficiency solar cells with low cost by using less and relative impure crystalline material because of its superior optical and optoelectronic properties.

3.3.2 Nanoscale Doping

Fabrication of nanowire radial p-n junction requires well-controlled nanoscale doping. In this study, nanoscale doping is achieved using a boron spin-on-dopant (SOD; Filmtronics B155) and the rapid thermal annealing (RTA). The radial doping profile, one of the most important parameters affecting semiconductor electronic properties, is investigated using characterization methods including I-V measurements, secondary ion mass spectrometry (SIMS) measurements and Silvaco Athena simulations.

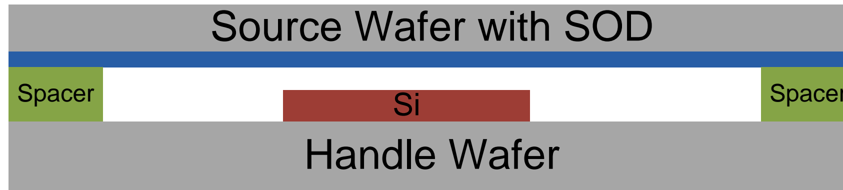


Figure 3.6: Schematic of boron diffusion using SOD in RTA.

Two diffusion techniques are used in this research: the one-step diffusion and two-step diffusion. In the one-step diffusion technique, the SOD containing boron source is spin-coated onto a dummy Si wafer as a source wafer. Then, as shown in the schematic of Figure 3.6, the Si substrate and source wafer are stacked in proximity with two spacers (~ 1 mm thick) in between each other, and transferred in a RTA furnace for heat treatment. When heated, the boron dopant evaporates from the source wafer and is transported to the surface of Si substrate. Following RTA, the Si substrate is dipped into BOE to remove any oxide formed during heat treatment. The two-step diffusion technique includes two steps: pre-deposition and drive-in. In the pre-deposition step, a constant source diffusion process is carried out in a similar way to the one-step diffusion for a short time. After removal of the source wafer, the drive-in step is performed, in which the Si substrate is annealed in a furnace for a longer time to obtain the desired doping profile.

To study the nanoscale doping, the boron diffusion process was first performed on planar n-type Si wafers with an arsenic doping concentration of 6.5×10^{17} cm^{-3}. After standard solvent cleaning of Si substrates, the SOD containing boron was

spin-coated (3000 rpm, 20 s) on dummy Si wafers as diffusion source. Before spin-coating, the SOD solution has been taken out of the refrigerator for over 6 hours to warm up to room temperature. It is necessary to have SOD at room temperature for good coating reproducibility. Unlike other types of SOD, no pre-diffusion baking is required to remove excess solvents in the boron SOD, as it would result in decomposition and evaporation of this layer. Thereafter, the Si substrates and source wafers were annealed in a RTA furnace at various temperatures (700 ℃, 780 ℃, 800 ℃, 820 ℃, 860 ℃, 900 ℃, 950 ℃, 1000 ℃) for different lengths of time (20 s, 40 s and 60 s) in N_2, followed by wet etch in BOE for removal of oxide.

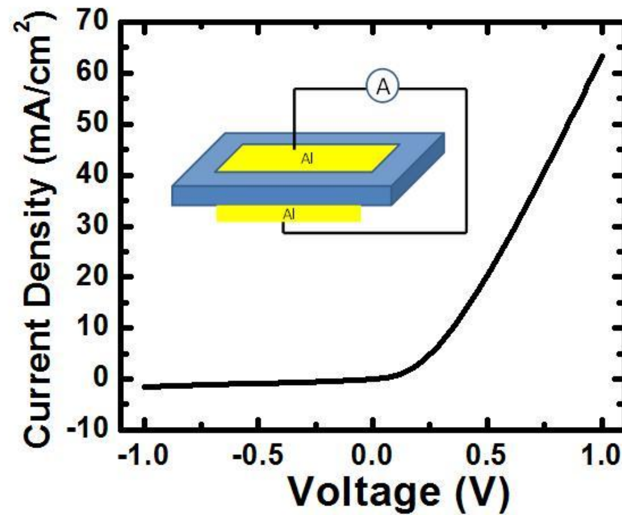


Figure 3.7: I-V curve of doped Si p-n junction. One-step diffusion was carried out at 800 ℃ for 20 s. The inset is the schematic of the p-n diode.

After diffusion process, the samples were etched in the ICP/RIE chamber to remove the doped p-type Si layer on the backside of Si substrates. Then Al was

deposited on both front and back surfaces of Si to form ohmic contacts, as illustrated in the inset of Figure 3.7. I-V characteristics of the doped Si substrates were determined by a semiconductor parameter analyzer (Agilent B1500). I-V curves of samples annealed at or above 800 ℃ exhibited clearly rectifying behavior, while those annealed below 800 ℃ showed linear I-V curves. One representative I-V curve of Si diode annealed at 800 ℃ for 20 s is shown in Figure 3.7. This result indicates that it requires annealing at elevated temperatures (800 ℃ or higher) to diffuse sufficient boron atoms into the top layer of n-type Si for conversion into p-type, thus forming a p-n diode.

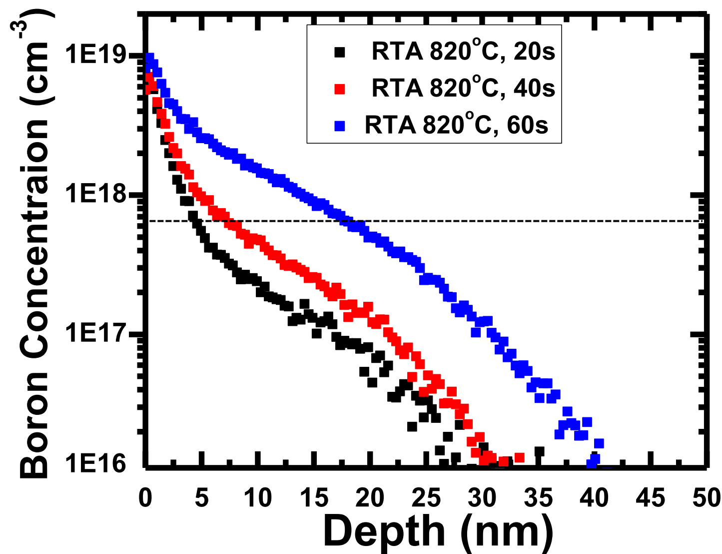


Figure 3.8: SIMS analysis of boron distribution profile in planar Si. The Si was doped using one-step diffusion at 820 ℃ for 20 s, 40 s and 60 s, respectively. The doping concentration of n-type Si wafer is 6.5×10^{17} cm^{-3}.

To investigate the doping profile of boron atoms diffused in Si, the SIMS

measurements was performed on n-type Si substrates (6.5×10^{17} cm^{-3}) annealed at 820 ℃ for 20 s, 40 s and 60 s. As exhibited in Figure 3.8, all samples show a boron doping concentration of ~1×10^{19} cm^{-3} at the surface, which sharply decreases to 6.5×10^{17} cm^{-3} at depths of 4.4 nm, 7.3 nm and 18.1 nm for 20 s, 40 s and 60 s RTA conditions, respectively. The temperature dependence of the doping profiles is attributed to the enhanced diffusivity of boron in Si at elevated temperatures. Our results indicate that boron doping profiles with nanoscale junction depths less than 5 nm can be achieved by SOD and RTA. The doping profiles can be further tuned by varying the annealing temperatures and times.

Therefore, we have successfully obtained nanoscale doping profile in planar Si wafer using SOD and RTA. To find out if this method is applicable to Si nanowires, it is necessary to determine the boron doping profile along the radial direction of Si nanowires. Due to the small size, it is difficult to perform SIMS analysis on nanowires. Thus, we used Silvaco Athena to numerically simulate boron diffusion from SOD into Si nanowires. The doped oxide diffusion model was utilized to model boron diffusion from SOD, due to their similar impurities diffusion behavior in Si.[112] The boron concentration in the doped oxide layer was chosen to be 5×10^{20} cm^{-3}.[113] Firstly, we simulated the boron diffusion in planar n-type Si with an arsenic concentration of 6.5×10^{17} cm^{-3}. We obtained a boron doping profile and determined the junction by the location of minimum net doping concentration in Si and compared to the

experimentally measured SIMS profile. The parameters (boron diffusivities in oxide and Si) in the doped oxide diffusion model were tuned to fit the simulated profiles to the measured SIMS profiles. Thereafter, we simulated the boron doping profile in Si nanowire using fitted parameters. For simulation of diffusion in Si nanowire, we considered a uniformly doped n-type cylindrical Si structure with a length of 2 μm and a radius of 100 nm. A pseudo-3D simulation was performed by taking a radial slice of the structure.

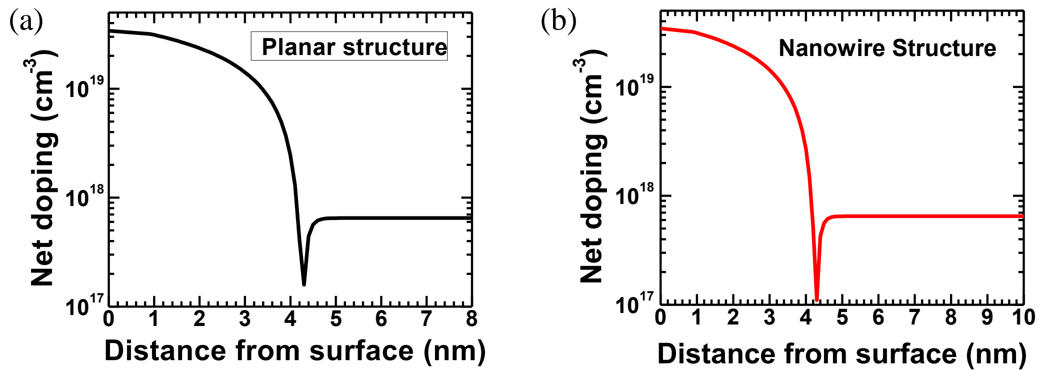


Figure 3.9: Silvaco Athena simulations of boron profiles in Si diffused at 820 ℃ for 20 s in (a) planar geometry and (b) cylindrical geometry. N-type Si with an arsenic concentration of 6.5×10^{17} cm^{-3} is considered.

Figure 3.9 shows the simulated boron doping profiles in Si planar and nanowire structures. The diffusion condition at 820 ℃ for 20 s is considered in the simulations. As illustrated in Figure 3.9 (a), the simulated doping profile in planar Si is consistent with experimentally measured SIMS profile. Particularly, the simulation result showed a junction depth of 4.3 nm and a surface doping of 3.4×10^{19} cm^{-3}, which were similar to data extracted from the SIMS profile. By comparing the simulated

profiles of planar and cylindrical structures, we only observed slightly higher average doping concentration in nanowire structure, with same values of junction depth and surface doping concentration. Thus, this result implies that a nanowire radial junction structure can be achieved using this well-controlled nanoscale doping technique.

3.3.3 Device Fabrication

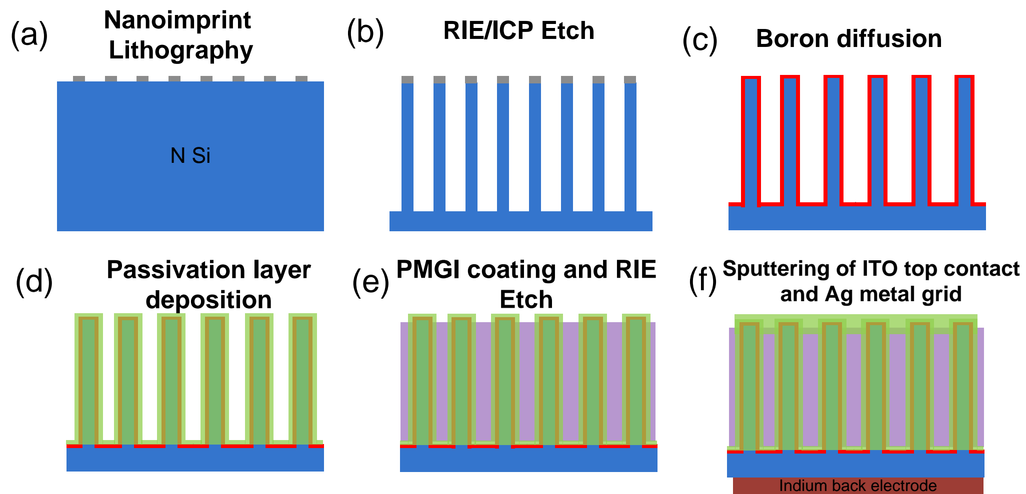


Figure 3.10: The fabrication process of Si nanowire radial junction solar cells.

The fabrication process of Si nanowire radial junction solar cells is illustrated in Figure 3.10. The large-area Si nanowire arrays were created using nanoimprint lithography and ICP/RIE etching. After etching off the Ni mask, a boron diffusion step was performed using SOD. Subsequently, a passivation layer was deposited on the surface of Si nanowires to passivate the surface states. The passivation materials studied in this work include Si_3N_4, ITO and Al_2O_3. Following surface passivation, the Si nanowire array was embedded in transparent Polymethylglutarimide (PMGI) polymer. Oxygen RIE was employed to remove excess resist to expose the nanowire

tips. The dielectric passivation layer (Si_3N_4 or Al_2O_3) on the nanowire tips was removed by wet etching for contact formation. Then ITO was sputtered on top surface as front contact, followed by deposition of Ag front grid electrode using photolithography and lift-off metallization. ITO layer was annealed at 300 ℃ for 1 min on a hotplate to improve the conductivity and transmittance. Indium was soldered on the backside of Si substrates as ohmic back electrode.

3.3.4 Effects of Doping Concentration of Nanowire Core

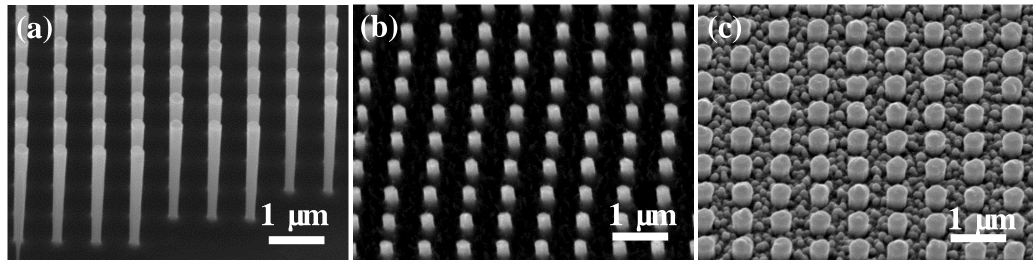


Figure 3.11: SEM images of (a) as-etched Si nanowires, (b) Si nanowires embedded in PMGI, and (c) Si nanowires with 300 nm ITO top contact.

In our research, a master mold with a size of 2×2 cm^2 was used. Using Ni dots as etch mask, we employed anisotropic RIE/ICP etching for 12 min to realize an almost defect-free Si nanowire array with a length of ~2.4 μm. Figure 3.11 (a) shows a SEM image of the high aspect ratio Si nanowire array, with a pitch size of ~600 nm and a diameter of ~ 200 nm. Two sets of Si nanowires were used in this study. The nanowire core of Set #1 is lightly doped with a doping concentration of $\sim 1 \times 10^{15}$ cm^{-3}; and that of set #2 is moderately doped with a concentration of 6.5×10^{17} cm^{-3}. Figure 3.11 (b) exhibited the Si radial junction nanowires embedded in PMGI polymer with

exposed nanowire tips. The length of exposed nanowire tips is ~350 nm. 300 nm ITO was sputtered on top surface as transparent contact, as illustrated in Figure 3.11 (c). No passivation layer was deposited on this set of samples. No Ag front grid electrode was employed.

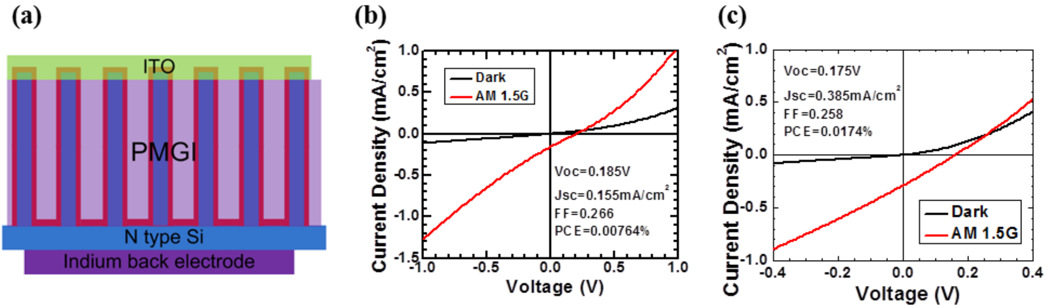


Figure 3.12: (a) Schematic of Si radial junction nanowire solar cell. I-V characteristics of Si nanowire radial junction nanowire solar cells with a core doping concentration of (b) 1×10^{15} cm^{-3}, and (c) 6.5×10^{17} cm^{-3}.

Table 3.2: Summery of performance of solar cells with different n-type core doping concentrations.

	Core doping (cm^{-3})	Diffusion	V_{oc} (mV)	J_{sc}(mA/cm^2)	FF	η(%)
#1	1×10^{15}	820 ℃,20s	0.185	0.155	0.27	0.00764
#2	6.5×10^{17}	820 ℃,20s	0.175	0.385	0.26	0.0174

To characterize the solar cells, I-V measurements were performed under Air Mass 1.5G (100 mW/cm^2) illumination. Figure 3.12 illustrates the schematic of the nanowire solar cell and representative I-V curves measured under dark and illumination. Both sets of devices show diode characteristics under dark and photocurrent was clearly observed upon illumination. Experimental results show the

device with lightly doped n-type core (1×10^{15} cm^{-3}) has a short-circuit current density (J_{sc}) of 0.155 mA/cm^2, an open-circuit voltage (V_{oc}) of 0.185 V, a power conversion efficiency (PCE) of 0.00764% and a fill factor (FF) of 0.27. On the other hand, the devices with moderately doped n-type core (6.5×10^{17} cm^{-3}) exhibit improved performance over those with a lightly doped n-type core. With moderately doped n-type core, the PCE, J_{sc}, V_{oc} and fill factor is 0.0174%, 0.385 mA/cm^2, 0.175 V and 0.26, respectively. As can be seen, the efficiency and short-circuit current density was increased by a factor of over 2 with moderately doped n-type core.

To understand the results discussed above, numerical simulation was carried out to model the band structures of Si radial junction nanowires. Using the simulated doping profiles (Figure 3.9 (b)), the band diagram of radial junction nanowire structure was simulated using Silvaco Atlas, and the results at equilibrium are shown in Figure 3.13. Although the simulated doping profile suggests a radial p-n junction structure for Si nanowires with both lightly (1×10^{15} cm^{-3}) and moderately doped (6.5×10^{17} cm^{-3}) core, the Silvaco Atlas simulation reveals a p-type band diagram with upward surface band bending for the one with lightly doped n-type core. This result is attributed to the fully depletion of Si nanowire core caused by the strong surface effects.[20, 114] In general, the surface state density increases as the diameter decreases. When diameter enters nanometer regime, the surface effects become a dominate factor in determining the carrier transport properties of semiconductors. In the case of Si, the

acceptor-like surface states trap free electrons and induce depletion of electrons inside the nanowire, resulting in enhanced conductivity for p-type Si nanowires and reduced conductivity for n-type Si nanowires.[20] When the density of surface states is higher than electron concentration, fully depletion of electrons may occur, thus n-type Si nanowires change to exhibit p-type characteristics (Figure 3.13 (a)). The surface states occupied by electrons carry negative charges and induce upward band bending. To avoid fully depletion of n-type Si nanowire core, it is necessary to have a higher doping concentration than the density of surface states. The smaller the nanowire diameters, the higher the n-type core doping concentration is required to avoid fully depletion.

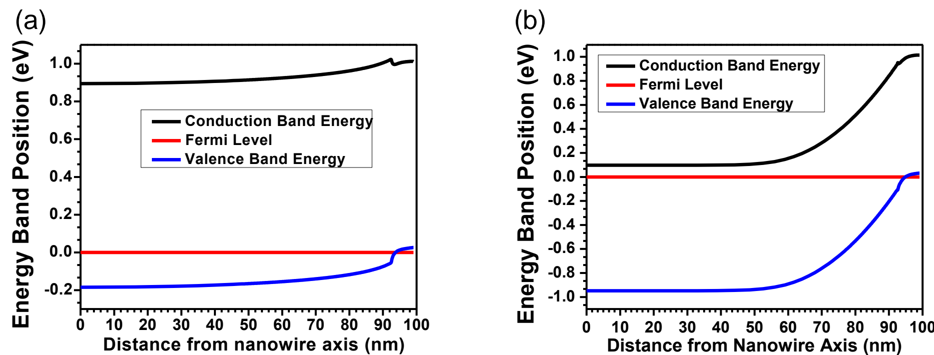


Figure 3.13: Simulated band diagrams of Si nanowires under zero bias. The arsenic doping concentrations of Si nanowire cores are (a) 1×10^{15} cm^{-3}, and (b) 6.5×10^{17} cm^{-3}. The nanowires were doped using boron diffusion at 820 ℃ for 20 s.

In a solar cell, the photocurrent relies on the separation, transport and collection of photo-generated carriers. The separation and transport of carriers occur because of (1) the presence of an electric field, (2) the presence of effective force

fields (changes in affinities and band effective density of states), (3) diffusion, and (4) thermal diffusion if there is temperature gradient.[115] As it is not an effective p-n junction, the build-in potential, which is caused by band bending, of Si nanowire with lightly doped core, is significantly lower than that of the one with moderately doped core. Thus the electric field and effective forces are dramatically reduced, resulting in low carrier collection efficiency.

In addition, as shown in Figure 3.13 (a), there is an electron barrier at the location of the junction depth of Si nanowire. The electron barrier of Si nanowire with lightly doped core is much larger than that of the one with moderately doped core. The origin of the electron barrier is attributed to the difference of band gaps of n core and p shell caused by band gap narrowing.[116] In Si, the impurity levels become broader as increasing doping concentration. In moderately to heavily doped Si, an impurity band forms because of the broadening of impurity levels. When impurity band merges into the conduction band, the band gap narrowing occurs.[116, 117] In non-degenerate Si, the band gap narrowing has a square-root dependence on the doping concentration, which can be express as, $\Delta E_g=22.5\ (n/10^{18})^{1/2}$ meV, at room temperature, where n is the carrier concentration in cm^{-3}. In degenerate Si, band gap narrowing can be obtained by the following equation, $\Delta E_g=162\ (n/10^{20})^{1/6}$ meV.[116] The bandgap narrowing increases with increasing doping concentration. Thus the electron barrier of Si nanowire with lightly doped is larger due to larger differences between carrier concentrations and

band gaps between core and shell. The effective force field resulting from this barrier hinders the transport of photo-generated electron to the nanowire core and hampers the carrier collection efficiency. As only the collected carriers contribute to photocurrent, the poor carrier collection efficiency decreases photocurrent and leads to low power conversion efficiency.

Thus, we have shown that it is critical to have moderately nanowire core doping concentration to avoid fully depletion. The Si nanowire solar cell with moderately core doping does exhibit improved performance but the efficiency is still lower than we expected from excellent light absorption. We suggest the low power conversion efficiency may be a result of poor carrier collection as there is no front grid electrode. In addition, there are several other deleterious factors affecting carrier collection, including (1) the high Auger recombination rate because of high doping concentration, and (2) the high surface recombination rate resulting from the large density of surface states. In the following sections, we will discuss in details regarding the methods to address these issues.

3.3.5 Auger Recombination

When electron-hole pairs are generated by incident photons, the free electrons may be collected by the electrodes to contribute to photocurrent. However, the excited electrons may also return to their ground state or some gap states without doing anything useful. This process which eliminates free electron-hole pairs is called

recombination. There are several recombination mechanisms:[115] (1) Shockley-Read-Hall (SRH) recombination, in which an free electron transits from conduction band into gap states and gives up energy by emission of phonons; (2) radiative recombination, in which electrons transit from conduction band into valence band and gives up its energy by emission of a photon; (3) Auger recombination, in which an electron and a hole recombine by giving energy to an electron in the conduction band or a hole in the valence band. The radiative recombination is only significant in direct bandgap materials. SHR process is the dominant recombination process in Si and other indirect bandgap materials at low carrier concentrations.

However, as Auger recombination rate is proportional to carrier concentration, Auger recombination can become dominant at high carrier concentrations. For Si radial junction nanowire solar cell discussed above, as the nanowire n core is a moderately doped (6.5×10^{17} cm^{-3}) and the p shell ($>1\times10^{19}$ cm^{-3}) is heavily doped, Auger recombination becomes an important factor that hinders the carrier collection. Thus it is important to reduce Auger recombination rate to the minimum to improve solar cell efficiency.

The key to reduce the loss of efficiency in Auger recombination is to lower the doping levels of nanowire core and shell. As it is required to have moderately doped nanowire core to avoid fully depletion, we will need to focus on lowering the shell doping levels. For the Si solar cell discussed above, the surface doping concentration

of p shell is ~3.4×10^{19} cm^{-3}. We carried out a modified two-step boron diffusion process using SOD to reduce the shell doping concentration and thus Auger recombination rate. In the following sections of this chapter, the n-type Si nanowires with a doping concentration of 6.5×10^{17} cm^{-3} were used unless otherwise specified. After pre-deposition at 800 ℃ for 10 s, the Si nanowire samples went through adrive-in process at 800 ℃ for 3 hrs in N_2. The doping profile of this nanowire structure was simulated using Silvaco Athena, as illustrated in Figure 3.14. The simulated profile indicates that the surface doping concentration was reduced to ~2.8×10^{18} cm^{-3} after the drive-in step.

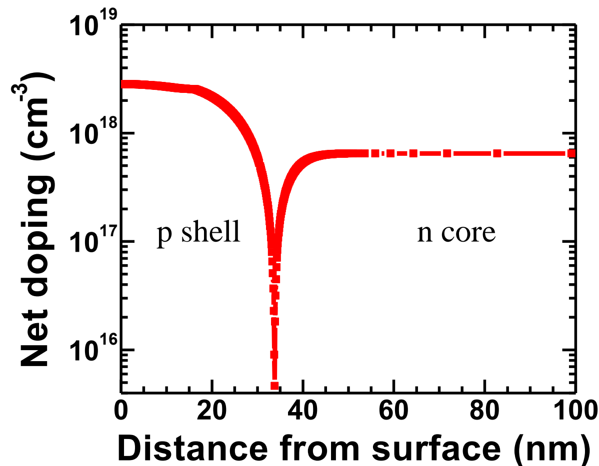


Figure 3.14: Silvaco Athena Simulation of doing profile of Si radial p-n junction nanowire. The radial p-n junction was created using two-step boron diffusion. The pre-deposition step was first carried out at 800 ℃ for 10 s, followed by a drive-in process at 800 ℃ for 3 hrs.

Two sets of Si nanowire samples were used for fabrication of solar cells. The set #5 were doped using one-step boron diffusion (820 ℃, 20s), and Set #6 were doped

using two-step boron diffusion (pre-deposition: 800 ℃, 10 s; drive-in: 800 ℃, 3 hrs). Following boron diffusion, a layer of ITO was deposited on the surface of Si nanowires to passivate the surface states. Subsequently, the Si nanowire array was embedded in PMGI polymer. Oxygen RIE was employed to remove excess resist to expose the nanowire tips. Then another layer of ITO was sputtered on top surface as front contact, followed by E-beam evaporation of Ag front grid electrode using photolithography and lift-off. ITO layer was annealed at 300 ℃ for 1 min on a hotplate to improve the conductivity and transmittance. Indium was soldered on the backside of Si substrates as ohmic back electrode.

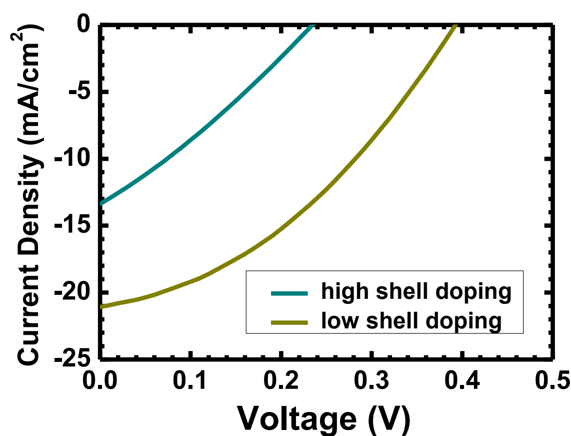


Figure 3.15: I-V curves of Si nanowire radial junction solar cells measured under AM 1.5G illumination (100 mW/cm^2).

The Si nanowire solar cells were characterized using I-V measurements under AM 1.5G illumination (100 mW/cm^2), and the results are shown in Figure 3.15 and Table 3.2. As a result of reduced Auger recombination, the device with lower shell

doping exhibited enhanced solar cell performance, with an open-circuit voltage of 394 mV, a short-circuit current density of 21.1 mA/cm^2, and a power conversion efficiency of 3.11%. The efficiency is over 3 times higher than the one with higher shell doping.

Table 3.3: Comparison of Si nanowire radial junction solar cells with different shell doping concentrations. The surface states of nanowires were passivated using a layer of ITO shell.

Sample ID	#5	#6
Diffusion Condition	820^{0}C for 20 s	800^{0}C for 10 s, then 800^{0}C for 3 hrs
Surface doping (cm^{-3})	3.3x10^{19}	4x10^{18}
Voc (mV)	235	394
Jsc (mA/cm^2)	13.4	21.1
η (%)	0.9	3.11
Fill Factor	0.20	0.37

3.3.6 Effects of Surface Passivation

The surface recombination is the process that occurs at or close to the surface of semiconductor. The high surface recombination rate has detrimental impact on both short-circuit current and open-circuit voltage, especially when the device dimension shrinks and surface-to-volume ratio increases. Particularly, owing to the high surface-to-volume ratio of nanowire structure, the high density of surface states causes a high surface recombination rate, which dramatically reduces the minority carrier

diffusion length and lifetime.[118, 119] Thus, the surface passivation must be reduced to a minimum to achieve high-efficiency solar cells.

In Si, the dominant mechanisms of surface recombination could be either SRH recombination or Auger recombination or both. In the previous section, we discussed the Auger recombination and the method to reduce its rate. This method can also be applied to reduce Auger recombination rate at the surface. In this section, we focus on discussing SRH mechanism of surface recombination.

In the SRH surface recombination process, an electron from the conduction band recombines with a hole in valence band via a defect level, i.e. surface state, within bandgap. The recombination rate U_s via a single-level surface state located at an energy E_t is given by,[27]

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}}$$

with $n_1 \equiv n_i \exp(\frac{E_t - E_i}{kT})$, $p_1 = n_i^2/n_1$, $S_{n0} \equiv \sigma_n v_{th} N_{st}$, $S_{p0} = \sigma_p v_{th} N_{st}$. S_{n0} and S_{p0} are the surface recombination velocity parameters of electrons and holes, n_s and n_p are the electron and hole concentrations at the surface, σ_n and σ_p are the capture cross sections for electrons and holes, N_{st} is the density of surface states, E_i is the intrinsic Fermi level, v_{th} is the thermal velocity of charge carriers (~10^7 $cm^{-1}s$ in Si at 300 K), k is Boltzmann's constant, T is the temperature, and n_i is the intrinsic carrier density. According to the above equation, the surface recombination rate is proportional to the

density of surface states and concentrations of electrons and holes.

In principle, minimization of loss from surface recombination lies on two mechanisms: (1) reduction of surface states, and (2) decrease of concentrations of electrons and holes. Reduction of density of surface states can be accomplished using surface passivation, either by immersing in polar liquids[120-122] or deposition of a passivation film. The wet chemical passivation is not applicable for solar cell applications because of the instability of passivated surface in air. Typically, a dielectric film is deposited on the surface to passivate the dangling bonds. In addition, the recombination rate can also be dramatically reduced by decreasing the concentrations of either type of carriers at the surface, as the SRH recombination process requires one electron and one hole. This can be realized by formation of an internal electric field below the surface, which drives the minority carrier away from the surface. There are two technologies typically used for formation of this electric field. One is to create a high-low doping profile to form a surface field. For example, a p^+-p high-low junction formed using aluminum alloying or boron diffusion is typically used to create a back surface field. This electron barrier decreases the electron concentration below the surface, thus resulting in low recombination rate at rear surface.[123] In addition, the surface electric field can also be induced by the fixed charge at the interface of Si and dielectric films, such as thermal SiO_2 and Si_3N_4.

The aforementioned passivation methods have been widely used in thin film Si

solar cells. However, little work has been reported on passivation of Si nanowires.[106, 124] Understanding of passivation effects of Si nanowires is critical to achieve high-efficiency nanowire solar cells. In this work, we investigated the passivation of p-type shell of Si radial junction nanowires using materials including Si_3N_4, ITO and Al_2O_3 and their impacts on the solar cell performance.

Table 3.4: A list of samples with different diffusion conditions and passivation materials.

Sample ID	Boron Diffusion	Passivation
#3	One-step: 820 ℃,20s	No
#4	One-step: 820 ℃,20s	Si_3N_4
#5	One-step: 820 ℃,20s	ITO
#6	Predeposition:800 ℃,10s; drive-in: 800 ℃,3hr	ITO
#7	Predeposition:800 ℃,10s; drive-in: 800 ℃,3hr	Al_2O_3

Five sets of Si radial junction nanowire samples were deposited with different materials to study the passivation effects. Table 3.4 lists the samples with different doping conditions and passivation materials. Specifically, set #4 were coated with Si_3N_4 using PECVD (Figure 3.16 (a)); set #5 and #6 were coated with ITO using sputtering (Figure 3.16 (b)); and set #7 were coated with Al_2O_3 using ALD (atomic layer deposition, Figure 3.16 (c)). For comparison, a group (#3) of samples without passivation was also fabrication. Please noted, group #3, #4 and #5 were doped using

one-step boron diffusion, while group #6 and #7 were doped using two-step boron diffusion.

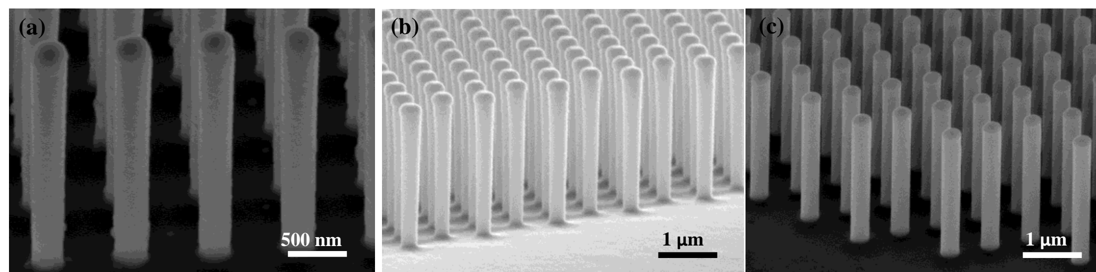


Figure 3.16: SEM images of Si radial junction nanowires with a layer of passivation material as shell: (a) PECVD Si_3N_4, (b) ITO, and (c) ALD Al_2O_3.

The fabrication of solar cells is similar to the process described in Section 3.3.3. Following boron diffusion, a passivation layer was deposited onto the surface of Si nanowires, followed by annealing at 425 ℃ for 30 min in N_2. Figure 3.16 illustrates the conformal coating of the passivation layers. Then the Si nanowires were embedded in PMGI polymer. Oxygen RIE was employed to remove excess PMGI polymer to expose the nanowire tips. The dielectric materials on tips of Si nanowires were removed using wet chemical etching, i.e., Si_3N_4 and Al_2O_3 was removed using diluted HF and BOE, respectively. Then a layer of ITO was sputtered on top surface as front contact, followed by E-beam evaporation of Ag front grid electrode using photolithography and lift-off. The samples were annealed at 300 ℃ for 1 min on a hotplate to improve the conductivity and transmittance of the ITO layer. Indium was soldered on the backside of Si substrates as ohmic back electrode.

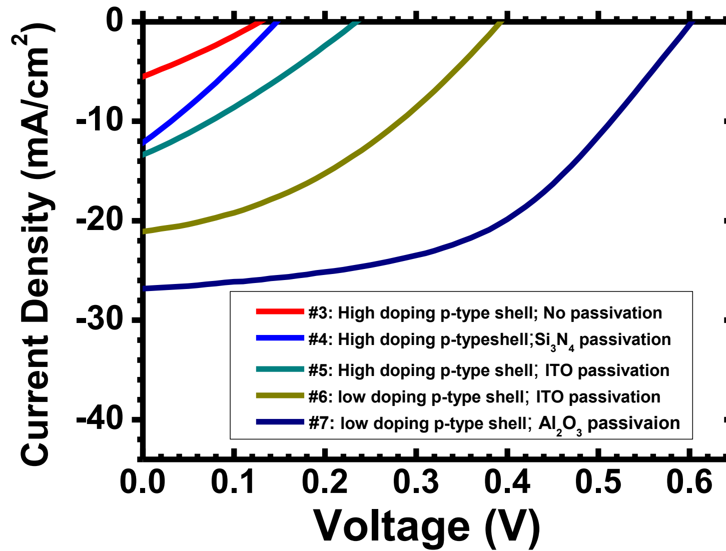


Figure 3.17: I-V curves of Si radial junction nanowire solar cells with various diffusion conditions and passivation layer measured under AM 1.5G illumination (100 mW/cm^2). #3: one-step diffusion (820 ℃, 20 s), no passivation layer. #4: one-step diffusion (820 ℃, 20 s), with Si_3N_4 shell. #5: one-step diffusion (820 ℃, 20 s), with ITO shell. #6: two-step diffusion (pre-deposition: 800 ℃, 10 s; drive-in 800 ℃, 3 hrs), with ITO shell. #7: two-step diffusion (pre-deposition: 800 ℃, 10 s; drive-in 800 ℃, 3 hrs), with Al_2O_3 shell.

The solar cells were characterized using I-V measurements under AM 1.5G illumination (100 mW/cm^2), and results are illustrated in Figure 3.17 and Table 3.5. Without passivation, the sample (#3) has a short-circuit current of 5.52 mA/cm^2, an open-circuit voltage of 130 mV and an efficiency of 0.194%. Both set 3# and #2 were doped using one-step diffusion process (820°C, 20 s). However, Ag grid front electrode was deposited on top of set #3 while not on #2. By comparing the parameters listed in Table 3.2 and Table 3.5, we can see that with Ag front grid electrode, both efficiency and short-circuit current density were over one order of

magnitude higher than the device without front grid electrode. The remarkable enhancement is attributed to the improved carrier collection efficiency of grid electrode.

Table 3.5: Summary of performance of solar cells with different p shell doping and passivation materials.

	Passivation	Diffusion	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF	η(%)
#3	No	820 ℃, 20 s	130	5.52	0.27	0.19
#4	Si_3N_4	820 ℃, 20 s	150	12.2	0.27	0.49
#5	ITO	820 ℃, 20 s	235	13.4	0.29	0.90
#6	ITO	Predeposition:800 ℃,10 s; drive-in:800 ℃,3hrs	394	21.1	0.37	3.1
#7	Al_2O_3	Predeposition:800 ℃,10 s; drive-in:800 ℃,3hrs	603	26.8	0.49	8.0

Si_3N_4 film has been widely used in the Si thin film solar cells, because it is useful not only for anti-reflection coatings but also for surface and bulk passivation.[27, 125-130] The Si_3N_4 film provides excellent passivation effects due to (1) field-effect passivation provided by the positive fixed charge, (2) the properties of the capture cross-sections of the dominant defects, and (3) hydrogen passivation of bulk defects.[131] In this work, we applied this technique to passivate Si radial junction nanowire solar cells. When the device is passivated with a layer of Si_3N_4, significant improvement of device performance has been observed. The device exhibits an open-circuit voltage of 130 mV, a short-circuit current of 12.2 mA/cm^2 and an

efficiency of 0.49%. The short-circuit current and efficiency are increased by a factor over 2 while there is a slight increase of open-circuit voltage compared to the control device without any passivation. The improvement of solar cell performance is due to the reduction of surface recombination resulting from passivation effects. However, the efficiency is still lower than expected. This can be explained by the disadvantage of passivating heavily doped p-type Si using Si_3N_4, although it has been proven to lead to ultra-low surface recombination velocities on n-type and 1 Ω·cm p-type Si.[129] In n-type Si, the fixed positive charges at the Si/Si_3N_4 interface propel the minority carrier holes away from the surface thus resulting in reduced surface recombination rate. However, in p-type Si, the fixed positive charges attract the minority carrier electrons and leads to increased electron concentration at the surface, which would facilitate the surface recombination process.

Another material studied in work for passivation of Si nanowires is ITO. Compared to dielectric materials, it is advantageous to use ITO as it can serve as a transparent conductive electrode besides passivating the surface states. As aforementioned, the radial junction nanowire structure provides a short path for charge separation and collection. With ITO coating on the nanowire surface, the charge collection path can be further reduced. In the case of Si nanowire passivated with dielectric materials or without any passivation, the photo-generated holes (in our case), after separation, still need to transport along the p shell to the nanowire tips to be

collected by the front contact. In contrast, Si radial junction nanowires passivated with ITO allow holes transport along the radial direction to be collected directly by the ITO electrode, resulting in a shorter collection path.

In this work, the ITO passivation layer was deposited onto heavily doped p-type Si shell using a RF magnetron sputtering system. Two sets of Si radial junction nanowire devices were tested and the results are shown in Figure 3.17 and Table 3.5. The set #5 went through one-step boron diffusion (820 ℃, 20 s) process while set #6 were doped using two-step boron diffusion (pre-deposition at 800 ℃ for 10 s, drive-in at 800 ℃ for 3 hrs). It has been reported that the minority carrier lifetime of ITO passivated Si is much lower than the one passivated by Si_3N_4, owing to the defects formed at the ITO/Si interface during sputtering.[132] The defects induce positive fixed charges at the interface thereby decreasing minority carrier concentration at the surface on n-type Si and increasing the minority carrier concentration on p-type Si.[133] However, as shown in Table 3.5, in spite of poor passivation properties of ITO, the efficiency of ITO passivated nanowire device is over 80% higher than the one passivated by Si_3N_4, as a result of shorter carrier transport path. In addition, by lowering the doping level of p-type shell, the efficiency of device (#6) can be further increased to 3.11% due to the suppressed Auger and surface recombination.

As discussed above, the fixed positive charges at the interface of Si and passivation material suppressed surface recombination on n-type Si by reducing

minority carrier concentration. Vice versa, to achieve excellent surface passivation on p-type Si, especially when the doping level is high, it is critical to passivate the Si surface with a material which induces fixed negative charges at the interface. These negative charges increase the barrier height for electrons thereby reducing the minority carrier concentration and surface recombination rate. It has been reported that the Al_2O_3 contains a high density of fixed negative charges.[134] Recently, Study on Si thin film devices shows Al_2O_3 film provides excellent surface passivation on moderately and heavily doped p-type Si emitter.[135, 136] In this work, we investigated the surface passivation of Si radial junction nanowires using Al_2O_3 film. The Si nanowires were doped using two-step boron diffusion. After RCA cleaning, the Al_2O_3 film was deposited onto Si nanowire surface using ALD at 250 ℃, followed by a thermal annealing at 425 ℃ for 30 min in N_2.[136] The result of a representative device passivated by Al_2O_3 is shown in Figure 3.17 and Table 3.5. Owing to the excellent passivation effects of Al_2O_3 film, the device shows significant improvement, with a short-circuit current of 26.8 mA/cm^2, an open-circuit voltage of 603 mV and a power conversion efficiency of 8.0%. This result reveals that the surface recombination is suppressed because of the fixed negative charges at the interface. As 15% of the front surface area was covered by the Ag front grid electrode, the effective short-circuit current is 31.5 mA/cm^2 and effective efficiency is 9.4% after exclusion of front contact area.

3.3.7 Conclusion

In conclusion, we have demonstrated Si radial junction nanowire solar cells. The well controlled nanoscale doping was achieved using boron SOD and RTA process. The doping profile was studies by SIMS analysis and Silvaco simulation. A variety of parameters that affecting device performance was investigated and optimization of solar cells was carried out. It is necessary to have moderately doped nanowire core to avoid fully depletion of the nanowire. The surface recombination mechanisms were extensively discussed and methods to reduce recombination rate were developed. By lowering the doping levels of p-type shell, the Auger recombination was dramatically reduced. Surface passivation of heavily doped p-type Si shell using materials including Si_3N_4, ITO and Al_2O_3 were studied. The Si_3N_4 film can effectively passivate the surface states but the fixed positive charges at the interface attract electrons to the surface thereby increasing the minority carrier concentration. ITO film passivated Si nanowire device exhibited higher efficiency than those passivated by Si_3N_4 owing the further reduced carrier collection distance. Al_2O_3 film provides excellent surface passivation of p-type Si because of the field-effect passivation induced by the fixed negative charges. With Al_2O_3 passivation, the Si radial junction nanowire solar cells showed an efficiency of 8%.

Chapter 3, in part, has been submitted for publication of the material that may appear in ACS Nano 2013. Yi Jing, Siarhei Vishniakou, Chulmin Choi, Ke Sun, Huisu Jeong, Muchuan Yang, Alireza Kargar, Sungho Jin, Gun Young Jung, and Deli Wang, "Effects of doping and passivation on Si radial junction nanowire solar cells". The dissertation author was the primary investigator and author of this paper.

Chapter 4: III-V Nanowire Solar Cells

4.1 Introduction

III-V compound semiconductor nanowires have been attracting extensive research interest for applications including field-effect transistor, lasers, light-emitting diodes, photodetectors, solar cells, chemical/biosensors and thermal-electric devices.[2, 3, 5, 66, 137] III-V materials are of particular interest for photovoltaic applications. A record efficiency of 44.4% has been reported for III-V triple-junction solar cells by Sharp.[138] However, III-V semiconductor devices are usually epitaxially grown on expensive planar lattice-matched III-V wafers, which greatly increase the manufacturing cost and hinder the widespread application of III-V solar cells. Therefore, heterogeneous integration of III-V materials with low cost substrates, such as Si, is highly desirable because it not only reduces the manufacturing cost but also enhances the device functionalities. However, due to the large mismatches of lattice and thermal constants, the III-V thin films epitaxially grown on Si suffer from large density of dislocations and antiphase boundaries.

On the contrary, the one-dimensional nanowire structure provides an alternative method to integrate III-V materials to Si. Owing to small dimensions (i.e. small contact area between a nanowire and its substrate), strains are relaxed within a

few atomic layers at the interface,[139] thus enabling heteroepitaxy of III-V nanowires on Si substrate by overcoming restriction of lattice mismatch. Various methods have been employed to epitaxially grow III-V nanowires on Si. The most popular one is vapor-liquid-solid (VLS) method, first proposed by Wagner and Ellis in 1964.[1] By introducing a catalytic metal nanoparticle, which absorbs reactants in vapor phase to form supersaturated liquid alloy inside the nanoparticle, single crystal semiconductor nanowires can grow from the nucleated seeds at the liquid-solid interface.[53] VLS mechanism have been widely used to synthesize almost all kinds of semiconductor nanowires, including Si,[1] Ge,[52] III-V compounds[53-55], II-V materials[140, 141] and so on. However, Au, which is the most commonly used metal catalyst for single crystal nanowire growth, forms unwanted deep level traps in semiconductor nanowires during growth. These traps are notoriously deleterious to the performance of nanowire devices.[56-58] Thus, it is highly desirable to synthesize III-V nanowires without use of Au as nucleation and growth seed. This has been achieved by self-catalyzed growth[59-65] or catalyst-free growth. In the case of self-catalyzed growth, one or more nanowire elements, usually In[61] or Ga[62] droplets, are used as the seed nanoparticles; thus it is also categorized as VLS growth. On the other hand, no catalyst is used during the nucleation and growth for the catalyst-free method. For example, selective-area growth uses partially masked substrate, usually by an oxide or nitride layer, with lithographically defined opening pattern.[142-144] Consequently, semiconductor materials

nucleate and initiate nanowire growth in the openings after increasing the temperature and introducing the reactant precursors. It is also reported that coating of the Si substrate with a layer of organic materials allows nucleation of direct growth of InAs nanowires without the use of catalysts.[145]

A simple alternative catalyst-free method is to directly synthesis III-V nanowires on substrates without use of any pre-deposited materials or mask.[146] In this work, we systemically study the direct heteroepitaxial growth of vertically aligned III-V nanowires on cheap and large-scale Si substrates; particularly InAs based nanowires and core/shell nanowire heterostructures, using a simple catalyst-free metal-organic chemical vapor deposition (MOCVD) method. This work provides insight and understanding of the growth mechanism. Moreover, by changing the precursors during the growth process, this catalyst-free method allows fabrication of core/multi-shell nanowire heterostructures and allows one to intentionally dope the nanowires. In this work, InAs based core/multi-shell nanowires were successfully synthesized and preliminary result of solar cells was demonstrated.

4.2 Catalyst-free Growth of InAs Nanowires

The InAs nanowire growth was carried out in a low pressure close-coupled showerhead (CCS) MOCVD system (Thomas Swan Scientific Equipment Ltd.). The carrier gas used was pure H_2 that was purified through a Pd membrane. The precursors

for group V and group III materials were 5% H_2 diluted arsine (AsH_3) and trimethylindium (TMI), respectively. After solvents cleaning and surface preparation processes, the Si substrates were immediately loaded into MOCVD reactor chamber. Prior to growth, the Si substrates were annealed at 635 ℃ for 10 min in H_2 ambient. Then the reactor was cooled down to the growth temperature of 550 ℃. As soon as the growth temperature was stabilized, the AsH_3 and TMI were introduced into the reactor simultaneously to initiate InAs growth. The mole fractions of AsH_3 and TMI were 2×10^{-4} and 2×10^{-6}, respectively. The chamber pressure was maintained at 100 Torr during growth and the total flow rate of H_2 carrier gas was 20 standard L/min. The growth time was 5 min unless otherwise specified. The growth was terminated by shutting off the TMI flow while maintaining AsH_3 flow until the reactor was cooled down to below 300^0C to prevent decomposition of InAs nanowires.

The surface condition of Si substrate is very critical to achieve high quality single crystalline InAs nanowire arrays on Si with high reproducibility and good coverage. Thus, we investigated the effects of Si surface preparation methods on the InAs nanowire to optimize the growth conditions and understand the growth mechanism. Si (111) wafers were cut into ~ 1×1 cm^2 size for nanowire growth. The Si substrates were first cleaned with solvents in an ultrasonic bath. Then the Si surface was treated differently for InAs nanowire growth, including (i) Si substrates with native oxide, 100 nm thick thermally grown SiO_2, or native oxide plus ozone plasma

treatment; (ii) Si surface treated with BOE and deionized water (DIW) rinsing for different lengths of duration; (iii) Si surface treated with BOE etch and re-oxidation in humid air. The treated substrates were blown dry with nitrogen and immediately loaded into a MOCVD chamber for nanowire growth.

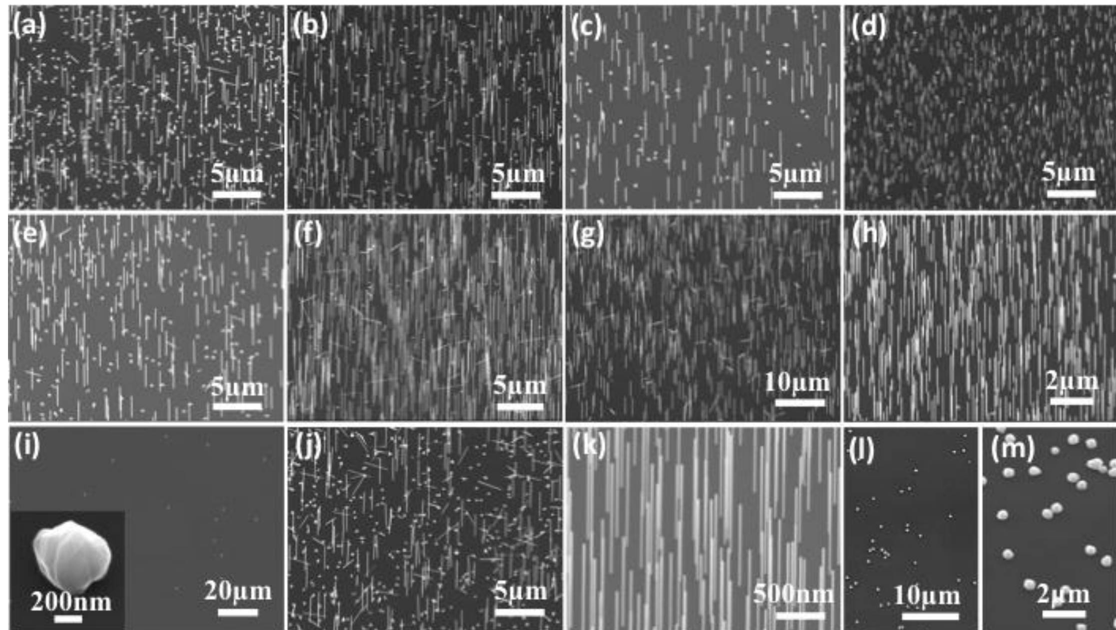


Figure 4.1: SEM Images of InAs growth on Si (111) at 45° tilted view. The growth were done at 550 ℃ for 5 min. (a-d) Si substrates were cleaned, BOE etched for 1 s (a), 3 s (b), 30 s (c), and 2 min (d) and rinsed with DIW for 15 s, and pre-baked in H_2 at 635 ℃ for 10 min prior to growth. (e-h) Substrate surface was treated with ozone plasma, BOE etched for 1 s (e), 3 s (f), 5 s (g), 30 s (g), and treated identically as in (a-d) before growth. (i-k) Substrates were treated with ozone plasma similarly as in (e-h) with BOE etching of 1 s (i), 10 s (j), 30 s (k), except no pre-baking was performed. (l) Si substrate with 100 nm thermal SiO_2. (m) Si substrate with native oxide.

We first studied the growth of InAs nanowires under identical growth conditions (pre-baking in hydrogen at 650 ℃ for 10 min, followed by InAs nanowire growth at 550 ℃ for 5 minutes) on Si substrates with different BOE etching time of

the native oxide. The SEM images of InAs nanowires grown on Si with varying BOE etch times are shown in Figure 4.1 (a)-(d). The DIW rinsing time is 15 s for this set of samples. As can be seen, vertical InAs nanowires were observed on Si after removal of native oxide by BOE regardless of the lengths of etching time. In the case of 1 s BOE etch (Figure 4.1 (a)), in addition to vertical nanowire growth, the presence of a large density of InAs islands and nonvertical nanowires were observed as well. As the BOE etching time increases, the density of InAs islands and non-vertical nanowires decreases (Figure 4.1 (b), (c)); when the BOE etching time is longer than 30 s, there is no significant change of islands density when etching time is further increased (Figure 4.1 (c), (d)). This result indicated that the native oxide was completely removed when etched in BOE for 30 s, exposing the oxide-free Si surface, which was favorable for InAs nanowire nucleation. However, the nanowire density is increased in Figure 4.1 (d) for 2 min etching, while the nanowires are thinner, which indicates more nucleation sites for longer etching time.

We have also tried, prior to the etching, ozone treatment of the Si substrates, which can remove organic contamination on the Si surface (uniform removal of oxide by BOE etching) as well as increasing the oxide thickness. Figure 4.1 (e)-(h) illustrate the SEM images of a set of samples which were treated with ozone plasma and BOE etching with different times. Compared to the samples without ozone treatment (Figure 4.1 (a)), the growth done with ozone treatment shows reduced density of

islands. The sample with 1 s BOE etch shows no significant change of density of nonvertical nanowires. However, the sample with 3 s BOE exhibits much larger density of nonvertical nanowires. The density of islands and nonvertical nanowires almost diminished for the growth done with 30 s BOE etching, which can be probably attributed to that there is less organic contaminations on Si surface after ozone treatment and substrates has very good uniformity in etching. These results suggest that completely removal of native oxide by BOE etching is critical for uniform growth. However, there are two other factors to be considered regarding the coverage of native oxide on the Si surface during the nanowire growth practice. (1) The DI water rinsing may also play a role as there could be regrowth of native oxide from Si oxidation from water. Growth under identical conditions on a substrate without DI water rinse cannot be performed due to the nature of HF handling and potential contaminants from the etchant residues. (2) The pre-baking practice in hydrogen at 650 ℃ prior to the nanowire growth may reduce the native oxide. Thus we hypothesize that the combination of the two leads to the formation of oxide patches on Si surface with original native oxide, which is line with the proposed catalyst-free III-V nanowire growth on Si substrates.[24]

To test this hypothesis, InAs nanowire growth without substrates prebaking was carried out. Interestingly, no nanowires but only InAs island growth (Figure 4.1 (i) and inset) was observed on the samples treated with ozone and 1s BOE etching,

similar to the cases of that on native oxide (Figure 4.1 (m)) and thermal oxide surface (Figure 4.1 (l)), which is presumably due to that 1 s BOE etching alone without hydrogen reduction during the prebaking step is not sufficient to remove all the native oxide and expose Si (111) surface. Even on substrate with 3 s BOE etching, it still shows high density of nonvertical nanowires and islands (Figure 4.1 (j)), which are similar to that from growth with 1s BOE etching and hydrogen prebaking (Figure 4.1 (e)). These results clearly suggest that prebaking in hydrogen has equivalent effect to BOE etching. The yield and morphology of InAs nanowires on the substrate when BOE etch time is above 30 s (Figure 4.1 (k)) becomes comparable to that with prebaking in hydrogen (Figure 4.1 (c)).

To further understand the surface treatment effects, we also studied the rinsing effect after BOE etching. Figure 4.2 (a)-(d) show the SEM images of InAs growth at 550 ℃ for 5 min with substrate pre-baking in H_2 at 635^oC for 10 min. The Si substrates were cleaned, BOE etched for 1 s, and rinsed with DIW for 1 s (a), 4 min (b), 8 min (c), and ultrasonication in DIW for 4 min (d), respectively. There is a clear trend of increasing density of vertical InAs nanowires and decreasing density of islands with DI water rinsing time. Interesting, ultrasonication in DI water (Figure 4.2 (d)) showed similar effect with running DI water rinsing (Figure 4.2 (b)). It appears that rinsing with running DI water for 8 min gives the best result with regarding the vertical nanowire density and morphology. We thus then compared the growth on

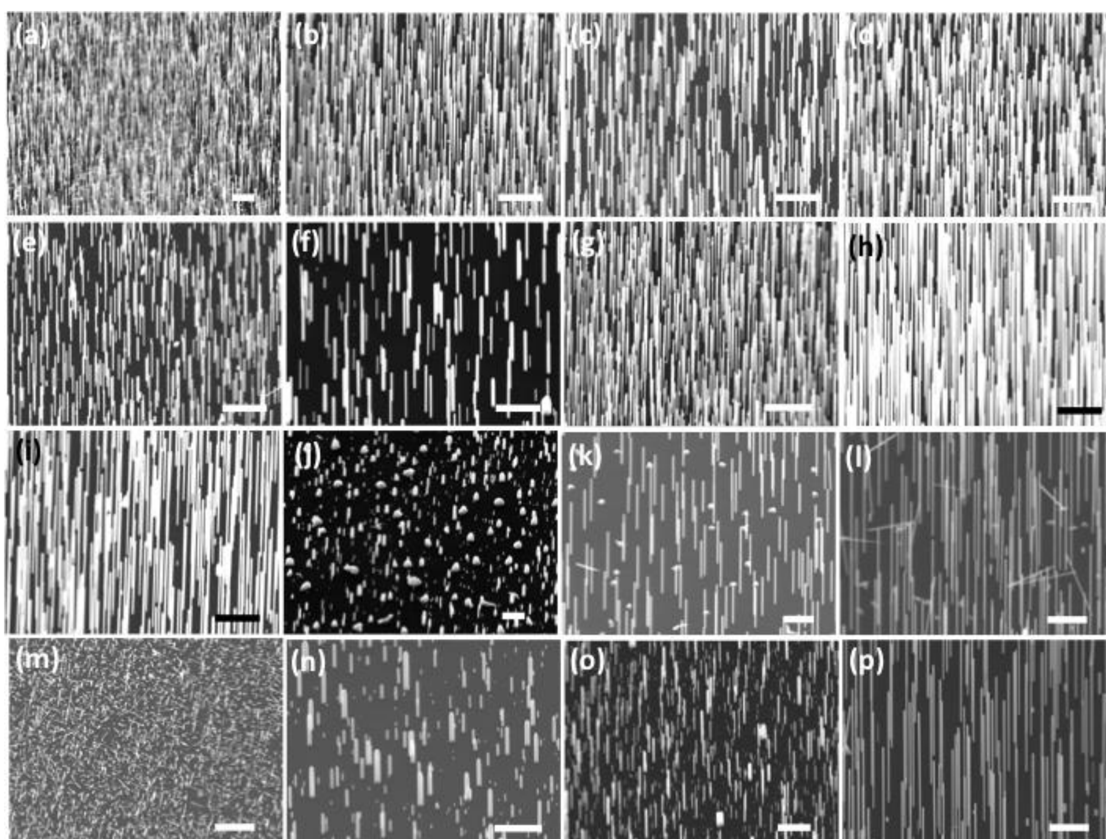


Figure 4.2: SEM Images of InAs growth on Si (111) with 45 ° viewing angle. The growth was done at 550 ℃ for 5 min with substrate baking in H_2 at 635 ℃ for 10 min prior to growth, unless otherwise specified. Scale bars are 1 μm. (a-d) Si substrates were cleaned, BOE etched for 1 s, and rinsed with DIW for 1 s (a), 4 min (b), 8 min (c), and ultrasonication in DIW for 4 min (d). (e-g) Substrate surface was BOE etched for 3 s (e), 20 s (f), 30 s (g), respectively, and rinsed in running DIW for 8 min. (h) Surface treatment identical to (e), with 3 s BOE etching and 8 min DIW rinse, but with 10 min growth. (i) Surface treatment with 20 s BOE etching and 4 min DIW rinse, but with 10 min growth. (j) Substrate surface was BOE etched for 3 s, quickly rinsed with DIW and rinsed with IPA for 4 min. (k-m) Si surface etched for 30 s and rinsed with DIW for 15 s, re-oxidized in humid air for 12 hrs (k), 24 hrs (l), and 130 hrs (535 ℃ growth) (m), respectively. (n-p) Substrate surface was coated for decane for 12 hrs, 17 hrs, and 26 hrs, respectively.

substrates with different BOE etching time (3 s in Figure 4.2 (e), 20 s in Figure 4.2 (f), and 30 s in Figure 4.2 (g)) and same rinsing time of 8 min. These results are very

comparable with that of BOE etching for 1 s (Figure 4.2 (c)), and there is no strong indication of etching time affecting the vertical nanowire growth and morphology. However, stronger contract was observed for the nanowire growth on Si substrates with organic solvent rinsing after BOE etching, where presumably there is no re-growth of native oxide. With identical surface treatment, longer growth time resulted in correspondingly similar morphology, longer nanowires and larger length variation, and higher density. Figure 4.2 (h) and (i) show the SME images of the growth with 3 s BOE etching and 8 min DIW rinse, but with 10 min growth (vs. Figure 4.2 (e)), and with 20 s BOE etching and 4 min DIW rinse, but with 10 min growth (vs. Figure 4.2 (f)). These results indicated new nucleation of new nanowires occurs during the growth, leading to larger variation of the nanowire length and diameter, and much longer nanowires. The nanowires are uniform in diameters along the axial direction.

Figure 4.2 (j) shows the SEM image of InAs nanowire growth on Si substrates with surface treated by BOE etching for 3 s, a rapid DIW rinsing and IPA rinsing for 4 min, where very few short InAs nanowires grown and formation of mainly irregular islands (In comparison with Figure 4.2 (b), (e)). This is presumably due to the IPA rinse prevents formation of oxide patches. We have also tested the nanowire growth on substrate with controlled regrowth of native oxide (with different thickness), where the Si wafers were first etched with BOE to remove the native oxide and exposed to

humid air (85% relative humidity at room temperature) for different lengths of time. Formation of islands and nonvertical nanowires was insignificant on Si re-oxidized for 12 hrs (Figure 4.2 (k)). However, as re-oxidation time increased, density of islands and nonvertical nanowires increases dramatically, and dominates after 130 hrs (Figure 4.2 (l) and (m)).[146] We have also performed the InAs nanowire growth on Si substrates with surface treated by organics. Figure 4.2 (l)-(n) show the SEM images of growth with substrate surface coated with decane for 12 hrs, 17 hrs, and 26 hrs, respectively. The results reflect the prior reported nanowire growth with decane coating.[145]

From the above results, we can see that the thickness and coverage of oxide is critical to the yield of nanowire growth. The BOE etch and prebaking can reduce the oxide thickness while humid air, ozone plasma and DIW rinsing can re-oxidize Si and form oxide patches. The key to achieve high yield vertical InAs nanowire growth is to have oxide-free Si surface for nanowire nucleation and oxide patches to hinder formation of large InAs islands. Based on these discussion, we have developed a simple catalyst-free method to grow vertical InAs nanowire array with minimal density of islands and nonvertical nanowires, uniform coverage and high-reproducibility on Si, i.e. use BOE etch to remove native oxide and DIW rinsing to modulate the oxide coverage. The optimal growth was achieved on BOE treated Si surface with 4-8 min DIW rinsing.

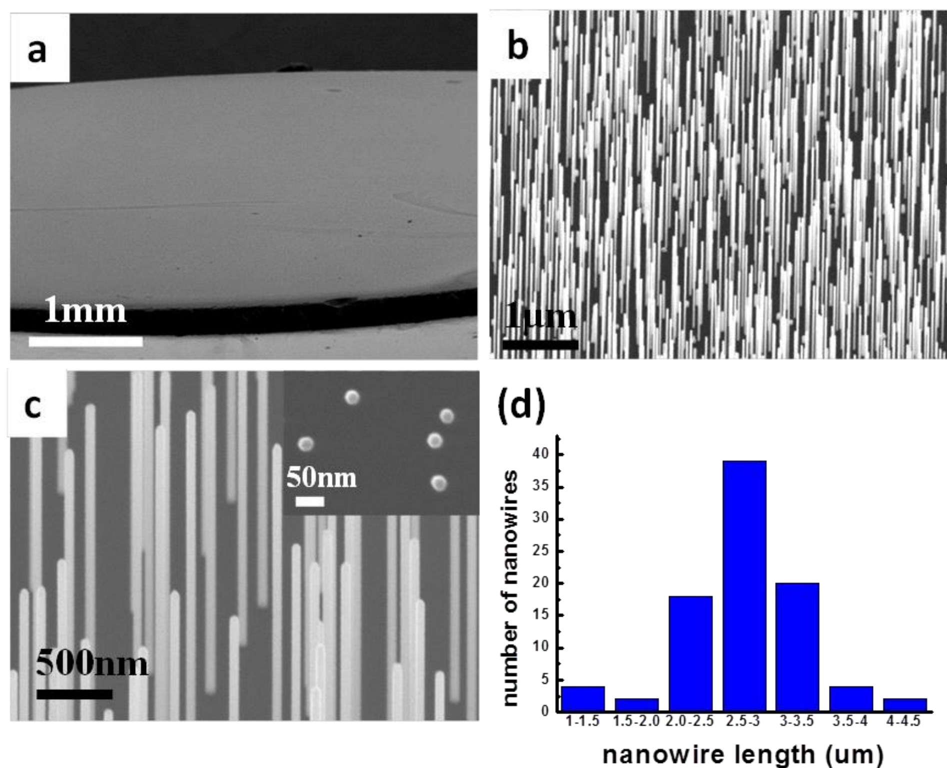


Figure 4.3: (a), (b) and (c) are SEM images of InAs nanowires grown for 5 min on Si(111) substrate. Si was treated with BOE etch for 30 s and rinsed in running DIW for 8 min. (d) Column graph showing distribution of nanowire diameters.

Figure 4.3 shows the SEM images of InAs nanowires grown on Si (111) substrates prepared using the optimal surface treatment conditions - with BOE etch for 30 s and rinsed in running DIW for 8 min. The InAs nanowires are vertically aligned to the surface, indicating epitaxial growth along [111] orientation, with uniform coverage on Si substrates (Figure 4.3 (b), (c)). The diameters of InAs nanowires are in the range of 30 to 80 nm; and the lengths range from 1.2 to 4.5 µm, with a majority around 2-3.5 µm (Figure 4.3 (d)). The InAs nanowires exhibit hexagonal cross section and smooth sidewall surface (Figure 4.3 (c) inset). From the Si (111) cleavage, we can

figure out that side facets of the nanowires are {110}. The nanowires are uniform in diameter without measurable tapering or large base at nanowire/substrate interface. On the contrary, InAs nanowires grown with Au catalyst usually show large base surrounding nanowire foot and are tapered when length is over the indium diffusion length (~1 μm).[53, 147] The morphology of our InAs nanowires is similar to those grown with selective-area MOCVD method.[142, 143, 145] However, the selective-area method requires a partially masked template with nanoscale opening patterns, where nanowires nucleate and grow without assistance of metal catalyst. The template is usually patterned by electron-beam lithography,[143, 148] which is a slow and expensive process and hardly scalable. Nucleation template formed by self-assembled organic coating[145] and nanosphere lithography[149] have been employed in selective-area growth to achieve large-area III-V nanowire array. In our method, no predefined mask layer is used to assist the nanowire growth, thus it can be easily scaled up to wafer size. In this work, wafer-scale InAs nanowire array has been successfully synthesized on 2-inch Si (111) wafers with uniform coverage using the catalyst-free MOCVD method. No noticeable difference was observed on nanowire morphology compared to growth on small Si substrates.

The results discussed herein revealed that oxide layer played a significant role on the growth quality and morphology of InAs nanowires. Our observation is consistent with those reported by Madsen et al.[150] The growth can be categorized into

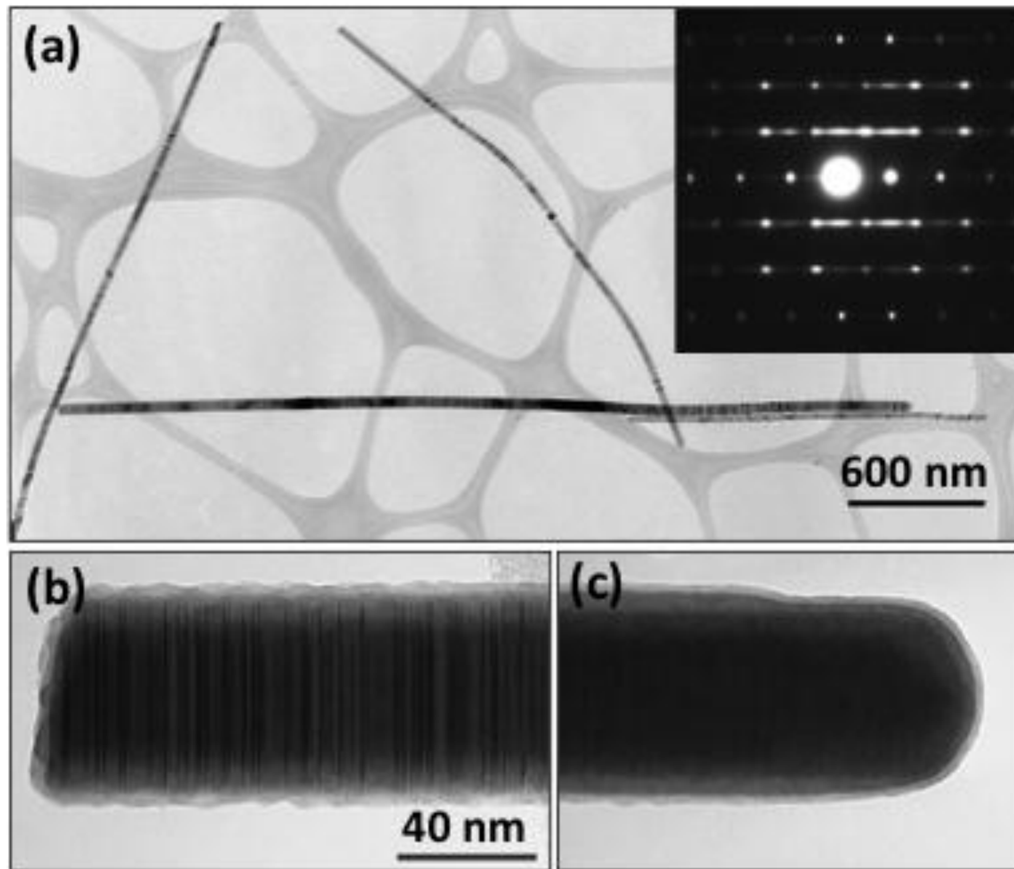


Figure 4.4: TEM micrographs of InAs nanowires. (a) Low resolution image of InAs nanowires. The corresponding electron diffraction pattern is shown in the inset. (b) High resolution TEM image of bottom portion of a nanowire. (c) High resolution TEM image of the top portion of a nanowire.

four regimes: (1) growth on Si without oxide (BOE treated with 15 s DIW rinsing) results in vertical nanowires dominated growth with a relatively high density of nonvertical nanowires and islands; (2) growth on Si with thin oxide patches (BOE treated with 8 min DIW rinsing) leads to high yield vertical nanowire growth, almost free of parasitic islands and nonvertical nanowire growth; (3) growth on thicker oxide (regrown oxide in humid air for 130 hrs) causes islands and nonvertical nanowires

dominated growth; (4) No nanowire but islands growth on thermal SiO_2 or native oxide.

TEM study was performed to provide insight on the growth mechanism. Figure 4.4 illustrates the TEM study of the crystal structure of InAs nanowires. The low-resolution image (Figure 4.4 (a)) shows that the nanowires are very uniform in diameter, without any visible tapering. The high-resolution TEM (HRTEM) and SAED (Figure 4.4 (b) inset) reveal that the nanowire has a zinc blende crystal structure and grows along [111] direction, with a high-density of twin planes and stacking faults, whereby the crystal structure alternatives between zinc blende and wurtzite over the entire nanowire length. Metal droplet is typically observed at the tip of nanowires grown by catalytic or self-catalytic methods.[151] In our case, however, no metal droplet is present as shown in the image of nanowire tip (Figure 4.4 (c)). The growth mechanisms proposed to realize catalyst-free III-V nanowire growth includes selective-area growth[142] and self-catalyzed VLS growth[151, 152] as discussed above. The selective-area growth is initiated by the nucleation of InAs inside pre-defined opening in the dielectric layer. On the contrary, in our method, vertical InAs nanowires can grow on oxide-free Si (111) surface. After BOE etch, the native oxide was removed to expose the atomically flat Si surface. Simultaneously, the Si surface was passivated by hydrogen bonds, preventing the formation of new oxide at least within a few minutes.[153-155] This reveals a different growth mechanism from selective-area growth.

On the other hand, self-catalyzed VLS growth relies on the formation of indium or gallium droplets to initiate nanowire growth.[64, 65, 156, 157] In our study, no indium droplet was noticed at the apex of nanowire. Non-tapered geometries of InAs nanowires excludes the possibility of consumption and crystallization of indium droplets by excess AsH_3 during post-growth cooling, since diminishment and eventual disappearance of metal catalysts would result in tapered nanowires with sharp tips.[158] Furthermore, VLS grown InAs nanowires usually exhibit large base at nanowire root and are tapered when length is over indium diffusion length,[53, 147] which were not observed in our study. This result indicates the growth is not governed by VLS mechanism. This is further corroborated by *in situ* reflection high energy electron diffraction (RHEED) studies reported by Hertenberger et al,[159] showing InAs nanowires nucleation under the absence of indium droplets and without any significant delay after introducing the precursors.

The InAs nanowire growth is believed to obey the Volmer-Weber growth mode.[160, 161] Due to the large lattice mismatch between Si and InAs (11.6%), 3D InAs islands spontaneously nucleate on the atomically flat and oxide-free Si (111) surface pre-treated with BOE. In plane InAs thin film growth is prevented because of the large interfacial energy, resulting in nanowire growth along [111] orientation, so that the strain can be relaxed laterally.[162-164] Only the InAs islands with sizes smaller than the critical diameter enable epitaxial nanowire growth.[162-164] The size of InAs islands can

be mediated by the preparation conditions of Si substrates. On a completely oxide-free surface treated with BOE etch, the indium adatoms are very mobile and large InAs islands form quickly, hindering vertical nanowire growth. Under optimal conditions, when, after BOE etch, the substrate is rinsed with DIW for a few minutes, SiO_x patches form on the surface. The indium adatoms are immobile on Si surface with SiO_x patches in contrast to that on clean oxide-free surface. Thus the density of large InAs islands are reduced to a minimal level, resulting in high density nanowire array. III-V nanowires typically grow preferentially along [111]B direction, thus vertical nanowires form on (111)B surface of III-V substrates. Si has nonpolar nature and there are four equivalent [111] directions on Si (111) surface; one is along vertical direction and the other directions are 19.6 °tilted with respect to the (111) surface.[165] Our results show that the InAs nanowires grow predominately along vertical [111] direction rather than the other three equivalent [111] directions. This is most likely due to the passivation of Si dangling bonds with As atoms when substrate surface is exposed to AsH_3 prior to growth.[142, 166] Once As-incorporated Si has formed on surface, which mimics the (111)B surface of III-V semiconductors, only vertical nanowires are allowed to grow on Si (111).

The cross sectional TEM was carried out on InAs nanowires grown on Si (111) to investigate the nanowire/substrate interface. Figure 4.5 (a) is a low resolution TEM image, showing an InAs nanowire perpendicular to the Si substrate. A magnified

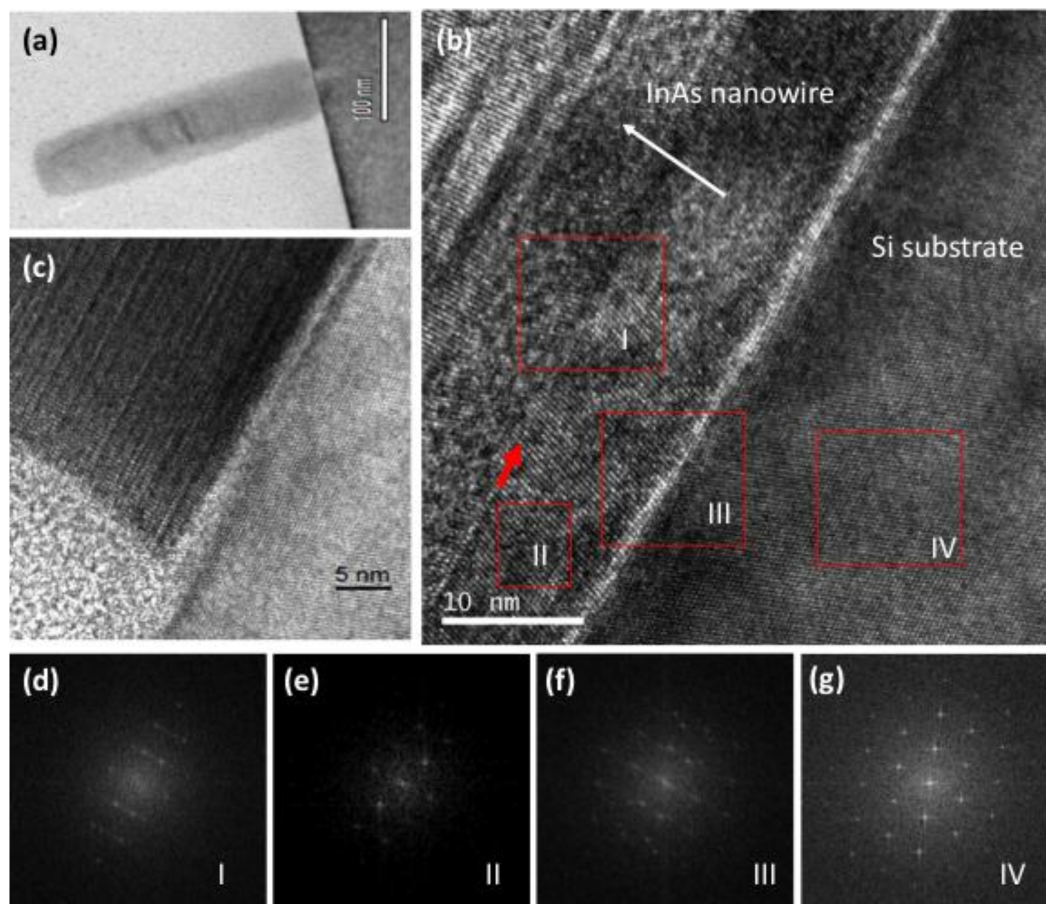


Figure 4.5: Cross sectional TEM images of InAs nanowires grown for 5 min on Si (111). (a) Low resolution TEM showing InAs nanowires embedded in PMGI polymer. (b) High resolution TEM of InAs/Si interface. (c) High resolution TEM of edge of InAs/Si interface. Fast Fourier transforms of (d) region I, (e) region II, (f) region III, and (g) region IV.

HRTEM image of nanowire/substrate interface (Figure 4.5 (b)) taken in the near-center region shows that InAs nanowire was epitaxially grown on Si (111), with an almost atomically flat interface between the InAs nanowire and Si substrate. The white arrow indicates the nanowire growth direction. Both the HRTEM (Figure 4.5 (b)) and fast Fourier transform from region II (FFT, Figure 4.5 (e)) reveal a zinc blende crystal structure at nanowire base, with a low density of defects. After a region

of 10 nm zinc blende InAs, rotational twining started to appear, as indicated by the red arrow in Figure 4.5 (b). The streaking in FFT pattern from region I (Figure 4.5 (d)) implies the presence of defects in this region. A high density of twin planes and stacking faults became to form after growth of 18 nm low-density defect region. The defects were observed along the entire nanowire length, as aforementioned. Twinning and stacking faults are often observed in InAs nanowire grown by Au-assisted VLS method[167, 168] and selective-area method.[142] The formation of these defects is due to the strain relaxation when nanowire length is above the critical thickness. Growth of defect-free InAs nanowires with pure zinc blende or wurtzite phase has been achieved by controlling nanowire diameter and growth temperature in the case of Au-assisted VLS method.[169] To our best knowledge, defect-free InAs nanowire grown by catalyst-free method has not been reported. Figure 4.6 (c) shows the presence of a thin (1-2 nm) amorphous layer at the edge of the heterogeneous interface, which was also observed by Cantoro *et al*.[166] This was attributed to the re-oxidation of the Si surface. FFT of region III results in an overlay of the Si (region IV) and InAs (region II) patterns. Because Si substrate and zinc blende InAs nanowire have similar crystal structure (the diamond structure is identical to the zinc blende structure with the exception that each atomic side is populated by the same atom) and the same orientation, the FFTs of region IV and II looks similar. However, the InAs spots are

located closer to the central spot than Si spots as illustrate in Figure 4.6 (f), since InAs has a larger lattice constant (6.0583Å) than Si (5.431Å).

4.3 Catalyst-free Growth of InAs based Core/multi-shell Nanowires

One most intriguing property of III-V compound semiconductors is the easy formation of heterostructures, which offer the flexibility to tailor the band structure of the materials to acquire desired electrical and optical properties. The heterostructures containing multiple group III (e.g. Al, In, Ga) and/or group V (P, As, Sb) elements are of particular interest for band gap engineered optoelectronic devices, such as lasers, broad band photodetectors and tandem solar cells. In addition, core/(multi-)shell nanowire structures, in which a doped nanowire core is surrounded by one or more shells of opposite doping type, allow maintaining good light absorption and enhanced carrier collection efficiency simultaneously by orthoganalizing the directions of light absorption and carrier collection.[35, 103] Various InAs based nanowire core/shell structures have been reported, including InAs/GaAs core/shell nanowires,[170-172] InAs/InP core/shell nanowires,[173-175] InAs/AlInAs and InAs/AlInP core/shell nanowires.[176] Most of them, however, were grown by VLS mechanism assisted by Au droplets, which is not compatible with current CMOS processing. Catalyst-free growth of InAs/GaAs has been reported by Paetzelt et al,[177] but the nanowires are either bended or has inhomogeneous shell coverage and irregular sidewalls due to lattice

mismatch. In the following, we will present the catalyst-free growth of vertically aligned InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires on Si. Heavily doped n-type Si (111) was used as substrates for nanowire growth. Unintentionally doped n-type InAs nanowire was used as the core material. Subsequently, nominally intrinsic (i) InGaAs, i-GaAs and p-type InGaP were deposited in succession onto InAs nanowire core as shells. To find out optimal growth conditions of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires, nanowire radial heterostructures including InAs/InGaAs and InAs/InGaAs/GaAs were studies as well. SEM and TEM were employed to investigate the morphology and crystal structure of the core/multi-shell nanowires. Current-voltage measurement was performed to study the electrical properties.

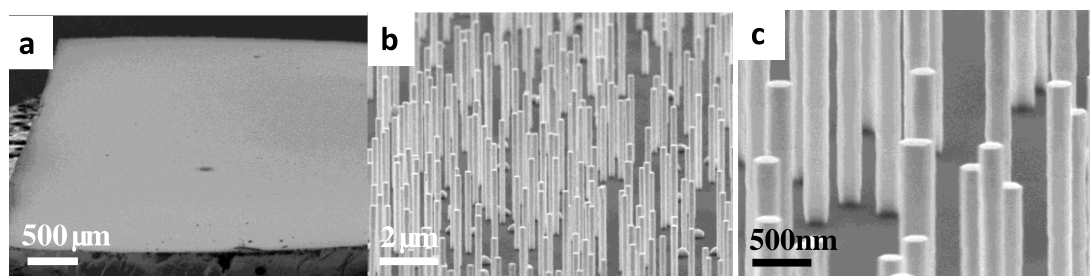


Figure 4.6: SEM images of InAs/InGaAs core-shell nanowires grown on Si (111) substrate (45° tilted view). (b) and (c) are higher magnification images of InAs/InGaAs core/shell nanowires (75° tilted view).

First of all, growth of InAs/InGaAs core/shell nanowires was studied using catalyst-free MOCVD method. InAs nanowire cores were grown under the optimal conditions as described hereinbefore on Si (111) substrates and followed by InGaAs

shell coating by switching on the trimethylgallium (TMG) precursor. Then growth of InGaAs shell was performed at 550 ℃ using precursors including TMG, TMI and AsH_3, with mole fractions of 1.08×10^{-4}, 1.08×10^{-5} and 1.68×10^{-3}, respectively, which are adjusted to yield a nominal indium composition of 9%. Large area growth of InAs/InGaAs core/shell nanowires were achieved on Si wafer. Figure 4.6 (a) shows uniform coverage over almost the entire substrate surface except the very edge. As can be seen in Figure 4.6 (b) and (c), a uniform layer of InGaAs shell was successfully grown on the vertical InAs nanowires, forming InAs/InGaAs core/shell nanowire heterostructure. The growth duration of InGaAs shell was 5 min. The resulting core/shell nanowires have the similar length and uniformly increased diameters compared to InAs nanowire, indicating predominately lateral shell growth. A higher magnification SEM image of Figure 4.6 (c) shows that core-shell nanowires retain the hexagonal cross-section, revealing epitaxial growth of InGaAs shell and catalyst-free nature. The diameter of core/shell nanowires increases linearly with growth time of InGaAs shell, with a radial growth rate of 10.6nm/min under this particular condition.

Secondly, based on InAs/InGaAs core/shell nanowire growth, the InAs/InGaAs/GaAs core/multi-shell nanowires were also investigated. The InAs core and InGaAs shell were grown in succession under the conditions as described above for 300 s and 60 s, respectively. Immediately following InGaAs shell growth, TMI flow was terminated while TMG and AsH_3 flows were retained to initiate GaAs shell

growth. The growth temperature for GaAs shell was 550 ℃ and mole fractions of TMG and AsH_3 were 6.15×10^{-5} and 1.4×10^{-3}, respectively. Figure 4.7 exhibits representative SEM images of as-grown InAs/InGaAs/GaAs core/multi-shell nanowires with 300 s growth of GaAs shell. The resulting nanowires show uniform diameter along the nanowire length, indicating uniform coverage of GaAs shell. Under the above condition, the nanowire diameter increased linearly with growth time, resulting in a GaAs shell growth rate of 7.3 nm/min.

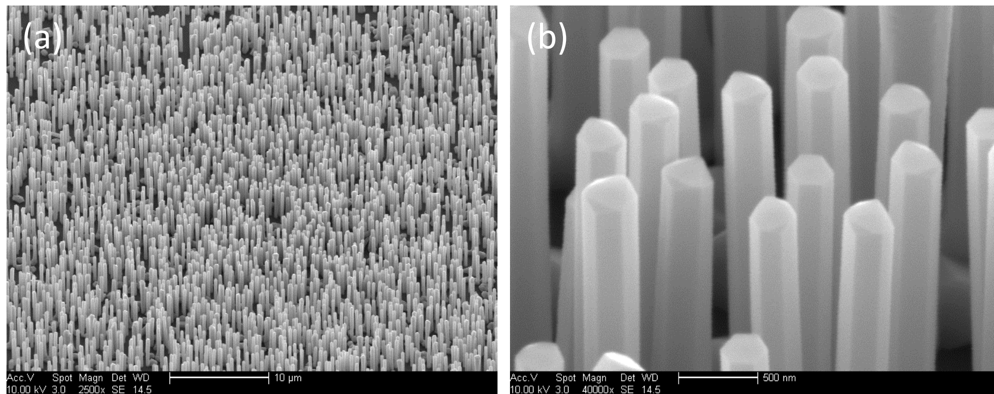


Figure 4.7: SEM images of InAs/InGaAs/GaAs core/multi-shell nanowires (45° tilted view).

Thirdly, following the formation of InAs/InGaAs/GaAs core/multi-shell nanowires, InGaP shell was further deposited by switching the precursors. We used the optimal growth parameters as described above for the growth of 300 s InAs core at 550 ℃, 60 s InGaAs shell at 550 ℃ and 300 s GaAs shell at 550 ℃. Then TMI, TMG and PH_3 were used as precursors for InGaP shell growth, with mole fractions of 1.65×10^{-5}, 1.54×10^{-5} and 3.04×10^{-3}. While InAs nanowire core is unintentionally

n-type doped due to Fermi level pinning and InGaAs and GaAs are nominally undoped, diethylzinc (DeZn) was used as a p-type dopant source for InGaP shell to form a n-i-i-p core/multi-shell nanowire heterostructure. The growth was performed at 550 ℃. The array of as-grown vertically aligned core/multi-shell nanowires was illustrated in Figure 4.8 (a). The nanowires exhibit uniform diameter and hexagonal cross-section, as can be seen in Figure 4.8 (b) and inset in Figure 4.8 (a).

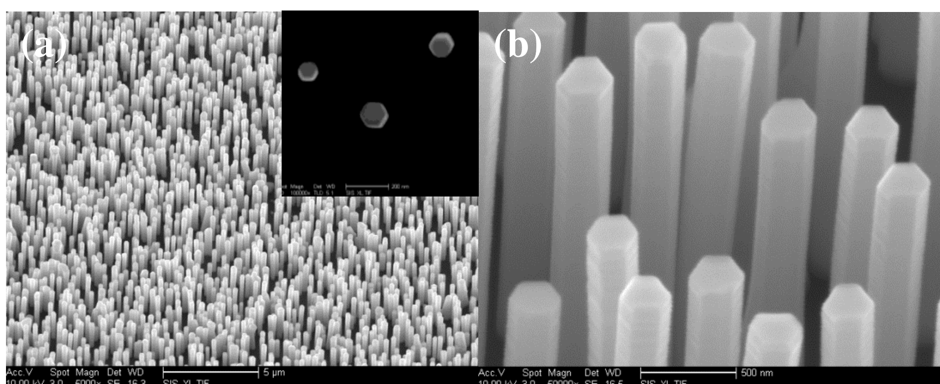


Figure 4.8: (a) and (b) are SEM images of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires at 45 °tilted view. Inset shows the top-view image.

TEM studies were conducted to investigate the crystal structure of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires. The nanowires were grown in succession under the optimal conditions as described above. The growth durations of InAs core, InGaAs, GaAs and InGaP shells are 5 min, 60 s, 60 s and 5 min, respectively. Figure 4.9 (a) illustrates a typical TEM image of an as-grown core/multi-shell nanowire transferred onto carbon coated holey grid. This nanowire has a total diameter of 225 nm. InAs core can be identified by the Moire fringes

pattern in the central region, which results from interference of two relaxed crystal lattices, showing a core diameter of 42 nm. Due to lattice mismatch between InAs core and InGaAs shell, it results in strain between the two materials, and the strain increases with shell thickness. If a critical thickness is exceeded, the shell will laterally relax and misfit dislocation will form.[178-182] The strain relaxation can be seen in the periodic Moire fringes along the nanowire length as illustrate in Figure 4.9 (a). The spacing (L) of Moire fringes can be obtained according to $L=d_1 \times d_2/(d_1-d_2)$, where d_1

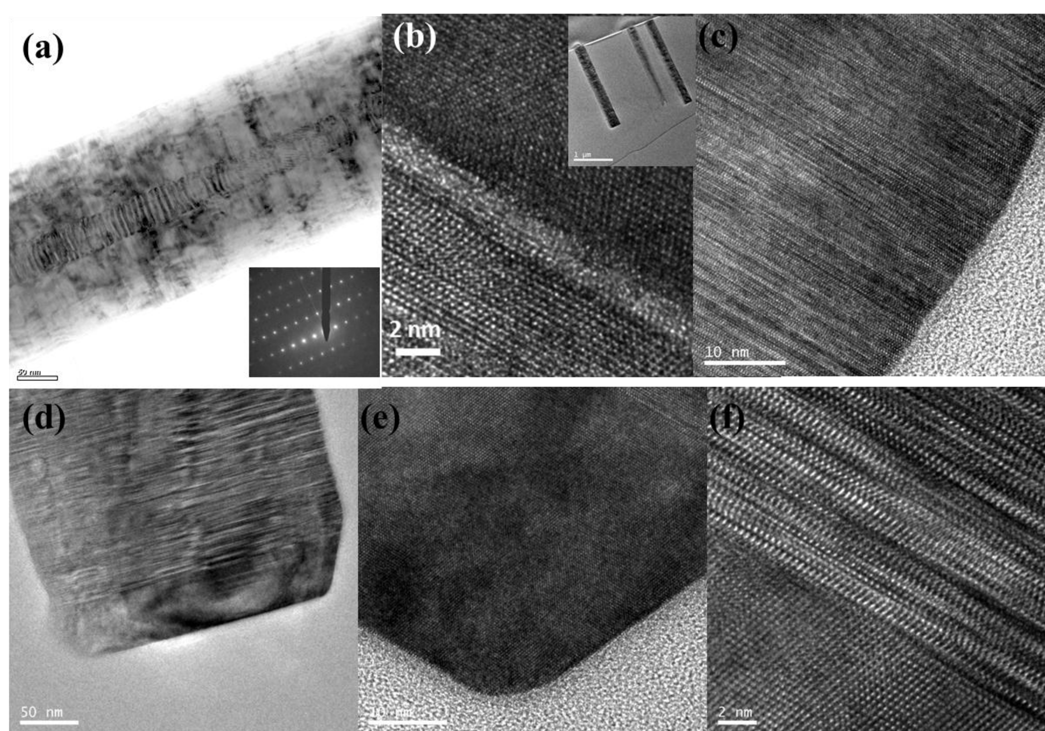


Figure 4.9: TEM images of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires. (a) Low resolution TEM. Electron diffraction pattern along {112} direction is shown in inset. (b) Cross-sectional HRTEM image of nanowire/Si interface. Inset shows a low resolution TEM image of nanowire fully embedded in PMGI. (c) High resolution TEM. (d) and (e) are high resolution TEM images showing the top portion of nanowire. (f) High resolution TEM image of nanowire top, showing interface between InGaP and GaAs.

and d_2 are interplane lattice spacing of the nanowire core and shell, respectively. In our case, d_1 and d_2 are the lattice spacing between (111) plane of InAs core and InGaAs shell. The measured spacing of Moire fringes from TEM images is 5.75-7.05 nm. Using $d_1=6.0583/\sqrt{3}Å=3.4978Å$ for (111) lattice spacing of zinc blende InAs core, the lattice constant of partially relaxed InGaAs shell is calculated to be 5.71-5.77 Å. This observation suggests occurrence of non-uniform partial lattice relaxation, comparing to the lattice constant (5.6897 Å) of InGaAs with nominal 9% indium composition. The outermost layer of InGaP shell is distinguishable in Figure 4.9 (a) as the InGaP shell appears as brighter contrast along the nanowire edge compared to GaAs region, due to smaller atomic mass. The thickness of InGaP shell grown on sidewall is not uniform, with a value of ~51 nm. Although there is a wide distribution of the diameters among different InAs nanowire cores, the thickness of shells on sidewall is quite consistent among different nanowires. No fringes pattern was observed between the InGaP and GaAs interface, as shown in the TEM image of Figure 4.9 (a), indicating that the InGaP outer shell was fairly well lattice matched to GaAs layer. On the contrary, the InGaAs was grown abruptly thus the strain relaxation occurred. The interplane spacing between (111) planes of InGaP shell is 3.3 Å as measured from the HRTEM image (Figure 4.9 (f)), corresponding to a lattice constant of 5.7 Å. This further confirms that the InGaP layer is roughly lattice matched to GaAs layer (lattice constant: 5.65325 Å), with a lattice mismatch of 0.83%. A representative

SAED pattern in the inset of Figure 4.9 (a) shows a zinc blende pattern with beam direction along $[\bar{1}12]$ zone axis. This pattern is not wurtzite pattern along $[\bar{2}110]$ zone axis because the ratio of long to short spot spacing is 1.63 of $[\bar{1}12]$ zinc blende pattern rather than 1.83 of the $[\bar{2}110]$ wurtzite pattern,[170, 183] although the patterns are both rectangular. This result suggest that nanowire core and three shell layers all have zinc blende crystal structure growing along [111] direction. In addition, the inset in Figure 4.9 (a) shows only one set of zinc blende diffraction pattern for the core/multi-shell nanowire system. And no additional double diffraction patterns or spot splitting, which are often seen in nanowire heterostructures,[170, 176] were observed. This is most like due to that three shell layers are roughly lattice matched and lattice mismatch between InAs core and shells is small (6.9% for InAs and GaAs). Therefore, the distances between the spots of the InAs core and shells corresponding to the same hkl plane are visually indistinguishable. And the superposition of diffraction patterns of InAs core and three shells appear as one diffraction pattern. Another possibility is that the InAs core is not detectable because the large diameter.

To further determine the nanowire crystal structure and nanowire/substrate interface characteristics, the cross sectional TEM was also performed. Figure 4.9 (b) inset illustrates the nanowires embedded in PMGI. The III-V core/multi-shell nanowire/substrate interface is similar as interface of InAs nanowire and Si (111) (Figure 4.9 (b)). The InAs core was grown epitaxially on Si (111) with outgrown

shells. There are a large density of twinning planes and stacking faults along the nanowire, as illustrated by the strain contrast in Figure 4.9 (c) of the HRTEM image of nanowire sidewall. On the other hand, the InGaP segment grown axially on top of the nanowire exhibits no visible defect. A similar phenomenon was observed in the VLS grown GaP/GaAsP/GaP core/multi-shell nanowire heterostructure, where a region of GaP outer shell at nanowire top was devoid of stacking faults immediately following the termination of GaAsP layer and the defects was reintroduced within the GaP segment after a length of 200 nm.[184] In our study, one possible explanation for the appearance of the defect-free InGaP segment at nanowire tops is that the InGaP outer shell is roughly lattice matched to the GaAs layer and the segment of InGaP is shorter than the critical thickness above which stacking faults are introduced. Figure 4.9 (e) and (f) illustrate the top region of a core/multi-shell nanowire, showing a defect-free InGaP outer shell with a thickness of 43 nm on nanowire top. This results reveals that the growth rate of InGaP shell on $(1\bar{1}0)$ sidewall surface is slightly higher than that on (111) nanowire top surface.

4.4 Transport Properties of Single InAs Nanowire

The electrical properties of the InAs nanowires were characterized by single nanowire back-gated field-effect transistor (FET) measurements.[185, 186] To fabricate single nanowire FET, InAs nanowires were dispersed in isopropanol alcohol (IPA)

using ultrasonication. Then the nanowires were horizontally transferred onto Si substrate with 600 nm thermally grown SiO_2 by applying a few drops of the solution on the surface. E-beam lithography followed by lift-off metallization was performed to deposit metal electrodes (Ti/Au) on two ends of the nanowires. The I_{ds}-V_{ds} and I_{ds}-V_{gs} curves and SEM images of a typical device are shown in Figure 4.10 and the insets. Ohmic contacts were formed between the nanowires and the electrodes. The InAs nanowires exhibited typical n-type FET behavior. The average resistivity, electron mobility and concentration was calculated to be 1.5×10^{-3} Ω·cm, ~1,000 cm^2/V s and 10^{18}-10^{19} cm^{-3}, respectively.[185, 186] These values are comparable to those of InAs nanowires grown using catalytic VLS growth.[187]

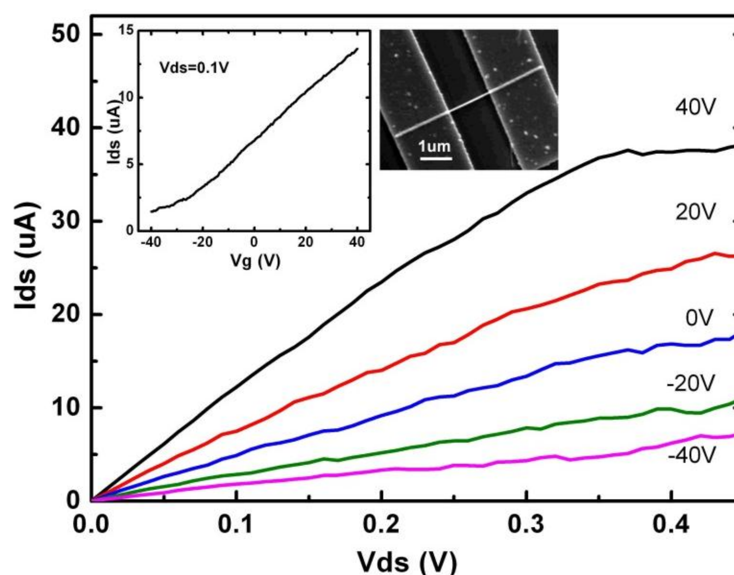


Figure 4.10: Ids-Vds measurements of a single InAs nanowire FET using a bottom-gate structure; inset is the Ids-Vgs curve and a SEM image of the device.

4.5 III-V Core/multi-shell Nanowire Solar Cells

For solar cells, it requires a built-in potential, which is typically created by a p-n junction or a p-i-n junction, to facilitate the separation of photo-generated carriers. In this work, the InAs core was unintentionally n-type doped. The InGaAs and GaAs shells were nominally intrinsic. And the InGaP outer shell was doped using DeZn during growth. To verify the formation of diode and characterize the electrical properties of the core/multi-shell nanowires, I-V measurements were carried out on a single nanowire device. Fabrication of single core/multi-shell nanowire devices is similar to the process of fabricating nanowire FETs as described in the previous section. The as-grown InAs/InGaAs/GaAs/InGaP core/multi-shell nanowires were dispersed in IPA using ultrasonication. Then the nanowires were horizontally transferred onto Si substrate with 600 nm thermal SiO_2, followed by patterning of metal electrodes (Ti/Au) on the two ends of nanowires using E-beam lithography and lift-off metallization.

Figure 4.11 exhibits a typical I-V curve of the single core/multi-shell nanowire, inset illustrating a SEM image of the device. The I-V curve shows clearly rectifying behavior with a ratio of 36 at $\pm$0.5V. As the InAs core is unintentionally n-type doped, this curve indicates successfully doping of p-type InGaP outer shell. The rectifying ratio is underestimated since one electrode is in contact with shell only while the other connected to core and shells, forming a current leakage route through the shell.

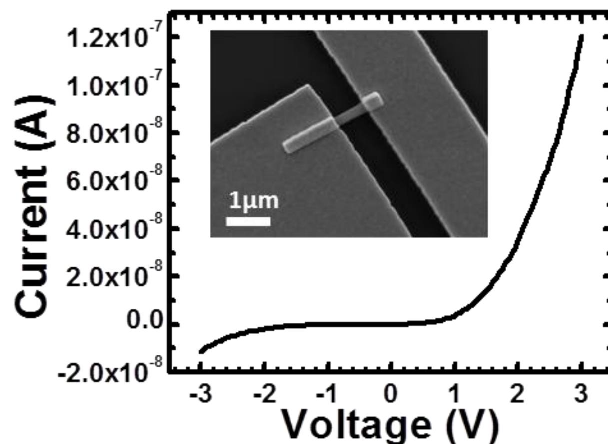


Figure 4.11: I-V measurement of a single InAs(n)/InGaAs/GaAs/InGaP(p) core/multi-shell nanowire diode. Inset is a SEM image of the single nanowire device.

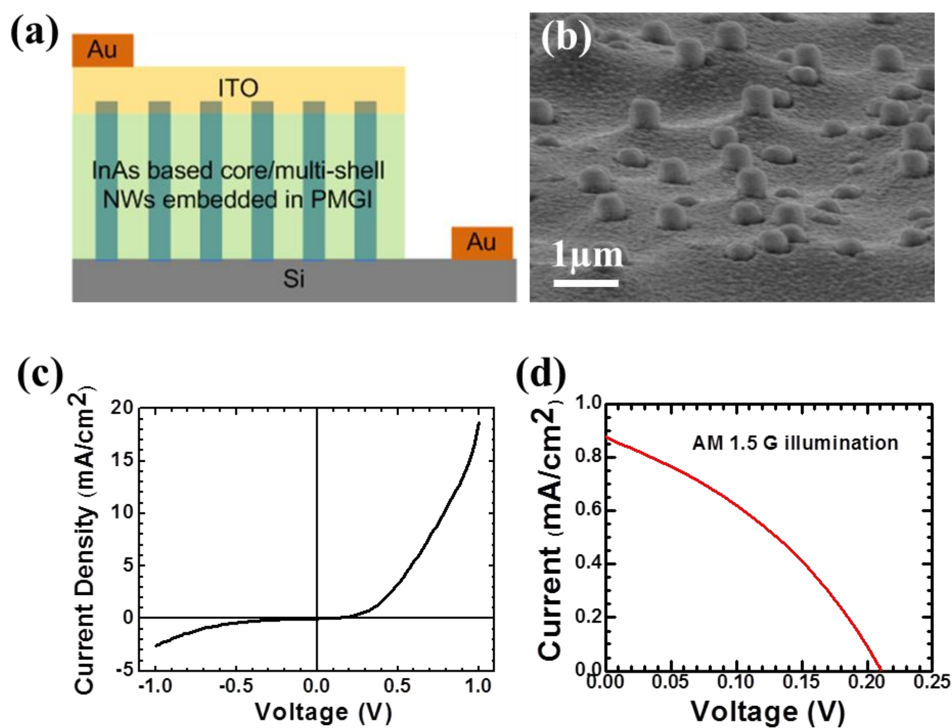


Figure 4.12: (a) Schematic of InAs/InGaAs/GaAs/InGaP core/multi-shell nanowire solar cell. (b) A SEM image of front surface of the device with ITO front contact. I-V measurement of InAs(n)/InGaAs/GaAs/InGaP(p) nanowire solar cell (c) under dark, and (d) with AM 1.5G illumination (100 mW/cm^2).

Figure 4.12 (a) illustrates the schematic of the InAs/InGaAs/GaAs/InGaP core/multi-shell nanowire solar cells. To fabricate the solar cell, the core/multi-shell nanowire array was embedded in transparent PMGI polymer by spin-coating after solvents cleaning. Oxygen RIE etching were employed to remove excess polymer to expose nanowire tips, followed by sputtering of ITO as top contact and deposition of Au on the Si substrate as bottom electrode.

The fabricated core/multi-shell nanowire solar cells were characterized using I-V measurements under dark and with AM 1.5G illumination, and the results are shown in Figure 4.12 (c) and (d). The formation of p-n junction was confirmed by the dark I-V curve, as shown in Figure 4.12 (c). The rectifying ratio was calculated to be 39 at ±1 V bias. When upon AM 1.5G illumination (100 mW/cm^2), the device showed clear photovoltaic effect. This core/multi-shell nanowire solar cell showed a short-circuit current density of 0.87 mA/cm^2, an open-circuit voltage of 0.23V, a fill factor of 0.33 and a power conversion efficiency of 0.066%. The efficiency of our nanowire devices was much smaller than the conventional planar III-V solar cells as they were not optimized. There are many parameters needed to be tuned to achieve optimal device performance, similar to what we did for Si radial junction nanowire solar cells. For example, passivation of surface states is essential to reduce the surface recombination rate. In addition, the doping concentrations and thicknesses of nanowire core and shells need to be optimized to suppress Auger recombination as well as

surface recombination. Moreover, further investigation is required to achieve catalyst-free growth of defect-free and pure phase III-V nanowires. The crystal structural property is a parameter of significant importance for electrical properties of III-V nanowires. It has been demonstrated both theoretically and experimentally that twinning and stacking faults act as scattering centers for charge carriers[188-191] and phonons.[192] Mixed wurtzite and zinc blende crystal structure can even affect the energy band structure.[193] For example, thin wurtzite segments inserted in a Zinc blende nanowire could result in a superlattice and give rise to minibands for the electrons and holes.

4.6 Conclusion

In conclusion, we have presented a catalyst-free MOCVD method to grow InAs nanowires and InAs based core/multi-shell nanowire heterostructures in a well-controlled and scalable manner. An optimal surface treatment and growth condition for high quality vertical InAs nanowires has been developed. The systematic study on the surface preparation and growth parameters leads to an optimal growth method of high quality vertical InAs nanowires and reveals mechanism of the catalyst-free growth. The optimal growth was achieved by BOE etch and DIW rinsing to form oxide patches on the surface, so that InAs can nucleate at the oxide-free regions while the oxide patches hinder the formation of large InAs islands to facilitate

the nanowire growth. The uniform InAs nanowires have a zinc blende single crystal structure and grow along the <111> direction with no measurable tapering. Cross sectional TEM study shows the interfere properties and reveals the epitaxial nature of the InAs nanowire growth on Si. The InAs based core/multi-shell nanowire heterostructure was successfully fabricated, which offers the flexibility to tailor the band structure of the materials to acquire desired electrical and optical properties. In addition, this radial junction nanowire heterostructure provides high carrier collection efficiency by orthogonalizing the directions of carrier collection and light absorption pathways. The core/multi-shell nanowire based solar cells has been demonstrated although further optimization of the devices is required. Thus, this research demonstrates direct and contamination-free integration of InAs based nanowire heterostructure with Si for photovoltaic application.

Chapter 4, in part, has been accepted for publication in The Journal of Physical Chemistry C, 2013. Yi Jing, Xinyu Bao, Wei Wei, Chun Li, Ke Sun, David Aplin, Yong Ding, Zhong-Lin Wang, Yoshio Bando, and Deli Wang, “Catalyst-free heteroepitaxial MOCVD growth of InAs nanowires on Si substrates”. The dissertation author was the primary investigator and author of this paper.

Chapter 5: Conclusion

5.1 Conclusion

In this dissertation, the development, fabrication and characterization of semiconductor nanowire, particularly Si and III-V nanowires, and their applications for optoelectronics, renewable energy and retinal prosthesis has been demonstrated. The Si nanowires were created using either chemical wet etching or ICP/RIE dry etch. Patterning techniques including E-beam lithography and nanoimprint lithography were used to define the size, location and distribution of Si nanowire array. In the case of III-V nanowires, a catalyst-free MOCVD has been developed to create the vertical nanowires and core/multi-shell nanowire heterostructure.

First, the Si nanowire photodetectors were discussed. Using a crossbar structure, an individually addressable vertical 8×8 Si nanowire photoconductor array was demonstrated. This device showed potential application for high-detectivity and small pixel image sensor. In addition, Si axial and radial junction nanowire photodiode were developed and characterized. These nanowire devices exhibited good photo response in visible wavelength and could be used to replace dysfunctional photo receptors in human retina for applications in retinal prosthesis.

Second, the Si nanowire solar cells were studied. A large-scale vertically

aligned Si nanowire array has been fabricated using a cost-effect chemical etching method. This nanowire array was utilized as light absorber to improve the light absorption of planar solar cells. The device with nanowire absorber exhibited over one magnitude higher efficiency than its planar counterpart. Furthermore, a systematic study on the design, develop and optimization of the Si radial junction nanowire solar cells was demonstrated. The Si nanowires were created using nanoimprint lithography and ICP/RIE etching. A well-controlled nanoscale doping process was developed to create the radial junction nanowire structure. A variety of parameters were studied and optimized to achieve optimal device performance. It has been shown that the nanowire core is required to be moderately doped to avoid fully depletion of nanowire core. The methods to reduce the Auger and surface recombination rates were also discussed.

Third, III-V core/multi-shell nanowire solar cells were investigated as well. A catalyst-free approach for heterogeneous integration of InAs nanowires and radial junction nanowire heterostructures were achieved. By a systematic study with the focus on varying the surface preparation and growth parameters, an optimal surface treatment and growth condition for high quality vertical InAs nanowires was achieved and an explanation of growth mechanism was proposed. The InAs based core/multi-shell nanowire heterostructure were successfully fabricated, which provides a shorter carrier collection path for enhanced collection efficiency and offers the flexibility to tailor the band structure of the materials for desired electrical and

photonic properties.

5.2 Future work

Based on the results obtained in this dissertation, there are research challenges that may be further exploited to improve the device performance and enhance the functionality.

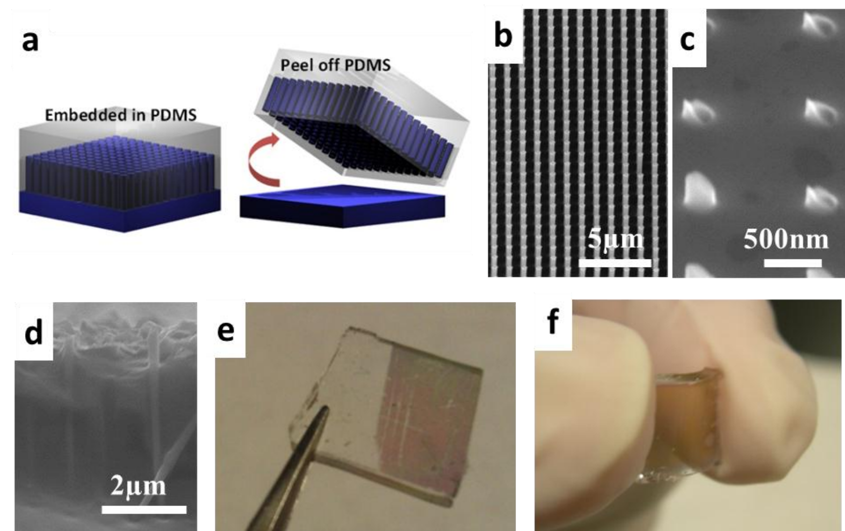


Figure 5.1: (a) Schematic of PDMS transfer process. (b) A SEM image of as-etched Si nanowire array at 45^0 tilted view. (c) A SEM image of Si substrate after peeling off the PDMS film. (d) A cross sectional SEM image of Si nanowires embedded in PDMS film. (e) and (f) show the optical images of PDMS films with embedded Si and InAs nanowire arrays, respectively.

Development of mechanically flexible electronic and optoelectronic devices is essential for applications in next-generation display, wearable electronics and medical devices. For instance, it is important to implement a flexible photodetector array to conform curvature of the retina for retinal prosthesis. In this work, preliminary result

of flexible Si and InAs nanowire arrays has been demonstrated by casting PDMS onto nanowire samples and peeling off PDMS film after curing. The PDMS elastomer was first mixed with the curing agent in a weight ratio of 10:1. Then the PDMS mixture was casted onto vertical nanowire arrays and degassed in a vacuum desiccator (Figure 5.1 (a)). Followed curing at 100 ℃ for 30 min, the PDMS film with embedded nanowires was removed from the substrate by either peeling or inserting a razor blade. The PDMS film with embedded nanowires shows good flexibility, as illustrated in Figure 5.1 (f). This method is generic and applicable to other materials. Further investigation is required to fabricate flexible function optoelectronic devices.

The III-V core/multi-shell nanowire solar cells were introduced but the optimization of device remains challenging. Further research efforts on catalyst-free growth conditions are required to reduce the twinnings and stacking faults which act as scattering centers for charge carriers[188-191]. The doping concentrations and thicknesses of each layer of this core/multi-shell nanowire heterostructure need to be optimized as well to reduce recombination rates.

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