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Algorithms and Architectures of Energy-Efficient Error-Resilient MIMO Detectors for Memory-Dominated Wireless Communication Systems

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Abstract—In a broadband MIMO-OFDM wireless communication system, embedded buffering memories occupy a large portion of the chip area and a significant amount of power consumption. Due to process variations of advanced CMOS technologies, it becomes both challenging and costly to maintain perfectly functioning memories under all anticipated operating conditions. Thus, Voltage over Scaling (VoS) has emerged as a means to achieve energy efficient systems resulting in a tradeoff between energy efficiency and reliability. In this paper we present the algorithm and VLSI architecture of a novel error-resilient K-Best MIMO detector based on the combined distribution of channel noise and induced errors due to VoS. The simulation results show that, compared with a conventional MIMO detector design, the proposed algorithm provides up-to 4.5 dB gain to achieve the near-optimal Packet Error Rate (PER) performance in the 4×4 64-QAM system. Furthermore, based on experimental results, when jointly considering the detector and memory power consumption, the proposed resilient scheme with VoS memory can achieve up to 32.64% savings compared to the conventional K-Best detector with perfect memory.

Index Terms—MIMO detector, MIMO OFDM, SRAM, VLSI, voltage over scaling, wireless communication.

I. INTRODUCTION

MULTI-INPUT multi-output, orthogonal frequency division multiplexing (MIMO-OFDM) is widely recognized as a key technology for modern broadband wireless communication systems such as LTE-Advanced as well as advanced wireless LAN 802.11ac and 802.11ad. With the growing size of system bandwidth (through carrier aggregation) and the number of antennas at both transmit and receive sides, large buffering memories are a prominent requirement for emerging systems to support

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vector operations such as fast fourier transform (FFT), two-dimensional channel estimation, MIMO detection, and hybrid automatic repeat request (HARQ). Moreover, miniaturization of semiconductor components facilitates the integration of large buffering memories into Systems on Chip (SoC). As an example, a digital baseband platform for a Software Defined Radio (SDR) is presented in [1] where the reported memory area is 8.7 Mbits (approximately 50% of total chip area). Not only do embedded buffering memories occupy a significant portion of the chip area but also a large percentage of the power consumption. According to the International Technology Roadmap for Semiconductors (ITRS) report [2], embedded memories are predicted to consume approximately 50% of power consumption for modern SoCs. On the other hand, due to the effects of process variations and reliability issues in advanced CMOS technology, maintaining perfectly functional memories under all operating conditions results in excessive design margining and extra power overhead. Therefore, reducing the power consumed by embedded memories is paramount to achieve energy-efficient mobile wireless communication systems.

Recently, Voltage over Scaling (VoS) was demonstrated as an effective technique to reduce power consumption of embedded memories by a significant amount [3], [4]. However, reducing the supply voltage of the buffering memories using VoS results in spatially uniform random errors which corrupt the stored data. These introduced errors are controlled by the amount of voltage reduction and are referred to as “parametric memory errors.” Thus, realizing an energy efficient system through the VoS technique comes at the cost of degrading signal quality. However, it is important to realize that a wireless communication system is inherently fault tolerant, as it is designed to handle data that is corrupted by channel artifacts (noise and interference). Since unreliable buffering memories introduce extra “parametric errors” to the system, the adoption of additional fault-tolerant signal processing techniques is required to guarantee negligible system performance degradation [5], [6].

In [7], a unified model that combines the statistics of data from the wireless channel and the distribution of parametric errors due to VoS was derived for SISO systems. In addition, in [8], a modified Viterbi decoder for single antenna systems under AWGN channel was presented where it utilizes statistical knowledge of both channel and memory noise. Furthermore, in [9], a statistical distribution that represents both the noise due to the wireless MIMO channel and the disturbances introduced by

parametric memory errors was presented. The effect of this new distribution on the signal detection performance of the MIMO receiver was illustrated and an approach that can recover the transmitted symbols was introduced. The algorithm described therein leads to a near-optimal BER performance with 40% to 50% of memory power savings.

Moreover, relevant works considering error-resilient or error-tolerant systems have been published in the literature. In [28] and [29], the effect of faulty memory on BER performance in MIMO-BICM systems is investigated. In [30] many different families of error-resilient FEC decoders such as Turbo decoders as well as Low Density Parity Codes (LDPC) are presented while in [31]–[33], studies concerning Turbo equalizations and Turbo code decoders are reported. In particular, [31] and [32] considers unreliable memories in Turbo decoder subsystems. The effect of memory errors on BER performance is analyzed and modifications of decoder schemes are proposed to compensate for the performance degradation. In addition, a similar approach is applied to the turbo equalization of inter-symbol interference (ISI) channels and reported in [33]. Designs of LDPC decoders that can compensate for memory errors are described in [34] and [35], while structures of Viterbi decoder that can mitigate timing errors in constituent circuits is proposed in [36]. Finally, authors of [37] investigate the impact of unreliable memories on general DSP systems and propose error-resilient data-representation methods and in [38] provide an overview of existing techniques for cross layer error resilience in general and for wireless systems in particular.

In this paper, we present a novel low-complexity algorithm and the corresponding VLSI architecture that can optimally perform MIMO detection in the presence of channel noise and hardware errors. The proposed algorithm is based on a novel child node enumeration strategy during the tree searching and can greatly reduce the search space compared with the approach presented in [9]. Moreover, the VLSI architecture of the proposed algorithm is presented. The optimization methods utilized to further reduce the complexity of the detector are presented. The detector is synthesized, placed and routed to confirm the validity and efficiency of the proposed design. In particular, the main contributions of the paper can be considered as follows

- A low-complexity algorithm to recover the transmitted symbols in the presence of channel noise and hardware errors is presented. The proposed “two-way sorting” approach can achieve a close-to optimal Packet Error Rate (PER) performance, while benefiting from the reduced power consumption due to memory VoS.
- The VLSI architecture for the proposed error-resilient detection algorithm is presented for a 4×4 MIMO system with 16-QAM and 64-QAM modulation schemes. The approaches that are employed to further reduce the hardware complexity are presented.
- The proposed MIMO detector is synthesized, placed, routed, extracted and simulated. The quantified results for benchmarking the performance and complexity are presented. Furthermore, detailed comparisons with conventional approaches are given.
- Complexity and power consumption analysis for memory sub-block and entire system are presented. The results verify that the proposed algorithm and architecture is a

promising approach to achieve an energy-efficient wireless communication system.

The paper is organized as follows. A review of the mathematical model for the distribution of the received signal after the buffering memory and memory error aware ML MIMO detection are presented in Section II. The proposed low-complexity *two-way sorting* algorithm is presented in Section III. Simulation results are presented in Section IV, while the VLSI architecture and complexity reduction techniques are presented in Section V. Implementation results and complexity analysis are given in Section VI. Finally, the paper is concluded in Section VII.

II. REVIEW OF MEMORY ERROR AWARE MIMO DETECTION

In MIMO systems, unreliable embedded buffering memories corrupt received data by introducing spatially distributed uniform random errors controlled by the amount of voltage reduction [7]. In this section, the resultant distribution of the data after faulty memories will be briefly reviewed and the modified MIMO detector algorithm will be revisited. Interested readers can refer to [7] and [9] for more detailed discussions and comprehensive derivations.

A. Joint Distribution of Channel and Memory Error

In a MIMO system with N_T transmit antennas and N_R receive antennas, the transmitted signal vector $\tilde{\mathbf{s}}$ contains N_T symbols that are mapped independently from the constellation of a modulation scheme. Hence the N_R -dimensional received signal vector $\tilde{\mathbf{x}}$ is given by

$$\tilde{\mathbf{x}} = \tilde{\mathbf{H}}\tilde{\mathbf{s}} + \tilde{\mathbf{n}} \quad (1)$$

assuming $\tilde{\mathbf{n}}$ represents the i.i.d complex Gaussian random vector with zero mean and $\sigma^2\mathbf{I}$ covariance matrix and $\tilde{\mathbf{H}}$ is the channel matrix. The preceding MIMO equation can be decomposed into real-valued numbers¹ [18] as follows

$$\mathbf{x} = \mathbf{H}\mathbf{s} + \mathbf{n} \quad (2)$$

The received signal vectors \mathbf{x} are usually stored in an embedded buffering memory preceding the MIMO detector and represented in the form of two's complement. In this memory, each word consists of N bits; d bits for the integer part and r bits for the fractional part, where $N = d + r$. When applying reduced supply voltage (V_{dd}) to the memory, errors affect stored data in the form of bit flips where the probability of having k bit flips simultaneously is given by

$$P(k) = P_e^k(1 - P_e)^{N-k} \quad (3)$$

and $P_e = P_e(V_{dd})$ the error rate in memory due to VoS. Typically, the data read from memories could have one or more bit flips. It has been shown in [7] that the case of one-bit flip is the dominant factor in the distribution of the data read from the faulty memories, since the error rate in the memory, P_e , is typically very small [10]. Thus the probability of having two or more erroneous levels simultaneously is extremely small. As a result, the received signal vector retrieved from the faulty memory (\mathbf{y})

¹Real-value decomposition of the channel matrix is not compulsory. Its major advantage is to create real-number operations instead of complex-number operations to simplify hardware implementations.

is either error free or has only one bit-flip at only one of the elements (y_i). In addition, one-bit flip errors in the least significant bits (LSBs) are less severe than those in the most significant bits (MSBs), and thus the distribution of the faulty data can be further simplified by considering bit flips in the integer part only. Based on that assumption, the retrieved data distribution has been derived in [9] and is given by

$$\log [f_{\mathbf{Y}|\mathbf{s}}(y|\mathbf{s})] = \log \left\{ e^{\frac{\log c_0 - \|\mathbf{y} - \mathbf{H}\mathbf{s}\|^2}{\sigma^2}} + \sum_{j=1}^{2N_T} \sum_{n=d}^{N-1} e^{\frac{\log c_1 - \|\mathbf{y} - \mathbf{H}\mathbf{s} \pm 2^{n_j-r} I_j\|^2}{\sigma^2}} \right\} \quad (4)$$

where

$$\log c_0 = \sigma^2 \log \frac{P_0^{2N_T}}{(\pi\sigma^2)^{N_T}}, \quad \log c_1 = \sigma^2 \log \frac{P_1 P_0^{2N_T-1}}{(\pi\sigma^2)^{N_T}}$$

And I_j is a vector of 1 at the j th element and 0 otherwise, and

$$P_0 = P(0) = (1 - P_e)^N \quad (5)$$

$$P_1 = P(1) = P_e(1 - P_e)^{N-1} \quad (6)$$

B. Modified Maximum-Likelihood Detection

It has been shown that the Maximum Likelihood (ML) detection can achieve optimal BER performance and its realization can be transformed into a tree-searching scheme where the tree nodes represent the set of modulation points [11], [12], [17]–[20]. However, the conventional ML detector assumes Gaussian distribution for the received symbol vector and, due to the hardware errors introduced by the buffering memory; this is no longer valid for the signal that is read from a faulty memory. Therefore, the ML criterion has to be modified based on the new distribution. Utilizing the joint distribution derived in (4), the ML symbol is given by

$$S_{ML} = \arg \max_{s \in \mathbb{S}} \log [f_{\mathbf{Y}|\mathbf{S}}(y|\mathbf{s})] \quad (7)$$

Based on the max-log approximation [39], and by applying the QR decomposition of the channel matrix $\mathbf{H} = \mathbf{Q}\mathbf{R}$, \mathbf{s}_{ML} can be expressed as

$$S_{ML} = \arg \min_{s \in \mathbb{S}} (\|\hat{\mathbf{y}} - \mathbf{R}\mathbf{s}\|^2 - \log c_0, \|\hat{\mathbf{y}} - \mathbf{R}\mathbf{s} \pm \hat{e}_{j,n}\|^2 - \log c_1) \quad (8)$$

where

$$\hat{\mathbf{y}} = \mathbf{Q}^H \mathbf{y}, \quad \hat{e}_{j,n} = \mathbf{Q}^H e_{j,n}$$

and

$$j = 1, 2, \dots, 2N_T, \quad n = d, d+1, \dots, N-1 \\ e_{j,n} = 2^{n_j-r} I_j$$

Therefore, the new path metric d_i for level i in the tree structure can be represented as follows

$$d_i = \left| \hat{\mathbf{y}}_i - \sum_{i=j}^{2N_T} \mathbf{R}_{ij} s_j \pm e_i \right|^2 - \log c_{0/1} \quad (9)$$

where

$$e_i = \begin{cases} 0 & \text{error free} \\ \hat{e}_{i,n} & \text{erroneous terms} \end{cases}$$

This results in a new path metric enumeration in the tree structure where the path metric d_i considers either one bit flip at any one of the integer bit positions (i.e., $\hat{e}_{i,n}$ and $\log c_1$) or no error (i.e., $e_i = 0$ and $\log c_0$).

III. ERROR-RESILIENT DETECTION ALGORITHM

An error-resilient MIMO detection algorithm that can support a 4×4 MIMO system with 16-QAM modulation was designed and presented in [9]. Both hard output and soft output scheme share the main part of the architecture with minor differences. Several complexity-reduction techniques have also been discussed therein. However, from the VLSI architectural point of view, the approach proposed in [9] could still result in degraded throughput and high complexity as compared to the conventional K-Best architectures. In this work, we will present a low-complexity algorithm that is more suitable for VLSI architecture design and can achieve close-to optimal PER performance in the presence of joint channel noise and hardware error.

A. Two-Way Sorting

One of the main reasons that the approach presented in [9] contains high complexity lies in the fact that it employs an exhaustive enumeration for the child nodes. In other words, while expanding the tree nodes, it considers all the candidates resulting from either the error-free scenario or all possible combinations of error terms. This results in an excessively expanded tree dimension and significantly increased computation overhead. Although a complexity-reduction technique based on the concept of “learning” was utilized in [9], the resulting complexity can still be further decreased.

Based on the observation that only one branch (among the error-free and all of the erroneous terms) associated with a certain QAM symbol needs to be expanded; in this section, we propose a novel node-enumeration strategy that does not require the computation of all the distances of erroneous branches. This idea can be explained through an example of 16-QAM modulation shown in Fig. 2. Assuming 16-QAM modulation with the real-value decomposition, the parent node at level i can possibly expand to four children at level $i-1$. However, by considering the scenario of only one bit flip at the MSB (which could result into positive or negative errors), four more children per each error scenario needs to be examined. Furthermore, considering the other single-bit flips at the remaining integer bits will significantly increase the number of child nodes being examined and branch distances being calculated. This will result into an explosion of the computation complexity. However, considering the fact that only one distance should be associated with each one of the four children, it can be argued that, for each QAM symbol, only the branch with the minimum distance should be valid and needs to be saved. Referring to the example shown in Fig. 2, only the smallest distance out of the three distances for any given modulation symbol is selected. When applying this idea to a K-Best scheme [12], [18], a concept of two-step (way) sorting is proposed. The first step is per parent node, for



Fig. 1. A simplified MIMO system.

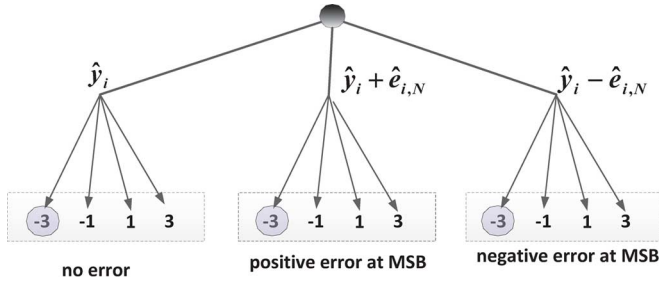


Fig. 2. Tree structure with erroneous children nodes using 16-QAM.

each symbol in the QAM scheme, to identify the one with minimum branch metric considering both error-free term and all of the erroneous terms. The second one is the typical sorting of the best K survivors out of all of the candidate child nodes. In the sequel, we will present an efficient algorithm to realize this *two-way* sorting.

Considering the scenario of one-bit flip at any of the d bits of the integer part, there exist $2d$ possible errors. Therefore for the candidate child of the QAM symbol, only the smallest distance out of the $2d + 1$ distances ($2d$ erroneous distances and one error-free distance) should be selected. Hypothetically, we divide these distances into two groups; error-free group containing only the distance of the child assuming no bit flips; and erroneous group containing the other distances. First, the proposed *two-way sorting* algorithm estimates the error that results in the minimum distance out of the erroneous group, without the need of computing all the distances. Then, it compares both distances (error-free distance and the minimum distance of the erroneous group) and selects the minimum. Given the definition of W_i shown in (10):

$$W_i = \hat{y}_i - \sum_{i=j}^{2N_T} R_{ij}s_j \quad (10)$$

the branch distance in (9) could be rewritten as

$$d_i = (W_i \pm e_i)^2 - \log c_i \quad (11)$$

This distance can be expanded as:

$$d_i = \begin{cases} W_i^2 - \log c_0, & \text{error free} \\ W_i^2 \pm 2W_i \times e_i + e_i^2 - \log c_1, & \text{erroneous terms} \end{cases} \quad (12)$$

So, considering the erroneous group, the minimum distance d_i associated with a certain symbol should be given as

$$d_i = \min_{e_i, e_i \neq 0} (W_i^2 \pm 2W_i \times e_i + e_i^2 - \log c_1) \quad (13)$$

where e_i represents the different possible error values of the equivalent bit flips. Since W_i^2 is a common term in all the distances, the distance could be written as:

$$d_i = W_i^2 + \min_{e_i, e_i \neq 0} (e_i^2 \pm 2W_i \times e_i - \log c_1) \quad (14)$$

Based on the sign of the metric W_i , the errors terms having the same sign of W_i give larger distances than these having the opposite sign. Therefore half of the error terms could be removed resulting in the following criterion:

$$d_i = W_i^2 + \min_{e_i, e_i \neq 0} (e_i^2 - 2|W_i| \times e_i - \log c_1) \quad (15)$$

Thus, the optimum value of the error \hat{e}_i which minimizes the distance of the erroneous terms can be given as:

$$\hat{e}_i = \arg \min_{e_i, e_i \neq 0} |e_i - |W_i|| \quad (16)$$

This means that we choose the error value that is closest to $|W_i|$. Hence, the minimum distance is either one of the following two distances:

$$d_i = \min (W_i^2 - \log c_0, (W_i - \hat{e}_i)^2 - \log c_1) \quad (17)$$

B. First Norm

A well-known method to reduce the hardware complexity of the branch distance calculation is to use the first norm (l^1), absolute value, instead of the second norm (l^2) [17]. Thus, the approximated distance can be obtained by replacing the squaring operation in (9) by the absolute value. This is shown in (18).

$$d_i \approx \left| \hat{y}_i - \sum_{i=j}^{2N_T} R_{ij}s_j \pm e_i \right| - \log c_{0/1} \quad (18)$$

Therefore, by using the definition of W_i in (10), the branch distances for both error-free and erroneous scenario are given by:

$$d_i \approx \begin{cases} |W_i| - \log c_0, & \text{error free} \\ |W_i \pm e_i| - \log c_1, & \text{erroneous} \end{cases} \quad (19)$$

By considering the erroneous group, the minimum distance d_i associated with a certain symbol should be given as

$$d_i = \min_{e_i, e_i \neq 0} (|W_i \pm e_i| - \log c_1) \quad (20)$$

In a similar manner, error terms which have the same sign as W_i can be excluded from the minimum comparison. Hence, the minimum distance can be expressed as:

$$d_i = \min_{e_i, e_i \neq 0} (||W_i| - e_i| - \log c_1) \quad (21)$$

It is obvious that the optimal error value that could result into the minimum distance is the one closest to $|W_i|$ which can be expressed similar to (16). Hence, the two distances should be compared to find the minimum one as given by (22).

$$d_i = \min \begin{cases} |W_i| - \log c_0, & \text{error - free} \\ ||W_i| - \hat{e}_i| - \log c_1, & \text{erroneous} \end{cases} \quad (22)$$

C. Comparing With the "Learning" Concept

In [9], the basic method for complexity reduction is based on learning the defect map. A defect map is a small memory inside the search engine that gives information about the errors in the buffering memory. For each supply voltage of the buffering memory, a learning operation is performed to set or reset the corresponding bit for the received vector which is stored in the faulty buffering memory. Logic "1" means that an error exists

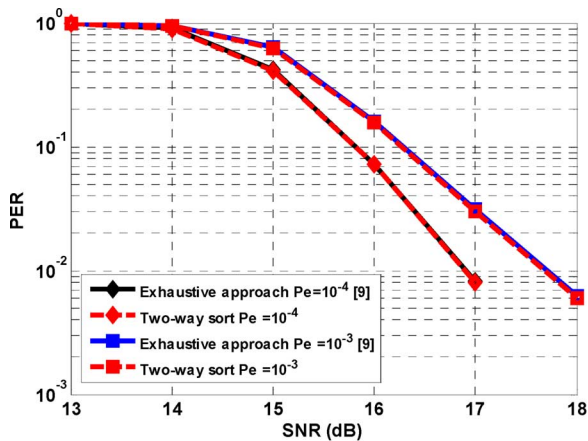


Fig. 3. PER comparisons between Two-way sorting and exhaustive method [9] using l^2 -norm.

in the integer bit of any of the elements of the received vector, while “0” means that the corresponding memory storage where the received vector is stored is error-free. After building the defect map, the K-Best algorithm checks the defect map to figure out if there is a need to check the erroneous branches or not. It has been shown by simulations in [9] that the learning-based defect map reduces the search complexity drastically. However, this technique suffers from the following disadvantages: 1) the average number of searched nodes is variable and depends on the memory error rate. Hence, the K-Best MIMO detector has a variable throughput depending on memory error rates, 2) it requires extra hardware complexity where several defect maps are required for different distinct values of memory supply voltages, and 3) training is required periodically to update the defect map with temperature and environment variations which reduces the system throughput.

On the other hand, the proposed *two-way sorting* alleviates all the preceding disadvantages of the learning-based defect map approach, since the proposed algorithm always considers different error scenarios at each level of the tree and there is no need for a defect map or learning in that sense. As a matter of fact, the proposed approach is implicitly in an “always-learning” mode. Another advantage is the relaxed sorting since the first step of sorting chooses only one candidate among of all erroneous and error free candidates. Then, any sorting algorithm can be applied for the candidates at each layer. Furthermore, the *two-way sorting* requires a much reduced number of registers to save intermediate results as compared to the learning-based approach in [9].

IV. SIMULATION RESULTS

In this section, performance results of the proposed *two-way sorting* algorithm are first compared against the algorithm in [9]. Then, based on first norm and second norm schemes, the PER simulation results of the proposed error-resilient MIMO detection algorithm is presented and compared against the conventional MIMO detector. All simulation results are based on soft-decision decoding.

We considered the same simulation setup as in [9], which is a 4×4 MIMO-OFDM system with 16-QAM and 64-QAM modulation schemes in an LTE channel environment. A group of

1700 packets with 15 OFDM symbols per packet and 512 subcarriers per symbol was used for the simulation. In addition, a rate 1/2 convolutional codes with a generating polynomial of (133,171) and a constraint length of 7 was employed. The soft-output Viterbi decoder has a trace back length of 35 and codeword block length of 280 bits. The wireless channel model was chosen to be fast fading “VehA” with 133 Hz Doppler [13]. For each received vector there are 8 received elements (representing 4 received antennas after real-value decomposition) and each element contains 12 bits with 4 integral bits. The P_e is assumed to be 10^{-3} and 10^{-4} .² It has been shown in [14] and [10] that for a standard six transistor 65 nm CMOS technology SRAM the chosen P_e 's equate to reducing the power consumption of the memory by approximately 50% and 40% respectively.

A. Two-Way Sorting Versus Exhaustive Scheme

In order to justify the effectiveness of the *two-way sorting* scheme (that considers only one erroneous branch), simulations results comparing the PER performance of the proposed *two-way sorting* versus the exhaustive approach in [9] (which considers all erroneous branches) are shown in Fig. 3 based on the l^2 -norm branch distance calculation methods. The results show that both algorithms achieve the same PER performance. Thus, it can be assured that there is no performance loss due to the *two-way sorting* algorithm. In addition, it is worth mentioning that one of the advantages of the *two-way sorting* algorithm is the fixed throughput as compared to [9] which suffers from variable search complexity according to memory error rates. The average number of search nodes is the same, independent of memory error rates, whereas in [9] the number of search points increases with P_e . In the following subsection, we will present the simulation results and comparisons between conventional K-Best detector and the proposed error-resilient detector based on the *two-way sorting* structure.

B. PER Performance Results

Fig. 4 presents PER performance for both the conventional K-Best MIMO detector and the proposed error-resilient one, whereas the error-resilient structure employs the *two-way sorting* algorithm described in Section III-A. The value of K is chosen to be 8 for 16-QAM and 10 for 64-QAM,³ and soft-decision decoding is assumed. Baseline in the figure refers to an error free K-Best detector, while ML refers to the exhaustive search soft-output ML detection using max-log approximation [39]. Moreover, the branch distance calculation is configured either to be l^2 -norm or l^1 -norm representations and PER performance is presented respectively. Fig. 4(a) shows the PER comparisons between the error-resilient K-Best detector and conventional approach under $P_e = 10^{-3}$ and $P_e = 10^{-4}$ with l^2 -norm representations. As shown in the figure, the proposed approach outperforms the conventional method for both values of the P_e . Specifically, when $P_e = 10^{-4}$ and for a targeted PER of 10%, the error-resilient K-Best method outperforms the conventional one by 0.5 dB for 16-QAM scheme and by

²Higher memory failure error rate (more than 10^{-3}) will result into catastrophic failure in memory cells and subsequently degraded signal quality.

³The choice of K results in a trade-off between complexity and BER performance. Works in [12], [15], [18], [21], and [22] studied and illustrated BER performances for various values of K s. The K value chosen in this work is based on a balance between BER performance and complexity.

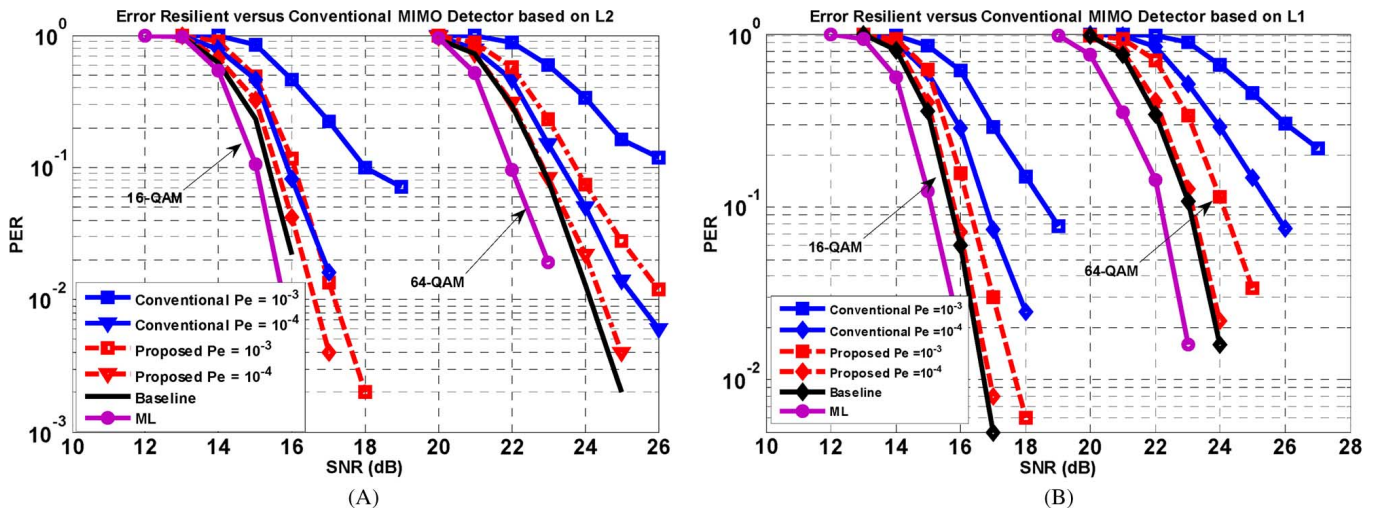


Fig. 4. PER comparisons between proposed error-resilient versus conventional detectors of 4×4 MIMO system with (a) l^2 -norm representation and (b) l^1 -norm representation. Each figure illustrates the PER performance and comparison for 16-QAM and 64-QAM modulation schemes respectively.

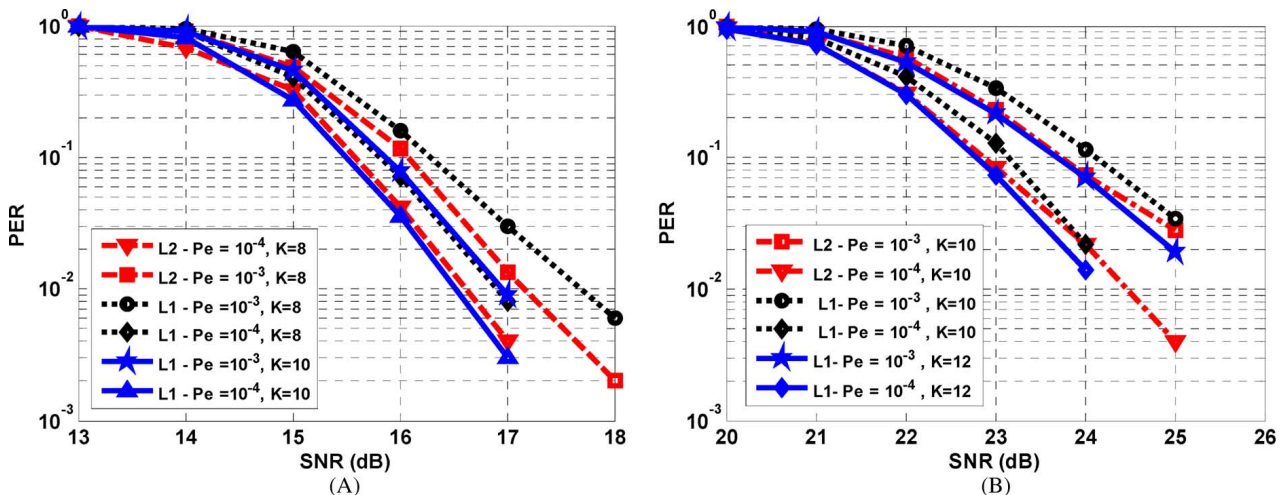


Fig. 5. Effect of increasing the K value of l^1 -norm versus l^2 -norm for (a) 16-QAM modulation scheme and (b) 64-QAM modulation scheme.

0.7 dB for 64-QAM scheme. Furthermore, the superiority of the error-resilient structure becomes much more prominent as memory errors increase. For example, as shown in Fig. 4(a), when $P_e = 10^{-3}$ and for a targeted PER of 10%, the error-resilient K-Best architecture outperforms the conventional one by more than 2 dB for both of the 16-QAM and 64-QAM schemes. In fact, under such scenario, the PER for the conventional detector approaches an error floor at higher SNR values, while that for the proposed algorithm does not exhibit that behavior. This is due to the reason that the memory errors dominate channel noise such that the conventional method can no longer correct the errors. Moreover, Fig. 4(b) further depicts PER comparisons between the K-Best detectors assuming l^1 representation. The error-resilient detector constantly outperforms the conventional one when employing l^1 -norm representation for branch distance calculation throughout the memory error rates and modulation schemes. It can be seen that a performance gain of the proposed algorithm over the conventional MIMO detector of 1 dB and 2.4 dB is observed at 10% PER for 16-QAM and 64-QAM modulation respectively with 10^{-4} memory error rate. Finally, it can also be seen from Fig. 4 that

with the selected values of K , the PER loss for the K-Best detector is marginal (less than 1 dB) as compared to the ML solution.

Specifically, it can be observed from Fig. 4(a) to 4(b) that the PER performance gap between l^1 -norm and l^2 -norm representations is fractional and decreases with the SNR. For example, for the 16-QAM modulation scheme targeted at 10% PER, there is a negligible performance degradation of 0.3 dB and 0.4 dB for 10^{-4} and 10^{-3} error rates in the memory respectively. For the 64-QAM scheme, a similar trend is observed with a performance gap of 0.28 dB and 0.39 dB for 10^{-4} and 10^{-3} error rates respectively. Thus, utilizing l^1 -norm representation can be justified as an effective approach in terms of balancing the performance-complexity trade-off. Moreover, this performance degradation can be alleviated by slightly increasing the value of K for the l^1 -norm based numeration. Fig. 5 shows that by increasing the value of K to 10 and 12 for the 16-QAM (shown in Fig. 5(a)) and 64-QAM (shown in Fig. 5(b)) modulation schemes respectively, the performance of the l^1 -based approach is enhanced and slightly outperforms the l^2 -based enumeration method.

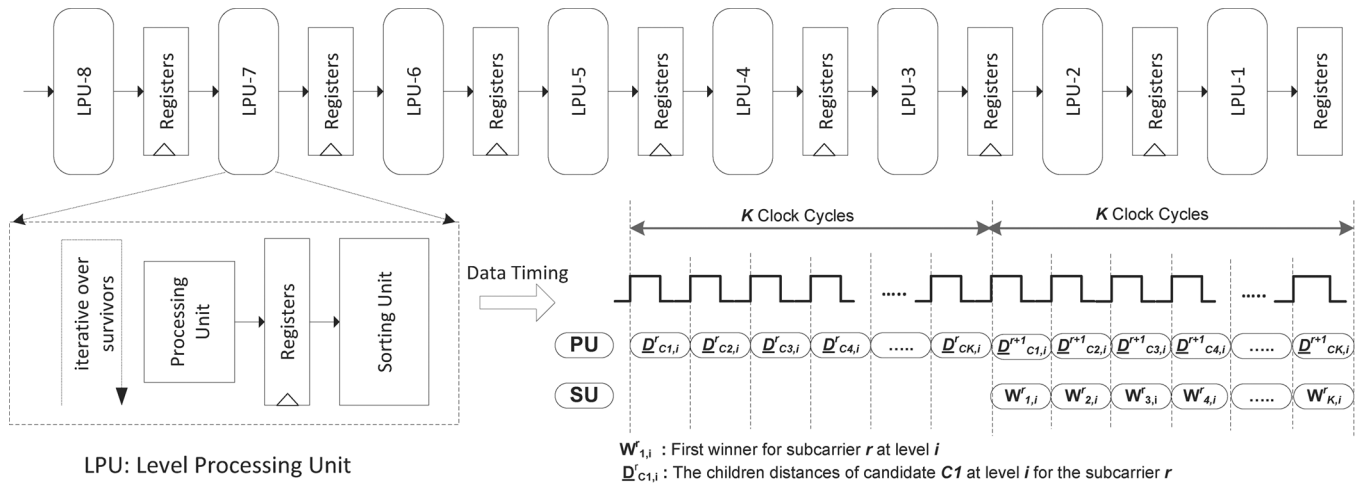


Fig. 6. High-level overview of the proposed architecture and data timing schedule.

In the following sections, a detailed description of the architecture of the proposed MIMO detector is presented along with the achieved power savings.

V. VLSI ARCHITECTURE OF THE DETECTOR

Based on the algorithms proposed in Section III, an error-resilient MIMO detector that can overcome parametric memory errors induced by VoS is designed, synthesized, placed and routed. The design is optimized for 4×4 MIMO system with 16-QAM and 64-QAM modulation schemes, in which the simulation results shown in Fig. 4 and Fig. 5 have verified close-to-ideal PER performance. The following discussion focuses on architectural innovations that reduce hardware complexity. Standard pre and post processing blocks such as soft-output stages etc. are not described in details for brevity.

A. High Level Architecture

A high level architectural overview of the proposed design is depicted in Fig. 6. As shown in the figure, the detector contains eight Level Processing Units (LPUs) in which each is responsible for processing one layer of the tree. Moreover, each LPU is comprised of two units namely Processing Unit (PU) and Sorting Unit (SU). The Processing Unit is responsible for computing the path metrics and identifying valid symbols (considering both error-free terms and erroneous terms) for each survivor node from previous levels. In other words, this unit will conduct the operations expressed in (10) to (17) or (18) to (22) for l^2 -norm and l^1 -norm respectively. The PU iterates over the K survivors and a total of K clock cycles will be consumed. After the PUs identify the valid symbols with the corresponding path metrics for each survivor, the Sorting Unit will take over and sort out the survivors of the current level and select the best K candidates. i.e., it performs the second step of the two-way sorting described previously in Section III-A. In this design, the chosen architecture for the Sorting Unit is based on the Winner Path Extension (WPE) scheme [12] which can enumerate one element per clock cycle, and thus requires a total of K clock cycles to finish the sorting operation. In addition, each LPU and the corresponding PU and SU is running concurrently in a pipelined fashion. In other words, each PU and SU within the LPU will

be processing on the specific level of the tree for different received vectors (subcarriers) at any single moment, with the aim of maximizing the processing throughput. Since both PU and SU require K clock cycles, after the pipeline is filled, this architecture can deliver the result of one received symbol vector for every K clock cycles. The data timing diagram of both PU and SU is shown in Fig. 6.

B. Processing Unit Architecture

The architecture of the Processing Unit for the 64-QAM modulation scheme is illustrated in Fig. 7. As shown in the figure, each PU is partitioned into three parts: 1) history computation circuit, 2) eight Processing Elements (PEs) running in parallel, and 3) sort and merge unit. The history computation circuit calculates the portion of the branch metric that is related to the tree nodes on the history path, that is, to compute the part of b_1 expressed by (23).

$$b_i = \hat{y}_i - \sum_{j=i+1}^{2N_r} R_{ij} s_j \quad (23)$$

Since this result will be identical for the same parent path, only one such unit is required for processing single survivor node. This part of the implementation utilizes a number of multipliers and adders, and occupies a significant amount of area and power consumption. In addition, for each survivor node, the PE is responsible for computing the complete path metrics and identifying the valid children for the symbol candidate from either error-free term or one of the erroneous terms. In other words, the PE will compute W_i and generate d_i represented in the (17). In order to maintain timing efficiency, in this architecture, multiple PEs are instantiated and running in parallel in which each one of them is operating on one symbol candidate. For example, as illustrated in Fig. 7, for a 64-QAM system, there are eight PE blocks performing the operations for symbols $-7, -5, -3, -1, 1, 3, 5,$ and 7 respectively. Once these eight valid symbol candidates are delivered, they will be sent to a sort and merge unit, in which the architecture is shown in Fig. 8(a) and (b), for a pre-sorting. The sorted results will then be saved to the registers. As mentioned previously in Section V-A, the Sorting Unit (SU) employed to identify the K best survivors

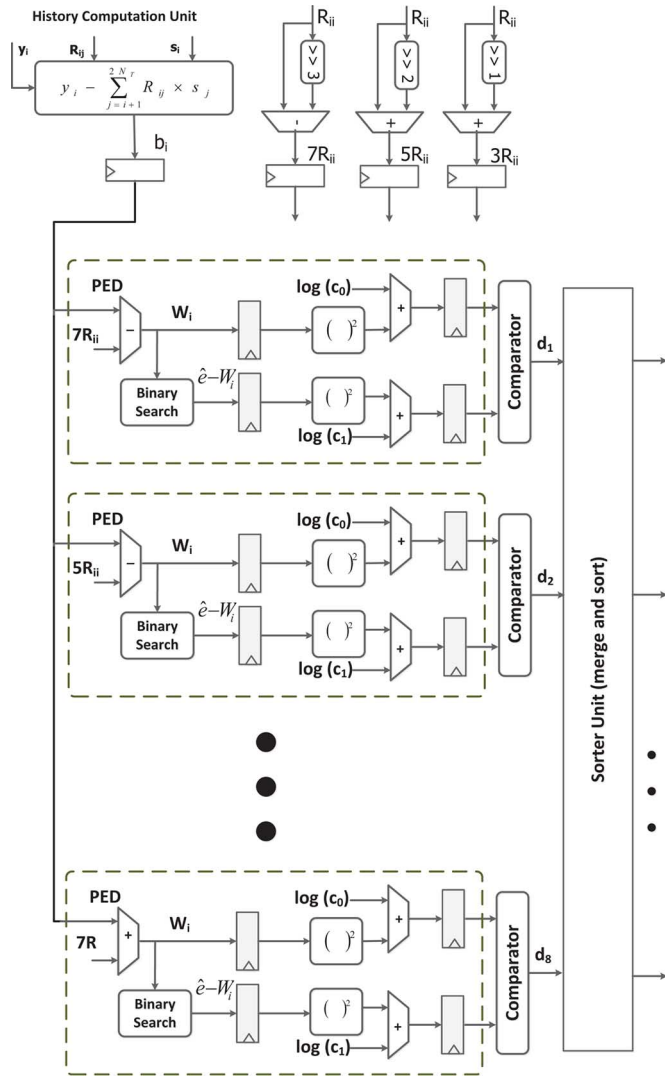


Fig. 7. Architecture of the processing unit.

is based on the WPE structure. The major characteristic of this scheme is to enumerate the child nodes according to their path metrics. Thus, the sort and merge block within the PU will arrange the child nodes for each parent node based on the path metrics, such that the WPE-based SU can extend to the next-winner candidate more efficiently. In short, the combination of the comparator circuit within each PE and the sort and merge circuit constructs the first step of the *two-way* sorting mentioned in Section III-A. The PU will iterate K times for processing all the K survivors and thus for each level of the tree, the PU will take up to K clock cycles. Finally, the detailed circuit for the binary search module is illustrated in Fig. 8(c). The design is presented as an example of four error terms. However, the design is scalable to accommodate more error terms. First, the metric $|W_i|$ is compared with the thresholds to identify the selection lines S_0 and S_1 which are then utilized with a tree of multiplexers to choose the optimum error term.

C. Sorter Unit

The SU represents the second step of the *two-way* sorting algorithm. The architecture of the WPE-based Sorting Unit is shown in Fig. 9 in which the children distances of each of the

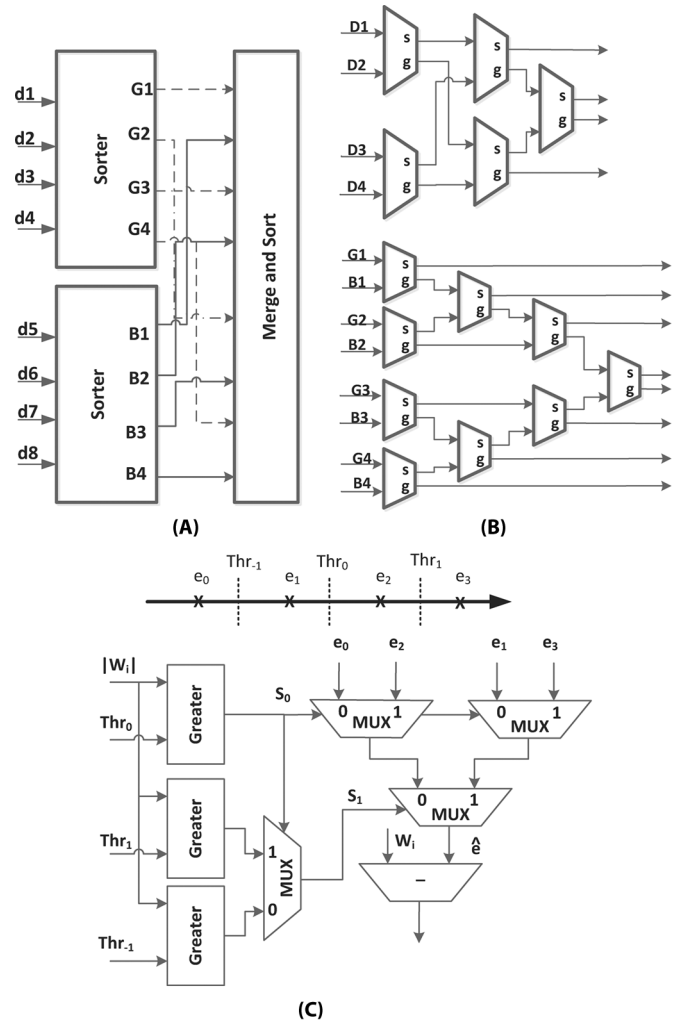


Fig. 8. (a) Architectural overview of sort and merge unit within the PU, (b) detailed structure using cascaded 2-input comparator units with smaller and greater outputs, and (c) detailed architecture of binary search circuit.

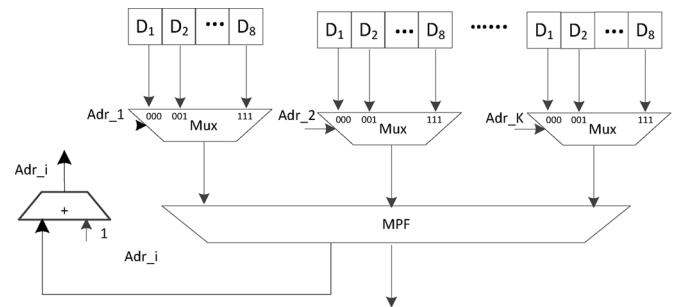


Fig. 9. WPE based sorting unit (SU).

K -parents are stored in ascending order. Initially, the multiplexer select line is pointing to the child with the minimum distance (D_1). The Minimum Path Finder (MPF) is a tree of comparators which finds the winner of K candidate distances. The select line of the winner is incremented to choose its sibling for the next search cycle. The sorting unit will take K clock cycles to find the best K children.

D. Reduced-Complexity PE Architecture

Since there are multiple PE blocks within the PU and each PE contains two squaring operations, it is of great significance

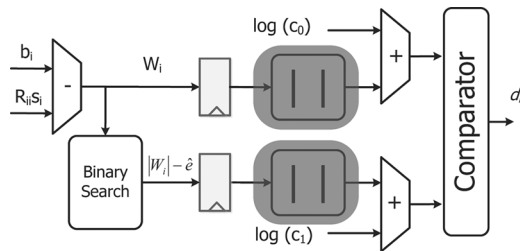


Fig. 10. The reduced-complexity architecture of the PE.

to reduce the complexity of a PE in order to achieve an efficient implementation. In addition, as shown in Fig. 7, the square operations within the PE lie on the critical path and become the bottleneck in terms of timing efficiency. Therefore, reduced-complexity PE architecture has been designed and is presented in Fig. 10. This architecture is based on the optimized algorithm presented in Section III-B where the major modification therein is to replace the squarer in the PE with an absolute value operator to perform an l^1 -norm computation instead of l^2 -norm operation. In other words, the circuit shown in Fig. 10 is designed to perform (22) instead of (17). This architectural optimization can achieve significant area and power savings, and can greatly reduce the propagation delay, owing to the removal of squaring units. The PER performance loss resulting from such a simplification step has been verified to be marginal as shown in Fig. 4 in Section IV, and can be alleviated by slightly increasing the value of K . The quantified results illustrating the efficiency and complexity improvements will be given in the next section.

VI. IMPLEMENTATION RESULTS

A. Implementation Results

The proposed error-resilient MIMO detector was designed to support a 4×4 MIMO system with 16-QAM and 64-QAM modulation schemes. The design was synthesized using General Purpose (GP) TSMC standard CMOS cell libraries with 65 nm technologies operating at the nominal supply voltage of 1.00 Volt and 25 °C temperatures. Synopsys Design Compiler was used for synthesis and the Cadence SoC Encounter was used for placement, routing and layout. The RTL, post-synthesis, and post-layout simulations were conducted and compared against the fixed point model to ensure functionality. Prime Time-PX was used for timing analysis and power consumption estimation from the post-layout results annotated with VCD switching activities. Estimates for the design in terms of throughput, area, and power are reported in Table I. Area is also reported in Kilo Gate Equivalents (kGE) to normalize the difference in technology, where a single two input NAND gate with drive strength of one is used as the reference gate. Moreover, the results for 16-QAM and 64-QAM modulations and the norm representations of l^2 and l^1 approaches are shown, where the 16-QAM scheme is based on 12-bit precision with $K = 8$ and 10 (l^2 and l^1 respectively) and 64-QAM is also based on 12-bit precision with $K = 10$ and 12 (l^2 and l^1 respectively).

As shown in the table, the reduced-complexity PU architecture described in Section V-D (using l^1 representation) helps reduce the area complexity as well as power consumption. In particular, for 16-QAM structure, the area is decreased by 23.04% and power consumption is reduced by 34.91%, whereas for 64-QAM architecture, the area is decreased by 29.27%, and

 TABLE I
 DESIGN ESTIMATES FOR THE PROPOSED ERROR-RESILIENT DETECTOR

Modulation Scheme	16-QAM		64-QAM	
	l^2	l^1	l^2	l^1
Norm Representation	l^2	l^1	l^2	l^1
K -value	8	10	10	12
Area (μm^2)	368,000	284,000	722,000	511,000
Area (kGE) ^a	230	177	451	320
Maximum Frequency (MHz)	499	641	499	641
Throughput (Mbps) ^b	998	1026	1198	1282
Power Consumption (mW) ^c	177.3	115.4	282.2	165.1
Power Consumption Overhead(mW),%	65.6 37%	20.77 18%	107 38%	31.37 19%
Area Overhead (μm^2),%	92,000 25%	51,000 18%	173,000 24%	97,000 19%

^a KGE: in terms on 2-input NAND gate of size ($2 \times 0.8 = 1.6 \mu\text{m}^2$).

^b Uncoded throughput.

^c Dynamic plus leakage power consumption at supply voltage of 1.00 V.

power consumption is reduced by 41.84%. This complexity reduction can be attributed to the removal of multiplication operations.

B. Power Consumption Analysis

It is important to realize that error tolerance comes at a cost when operating the detector in the nominal mode (i.e., buffering memory operates at the nominal voltage), since there is an overhead in area as well as power consumption. The intention of adding the error tolerance is to allow the detector to operate with buffering memories running at much lower supply voltages than nominal, while still yielding correct results. This approach results in power savings that the nominal architecture *cannot provide* when operating under the same conditions. In order to provide more insights in terms of complexity overhead resulting from the error-resilient scheme as compared to the conventional detector, we synthesized the conventional K-Best detector by employing the same design entity with the exception of removing the part that is only necessary for the error-resilient property. We then compare the area and power complexity between the error-resilient architecture with the conventional scheme where the results are illustrated in Table I (last two rows). It can be seen that the error-resilient detector results in higher complexity when compared with conventional schemes, due to the required additional hardware components. For instance, the power consumption is increased by approximately 19% and area is enlarged by approximately 19% for 64-QAM scheme with l^1 -norm representation.

In Table II, we analyze the performance and power consumption of the system including the MIMO detector and the memory sub-system at reduced voltages. In this table, we consider a 4×4 , 64-QAM MIMO with an embedded memory of 2 Mbits. This choice of memory size is motivated by considering an example of a 4×4 MIMO in the downlink of LTE Rel. 8 (20 MHz B.W), where the number of active sub-carriers per OFDM symbol is 1200 and the number of OFDM symbol per sub-frame is 14. Assuming 16 bits precision, the required buffering memory to store only one sub-frame is

TABLE II
SYSTEM POWER CONSUMPTION WITH DIFFERENT V_{dd} TO THE MEMORY

Detector Power (mW)	Memory Power ^λ (mW)	Total Power (mW)	Required SNR(dB) @ PER=10%
165.1 ^α	119.67 @ 1.00V	284.77	23.04
	101.71 @ 0.90V	266.81	23.08
	81.37 @ 0.80V	246.47	23.10
	72.99 @ 0.70V	238.10	23.14
	58.64 @ 0.65V	223.74	24.12
133.7 ^β	119.67 @ 1.00V	253.37	23.04

^λ Assuming memory size equal to 2 Mbit.

^α The proposed error-resilient design with l^1 -norm for 64-QAM.

^β The conventional design with l^1 -norm for 64-QAM.

approximately 2.05 Mbits. Higher configurations will require even more memory. The SRAM memory was generated by Artisan Memory compiler with the same 65 nm CMOS technology [22]. l^1 -norm representation is used in the detectors. As shown in the table, compared with conventional system configuration (which consists of conventional detector and memory operating at nominal voltage), the proposed scheme achieves 3.11%, 6.46%, and 12.08% reductions in terms of detector-plus-memory power consumption for the supply voltages equal to 0.8 V, 0.7 V, and 0.65 V respectively.

In addition, Table II also summarizes the SNR degradation compared with the conventional system-setup. Fig. 11 further summarizes the power consumption of *detector-plus-memory* for various memory sizes assuming conventional scheme as well as the proposed error-resilient scheme respectively. As illustrated from the figure, the extent of power savings for the error-resilient scheme over conventional scheme increases along with the memory size, as it becomes more significant in dominating the system power consumption. To be specific, as shown in the figure, when the memory size approaches 8 Mbits, the total power for the proposed configuration is equal to 351 mW, which is a 32.63% reduction compared to the conventional structure. This result suggests that the proposed scheme is more suitable for high dimension MIMO-OFDM wireless system (i.e., more antennas and/or more subcarriers), where embedded memories with much larger sizes are typically utilized. For example, an increment of the number of antennas or number of subcarriers by a factor of 2 implies doubling the memory size. This is the scenario for emerging wireless communication systems such as 802.11ac and LTE Release 12 and beyond, where support of 8×8 MIMO with higher-order modulation schemes and transmission bandwidth up to 160 MHz will require massive buffering memory at the receiver side.

C. Effective Throughput

Even though the proposed and the conventional detectors achieve the same detection throughput, the correctness of the detected data is not the same. In order to further elucidate the design trade-offs, extended experiments and analyses have been conducted. First, we consider the *effective throughput* versus supply voltage given various targeted SNRs, in which the *effective throughput* is defined as follows

$$effective\ throughput = (1 - PER) \times Throughput_{Max} \quad (24)$$

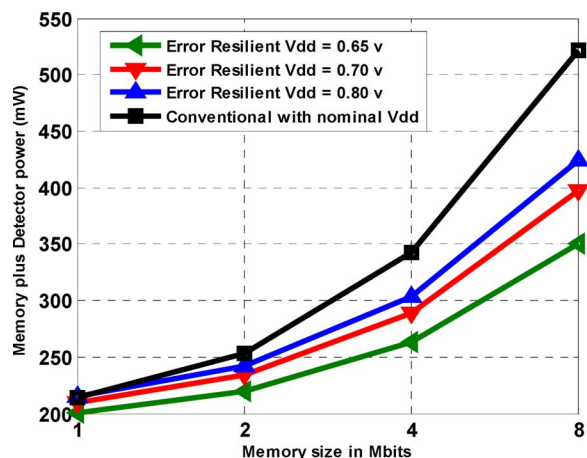


Fig. 11. System power consumption with various memory sizes.

As can be inferred from (24), the *effective throughput* takes transmission quality (i.e., Packet Error Rate) into consideration and thus can be interpreted as *the capability of delivering a number of reliable (effective) bits per second*. The comparison of the normalized effective throughput between the proposed scheme and the conventional structure is illustrated in Fig. 12, where Fig. 12(a) shows the results for a 64-QAM scheme and Fig. 12(b) presents that for a 16-QAM scheme. The SNR values are chosen corresponding to 10% and 1% PER performance of the error-free MIMO detector (the baseline with $K = 10, 12$ for 16- and 64-QAM respectively). As shown in the figures, when supplied with the nominal voltage, the effective throughput of the proposed and conventional designs is the same. As the supply voltage starts to drop, the conventional detector degrades the effective throughput drastically as compared with that of the proposed error-resilient design. This is because the error-resilient scheme has the capability to correct the errors introduced from the memory whereas the conventional structure does not. Specifically, assuming a V_{dd} equal to 0.7 V for the 64-QAM system with targeted SNR = 22.70 dB, the effective throughput of the proposed architecture outperforms that of the conventional design by 46%. As a result, it can be concluded that the proposed error-resilient MIMO detectors can operate more reliably under reduced supply voltages, with reduced power consumption as shown in Table II. Alternatively when comparing both error-resilient and conventional detectors at a fixed throughput, the proposed error-resilient detector can deliver the same throughput at a much lower memory power consumption. Specifically, matching both detector throughputs at 86% using 64-QAM modulation, the proposed system can operate the buffering memory at a supply voltage of 0.7 V while the conventional one needs to operate the buffering memory at the nominal supply voltage (1.00 V) which will result into 39% power savings in the buffering memory.

D. Required SNR

In order to study the effects of memory supply voltage on transmission power of wireless signal, in Fig. 13, we further present the required SNR to achieve a targeted 10% PER for various supply voltages. Both the error-resilient and conventional MIMO detectors have the same value of K (8 and 10 for the 16-QAM and 64-QAM respectively) and are based on l^1 -norm enumeration. As shown in the figure, for both the 16-QAM and

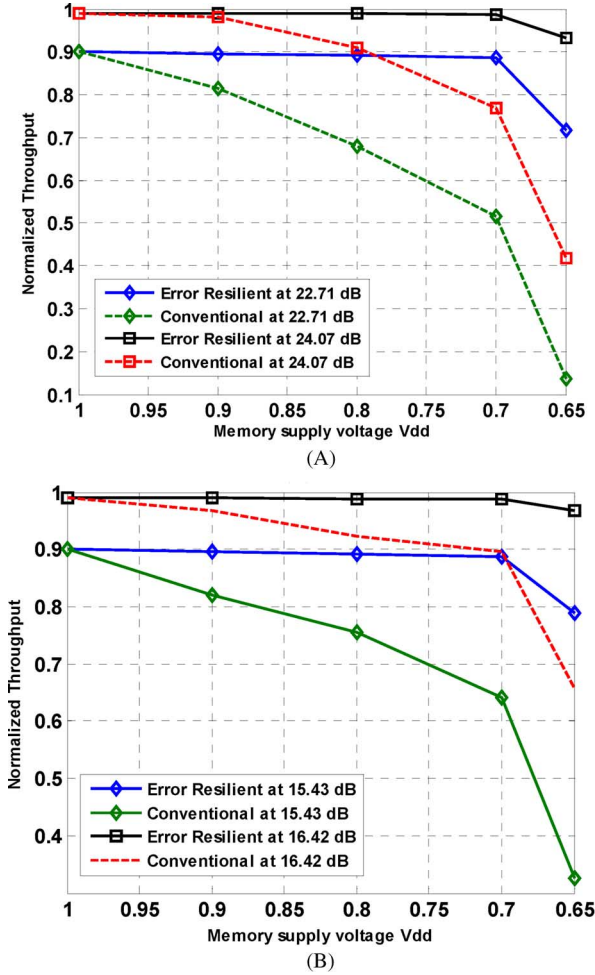


Fig. 12. Effective throughput versus supply voltages for (a) 64-QAM with $K = 12$ and (b) 16-QAM with $K = 10$, both assuming l^1 -norm representation.

64-QAM modulation schemes, to achieve 10% PER, the proposed scheme requires less SNR compared with the conventional approach when operated at lower voltages. Moreover, the difference of required SNR between the two methods increases when supply voltage of the memory is further reduced. Specifically, at supply voltage equal to 0.65 V and assuming 64-QAM modulation scheme, the required SNR for the proposed structure is 4.18 dB less compared with that for the conventional scheme. The results also verify that when the memory is operating under reduced supply voltage (in order to save memory power consumption), the proposed MIMO detector can achieve a much better signal quality compared with conventional schemes. In addition, it is noted here that a lower required SNR and reduced supply voltage both imply a saving in power consumption.

E. Comparison With Previous Work

Comparisons between the proposed error-resilient MIMO detector and previously reported conventional MIMO detectors are summarized in Table III. Several architectures and VLSI implementations for the K-best MIMO detector have been presented in the literature. To be consistent with the simulation results of the l^2 -based conventional MIMO detector in Section IV, we picked most recent architectures such that they have $K = 10$ for 4×4 64-QAM and $K = 8$ for 4×4 16-QAM. For fair comparison, the power consumption and the throughput are both

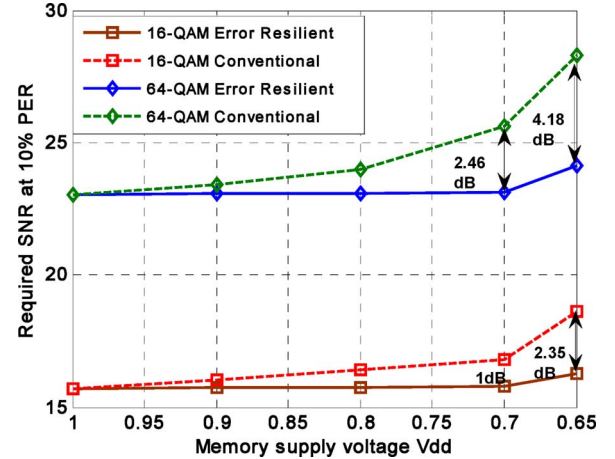


Fig. 13. Required SNR versus supply voltages for targeted PER.

scaled down to the 65 nm CMOS technology [16]. Since the detection throughput is linearly proportional to the maximum frequency (which itself should approximately scale linearly with technology), the expected throughput at 65 nm is given by

$$Throughput_{65 \text{ nm}} = Throughput \times \frac{CMOS \text{ Technology}}{65} \quad (25)$$

With the existence of VoS memories, the effective throughput of the proposed error-resilient MIMO detector is compared against the effective throughput of the conventional MIMO detectors (scaled to 65 nm) at a target SNR of 15.35 dB and 22.71 dB at which the conventional MIMO detector with perfect memory achieves 10% packet error rate for 16-QAM and 64-QAM modulation schemes respectively. In this table, the proposed design is based on the l^1 -norm and the value of K is equal to 10 for 16-QAM and 12 for 64-QAM; whereas the conventional detectors are based on the l^2 -norm and the value of K is equal to 8 for 16-QAM and 10 for 64-QAM.

In addition, at older CMOS technology such as 0.13 μm and 0.18 μm , dynamic power is the dominant contributor for the total power consumption and the contribution of the leakage power is negligible. However, when using smaller feature length CMOS technology such as 65 nm technology, leakage power accounts for at least 20% to 30% of the total power consumption [2], [24]–[27]. Therefore, an estimation of the scaled power consumption at 65 nm technology could be expressed by (26) assuming that the leakage power is 20% of the dynamic power.

$$P_{65 \text{ nm}} = P \times \left(\frac{1.00}{V}\right)^2 \times \left(\frac{65}{Tech.}\right) \times \left(\frac{f_{65 \text{ nm}}}{f}\right) \times 1.20 \quad (26)$$

The authors in [18] and [21] proposed 64-QAM MIMO detector design based on the K-Best approach. The work in [18] achieves comparable processing throughput with the proposed architecture with less area and power consumption since the proposed scheme contains the additional feature of achieving error-resilience. The design in [21] achieves higher throughput with significantly increased area and power complexity. This is due to the fact that this structure operates in the complex domain and utilizes complex-number operations as well as highly parallel architectures. Furthermore, in [15], the authors proposed a configurable architecture based on an early-pruned K-Best approach. Since the early-pruned feature helps reduce the number of search nodes, the maximum processing throughput can be

TABLE III
COMPARISONS WITH PREVIOUS K-BEST MIMO DETECTOR ARCHITECTURES FOR 4×4 MIMO SYSTEM

Modulation	This Work ^λ		[21], 2013	[18], 2012	[15], 2010	[22], 2010
	16-QAM	12	10	10	10	8
K-value	10	12	10	10	10	8
Technology (nm)	65	65	130	130	130	180
Nominal Supply Voltage (V_{dd})	1.0 V	1.0 V	1.2 V	1.3 V	1.2 V	1.8 V
Target SNR	15.35 dB	22.71 dB	22.71 dB	22.71 dB	22.71 dB	15.35 dB
PER at Target SNR	0.28	0.29	0.69	0.69	0.69	0.68
Max Frequency (MHz)	641	641	834 ^β	564 ^β	275 ^β	388 ^β
Max Throughput (Mb/s)	1026	1282	2000 ^β	1350 ^β	2200 ^β	775 ^β
Effective Throughput (Mb/s)	739	910	620	419	682	240
Area (kGE)	177	320	340	114	491	582
Scaled Detector Power (mW) ^β	115.4	165.1	1417	96	154	210
Detector ^ξ +Memory Power (mW) ^α	174	223.7	1475	155	213	269
Energy per effective bit (pJ/b)	235	246	2380	369	312	1119

^λ Assuming the implementation results of l^1 -norm representation

^β Scaling to the 65 nm technology

^ξ The detector is running at nominal supply voltage (1.00 V)

^α Assuming memory size of 2 Mbits and memory supply V_{dd} of 0.65 V

improved. However, the processing throughput is not deterministic, but varies with SNR and channel conditions. Also, due to its configurable capability to support multiple antenna and modulation schemes, the area and power consumption are also increased. In addition, [22] reported a MIMO detector targeting 16-QAM modulation scheme. The approach presented in [22] employs an enhanced tree search to reduce the latency and improve the efficiency. Compared with the proposed architecture, the one in [22] achieves comparable throughput with an increased area and power complexity.

The proposed architecture outperforms other designs in terms of effective throughput when VoS is applied to memories. This is because of the innovative error-resilient feature proposed in this work. Furthermore, in terms of energy consumption per effective bit for the detector-plus-memory, the proposed architecture achieves the best performance. As suggested from Table III, the proposed detector requires less energy to correctly decode transmitted bits when compared to the other conventional MIMO detectors.

VII. CONCLUSION

In this paper a novel error-resilient K-Best MIMO detector based on the combined distribution of channel noise and induced VoS errors was presented. Based on simulation results, the proposed algorithm achieves near-optimal performance in the presence of buffering memory errors with a gain up-to 4.5 dB as compared to the conventional MIMO detector algorithm with 64-QAM. Furthermore, the VLSI architecture and the reduced-complexity design considerations for the error-resilient MIMO detector were presented. The proposed architecture was synthesized, placed and routed. Layout based performance and complexity benchmarks were presented. From a system point of view, the combined VoS memory and error-resilient detector can achieve up to 32.64% power reduction compared to the conventional K-Best detector with perfect memory.

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