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Santa Barbara

Development of Scalable Quantum Nano-Electronic Devices Using Bottom-Up and Top-Down Fabrication

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical and Computer Engineering

by

Aranya Goswami

Committee in charge:

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September 2022

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May 2022

Development of Scalable Quantum Nano-Electronic Devices Using Bottom-Up and Top-Down Fabrication

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by

Aranya Goswami

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A PhD is a long journey and like most people, when I joined the program in the Fall of 2016, I had very little idea of how the next few years would turn out. Leaving my family and settling down in a new country halfway across the world was not easy for me, nor was learning to manage my finances, performing household chores and of course doing coursework, teaching and research in addition to everything else. It was overwhelming, as I'm sure most international students will be able to relate to. Over time, however, I fell in love with UCSB and enjoyed my time in Santa Barbara to the fullest. This would have been impossible to do alone and each and every person who ever helped me and supported me during these years deserves a huge thank you.

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Graduate school is a long journey and comes with good and bad days. On top of the usual ups and downs, the pandemic led to a complete shutdown of experimental facilities right in the middle of my PhD and resulted in panic, anxiety and uncertainties about the future – both for me and all my friends. For me, surviving these bad times would have been impossible without the support from friends and family. Here, I would first like to acknowledge and thank the constant support of my parents. Thank you for being there to celebrate every little success and consoling me during hard times, for visiting and going on trips and for everything you guys have taught me. Also, a thank you to my grandma who always looked forward to my visits home and pampered me (with food) through the years.

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[4] "Confined lateral epitaxial overgrowth of InGaAs: Mechanisms and electronic properties" **A. Goswami**, B. Markman, S. T. Šuran Brunelli, S. Chatterjee, J. Klamkin, M. Rodwell, C. J Palmstrøm J. App. Phys. 130 (8), 085302 (2021)

[5] "Controlling magnetoresistance by tuning semimetallicity through dimensional confinement and heteroepitaxy" S. Chatterjee, S. Khalid, H. S Inbar, **A. Goswami**, T. Guo, Y. Chang, E. Young, A. V. Fedorov, D. Read, A. Janotti, C. J. Palmstrøm, Science Advances 7 (16) (2021)

[6] "Identifying the fingerprints of topological states by tuning magnetoresistance in a semimetal: The case of topological half-Heusler $Pt_{1-x}Au_xLuSb$" S. Chatterjee, F. C. de Lima, J. A. Logan, Y. Fang, H. Inbar, **A. Goswami**, C. Dempsey, J. Dong, S. Khalid, T. Brown-Heft, . Chang, T. Guo, D. J. Pennachio, N. Wilson, S. Chikara, A. Suslov, A. V. Fedorov, D. Read, J. Cano, A. Janotti, and C. J. Palmstrøm

[7] "Controlling facets and defects of InP nanostructures in confined epitaxial lateral overgrowth" **A. Goswami**, S. T. Šuran Brunelli, B. Markman, A. A. Taylor, H. Tseng, K. Mukherjee, M. Rodwell, J. Klamkin, and C. J. Palmstrøm, Phys. Rev. Materials 4, 123403 (2020)

[8] "Antiphase Boundary Free InP Microridges on (001) Silicon by Selective Area Heteroepitaxy" B. Shi, **A. Goswami**, A.Taylor, S. T. Šuran Brunelli, C. Palmstrøm, J. Klamkin, Cryst. Growth Des. 2020, 20, 12, 7761–7770 (2020)
"Epitaxial Al/GaAs/Al tri-layers fabricated using a novel wafer-bonding technique" A.P. McFadden, **A. Goswami**, M. Seas, C. Rae H. McRae, R. Zhao, D. P. Pappas and C. J. Palmstrøm, J. App. Phys. 128, 115301, (2020)

[9] "$In_{0.53}Ga_{0.47}As$/InAs Composite Channel MOS-HEMT Exhibiting 511 GHz f_T and 256 GHz f_{max}," B. Markman, S. T. Šuran Brunelli, **A. Goswami**, M. Guidry, Chris Palmstrøm M. J. W. Rodwell, IEEE Journal of the Electron Devices Society, vol. 8, pp. 930-934, (2020)

[10] "Horizontal Heterojunction Integration via Template-Assisted Selective Epitaxy" S. T. Šuran Brunelli, **A. Goswami**, B. Markman, H. Tseng, M. Rodwell, C. Palmstrøm, J. Klamkin, Cryst. Growth Des. 19, 12, 7030-7035, (2019)

[11] "Selective and confined epitaxial growth development for novel nano-scale electronic and photonic device structures" S. T. Šuran Brunelli, B. Markman, **A. Goswami**, H. Tseng, S. Choi, C.J. Palmstrøm, M. Rodwell, and J. Klamkin, Journal of Applied Physics 126, 015703, (2019)

[12] "Weak antilocalization in quasi-two-dimensional electronic states of epitaxial LuSb thin films" S. Chatterjee, S. Khalid, H. S. Inbar, **A. Goswami**, F. C. de Lima, A. Sharan,F. P. Sabino, T. L. Brown-Heft,Y. Chang, A. V. Fedorov, D. Read, A. Janotti, C. J. Palmstrøm,
Phys. Rev. B 99, 125134, (2019)

[13] "Energy Efficient and High-Performance Current-Mode Neural Network Circuit using Memristors and Digitally Assisted Analog CMOS Neurons" **A. Goswami**, S. Kumashi, V. Sehwag, S. Kumar Singh, M. Jain, K. Roy, M. Sharad, arxiv.org/abs/1511.09085 (2016)

[14] "Tunneling triggered bipolar action in junctionless tunnel field effect transistor" S. Gundapaneni, **A. Goswami**, O. Badami, R. Cuduvally, A. Konar, M. Bajaj and K. V. R. M. Murali, Appl. Phys. Exp., Vol 7, No 12, (2014)

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ABSTRACT

Development of scalable quantum nano-electronic devices using bottom-up and top-down fabrication

Aranya Goswami

The invention of integrated circuits (ICs) in the 1960s and the subsequent microelectronics revolution fundamentally altered every aspect of modern technology, ranging from communication to computation and healthcare. Through the last few decades, continued miniaturization of such ICs has led to rapid improvements of device functionalities as well as exponentially reducing cost, thus making these technologies more accessible to everyone. This aggressive scaling has however, pushed device features towards sub-100 nanometer regimes, challenging conventional fabrication techniques. Semiconductor nanostructures can circumvent these challenges and enable further scaling for advanced logic and memory devices. Additionally, such nanostructures exhibit electronic and optical properties, that are of tremendous interest for alternative computing architectures such as quantum computing and photonic circuits, or to build power efficient and ultrafast platforms through low-energy and spin-based devices.

Fabricating such nanostructures is not trivial but can be achieved through both "top-down" and "bottom-up" approaches. Top-down approaches, which are commonly followed in the semiconductor industry typically start with a bulk material and fabricate nanostructures through various etching steps. Although this technique is scalable and has been extremely successful in building modern ICs, the damage induced from etching can

prove detrimental to the performance of low-dimensional systems. Bottom-up techniques generally refer to growing the nanostructures in an additive method in pre-defined positions on a wafer. Bottom-up approaches have the inherent advantage of exhibiting less defects, due to the elimination of etching steps and can be combined with in-situ patterning to build novel hybrid devices. However, these techniques are simultaneously more challenging to integrate and scale up reliably. For optimal performance of such nanostructures, it is critical to have precise control over their chemical composition, geometries, and material qualities. In this thesis, we will explore both bottom-up and top-down approaches, to achieve such defect-free scalable nanostructures in the context of low-power electronics and quantum computing.

For bottom-up approaches, we investigate two templated epitaxial growth techniques: confined epitaxial lateral overgrowth (CELO) to grow III-V lateral heterostructures and selective area growth (SAG) to grow in-plane III-V nanowires coupled to superconductors. We first discuss the inherent advantages of CELO to fabricate low-power tunneling devices. Next, we explore the use of growth conditions to reduce defects, engineer facets and improve the material qualities and morphologies in CELO nanostructures. Using this, we demonstrate high-quality lateral III-V quantum wells for heterojunction tunnel transistors. For in-plane selective area growths, we investigate the effect of fundamental parameters such as growth temperature, cooldown processes and nanowire orientation and geometries on the nucleation of highly lattice mismatched heterostructures (indium arsenide on indium phosphide). These nanowires can lead to the fabrication of scalable systems with enhanced electrical and optical properties. We also develop in-situ shadowing techniques to create patterned heterostructures of dissimilar

materials with pristine disorder-free interfaces. Subsequently, we use this to demonstrate superconductor-semiconductor hybrid nanowire networks for probing low-temperature effects in topologically non-trivial systems.

In the last part of this dissertation, we will shift our focus to top-down techniques for defining aluminum/silicon/aluminum trilayer nanostructures with extreme aspect ratios. Such nanostructures can reduce footprint and enable scaling up of Josephson-junction based superconducting qubit systems.

In conclusion, using both bottom-up and top-down techniques we combine advanced fabrication and epitaxial growth to achieve defect-free III-V scalable nanostructures with disorder-free interfaces. In the future, these nanostructures will enable the scalable fabrication of next-generation efficient computing platforms.

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I. Introduction

I A. Nanostructures for electronic, photonic and quantum devices

Semiconductor nanostructures are low-dimensional structures - such as rods, pillars or wires – with dimensions typically below 100 nm. Having such small dimensions in one, two- and three-dimensions results in nano-sheets, nanowires and quantum dots respectively. These nanostructures differ significantly from their bulk counterparts, due to quantum confinement effects that dominate at these dimensions. For example, the density of states (DOS) of these nanostructures changes significantly with each added dimension of confinement. While the DOS of a 2D electron gas (1 degree of confinement) is a constant (for one subband), the DOS for a 1D nanowire (2 degrees of confinement) and a 0D quantum dot (3 degrees of confinement) exhibit logarithmic and delta-like singularities for each subband. Thus, due to a reduced k-space for electron scattering, quantum nanowires can potentially exhibit enhanced electron mobilities useful for high-speed nano-electronic devices through nanowire field effect transistors[1], [2]. For optoelectronics, DOS engineering using dimensional confinement can result in high density of electrons and holes in the active region of a laser. This can in turn reduce threshold currents, improve differential gains and offer more robustness towards temperature sensitivity[3]. Nanostructures can also be used to probe electrical transport at cryogenic temperatures where interesting effects such as Coulomb blockade, single electron tunneling and interfacial interaction between superconductors and ferromagnetic

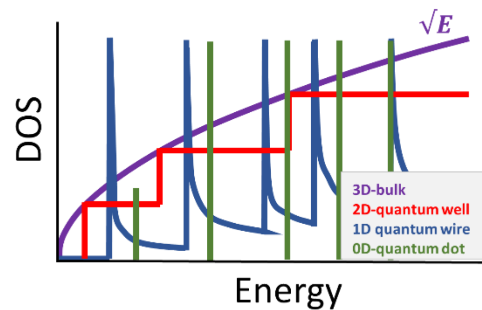


Figure 1.1 Density of states *(DOS)* vs *e*nergy diagram for various levels of confinement

materials in 1D and quasi-1D channels can be explored[4]–[9]. This can help fabricate single electron transistors or devices applicable for quantum computing[10].

Nanostructures have certain inherent advantages. III–V NWs have very good strain tolerance, which can accommodate large lattice and thermal expansion coefficient mismatch between the III–V nanowires and substrates [11], [12]. It can reduce generation of antiphase domains when growing polar III–Vs on non-polar substrates, thus improving integration on dissimilar substrates[13]. Unlike conventional III-V thin film growths, the crystal structure of most III–V NWs can be tuned between the zinc blend (ZB) and the wurtzite (WZ) phases by changing the growth conditions[14]. This provides additional control knobs for changing the band structure, and subsequently harnessing novel optical and electrical properties of the materials. As a result, nanostructures (and in particular NWs) open up a wide range of possibilities for defect-free integration of multiple materials, study the fundamental properties of materials through interesting experiments that can lead to new discoveries and applications[15].

Before delving into how such nanostructures can be efficiently fabricated – which is the focus of this thesis – a few specific examples of the applications of these nanostructures are discussed with respect to electronics, photonics and quantum computing.

For decades, the tremendous success of microelectronic devices and the use of silicon-based integrated chips across all modern technology has enabled unprecedented technological progress and impacted a major section of the global economy. Continued device miniaturization through aggressive scaling of transistors- the building blocks of modern integrated circuits (ICs)- following the 'Moore's law' is however, expected to reach significant roadblocks in the next decade due to short channel effects severely limiting the performances

of such devices. Silicon nanostructures such as trigate FinFETs and, more recently, gate-all-around (GAA) nanosheet geometries [16] have been implemented to achieve improved electrostatic control and reduce footprint. Although from an industrial point of view it is challenging to replace silicon completely as the transistor gate element, III-V semiconductors are strong contenders as alternative materials. This is primarily due to their high mobilities and low electron effective masses[17]–[19]. For extremely scaled FETs, this high mobility is translated to high source-side carrier injection velocity. Therefore, III-V transistors have been widely used for high-speed and RF electronic applications [20]–[22]. III-V nanostructure transistors can also potentially solve the challenge of extremely high-power densities and the problems of dissipating power efficiently in modern Si ICs. III-V (especially InAs) based transistors can deliver similar performances to Si, at lower supply voltages thus causing less heating problems. III-V nanowires exhibit improved subthreshold swings thus having very low leakage currents. Although mobility decreases with thinner channels due to increase in interface scattering, short gate-length transistors exhibiting near ballistic transport are much less affected[23]. A III-V nanostructure (such as vertically aligned nanowires) therefore has the potential to scale to very small dimensions . With the footprint scaling and gate length scaling decoupled, a higher transistor density can be achieved. Contact resistances and parasitic capacitances can also be lowered since gate and contact lengths do not affect the footprint [24], [25]. In summary, the several current challenges in scaling and power management in modern transistors can be potentially solved by III-V nanostructure devices.

Optical signals are well established means for efficient data transfer in both long range (internet) to short range (rack-to-rack in data centers) applications. There has been a tremendous interest in implementing on chip photonics communication which requires

nanoscale optical sources, detectors and circuits to encode and transmit data. Photonic crystal nanostructures offer extremely tight light confinement[26], thus providing strongly enhanced nonlinear effects for microwatt pump power levels [27], [28], modulators with very low (femtojoule per bit level) switching energy [29], [30] and the opportunity for enhancing and suppressing spontaneous emission [31]. Modification of energy structures due to quantum confinement in nanostructures can improve radiative recombination – thus finding applications in more efficient photonic devices. Using III-V materials in such nanostructures offers a wide range of advantages. III-V materials have direct bandgaps, thus exhibiting very low losses in recombination. III-V nanowires can break the Shockley-Queisser limit for solar cells by using their large absorption cross section, possess superior antireflection and light trapping properties, can act as efficient laser and diode sources integrated directly on Si and can also be used to fabricate the gain media and waveguides. In addition, the one-dimensional (1D) nature of nanowires permits materials synthesis in traditionally inaccessible compositional regions, which has been recently demonstrated in single-crystalline InGaN nanowires with a tunable bandgap from the UV to the near-infrared [32]. Such nanowires with tunable electronic structures hold great promise in photovoltaics, solid-state lighting and solar-to-fuel energy conversion. Thus, nanostructures play an important role in modern integrated photonics and optoelectronic devices.

Quantum phenomena often involving individual particles or excitations are typically observed at nanoscale structures [33]. The ability to efficiently fabricate such nanostructures has led to controlling these quantum mechanical effects with wide ranging potential applications in communication, computation and sensing. Silicon [34] and InAs [35] nanowires have been used for CMOS compatible spin qubits. For topological quantum computing,

protected quantum operations require quasiparticles with non-Abelian exchange statistics [36], which emerge in various engineered nanostructures where electrons are confined to one or two dimensions. Spin–orbit coupled nanowires with induced superconductivity in an external magnetic field is a widely investigated platform [37], [38] for this application. III-V nanowires can act as ballistic interconnects for coherent information transport between connected quantum devices. Such 1D networks can be applicable for Gatemons, Majorana Fermions, parafermions and cooper pair splitters, spintronic components, ballistic transistors and nonlinear circuit elements [39]. Superconducting qubits have also been demonstrated in III-V nanowires coupled to superconductors[40]. Optomechanics based quantum transduction using Si nanowires can lead to distributed quantum networks[41] . Quantum photon emitters fabricated from III-V nanowires or quantum dots embedded in nanowires have demonstrated high indistinguishability and brightness and are a potential route to integrated quantum photonics for quantum communication. Superconducting nanowires are used for high-speed high-quantum-efficiency low-dark-count-rate single-photon-detectors for quantum optics primarily in the infrared regime [42] . Thus, nanostructures are crucial to successfully studying quantum effects and harnessing them for devices applicable for quantum computing and communication.

In summary, it is well established that nanostructures are an essential component to integrate next-generation electronic, photonic and quantum devices. When the nanostructures are fabricated from III-V compounds instead of Si, there are certain additional advantages in terms of electronic and optical properties. Such nanostructures can be fabricated by both bottom-up and top-down processing and will be the topic of discussion in the next section.

I B. Bottom-up vs top-down approaches to fabricate nanostructures

Despite the promising properties of nanowires (and nanostructures in general) growing or fabricating such structures without compromising on the quality of the materials is challenging. Both top-down and bottom-up approaches are used for creating such nanostructures. Top-down approaches refer to starting with a bulk material and using various dry and wet etching to define the nanostructures of interest. Instead, bottom-up methods directly grow these nanostructures using some form of epitaxial growth. In the following paragraphs the techniques and advantages of each method is discussed.

Various methods of serial and parallel lithographic techniques are used in top-down approach. In the very basic sense, a material is protected in certain sections by a masking material (usually an organic polymer or a dielectric) and the material in the unprotected areas are etched away. Chemical etching can be performed using acids or bases and mechanical etching is typically performed using ions or molecules. The patterning of the mask layer can be done by optical lithography or electron (or ion) beam lithography. The resolution of the lithography can be calculated from the Rayleigh criterion which is given by $\mathrm{L_{min}} = 0.61 * \frac{\lambda}{NA}$ where NA is the numerical aperture. Modern photolithographic techniques can define structures of ~150–200 nm using ArF and F_2 excimer lasers (λ =193 nm and 157 nm respectively) and can go down to 10-70nm with extreme ultraviolet lithography (EUV).

Top-down fabrication methods require (1) precise control over dimensions, shape and morphology (2) etch-damage free surfaces (3) tailored profiles for specific applications and (4) large area uniformity and scalability [43]. It is also crucial to analyze and control surface defects and strain in the fabricated nanostructures. Etch profiles in a plasma based dry etch (such as inductively coupled plasma or reactive ion etching) depend heavily on the substrate

temperature at which the etch is performed. Lower temperatures can for example result in sloped sidewalls indicating reduced volatility of the etch products [43], [44]. The gas chemistry, not surprisingly, affects etch rates significantly as is seen by reduction of etch rate of GaN in Cl_2/Ar plasma with addition of H_2 [45] .Etch induced surface damage can be detected by surface spectroscopic techniques such as photoluminescence and Raman spectroscopy. Smaller mass ions in general result in lower surface defects. Wet chemical etches can be used to remove the damage from the first few layers of the nanostructure. For example, a dilute H_2SO_4 etch can etch the oxidized outside layers of a InGaAs nanostructure, to remove damage from dry etching[46]. Polarity selective etchants such as KOH can selectively etch certain facets (KOH attacks N-polar planes and not Ga-polar surfaces in GaN) due to the different states of surface bonding. However, this technique becomes challenging when the nanostructure dimensions reach below 20-50 nm due to relatively low control of the etch rates. Etch rates can be potentially reduced by decreasing temperature of etch (such as by using ice baths) but is still challenging. Nanostructures can be also patterned without using resists by direct writing with ions (Ga, He, Si) in a focused ion beam chamber [47]but is a slow (serial) and expensive technique. Although decades of effort have gone into these top-down etching processes thanks to the semiconductor industry mostly focusing on Si fabrication, several of these processes cannot be translated easily to other material system. Top-down etching fundamentally excludes exploration of certain semiconductor systems due to the lack of well-developed etches and because high quality epitaxial layers are hard to grow when it is a lattice mismatched system (such as InAs on Si). Lastly, patterning nanostructures using electron beam lithography is time-consuming and expensive.

Bottom-up techniques can solve a number of these challenges. It relies on the inherent characteristics of the substrate and the thermodynamics and kinetics of nucleation and growth to grow billions of nanostructures simultaneously. Their features can be tuned by substrate temperature, deposition rate, ratios of precursors used, as well as the preparation of the substrate prior to initiating growth. Since this method is highly parallel and avoids any damage inducing etching processes, it has the potential to create high quality nanostructures in a scalable and economical way [48]. Following the pioneering works of Lieber, Yag and Samuelson in the 90s, a wide variety of III-V semiconductor nanowires with atomically sharp heterojunctions have been demonstrated using bottom-up growth techniques[49]–[53]. These nanowires can relax strain through its sidewalls enabling growth of high quality III-V nanostructures on highly lattice mismatched materials such as Si [54], [55]. Bottom-up grown nanowires also have a greater control of resulting facets and exhibit less defective surfaces compared to those prepared through top-down etching. Some examples of applications of bottom-up grown nanowires are single electron transistors, solar cells, light emitting diodes, lasers, photodetectors, thermoelectric devices, sensors, quantum light sources, spin quantum systems and hybrid semiconductor-superconductor devices [53]. Vapor-liquid-solid (VLS) growth (first demonstrated by Wagner and Ellis in 1960s [56]) is one of the most commonly used technique for bottom-up growth of nanowires using a metal catalyst (commonly gold). Bottom-up nanostructures can also be grown using a catalyst free method known as selective area growth. This offers a more scalable position-controlled method to fabricate such nanostructures. .

IC. Organization of this dissertation

This dissertation solves three different problems using both bottom-up and top-down methods to fabricate nanostructures quantum devices. **Chapter II** provides an overview and literature review of two different bottom-up growth techniques used in this work, namely selective area growth and confined lateral epitaxial overgrowth. **Chapter III** discusses the common epitaxial growth mechanisms for bottom-up growth of these nanostructures and a comparison among the various growth kinetics and thermodynamics. In **Chapter IV** comprehensively studies confined epitaxial lateral overgrowth (CELO) as a technique to fabricate lateral heterojunction tunnel field effect transistors. Electron microscopic techniques are developed to characterize the quality of these nanostructures and the influence of growth conditions. Finally, defect-free lateral heterojunctions are demonstrated. Further, this work solves the problem of parasitic growth in CELO grown devices and demonstrates a process to reliably fabricate devices and electrically characterize the nanostructures at cryogenic temperatures. **Chapter V** addresses selective area grown in-plane nanowires and coupling them with superconductors with disorder free interfaces. Nucleation of InAs on InP nanowires is studied in depth with the use for growth conditions, cooldown processes and buffer layer materials to improve nanowire morphologies. Hetero-junction nanowires with defect-free quantum wells are demonstrated. **Chapter VI** introduces *in-situ* superconductor patterning on selective area grown nanowires using pre-patterned shadow-walls. While Chapters 2-6 focus on solving challenges in two separate bottom-up epitaxy platforms, **Chapter VII** focuses on superconducting qubits using a top-down fabrication method. A new silicon fin-based qubit architecture is proposed which helps reduce device footprint by orders of magnitude - a current

problem affecting the superconducting qubit community. Low loss fin capacitors are demonstrated and measured.

This work utilizes advanced nanofabrication methods, epitaxial growth, material characterization using electron microscopy and electrical transport measurements. It demonstrates the true power of nanostructures in solving important problems in electronics, photonics and quantum computing and tackles some of the pressing challenges in fabricating such high-quality nanostructures.

References:

[1] H. Sakaki, "Scattering suppression and high-mobility effect of size-quantized electrons in ultrafine semiconductor wire structures," *Japanese Journal of Applied Physics*, vol. 19, no. 12, pp. L735–L738, 1980, doi: 10.1143/JJAP.19.L735.

[2] H. Lueth, "Semiconductor nanostructures: a new impact on electronics," *Applied Surface Science*, vol. 130–132, pp. 855–865, Jun. 1998, doi: 10.1016/S0169-4332(98)00166-4.

[3] B. Zhao, T. R. Chen, and A. Yariv, "The Extra Differential Gain Enhancement in Multiple-Quantum-Well Lasers," *J. Watson Sr. Laboratories of Applied Physics*, vol. 4, no. 2, pp. 128–95, 1992.

[4] S. Vaitiekėnas, Y. Liu, P. Krogstrup, and C. M. Marcus, "Zero-bias peaks at zero magnetic field in ferromagnetic hybrid nanowires," *Nature Physics 2020 17:1*, vol. 17, no. 1, pp. 43–47, Sep. 2020, doi: 10.1038/s41567-020-1017-3.

[5] Y. Liu *et al.*, "Semiconductor-Ferromagnetic Insulator-Superconductor Nanowires: Stray Field and Exchange Field," *Nano Letters*, vol. 20, no. 1, pp. 456–462, Jan. 2020, doi: 10.1021/ACS.NANOLETT.9B04187/SUPPL_FILE/NL9B04187_SI_001.PDF.

[6] J. Wang *et al.*, “Interplay between superconductivity and ferromagnetism in crystalline nanowires,” *Nature Physics 2010 6:5*, vol. 6, no. 5, pp. 389–394, Mar. 2010, doi: 10.1038/nphys1621.

[7] J. Tang and K. L. Wang, “Electrical spin injection and transport in semiconductor nanowires: challenges, progress and perspectives,” *Nanoscale*, vol. 7, no. 10, pp. 4325–4337, Feb. 2015, doi: 10.1039/C4NR07611G.

[8] F. A. Zwanenburg, D. W. van der Mast, H. B. Heersche, L. P. Kouwenhoven, and E. P. A. M. Bakkers, “Electric field control of magnetoresistance in InP nanowires with ferromagnetic contacts,” *Nano Letters*, vol. 9, no. 7, pp. 2704–2709, Jul. 2009, doi: 10.1021/NL901184M/SUPPL_FILE/NL901184M_SI_001.PDF.

[9] Y. J. Doh, S. de Franceschi, E. P. A. M. Bakkers, and L. P. Kouwenhoven, “Andreev reflection versus Coulomb blockade in hybrid Semiconductor nanowire devices,” *Nano Letters*, vol. 8, no. 12, pp. 4098–4102, Dec. 2008, doi: 10.1021/NL801454K/SUPPL_FILE/NL801454K_SI_001.PDF.

[10] C. Thelander *et al.*, “Single-electron transistors in heterostructure nanowires,” *Applied Physics Letters*, vol. 83, no. 10, p. 2052, Sep. 2003, doi: 10.1063/1.1606889.

[11] E. P. A. M. Bakkers, M. T. Borgström, and M. A. Verheijen, “Epitaxial Growth of III-V Nanowires on Group IV Substrates,” *MRS Bulletin 2007 32:2*, vol. 32, no. 2, pp. 117–122, Jan. 2011, doi: 10.1557/MRS2007.43.

[12] G. E. Cirlin *et al.*, “Critical diameters and temperature domains for MBE growth of III-V nanowires on lattice mismatched substrates,” *Phys. Status Solidi RRL*, vol. 3, no. 4, pp. 112–114, 2009, doi: 10.1002/pssr.200903057.

[13] J. Johansson and K. A. Dick, “Recent advances in semiconductor nanowire heterostructures,” *CrystEngComm*, vol. 13, no. 24, pp. 7175–7184, Nov. 2011, doi: 10.1039/C1CE05821E.

[14] P. Staudinger, S. Mauthe, K. E. Moselund, and H. Schmid, “Concurrent Zinc-Blende and Wurtzite Film Formation by Selection of Confined Growth Planes,” *Nano Letters*, vol. 18, no. 12, pp. 7856–7862, Dec. 2018, doi: 10.1021/acs.nanolett.8b03632.

[15] Y. Zhang, J. Wu, M. Aagesen, and H. Liu, “III–V nanowires and nanowire optoelectronic devices,” *Journal of Physics D: Applied Physics*, vol. 48, no. 46, p. 463001, Oct. 2015, doi: 10.1088/0022-3727/48/46/463001.

[16] C. Y. Huang *et al.*, “3-D self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued moore’s law scaling,” *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2020-December, pp. 20.6.1-20.6.4, Dec. 2020, doi: 10.1109/IEDM13553.2020.9372066.

[17] J. A. del Alamo, “Nanometre-scale electronics with III–V compound semiconductors,” *Nature 2011 479:7373*, vol. 479, no. 7373, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[18] W. M. Kim *et al.*, “Electron transport in direct-gap III-V ternary alloys,” *Journal of Physics C: Solid State Physics*, vol. 14, no. 6, p. 891, Feb. 1981, doi: 10.1088/0022-3719/14/6/014.

[19] T. P. Pearsall and J. P. Hirtz, “The carrier mobilities in Ga0.47In0.53as grown by organo-mettalic CVD and liquid-phase epitaxy,” *Journal of Crystal Growth*, vol. 54, no. 1, pp. 127–131, Jul. 1981, doi: 10.1016/0022-0248(81)90258-X.

[20] S. Johansson, E. Memisevic, L. E. Wernersson, and E. Lind, “High-frequency gate-all-around vertical InAs nanowire MOSFETs on Si substrates,” *IEEE Electron Device Letters*, vol. 35, no. 5, pp. 518–520, 2014, doi: 10.1109/LED.2014.2310119.

[21] E. Y. Chang, C. I. Kuo, H. T. Hsu, C. Y. Chiang, and Y. Miyamoto, “InAs thin-channel high-electron-mobility transistors with very high current-gain cutoff frequency for emerging submillimeter-wave applications,” *Applied Physics Express*, vol. 6, no. 3, p. 034001, Mar. 2013, doi: 10.7567/APEX.6.034001/XML.

[22] D. H. Kim, J. A. del Alamo, P. Chen, W. Ha, M. Urteaga, and B. Brar, “50-nm E-mode in0.7Ga0.3As PHEMTs on 100-mm InP substrate with fmax > 1 THz,” *Technical Digest - International Electron Devices Meeting, IEDM*, 2010, doi: 10.1109/IEDM.2010.5703453.

[23] “Injection velocity in thin-channel InAs HEMTs | IEEE Conference Publication | IEEE Xplore.” https://ieeexplore.ieee.org/document/5978395 (accessed May 15, 2022).

[24] J. A. del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi, and X. Zhao, “Nanometer-Scale III-V MOSFETs”, doi: 10.1109/JEDS.2016.2571666.

[25] A. V. Y. Thean *et al.*, “Vertical device architecture for 5nm and beyond: Device & circuit implications,” *Digest of Technical Papers - Symposium on VLSI Technology*, vol. 2015-August, pp. T26–T27, Aug. 2015, doi: 10.1109/VLSIT.2015.7223689.

[26] F. Priolo, T. Gregorkiewicz, M. Galli, and T. F. Krauss, “Silicon nanostructures for photonics and photovoltaics,” *Nature Nanotechnology 2014 9:1*, vol. 9, no. 1, pp. 19–32, Jan. 2014, doi: 10.1038/nnano.2013.271.

[27] M. Notomi *et al.*, “Optical bistable switching action of Si high-Q photonic-crystal nanocavities,” *Optics Express, Vol. 13, Issue 7, pp. 2678-2687*, vol. 13, no. 7, pp. 2678–2687, Apr. 2005, doi: 10.1364/OPEX.13.002678.

[28] M. Galli *et al.*, “Low-power continuous-wave generation of visible harmonics in silicon photonic crystal nanocavities,” *Optics Express, Vol. 18, Issue 25, pp. 26613-26624*, vol. 18, no. 25, pp. 26613–26624, Dec. 2010, doi: 10.1364/OE.18.026613.

[29] A. Shinya *et al.*, “20-Gbit/s directly modulated photonic crystal nanocavity laser with ultra-low power consumption,” *Optics Express, Vol. 19, Issue 3, pp. 2242-2250*, vol. 19, no. 3, pp. 2242–2250, Jan. 2011, doi: 10.1364/OE.19.002242.

[30] K. Debnath *et al.*, “Cascaded modulator architecture for WDM applications,” *Optics Express, Vol. 20, Issue 25, pp. 27420-27428*, vol. 20, no. 25, pp. 27420–27428, Dec. 2012, doi: 10.1364/OE.20.027420.

[31] M. Fujita, S. Takahashi, Y. Tanaka, T. Asano, and S. Noda, “Applied physics: Simultaneous inhibition and redistribution of spontaneous light emission in photonic crystals,” *Science (1979)*, vol. 308, no. 5726, pp. 1296–1298, May 2005, doi: 10.1126/SCIENCE.1110417/SUPPL_FILE/FUJITA.SOM.PDF.

[32] T. Kuykendall, P. Ulrich, S. Aloni, and P. Yang, “Complete composition tunability of InGaN nanowires using a combinatorial approach,” *Nature Materials 2007 6:12*, vol. 6, no. 12, pp. 951–956, Oct. 2007, doi: 10.1038/nmat2037.

[33] A. Laucht *et al.*, “Roadmap Roadmap on quantum nanotechnologies,” *Nanotechnology*, vol. 32, no. 48pp, p. 33, 2021, doi: 10.1088/1361-6528/abb333.

[34] R. Maurand *et al.*, “A CMOS silicon spin qubit,” *Nature Communications 2016 7:1*, vol. 7, no. 1, pp. 1–6, Nov. 2016, doi: 10.1038/ncomms13575.

[35] S. Nadj-Perge, S. M. Frolov, E. P. A. M. Bakkers, and L. P. Kouwenhoven, “Spin–orbit qubit in a semiconductor nanowire,” *Nature 2010 468:7327*, vol. 468, no. 7327, pp. 1084–1087, Dec. 2010, doi: 10.1038/nature09682.

[36] C. Nayak, S. H. Simon, A. Stern, M. Freedman, and S. das Sarma, “Non-Abelian anyons and topological quantum computation,” *Reviews of Modern Physics*, vol. 80, no. 3, pp. 1083–1159, Sep. 2008, doi: 10.1103/REVMODPHYS.80.1083/FIGURES/23/MEDIUM.

[37] Y. Oreg, G. Refael, and F. von Oppen, “Helical liquids and Majorana bound states in quantum wires,” *Physical Review Letters*, vol. 105, no. 17, p. 177002, Oct. 2010, doi: 10.1103/PHYSREVLETT.105.177002/FIGURES/3/MEDIUM.

[38] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, “Signatures of majorana fermions in hybrid superconductor-semiconductor nanowire devices,” *Science (1979)*, vol. 336, no. 6084, pp. 1003–1007, 2012, doi: 10.1126/science.1222360.

[39] J. Gooth *et al.*, “Ballistic One-Dimensional InAs Nanowire Cross-Junction Interconnects,” *Nano Letters*, vol. 17, no. 4, pp. 2596–2602, Apr. 2017, doi: 10.1021/ACS.NANOLETT.7B00400/ASSET/IMAGES/LARGE/NL-2017-00400H_0004.JPEG.

[40] T. W. Larsen *et al.*, “Semiconductor-Nanowire-Based Superconducting Qubit,” *PRL*, vol. 115, p. 127001, 2015, doi: 10.1103/PhysRevLett.115.127001.

[41] A. H. Safavi-Naeini, “Quantum Optomechanics with Silicon Nanostructures”.

[42] C. M. Natarajan, M. G. Tanner, and R. H. Hadfield, “Superconducting nanowire single-photon detectors: physics and applications,” *Superconductor Science and Technology*, vol. 25, no. 6, p. 063001, Apr. 2012, doi: 10.1088/0953-2048/25/6/063001.

[43] R. Debnath *et al.*, “Top-down fabrication of large-area GaN micro- and nanopillars,” *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 32, no. 2, p. 021204, Feb. 2014, doi: 10.1116/1.4865908.

[44] D. Paramanik *et al.*, “Formation of large-area GaN nanostructures with controlled geometry and morphology using top-down fabrication scheme,” *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 30, no. 5, p. 052202, Jul. 2012, doi: 10.1116/1.4739424.

[45] R. J. Shul *et al.*, “Selective inductively coupled plasma etching of group-III nitrides in Cl2- and BCl3-based plasmas,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 16, no. 3, p. 1621, Oct. 1998, doi: 10.1116/1.581130.

[46] X. Zhao and J. A. del Alamo, “Nanometer-scale vertical-sidewall reactive ion etching of ingaas for 3-D III-V MOSFETs,” *IEEE Electron Device Letters*, vol. 35, no. 5, pp. 521–523, 2014, doi: 10.1109/LED.2014.2313332.

[47] P. Li *et al.*, “Recent advances in focused ion beam nanofabrication for nanostructures and devices: fundamentals and applications,” *Nanoscale*, vol. 13, no. 3, pp. 1529–1565, Jan. 2021, doi: 10.1039/D0NR07539F.

[48] C. v. Cojocaru, F. Ratto, C. Harnagea, A. Pignolet, and F. Rosei, “Semiconductor and insulator nanostructures: challenges and opportunities,” *Microelectronic Engineering*, vol. 80, no. SUPPL., pp. 448–456, Jun. 2005, doi: 10.1016/J.MEE.2005.04.105.

[49] L. Samuelson, S.-B. Carlsson, T. Junno, H. Xu, and L. Montelius, “Real time control of nanowire formation,” *Nanoscale Science and Technology*, pp. 19–22, 1998, doi: 10.1007/978-94-011-5024-8_3.

[50] Y. Wu and P. Yang, “Germanium nanowire growth via simple vapor transport,” *Chemistry of Materials*, vol. 12, no. 3, pp. 605–607, 2000, doi: 10.1021/CM9907514/ASSET/IMAGES/MEDIUM/CM9907514E00003.GIF.

[51] J. Hu, M. Ouyang, P. Yang, and C. M. Lieber, “Controlled growth and electrical properties of heterojunctions of carbon nanotubes and silicon nanowires,” *Nature 1999 399:6731*, vol. 399, no. 6731, pp. 48–51, May 1999, doi: 10.1038/19941.

[52] X. Duan and C. M. Lieber, “Laser-assisted catalytic growth of single crystal GaN nanowires,” *J Am Chem Soc*, vol. 122, no. 1, pp. 188–189, Jan. 2000, doi: 10.1021/JA993713U/ASSET/IMAGES/LARGE/JA993713UF00002.JPEG.

[53] V. Demontis, V. Zannier, L. Sorba, and F. Rossella, “Surface Nano-Patterning for the Bottom-Up Growth of III-V Semiconductor Nanowire Ordered Arrays,” *Nanomaterials 2021, Vol. 11, Page 2079*, vol. 11, no. 8, p. 2079, Aug. 2021, doi: 10.3390/NANO11082079.

[54] L. Güniat, P. Caroff, and A. Fontcuberta I Morral, “Vapor Phase Growth of Semiconductor Nanowires: Key Developments and Open Questions,” *Chemical Reviews*, vol. 119, no. 15, pp. 8958–8971, Aug. 2019, doi: 10.1021/ACS.CHEMREV.8B00649/ASSET/IMAGES/LARGE/CR-2018-00649N_0006.JPEG.

[55] P. Caroff, M. E. Messing, B. Mattias Borg, K. A. Dick, K. Deppert, and L. E. Wernersson, “InSb heterostructure nanowires: MOVPE growth under extreme lattice mismatch,” *Nanotechnology*, vol. 20, no. 49, p. 495606, Nov. 2009, doi: 10.1088/0957-4484/20/49/495606.

[56] R.S. Wagner & W.C. Ellis “Vapor–liquid–solid mechanism of single crystal growth”. Appl. Phys. Lett. 4, 89–90 (1964)

II. Templated bottom-up growth of nanostructures – a brief review

A. Selective area growth (SAG)

B. Confined epitaxial lateral overgrowth (CELO)

II A. Selective area growth (SAG)

Selective epitaxial growth was first reported in 1962 [1]when an oxide-masked wafer in an epi reactor showed an absence of silicon nucleation on the oxide at the periphery of the seed holes. Selective area growth (SAG) refers to the process of epitaxial growth at specific areas of a sample, which is predetermined by lithographic techniques. The general approach consists of depositing a dielectric material on the crystalline substrate. Thereafter, a combination of dry and wet etches can be used to etch the dielectric mask in specific regions leaving the other areas covered. The patterned sample is then loaded into the growth chamber of choice. Selective area growth can be performed by a variety of epitaxial techniques such as metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), and chemical beam epitaxy (CBE). These are discussed in detail in **Chapter 3**. In some instances, metal catalysts are introduced in the etched trenches to induce vapor-liquid-solid phase reactions [2]. The epitaxial growth nucleates in the etched trenches and proceeds to "fill up" the pattern that was etched using lithography. This technique of growing crystalline materials selectively in certain locations of the substrate is referred to as selective area growth (SAG), template assisted selective epitaxy (TASE) or epitaxial lateral overgrowth (ELO).

The ratio of the vertical to lateral growth rate can be effectively controlled by tuning growth conditions and ELO generally refers to growths where there is significant lateral growth on top of the dielectric mask. Further, the prefabricated dielectric templates can be made more complex, where the lateral epitaxial growth can be further constrained by a top dielectric

ceiling. Subsequently, epitaxial growth then proceeds perfectly laterally which is referred to as confined epitaxial lateral overgrowth (CELO), confined lateral selective epitaxial growth (CLSEG) (and sometimes just referred to as TASE). In case of CELO. the precursors generally reach the nucleation area though the "via" hole in the top dielectric ceiling.

The basic requirement for achieving selectivity in this growth mechanism is that nucleation and crystal growth must only occur on the underlying substrate inside the mask openings. As a result, the sticking coefficient of the adatoms should be very low to minimize nucleation on the mask. Such unintended growth on the mask is also referred to as parasitic nucleation. **Chapter 4** focuses on selectively removing such parasitic nucleation. In addition, the mask material should be heat tolerant and inert to the precursors. The mask material should also be compatible with standard lithography techniques such as dry or wet etches. As a result, Al_2O_3, SiO_2 and SiN_x are commonly used masks. These can be deposited using various deposition techniques such as plasma enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD) and sputtering tools. A slightly different solid-phase epitaxial approach uses deposition of amorphous semiconductors and recrystallizing them using laser annealing or strip heaters[3] . The chemical composition and uniformity of the dielectric layer is critical to achieving selectivity. Pinholes and rough surfaces often increase the parasitic nucleation on the dielectric layer [4].

Although the dielectric mask mainly functions in limiting epitaxial growth areas to specific sections of the substrate, it has several other functions. Selective area growth can enable defect reduction in the case of heteroepitaxy of lattice mismatched substrates using "aspect ratio trapping." In this, threading dislocations that are initiated at the heterointerface are effectively terminated inside the dielectric hole resulting in a completely defect-free lateral

overgrowth layer[5]. Utilizing this however requires a careful design of the trench dimensions based on the orientation of substrates and the respective slip planes. In case of VLS style templated growth with a metal catalyst, the etched trenches can also act as confining areas for the metal droplets and changing their wetting angles can change the morphology of the nanowire growths [6]–[8]. Metal masks using Tungsten have also been used as bottom gates for InAs nanowire field effect transistors and TiN masks have been used as superconducting templates to produce clean superconductor-semiconductor interfaces for hybrid quantum devices[9].

Selective area growth (SAG or SAE-selective area epitaxy) has been adopted widely as one of the most efficient techniques for bottom-up growth of nanostructures [10]. In 1989, Salerno et.al. demonstrated selective MOCVD growth of compound semiconductor (GaAs alloys) on Si (001) substrates [11], followed by a similar demonstration by Yamaguchi [6] . Karam et.al demonstrated GaAs on Si SAG for elimination of wafer warpage to reduce film cracking and reduce tensile stresses. In the 1990s and 2000s III-V SAG technology was used for monolithic optoelectronic device fabrication, replacing wire or bump bond based interconnections of photodiodes and their silicon readout circuitry[12] . In 2000-01, MQW GaN-InGaN blue LEDs and InAs QDs were reported using SAG on Si substrates. Subsequently in the mid-2000s GaAs and GaN nanocolumns were grown using SAG on Si (111) substrates [13]. In parallel to heterogeneous integration on Si, SAG has been widely used for homoepitaxy of III-V nanowires on (111)B oriented III-V substrates. Position controlled polygonal nanostructures including vertically aligned nanowires with {-110} vertical sidewalls have been demonstrated for compound III-V semiconductors such as GaAs, InP, InAs, InGaAs, GaAsP as well as nitrides and oxides. Position controlled AlGaAs/GaAs, InAs/InP

and GaAsP/GaAs core shell NWs and InP/InAs/InP NWs have been reported by using SAG with MOCVD growth. Axial heterostructures of InGaAs/GaAs, InAsP, InP and AlGaAs/GaAs in such vertical nanowires have also been reported. Such nanowires are critical to the development of advanced electronic and photonic devices. More recently, SAG grown in-plane III-V nanowires coupled with superconductors have attracted particular interest for their applications in topological quantum computing[14], [15].

II B. Confined epitaxial lateral overgrowth (CELO)

The concept of confining epitaxial lateral overgrowth (ELO) in the third dimension using a dielectric cantilever arose in the semiconductor device community in 1989 [16], [17] with the first demonstrations of a silicon on insulator growth using confined lateral selective epitaxial growth (CLSEG). CLSEG allowed larger surface area of the lateral growths to be efficiently characterized thus enabling better understanding of the growth mechanisms and generation of defects in these nanostructures. CLSEG also facilitated growth of high aspect ratio arbitrary geometries for ultra-thin-body (UTB) devices. The technique allowed 3D integration using stackable SOI layers. With continued scaling of CMOS transistors device isolation (reducing leakage currents and cross coupling between neighboring devices on a chip) was a huge challenge in the 1980s. CLSEG can form a uniform silicon film isolated from the substrate. In addition, the connectivity to the substrate could potentially allow removal of bottom dielectric thus allowing self-isolation through backside oxidation of the silicon films [18]. A vast body of literature exist from the early 1990s that attempt to integrate this technique for fabricating high quality SOI based electronic devices. Possibly due to the remarkable success of smart-cut technology and wafer bonding [19], [20], CLSEG (or CELO) lost its importance in this community over the next several decades.

CLSEG (or CELO) regained prominence in the mid-2010s due to the growing interest in heterogeneous integration for advanced electronic and photonic devices and the technique's suitability for these applications. It was quickly realized that CELO can enable site-selective integration of III-V materials on silicon with the additional advantage of filtering defects arising from lattice and symmetry mismatch. This was extremely useful for both hybrid III-V CMOS technology and integration of III-V photonic devices on silicon. InGaAs-on- insulator FinFETs were demonstrated on silicon [21] followed by complementary InAs/GaSb heterostructure tunnel FETs integrated on silicon [22]. Subsequently, CELO was used to integrate III-V lasers, photodiodes and waveguides on silicon with room temperature operation and efficient coupling among the individual components. Such III-V devices integrated directly on silicon holds tremendous promise for the future of high-speed low-power electronics as well as integrated photonic devices that are compatible with the Si industrial process flow. CELO has recently been also used to fabricate quantum nano-electronic devices. Ballistic interconnects were demonstrated with InAs CELO nanowires exhibiting quantized Hall plateaus[23]. CELO of InAs in a TiN template allowed fabrication of hybrid superconductor-semiconductor devices with low-disorder interfaces that are significant for topological quantum computing[9].

In summary, both selective area growth and confined epitaxial lateral overgrowth can enable the growth of high-quality nanostructures heterogeneously integrated on industry compatible substrates such as Si. These can therefore be viable pathways for wafer scale fabrication of densely integrated nanostructures for electronic, photonic and quantum devices.

The epitaxial growth conditions play a crucial role in the bottom-up growth of these nanostructures and is discussed in the following chapter.

References :

[1] B. D. Joyce and J. A. Baldrey, “Selective Epitaxial Deposition of Silicon,” *Nature 1962 195:4840*, vol. 195, no. 4840, pp. 485–486, 1962, doi: 10.1038/195485a0.

[2] D. Dalacu *et al.*, “Selective-area vapour--liquid--solid growth of InP nanowires,” *NANOTECHNOLOGY*, vol. 20, p. 6, 2009, doi: 10.1088/0957-4484/20/39/395602.

[3] H. I. Smith, M. W. Geis, C. v. Thompson, and H. A. Atwater, “Silicon-on-insulator by graphoepitaxy and zone-melting recrystallization of patterned films,” *Journal of Crystal Growth*, vol. 63, no. 3, pp. 527–546, Oct. 1983, doi: 10.1016/0022-0248(83)90165-3.

[4] F. Krizek, “Semiconductor Nanowire Networks Grown By Molecular Beam Epitaxy Vapor-Liquid-Solid,” *Phd. Thesis*, 2018.

[5] J. Z. Li *et al.*, “Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping,” *Applied Physics Letters*, vol. 91, no. 2, p. 021114, Jul. 2007, doi: 10.1063/1.2756165.

[6] V. G. Dubrovskii, W. Kim, V. Piazza, L. Güniat, and A. Fontcuberta I Morral, “Simultaneous Selective Area Growth of Wurtzite and Zincblende Self-Catalyzed GaAs Nanowires on Silicon,” *Nano Letters*, vol. 21, no. 7, pp. 3139–3145, Apr. 2021, doi: 10.1021/ACS.NANOLETT.1C00349/ASSET/IMAGES/MEDIUM/NL1C00349_M006.GIF.

[7] Y. Calahorra, A. Kelrich, S. Cohen, and D. Ritter, “Catalyst shape engineering for anisotropic cross-sectioned nanowire growth,” *Scientific Reports 2017 7:1*, vol. 7, no. 1, pp. 1–8, Jan. 2017, doi: 10.1038/srep40891.

[8] D. Gentili, G. Foschi, F. Valle, M. Cavallini, and F. Biscarini, “Applications of dewetting in micro and nanotechnology,” *Chemical Society Reviews*, vol. 41, no. 12, pp. 4430–4443, May 2012, doi: 10.1039/C2CS35040H.

[9] M. F. Ritter *et al.*, “Semiconductor Epitaxy in Superconducting Templates,” vol. 42, p. 48, 2022, doi: 10.1021/acs.nanolett.1c03133.

[10] B. Yun, “III-V COMPOUND SEMICONDUCTOR SELECTIVE AREA EPITAXY ON SILICON SUBSTRATES”.

[11] J. P. Salerno, J. W. Lee, and R. E. McCullough, “Selective OMCVD growth of compound semiconductor materials on silicon substrates - US Patent US4826784A,” May 1989. https://patents.google.com/patent/US4826784A/en?inventor=Jack+P.+Salerno&page=1 (accessed May 15, 2022).

[12] A. M. Joshi, R. Brown, E. A. Fitzgerald, X. Wang, S. M. Ting, and M. T. Bulsara, “Monolithic InGaAs-on-silicon shortwave infrared detector arrays,” *https://doi.org/10.1117/12.271192*, vol. 2999, no. 15, pp. 211–224, Apr. 1997, doi: 10.1117/12.271192.

[13] K. Tomioka *et al.*, “Selective-area growth of III-V nanowires and their applications,” 2011, doi: 10.1557/jmr.2011.103.

[14] P. Aseev *et al.*, “Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks,” *Nano Letters*, p. acs.nanolett.8b03733, 2018, doi: 10.1021/acs.nanolett.8b03733.

[15] P. Aseev *et al.*, “Ballistic InSb Nanowires and Networks via Metal-Sown Selective Area Growth,” *Nano Letters*, vol. 19, no. 12, pp. 9102–9111, Dec. 2019, doi: 10.1021/ACS.NANOLETT.9B04265/SUPPL_FILE/NL9B04265_SI_001.PDF.

[16] D. Pribat, L. Karapiperis, and C. Collet, “Conformal vapor phase epitaxy,” *Applied Physics Letters*, vol. 55, no. 24, p. 2544, Jun. 1998, doi: 10.1063/1.101976.

[17] A. Ogura and Y. Fujimoto, “Novel technique for Si epitaxial lateral overgrowth: Tunnel epitaxy,” *Applied Physics Letters*, vol. 55, no. 21, pp. 2205–2207, Nov. 1989, doi: 10.1063/1.102061.

[18] P. P. Kongetira, G. W. Neudeck, and J. P. Denton, “MODELING OF GROWTH RATES OF SELECTIVE EPITAXIAL GROWTH (SEG) AND EPITAXIAL LATERAL OVERGROWTH (ELO) OF SILICON IN THE SIH2CL2-HCL-H2 SYSTEM”, Accessed: May 15, 2022. [Online]. Available: http://docs.lib.purdue.edu/ecetrhttp://docs.lib.purdue.edu/ecetr/202

[19] J. B. Lasky, “Wafer bonding for silicon-on-insulator technologies,” *Applied Physics Letters*, vol. 48, no. 1, p. 78, Jun. 1998, doi: 10.1063/1.96768.

[20] M. Bruel, B. Aspar, and A. J. Auberton-Hervé, “Smart-cut: A new silicon on insulator material technology based on hydrogen implantation and wafer bonding,” *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 36, no. 3 SUPPL. B, pp. 1636–1641, Mar. 1997, doi: 10.1143/JJAP.36.1636/XML.

[21] L. Czornomaz *et al.*, “Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates,” in *Digest of Technical Papers - Symposium on VLSI Technology*, Aug. 2015, vol. 2015-August, pp. T172–T173. doi: 10.1109/VLSIT.2015.7223666.

[22] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, and H. Riel, “Complementary III-V heterojunction lateral NW Tunnel FET technology on Si,” *Digest of Technical Papers - Symposium on VLSI Technology*, vol. 2016-Septe, no. 619509, pp. 1–2, 2016, doi: 10.1109/VLSIT.2016.7573444.

[23] J. Gooth *et al.*, “Ballistic One-Dimensional InAs Nanowire Cross-Junction Interconnects,” *Nano Letters*, vol. 17, no. 4, pp. 2596–2602, Apr. 2017, doi: 10.1021/ACS.NANOLETT.7B00400/ASSET/IMAGES/LARGE/NL-2017-00400H_0004.JPEG.

III. Epitaxial growth mechanisms

III A. MBE, MOCVD and CBE

III B. Comparison between the growth methods

III A. MBE, MOCVD and CBE

Selective area growth can be performed in MBE, CBE or MOCVD. The samples in the first part of this thesis were grown using MOCVD, while the SAG samples were grown using the CBE. Solid source MBE was used to grow some of the nanowire samples in this dissertation. Each of these growth methods have vastly different growth mechanisms and growth condition requirements to achieve selectivity. The following provides a brief introduction to each growth method and a comparison [a significant part of this discussion follows from the informative reference [1]].

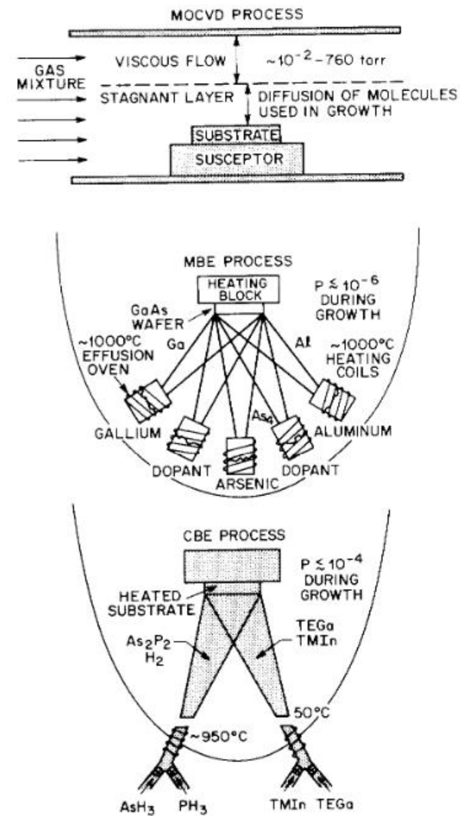


Figure 3.1 Basic processes inside the growth chambers of (a) MOCVD (b) MBE and (c) CVD (reproduced from [2] with permission from Elsevier)

Molecular beam epitaxy (MBE) is an epitaxial growth method that uses molecular beams generated from heating up high-purity elements in an ultra-high vacuum (UHV) vacuum chamber. The background vacuum pressure in the chamber is generally of the order 10^{-10} torr or lower, during no deposition. The UHV makes the mean free path of the evaporated atoms several times longer than the chamber dimensions thus generating the molecular beam. By co-depositing (or through sequential shuttered deposition techniques

[2]) multiple source elements can be used to epitaxially grow a compound on top of a crystalline substrate. The flux from the source can be controlled by changing the temperature of the effusion cells containing that element. The extreme cleanliness in the UHV chamber keeps unintentional background doping during growth to a minimum and ultra-high mobility samples can be grown in these chambers. The growth can be monitored in-situ using reflection high energy electron diffraction (RHEED).

Metal organic chemical vapor deposition (MOCVD) uses gas phase reactions with metal organic gas sources to perform epitaxial growth. Chamber base pressures are usually in the 10^{-3} Torr range and can go up to 10^{2} Torr during growth. Metal organic gas sources are controlled by using mass flow controllers or Baratron capacitance manometers (pressure transducers) with needle valves connected via a PID loop. Since hydrogen is used as a carrier gas for the metal-organic molecules, significant hydrogen incorporation happens during growth. In addition, there is also a considerable carbon incorporation due to the cracking of metal morganic molecules. Although RHEED can not be used for the high chamber pressures, reflectance absorption spectroscopy (RAS) [3] and reflectance difference spectroscopy (RDS) [4], [5] can be used as an *in-situ* feedback mechanism. Since MOCVD grows materials with a much higher flux compared to MBE, it is well suited and popular for industrial production.

Chemical Beam Epitaxy (CBE) is a unique hybrid combination of a MBE and a MOCVD. In the CBE system all the sources are gaseous and are derived from group-III alkyls and group-V hydrides[6]. For group III, In and Ga are derived from the pyrolysis of either trimethylindium (TMIn) and triethylgallium (TEGa) on the heated substrate surface respectively. The As_2 and P_2 are obtained by thermal decomposition of Arsine and Phosphine, passing through heated

tantalum or molybdenum tubes respectively. Commonly, researchers use low pressure cracking capillaries, where the AsH_3, PH_3, etc. are thermally decomposed by means of a heated metal (Ta etc.) filament or foil . A different principle is applied in the high-pressure effusion source, usually applied in connection with flow-controlled inlet systems. The hydrides are injected at a pressure between 0.2 and 2 atm through alumina tubes with fixed small leaks into the UHV chamber. The tubes are heated, such that the hydrides are effectively decomposed by gas phase collisions within the tube. On their path through the leak, there is a transition from hydrodynamic to molecular flow in the UHV environment [7]. A low-pressure arsine and phosphine cracker with a reduced input pressure of ~200 Torr is sometimes maintained on the high-pressure side of an electronic mass flow controller (when used). The cracking temperature is around 900°C. The flow rates for the various gases can be adjusted by setting the line pressures. Unlike MOCVD, in which the chemicals reach the substrate surface by diffusing through the stagnant carrier gas boundary layer above the substrate, the chemicals in CBE were admitted into the ultra-high vacuum modified MBE growth chamber and impinge directly line of sight onto the heated substrate surface in the form of molecular beams. Mechanical shutters can be used reduce the transient flow effect during valving and very abrupt composition and

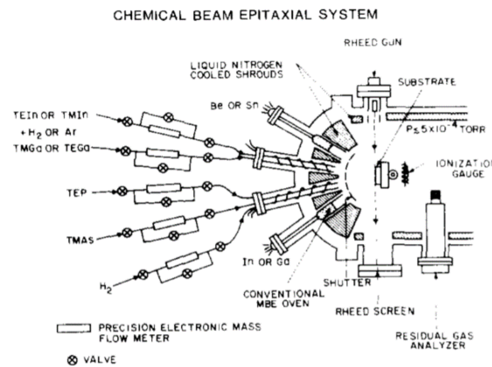


Figure 3.2 Gas handling system and growth chamber with conventional MBE condensed phase elemental sources and *in-situ* surface diagnostic capabilities in a MOMBE system (reproduced from [2] with permission from Elsevier)

doping changes can be achieved for ultrathin epitaxial layers. In addition to this, solid source effusion cells can also be added to the chamber similar to conventional MBEs akin to a gas source MBE. The growth chamber is equipped with RHEED for in situ feedback of surface reconstructions and smoothness, ion gauges to measure pressure, residual gas analyzer for measuring gaseous species and is pumped using a diffusion pump with a liquid nitrogen cooled trap (this is specific to a VG Semicon manufactured chamber, such as the one used for growths in this dissertation). During growth chamber pressures are usually maintained at high 10^{-6} to 10^{-5} Torr. The high chamber pressure is primarily due to cracked group-V hydrides and hydrogen which are slow to pump out [8].

III B. Comparison between the growth methods

In a conventional **MBE** adatoms impinging on the surface of a substrate diffuse on the surface and incorporate into the lattice sites in the presence of excess group V molecular beams in the form of dimers or tetramers. Here, typically the sticking coefficient of the group III atoms on the surface of the substrate is approximately unity and as a result, the growth rate is group III limited. The group III atoms are are derived from thermal evaporation of solid elemental sources and hence reach the sample surface without any additional chemical reactions. Gas source MBEs (which use an effusion cell for group III and the group V is derived from thermal cracking of group-V hydrides) follow a similar reaction kinetics.

In **MOCVD** the group III alkyls in the gas stream of H_2 and N_2 diffuse through a stagnant boundary layer above the heated substrate, and thermally dissociate the alkyl radicals at the substrate surface to yield group III atoms. These migrate to the appropriate lattice sites and epitaxially incorporate by capturing a group V atom, which is a result of thermal cracking of

the hydrides at the heated substrate surface or thermal pre-cracking upstream. The growth rate at standard growth temperatures is limited by diffusion of precursors through the stagnant boundary layer to the heated substrate surface. Within the residence time during which the group III alkyl molecules are adsorbed on the surface all of them are dissociated leaving group III atoms. One of the challenges of MOCVD is that the precursors can undergo pyrolysis in the gas phase and result in gas-phase reactions leading to unwanted by-products.

In **CBE**, the beam of group III alkyl molecules impinges direct line of sight into the heated substrate surface. No boundary layer exists on top of the substrate surface. The mean free paths at pressures of 10^{-6} to 10^{-5} torrs is long (for example, mean free path of nitrogen at $1x10^{-6}$ torr is approximately 193 feet) and as a result there is no molecular collisions on the path [6]. After a group III alkyl molecule arrives at the heated sample surface it can either acquire enough energy to completely dissociate the alkyl groups leaving behind an elemental atom or it can reevaporate undissociated or partially dissociated, depending on the substrate temperature. At high enough growth temperature, therefore, the growth rate is limited by arrival of group III alkyls. For example, as shown in the figure, for a constant flow rate, the growth rate of GaAs increases linearly with increasing temperature upto 550 °C but stayed constant after that. Below 550 °C the growth rate is limited

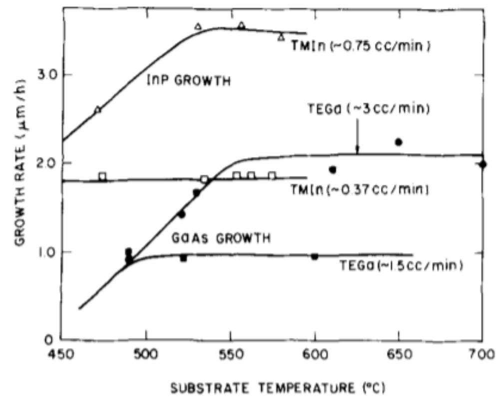


Figure 3.3 Growth rates of InP from TMIn and GaAs from TEGa as a function of substrate temperature at different absolute flow rates of group III alkyls. (reproduced from [9] with permission from AIP publishing).

by TEGa dissociation process with an activation energy of about 50kCal/mol (mean bond dissociation energy of metal ethyl bonds in TEGa). The growth rate scales linearly with the flow rate above the critical temperature of 550 °C in this example. A similar behaviour is observed with InP growth using TMIn. It should be stressed that in CBE decomposition reactions take place during surface diffusion [1]. Additionally, during CBE, the `sticking coefficient' of the group III species can be non-unity depending on growth conditions and facets of incorporation and consequently, desorption cannot be neglected [1].

References:

[1] M. R. Leys, "Fundamental growth kinetics in MOMBE/CBE, MBE and MOVPE," *Journal of Crystal Growth*, vol. 209, no. 2–3, pp. 225–231, Feb. 2000, doi: 10.1016/S0022-0248(99)00544-8.

[2] W. T. Tsang, "From chemical vapor epitaxy to chemical beam epitaxy," *Journal of Crystal Growth*, vol. 95, no. 1–4, pp. 121–131, Feb. 1989, doi: 10.1016/0022-0248(89)90364-3.

[3] V. L. Berkovits and D. Paget, "Reflectance anisotropy spectroscopy: a new method for semiconductor surface chemistry investigation," *Thin Solid Films*, vol. 233, no. 1–2, pp. 9–13, Oct. 1993, doi: 10.1016/0040-6090(93)90051-P.

[4] D. E. Aspnes, “Reflectance-Difference Spectroscopy: A New Probe of Crystal Growth by MBE and OMCVD,” *IEEE Journal of Quantum Electronics*, vol. 25, no. 5, pp. 1056–1063, 1989, doi: 10.1109/3.28000.

[5] D. E. Aspnes, J. P. Harbison, A. A. Studna, and L. T. Florez, “Application of reflectance difference spectroscopy to molecular-beam epitaxy growth of GaAs and AlAs,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 6, no. 3, p. 1327, Jun. 1998, doi: 10.1116/1.575694.

[6] J. S. Foord, G. J. Davies, and W. T. Tsang, *Chemical beam epitaxy and related techniques*. Wiley, 1997.

[7] H. Lüth, “Chemical beam epitaxy - a child of surface science,” *Surface Science*, vol. 299–300, no. C, pp. 867–877, Jan. 1994, doi: 10.1016/0039-6028(94)90703-X.

[8] W. T. Tsang, “Chemical beam epitaxial growth of very low threshold Ga0.47In0.53As/InP double-heterostructure and multiquantum well lasers,” *Applied Physics Letters*, vol. 49, no. 16, p. 1010, Jun. 1998, doi: 10.1063/1.97455.

[9] W. T. Tsang, “Chemical beam epitaxy of InP and GaAs,” *Applied Physics Letters*, vol. 45, no. 11, p. 1234, Jun. 1998, doi: 10.1063/1.95075.

IV. CELO based triple heterojunction TFETs

IV A. Introduction

IV B. Fabrication of CELO templates MOCVD growth of nanostructures

IV C. Tuning defects and facets in CELO of InP

IV D. Horizontal heterojunctions in CELO

IV E. Electrical characterization of InGaAs CELO

IV F. Future directions for CELO

IV A. **Introduction**

Inspired by the successful demonstrations of confined epitaxial lateral overgrowth (CELO) [1]– [3], a CELO based high on-current triple heterojunction tunnel field effect transistor device was proposed [4]–[6]. Tunnel FETs are transistors that use electron tunneling from the valence band to the conduction band of the device to flow current. This tunneling is modulated by gate voltage induced band bending[7]. The tunneling mechanism allows tunnel FETs to theoretically reach below 60mV/dec subthreshold swings and very low off currents. However, the main challenge with current state-of-the-art tunnel FET is that the tunneling barriers are considerably thick. Since tunneling current scales exponentially with tunneling distance, the device on-currents are therefore sub-par (I_{ON} <100uA/μm) compared to high performance transistors. To solve this issue and increase the on-current, three separate

approaches were simultaneously adopted for the proposed III-V triple heterojunction tunnel FET[4]–[6].

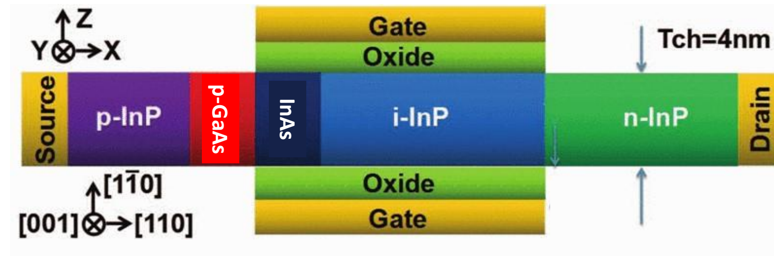


Figure 4.1 Device structure, material composition, and design parameters of the 3HJ TFET design (adapted from [8] with permission)

One, III-V materials have anisotropic electron and hole bands. Choosing [110] as the tunneling orientation simultaneously lowers the transport effective mass and the tunnel barrier compared to a [100] tunneling orientation. Second, adding extra heterojunctions in both the source and the drain creates quantum wells and resonant states that work constructively to enhance the tunneling probabilities. A larger hole effective mass in the chosen orientation lowers the source-to-drain leakage currents. Third, inserting transition layers in the source and channel heterojunctions increases the electric field at the tunnel junction, further improving the overall transmission probabilities[4]. Although the initial proposed hetero-structure comprised of a AlInAsSb/InAs/GaSb/AlGaSb device, further iterations on simulations simplified the structure and eliminated Sb based compound semiconductors to a doped-InGaAs/p-InP/strained p-GaAs/ strained intrinsic InAs/InP heterojunction (Figure 4.1) [8].

Current TFET fabrication techniques include facet selective etching, nanowire etching and nanowire growth [9]–[11]. However, producing ultra-thin body (UTB) structures <10nm in thickness are difficult using this technique. Facet selective etching and transistor fabrication

on the etched facets does not provide the necessary lateral confinement and limits transport along <111> rather than [110] crystallographic orientation. Finally, nanowire transistors often suffer from poor gate alignment along the vertically oriented junction. To produce an effective 3HJ-TFET it is critical to have a channel thickness of < 10 nm, gates aligned within 2nm (to ensure high field region is at tunnel junction and have a steep subthreshold swing) [12] , and atomically abrupt heterojunctions.

The technique of CELO is highly suited for fabrication of such a nanostructured device. It allows the vertical device dimensions to be defined purely by the thickness of the deposited sacrificial layer and the lateral dimensions determined by standard lithography techniques. CELO enables the selection of an arbitrary orientation of the nanostructure growth on the substrate. Further, by choosing the correct orientation it might be possible to generate a flat vertical facet in the direction of the growth. Such facets can enable the growth of lateral heterojunction-based devices, while enabling simple planar gating. The horizontal (in-plane) gate allows for high accuracy in alignment with the junction.

IV B. Fabrication of CELO templates MOCVD growth of nanostructures

This section summarizes the main results of fabrication of templates and MOCVD growth inside the templates. For more details on fabrication and growth conditions, refer to[13], [14] and the thesis of Brian Markman[15] and Simone Šuran Brunelli who were part of this project at UCSB. .

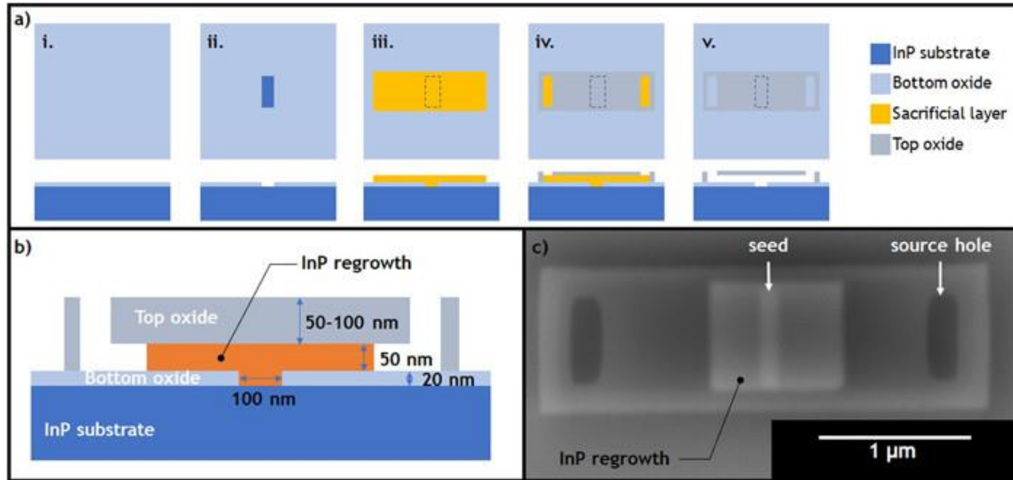


Figure 4.2 (a) Illustration of general template fabrication. (b) Illustration of cross-section of the template after growth. (c) Top-down SEM image of template after homoepitaxy of InP. The contrast allows seeing the seed location, the confined lateral overgrowth, and the unfilled cavity (reprinted from [13] with permission from AIP publishing)

The fabrication of the CELO template contains three main parts - the bottom patterned oxide, the sacrificial layer and the top patterned oxide (Figure 4.2). Choosing the optimum deposition technique and etch chemistries are paramount to successfully fabricating a high yield of such templates and achieving high quality growth with minimal parasitic growth. Unlike Si, where high quality thermal oxide is often used for fabricating the mask, thermal

oxides are not available for III-V materials. For depositing the seed (bottom) dielectric, the deposition methods under consideration were ALD, PECVD and sputtered oxides. Preliminary tests with depositing via all three techniques were followed by MOCVD growth of InP to check the levels of parasitic growths. The minimum parasitic growth was found to occur in PECVD deposited templates [15]. Maintaining low roughness in this initial layer is crucial since it can lead to significant deviations in the overgrown III-V layer roughness which in turn can affect transport and quantization properties of the nanostructure. Since roughness scales with thickness, the thickness was kept low (~30nm). Inductively coupled plasma with a fluorine chemistry was used to etch the seed holes. A dry etch is necessary since a wet etch (with HF or similar) does not provide enough control to etch dimensions that are about 100nm or below.

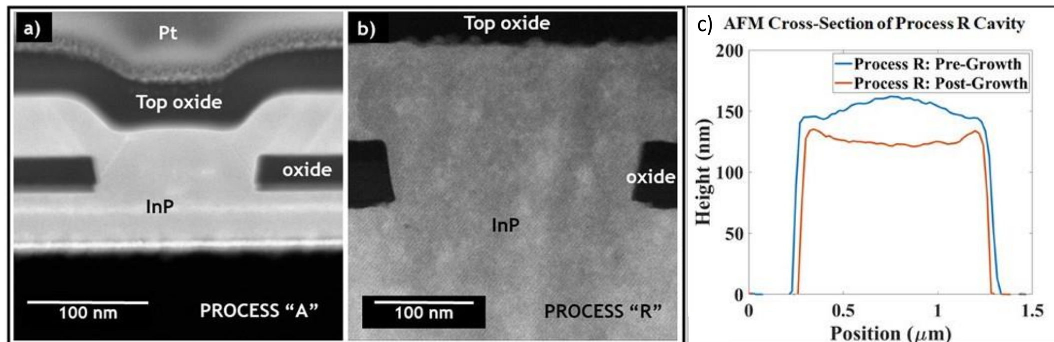


Figure 4.3 Cross sectional TEM showing process A (with a-Si sacrificial layer), Process R (with CSAR sacrificial layer and HSQ top oxide) and cavity bowing before and after growth. (reprinted from [13] with permission from AIP publishing)

While MOCVD showed decent selective area growths on these samples, CBE growths failed exhibiting island nucleation. Damage from exposure to the plasma and the fluorinated InP surface (forming non-volatile In_xF_x) were assumed to be the main causes. Aggressive cleaning with H_3PO_4: HCl 3:1 improved the CBE growths at the cost of significant undercutting. To solve this, an etch stop AlO_x layer was deposited with thermal (no plasma) ALD prior to depositing the SiO_x layer. This combined with a remote plasma clean to remove

organic residues (using the Gasonics 2000 downstream plasma asher) improved growths in the CBE.

For the sacrificial layer, two different approaches were followed. One (process-A), with amorphous Si that was subsequently followed by a PECVD deposited top SiO_x dielectric. Prior to a-Si removal, an oxide densification anneal at greater than 700°C was performed to improve etch selectivity of a-Si/SiOx in xenon difluoride (XeF_2). The a-Si was etched by a XeF_2 etch, which avoids the slow TMAH (which simultaneously etches the SiO_2). The second method (process-R) was using spun-on CSAR (chemically semi amplified resist) resist as a sacrificial layer. This was followed by using spun-on HSQ (hydrogen silesquioxane) which on subsequent exposure in the EBL and development in basic chemistry, forms the top oxide, leaving the CSAR layer untouched. Prior to loading into the MOCVD reactor, the diced samples were dipped in 0.3% HF for 10 seconds. This was found to remove parasitic growths significantly.

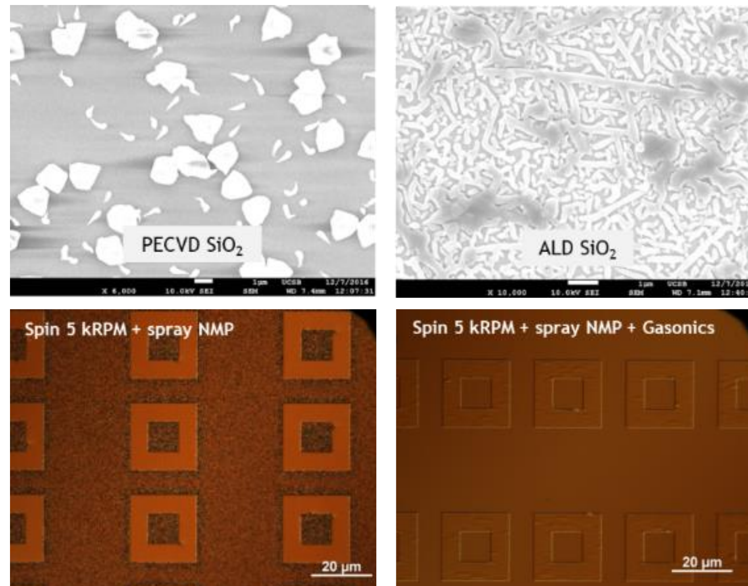


Figure 4.4. MOCVD growth selectivity with (a)-(b) various bottom oxide deposition techniques and (c)-(d) with cleaning (adapted from [15]) .

Since growth at MOCVD usually happens at temperatures of 580-620°C. thermal mismatch of the oxide mask and the semiconductor resulted in significant bowing of the template ceilings during warmup and cooldown. The bowing was especially pronounced in the samples prepared using HSQ as the top oxide (Figure 4.4). This is assumed to be primarily due to the expansion /contraction of the HSQ oxide and a relatively large (>20%) reported value of thermal distortion in HSQ for temperatures above 600°C[16], [17]. In addition, poor adhesion of HSQ to PECVD SiO_x bottom oxide was observed leading to templates being disconnected from the bottom oxide.

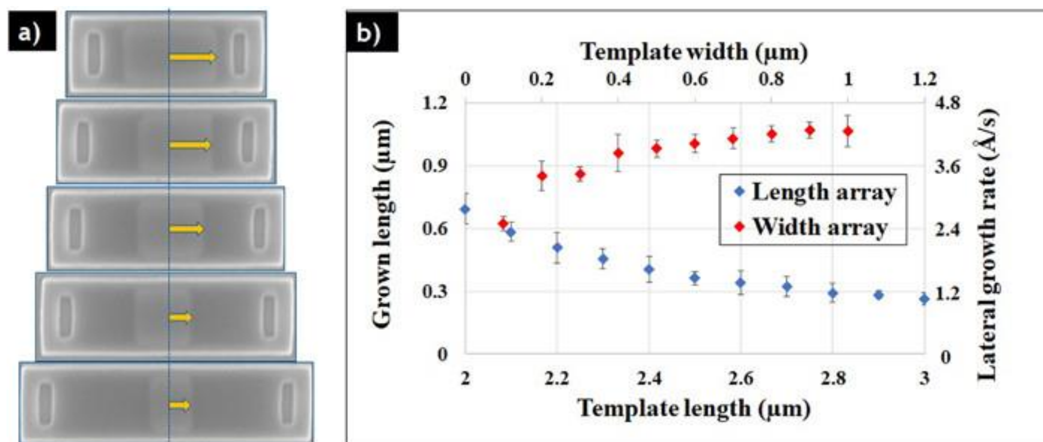


Figure 4.5. CELO InP growth length vs template length with all other template dimensions and growth conditions fixed. (b) shows growth length variation with both length and width variation of templates (reprinted from [13] with permission from AIP publishing)

Template geometry affects mass transport for epitaxial lateral growth in CELO templates as evidenced by growth rate and faceting. Growth rate decreases as template lengths increase explained by longer time for diffusion of precursors to the growth front inside the template. Larger template widths resulted in higher growth rate because of the larger source hole for higher mass transport. Increasing packing densities were however observed to

decrease growth rates similar to a commonly observed loading effect[18] that is in contrast to previous reports where they were mostly constant [19]. This can be explained by differences in template geometries as well as pitch lengths between this and the cited work.

The facets and defects in these nanostructures also vary considerably not only with the choice of substrates and orientation of growth but also with the growth conditions such as growth temperature and V/III ratio. This is discussed in depth in the following section.

IV C. Tuning defects and facets in CELO of InP

IV C.(i). Facets

Facets play a critical role in the chemical and electronic properties of a nanostructure. The ability to control these facets with control knobs such as nanostructure growth conditions presents attractive avenues to fabricate new devices and probe interesting physics at the nanoscale. For example, the effects of electron confinement (that is negligible in macroscopic devices) becomes an important parameter to consider in devices with nanoscale dimensions. This can be understood using the classic example of the n-dimensional confined density of states of electrons for a quantum well (2D), quantum wire (1D) or quantum dot (0D). In III-V semiconductors, basic material parameters such as heavy-hole bands and effective carrier masses area highly anisotropic and depend on the orientation selected, confinement direction and strain in the nanostructures[20], [21] . As a result, in a crystalline material, the facets (crystal orientation) chosen for the particular application (ex, direction of electron tunneling) matters significantly. For example, in InAs/GaSb tunnel FET, the $(1\bar{1}0)$ confined structure has a lower effective hole mass and smaller tunnel barrier compared to (100) confinement. As a result, the tunneling probabilities (and hence currents) are higher for a $(1\overline{10})$ confined device[22] . Therefore, it is incredibly useful to be able to control the facets of the bottom-up grown nanostructure device to have the desired orientation of transport and confinements.

The formation of facets in semiconductor crystals is governed by equilibrium thermodynamics. The equilibrium shape is often found by minimizing the total surface energy subjected to the constraint of constant volume. If surface energies of all the facets were equal the resulting equilibrium shape would be a sphere. Wulff *et.al.* [23]–[25] demonstrated that the equilibrium crystal shape can be obtained from the surface energy plot. Apart from growth

thermodynamics, growth kinetics also plays an important role in determining final facet shapes. Growth rates are dependent on anisotropy of surface processes such as adsorption, desorption and surface diffusion with equal mass transport to the different facets[26]. This can be accounted for by using the kinetic Wulff's plot or ν plot). Surface energies are dependent on temperature and precursor fluxes. As a result, growth conditions can be a powerful tool to design the facets in nanostructures. Confined epitaxial lateral overgrowth deviates from ideal equilibrium stabilized growths in several ways. Clearly, the template restricts natural growth in certain orientations resulting in epitaxial growth that is not dictated solely by Wulff's plots. However, once the lateral growth initiates, the facets at the growth front can essentially evolve freely fulfilling the necessary conditions for determining equilibrium facet shapes through thermodynamics.

Characterization of nanostructures:

In the MOCVD growths of CELO nanostructures the first challenge is to accurately characterize the nanostructure facets. This seems relatively straightforward since the combination of top-down and slanted SEM micrography along with cross-sectional TEM provides an accurate analysis of the nanostructure material quality. However, it is important to note that these are only representative of a small part of the whole nanostructure. First, the information obtained from a cross-sectional TEM of a single slice at the center of the nanostructure does not provide any information of the material quality at the edges near the confining walls. Second, CELO shows a variation with respect to minute variation in fabrication of templates. As a result, it is often crucial to derive conclusion from multiple structures rather than a single TEM. This necessitates the use of a technique that can

simultaneously provide a complete picture of the whole nanostructure growth and provide sufficient resolution and confidence over the observed features.

In this work, a combination of plan-view and cross-sectional TEM was implemented (Figure 4.6). Even though individually cross-sectional and plan view TEMs are used regularly for film quality analysis, no such study combining TEM in plan-view and cross-section (to the best of our knowledge) has been performed at the same position on nanostructures or devices. As a result, the technique developed in this study, is not only applicable for our current topic of discussion but can be very useful for analyzing any future nanostructure. The process of fabricating such TEM lamellas and the imaging techniques have been outlined in the following section.

IV C. (ii) Simultaneous plan-view and cross-section TEM lift out technique

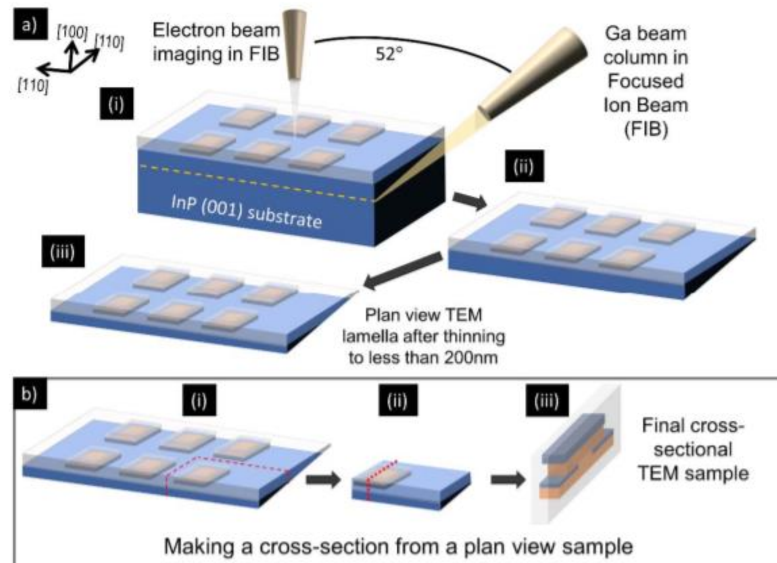


Figure 4.6. Focused Ion Beam steps to make a plan view specimen of the CELO structures (a.i-a.iii)and preparing a cross-section from a plan-view lamella (b.i-b.iii) (reprinted with permission from [27]. Copyright {2020} American Physical Society).

Cross-sectional transmission electron microscopy (TEM) samples were prepared using a standard lift-out technique in a FEI Helios Dualbeam Nanolab 600 Focused Ion Beam (FIB) system[28]. To prepare the plan-view TEM samples from a particular region of the sample containing the templates, a modified technique based on Li et al. is followed[29]. A wedge-shaped area containing the templates was lifted out from the surface of the sample using above mentioned FIB technique and thereafter thinned from the back using the gallium beam milling

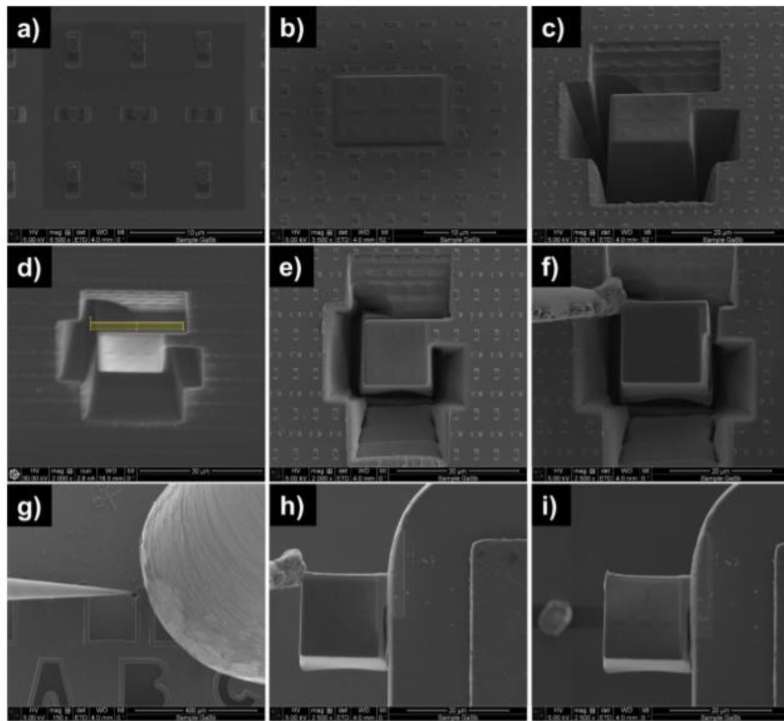


Figure 4.7. Steps for plan view lift-out (a) Top SEM view of area of interest with a protective carbon layer. (b) Same area as (a) after deposition of a thicker protective layer of ion-beam carbon. (c) After cutting trenches on three sides of the area of interest (d) Sample at 0° tilt with area marked out for ion-beam milling to create a wedge (e) after milling using Ga ion beam and formation of wedge (f) attachment of Omniprobe needle and cutting out right bridge to free the wedge structure (g) zoomed out view of copper grid with Omniprobe needle and the gas injection system needle (h) after attachment of lamella to copper grid. (i) after detachment of Omniprobe needle (reprinted with permission from [27]. Copyright {2020} American Physical Society).

until it was electron transparent. This technique allowed site specific wide area (11µm × 10 µm) electron transparent lamellas which were around 200 nm thick and could accommodate a 3 × 4 array of the CELO templates thus giving results from multiple CELO grown structures from a single TEM lamella.

To prepare the area specific plan-view TEM samples, the 1cm x 1cm square diced CELO sample was mounted on a standard metal stub covered with copper tape, with a piece of carbon tape contacting the top corner edge of the sample. The TEM Cu grid was put face down on the sample with an edge contacting the carbon tape to keep it from falling when tilted inside the SEM. The right orientation of the Cu grid has to be ensured so that the flat surface of the Cu grid is facing the top. This is essential for proper in-plane transfer of the lamella. Once the alignments are done in the SEM, two protective carbon layers, one using an electron beam deposition (200nm thick with 5kV 0.69nA beam) and the other using an ion-beam deposition (500nm thick with 16kV 1.4nA beam) were deposited on top of the CELO templates (without removing top oxide layers). Subsequently the sample was tilted to 52° and 4 regular cross-section (RCS) trenches (using 30kV 9.3nA ion beams) about 17um deep were cut out on the 4 sides (slightly shorter on one side to keep it attached to the sample once the trench milling has been done) of the rectangular carbon deposited area.

After running a 30kV 6.5nA cleaning cross section (CCS) on all sides to clear off the redepositions, the sample was tilted back to 0° and using a 30kV 2.8nA ion beam, a rectangle was milled to release most of the bottom of the wedge.The final step involves bringing in the Omniprobe needle and attaching it to one corner of the lamella using Pt deposition, followed by cutting off the small bridge that kept the lamella attached to the sample. Once the lamella

is free, the lifted-out lamella is attached to the stem of the Cu grid using Pt deposition and detached from the Omniprobe needle (Figure 4.7). At this stage, the sample is taken out of the SEM and the Cu grid is remounted vertically. Next using a 30kV 2.8nA ion beam, the wedge-shaped structure is thinned from the back until about 400nm thick. Using 30kV 0.47nA ion beam, the structure is further thinned until we are close to the top carbon layer. This layer is measured to be around 200nm thick. A lower current of 0.28nA is used to further thin it until the back of the templates just starts to be visible in the SEM contrast. Finally, a 5kV 1.5nA beam setting is used to do a final polish. The lamella is then rotated 180° to thin out the front side and remove redepositions from the lift out. The same 5kV beam is used to make a couple

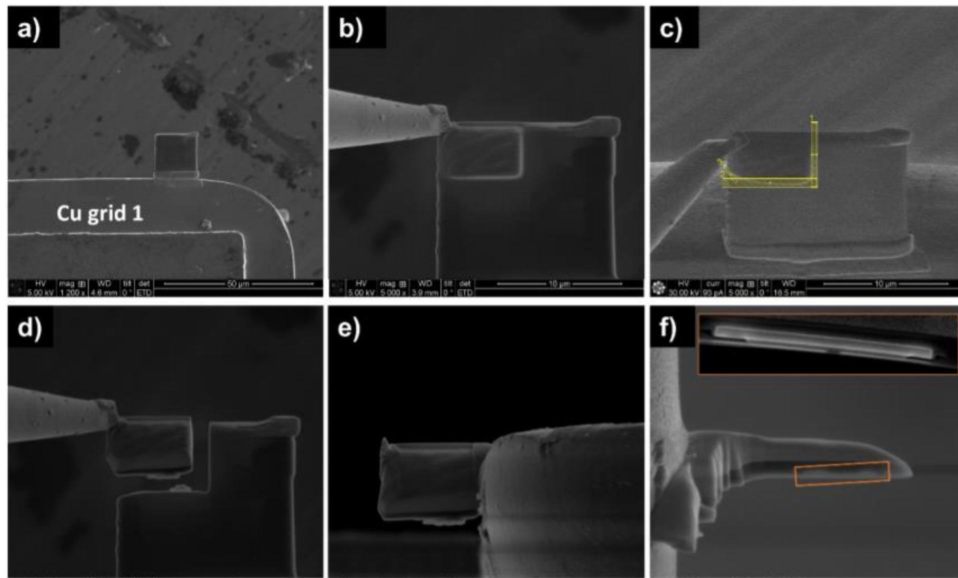


Figure 4.8. Steps for cross-section of plan view lamella liftout using FIB (a) Plan-view Lamella attached to a copper grid (b) Omniprobe needle attached to a corner of the area of interest after deposition of protective carbon layer (c) Rectangle pattern for ion beam cut-out (d) Are of interest after ion-beam cutting (e) New lamella attached to another copper grid holder (f) After thinning down of lamella in (e) using Ga ionbeam. Orange inset shows a zoomed SEM image of the electron transparent cross section (reprinted with permission from [27]. Copyright {2020} American Physical Society).

of passes until the top of the templates look uniformly darker than the rest of the lamella, thus indicating that it is only a thin film of carbon covering the top of these templates. Keeping the lamellas thicker generally produced better results because it avoids damage or non-uniform ablation of these templates.

After comprehensive TEM analysis of the plan-view samples, the plan-view lamella was put back into the FIB to make a cross-section sample out of a specific region of the lamella. The area of interest on the plan-view lamella was protected by in situ deposited Pt, lifted out and subsequently thinned down in steps (Fig 4.8). The ion beam settings used were 30kV 0.47nA at 52° till the template structure is visible from both sides of the lamella. Then the beam voltage is lowered to 5kV 1.4nA to thin it down further. Final polishing was performed at 2kV 47pA at a 2-degree tilt on either side. Care was taken to keep the incident beam angle of the lamella against the ion beam relatively low (less than 2◦, unlike conventional cross-sectional TEM lamella thinning) to prevent damaging the region of interest at the bottom 100 nm of the lamella. Thus, a cross-sectional sample from a plan-view sample can be achieved. One of the advantages of this method is that multiple such cross-sectional samples can be prepared from the same plan-view lamella if they are sufficiently far apart. This is therefore a

comprehensive and fast feedback method applicable to characterizing other nanostructures as well.

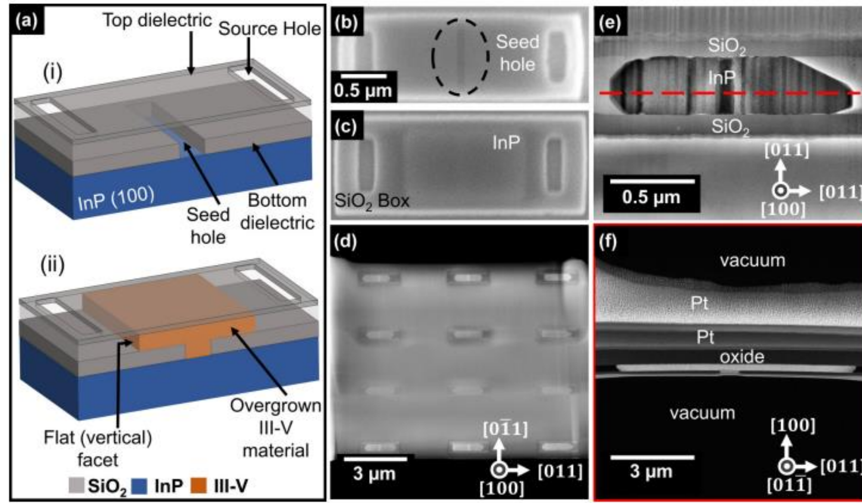


Figure 4.9 a) Schematic of CELO template before growth (a.i) and after III-V overgrowth (a.ii) (b), (c), respectively, show top-down scanning electron microscopy images of a CELO template before growth and after InP overgrowth. (d) High-angle annular dark field (HAADF) STEM of a plan-view lamella containing CELO structures post-InP growth. (e) Plan-view bright field STEM image of a CELO template with grown InP inside it. The light and dark contrast corresponds to regions with and without defects. (f) Cross-section HAADF STEM from the plan-view sample (e) along the red dashed line (reprinted with permission from [27]. Copyright {2020} American Physical Society).

The plan-view lamellas were inspected and analyzed in a FEI Titan 80–300 kV FEG TEM STEM using the scanning TEM (STEM) mode at 300 kV. The high beam current makes sure that a considerable signal can be achieved from a relatively thick sample with a convergent beam. For the bright field (BF) STEM images, the sample was aligned to a zone axis and a 50-μm objective aperture was used to select the central transmitted beam. This is a particularly useful technique to study defects and dislocations in thicker TEM samples[30], [31]. High-angle annular dark field (HAADF) STEM images are also acquired for the same structures to inspect any variation of chemical composition using Z (atomic number) contrast. The cross-sectional lamellas made from the plan-view lamellas further corroborate this information. Dark

field (DF) TEM and HAADF STEM on these cross-sectional samples are used to correlate the defects and dislocations observed in plan-view imaging with cross-sectional data.

By using a combination of plan-view STEM, cross-sectional dark field TEM, and cross-sectional STEM of the CELO templates, a complete picture of the facets and defects can be achieved.

IV C.(iii) Effects of growth temperature on facets of InP CELO on (100) InP substrate

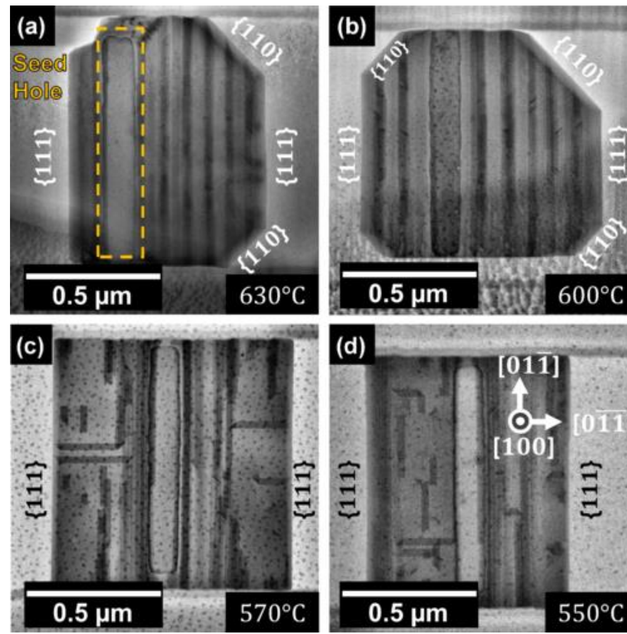


Figure 4.10. BF STEM plan-view images of InP CELO grown on (100) InP substrates at different growth temperatures of (a) 630 °C, (b) 600 °C, (c) 570 °C, and (d) 550 °C. The samples (a), (b) grown at higher temperatures show {110} type side facets and {111} type end facets (plan-view STEM cannot distinguish between, for instance, $(1\bar{1}0)$ and $(\bar{1}\bar{1}0)$ or between $(1\bar{1}\bar{1})A$ and $(\bar{1}\bar{1}\bar{1})B$. Hence, {110} or {111} is used). The samples (c), (d) grown at lower temperatures show rectangular overgrowths with primarily {111} type end facets. The orientation of all the samples is the same [as shown in (d)] and the

direction of the template is along $[0\bar{1}\bar{1}]$ (reprinted with permission from [27]. Copyright {2020} American Physical Society).

To understand the effects of growth temperature on the evolution of facets in CELO nanostructures, the growths were performed at four different temperatures of 630°C, 600°C, 570°C, and 550°C. The growths were performed on a (100) InP substrate in a metalorganic chemical vapor deposition (MOCVD) chamber using a V/III (TBP/TMIn) ratio of 450. Plan-view STEM is used to characterize the facets and defects in these structures (Figure 4.9).

It was observed that the high-temperature growths (630°C and 600°C) exhibit two {110} type side facets which form 45° angles to the template direction (along [011]), along with a {111} facet forming a 90° angle to the template direction [Figs. 2(a) and 2(b)]. The low-temperature growths (570 °C and 550 °C) result in predominantly rectangular shaped overgrowths with {111} facets [Figs. 4.10(c) and 4.10(d)] at an angle of 90° to the template direction. To further assess the structural quality of these crystals, we performed cross-sectional STEM on the plan-view STEM lamellas. To understand the exact orientation of the end facets, we looked at both the plan-view and cross-sectional STEM of a CELO nanostructure, grown at 600°C (Figure 4.11).

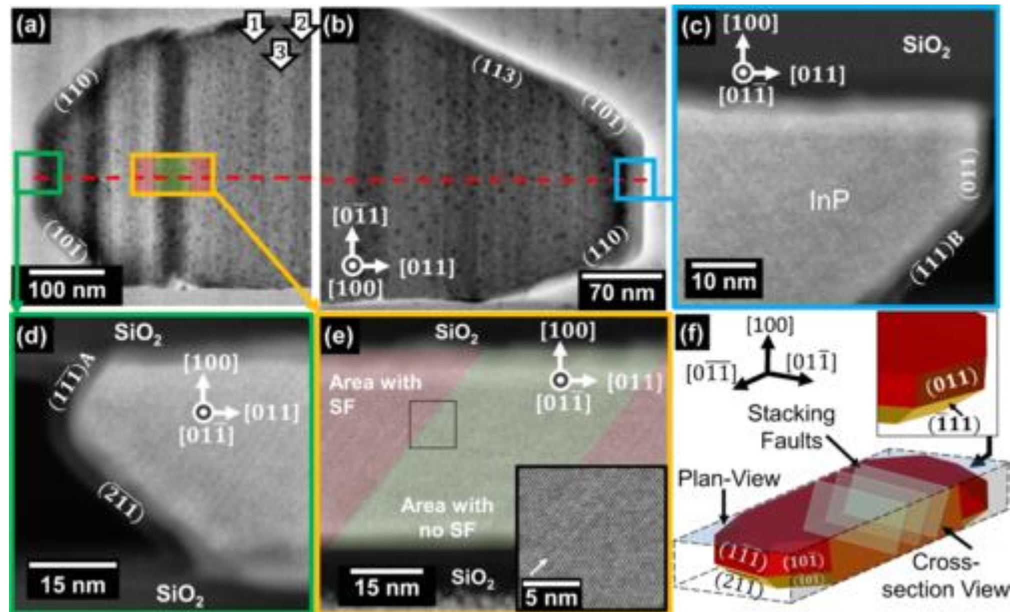


Figure 4.11 InP CELO grown on (100) InP at 600 °C. (a) BF STEM image of the plan-view sample showing defective (light) and non-defective (dark) areas. White arrows (1,2) point to two relatively defect-free areas, arrow 3 points to a defect-dense area. (b) Shows the plan-view BF STEM of the other end of the same growth. (c) HAADF STEM of cross section taken along red line in (b) showing a (011) and a $(\bar{1}11)$ B facet. (d) Cross-section STEM of the plan-view lamella in (a) taken along the red dashed line showing $(1\bar{1}\bar{1})$A and $(\bar{2}\bar{1}\bar{1})$B end facets. (e) STEM corresponding to the area marked by the yellow box in (a) showing a defect-free region (green) in between areas with high densities of SFs and twins (red). Inset shows a high-resolution STEM of the region marked by the black square. White arrow points to a stacking fault. (f) Three-dimensional (3D) visualization of the facets in this overgrowth (reprinted with permission from [27]. Copyright {2020} American Physical Society).

In this high temperature growth mode, large {110} type facets (marked by red dotted lines) appear in combination with {111} facets. Cross-sectional STEM reveals that the left end of the overgrowth shows a combination of small $(1\bar{1}\bar{1})$ A and large (211) B facets [Figure 4.11 (d)] and a combination of {111} B and {110} facets [Figure 4.11 (c)] on the right end. Cross-sectional STEM images confirm the side facets to be {110} type. The structures also occasionally show the appearance of other higher-order facets, such as (113) [Figure 4.11 (b)]. Thus, at high temperatures, we observe a combination of {110} and {111} (mostly B type) facets. We then examine the facets in low-temperature growth by performing STEM analysis

on a CELO sample grown at 570 °C (Fig. 4.12). The plan-view STEM [Fig. 4.12(a)] and its cross-section [Figs. 4.12(b)–4.12(d)] images show that the end facets in this case are primarily {111} B type facets with only a small fraction of {110} type facets. Both ends of the overgrown structure show the same facet combinations. At 45° to the direction of the template, the {110} facets either do not appear, or are very small. Therefore, at low-temperature growths we can effectively eliminate any side facets and have a single growth front composed of {110} and {111} B facets. Thus, these result show that the growth temperature plays an important role in tuning the ratio of the {111} B to the {110} facets in the CELO nanostructures grown on (100) InP substrates.

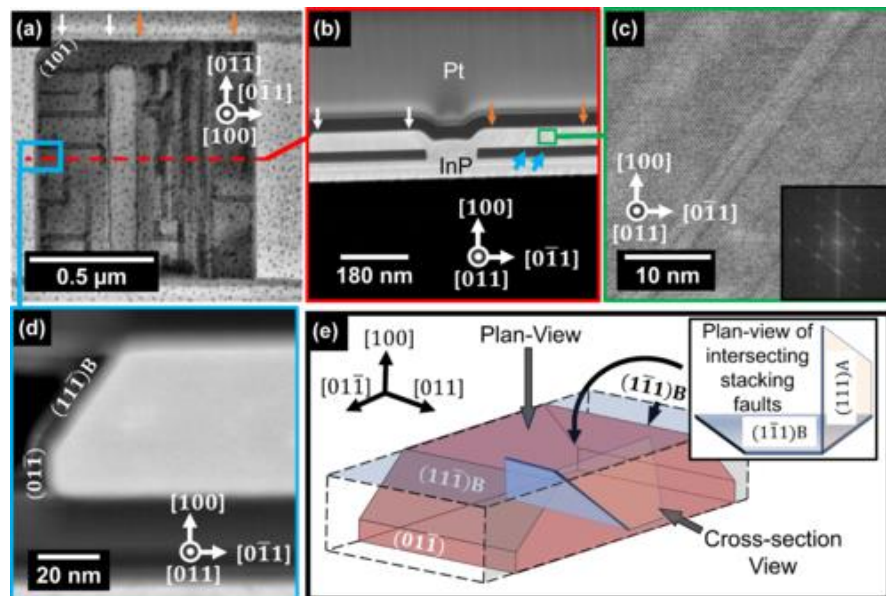


Figure 4.12 InP CELO on InP (100) substrates grown at 570 °C. (a) BF STEM of a CELO structure showing defects as dark contrasts.(b) shows HAADF STEM of a cross-sectional cut taken along red dashed line in (a). In (a), (b) orange and white arrows show limits of defective and defect-free regions, respectively. Blue arrow marks SFs in the defective part. (c) shows a high-resolution cross-section STEM of the region marked by a blue box in (b). Inset shows Fourier transform with the streaks along [111] corresponding to the SFs. (d) shows cross-sectional STEM of the end facet marked by the blue box in (a). (e) shows a 3D visualization of the facets and orientation of the intersecting stacking fault planes. The inset shows the pair of intersecting SFs as seen when looking along the top gray arrow (plan view) (reprinted with permission from [27]. Copyright {2020} American Physical Society).

IV C. (iv) Effects of growth temperature on defects of InP CELO on (100) InP substrate

To understand the impact of growth temperature on defect formation, we again analyze the STEM micrographs to map the position and orientation of the defects. The light and dark contrasts in plan-view STEMs provide crucial information on the crystal quality. For example, in a crystal aligned to a major zone axis, such as [110], areas of high crystalline quality are expected to appear relatively dark in bright field (BF) STEM. This is due to the high diffraction probability of the incident beam electrons by one of the many sets of atomic planes close to their Bragg diffraction condition, and subsequently getting blocked by the objective aperture in a BF mode[30], [31]. Conversely, areas that have a high concentration of stacking faults and planar defects will appear lighter. This is due to the lower interaction cross section of the incident beam with these areas of reduced long-range crystalline order.

In the samples grown at high temperature [Figures 4.10(a)-(b), 4.11(a)-(b)], we observe alternate bands of light and dark contrast in the plan-view TEM image indicating areas with and without defects. In Figure 4.11(a), the white arrows marked 1 and 2 correspond to regions with low density of defects (hence darker), while arrow 3 points to a region with a high density of stacking faults (hence lighter). Dark field cross-sectional TEM images confirm this result. HR STEM [Figure 4.11(e)] images collected from the cross section along red dashed line in Figure 4.11(a) confirm that the bands of dark contrast [Figs. 4.11(a) and 4.11(e), green shaded part of yellow box] are areas of pure zinc-blende InP crystal with no defects. Neighboring areas [Figs. 4.11(a) and 4.11(e), red shaded parts of yellow box] with stacking faults or a mix of zinc-blende and wurtzite crystal phases appear as lighter contrast in the plan-view STEM

image. The brightness of these lighter regions full of stacking faults or mixed phases roughly correlates to the density of defects. The width of the alternating dark and light bands are uniform over CELO structures from the same sample. Thus, at high temperatures we observe areas of the overgrowth exhibiting a high density of stacking faults in between areas of crystals with no defects.

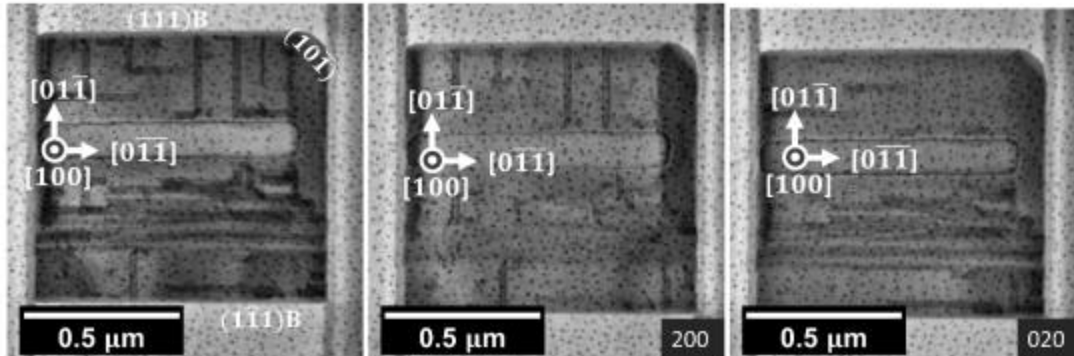


Figure 4.13. CELO for low growth temperature (570 °C) on (100) InP substrate. The contrast from the perpendicular trapezoidal regions disappears at two different two beam conditions(reprinted with permission from [27]. Copyright {2020} American Physical Society).

When grown at a lower temperature (570 °C), the CELO samples have far fewer defects compared to the high temperature grown samples (Fig. 4.12). Notably, large areas of the crystal appear completely free of planar defects. However, we observe some stacking faults, which appear as darker trapezoids intersecting each other perpendicularly throughout the whole crystal. (200) and (020) two beam conditions in the TEM show contrasts that are consistent (Figure 4.13). The stacking faults are in the {111} B planes and perpendicularly intersect, possibly along a line dislocation [Figure 4.12(e)]. Isolated stacking faults also appear, bound on both sides by partial dislocations. The high-resolution cross-sectional STEM taken on the lamella cut along the red dashed line [Figs. 4.12(a)–(c)] confirms the presence of these stacking faults along the {111} B planes. Thus, low-temperature growths show nanostructures with

significantly fewer defects than for the high-temperature growths. Growth temperature is therefore an important control knob to lower the density of defects observed in these CELO grown structures.

IV C.(v) Effects of P/In ratio for CELO on a (100) InP substrate

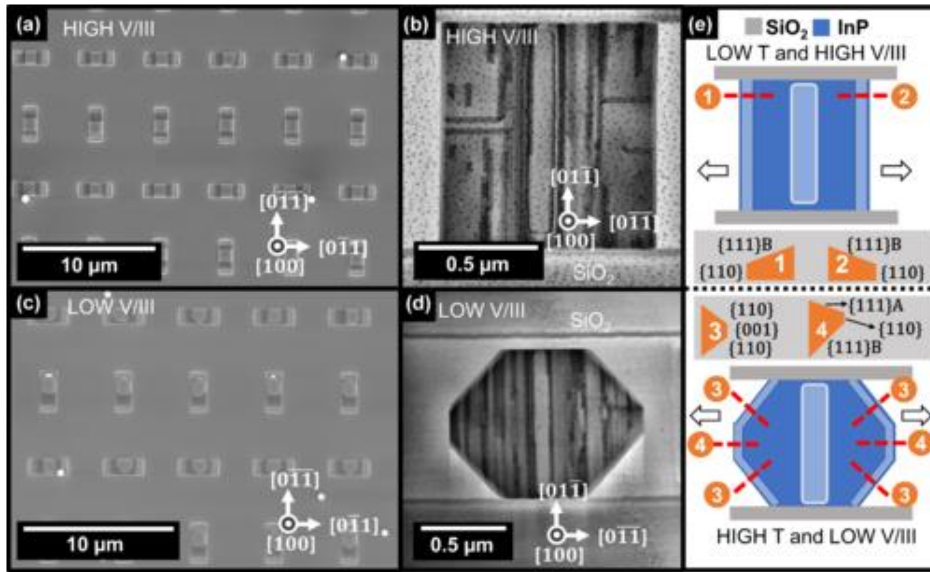


Figure 4.14 InP CELO growths on (100) InP substrate at 570 °C with different V/III ratios. (a), (b) show the top-view SEM (of a region with multiple CELO templates) and BF STEM of a representative structure, respectively, for a growth done at a high V/III ratio of 700. (c), (d) show the top-view SEM (of regions with multiple CELO templates) and BF STEM of a representative structure, respectively, for a growth done at low V/III ratio of 240. The scale bars in (a), (c) are both 10 µm. (e) shows a schematic top-down view representation of the change in faceting with temperature and V/III ratio. The insets show cross-section schematics of the facets observed, where the relative ratio of the facets varies. The arrows in (e) point to the growth direction out of the center seed hole (reprinted with permission from [27]. Copyright {2020} American Physical Society).

Surface energies of facets and growth rates are often dependent on the V/III ratio during growth and can significantly control final facet morphologies in CELO. Therefore, we explore the impact of V/III ratios during growth in controlling facets and defects of InP CELO

nanostructures. For this, two InP CELO samples were grown at 570 °C at two different V/III ratios of 450 and 225, by adjusting the group-V flux and keeping the group-III flow fixed at 4 $\times$ 10^{-6} mol/min. Overgrowths containing {111} type end facets [Fig. 4.14(b)] were predominantly observed in the higher V/III ratio growth. The lower V/III ratio growth, on the other hand, yields a higher percentage of {110} facets, which are at 45° to the template direction [Fig. 4.14(d)]. Comparing dependence of growths on temperature (Fig. 4.10) and V/III ratios (Fig. 4.14), we observe that high V/III ratio [Fig. 4.14(b)] and low temperature [Figs. 4.10(c) - (d)] have similar facets and defects. Samples grown at low V/III ratio [Fig. 4.14(d)] and high temperature [Figs. 4.10(a) and 4.10(b)] also show similar facets and defects. Therefore, similar to temperature, V/III ratio gives us a second control knob in tuning the facets and defects in CELO grown InP nanostructures. In effect, by changing temperature or V/III ratios we can adjust the relative stabilities or growth rates of different facets.

IV C. (vi) Influence of template orientation for CELO on (100) InP substrate

To examine the effects of growing along different template orientations, we fabricate CELO templates along different directions at 18◦ intervals away from the [011] [Fig. 4.15(a)]. We grew this at 570 °C because this temperature previously led to lower defect density (Fig 4.10). From the previous results (Fig. 4.14), a low-temperature growth should result in a higher fraction of {111}B type facets compared to {110} facets in the final structures. This is confirmed by the plan-view BF STEM (Fig. 4.15). The growths in the templates oriented along the [010] direction show regions with the largest area of defect-free overgrown crystal [Fig. 4.15(b)]. Stacking faults form along the edges, parallel to the {110} side facets. The total area of the growth varies with the orientation of the templates [Fig. 4.15(g)], decreasing from the

maximum in templates aligned along [010] to a minimum for templates along [$0\bar{1}1$], and then increasing again. Similarly, as the direction of the template changes from being oriented along [0 1 0] [Fig. 4.15(b)] to being oriented along [$0\bar{1}1$], the area of defect-free crystal decreases and stacking faults increase throughout the crystal [Fig. 4.15(e)]. This is illustrated in the plot of Fig. 4.15(h). Note that the stacking faults appear to be nucleated at the mask sidewalls suggesting that optimal template orientations can be used to design CELO overgrowths with a lower density of defects.

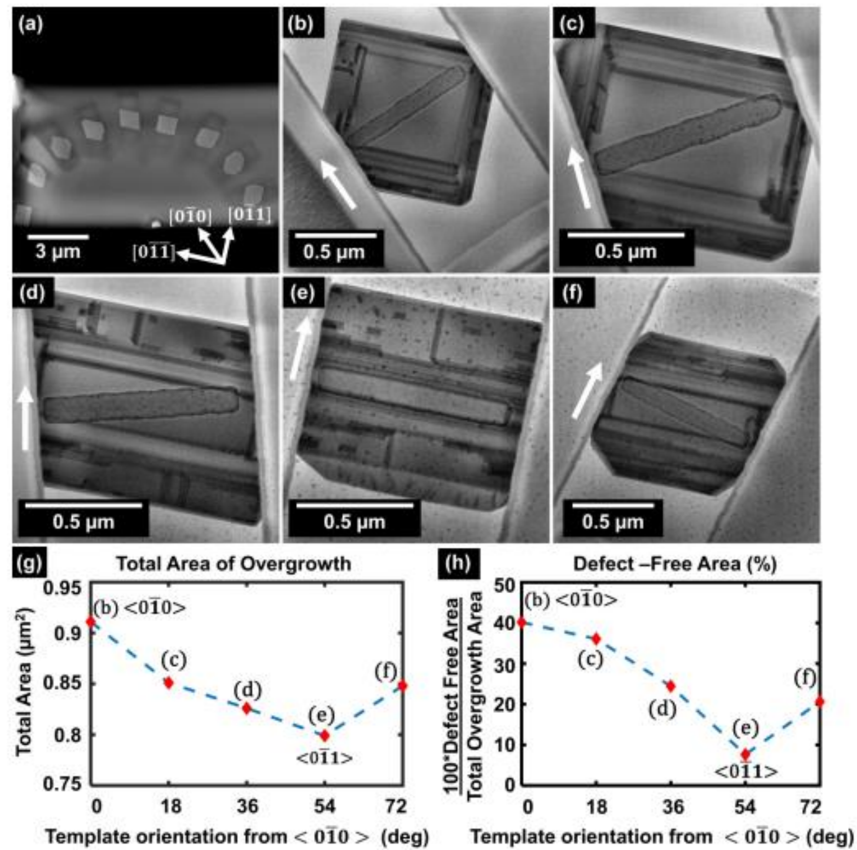


Figure 4.15 Plan-view TEM micrographs analyzing growth in different orientations on a (100) InP substrate. (a) shows the HAADF STEM of the entire lamella with a flower pattern of CELO templates starting from the one oriented along [110] and with separations of 18° between consecutive templates. (b)–(f) BF STEM of individual templates oriented in different directions on the wafer. The nature and density of defects change as the orientations of the templates vary from [$0\bar{1}\bar{1}$] to [$0\bar{1}1$]. The white arrows

point to the direction that the templates are oriented. (g) shows the total area of overgrown III-V materials in each of these templates and (h) shows the fraction of defect-free area in the different samples (reprinted with permission from [27]. Copyright {2020} American Physical Society).

IV C.(vii). CELO on a (110) InP substrate

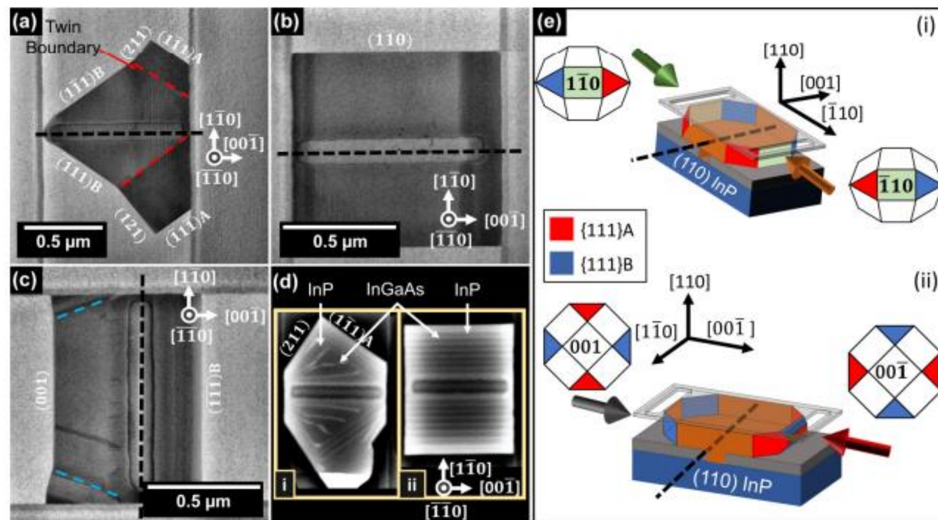


Figure 4.16 Plan-view TEM of InP CELO grown on InP(110) substrates. (a), (b) show representative growths in templates oriented along [110]. (a) shows twinning along the {111}A planes (red dashed line); (b) shows perfect sharp {110} type vertical flat facets. (c) shows CELO growth in templates oriented along [100]. The growth towards ⟨100⟩ orientation is terminated by a sharp {100} facet while the ⟨00$\bar{1}$⟩ orientation is terminated by {111}B facets. There are edge twins on the side growing towards ⟨001⟩ . Twin planes are marked by blue dashed lines. (d) shows backscatter SEM of two different growths in templates oriented along [110]. The bright lines are InGaAs markers in between InP growths. (e) shows how the crystal facets on the growth plane are different depending on which orientation the crystal grows in. The red and blue planes represent the {111}A and {111}B planes, respectively. The Miller cubes shown correspond to how it would look when viewed along the corresponding arrows (reprinted with permission from [27]. Copyright {2020} American Physical Society).

For fabricating lateral heterojunction-based devices, heterojunctions with single facets perpendicular to the lateral growth direction of the template are optimal[4]–[6]. From our study of growth on (100) InP substrates, the ratios of the {110} and {111} facets can be adjusted using temperature and V/III ratio. This suggests that changing the substrate orientation and choosing the correct template alignments might enable the {111} or {110} surfaces to form the desirable perpendicular flat facet structures. A (110) substrate can potentially allow the formation of this perpendicular {110} facet, since {111} planes are absent in the $[1\bar{1}0]$ direction of growth. Therefore, we explored CELO growths on a (110) type InP substrate as a possible route to achieving these vertical facets.

The templates examined here are oriented either towards [001] or [110]. This orientation on the (110) InP substrate is crucial, since unlike the (100) substrate the mutually perpendicular [001] and [110] growth directions offer asymmetric crystallographic planes to grow on. As a result, the growths in these perpendicular templates will be different and need to be explored separately. In addition, we grew InP CELO samples with InGaAs spacers. The lattice matched InGaAs layers appear brighter in STEM due to Z contrast and help elucidate the progress of the growth front from the start of the growth to the final facets. The facet shapes remain unchanged with the introduction of the InGaAs layer. In the (110) growths we observed tunability of final facets in overgrowths using template orientation, ultimately leading to a defect-free overgrowth with perfect flat facets. A large number of growths in the templates directed along [110] are twinned along {111}A [red dashed lines, Fig. 4.16(a)]. A combination of {111}A, {112}, and {111}B facets terminate the growth along with the formation of twins. Comparing the total length of growth in each orientation, the growth rates appear higher on {111}A compared to {111}B [Fig. 4.16 (a)]. The initial portion of the crystal growth close to

the seed hole contains no defects, until the formation of the twin. The twinned part of the crystal has a high density of stacking faults. Occasionally we also found a small number of stacking faults running along the direction of growth.

The most striking observation in these CELO growths on (110) InP substrates is the formation of flat {110} vertical facets in the templates oriented along [$1\bar{1}0$] [Fig. 4.16 (b)]. Such growths have a perfect rectangular shape and appear to show no defects from the plan-view STEM studies. The yield of such nanostructures is currently about 20%. InGaAs spacer layers lattice matched to InP track the evolution of growths in the lateral overgrowths in such [110] oriented templates [Fig. 4.16 (d)]. Top-view SEM backscatter images show that in the structures that result in {111} final facets, the {111}A facets grow as growth times proceeds [Fig. 4.16 (d.i)]. However, in the overgrowths displaying the perfect flat facets, the growth happens entirely on a single {110} surface [Fig. 4.16 (d.ii)]. Figure 4.16 (d.ii) also clearly demonstrates that lateral heterojunctions with flat facets are achievable. Growing in templates oriented along [100] orientation yields a mixture of flat (001) facets and {111}B facets in these templates in [Fig. 4.16 (c)].

The orientations <00$\bar{1}$> and <001> offer different crystallographic planes for growth, resulting in different end facets for the growth in a single template [Fig. 4.16 (e)]. Here, the growth front has two {111}B top and bottom planes and two other {111}A side planes when looking along <00$\bar{1}$>. The A and B planes get interchanged when viewing along <001>. Growths towards <00$\bar{1}$> are mostly terminated by {111}B type facets and form stacking faults [along blue {111}B planes in Fig. 4.16 (e.ii)]. The growths on the other side of the seed hole (towards <001>) are terminated by flat (001) type vertical facets perpendicular to the template, sometimes accompanied by small higher-order side facets, such as {211}. The growths towards

<001> are relatively defect free, with a few occasional stacking faults at the edges and small twins at the corner edges [blue dashed lines in Fig. 4.16 (c)]. Thus, we demonstrate that on a (110) InP substrate, defect-free CELO overgrowths with vertical flat facets can be achieved in templates aligned along [110]. The perpendicular templates along [001] also form nanostructures with flat {001} facets on one end, which can also find use in fabricating lateral heterojunctions.

IV C. (viii) a. DISCUSSION: FACETS

We observe that in CELO overgrowths on a (100) InP substrate growth, temperature and V/III ratio control the final facet shapes of the nanostructures (Figs. 4.10 and 4.14). At high growth temperature (T > 600 ° C), {110} and {111} facets form, while at temperatures below 570 °C, primarily {111}B facets form (Fig. 4.10). Similar tuning of facet ratios is achieved by changing the group-V/group-III flux ratios at 570 °C (Fig. 4.14). Collectively, these results suggest that the facet ratios are controlled by the effective phosphorus overpressure (chemical potential) on the facets, which, can be changed by both temperature and V/III ratio. Changing surface reconstructions on different facets changes their surface energies and growth rates. Density functional theory and other first principle calculations predict that, for a {111}B surface of InP, a high phosphorus overpressure will form P trimers, resulting in a (2×2) surface reconstruction[32]–[34]. Similar As trimer formation has been previously reported on GaAs epitaxial lateral overgrowth[35]–[37]. These stable P trimers significantly suppress the growth rate on the {111}B planes, as they block sites for the

attachment of the incoming In atoms/trimethylindium molecules[38]. This reduces the effective indium incorporation coefficient on the {111}B surface, resulting in the growth rate of other surfaces, such as the {110} surfaces, dominating the growth. The {111}B thus becomes the slowest growing and dominant surviving facet of the structure[39] for highly effective group-V overpressure (high V/III or low-temperature growth condition). However, at lower effective phosphorus overpressure (achieved either by higher growth temperature or low V/III flux ratio), large {110} type facets and smaller {111}B facets are formed. This arises from the effective V/III ratio decreasing and the (2 × 2) P trimer surface reconstruction becomes less favorable resulting in an In-rich (√3 × √3) surface becoming more stable[33]. This increases the In incorporation ratio and hence, the growth rate on the {111}B surface. Therefore for (100) substrates, V/III ratio and growth temperature can control the ratio of {110} and {111}B surface areas in the CELO nanostructures. This offers tunability of facets and shapes of selective area grown nanostructures to fabricate nanoscale devices with desired geometries.

Despite achieving this control over tuning facet ratios, the dominating final facets in CELO grown on (100) substrates are a combination of {110} and {111}B. This limits the use of these nanostructures for horizontal heterojunctions, for lack of flat single facets perpendicular to the lateral direction of growth. To achieve such flat lateral perpendicular facets, we explored a (110) InP substrate, where in a template aligned along <110>, {111} B planes are absent in the direction of growth. This provides an opportunity to form flat perpendicular facets in the direction of growth. A large number of the growths in these templates, however, show twinned crystal growths [Fig. 4.16 (a)]. From the InGaAs marker layer growths [Fig 4.16 (d.i)], we assume that a small {111}A facet was formed in the overgrowth immediately after it extended out of the seed hole. As the growth proceeded, more

precursor materials diffuse to the {110} facet from the {111}A surface (which has a lower growth rate). The nonuniform diffusion causes the {110} surface to grow thicker on the side closer to the {111}A facet, thus forming a slanted growth front. As the growth proceeds further, the {110} is completely transformed to a {112}B and then the growth proceeds primarily on the {111}A surface. The growth can stop on a {111}B instead of a {112}B giving rise to the facets seen in Fig. 4.16 (a). However, when the {111} facet does not form at the start, the crystal can grow entirely on the {110} surface. This results in completely flat and vertical {110} facets [Fig. 4.16 (b)]. The InGaAs markers included in the growth confirm this growth evolution [Fig. 4.16 (d.ii)]. A critical factor in achieving these facets is the suppression of the {111}A facet as the material grows out of the seed hole. This process is assumed to be affected partly by the roughness of the dielectric sidewalls, as explained in the "Defects" section below.

Hence, we have demonstrated that the $\langle 1\bar{1}0 \rangle$ oriented templates on a (110) InP substrate can form flat vertical facet surfaces, which is one of the main requirements in building horizontal lateral heterojunctions and superlattices with flat interfaces. Templates oriented along the <001> orientation also produce flat {001} facets on one end of the nanostructures [Fig. 4.16 (c)]. This is of key interest because the 001 orientation of a CELO template oriented along <100> might offer another favorable direction to achieve lateral heterojunctions. The results of this study can be extended to other IIIV CELO growth systems. Although the III-V nucleation on other mismatched substrates (such as Si) is different from homoepitaxy, once the epitaxial layer starts growing out on top of the oxide template, the same growth mechanism and facet dependencies on temperature and V/III ratio should apply.

IV C.(viii).b Discussion : Defects

Growth temperature and V/III ratios play a significant role in changing defect type and density in CELO grown nanostructures on a (100) InP substrate. At lower temperatures or high V/III ratios during growth, the growth along the {111}B planes is suppressed and growth proceeds more on the {110} surfaces. This growth suppression lowers the number of planar defects that form on the {111} planes (Figs. 4.10 and 4.14). The trapezoidal shape of the stacking faults arises from the interference fringes from one or more closely located stacking faults[40]. Low-temperature or high V/III ratio growth also exhibits stacking faults bound by partial dislocations [41] and incomplete stacking fault pyramidal loops. These defects are known to be generated by various stress mechanisms induced by thermal expansion coefficient mismatch[42]. This suggests that roughness or thermal expansion mismatch induced stress from the CELO oxide sidewalls might lead to these defects. At higher growth temperature or lower V/III ratio, the increased growth rate on the {111}B surfaces favors the formation of bands of stacking faults and twins along the growth front. These planar defects are aligned along the {111}B plane, consistent with the fact that the {111} plane is the primary twinning plane for III-V semiconductors[43], [44].

At high temperatures, isolated stacking faults do not appear. This is possibly because the defects are more mobile at elevated temperatures, enabling them to spread to the edges of the nanostructures. Many of the defects appear to be generated from interaction of the growing III-V material with the rough sidewalls of the template (Fig. 4.14). In a confined system such as CELO, the roughness of the inner sidewalls of the template can play a significant role in defect formation. Interaction of the III-V crystal with a rough oxide has been reported to cause bond distortions in GaAs, leading to formation of twins and stacking faults[45]. In our case,

we hypothesize that etching induced roughness of the oxide sidewalls (of both the seed and template) contributes to the formation of stacking faults. In addition, it must be noted that the thermal expansion coefficient for InP is $\alpha = 4.6 \times 10^{-6}$ °C^{-1} while that of SiO is $\alpha = 0.5 \times 10^{-6}$ °C^{-1}. This large thermal expansion mismatch will result in stress in the InP epitaxial lateral overgrowth upon cooling after growth [46]–[51]. The highest stress appears at the edges of the oxide template, which is likely to result in stacking faults and twins starting at the edge of the dielectric [47]. While high V/III ratios during growth lower the defect densities in the overgrown template farther away from the seed hole, no considerable changes in the defect densities near the seed hole were observed (Fig. 4.14). A detailed study to decouple the effects of local growth parameters, oxide roughness, and thermal expansion mismatch in defect generation is beyond the scope of this thesis. We observe that the orientation of the templates impacts the defect densities. On InP(100), growths in the templates oriented along the [001] direction [Fig. 4.15(b)] show regions with the largest area of defect-free overgrown crystal. This result agrees with the study by Staudinger et al. [43]. The growth in the [001] orientation is free of any {111} planes along the direction of growth, thus reducing the formation of stacking faults. The growths, however, show the formation of stacking faults along the side facets, which contain {111} planes. As the direction of the template changes from being oriented along [001] [Fig. 4.15(b)] to being directed along [110] [Fig. 4.15(e)], the growth front has a higher percentage of {111} planes. As a result, we see stacking faults increase and the areas of defect-free crystal decrease. The interaction of III-V materials with a SiO2 surface contributes to the formation of the stacking faults, as mentioned above. Therefore, we demonstrate that overgrowths with larger areas in contact with the sidewalls will show a higher number of defects (Fig. 4.15).

On a (110) InP substrate, if the growth occurs primarily on the {110} surfaces, the likelihood of forming twinning or stacking faults is lower compared to growth on the {111} surfaces. Thus, in <110> oriented templates on a (110) substrate, when a higher fraction of the growth front is along <110> a relatively defect-free crystal forms. Subsequently, after twin formation, when growth proceeds primarily on a {111} surface, stacking faults appear [Fig. 4.16 (a)]. Such stacking faults also appear in growths along 001 where the growth front consists of {111}B surfaces. If, however, the growth proceeds entirely on the {110} surface, no defects appear in the entire structure [Fig. 4.16(b)]. Such defect-free nanostructures with perpendicular flat facets can enable the fabrication of high-quality lateral heterojunction devices. Similarly, growths in the <001> have very few stacking faults, as growth happens primarily on the {001} surface. By choosing template orientations, we can effectively lower the defect densities for nanostructures grown on a (110) substrate. It should be noted here that, in addition to the CELO induced defects observed in this study, for heteroepitaxial III-V CELO growth on mismatched substrates (such as Si), additional dislocations, stacking faults, and antiphase boundaries will result from lattice and symmetry mismatch. Although the oxide template beside the seed hole should in principle trap most of these defects, it is not always guaranteed and often they can spread into the overgrown epitaxial layer.

IV C.(ix). Conclusion

In conclusion, we demonstrate that for homoepitaxial InP CELO on InP substrates, the facets, defect types, and defect densities all depend heavily on the growth conditions, such as temperature, V/III ratio, template orientation, and InP substrate orientation. For (100) InP substrates, high growth temperature (or low V/III ratio) results in nanostructures with a combination of {110} and {111}B type facets. Conversely, for low growth temperature (or

high V/III ratio), {111}B end facets dominate. We attribute this dependence on temperature and V/III ratios to surface energies and formation of phosphorus trimers in phosphorus-rich environments suppressing growth on the {111}B plane. We also show that low growth temperature (or high V/III ratio) and alignment of templates along [010] together can give very low defect densities on a (100) InP substrate. To achieve vertical facets critical for growing lateral heterojunctions, we utilize templates aligned along [110] on a (110) InP substrate. With these templates, we demonstrate nearly defect-free and perfectly vertical {110} type facets, with a single growth front – making them promising for the formation of lateral heterojunctions with flat vertical interfaces. Such horizontal heterojunctions will be discussed in depth in the next section. Our results show the ability to grow CELO nanostructures with well-controlled facets. This will widen applications of CELO for fabricating quantum well based devices, where orientations of the quantum wells are crucial for harnessing the benefits of orientation dependent carrier confinement and mobility.

IV D. Horizontal heterojunctions in CELO

In this section, we demonstrate that CELO can be a novel and efficient way to grow various lateral horizontal heterojunctions (HJ) for a number of HJ-based devices. The previous section provided us with the correct substrate orientation and template orientation to grow perfectly vertical facets and horizontal junctions (namely a (110) InP substrate and a $[1\bar{1}0]$ oriented template). Here, we demonstrate the successful growth of an InP/InAs HJ, (important for telecom wavelength room temperature lasers), InP/GaAs HJ (important for a type-II band alignment exhibiting interesting quantum-confinement properties), an InGaAs/InP triple quantum well (important for energy filtering applications[52], [53]) and a InP/InAs/GaAs/InP triple heterojunction (3HJ) structure (important for the proposed high on-current TFET). Cross-sectional high-resolution transmission electron microscopy (TEM) analysis shows the high quality of the material grown.

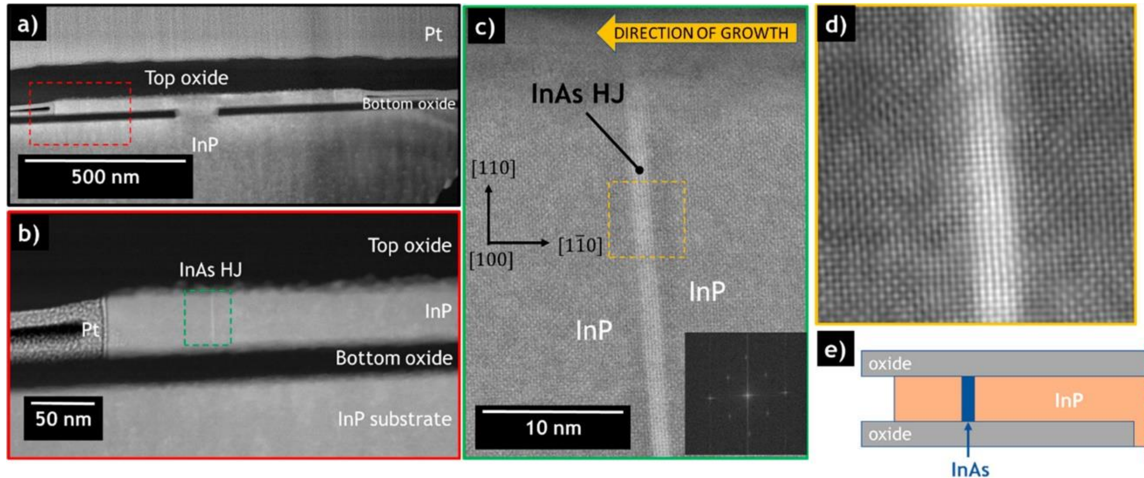


Figure 4.17: Cross section of a confined growth of InP with an InAs layer. (a–c) HAADF-STEM imaging. (d) Detail of the InAs HJ (with applied Fourier filtering). (inset) Electron diffraction pattern for the InAs. (e) Schematic diagram of the structure. (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

The InP/InAs/InP HJ (Figure 4.17) exhibits defect-free abrupt heterointerfaces in high-resolution STEM imaging. The InAs layer grown is ~1.5 nm thick (below the Matthew

Blakeslee critical thickness for InAs on InP, which is ~2.1 nm for a 3.2% lattice mismatch). Strain maps (Figure 4.18) made using geometric phase analysis shows the strain in the InAs layer and no relaxion. InP/GaAs/InP horizontal heterojunctions (Figure 4.19) also exhibit abrupt, vertical interfaces, with perfect crystallinity.

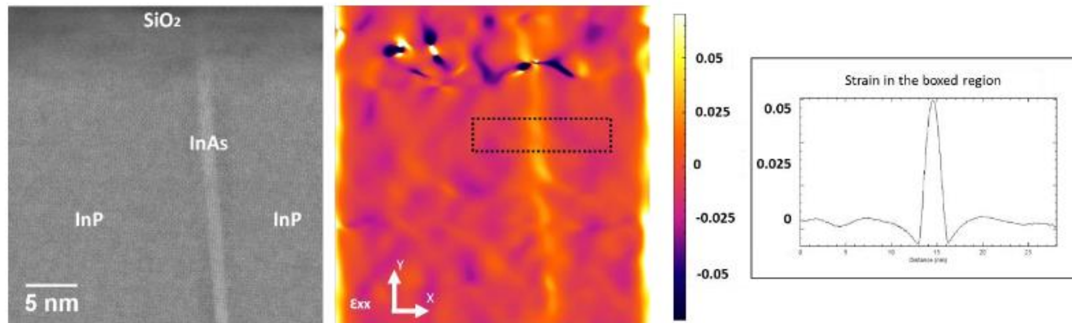


Figure 4.18 Strain map across the InAs HJ showing presence of strain in the InAs layer and an abrupt change in strain value across the heterointerfaces. (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

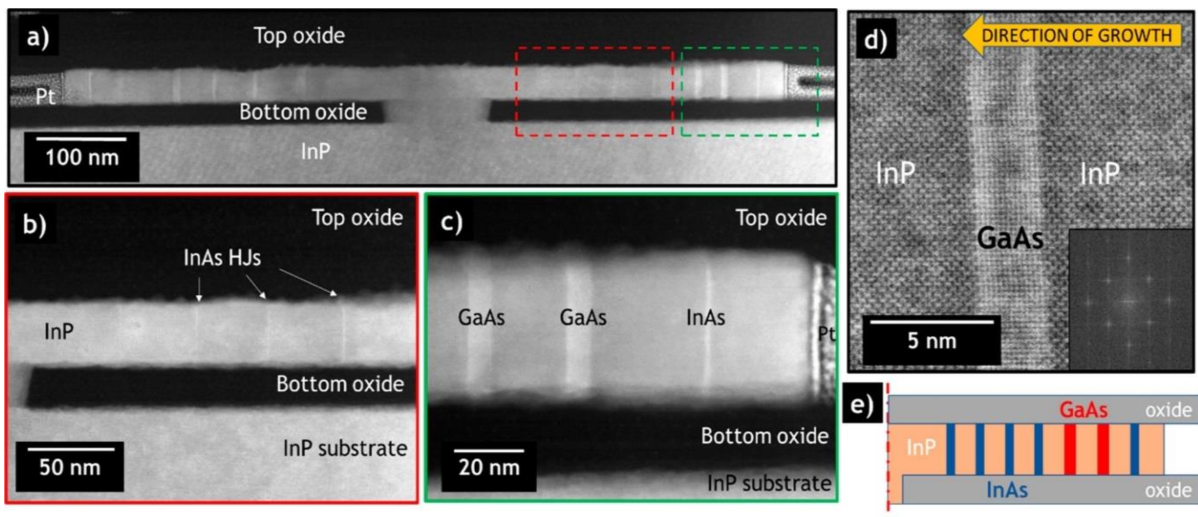


Figure 4.19 Cross section of a confined InP growth with InAs and GaAs layers. (a–c) HAADF-STEM imaging. (d) Detail of a GaAs HJ (with applied Fourier filtering) from a similar growth. (inset) Electron diffraction pattern for the GaAs. (e) Schematic diagram of the structure (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

A three-well InP/InGaAs superlattice was grown. The growth is asymmetric across the seed and such growth asymmetries in CELO are discussed in the following sections. After the superlattice, a thick InGaAs layer was included, to act as a contact layer in a final superlattice filter device[52],[53]. The facets are flat, and the interfaces are abrupt. As/P intermixing, a common problem when switching group V during growth results in slightly fuzzy boundaries between InGaAs and InP. Damage of the lamella from focused ion beam (FIB) induced gallium damage possibly contributed to the "blurriness" of the interface.

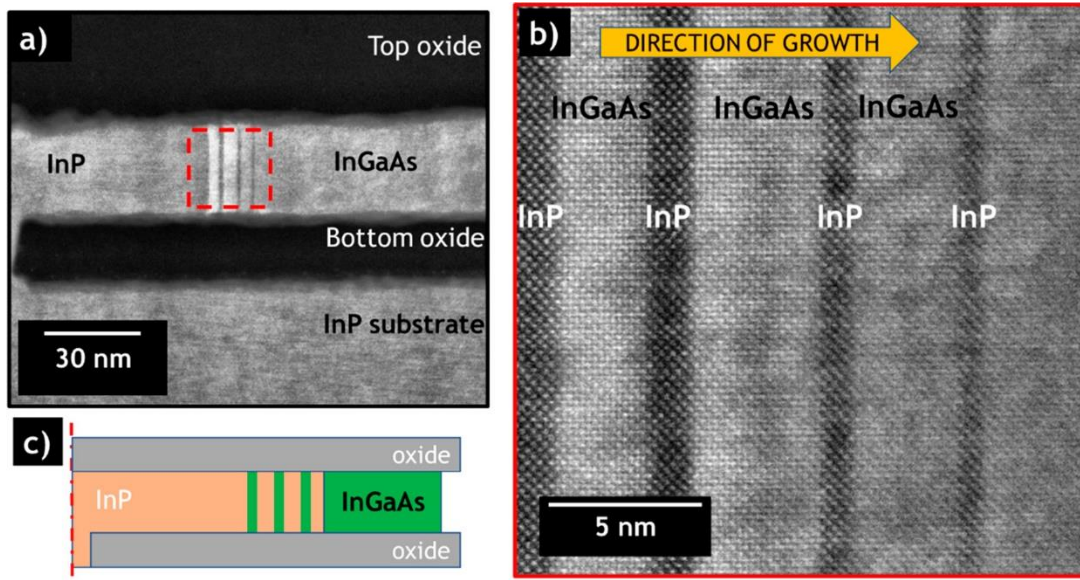


Figure 4.20 Cross section of an InP and InGaAs growth with InP/InGaAs HJs. (a, b) HAADF-STEM imaging. (c) Schematic diagram of the structure (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

Compositional gradients in bulk ternary material via confined epitaxy due to differences in the diffusion between the group III precursors have been reported in literature previously. We executed a TEM energy-dispersive spectroscopy (EDS) measurement to verify this in the CELO InGaAs growth. The change in In composition along the cavity shown in Figure 4.19, suggested by measuring the InL/AsL and the GaK/AsK, is 15% and 10%, respectively, measured from seed to growth front across 350 nm. Once the gradient is known, progressively adjusting the molar flow ratio of precursors during the growth should lead to a

constant composition within the cavity. This also presents an opportunity for the use of CELO in growing graded ternary compounds automatically.

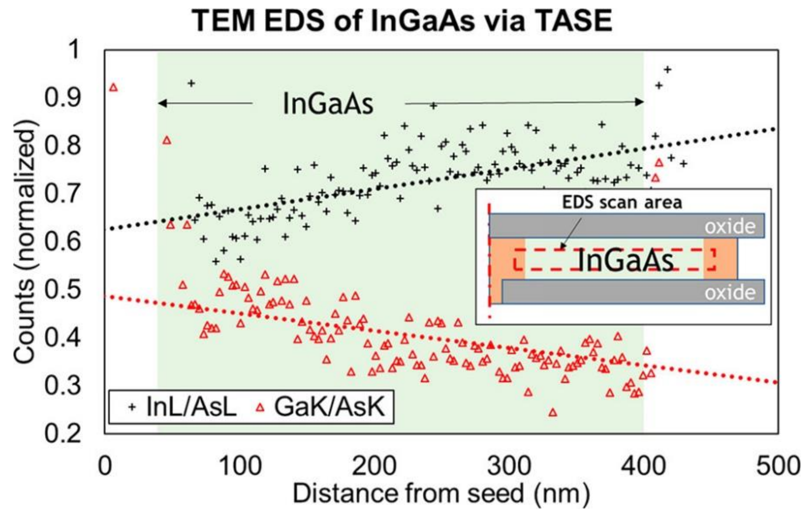


Figure 4.21 TEM EDS data of an InGaAs growth via TASE/CELO. The plot shows InL and GaK counts normalized to AsL and GaK, respectively. The green area indicates the position of the InGaAs inside the template. (inset) Schematic diagram of the structure (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

Lastly, a triple heterojunction structure, consisting of InP/GaAs/InAs/InP with InAs growth markers was demonstrated and cross-sectional TEMs are shown in Figure 4.22. Again, the growth is not symmetrical, with the left side being longer than the right, as clearly seen in Figure 4.22 (e). Comparing the left and right sides of the template, seen in Figure 4.22 (a-b), the same HJs are present with scaled spacing and thicknesses. It is possible that the growth initiated asymmetrically due to non-uniformities in the seed trench or non-uniformities in the template box itself. Since growth is faster (discussed more in the next section) the farther it is away from the source hole, the growth rates could have been highly different during the growth start. The effects were less as the growth was closer to the source hole for easier mass transport. This asymmetric growth behavior is seen in other SAG literature[54] but requires further investigation.

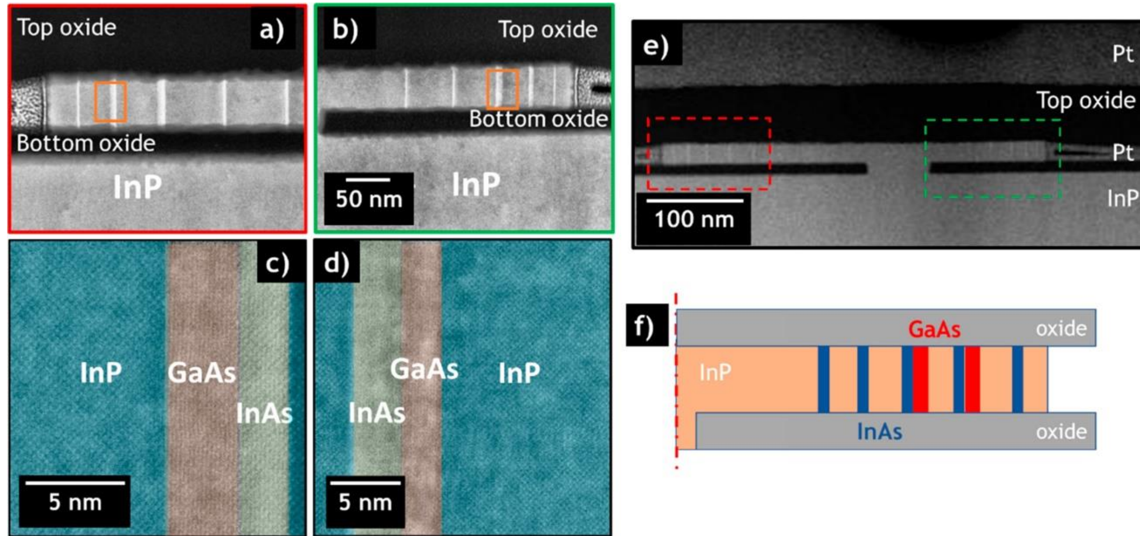


Figure 4.22 Cross section of an InP growth with InP/InAs/GaAs triple heterojunction and InAs marker layers. (a-b and e) cross-sectional HAADF-STEM (c-d) corresponding high resolution images showing one triple heterojunction (f) a schematic of the structure (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

Growth Rate Inside the Template. Including HJs enables tracking of the progression of growth and changes in growth rate (R_g) within the confined cavity. The presence of different materials changes the surface energy at the growth front, and thus the growth initiation, but on first approximation measuring the thickness of the InP spacers between the HJs provides an estimate on R_g in the cavity. The length of the InP layers between the HJs shown in Figure 4.19 and Figure 4.22 was measured and divided by the individual growth time for that layer to obtain the average growth rate for each. This average growth rate is then plotted versus distance from seed in Figure 4.23. InP spacers in the 3HJ sample grown under the same conditions and for the same time, exhibit a reduction of growth rate with increasing distance from the seed hole (Figure 4.23). This is in contrast with expectations: during the confined epitaxy the growth front advances toward the source hole, reducing the distance between them, and since MOCVD

growth is driven by diffusion, growth rates are then expected to increase with time, as has been observed in previous studies. A possible cause of this reduction of R_g is the presence of nonselective growth, that is, parasitic nucleation on the dielectric. While selectivity is almost perfect for InP homoepitaxy, arsenic-containing growths are more prone to forming parasitic growths. With the progression of growth these parasitic nucleation, being exposed to the precursors directly, quickly and disproportionately increase in size due to the low fill factor and consequent strong loading effect typical of SAG. We hypothesize that these parasitics, when located near template source holes, act as capture sites for the metal organic precursors in the nearby gas phase, partially impeding diffusion inside the templates. The effect is a local lowering of the precursor molar flow toward the growth interface, thus reducing Rg of the confined growth. The other explanation is that at a high growth temperature there is also significant desorption of precursors and as the growth nears the source holes, the desorption rate also increases thus reducing total growth rate.

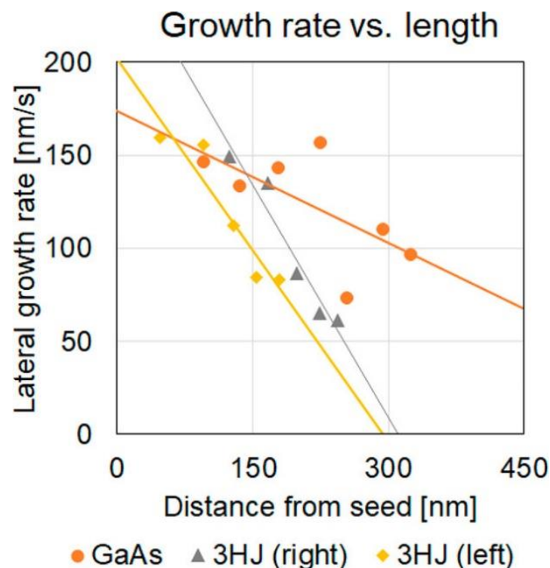


Figure 4.23 Average lateral growth rates for the individual InP layers between the HJs (reprinted with permission from [14]. Copyright {2019} American Chemical Society).

Conclusion: In conclusion, the integration of multiple horizontal heterojunctions in a dielectric template via confined epitaxy in MOCVD is demonstrated. This is to the best of our knowledge, the first demonstration of such multiple lateral quantum well systems. The use of templates fabricated on (110) InP wafers and oriented along the $[1\bar{1}0]$ results in flat vertical facets that enable abrupt quantum-well heterostructures. The structures are grown laterally thus allowing for planar gating of devices. STEM imaging is used to show the achieved abrupt interfaces between layers and the preserved crystalline order across the junctions. The structures presented are building blocks for novel electronic devices that rely on HJs to be aligned to specific crystal orientations and geometry like, for example, 3HJ TFETs and SL energy-filter FETs.

IV E. Electrical characterization of InGaAs CELO

Material properties in nanostructures, such as CELO, often deviate significantly from those of planar epitaxial structures grown under similar conditions [55]–[57]. For example, depending on growth conditions, CELO-grown III–V materials exhibit variations in defect densities [27], spatial gradients in ternary compositions, and facet-specific group-III incorporations [58]. Quantum confinement in these low-dimensional nanostructures can result in a change in band parabolicity leading to changes in carrier effective mass and mobilities. As a result, electrically characterizing CELO nanostructures is crucial for both understanding material qualities and optimizing growth conditions.

Unfortunately, as mentioned in the previous section, CELO growths often exhibit unwanted III–V nucleation [Figs. 4.24(a)–(c)] on the dielectric mask, also known as parasitic growth[59]. Growing CELO nanostructures with no parasitic nucleation is challenging and often requires constraining the growth parameters within a narrow window, which may not yield the highest electronic properties. Clear and precise alignment marks are essential for further device processing requiring sub-micrometer alignments. Epitaxial growths of a few hundred nanometers inside the CELO templates often result in parasitic nucleation that are tens of micrometers in size [13]. Preferential nucleation of parasitic growths on rough edges of the patterned dielectric often covers these alignment marks completely. This makes the sample alignment required for further lithographic processing of CELO structures nearly impossible. In addition, due to the rough oxide topography resulting from nucleation, there is a high failure rate in forming metal contacts to the nanostructures. Hence, a method to circumvent the parasitic growth is required in order to enable further processing of these nanostructures into devices for subsequent electrical characterization.

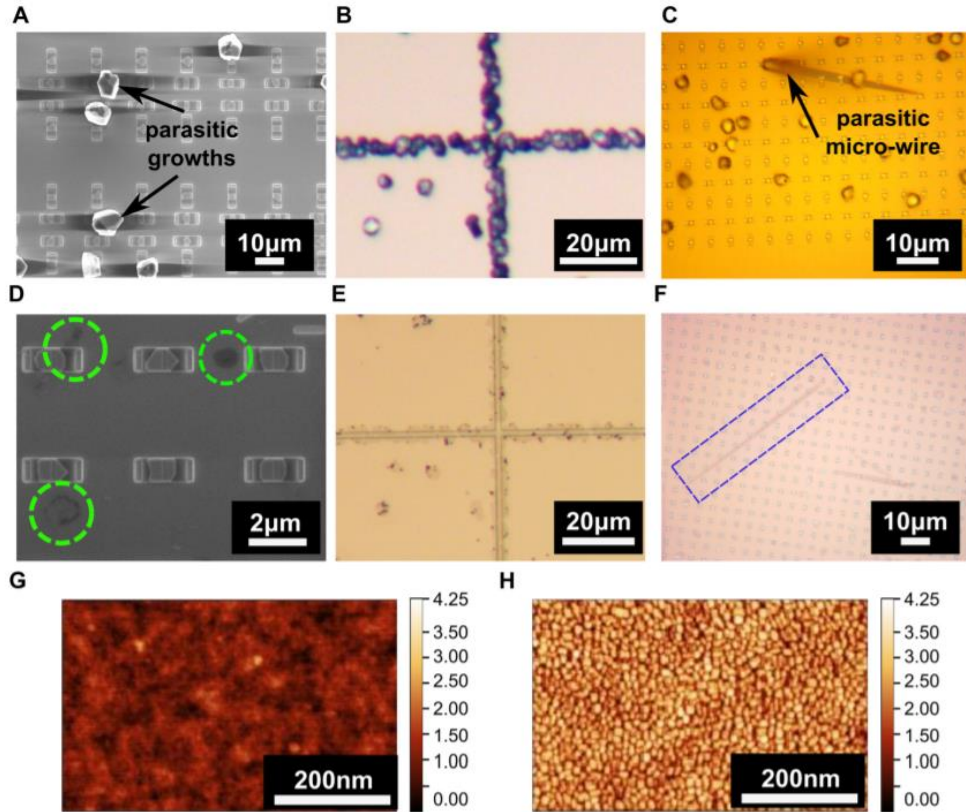


Figure 4.24 (a), (b), and (c) show a CELO InGaAs sample and (d), (e), and (f) the corresponding samples after the cleaning processes described in the text. (a) and (d) are SEM images, while (b), (c), (e), and (f) are optical microscope images. Green circles in (d) show where parasitic growths were before the cleaning process. Dashed box in (f) shows a region (different from c) where a parasitic microwire growth existed before etching. (g) shows the surface of SiO2 after the wet etch process. (h) shows the SiO2 surface after 20 min of exposure to MHA plasma etch in the RIE (reproduced from [60] with permission from AIP publishing).

In this section, we demonstrate a rapid, yet gentle multi-step etch method, which removes the parasitic growths while leaving the growths inside the template undisturbed. With the successful removal of parasitic growths, it is now possible to fabricate devices and perform electrical measurements, which opens up the possibility of investigating a broad range of materials and growth conditions. In this study, we explore the technologically relevant InGaAs material system. This material's high electron mobility and direct bandgap makes it attractive

for a wide range of electronic and photonic applications, especially for telecommunications, high frequency electronics, and topological quantum computing [61]–[67]. Electrical transport measurements at low temperatures can allow us to extract parameters important for the use of InGaAs in semiconductor nanowire networks for Majorana fermions[61], spin field effect transistors,[62]–[64] high-performance nanoelectronics [65], terahertz detectors [66], or optoelectronic devices [67].Here, we demonstrate the fabrication of devices and measurements of magnetoresistance behaviors at cryogenic temperatures for in-plane InGaAs CELO nanostructures in samples with a high density of parasitic growths. We achieve this with the use of the post-growth parasitic growth removal process, which makes the precise alignment and fabrication of contacts possible. Due to the small size of the nanostructures, a two-terminal device design was chosen over making a more conventional four or six contact Hall device for yielding more reliable contacts. From the observed Shubnikov–De Haas (SdH) oscillations in the magnetoresistance of these two terminal devices, we extract doping concentration, effective mass, and quantum mobility in these nanostructures. These measurements clearly reveal variability in material parameters between different growth runs, which is crucial to understand device performance. Thus, the use of our etching process flow allows one to grow with a wider range of growth conditions and materials and their heterostructures in the CELO geometry, optimize the material quality, and fabricate electronic and photonic devices with greater control. The mechanism outlined here is generalizable and can be extended to investigation of interesting physics in the nanostructures of a broad range of other semiconductors, metals, and topological materials.

Solving alignment issues during fabricating devices from samples with parasitic growths

To fabricate a full device, reliable fabrication of vias and contacts are required. The CELO nanostructure dimensions are usually sub-micron. In an EBL system, to expose a pattern, usually automatic alignment is used, to correct for in-plane shifts and rotations. If parasitic growths are covering up most of the alignment marks, this alignment becomes practically impossible. Manual alignment is never accurate enough to align the entire pattern correctly over a wide area. Here, we show results from attempts to align samples (using automatic alignments) with alignment marks covered by parasitic growths **(**Figure 4.25 (a)-(c)**).** The alignment was off on every process run. The vias were misaligned and shifted from

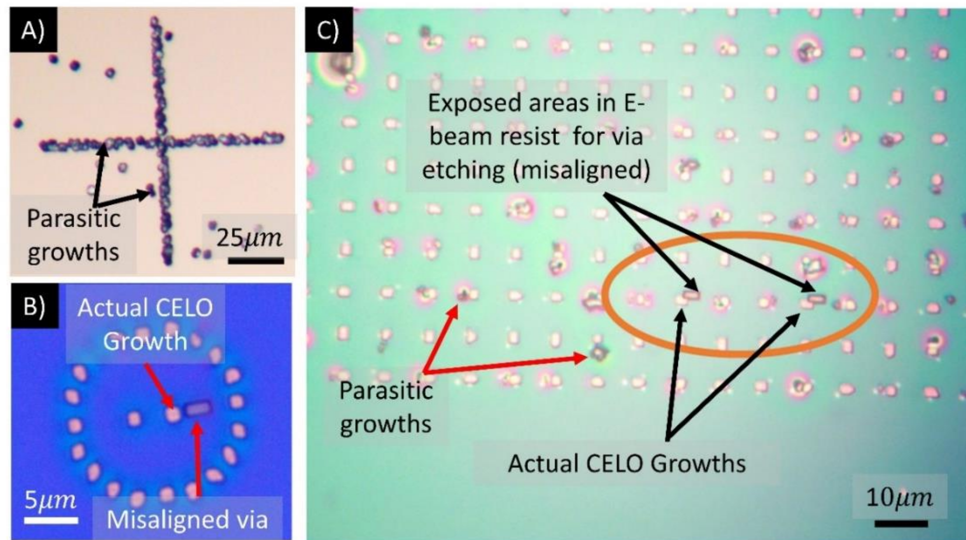


Figure 4.25: (A) shows EBL alignment mark covered in parasitic growths in a CELO sample (B) and (C) show attempts at fabricating devices on that CELO sample. The samples are imaged post development after EBL exposure of vias. The actual CELO growth and the exposed vias are misaligned in two separate parts of the sample as a result of the alignment marks being covered by the parasitic growths(reproduced from [60] with permission from AIP publishing)

the actual CELO growths. This prevented us from fabricating any working devices with samples covered with parasitic growths. In addition, the parasitic growths being tens of

microns in height, result in considerable resist topography around it. As a result, if there is a parasitic growth nearby a targeted CELO device, the exposure and resolution can get seriously affected by the resist topography. This re-emphasizes the importance of removing the parasitic growths before device fabrication. By using the process outlined in the following paragraphs we were able to repeatably fabricate devices with high yield and perform magneto-transport measurements.

Growth using metal organic chemical vapor depositions (MOCVD) was performed in a horizontal reactor using trimethylindium (TMIn), trimethylgallium (TMGa), tertiarybutylphosphine (TBP), and tertiarybutylarsine (TBA) with H_2 as carrier gas. The samples were grown at 600°C, with a group III flux of 5×10^{-6} mol/min and a V/III ratio of 570. For the samples discussed in the study, the growth was initiated with a few monolayers of InP before switching the growth to n-doped InGaAs. Si doping is incorporated in the InGaAs layer with a disilane flux of 1.43×10^{-8} mol/min. Planar epitaxial Si-doped InGaAs samples for carrier density comparison were grown at 600 °C, with a group III flux of 3.82×10^{-5} mol/min, a V/III ratio of 8.8, and a disilane fluxes of 1.43×10^{-8} mol/min. We used a combination of dry and wet etching to selectively remove the parasitic growths (Figure 4.26). After rinsing the sample in acetone and isopropanol, 6 nm aluminum oxide (Al_2O_3) was deposited on the sample in an atomic layer deposition (ALD) chamber using a trimethylaluminum-water (TMA-H_2O) recipe at 300 °C. This conformally coats the sample including the outside surface of the growth inside the CELO templates and the parasitic growth [Figure 4.26 (c)]. The samples were then etched in an inductively coupled plasma (ICP) chamber using BCl_3/Cl_2 chemistry for 15 s with an approximate etch rate of 80 nm/min. Since ICP etching is highly anisotropic, the etch removes Al_2O_3 that is in line of sight of the ions that

are accelerated toward the bottom cathode. The thick silicon dioxide top layer stops the ion beams from etching the Al_2O_3 that covers the outer surfaces of the overgrowths inside the CELO templates [Figure 4.26 (d)]. Similarly, the Al_2O_3 that is underneath the parasitic growths are protected from incoming ions. The ICP etching effectively exposes the top of the parasitic growths while keeping the nanostructures of interest inside the cavity protected by Al_2O_3. It is important to note here that for the successful use of this process, the outer edge of growth inside the CELO cavity should be under the top dielectric and laterally shorter than the seed holes. Otherwise, the ICP etch will remove the ALD dielectric under the seed hole and expose the active area to subsequent etching steps. Using a wet etch we then selectively etched these parasitic growths without affecting the overgrowths in the CELO templates [Figure 4.26 (e)]. For the InGaAs CELO sample, we used a H_3PO_4/H_2O_2/ H_2O (1:1:20) solution for 12 min to etch away the parasitic growths. After careful inspection of the samples to make sure that all parasitic growths had been etched completely, the samples were put into AZ 300 MIF (Metal Ion Free 0.261 N tetramethylammonium hydroxide) developer solution for 5 min to etch away

any remaining Al_2O_3 (etch rate of 1.6 nm/min). A quick rinse in acetone and isopropanol was used to clean any residues.

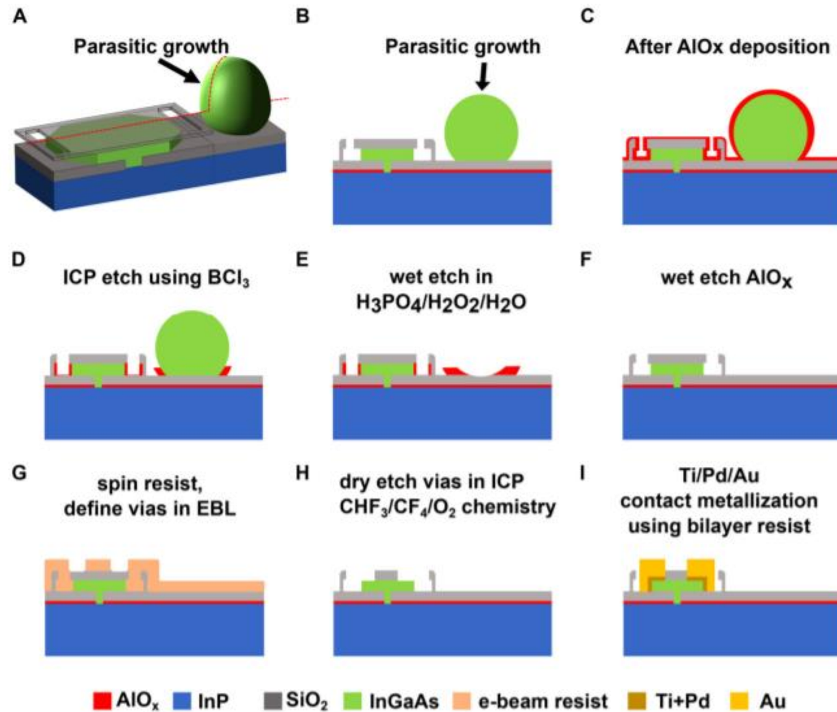


Figure 4.26 (a) shows the 3D schematic of InGaAs CELO growth along with a parasitic growth. (b) shows a cross section schematic taken along the red dashed line in (a). (c)–(i) show the process flow for selectively cleaning parasitic growth and fabrication of vias and contacts. It is critical that the outer edge of the active region (green area in c) is protected by the top dielectric for subsequent etching steps (reproduced from [60] with permission from AIP publishing).

The samples are thus clean of any parasitic growths and with the original overgrown structures intact [Figure 4.26 (f)]. Dark outlines are sometimes observed after the entire cleaning process in the positions where the parasitic growths initially existed [Figure 4.24 (d)]. We hypothesize that these result from local changes in the oxide due to the parasitic growths' nucleation. These dark spots are of negligible thickness and do not pose any problems while aligning samples or depositing contacts. After achieving selective removal of parasitic growths, we were now able to proceed with the device fabrication on the InGaAs CELO

samples. The alignment marks, free of all parasitic growths [Figure 4.24(e)], could now be used in the electron beam lithography (EBL) tool. Using CSAR, vias were defined [Figure 4.24 (g)]. The vias were etched in the silicon dioxide top layer of the CELO templates using a $CHF_3/CF_4/O_2$ recipe in the ICP [Figure 4.26 (h)]. After cleaning the samples in a plasma asher followed by solvent rinse, contacts were patterned using a bilayer resist process. The resist stack consists of 100 nm of copolymer EL9 (ethyl lactate 9%) and 400 nm of PMMA 950 K. To ensure that all remaining surface oxides are etched for making an ohmic contact, a 30 s dilute HCl (1:10) etch was performed immediately before metal deposition. To ensure proper adhesion and ohmicity of the contacts, we deposited a metal stack 10 nm of Ti followed by 10 nm of Pd and 200 nm of Au using electron beam evaporation [Figure 4.26 (i)].

Our process flow achieved successful parasitic growth removal on the InGaAs CELO samples as characterized by scanning electron and optical micrographs [Figs. 4.24 (a)–(f)]. Notably, large micro-wire parasitic growths that were present previously [Fig. 4.24 (c)] were completely removed [Fig. 4.24 (f)]. The contrast from the InGaAs growth inside the templates remains unchanged in the optical microscope and SEM images, indicating that the CELO growths inside the templates are unaffected by this etching process. We compared the effects of our etching process to a conventional plasma-assisted dry etch using a $CH_4/H_2/Ar$ chemistry in a reactive ion etcher (RIE). Although RIE-based etches can partially remove the parasitic growths, the etch rates were found to be low and the time to completely remove thick parasitic growths (which are often tens of micrometers thick) was long (>30–40 min). Atomic force microscopy (AFM) scans revealed that a 20-min RIE etch results in an extremely rough surface oxide [Fig. 4.24 (h)]. Such plasma processes are known to introduce highly mobile defects in semiconductors [68] and deteriorate the quality of the exposed oxide. In comparison, AFM

scans of our wet etch processed samples show that the root mean square roughness of the oxide is considerably lower than that of RIE-etched samples [Fig. 4.24(g)].

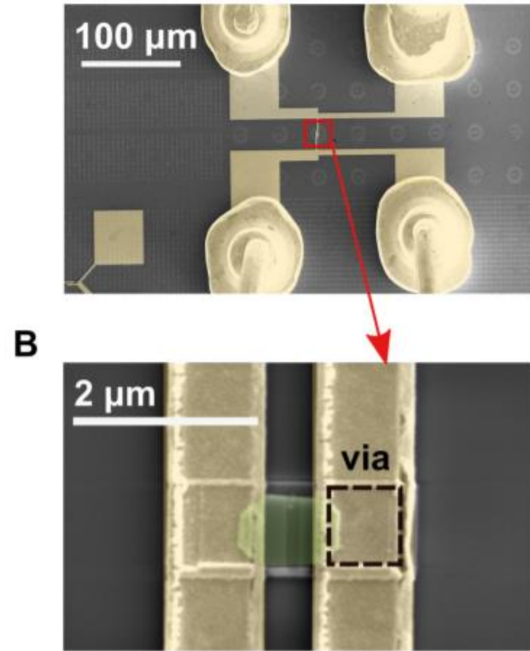


Figure 4.27 (a) False color SEM images of device with contacts and (b) magnified SEM image of the InGaAs CELO device (marked in green) with vias and contacts (reproduced from [60] with permission from AIP publishing)

IV E.(ii). Electrical measurements

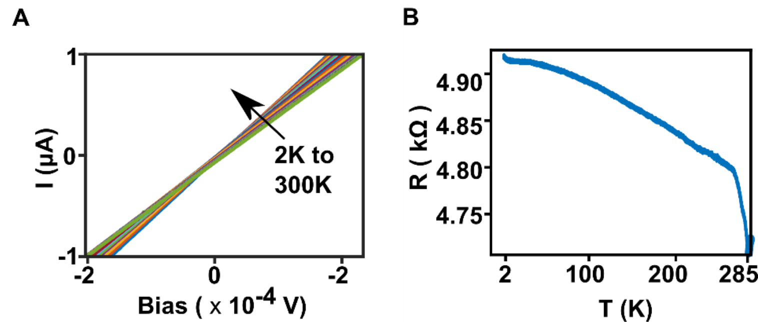


Figure 4.28 : (A) I-V curves at different temperatures(measured in 4-probe configuration for sample 1) (B) Resistance vs Temperature curve for longitudinal resistance (measured in 2-probe configuration for sample 2) ((reproduced from [60] with permission from AIP publishing)

To characterize the material properties of these nanostructures after sample cleaning and fabrication of devices, we use linear two terminal magneto-transport measurements in both

two-terminal and four-terminal (separate probes for current and voltage on the same metal/semiconductor contact) configurations (Figure 4.27). Such transport measurements can help reveal variations in electrical properties of these nanostructures grown under different growth conditions and spatial variations in a single sample. Given the small dimensions of the nanostructures, two-terminal devices offer advantages in terms of fabricating reliable contacts [69], [70] compared to a conventional Hall device, which requires at least four terminals. The technique also avoids variabilities in gate dielectric properties for field effect measurements of mobility. The devices were measured in a Quantum Design Physical Property Measurement System (PPMS). The devices were wire-bonded to a PPMS puck using a 25 μm gold wire. The devices were found to be extremely sensitive to electro-static discharge, so caution was taken to ground the sample while bonding and transfer. The InGaAs devices were measured using standard AC low frequency (13 Hz) lock-in technique at temperatures ranging from 2 to 300 K. The contacts were found to be ohmic at all temperatures [Figure 4.28]. The resistance of the device increases with decreasing temperatures [Figure 4.28].

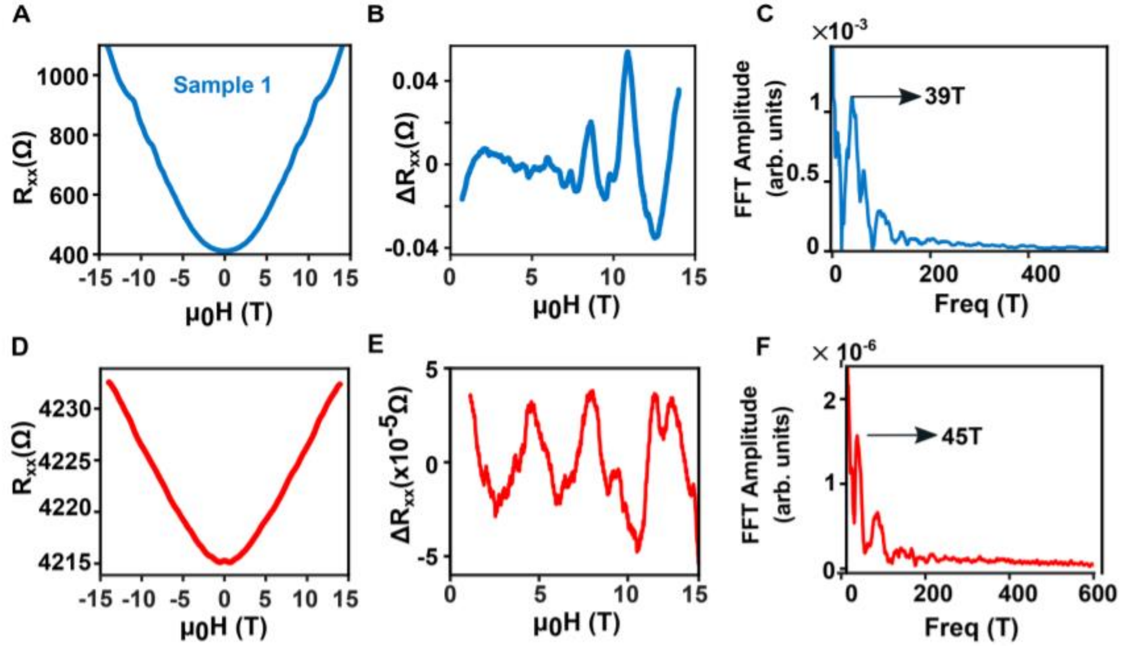


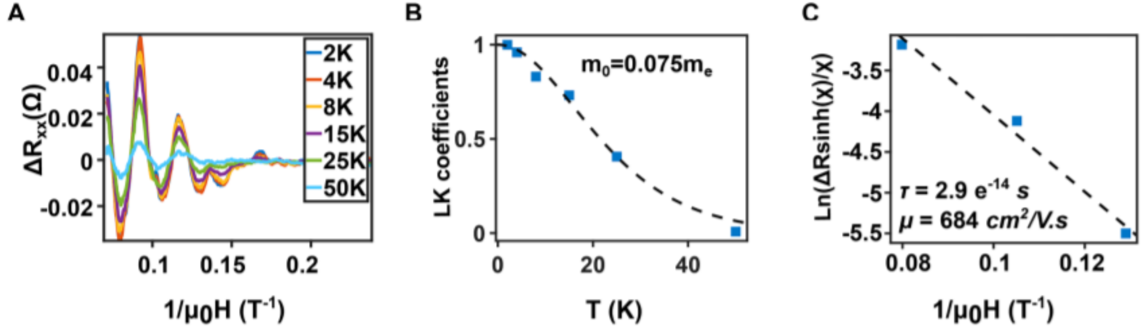
Figure 4.29 : Low-temperature magneto-transport. (a)–(c) show measurements for sample 1 and (d)–(f) show measurements of sample 2. (a) and (d) show longitudinal magnetoresistance for sample 1. (b) and (e) show data in (a) and (d) after background subtraction, respectively. SdH oscillations are visible in both samples. (c) and (f) show the FFT of ΔR_{xx} vs ($1/\mu_0 H$) for the two samples. Peaks are observed for subband oscillations corresponding to 39 and 45 T for samples 1 and 2. These correspond to doping concentrations of 1.4×10^{18} and 1.9×10^{18} cm^{-3}, respectively. Sample 1 was measured in a four-probe configuration, while sample 2 was measured in a two-probe configuration (with 4 kΩ series line resistance). (reproduced from [60] with permission from AIP publishing)

The successful fabrication of contacts on InGaAs CELO samples allows us to perform transport measurements to characterize the material quality in these samples. Magnetoresistance measurements of two samples grown under the same growth conditions and similar Si doping concentrations are explored (Fig. 4.29). Sample 1 [Figs. 4.29(a)–(c)] was measured using a four-probe configuration, while sample 2 [Figs. 4.29(d)–(f)] was measured in a two-probe configuration (for two-probe configuration, total line resistance of 4 kΩ is

effectively added to the device resistance). Longitudinal resistance R_{xx} was measured as a function of a perpendicular magnetic field (applied out of plane to the sample surface) at 2 K. The resistance exhibits positive magnetoresistance with well-defined superimposed oscillations at high fields [Figs. 4.29(a) and 4.29(d)]. A parabolic background is observed in the magneto-resistance plots, which typically arises from the Drude conductivity being inversely related to $[1+(\mu B^2)]$, μ being the mobility and B being the magnetic field. To analyze the observed oscillations more clearly, a third-order polynomial background subtraction was performed [Figs. 4.29(b) and 4.29(e)]. At magnetic fields higher than 2 T, ΔR_{xx} oscillates periodically in an inverse magnetic field (1/B). This can be interpreted as Shubnikov–de Haas oscillations due to the formation of Landau levels (LL) in the high magnetic field. Fast Fourier Transform analysis of the oscillations [Figs. 4.29(c) and 4.29(f)] reveals frequencies of B_F= 39 T and B_F= 45 T corresponding to sample 1 and sample 2, respectively. Assuming a spherical Fermi surface, the Fermi wavevector corresponding to these two frequencies are k_{F1} = 0.3463 nm^{-1} and k_{F2} = 0.3695 nm^{-1} with doping levels of 1.4×10^{18} and 1.9×10^{18} cm^3, respectively. These two samples were expected to show similar behaviors because of same growth conditions but surprisingly revealed variabilities of doping incorporations between different growth runs. This variability further underscores the importance of characterizing material quality in CELO growths.

To compare doping densities in CELO to doping incorporations in conventional planar samples, room temperature Hall measurements were performed on Si-doped planar InGaAs samples. The planar sample was grown with the same disilane flux as for the CELO samples (1.43×10^{-8} mol/min) but with a lower V/ III ratio. The doping concentration measured in this sample was 2.53×10^{18} cm^3. However, it is not straightforward to compare doping densities

from planar growth to CELO nanostructures; because compared to planar epitaxial growth, CELO growths typically require a significantly lower group-III flux to lower parasitic growth rates. Since Si doping in planar InGaAs growths decreases significantly with increasing V/III ratio [71], the Si incorporation at a V/III ratio comparable to a CELO growth is likely lower than this number. As a result, Si doping incorporation in InGaAs CELO appears to be



comparable to doping incorporation in planar epitaxial growths.

Figure 4.30 (a) Shows the background subtracted magnetoresistance for sample 1 [Fig. 4.27(a)] in the inverse field at temperatures from 2 to 50 K measured in a four-probe configuration. (b) Fit of peak amplitude to Lifshitz–Kosevich equation to extract effective mass of m = 0.075 × m_e. (c) shows the Dingle plot extracted from peak amplitudes in (a). Slope from linear fits gives quantum scattering lifetime and quantum mobility (reproduced from [60] with permission from AIP publishing)

To obtain electron effective mass, mobility, and scattering length in these nanostructures, the temperature dependence of SdH oscillations in ΔR_{xx} was analyzed. The amplitude of the SdH oscillations decreases with increasing temperature, but the oscillations are observed distinctly up to 50 K [Fig. 4.30 (a)]. Measuring the resistance values at the peak corresponding to $\frac{1}{B} = 0.092\ T^{-1}$, we fit the peak amplitudes to the Lifshitz–Kosevich equation (LK) [72],

$$\frac{X}{\sinh(X)}, where\ X = \frac{2\pi^2 k_B m_e \left(\frac{1}{B}\right) m^* T}{\hbar e}$$

Here, k_B is the Boltzmann constant; m_e is the rest mass of an electron; m* is the dimensionless effective cyclotron electron mass, i.e., m* = m/me, where m is the mass of electrons in InGaAs; T is the temperature in Kelvin; $\hbar = \frac{h}{2\pi}$, h being the Planck constant; and e is the charge of an electron in Coulombs. From the temperature dependence of the peak amplitude to the LK equation [Fig. 4.30 (b)], the effective mass was estimated to be m = 0.075 × m_e. This value is higher than the typical value of electron effective mass in planar $In_{0.53}Ga_{0.47}As$ samples lattice matched to InP reported in other works [73]. The increase in electron effective mass in CELO InGaAs compared to a planar sample can be because of combination of factors such as higher band parabolicity due to quantum confinement in the nanostructures [74], [75], penetration of electron wavefunction into the barrier oxide layers[76], or possible higher subband occupations[77] . The scattering time τ can be extracted from the slope of the plot of $\ln(\frac{\Delta R_{xx}\sinh(X)}{X})$ vs $\frac{1}{B}$ for the peaks in ΔR [Fig. 4.30 (c)]. The slope value of −45.9 (slope equals to$-\frac{\pi.m}{e.\tau}$) corresponds to an estimated quantum lifetime of τ =2.919 e^{-14} s and a Dingle temperature $T_D = h/(4\pi^2 \times k_B . \tau)$ of 41.6 K. These values of effective mass and scattering time correspond to a quantum mobility of

$$\mu = \frac{e.\tau}{m^* m_e} = 684\frac{cm^2}{V.s}$$

and a scattering length of

$$l_F = \tau \times h.\frac{k_F}{m} = 15.6\,nm$$

In comparison, room temperature Hall measurements on 100 nm thick InGaAs films grown on semi-insulating InP yielded mobilities of 3900 cm^2 /V s corresponding to a doping density of 3.0 × 10^{18} cm^{-3} . Similar films grown by molecular beam epitaxy yielded similar Hall mobilities at room temperature[78]. Since mobility generally increases with lower

temperature due to reduction in phononic scattering source, we can see that the mobility in the CELO nanostructures is considerably lower compared to planar InGaAs films. InGaAs nanowires with low defect densities have also been reported to show higher mobility values of 7500 cm^2 /Vs at low temperatures[65]. The low scattering length and low mobility in CELO InGaAs suggests the presence of a large number of defects in this particular sample. This observation correlates well with transmission electron microscopy studies of these nanostructures exhibiting significantly high density of stacking faults at a growth temperature higher than 600 °C [27]. Low-field ΔR_{xx} data show signatures of weak localization (WL) in both samples (Figure 4.31), which also indicate the presence of disorder in these nanostructures. In addition, mobility in the CELO nanostructures can be degraded due to increased surface scattering from sidewall roughness[65] and enhanced charged impurity scattering at lower temperatures. Thus, the magneto-transport measurements serve as comprehensive feedback for understanding and improving the material quality in CELO nanostructures.

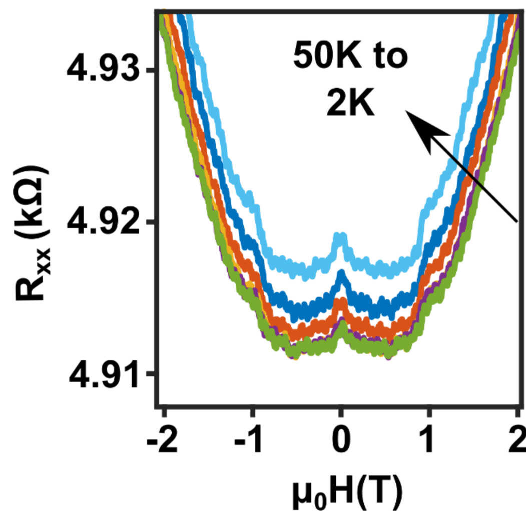


Figure 4.31 : Longitudinal magnetoresistance of sample 2, measured in 2-probe configuration showing peaks at low field (<1T) pointing to signatures of weak localization in the sample. The peak amplitude decreases with increasing temperatures.

IV E.(iii). Conclusion and future directions

In summary, we extracted important material parameters in CELO by fabricating two-terminal devices to perform electrical measurements in magnetic fields up to 14 T. The low-temperature magneto-transport measurements showed Shubnikov–de Haas oscillations in the longitudinal resistance of these nanostructures from which doping concentrations were extracted. The dopant incorporations were found to be comparable to the values measured from planar InGaAs growths. We demonstrated how growth variabilities from different growth runs with similar parameters can be revealed using these measurements. We also extracted effective mass, carrier scattering lifetimes, and quantum mobilities from the temperature dependence of SdH oscillations revealing the presence of a high density of defects in the grown nanostructures. This was made possible by the gentle wet etch process that removes micrometers of parasitic growth in InGaAs CELO, without affecting the nanostructures of interest. Even for samples that had alignment marks completely covered by parasitic growth, the parasitic growth removal procedure allowed us to achieve perfect alignment of vias and fabricate contacts on these nanostructures.

The mechanism outlined here can be extended to lateral growth of other materials including semiconductors such as GaAs[55] or GaSb[79] that exhibits a large number of parasitic growths. It not only helps in achieving perfect alignment during electron beam lithography, but also removes the constraint on the choice of dielectrics that can be used as a masking material even if they result in the formation of parasitic growths [80]. The crucial mechanism of this technique relies on conformal coating of the CELO nanostructures using an ALD dielectric. If the top of the nanostructure (active region) is protected by an oxide template, a subsequent directional dry etch of the ALD dielectric will always preferentially expose the

parasitic growth and keep the nanostructures completely encased and protected. It is critical that the outer edge of the grown nanostructure is protected by the top dielectric in the CELO cavity and is not exposed to seed holes. This helps in selective wet etching the parasitic growth without affecting the CELO nanostructures irrespective of the material used in the active region. Extending the concept of this selective wet etching, future studies can explore growing an etch stop material that completely covers the overgrowth but only partially covers the parasitic growth, such that the wet etchant can selectively etch the parasitic growth. The two-terminal magneto-transport measurement provides a simple yet comprehensive material characterization technique that avoids the unreliability of fabricating multiple contacts on a small nanostructure. In addition, it circumvents common issues in field effect measurements of nanostructures such as gate dielectric leakage, knowledge of the gate dielectric, and thickness that complicates mobility estimates.

IV F. Future directions for CELO

CELO or TASE is a versatile epitaxial growth technique that offers several flexibilities to engineer nanoscale structures which is not typically provided in conventional planar epitaxial growth. The biggest advantage of CELO is that it allows lateral growth in arbitrary orientations in geometries defined purely by lithography. Facets can be controlled using growth conditions and proper choice of substrate orientations and low defect nanostructures can be successfully achieved. In addition, the post-growth removal of parasitic growths opens up the ability to grow a wide variety of materials as well as use growth conditions that are optimized for best quality of growth and not solely the best selectivity. The demonstration of lateral

heterojunctions and quantum wells in this work can pave the way for several interesting applications of this technique.

The potential applications of this technique are several. CELO can eb used for fabricating arbitrary in-plane III-V heterostructures for high-speed low-power electronic devices, nanowires for exploration of one-dimensional transport physics, in-plane quantum dots for light emission and integrated lasers. The ability to perform CELO on Si substrates offers attractive avenues for heterogenous integration for both electronic and photonic applications. In general, this can eb extended to integration of lattice mismatched materials with efficient defect trapping in the initial layers. CELO can also be used to fabricate networks of nanostructures for interconnects and three-dimensional integration of devices.

Despite the huge number of potential applications, several problems with regards to material quality, reliability and yield of growths need to be still solved in CELO. These are not only attractive by themselves as a materials science and process development challenge but also will directly translate to rapid adoption of this technique in industrial applications.

References:

[1] L. Czornomaz *et al.*, "Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates," in *Digest of Technical Papers - Symposium on VLSI Technology*, Aug. 2015, vol. 2015-August, pp. T172–T173. doi: 10.1109/VLSIT.2015.7223666.

[2] H. Schmid *et al.*, "Template-assisted selective epitaxy of III-V nanoscale devices for co-planar heterogeneous integration with Si," *Applied Physics Letters*, vol. 106, no. 23, Jun. 2015, doi: 10.1063/1.4921962.

[3] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, and H. Riel, "Complementary III-V heterojunction lateral NW Tunnel FET technology on Si," *Digest of Technical Papers - Symposium on VLSI Technology*, vol. 2016-Septe, no. 619509, pp. 1–2, 2016, doi: 10.1109/VLSIT.2016.7573444.

[4] J. Z. Huang, P. Long, M. Povolotskyi, G. Klimeck, and M. J. W. Rodwell, "P-Type Tunnel FETs with Triple Heterojunctions," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 6, pp. 410–415, Nov. 2016, doi: 10.1109/JEDS.2016.2614915.

[5] J. Z. Huang *et al.*, "A Multiscale Modeling of Triple-Heterojunction Tunneling FETs," *IEEE Transactions on Electron Devices*, vol. 64, no. 6, pp. 2728–2735, Jun. 2017, doi: 10.1109/TED.2017.2690669.

[6] P. Long *et al.*, "A tunnel FET design for high-current, 120 mV operation," in *Technical Digest - International Electron Devices Meeting, IEDM*, Jan. 2017, pp. 30.2.1-30.2.4. doi: 10.1109/IEDM.2016.7838511.

[7] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 4, pp. 44–49, 2014, doi: 10.1109/JEDS.2014.2326622.

[8] J. Z. Huang, P. Long, M. Povolotskyi, G. Klimeck, and M. J. W. Rodwell, "Sb-And Al-free ultra-high-current tunnel FET designs," *2017 5th Berkeley Symposium on Energy Efficient Electronic Systems, E3S 2017 - Proceedings*, vol. 2018-January, pp. 1–3, Jun. 2017, doi: 10.1109/E3S.2017.8246174.

[9] E. Lind, E. Memiševi, A. W. Dey, and L. Wernersson, "III-V Heterostructure Nanowire Tunnel FETs", doi: 10.1109/JEDS.2015.2388811.

[10] T. Vasen *et al.*, "Vertical Gate-All-Around Nanowire GaSb-InAs Core-Shell n-Type Tunnel FETs OPEN", doi: 10.1038/s41598-018-36549-z.

[11] G. Dewey *et al.*, *Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing*. 2011. doi: 10.1109/IEDM.2011.6131666.

[12] K.-H. Kao *et al.*, "Optimization of Gate-on-Source-Only Tunnel FETs With Counter-Doped Pockets," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, 2012, doi: 10.1109/TED.2012.2200489.

[13] S. T. Šuran Brunelli *et al.*, "Selective and confined epitaxial growth development for novel nano-scale electronic and photonic device structures," *Journal of Applied Physics*, vol. 126, no. 1, 2019, doi: 10.1063/1.5097174.

[14] S. T. Šuran Brunelli *et al.*, "Horizontal heterojunction integration via template-Assisted selective epitaxy," *Crystal Growth and Design*, vol. 19, no. 12, pp. 7030–7035, 2019, doi: 10.1021/acs.cgd.9b00843.

[15] B. Markman, “III-V InxGa1-xAs / InP MOS-HEMTs for 100-340GHz Communications Systems,” 2020. Accessed: Mar. 16, 2022. [Online]. Available: https://escholarship.org/uc/item/6st812pb

[16] H. C. Liou and J. Pretzer, “Effect of curing temperature on the mechanical properties of hydrogen silsesquioxane thin films,” *Thin Solid Films*, vol. 335, no. 1–2, pp. 186–191, Nov. 1998, doi: 10.1016/S0040-6090(98)00881-5.

[17] S. Choi, M. J. Word, and V. Kumar, “Comparative study of thermally cured and electron-beam-exposed hydrogen silsesquioxane resists Optimization of hydrogen silsesquioxane for photonic,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing*, vol. 26, p. 2045, 2008, doi: 10.1116/1.2960565.

[18] A. Ishitani, H. Tsuya, and N. Endo, “Local Loading Effect in Selective Silicon Epitaxy,” *Japanese Journal of Applied Physics*, vol. 23, no. 6, pp. L391–L393, Jun. 1984, doi: 10.1143/JJAP.23.L391/XML.

[19] M. Borg, H. Schmid, K. E. Moselund, D. Cutaia, and H. Riel, “Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si,” *Journal of Applied Physics*, vol. 117, no. 14, Apr. 2015, doi: 10.1063/1.4916984.

[20] A. Nainani, B. R. Bennett, J. Brad Boos, M. G. Ancona, and K. C. Saraswat, “Enhancing hole mobility in III-V semiconductors,” *Journal of Applied Physics*, vol. 111, no. 10, p. 103706, May 2012, doi: 10.1063/1.4718381.

[21] S. Lö, S. Mendach, T. Vonau, C. Heyn, and W. Hansen, “Highly anisotropic electron transport in shallow InGaAs heterostructures”, doi: 10.1103/PhysRevB.67.045309.

[22] P. Long, J. Z. Huang, M. Povolotskyi, G. Klimeck, and M. J. W. Rodwell, “High-current tunneling FETs with (1-10) orientation and a channel heterojunction,” *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 345–348, Mar. 2016, doi: 10.1109/LED.2016.2523269.

[23] G. Wulff, “XXV. Zur Frage der Geschwindigkeit des Wachsthums und der Auflösung der Krystallflächen,” *Zeitschrift für Kristallographie - Crystalline Materials*, vol. 34, no. 1–6, pp. 449–530, Dec. 1901, doi: 10.1524/ZKRI.1901.34.1.449.

[24] D. W. Hoffman and J. W. Cahn, “A VECTOR THERMODYNAMICS FOR ANISOTROPIC SURFACES 1. FUNDAMENTALS AND APPLICATION TO PLANE SURFACE JUNCTIONS.”

[25] J. l. Cahn and D. l. Hoffman, “A vector thermodlnamics for anisotropic surfaces—II. Curved and faceted surfaces,” *Acta Metallurgica*, vol. 22, no. 10, pp. 1205–1214, Oct. 1974, doi: 10.1016/0001-6160(74)90134-5.

[26] V. Jindal and F. Shahedipour-Sandvik, “Theoretical prediction of GaN nanostructure equilibrium and nonequilibrium shapes,” *J. Appl. Phys*, vol. 106, p. 83115, 2009, doi: 10.1063/1.3253575.

[27] A. Goswami *et al.*, “Controlling facets and defects of InP nanostructures in confined epitaxial lateral overgrowth,” *Physical Review Materials*, vol. 4, no. 12, pp. 1–12, 2020, doi: 10.1103/PhysRevMaterials.4.123403.

[28] L. A. Giannuzzi and F. A. Stevie, “A review of focused ion beam milling techniques for TEM specimen preparation.” Accessed: Sep. 04, 2019. [Online]. Available: www.elsevier.com/locate/micron

[29] C. Li, G. Habler, L. C. Baldwin, and R. Abart, “An improved FIB sample preparation technique for site-specific plan-view specimens: A new cutting geometry,” *Ultramicroscopy*, vol. 184, pp. 310–317, Jan. 2018, doi: 10.1016/j.ultramic.2017.09.011.

[30] C. J. Humphreys, “Fundamental concepts of stem imaging,” *Ultramicroscopy*, vol. 7, no. 1, pp. 7–12, 1981, doi: 10.1016/0304-3991(81)90017-6.

[31] P. J. Phillips, M. J. Mills, and M. de Graef, “Systematic row and zone axis STEM defect image simulations,” *Philosophical Magazine*, vol. 91, no. 16, pp. 2081–2101, Jun. 2011, doi: 10.1080/14786435.2010.547526.

[32] H. Shu, X. Chen, X. Zhou, Z. Ding, and W. Lu, “First-principles study of initial growth of InP nanowires: Self-catalytic effect and nucleation mechanism of in adatoms,” *Journal of Physical Chemistry C*, vol. 114, no. 22, pp. 10195–10201, Jun. 2010, doi: 10.1021/jp100256y.

[33] H. Shu, X. Chen, R. Dong, X. Wang, and W. Lu, “Thermodynamic phase diagram for hydrogen on polar InP(111)B surfaces,” in *Journal of Applied Physics*, 2010, vol. 107, no. 6. doi: 10.1063/1.3331767.

[34] E. Pehlke and M. Scheffler, “Equilibrium shapes and energies of coherent strained inp islands,” *Physical Review B - Condensed Matter and Materials Physics*, vol. 60, no. 24, pp. 17008–17015, 1999, doi: 10.1103/PhysRevB.60.17008.

[35] and L. E. S. D.K. Biegelsen, R.D. Bringans, J.E. Northrup, “Reconstructions of GaAs (111) Surfaces Observed by STM,” vol. 65, no. 4, p. 452, 1990.

[36] H. Paetzelt, V. Gottschalch, J. Bauer, G. Benndorf, and G. Wagner, “Selective-area growth of GaAs and InAs nanowires-homo- and heteroepitaxy using SiNx templates,”

Journal of Crystal Growth, vol. 310, no. 23, pp. 5093–5097, 2008, doi: 10.1016/j.jcrysgro.2008.06.065.

[37] K. Nakamura, T. Mano, M. Oshima, H. W. Yeom, and K. Ono, "High-resolution core-level photoemission study on GaAs (111) B surfaces," *Journal of Applied Physics*, vol. 101, no. 4, 2007, doi: 10.1063/1.2434001.

[38] H. J. Chu, T. W. Yeh, L. Stewart, and P. D. Dapkus, "Wurtzite InP nanowire arrays grown by selective area MOCVD," *Physica Status Solidi (C) Current Topics in Solid State Physics*, vol. 7, no. 10, pp. 2494–2497, 2010, doi: 10.1002/pssc.200983910.

[39] N. Julian *et al.*, "Coalescence of InP epitaxial lateral overgrowth by MOVPE with V/III ratio variation," *Journal of Electronic Materials*, vol. 41, no. 5, pp. 845–852, May 2012, doi: 10.1007/s11664-012-2020-y.

[40] D. Hull and D. J. Bacon, *Introduction to Dislocations*. Elsevier Ltd, 2011. doi: 10.1016/C2009-0-64358-0.

[41] C. Frigeri, R. Gleichmann, C. Pelosi, and G. Attolini, "Relationship between dislocation generation, vapour phase supersaturation and growth rate in InP layers obtained by vapour phase epitaxy," 1991.

[42] G. Salviati *et al.*, "Structural characterization of InGaAs/InP heterostructures grown under compressive and tensile stress," *Applied Surface Science*, vol. 188, no. 1–2, pp. 36–48, Mar. 2002, doi: 10.1016/S0169-4332(01)00726-7.

[43] P. Staudinger, S. Mauthe, K. E. Moselund, and H. Schmid, "Concurrent Zinc-Blende and Wurtzite Film Formation by Selection of Confined Growth Planes," *Nano Letters*, vol. 18, no. 12, pp. 7856–7862, Dec. 2018, doi: 10.1021/acs.nanolett.8b03632.

[44] H. A. Fonseka, P. Caroff, J. Wong-Leung, A. S. Ameruddin, H. H. Tan, and C. Jagadish, “Nanowires grown on InP (100): Growth directions, facets, crystal structures, and relative yield control,” *ACS Nano*, vol. 8, no. 7, pp. 6945–6954, Jul. 2014, doi: 10.1021/nn5017428.

[45] C. Renard *et al.*, “Dislocation and antiphase domain free microscale GaAs crystals grown on SiO 2 from (001) Si nano-areas,” *Applied Physics Letters*, vol. 102, no. 19, May 2013, doi: 10.1063/1.4807386.

[46] M. E. Groenet, “Monolithic Heteroepitaxial Integration of III-V Semiconductor Lasers on Si Substrates,” *Phd. Thesis*, 2002.

[47] S. Ghosh, D. Leonhardt, and S. M. Han, “Experimental and theoretical investigation of thermal stress relief during epitaxial growth of Ge on Si using air-gapped SiO2 nanotemplates,” *Applied Physics Letters*, vol. 99, no. 18, pp. 2–5, 2011, doi: 10.1063/1.3659320.

[48] T. Fujii, T. Sato, K. Takeda, K. Hasebe, T. Kakitsuka, and S. Matsuo, “Epitaxial growth of InP to bury directly bonded thin active layer on SiO2/Si substrate for fabricating distributed feedback lasers on silicon,” *IET Optoelectronics*, vol. 9, no. 4, pp. 151–157, 2015, doi: 10.1049/iet-opt.2014.0138.

[49] W. Ju, D. A. Gulino, and R. Higgins, “Epitaxial lateral overgrowth of gallium nitride on silicon substrate,” *Journal of Crystal Growth*, vol. 263, no. 1–4, pp. 30–34, 2004, doi: 10.1016/j.jcrysgro.2003.11.107.

[50] P. M. J. Marée, J. C. Barbour, J. F. van der Veen, K. L. Kavanagh, C. W. T. Bulle-Lieuwma, and M. P. A. Viegers, “Generation of misfit dislocations in semiconductors,” *Journal of Applied Physics*, vol. 62, no. 11, pp. 4413–4420, 1987, doi: 10.1063/1.339078.

[51] J. Selvidge *et al.*, “Defect filtering for thermal expansion induced dislocations in III-V lasers on silicon,” *Applied Physics Letters*, vol. 117, no. 12, 2020, doi: 10.1063/5.0023378.

[52] P. Long, M. Povolotskyi, B. Novakovic, T. Kubis, G. Klimeck, and M. J. W. Rodwell, “Design and simulation of two-dimensional superlattice steep transistors,” *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1212–1214, Dec. 2014, doi: 10.1109/LED.2014.2364593.

[53] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi, and G. Baccarani, *Performance Limits of Superlattice-Based Steep-Slope Nanowire FETs*. 2011. doi: 10.1109/IEDM.2011.6131491.

[54] M. Fahed, L. Desplanque, C. Coinon, D. Troadec, and X. Wallart, “Impact of P/In flux ratio and epilayer thickness on faceting for nanoscale selective area growth of InP by molecular beam epitaxy.,” *Nanotechnology*, vol. 26, no. 29, p. 295301, Jul. 2015, doi: 10.1088/0957-4484/26/29/295301.

[55] J. Wallentin and M. T. Borgström, “Doping of semiconductor nanowires,” *Journal of Materials Research*, vol. 26, no. 17, pp. 2142–2156, 2011, doi: 10.1557/jmr.2011.214.

[56] S. A. Dayeh, R. Chen, Y. G. Ro, and J. Sim, “Progress in doping semiconductor nanowires during growth,” *Materials Science in Semiconductor Processing*, vol. 62, no. October, pp. 135–155, 2017, doi: 10.1016/j.mssp.2016.10.016.

[57] N. Bologna *et al.*, “Dopant-Induced Modifications of Ga xIn(1- x)P Nanowire-Based p-n Junctions Monolithically Integrated on Si(111),” *ACS Applied Materials and Interfaces*, vol. 10, no. 38, pp. 32588–32596, 2018, doi: 10.1021/acsami.8b10770.

[58] M. Borg *et al.*, “Facet-selective group-III incorporation in InGaAs template assisted selective epitaxy,” *Nanotechnology*, vol. 30, no. 8, Feb. 2019, doi: 10.1088/1361-6528/aaf547.

[59] P. Aseev *et al.*, “Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks,” *Nano Letters*, p. acs.nanolett.8b03733, 2018, doi: 10.1021/acs.nanolett.8b03733.

[60] A. Goswami, B. Markman, S. T. Š. Brunelli, S. Chatterjee, M. Rodwell, and C. J. Palmstrøm, “A gentle parasitic growth removal process to enable low temperature magneto-transport characterization in confined epitaxial lateral growth of InGaAs”.

[61] M. Friedl *et al.*, “Template-Assisted Scalable Nanowire Networks,” *Nano Letters*, vol. 18, no. 4, pp. 2666–2671, 2018, doi: 10.1021/acs.nanolett.8b00554.

[62] P. Chuang *et al.*, “All-electric all-semiconductor spin field-effect transistors,” *Nature Nanotechnology*, vol. 10, no. 1, pp. 35–39, 2015, doi: 10.1038/nnano.2014.296.

[63] T. Schäpers, J. Knobbe, and V. A. Guzenko, “Effect of Rashba spin-orbit coupling on magnetotransport in InGaAs/InP quantum wire structures,” *Physical Review B - Condensed Matter and Materials Physics*, vol. 69, no. 23, pp. 1–5, 2004, doi: 10.1103/PhysRevB.69.235323.

[64] K. Takase, Y. Ashikawa, G. Zhang, K. Tateno, and S. Sasaki, “Highly gate-tuneable Rashba spin-orbit interaction in a gate-all-around InAs nanowire metal-oxide-semiconductor field-effect transistor,” *Scientific Reports*, vol. 7, no. 1, pp. 1–9, 2017, doi: 10.1038/s41598-017-01080-0.

[65] J. J. Hou *et al.*, “Diameter dependence of electron mobility in InGaAs nanowires,” *Applied Physics Letters*, vol. 102, no. 9, 2013, doi: 10.1063/1.4794414.

[66] R. Rana *et al.*, “Nonlinear Charge Transport in InGaAs Nanowires at Terahertz Frequencies,” *Nano Letters*, vol. 20, no. 5, pp. 3225–3231, 2020, doi: 10.1021/acs.nanolett.9b05328.

[67] I. Yang *et al.*, “Radial Growth Evolution of InGaAs/InP Multi-Quantum-Well Nanowires Grown by Selective-Area Metal Organic Vapor-Phase Epitaxy,” *ACS Nano*, American Chemical Society, 2018. doi: 10.1021/acsnano.8b05771.

[68] M. Avram, A. Avram, M. Purica, A. M. Popescu, and C. Voitincu, “Characterization of defects generated during reactive ion etching,” *Proceedings of the International Semiconductor Conference, CAS*, vol. 1, pp. 249–252, 2009, doi: 10.1109/SMICND.2009.5336557.

[69] F. Léonard and A. A. Talin, “Electrical contacts to one- and two-dimensional nanomaterials,” *Nature Nanotechnology*, vol. 6, no. 12, pp. 773–783, 2011, doi: 10.1038/nnano.2011.196.

[70] A. Guo, “Nano-scale metal contacts for future III-V CMOS,” *Phd. Thesis*, pp. 1–66, 2012, [Online]. Available: http://dspace.mit.edu/handle/1721.1/78460%5Cnfiles/202/2012 - Guo - Nano-scale metal contacts for future III-V CMOS.pdf

[71] J. B. Yoo *et al.*, “Effects of V/III ratio on Si-doping in InGaAs lattice-matched to InP grown by organometallic vapor phase epitaxy,” *Journal of Crystal Growth*, vol. 132, no. 1–2, pp. 43–47, 1993, doi: 10.1016/0022-0248(93)90245-R.

[72] E. M. Lifshits and A. M. Kosevich, “Theory of the Shubnikov-de Haas effect,” *Journal of Physics and Chemistry of Solids*, vol. 4, no. 1–2, pp. 1–10, 1958, doi: 10.1016/0022-3697(58)90189-6.

[73] R. J. Nicholas, J. C. Portal, C. Houlbert, P. Perrier, and T. P. Pearsall, “An experimental determination of the effective masses for Ga xIn1-xAsyP1-y alloys grown on InP,” *Applied Physics Letters*, vol. 34, no. 8, pp. 492–494, 1979, doi: 10.1063/1.90860.

[74] D. Schneider, L. Elbrecht, J. Creutzburg, A. Schlachetzki, and G. Zwinge, “In-plane effective mass of electrons in InGaAs/InP quantum wells,” *Journal of Applied Physics*, vol. 77, no. 6, pp. 2828–2830, 1995, doi: 10.1063/1.358694.

[75] R. W. Martin *et al.*, “Selective area epitaxy of InGaAs/InGaAsP quantum wells studied by magnetotransport,” *Semiconductor Science and Technology*, vol. 11, no. 5, pp. 735–740, 1996, doi: 10.1088/0268-1242/11/5/014.

[76] A. M. Kurakin *et al.*, “Quantum confinement effect on the effective mass in two-dimensional electron gas of AlGaN/GaN heterostructures,” *Journal of Applied Physics*, vol. 105, no. 7, 2009, doi: 10.1063/1.3100206.

[77] D. Schneider, F. Hitzel, A. Schlachetzki, and P. Boensch, “Dependence of electron effective mass on the subband occupation in In0.53Ga0.47As/InP quantum wells,” *Physica E: Low-Dimensional Systems and Nanostructures*, vol. 12, no. 1–4, pp. 562–565, 2002, doi: 10.1016/S1386-9477(01)00472-6.

[78] A. Baraskar, “Development of Ultra-Low Resistance Ohmic Contacts for InGaAs / InP HBTs,” *Phd. Thesis*, no. September, p. 165, 2011.

[79] M. Fahed, L. Desplanque, D. Troadec, G. Patriarche, and X. Wallart, “Selective area heteroepitaxy of GaSb on GaAs (001) for in-plane InAs nanowire achievement,” *Nanotechnology*, vol. 27, no. 50, 2016, doi: 10.1088/0957-4484/27/50/505301.

[80] F. Krizek, “Semiconductor Nanowire Networks Grown By Molecular Beam Epitaxy Vapor-Liquid-Solid,” *Phd. Thesis*, 2018.

V. Semiconductor-superconductor hybrid nanostructures for topological quantum computing

V.A. Introduction

V.B. SAG template fabrication and growth processes

V.C. SAG nanowire growths

V.A. Introduction:

Italian physicist Ettore Majorana proposed in 1937 that certain neutral spin-1/2 fermionic particles can behave as their own antiparticle [1] . The non-Abelian particle exchange statistics of these quasiparticles in condensed matter systems makes them particularly attractive, since information can be stored and manipulated through adiabatic exchange of these particles[2]–[4] . A non-trivial topology results which protects the system from local perturbations. This property makes Majorana fermions an attractive building block for fault-tolerant topological qubit.

In superconducting materials, a Majorana fermion can emerge as a quasiparticle commonly referred to as a Bogoliubov quasiparticle[5] . Kitaev proposed that a 1D chain of electrons with a specific pairing can host Majorana states[6] . Realizing this proposal experimentally, requires a p-wave superconductor. Luchyn et.al. proposed a simple condensed matter system that satisfies all the requirements[7] . This included a 1D system (such as a nanowire) with a strong spin orbit coupling, large Lande g-factor and chemical potential tunability, coupled to a s-wave superconductor. Several experimental works have followed this proposal attempting to realize such topological quantum devices[8]–[10].

Although a large number of experiments were performed since 2012, conclusive robust evidence of Majorana fermions in solid state system and using it to store information are yet

to be experimentally demonstrated. One of the limiting factors in such experiments have been the material quality of the semiconducting nanowire and the interfaced superconductor. A small density of defects in the nanowires and disorder at the semiconductor-superconductor interface can both negatively affect the coherence times of carriers in such wires- resulting in ambiguous signatures in electrical transport and inability to stabilize the Majorana state. The second limiting factor is the fundamental inability to design complex transport experiments (such as braiding) since most of these measurements and device fabrication were done using single VLS grown nanowires, individually transferred to a substrate using micro-manipulators. To perform more complicated measurements, one requires a complex network of nanowires connected to superconductors, which is impossible to grow using the VLS technique.

Selective area grown in-plane nanowires have found particular attention for their potential to solve these challenges by (1) growing an arbitrarily complicated network of in-plane nanowires, defined by lithography and (2) improving the material quality of these nanowires by incorporating buffer materials and quantum wells drawing from the well-established knowledge of planar epitaxial growth of high mobility quantum wells. As a result, SAG nanowires grown using MBE, CBE or MOCVD are the subject of intense exploration [11]–[14] .

However, SAG differs significantly from planar epitaxial growth and new factors such as dielectric quality, roughness, pattern dimensions, growth rate enhancement in trenches, differences in mass transport come into play. The requirement of a high g-factor material limits the choice of III-V semiconductors to a few, namely InAs, InSb, InGaAs or alloys of these materials. The necessity of performing transport experiments on these nanowires requires the substrate to be non-conducting at the temperature of measurements. As a result, large-bandgap

semi-insulating InP and GaAs wafers are most commonly used. Therefore, the large lattice mismatch between the grown nanowires and the substrate gives rise to a high density of misfit and threading dislocations that degrade the electronic quality of the nanowires. As a result, despite the initial promises, it was quickly observed that the material qualities (in particular, mobilities) of such SAG nanowires are significantly lower than the VLS grown nanowires or epitaxial planar growths. The work in this chapter addresses these problems by combining template design, growth of buffered and heterojunction quantum well nanowires and in-situ superconductor patterning techniques to improve material quality of the nanowires as well as fabricate a disorder free semiconductor-superconductor interface. The following sections first discuss InAs SAG nanowires with buffer growth and InGaAs quantum well nanowires. This is followed by the section describing the design of in-situ shadow wall structures.

V.A. (ii). Other applications of in-plane selective area grown nanowires:

Before describing the growth of SAG nanowires, it must be mentioned that such in-plane grown nanowires also have extensive applications outside topological quantum computing. In-plane multi quantum well InP/InGaAs nanowires can be used as both lasers and photodetectors in the telecommunication range, making them very important for building integrated photonic components [15]–[17]. High mobility SAG nanowires can be used for high-speed III-V transistors integrated on silicon [18]. Selective area grown quantum dots can also be used as single photon sources for on-chip quantum photonics circuits [19].

V.B. SAG template fabrication and growth

The fabrication of the selective area growth templates starts with atomic layer deposition of 6-7nm of aluminum oxide using a TMA+H_20 recipe at 300°C on a 2” semi-

insulating Fe doped InP (001) wafer. This is followed by a PECVD deposition of 30nm silicon oxide. Using the electron beam resist CSAR, alignment marks are first defined in a JEOL electron beam writer. A $CHF_3/CF_4/O_2$ recipe is used to etch into the SiO_2 at an etch rate of 70nm/min using an inductively coupled plasma etcher. The resist is removed first by an Acetone rinse and then ashing the sample in a Gasonics plasma asher at 350 C. After cleaning the sample, in solvents, the aluminum oxide is etched using a wet etch with AZ300MIF developer. The sample is then etched in a RIE plasma etcher in a Methane/Hydrogen/Argon chemistry for 20 minutes (roughly corresponds to about 500nm-1um of InP etched). After this all the oxides are removed from the sample surface using a buffered HF dip for 5 minutes. The ALD AlOx and PECVD SiO_2 is redeposited, and the selective area growth patterns are defined in the EBL. A similar dry etch, wet etch and resist removal as described before, follows. The sample is then diced into 1cm x 1cm squares and sonicated in acetone and isopropanol. Before loading into the CBE, the samples are oxidized using UV Ozone for 10 minutes and etched in a dilute hydrochloric acid solution (1:10) for 45 seconds (process repeated twice). This etches the first few layers of the InP surface inside the trenches.

The samples are mounted using indium on molybdenum carrier blocks and loaded into the chemical beam epitaxy chamber. In the preparation chamber, they are outgassed at 250°C in a heater stage until the pressure comes down to approximately $2x10^{-9}$ torr. Then, the sample is transferred to the growth chamber. The sample is heated up to 520°C under a PH_3 overpressure to desorb the oxide on the surface. The pyrometer temperature is calibrated by using the (2x1) to (2x4) surface reconstruction transition, visible in the reflection high energy electron diffraction (RHEED). InP is typically grown at 520°C with a TMI line pressure of 0.5 torr and PH_3 line pressure of 18 torr. InAs is grown at 520°C with TMI line pressure of 0.5 torr

and AsH_3 line pressure of 12 torr. InGaAs (lattice matched) is grown at 520°C with TMI line pressure of 0.5 torr, TEG line pressure of 0.66 torr and AsH_3 line pressure of 12 torr. Deviations from these growth conditions for specific experiments will be mentioned in the corresponding sections.

V.C. SAG Nanowire growths

For the nanowire growths we explore a wide range of growths at various growth conditions and perform extensive SEM, AFM and TEM measurements to understand the dependence of facets and defects on template geometry and orientation and improving the yield of well-formed continuous nanowires. The main goal of this work is to improve the electron mobility in these SAG nanowires or in turn reduce sources of electron scattering. If the nanowire structures are examined, such sources of scattering can arise from various interface scattering mechanisms, defects extending through the transport channel, and scattering from the surface of the nanowire. In this work a two-fold approach is adopted. First, we examine how to reduce the defect densities in the channel by buffer engineering and reducing lattice mismatch between the buffer material and the channel. Second, we explore certain capping materials that can effectively passivate the surface of the nanowire and reduce its scattering contribution. However, to grow these complex structures in these selective area geometry each stage of the growth process needs to be optimized. The following sections first examine growth of InP buffer inside the channels, followed by growth of InAs under various conditions of growth initiation and cooldown. Finally buffered nanowires and capping layer growths are investigated. For all these studies wire widths are varied from 1um down to 60nm and orientations on a (100) InP sample are varied between $[0\bar{1}\bar{1}]$, $[00\bar{1}]$ and $[0\bar{1}1]$ directions.

V.C. (i) SAG of InP nanowires on InP (001) substrates

The first step of growing the heterostructure nanowire in SAG templates is growing a buffer layer of InP. This has several purposes. One, the starting InP surface after the processing of the template is likely to contain residues and damages. Enough precautions are taken to protect this surface from plasma and fluorine compounds (which can form nonvolatile InF_x) in the dry etcher by using an alumina etch stop layer and also performing digital etches prior to sample growth. However, ensuring that trenches less than 200-300nm thick are completely clean and pristine is challenging. The extra InP buffer before the start of the channel growth ensures that the actual channel growth initiates on a pristine InP surface. Additionally, it moves the channel away from the substrate interface (see Figure 5.20 in section 5c.VI.) and likely reduces the effects of any disorder at that interface .

InP is typically grown at 520 °C with a TMI line pressure of 0.5 torr and PH_3 line pressure of 18 torr. To understand the nucleation and growth progress in this SAG homoepitaxy, 3 samples are grown with growth times of 2 minutes, 6 minutes and 8 minutes. The top view SEM images of these growths with various growth times and nanowire orientations (along $[0\bar{1}\bar{1}], [00\bar{1}]$ and $[0\bar{1}1]$) on the substrate are demonstrated in Figure 5.1. Nanowires with channel widths from 1um to 80nm are shown.

From the 2-minute growths in all orientations the growth in the wide trenches (1μm to 400nm) appear to be uniform with considerable roughness and discontinuities at the edges. The thinner trenches (≤ 200nm) exhibit highly non-uniform growth with island nucleation and wide discontinuities at the merging points (Figure 5.1 G). The 6-minute and 8-minute growths are smoother and more uniform, even for thinner nanowires. This demonstrates the importance of having a sufficiently thick homoepitaxial InP buffer before starting to grow the channel layer. Additionally, as mentioned in previous works[20], it is observed that for thicker growths, uniformity is dependent on the precise growth time used. Longer growth times can lead to micro-faceting especially in thinner nanowires.

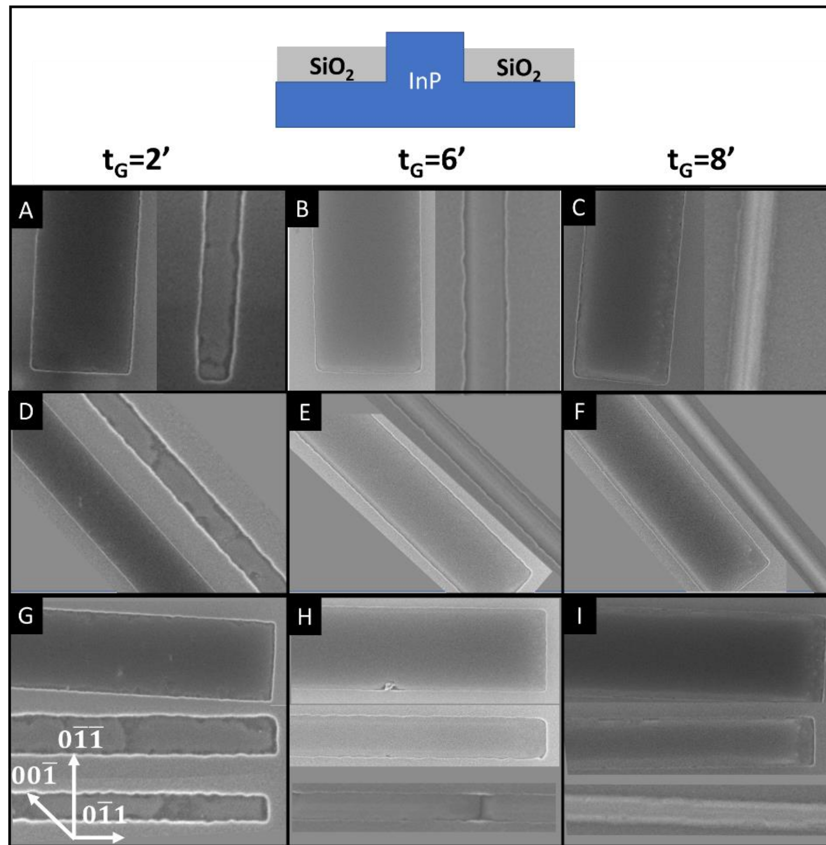


Fig 5.1 : Top-down SEM images of SAG InP grown for 2 minutes (A,D,G), 6 minutes (B,E,H) and 8 minutes (C,F,I) respectively. (A-F) show two wires each with widths 1um

and 100nm. (G-I) shows three wires each with widths 1um, 200nm and 100nm (top to bottom in each image).

The $[0\bar{1}\bar{1}]$ nanowires exhibit a combination of {111}B and {011} side facets. However, for thinner nanowires, the growth appears asymmetric with the possible formation of {211} facets. Both for the 6-minute and 8-minute growths for wider nanowires there is a considerable roughness that is visible only on the right edge of the $[0\bar{1}\bar{1}]$ and $[0\bar{1}1]$ (less clearly) oriented nanowires (Figure 5.1C). The origin of this is not clearly understood but could be due to slight misalignments in the template fabrication.

For the $[00\bar{1}]$ oriented nanowires, the 6-minute and 8-minute growths show a considerably abrupt change in facet shapes around 200nm channel width. Nanowires thicker than 200nm exhibit a combination of primarily vertical {010} and small slanted {110} type facets. Nanowires that are 200nm or thinner only have the 45° slanted {110} type facets. This change in the nature of the facets is evident in both the 6-minute (Figure 5.1 E) and 8-minute growths (Figure 5.1 F).

For the $[0\bar{1}1]$ oriented nanowires the 6-minute growths contain primarily (011) type facets for thicker nanowires and the thinner nanowires (≤ 200nm in thickness) exhibit a combination of {111}A and {011} facets. The 8-minute growths are less uniform and show micro-faceting. Nucleation in $[0\bar{1}1]$ nanowires is significantly more non-uniform than growth in the previous two orientations even for thicker nanowires and could be linked to asymmetric diffusion between the $[0\bar{1}1]$ and [011] orientations.

Summary:

Homoepitaxial growth of InP in selective area growth nanowires exhibit roughness and uneven nucleation for 2-minute growths but appeared smooth and uniform for 6 minute and 8

minute growths. For $[0\bar{1}\bar{1}]$ oriented nanowires the right edge appeared rough and consisting of a $\{211\}$ facet which can be from misalignment of templates to crystal facets during the EBL write. $[00\bar{1}]$ oriented wires below 200nm exhibit primarily $\{011\}$ type facets.

For the results in the following section, the buffer growth time was chosen according to the total thickness of the nanowire and the nanowire width required. Since primarily the 100-200nm nanowires were used for various measurements, the 8-minute InP buffer was selected for InAs channel growths and a 6-minute InP buffer was chosen for the thicker InGaAs quantum well structures.

V.C. (ii). Arsenic flush on SAG InP nanowires on InP(100) substrates

Typically growing an InAs channel on top of a InP buffer (in the SAG geometry) requires switching the group-V precursors from PH_3 to AsH_3. While switching the group-V, a flush under As is performed before turning on the TMI (for InAs). This minimizes intermixing of As and P and subsequently the formation of InAsP at the interface. In this experiment, the effect of annealing a InP nanowire under As is explored to investigate the surface roughening, before the group-III is introduced. A total of 4 separate growths were performed. The growth time for the InP buffer was varied (for reasons explained later) and the temperature of As annealing is also changed from 520°C to 480°C for sample 4. Sample information and SEM images are below. The switch from PH_3 to AsH_3 was done abruptly after the buffer growth. All the samples were cooled down under As.

Sample number	Growth time for InP buffer layer	Temperature at which a 60 second anneal was performed under As before cooldown
1	8’	520°C
2	11’	520°C
3	2’	520°C
4	8’	480°C

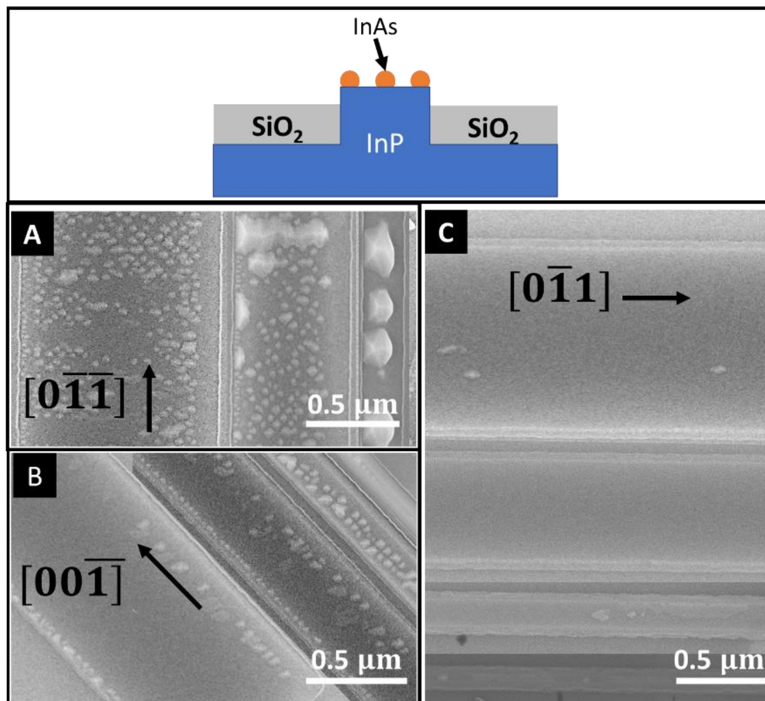


Figure 5.2: Sample 1 – 60s anneal under As at 520°C on 8m InP buffer and cooldown under As

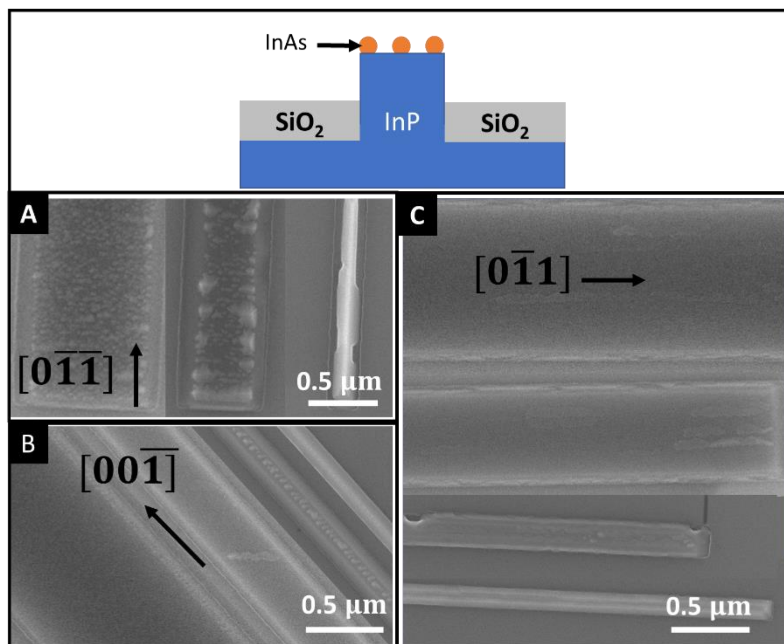


Figure 5.3: Sample 2 – 60s anneal under As at 520°C on 11m InP buffer and cooldown under As

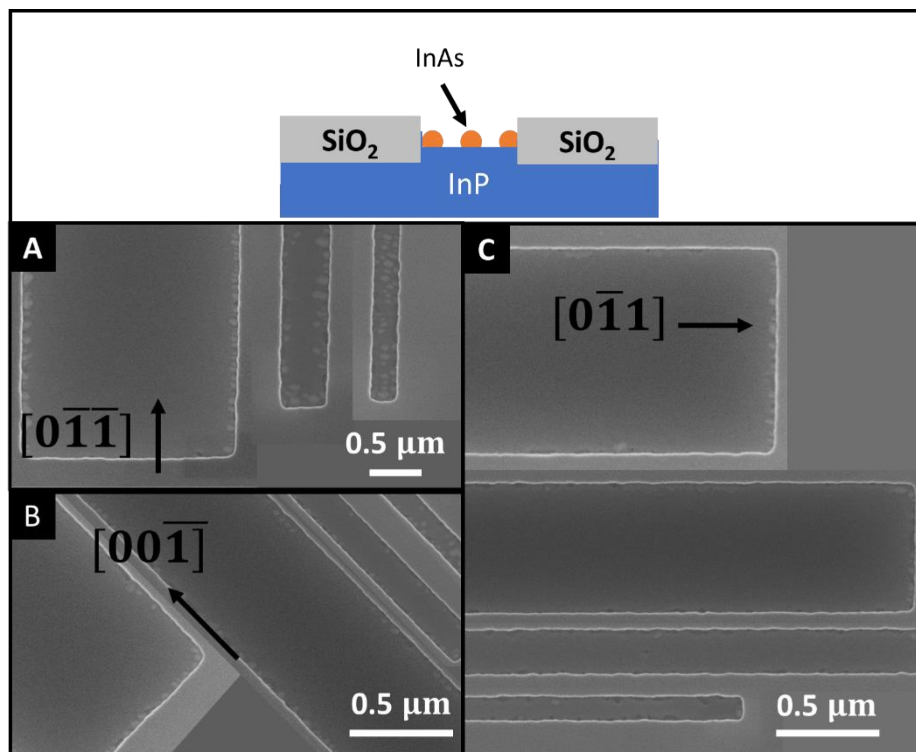


Figure 5.4: Sample 3 – 60s anneal under As at 520°C on 2m InP buffer and cooldown under As

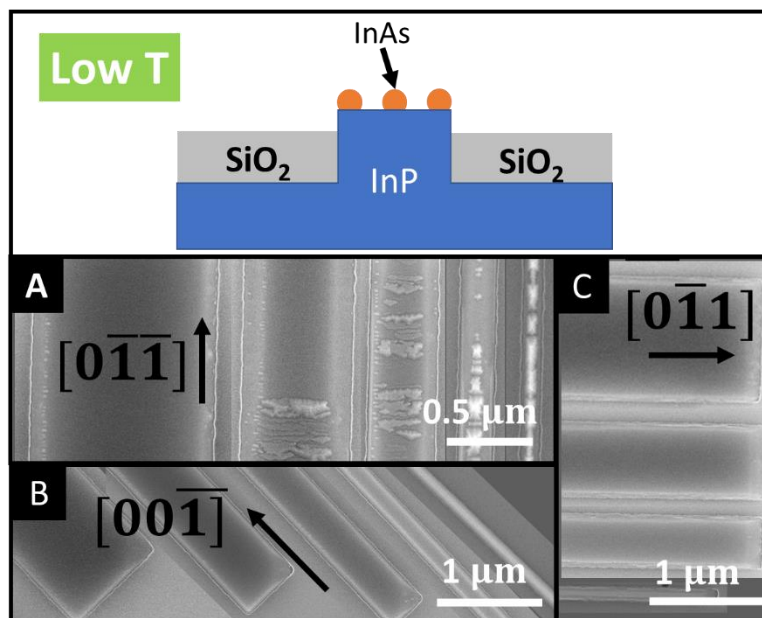


Figure 5.5: Sample 4 – 60s anneal under As at 480°C on 8m InP buffer and cooldown under As

For sample 1, the $[0\bar{1}\bar{1}]$ oriented nanowires exhibit small islands formed mainly on the (100) top surface. As the nanowire widths shrink from 1um to 60nm, the islands first merge into larger islands and then spans the entire width of 200nm wide $[0\bar{1}\bar{1}]$ nanowires. Below 200nm nanowire widths, more uniform sections of nanowires form. For the $[00\bar{1}]$ oriented nanowires, a significant portion of the wider nanowires do not exhibit any island nucleation on the top (100) surface but nucleations exist on the edges and the side {010} surfaces. With shrinking widths the nuclei merge and form larger islands similar to the previous case, and for nanowires thinner than 100nm, nucleation densities of these islands reduce. For $[0\bar{1}1]$ oriented nanowires, these island nucleations are almost nonexistent, except for very narrow wires (<100nm width), where it seems the nucleation is mostly due to the non-uniformity of the InP buffer layer itself.

Note that from sample 1, the nucleations appear to be highly orientation dependent and therefore cannot be solely explained by strain driven nucleation on the (100) InP surface. The fact that the $[00\bar{1}]$ oriented nanowires are smooth and all the other nanowires are full of streaky InAs nucleations, suggests that the {111}B InP surfaces are less stable and are likely decomposing during the As flush stage, forming indium droplets. These possibly then diffuse along $[0\bar{1}1]$ (the fast diffusion direction) to form nucleations on the (100) InP surface either immediately or during the anneal process and cooldown. This phenomenon is also likely driven by As/P exchange at the high temperature thus eroding the side edges ({111}B sides) of the InP nanowire.

To test this hypothesis further, we grow two more samples (#2 and #3) with a 11 minute InP buffer and a 2 minute InP buffer. If the formation of the observed nucleations is indeed

driven by the decomposition of the side facets in sample #2 we should observe a difference in the nucleation densities with changing ratios of side to top facets.

Figures 5.3 and 5.4 show the results from these experiments. Sample #2 (Figure 5.3) appears to show a higher density of island like nucleations in the $[0\bar{1}\bar{1}]$ oriented wires. However sample #3 (Figure 5.4) looks dramatically different from sample #1 and sample #2. There are almost no island nucleations on the top surface of the wide nanowires (>600nm) for any orientation. However, the edges exhibit nucleations which are believed to form from the {111}B facets that form at the edges due to the non-uniformities and roughness of the channel fabrication. As the nanowire widths are reduced the effects of the edge nucleation are likely stronger and result in formation of the island nucleations all across the channels. This also corroborates with the observation that for thinner nanowires (≤ 200nm wide) the 2 minute InP nucleation by itself is very non uniform(Figure 5.1) and probably results in spurious InAs nucleations at the positions where the InP nuclei merge. Therefore , this study suggests that the decomposition of the side {111}B facets are likely one of the contributing factors to the formation of the island nucleations for an anneal of InP nanowires under As at 520°C.

Since this appeared to be a temperature driven effect, a lower temperature (480°C) as anneal was investigated next. Figure 5.5 shows that with reduction in annealing temperature, the surfaces again look extremely smooth without the formation of nucleation on the (100) surface. However, as the $[0\bar{1}\bar{1}]$ oriented nanowire widths are reduced, streaky nucleations are observed. This effect increases for <200nm wide nanowires. Comparison of the 200nm wide nanowires oriented along $[0\bar{1}\bar{1}]$ for sample# 1, sample #2 and sample #4 suggests that the lower temperature likely reduced the decomposition of the {111}B surfaces.

However, it must be noted that this phenomenon is not only driven by temperature of nucleation and InP buffer thickness, but also the cooldown process. This is explained in section **V.C. (iv).** In addition, for all samples with nanowires that look smooth, it is possible that a very thin InAsP layer is formed on the top of the nanowire which is challenging to detect in the SEM (cross-sectional TEMs can further elucidate this).

Summary:

We observed that an arsenic anneal forms dot like island nucleations on top of the InP (100) surfaces only for $[0\bar{1}\bar{1}]$ oriented nanowires. This phenomenon is absent for $[0\bar{1}1]$ and $[00\bar{1}]$ oriented nanowires. A possible mechanism suggested here is the decomposition of the {111}B side facets during the arsenic anneal, leading to increased As/P exchange and diffusion to the top surface to form islands. The effect can be almost completely suppressed for wider nanowires if the InP buffer is thin (2 minutes) leading to the absence (or minimal formation) of {111}B side facets. The effect can be also considerably tuned by anneal temperature, since a 480°C anneal leads to formation of very few nucleations. The material transport during the As/P exchange is also linked to cooldown processes as we will demonstrate in Section **V.C. (iv).**

V.C. (iii). Nucleation of InAs on InP SAG nanowires:

To test the nucleation of InAs on the grown InP SAG buffers, InAs was grown for 15 seconds on top of a 8 minute thick InP buffer. Three different samples were grown at temperatures of 520°C , 500°C and 480°C (Figure 5.6). With increase in InAs growth temperature, the island sizes increase and the densities decrease. The islands are elongated along the $[0\bar{1}1]$ fast diffusion orientation. The decomposition of the {111}B surfaces at a

higher temperature can be clearly observed in the nanowires with widths <200nm (right panels in Figure 5.6) . The 480°C InAs growth shows very uniform nucleation (Figure 5.7).

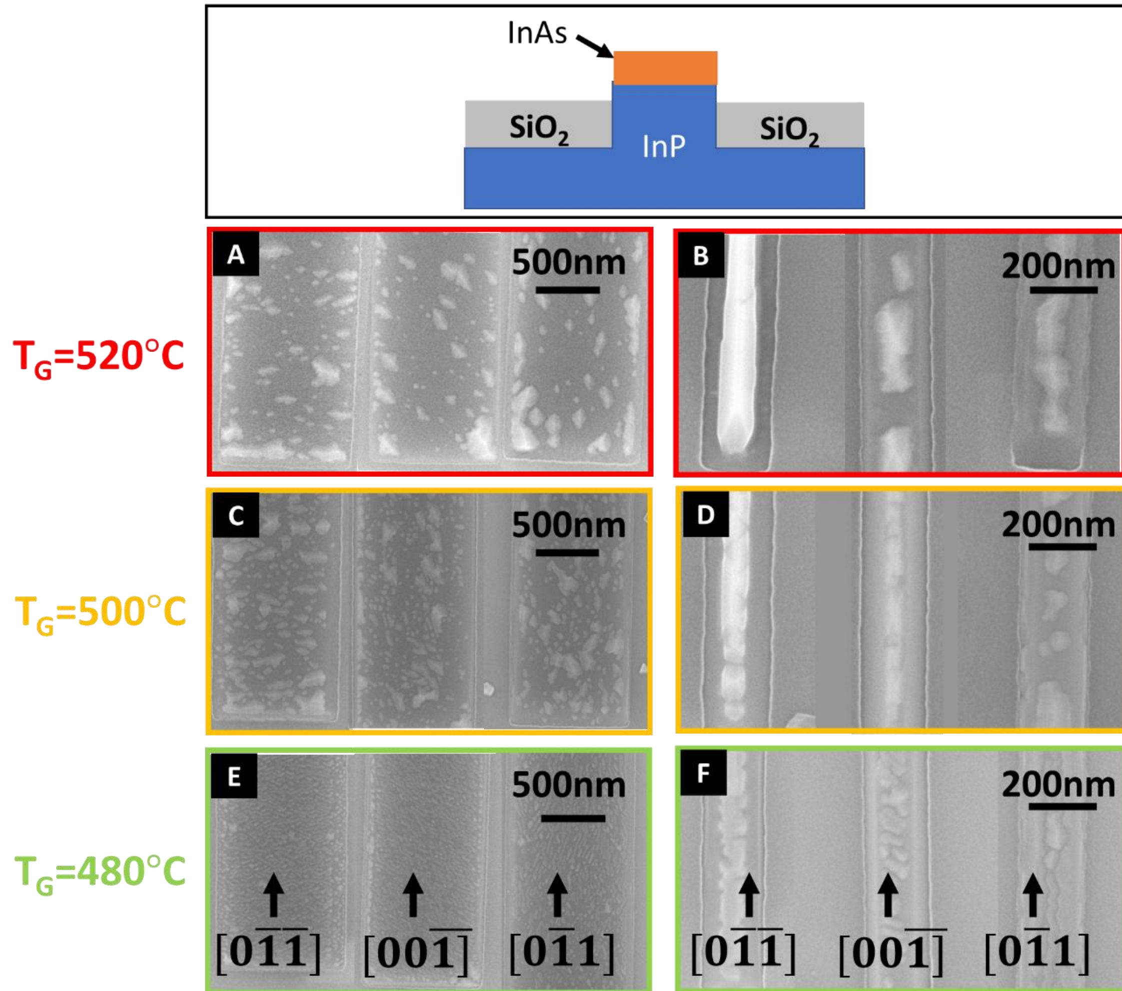


Figure 5.6: 15 seconds of InAs growth on InP 8m buffers at different growth temperatures for the InAs.

To verify if this nucleation is still driven by the edge {111}B facets, a similar 15 seconds of InAs is grown on a 2-minute InP buffer at 520°C and compared (Figure 5.8). No elongated islands are observed, suggesting that it is likely caused by the decomposition of the side facets

at a higher temperature. Of course, the uneven InP buffer growth for the 2-minute buffer contributes to the non-uniformity observed for nanowires that are less than 200nm wide.

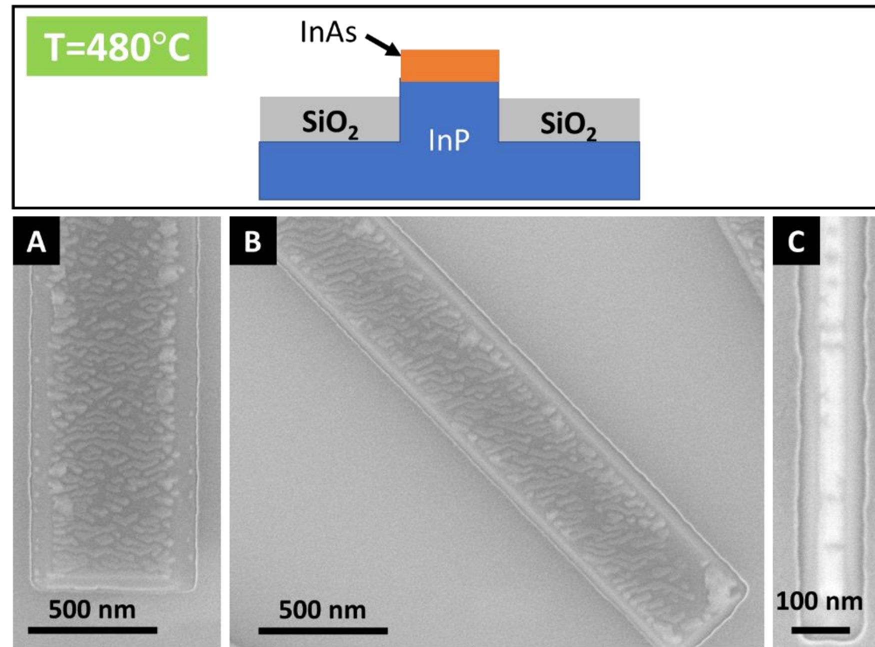


Figure 5.7: 15 seconds of InAs growth on InP 8m buffers at 480°C.

A thicker InAs channel (2-minutes of growth) is grown at two different temperature, 520°C (Figure 5.9 and Figure 5.10 – top panel) and 500°C (Figure 5.10- bottom panel) . The effects match the nucleation study that was described in the previous paragraphs. Nanowires above 200nm have a rough and island like surface in all 3 orientations. The $[0\bar{1}\bar{1}]$ oriented wires show significant absence of material along the edges of the nanowire. This is likely due to a combination of {111}B surface decomposition and arsenic-phosphorus exchange. A similar effect is observed at the right edges of the $[0\bar{1}1]$ oriented wires. $[00\bar{1}]$ oriented nanowires that are 100-200nm in width exhibit smooth surfaces with clearly formed {110}

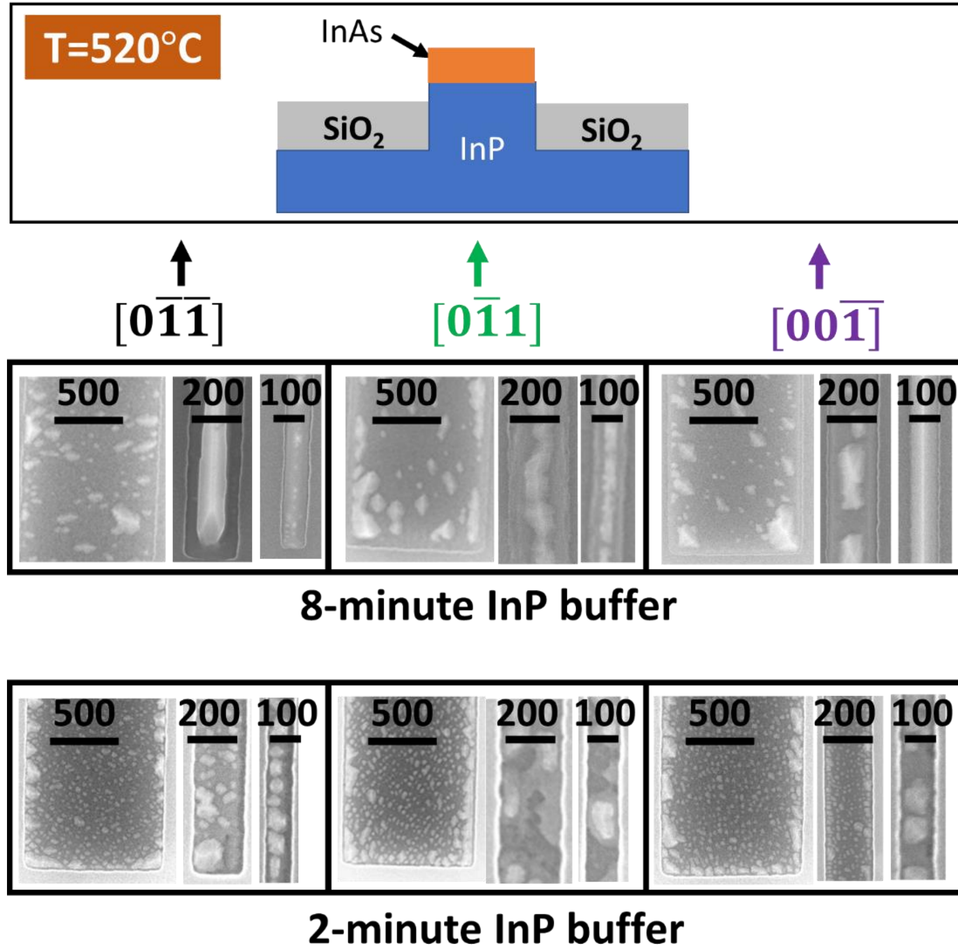


Figure 5.8: Effect of InP buffer thickness on 15 seconds of InAs growth on InP buffers at 520°C.

facets. Along [0$\bar{1}$1] the nanowires below 200nm contain {011} and {111} facets. The 200nm nanowire clearly shows both the InAs channel and the InP buffer layers. For the low temperature growth (500°C), the nanowires were observed to be more conformal and smoother.

Summary:

We observed that the growth temperature plays an important role in the nucleation of InAs on InP nanowires. A lower InAs growth temperature was observed to form more uniform and conformal growth and less decomposition of the {111}B surfaces. A lower growth

temperature also forms smoother nanowires for thicker channels. An approximate schematic of the proposed formation mechanism of these InAs islands is provided in Figure 5.11.

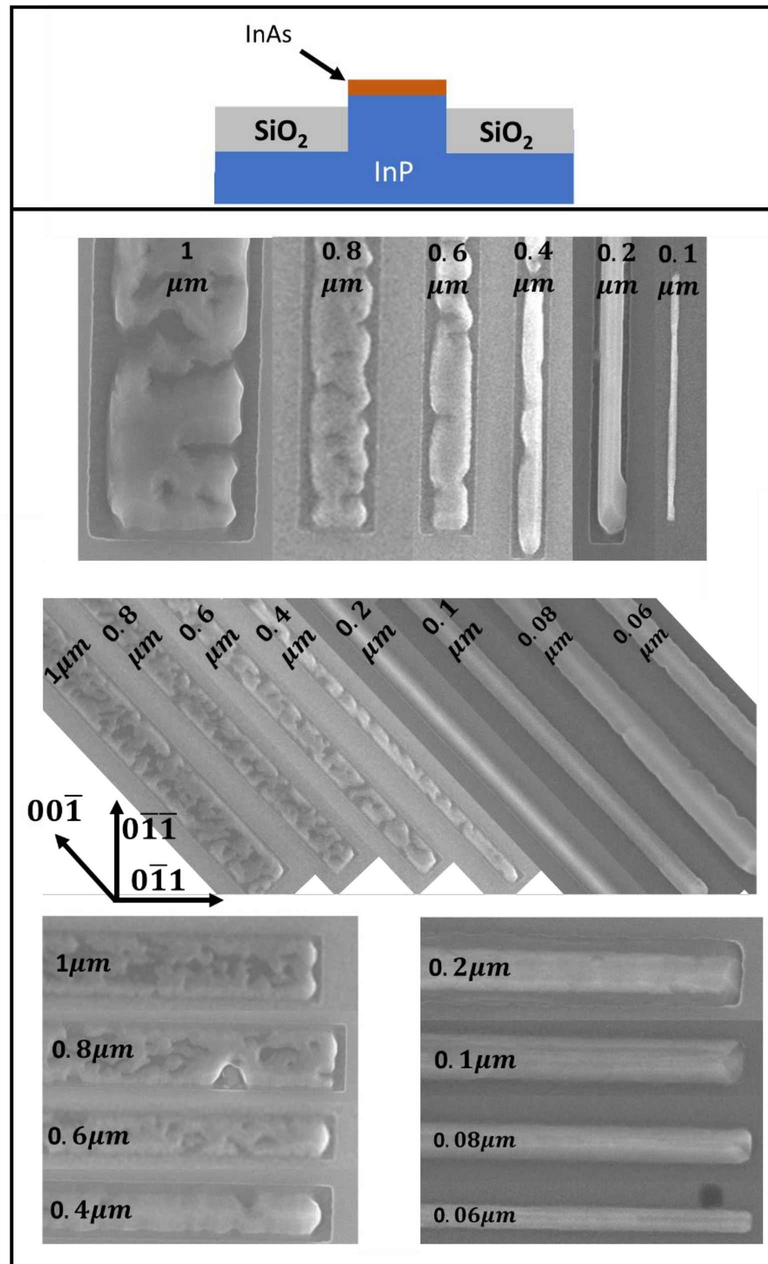


Figure 5.9: 2-minute InAs growth on 8-minute InP buffer in SAG template on InP (001) substrate at 520°C.

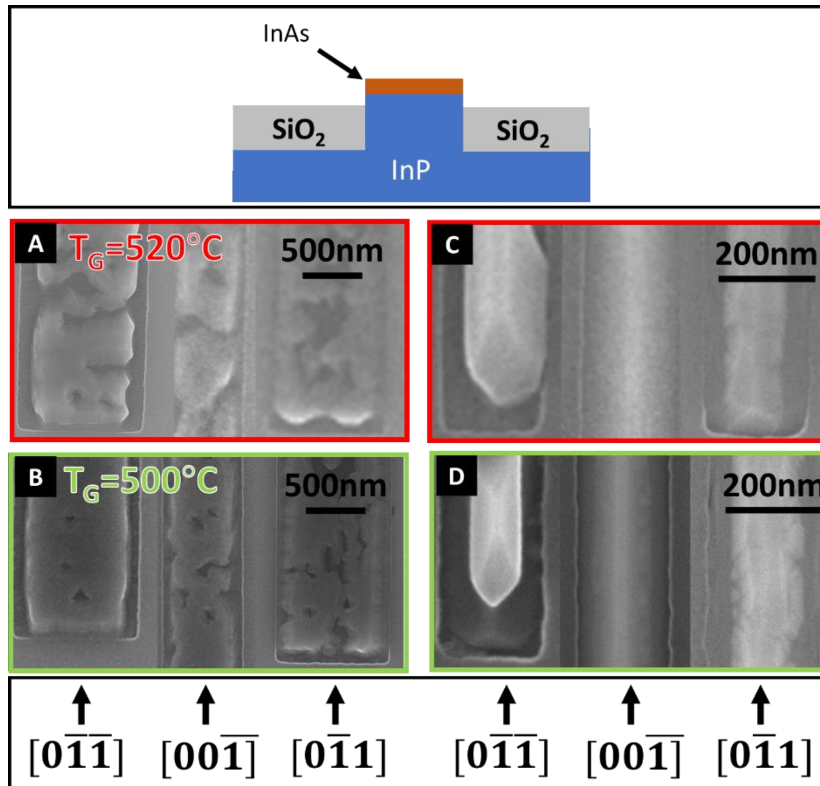


Figure 5.10: 2-minutes InAs growth on InP 8m buffers at 520°C and 500°C.

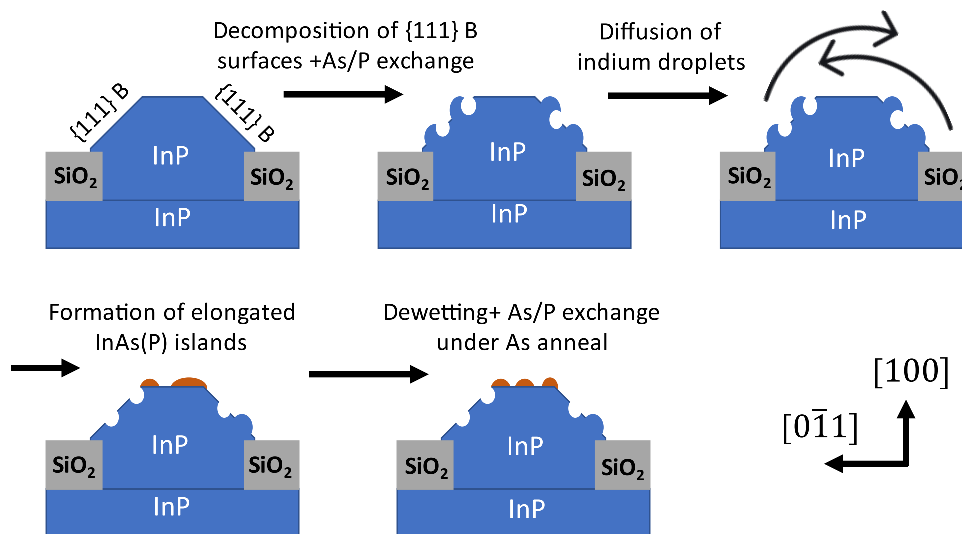


Figure 5.11: Schematic of proposed formation of island nucleation on the nanowires.

V.C. (iv). SAG of InAs nanowires on InP substrates various cooling procedures

Arsenics/phosphorus (As/P) exchange reactions can also occur during the cooldown process where the nanowire effectively spends 10-20 minutes (average time to cooldown samples with a standard rampdown in the CBE) under an arsenic flux at elevated temperatures. To understand the effect of the cooldown process, the following samples were investigated.

Sample number	Growth time for InP buffer layer	InAs growth time	InAs growth temperature	Cooled down after growth under	Figure number
5	8’	2’	520°C	As	12
6	8’	2’	520°C	P	12
7	8’	15”	480°C	As	13
8	8’	15”	480°C	No group-V	13
9	8’	15”	520°C	As	14
10	8’	15”	520°C	No group-V below 510 C	14

Figure 5.12 shows the SEM’s of sample # 5 and #6. When cooled under P, the nanowires exhibit a markedly different surface morphology compared to when cooled down under As. No degradation is observed along the {111}B surfaces for $[0\overline{1}\overline{1}]$ oriented nanowires and all the edge voids observed in Figure 5.12 A and 5.12 C are absent. The nanowire has a smooth

conformal shape with the presence of elongated island like nucleations. This can be explained by the phosphorus/arsenic exchange reactions (opposite mass transfer to arsenic/phosphorus exchange reaction) occurring under a high phosphorus overpressure. InP forms selectively around the InAs nucleations and proceeds to "fill up" the nanowire. This has been observed before in similar conditions [21] and is a strain driven process. Thus, the entire nanowire is covered with InP layer and also generates the same facets as the initial InP buffer layer, that can be understood by a minimization of total surface energy argument.

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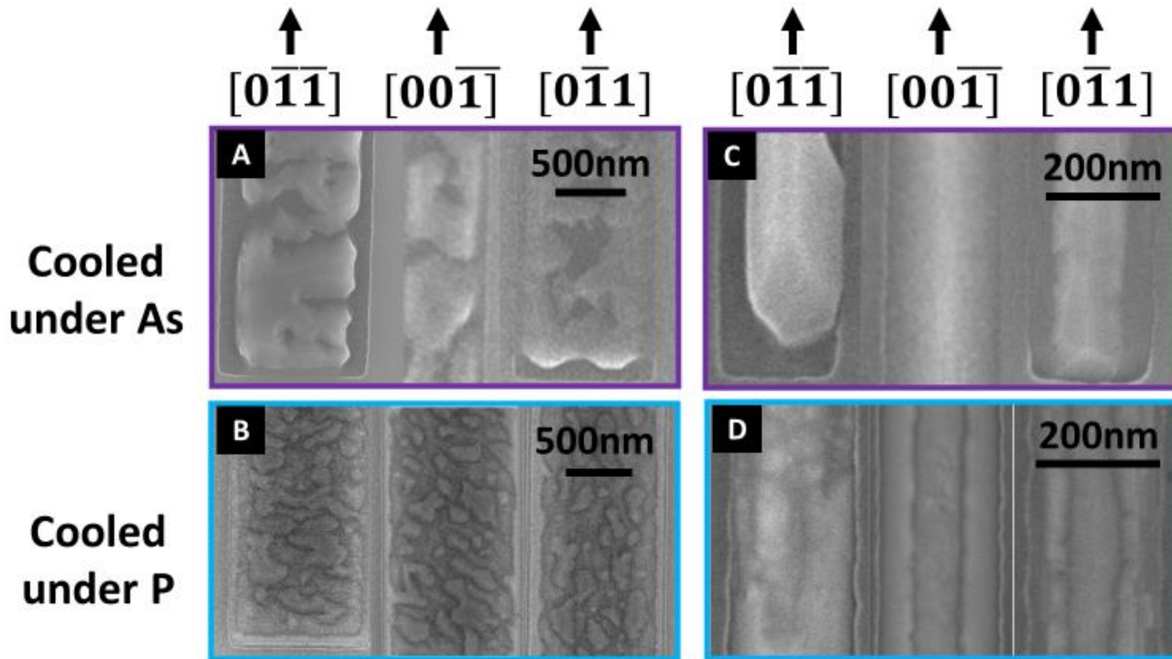

Figure 5.12: 2minutes InAs growth on InP 8m buffers at 520°C cooled under As and under P

Since the P cooling did not result in a desirable solution to obtain smoother InAs nanostructures, a different cooldown process was explored for samples #8 and sample #10. For sample #8 a 15 second InAs growth was performed at 480°C and then all group-V is stopped

and the sample was cooled down fast under no precursor overpressures. Sample #10 is similar except the growth of the InAs occurred at 520°C and all group-V was shut down below 510°C. These samples are then compared to samples #7 and sample #9 which are identical to samples #6 and #10 respectively, except that they were cooled under a As overpressure.

The results and the changes in nucleation are dramatic. For the 480°C growth the nucleation clearly exhibits larger islands in the case of a cooldown under As compared to a cooldown under no group-V. This suggests that a considerable amount of surface roughening and ripening [21] actually occurs during the cooldown. For the no group-V cooled sample, long strands of nucleations elongated along $[0\bar{1}1]$ are observed. These nucleation are presumably how the InAs actually nucleates prior to forming larger conglomerates and roughening during cooldown under As. Such "quantum wires" have been observed frequently in literature[21].

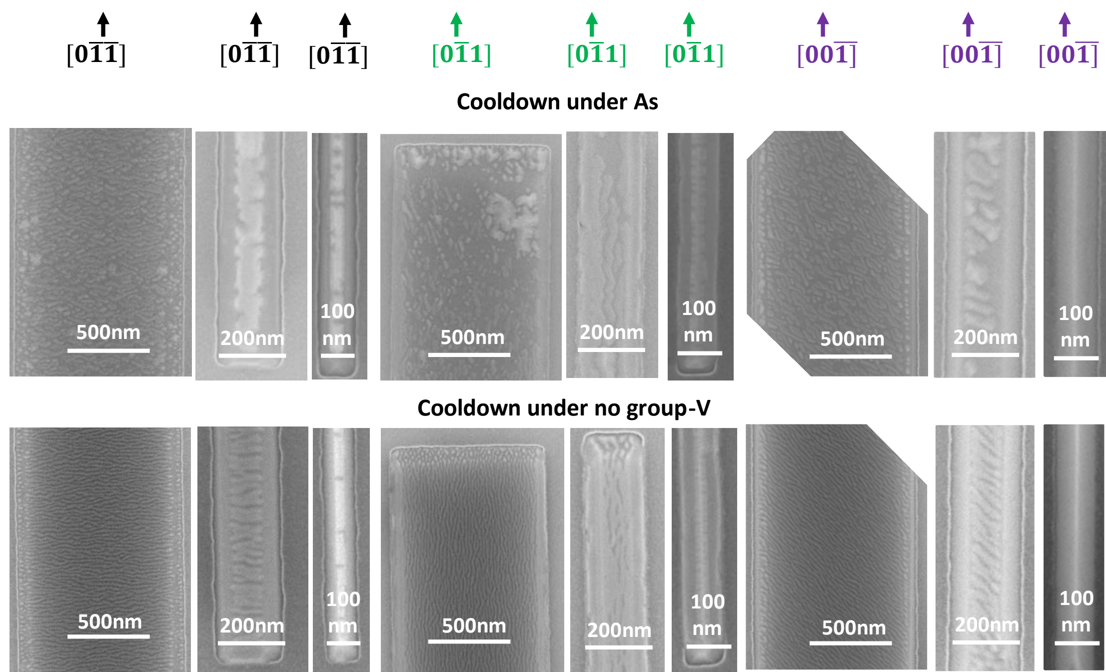

Figure 5.13: 15 seconds InAs growth on InP 8m buffers at 480°C cooled under As and under no group-V

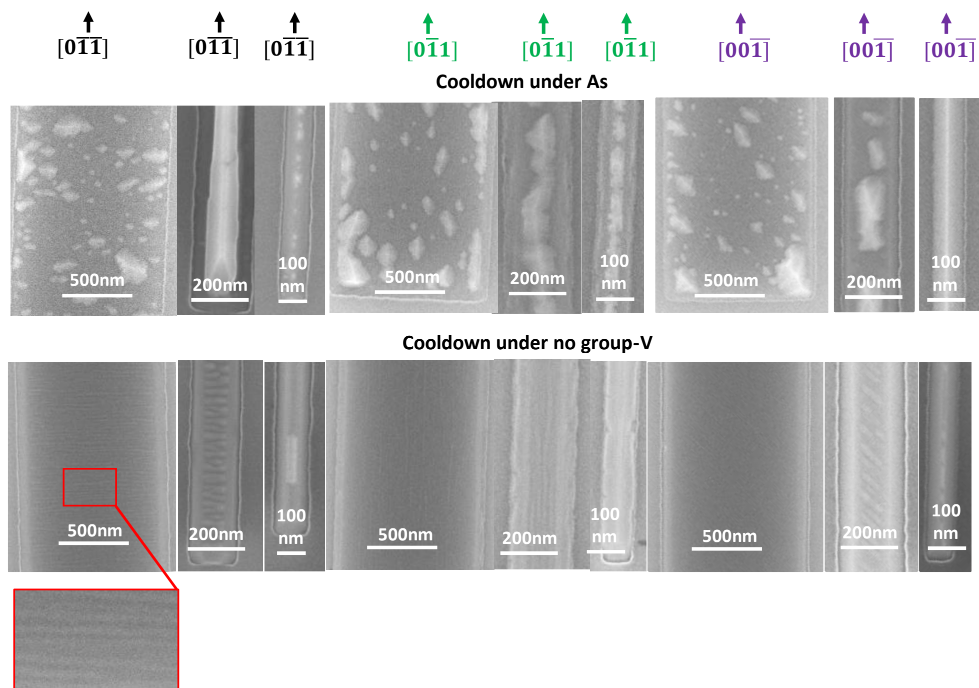

Figure 5.14: 15 seconds InAs growth on InP 8m buffers at 520°C cooled under As and under no group-V (inset shows long streaks of InAs nucleation)

For the 520°C growths (Figure 5.14) the nucleations for sample #10 (cooled under no group-V) exhibits long strands of nucleation ("wires/dashes"). When the sample is cooled under As, these islands "ripen" to form larger islands. The initial formation of these streaky InAs islands is believed to have a similar origin from controlled by the decomposition of the {111}B side facets. Figures 5.13-5.14 suggest that the roughening(through As/P exchange) / extra decomposition of the side facets probably occur during the long cooldown under As after the growth of the InAs channel.

Summary:

Cooldown processes post channel growth are extremely crucial in determining the final morphologies of the nanowires, but are often overlooked. A cooldown under no group-V overpressure was observed to preserve the initial shape of the nanostructures and prevents further roughening by limiting As/P exchange reactions. A cooldown under As resulted in ripening and decomposition of the side {111}B facets. A cooldown under P environment after the growth of the channel layer initiated P/As exchange and growth of InP around the InAs nucleations. Post-growth cooling environment can be an extremely important control knob in tuning the morphologies of the nanowires.

V.C. (v). SAG of InAs nanowires on InP (001) substrates using InGaAs buffers

Growing smooth InAs channels directly on InP (001) nanowires is always challenging due to the 3.1% lattice mismatch corresponding to a critical thickness of approximately 2-3nm. Therefore, in this section, the effect of a buffer layer on the InAs nucleation is investigated. The choice of a buffer material can be several for this system, but was determined by the availability of the precursors available in our CBE system. We first chose to use an indium gallium arsenide (InGaAs) buffer. Apart from relaxing mismatch conditions, an InGaAs buffer

layer can potentially reduce the As/P exchange reactions. Such techniques have been adopted in literature for nucleating InAs quantum dots [21] .

To ensure that InGaAs grows in these SAG templates, we first performed a InP(001) SAG growth followed by 3 different compositions of $In_xGa_{1-x}As$ (x=0.53, 0.65, 0.75) each for 1 minute growth and finally no InAs channel. The growths appear smooth and uniform with nicely defined facets. The parasitic growths were restricted to this particular sample.

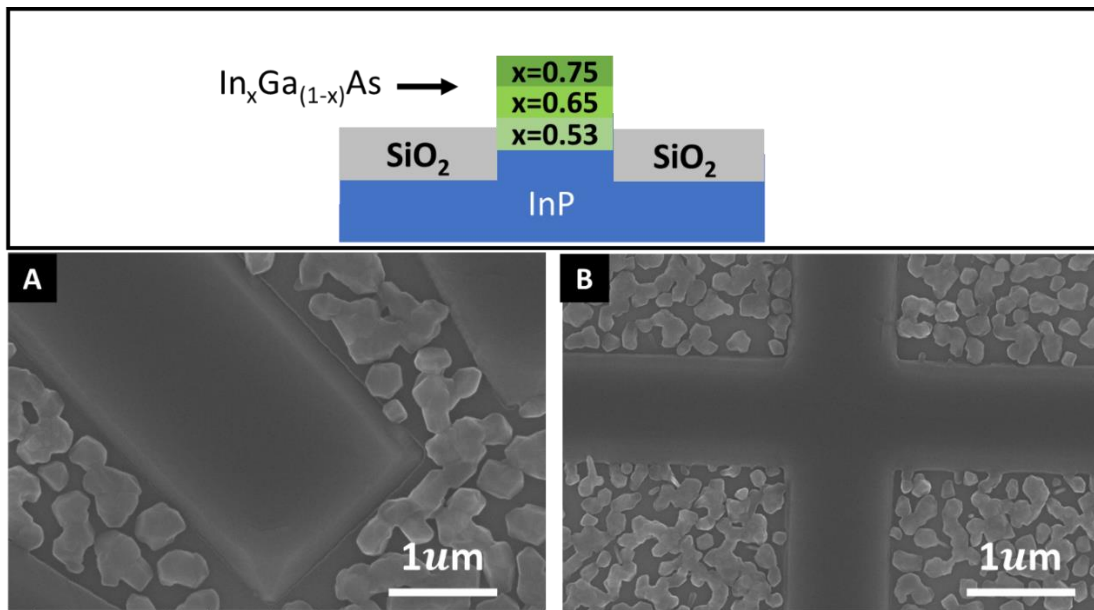

Figure 5.15: Graded InGaAs buffer grown on top of InP SAG buffer on InP (100) substrate.

For the first buffered InAs growth, a $In_{0.75}Ga_{0.25}As$ buffer grown for 2 minutes 30 seconds. Because of the high lattice mismatch with InP, this InGaAs buffer should be a partially relaxed. Compared to the InAs growths without buffer layers (Figure 5.8), the InAs nucleation on the $In_{0.75}Ga_{0.25}As$ buffer appears very different (Figure 5.16).

In the $[0\bar{1}\bar{1}]$ oriented nanowires, the nucleation initiates at the edges of the nanowire and then merge. While the islands in the 1um wide $[0\bar{1}\bar{1}]$ nanowire are un-merged, the 0.6 μm wide $[0\bar{1}\bar{1}]$ nanowire exhibits nearly merged islands. The 0.2 μm wide nanowire shows 3D island like nucleation that merge with {111}A facets. Below that width, the nanowires are overgrown and show micro-faceting. The $[0\bar{1}1]$ and $[00\bar{1}]$ nanowires also exhibit similar characteristics, and the fast diffusion direction (as suggested by the elongated InAs islands) is along $[0\bar{1}1]$. The $[0\bar{1}1]$ nanowires look much smoother compared to InAs without buffer (Figure 5.8-5.9). For widths below 200nm width, overgrowth results in micro-faceting. Overall, the use of the buffer layer improved growth morphologies in buffered InAs SAG nanowires.

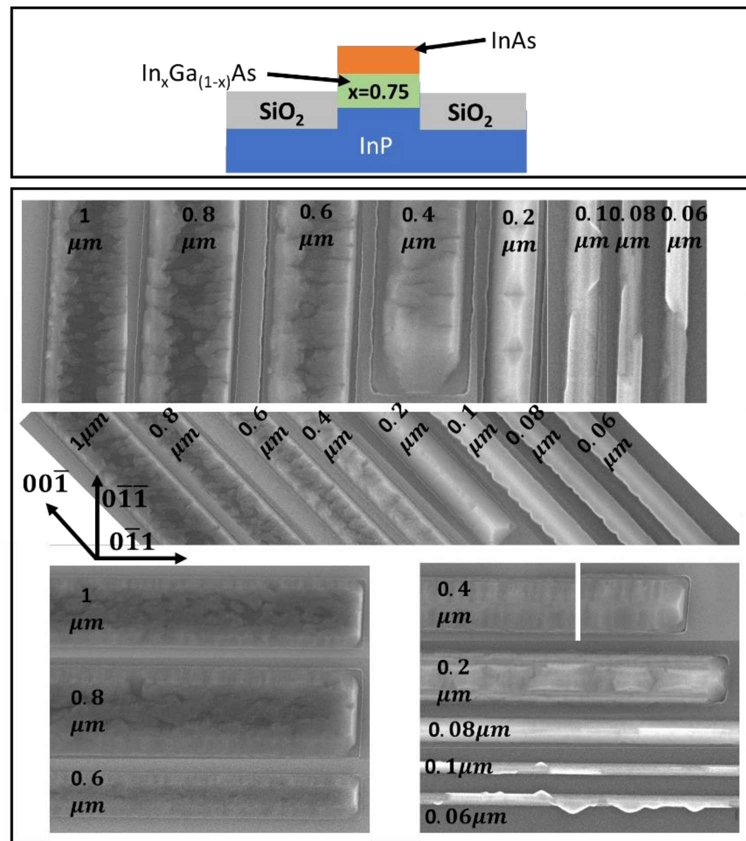

Figure 5.16: InAs grown on 150 seconds of $In_{0.75}Ga_{0.25}As$ buffer on InP SAG on InP (001) substrate.

Although a $In_{0.75}Ga_{0.25}As$ buffer works better, it has a relatively low band gap and potentially offers poor confinement for the channel. To solve this issue a graded buffer, similar to Figure 5.15, was explored. The buffer includes $In_xGa_{1-x}As$ (x=0.53, 0.65, 0.75) with each layer grown for 1 minute. The InAs channel was grown on top of this buffer (Figure 5.17).

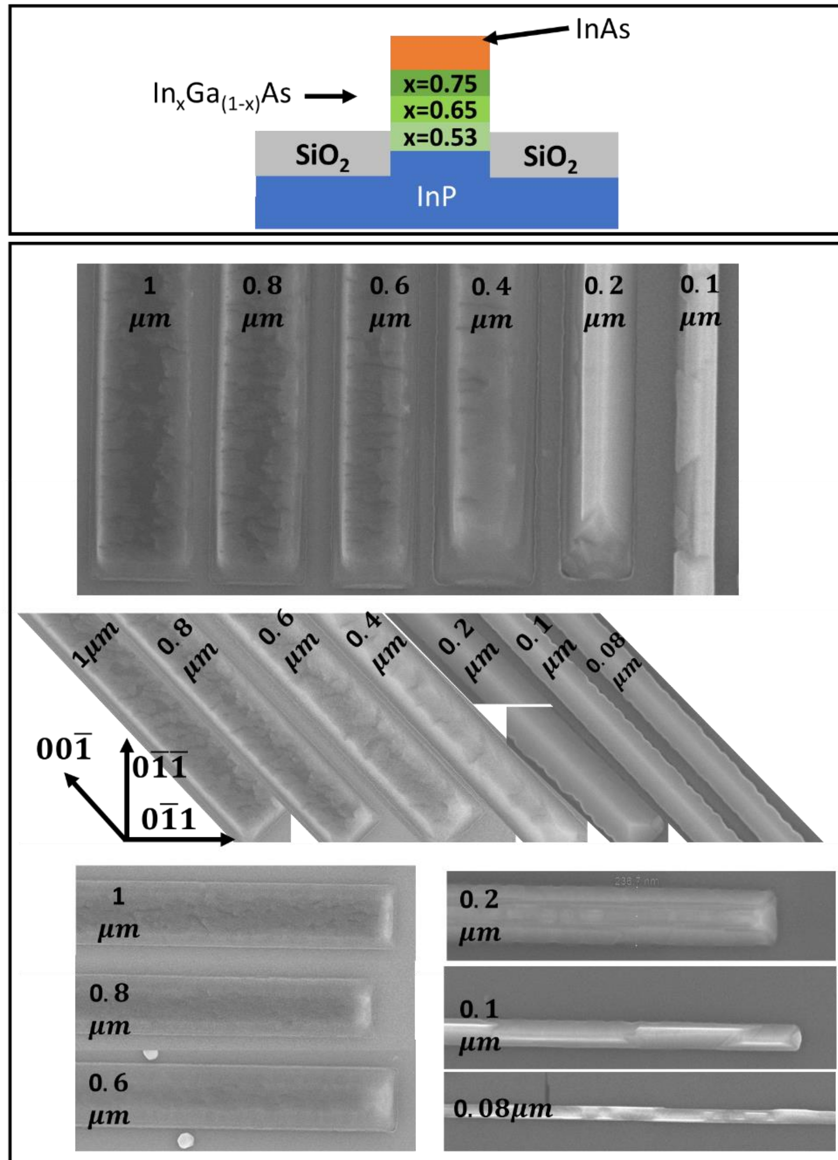

Figure 5.17: InAs grown on graded- InGaAs buffer on InP SAG on InP (001) substrate.

The nanowire growths look smooth for wide nanowires in all 3 orientations. The nucleations look almost identical to the previous growth (Figure 5.16). It should be noted that the total growth time for the InGaAs buffer is 30 seconds more than the previous growth, but

the InAs channel layer was grown for the same 60 seconds. The 200nm wide $[0\bar{1}\bar{1}]$ orientations look conformal and bound by primarily {111} facets. The 200nm wide nanowire oriented along $[00\bar{1}]$ exhibit smooth {110} facets. Along $[0\bar{1}1]$ a combination of {011}, {111}A and {100} facets emerge. The highly conformal InAs nucleations suggest low mismatch between the top layer of the buffer and the InAs channel.

A cross-sectional TEM characterization of this buffer layer (Figure 5.20) on the 200nm wide $[00\bar{1}]$ oriented nanowire shows the expected increase in indium concentration in the InGaAs buffer. (Note : the sample used for the TEM had a different channel thickness but identical buffer growth).The InGaAs buffer/ InP buffer interface also demonstrates no observable defects with clean sharp interfaces demonstrating minimal elemental interdiffusion.

Summary:

InGaAs buffers result in smoother morphologies of the InAs/InGaAs/InP nanowires. Both 70% indium and graded buffers exhibit smoother nucleation of the InAs channel and appears to completely suppress As/P exchange and decomposition of the side {111}B facets, consistent with previous observations[21] .

V.C. (vi). SAG of InAs channels with capping layers

In addition to engineering the buffer layer to reduce mismatch, it is crucial to passivate the nanowire surfaces to reduce scattering from surface roughness, surface oxidation or various adsorbates. Such strategies to improve mobilities using surface passivation have been reported in literature for VLS nanowires[22] . The next two growths study the morphology of the SAG nanowires using two different capping materials.

InP capping layer on InAs/InP (001) SAG nanowires

A 60 seconds InP layer was grown at 520°C on top of a InAs (2-minute growth) /InP buffer (8-minute growth)/InP (001) SAG sample. The SEMs (Figure 5.18) show that the growths are identical to the growth of InAs channel with a PH_3 cooldown (Figure 5.12). InAs nuclei are formed clearly on the 1um wide nanowires that diffuse faster along $[0\bar{1}1]$ and merge partially or fully in nanowires that are 200nm or less wide. The areas in between the nuclei are "filled up" by InP due to a strain driven P/As exchange reaction. Smooth growths can be achieved for <200nm wide wires along $[00\bar{1}]$, but the growth times needs to be carefully adjusted.

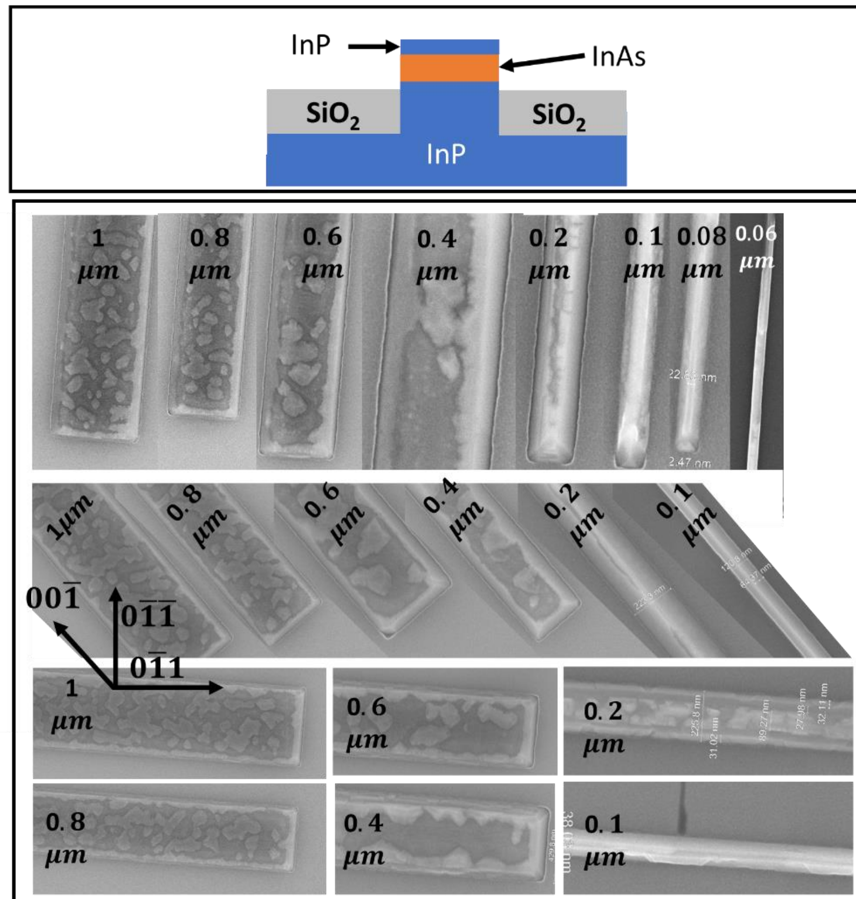

Figure 5.18: InAs grown on InP SAG on InP (001) substrate, with InP cap layer.

InGaAs capping layer on InAs/InP (001) SAG nanowires with graded InGaAs buffers

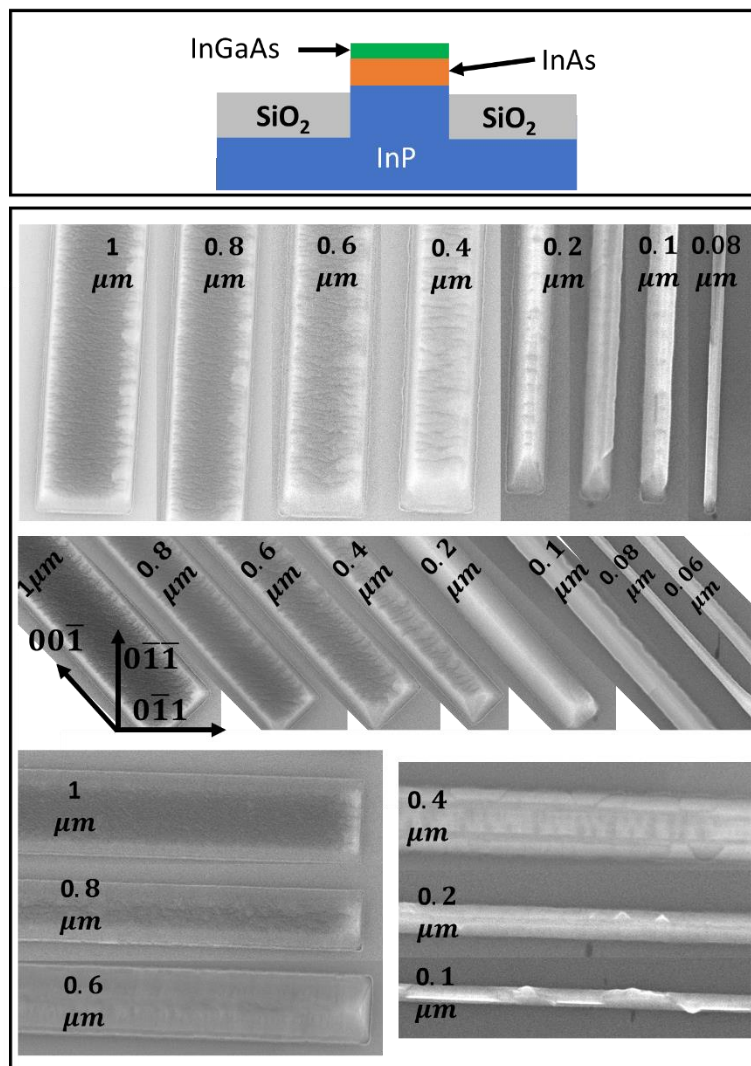

Figure 5.19 InAs SAG channel growth on a graded InGaAs/InP buffer and a InGaAs cap

Since a InP cap suffers from a lattice mismatch as well as a P/As exchange problem, an InGaAs capping layer was explored for the next structure. This sample was grown with a graded InGaAs buffer, identical to the one described before (Figure 5.17). The InAs channel was grown for 15 seconds (instead of the usual 60 seconds) and the top $In_{0.75}Ga_{0.25}As$ cap was

grown for 30 seconds after a 30 second anneal in between the InAs channel growth and the capping layer growth.

The growth in the wider $[0\bar{1}\bar{1}]$ oriented nanowires look rough, presumably because the InAs layer nucleated in long elongated dashes (similar to Figure 5.14). However, the thinner channels particularly in the $[00\bar{1}]$ orientation look smooth and uniform with clear $\{110\}$ facets. To investigate the buffer layer growth cross-sectional HAADF-STEM was performed on the $[00\bar{1}]$ oriented 200nm wide nanowire. The STEM micrograph (Figure 5.20) shows the InP buffer region, the graded InGaAs buffer and the InAs channel (along with the InGaAs capping layer) distinctly with sharp interfaces. The InP/InGaAs interface appears defect free and

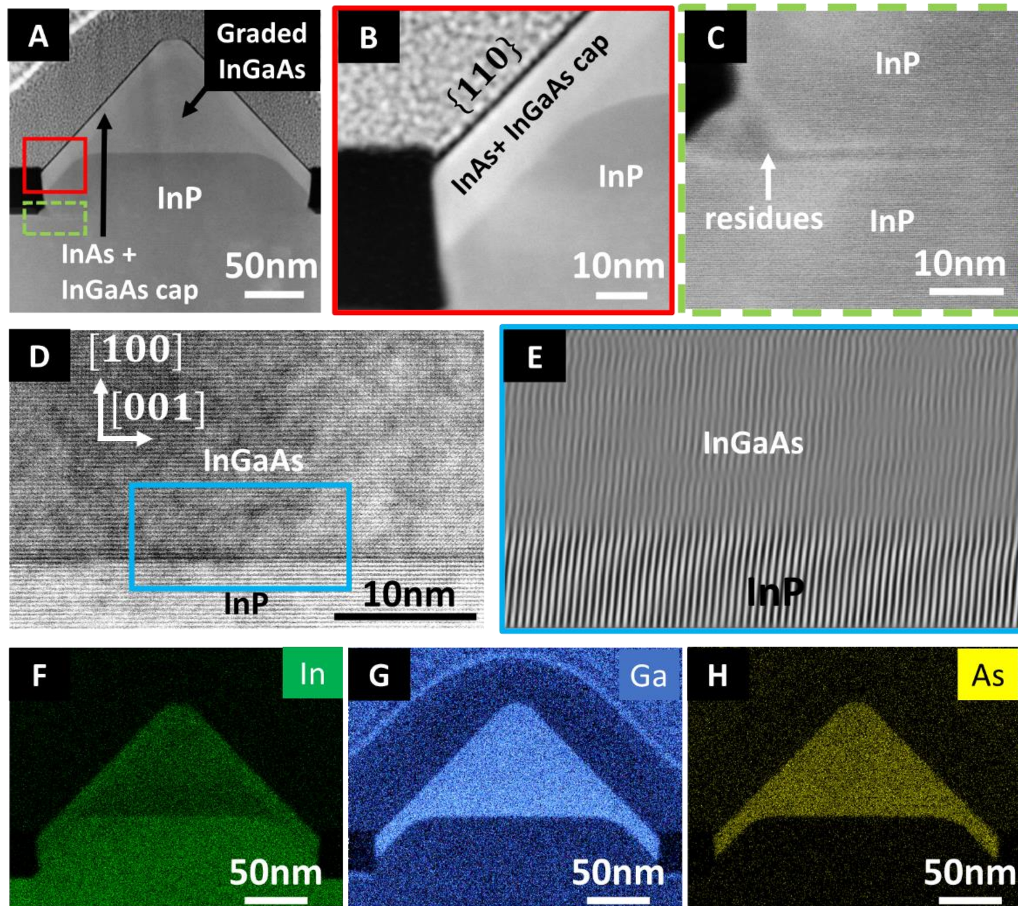

Figure 5.20: InAs SAG channel growth on a graded InGaAs/InP buffer and a InGaAs cap

continuous. The substrate-buffer interface shows some damage (or residues), shown in Figure

5.20 C. This demonstrates the importance of keeping the channel away from the substrate interface using the InP buffer layer. Energy dispersive X-ray (EDX) scans show the increase in indium content with height in the InGaAs buffer region as intended (Figure 5.20F). The InAs channel and the InGaAs capping layer cannot be distinguished in the thin layer.

Summary:

Growth of InP capping layers on InAs channels result in considerable and uncontrolled P/As exchange and growth of InP around the InAs nuclei. $In_{0.75}Ga_{0.25}As$ capping layers on a thin InAs channel appear smooth and uniform. This establishes the feasibility to cap the SAG nanowires effectively. Further optimization is required with growth rates and growth temperatures to grow smooth nanowires without micro-faceting for a targeted nanowire thickness.

V.C. (vii). SAG of nanowire InP/InGaAs/InP quantum wells

Quantum wells can result in high mobilities for planar films due to reduction in surface scattering, electron confinement effects and the formation of a 2D electron gas with very low scattering in carefully designed systems[23] .In this work, InP/InGaAs/InP quantum wells are grown with two different In/Ga compositions. The effect of channel width and channel orientations are studied.

Growth of InP was performed for 6-minutes at a corresponding planar growth rate of 0.5 ML/s**.** This growth rate does not accurately correspond to the growth rate inside small trenches as we will see in the next section. After the growth of the initial InP buffer layer, the TMI flow was stopped, and the sample was annealed at the same temperature under an overpressure of phosphorus. PH_3 was then switched to AsH_3 and after 5 seconds of AsH_3 flow

at 12 torr line pressure, both TMI and TEG were opened with respective line pressures of 0.5 torr and 0.66 torr for the lattice matched InGaAs case. The growth was continued for 45 seconds. The RHEED usually becomes a slightly fuzzier (2 x 4) reconstruction. TMI and TEG were then turned off. AsH_3 was turned off and switched to PH_3 flowing at 12 torr line pressure. The PH_3 flow was continued for 15 seconds before turning on TMI (0.5 torr) and a 3-minute growth of InP. After growth is complete, the sample was cooled down under a phosphorus overpressure.

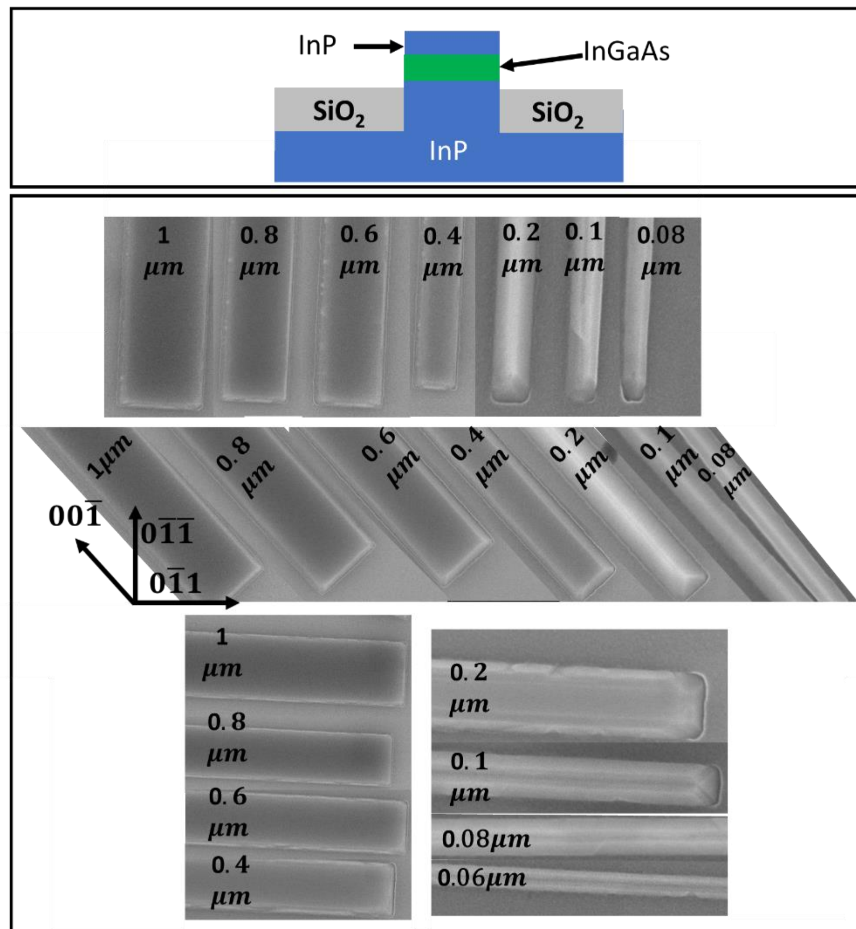

Figure 5.21: SEM of InP/ $In_{0.53}Ga_{0.47}As$ /InP heterostructure growths

SEM characterization (Figure 5.21) shows well faceted in-plane nanowires for all the wire thicknesses from 80nm to 1μm and all three orientations.

To analyze the facets and defects in these structures cross-sectional STEM analysis was performed on wires of different widths and different orientations for two different compositions of InGaAs channel. The 3 orientations chosen were along $[0\bar{1}\bar{1}]$, $[0\bar{1}1]$ and $[00\bar{1}]$ and the wire widths varied between 80nm to 1 um. These TEMs are shown in the Figures 5.22 and 5.24 for the lattice matched and high indium compositions respectively.

For $In_{0.53}Ga_{0.47}As$ channels, (Figure 5.22) the shapes of the quantum wells were observed to change dramatically with the width of the nanowires. For $[0\bar{1}\bar{1}]$ oriented nanowires initially a combination of {111}B and {311} facets were observed in both the InP buffer and capping layers as well as the InGAs QW. For the $[0\bar{1}1]$ oriented samples a combination of {111}A and {311} facets were observed. For both $[0\bar{1}\bar{1}]$ and $[0\bar{1}1]$ orientated nanowires (top 2 panels in Fig 5.22), the QW shape changed from a main center channel bound by side facets (of {111} and {311} type) to a horizontal quantum well with a smooth top (001) facet and small side facets. This transition was typically observed for nanowire widths above 200nm. In both these cases there is an increase in thickness towards the edge of the QW which has been reported previously in similar QW structures [24]. For the $[00\bar{1}]$ oriented nanowires (bottom panel in Fig 5.22) the QWs appeared markedly different. Below 200nm, the QWs contained two {110} type facets. Wires that are 220nm and wider exhibit a completely different QW shape with primarily (100) top facet and small {110} side facets.

In all three orientations, the thickness of the QW decreased as the width of the wires increase from 80 nm to 850nm (Figure 5.23).While the starting thicknesses were different due to the different shapes of the nanowires, the trend is consistent. This demonstrates that initially the quantum well thicknesses are determined completely by the shape of the InP buffer, but as

the wire widths increase, the growth becomes increasingly like a planar growth and saturates to the same planar growth thickness of approximately 13.5nm in all three orientations.

Both the $[0\bar{1}\bar{1}]$ and $[0\bar{1}1]$ oriented nanowires (top 2 panels in Fig 5.22) demonstrated a high density of defects. Stacking faults are observed along the {111} orientation originating from the edge of the silicon oxide mask. As the channel gets wider most of these stacking faults do not intersect the InGaAs channel. That the final shape of the InP cap is affected by these stacking faults, points to the fact that these are formed during the epitaxial growth and not because of thermal stresses induced by post growth cooling. The $[00\bar{1}]$ oriented samples did not show any of these defects possibly because the side facets in this orientation are devoid of

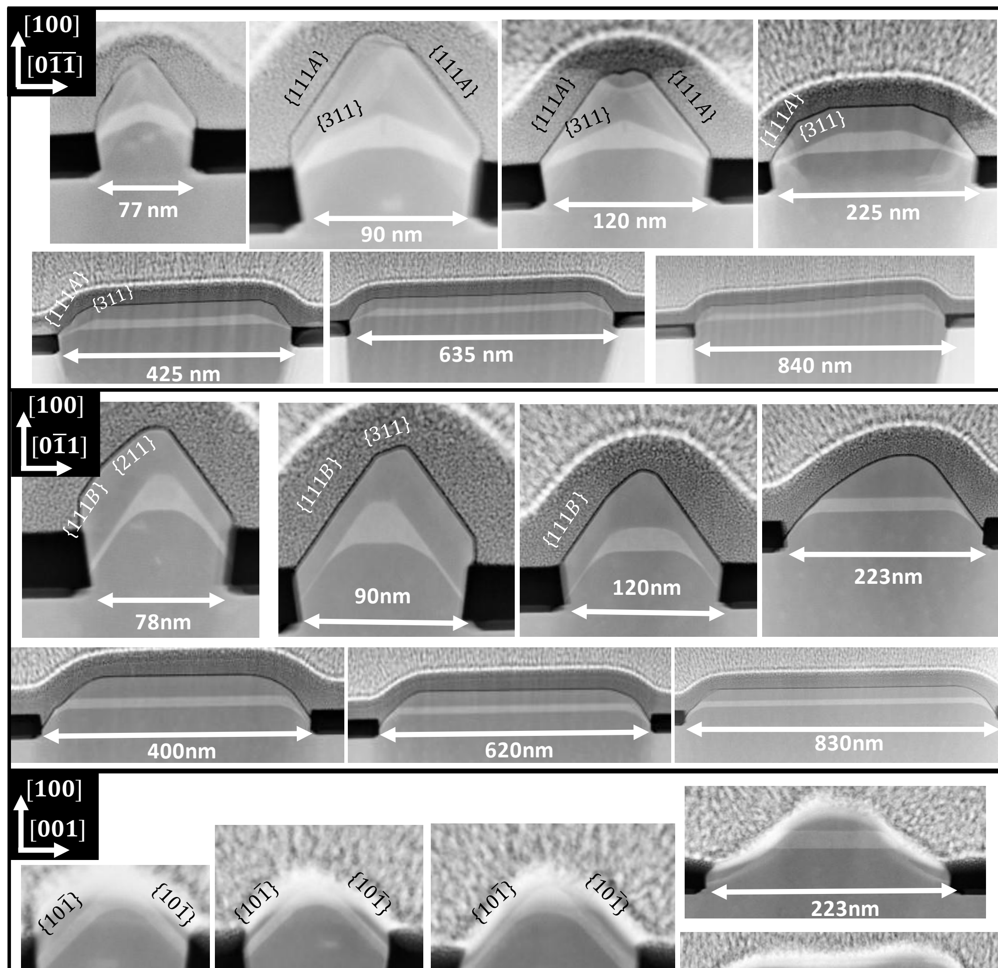

Figure 5.22: InP/ $In_{0.53}Ga_{0.47}As$ /InP quantum wells along three different orientations and different nanowire widths for lattice matched InGaAs composition.

any {111} type facets. This presents an excellent opportunity to use these $[00\bar{1}]$ oriented nanowires (and the wider nanowires in the other 2 orientations) to form defect free transport channels and reduce scattering/ improve mobility in these wires.

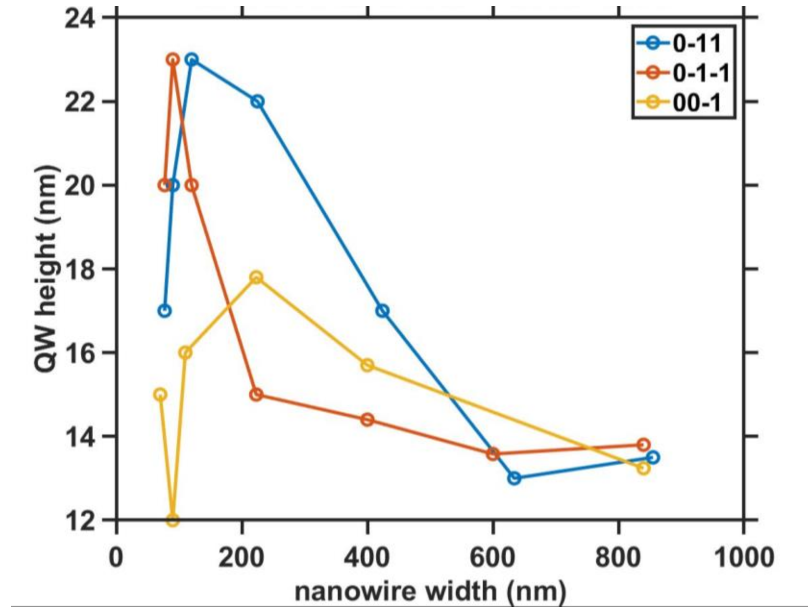

Figure 5.23: Lattice matched $In_{0.53}Ga_{0.47}As$ quantum well height vs nanowire width along three different orientations for InP $In_{0.53}Ga_{0.47}As$ /InP quantum wells in SAG on InP (100) substrate.

In the InP/$In_{0.70}Ga_{0.30}As$/InP QWs, the nanowires oriented along $[0\bar{1}1]$ and $[001]$ (top and bottom panels in Fig 5.24) appeared similar to the nanowires in the same orientations from the lattice matched InP/ $In_{0.53}Ga_{0.47}As$ /InP growths. However, for the nanowires oriented along $[0\bar{1}\bar{1}]$ (middle panel in Fig 5.24) the top surfaces of the quantum wells appeared thicker indicating increased surface diffusion along $[0\bar{1}1]$ with increasing indium content (and thereby increased lattice mismatch). However, the transition to a planar quantum well with side facets occurred at approximately the same thickness of the nanowire (~200nm). The defects appeared similar as well, mostly appearing in the nanowires oriented along $[0\bar{1}1]$ and $[0\bar{1}\bar{1}]$, while the

nanowires oriented along [001] are defect free. These stacking faults originating from the SiO_2/InP interface are shown more clearly in Figure 5.25. Figure 5.25 (C) demonstrates how the [001] oriented nanowires did not exhibit any stacking faults at the SiO_2/InP boundary. The InGaAs quantum wells in the [001] orientation also appeared defect free and crystalline including controllable growth of atomically sharp monolayer InGaAs quantum wells (Figure 5.26).

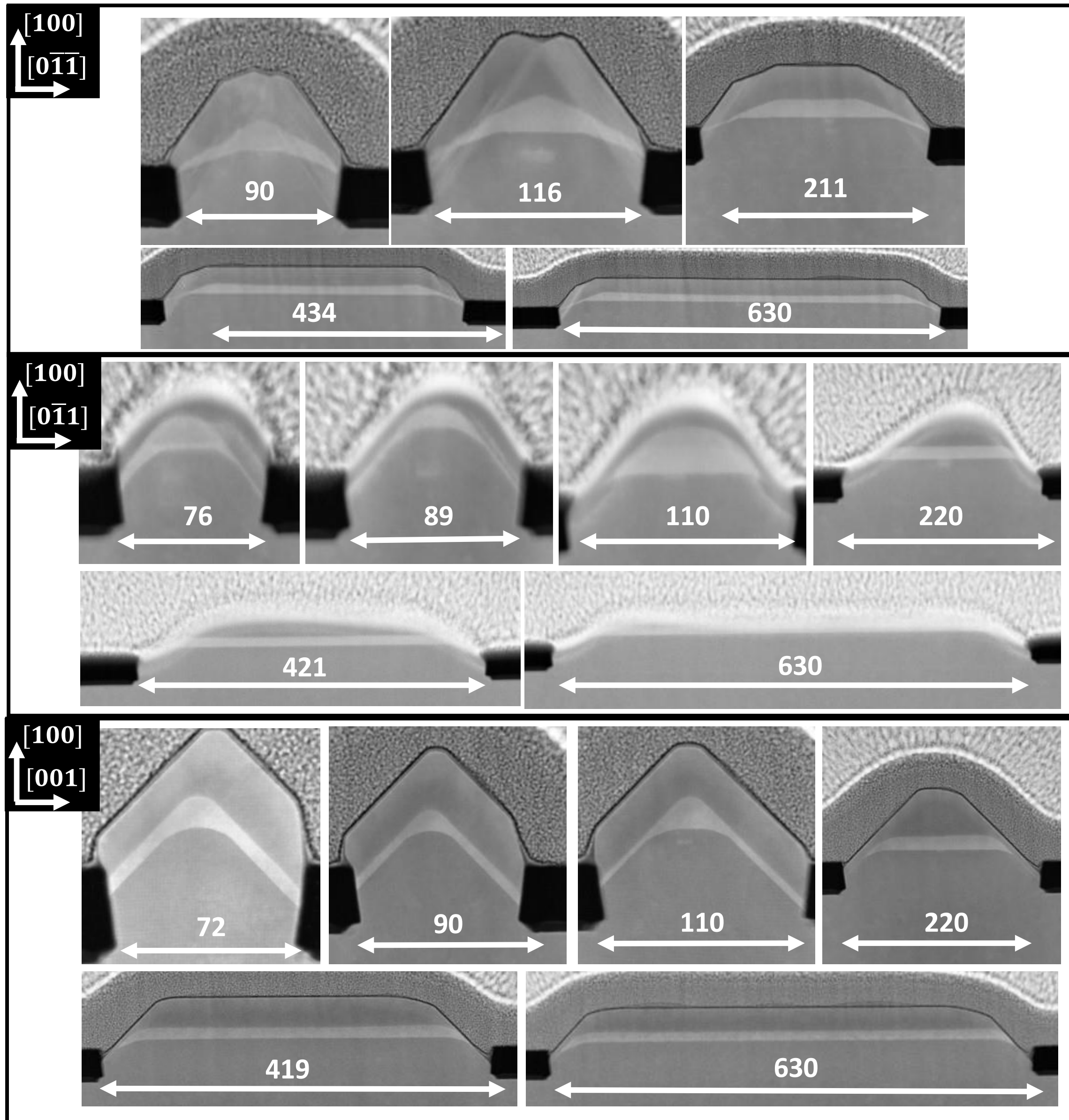

Figure 5.24: InP/ $In_{0.7}Ga_{0.3}As$ /InP quantum wells along three different orientations and different nanowire widths.

The interfaces between the heterostructures (such as InP/InGaAs) is of crucial interest. Non-uniformity at these junctions can lead to changes in electron scattering and wavefunction confinement inside the quantum well. In the InP/InGaAs/InP quantum wells a group V switch occurs at both the interfaces. While the phosphorus to arsenic transition is extremely abrupt in the cross-sectional STEM images (Figure 5.26), the arsenic to phosphorus transition in general appears fuzzy in various quantum well geometries and orientations (Figure 5.26 (A)-(B)). This phenomenon has been previously observed in planar epitaxy.

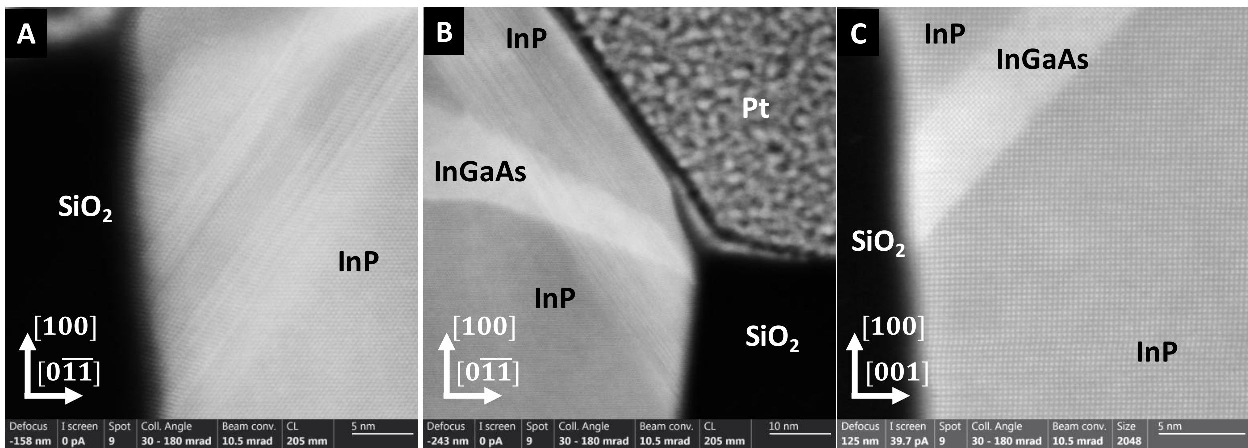

Figure 5.25: InP/$In_{0.7}Ga_{0.3}As$/InP quantum wells exhibiting stacking faults along {111} for nanowires oriented along [0$\bar{1}$1] (A and B), originating at the semiconductor/ SiO_2 interface. (C) The same interface when the nanowire is oriented along [00$\bar{1}$].

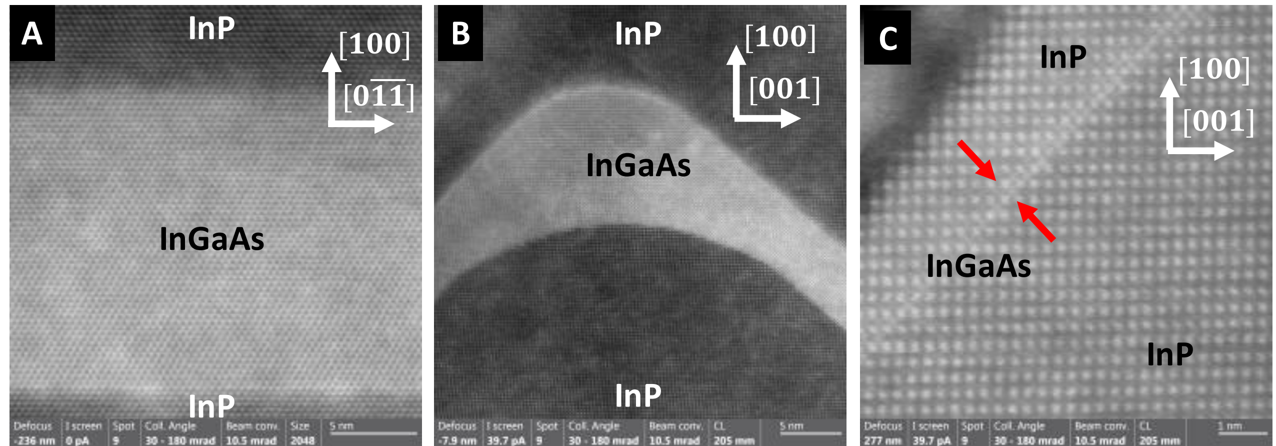

Figure 5.26: InP/$In_{0.7}Ga_{0.3}As$/InP quantum wells along three different orientations and different nanowire widths for $In_{0.7}Ga_{0.3}As$ composition.

Summary:

InP/InGaAs/InP quantum wells were successfully grown in the SAG geometry with two different compositions of the InGaAs channel (53% indium and 70% indium) and structural characterization was performed using STEM. Defect-free channels were observed along the $[00\bar{1}]$ orientation, while the other orientations demonstrate stacking faults. Careful optimization of growth times was used to demonstrate that the transport channel can be grown completely free of defects. The shapes of the quantum wells can be tuned to a large extent by selecting the nanowire widths and orientation. This opens the door to creating "designer quantum wells" in the SAG nanowires and offers the opportunity to perform interesting transport experiments at low temperatures. The top InP thickness can be adjusted to make it into a tunneling barrier for spin injection from a ferromagnet or cooper pair tunneling from an adjacent superconductor. Future work in this will aim to electrically characterize these nanowires and optimize growth conditions to achieve higher mobilities.

References:

[1] E. Majorana, “Teoria simmetrica dell’elettrone e del positrone,” *Il Nuovo Cimento (1924-1942) 1937 14:4*, vol. 14, no. 4, pp. 171–184, Sep. 2008, doi: 10.1007/BF02961314.

[2] J. Alicea, Y. Oreg, G. Refael, F. von Oppen, and M. P. A. Fisher, “Non-Abelian statistics and topological quantum information processing in 1D wire networks,” *Nature Phys.*, vol. 7, no. 5, pp. 412–417, 2011, doi: 10.1038/nphys1915.

[3] J. D. Sau, D. J. Clarke, and S. Tewari, “Controlling non-Abelian statistics of Majorana fermions in semiconductor nanowires,” *Phys. Rev. B*, vol. 84, no. 9, p. 094505, Sep. 2011, doi: 10.1103/physrevb.84.094505.

[4] A. Y. Kitaev, “Fault-tolerant quantum computation by anyons,” *Ann. Phys.*, vol. 303, no. 1, pp. 2–30, 2003, doi: 10.1016/s0003-4916(02)00018-0.

[5] M. Sato and S. Fujimoto, “Majorana Fermions and Topology in Superconductors,” 2016, doi: 10.7566/JPSJ.85.072001.

[6] A. Y. Kitaev, “Unpaired Majorana fermions in quantum wires,” *Physics-Uspekhi*, vol. 44, no. 10S, p. 131, Oct. 2001, doi: 10.1070/1063-7869/44/10S/S29.

[7] R. M. Lutchyn, J. D. Sau, and S. das Sarma, “Majorana fermions and a topological phase transition in semiconductor-superconductor heterostructures,” *Physical Review Letters*, vol. 105, no. 7, p. 077001, Aug. 2010, doi: 10.1103/physrevlett.105.077001/figures/3/medium.

[8] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, “Signatures of majorana fermions in hybrid superconductor-semiconductor nanowire devices,” *Science (1979)*, vol. 336, no. 6084, pp. 1003–1007, 2012, doi: 10.1126/science.1222360.

[9] A. Das, Y. Ronen, Y. Most, Y. Oreg, M. Heiblum, and H. Shtrikman, “Zero-bias peaks and splitting in an Al–InAs nanowire topological superconductor as a signature of Majorana fermions,” *Nature Physics 2012 8:12*, vol. 8, no. 12, pp. 887–895, Nov. 2012, doi: 10.1038/nphys2479.

[10] J. Chen *et al.*, “Ubiquitous non-Majorana zero-bias conductance peaks in nanowire devices,” *Physical Review Letters*, vol. 123, no. 10, p. 107703, Sep. 2019, doi: 10.1103/PHYSREVLETT.123.107703/FIGURES/4/MEDIUM.

[11] J. Jung *et al.*, “Universal Platform for Scalable Semiconductor-Superconductor Nanowire Networks,” *Advanced Functional Materials*, vol. 31, no. 38, p. 2103062, Sep. 2021, doi: 10.1002/ADFM.202103062.

[12] P. Aseev *et al.*, “Ballistic InSb Nanowires and Networks via Metal-Sown Selective Area Growth,” *Nano Letters*, vol. 19, no. 12, pp. 9102–9111, Dec. 2019, doi: 10.1021/ACS.NANOLETT.9B04265/SUPPL_FILE/NL9B04265_SI_001.PDF.

[13] R. L. M. Op het Veld *et al.*, “In-plane selective area InSb–Al nanowire quantum networks,” *Communications Physics 2020 3:1*, vol. 3, no. 1, pp. 1–7, Mar. 2020, doi: 10.1038/s42005-020-0324-4.

[14] P. Aseev *et al.*, “Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks,” *Nano Letters*, p. acs.nanolett.8b03733, 2018, doi: 10.1021/acs.nanolett.8b03733.

[15] S. Mauthe *et al.*, “High-speed III-V nanowire photodetector monolithically integrated on Si,” *Nature Communications 2020 11:1*, vol. 11, no. 1, pp. 1–7, Sep. 2020, doi: 10.1038/s41467-020-18374-z.

[16] Z. Wang *et al.*, “Room-temperature InP distributed feedback laser array directly grown on silicon,” *Nature Photonics 2015 9:12*, vol. 9, no. 12, pp. 837–842, Oct. 2015, doi: 10.1038/nphoton.2015.199.

[17] Y. Y. Hhh *et al.*, “Bufferless 1.5 µm III-V lasers grown on Si-photonics 220 nm silicon-on-insulator platforms,” *Optica, Vol. 7, Issue 2, pp. 148-153*, vol. 7, no. 2, pp. 148–153, Feb. 2020, doi: 10.1364/OPTICA.381745.

[18] K. Tomioka and T. Fukui, “Recent progress in integration of III–V nanowire transistors on Si substrate by selective-area growth,” *Journal of Physics D: Applied Physics*, vol. 47, no. 39, p. 394001, Sep. 2014, doi: 10.1088/0022-3727/47/39/394001.

[19] N. Gogneau *et al.*, “One-step nano-selective area growth (nano-SAG) of localized InAs/InP quantum dots: First step towards single-photon source applications,” *Journal of Crystal Growth*, vol. 310, no. 15, pp. 3413–3415, Jul. 2008, doi: 10.1016/J.JCRYSGRO.2008.04.019.

[20] F. Krizek, “Semiconductor Nanowire Networks Grown By Molecular Beam Epitaxy Vapor-Liquid-Solid,” *Phd. Thesis*, 2018.

[21] von Dipl-Phys Oliver Bierwagen, C. Markschies, C. Limberg Gutachter, W. T. Masselink, R. Fornari, and G. J. Salamo, “Growth and anisotropic transport properties of self-assembled InAs nanostructures in InP”.

[22] Q. Hang *et al.*, “Role of molecular surface passivation in electrical transport properties of InAs nanowires,” *Nano Letters*, vol. 8, no. 1, pp. 49–55, Jan. 2008, doi: 10.1021/NL071888T/ASSET/IMAGES/MEDIUM/NL071888TN00001.GIF.

[23] S. A. Studenikin, G. Granger, A. Kam, A. S. Sachrajda, Z. R. Wasilewski, and P. J. Poole, “Nonlinear magnetotransport phenomena in high-mobility two-dimensional electrons

in InGaAs/InP and GaAs/AlGaAs," *Physical Review B - Condensed Matter and Materials Physics*, vol. 86, no. 11, p. 115309, Sep. 2012, doi: 10.1103/PHYSREVB.86.115309/FIGURES/8/MEDIUM.

[24] I. v. Kulkova, S. Kadkhodazadeh, N. Kuznetsova, A. Huck, E. S. Semenova, and K. Yvind, "High-quality MOVPE butt-joint integration of InP/AlGaInAs/InGaAsP-based all-active optical components," *Journal of Crystal Growth*, vol. 402, pp. 243–248, 2014, doi: 10.1016/J.JCRYSGRO.2014.06.026.

[25] D. J. Carrad *et al.*, "Shadow Epitaxy for In Situ Growth of Generic Semiconductor/Superconductor Hybrids," *Advanced Materials*, vol. 32, no. 23, p. 1908411, Jun. 2020, doi: 10.1002/ADMA.201908411.

[26] S. Heedt *et al.*, "Shadow-wall lithography of ballistic superconductor–semiconductor quantum devices," *Nature Communications 2021 12:1*, vol. 12, no. 1, pp. 1–9, Aug. 2021, doi: 10.1038/s41467-021-25100-w.

[27] Y. Jiang *et al.*, "Selective area epitaxy of PbTe-Pb hybrid nanowires on a lattice-matched substrate," *Physical Review Materials*, vol. 6, no. 3, p. 034205, Mar. 2022, doi: 10.1103/PHYSREVMATERIALS.6.034205/FIGURES/4/MEDIUM.

[28] J. Jung *et al.*, "Universal Platform for Scalable Semiconductor-Superconductor Nanowire Networks," *Advanced Functional Materials*, vol. 31, no. 38, p. 2103062, Sep. 2021, doi: 10.1002/ADFM.202103062.

VI. *In-situ* shadow wall deposition of tin on selective area grown InAs nanowires

A fundamental requirement in fabricating hybrid superconductor-semiconductor nanowire devices is to have clean disorder free interface[25]. This clean interface is crucial to inducing a hard proximity induced superconducting gap in the semiconducting nanowire. Presence of subgap states - also known as a soft gap – that arise primarily due to disorder (oxides, carbon, damage) at the superconductor-semiconductor interface. A possible route to ahcieve such pristine interfaces is to deposit the superconductor *in-situ* (without breaking vaccum) after the growth of the nanowires. A blanket deposition of such a superconductor will however require etching off the superconductor in the undesirable areas to be able to create contacts.

This technique, although will result in a pristine superconductor-semiconductor interface, suffers from two major problems. One, any kind of wet or dry etch (with or without plasma) to etch the superconductors will inevitably introduce damage and form defects and/or ion implantations in the semiconducting nanowire, thus reducing its electrical quality. Second, the chemistry to properly etch a number of superconductors is not well known and as a result for the majority of the experiments common superconductors such as aluminum or tin have to be used. These challenges warrant finding a technique that can in-situ deposit superconductors, but only at sites on the nanowire where they are required.

For such *in-situ* patterning, a number of techniques have been proposed. In a shadow mask technique a stencil mask is fabricated from silicon nitride on top of a trench containing a VLS nanowire seed [25]. After the growth of the vertical nanowires these stencil masks are used to deposit superconductors only in specific regions of the vertical nanowire. This

technique, though elegant suffers from scalability challenges. Using this technique one can only fabricate indivdual nanowires that have to be thereafter picked-and-placed using a micromanipualtor onto a substrate. Moreover, the smallest resolution of the superconducting gap or superconducting islands one can achieve using this technique is limited to the lowest width of the delicate SiN_x membrane mask.

The second technique makes use of "smart walls" which are dielectric walls fabricated on a silicon substrate [26]. These walls can have high aspect ratios and the thickness of these structures can be very small (~100nm or of the order of). Next, VLS grown semiconducting nanowires are picked and placed horizontally near these walls. A hydrogen claning procedure is performed to clean the surface of the semiconducting nanowire from oxides or absorbed contaminants and thereafter the shadow walls are used to mask the nanowire in areas during the angled superconductor deposition. This process can successfully create very short junctions on the nanowire but again suffers from a number of challenges. One, the nanowire is picked and placed and in the process of pushing it close to the shadow walls undergoes a large amount of strain and mechnaical distortion. The distance from the nanowire to the nearest shadow wall will be variable and highly dependent on the particular pick-and-place run. Next, the hydrogen cleaning step requires that the exact conditions to clean each facet of the nanowire be known. Since hydrogen cleaning is highly facet dependent, the only reliable method to test its success is by performing atomic resolution STM or high-resolution TEM. It is an extremely complex and time-consuming technique to choose for cleaning up the nanowire. Hydrogen cleaning also might not work for a number of semiconductors and therefore the process limits the materials that researchers can explore for performing such experiments.

The third technique is using silicon oxide shadow walls that are prefabricated by exposing the "spin-on glass" Hydrogen SilsesQuioxane (HSQ) and depositing the AlO_x mask, finally wet etching the AlO_x to open up selective area growth trenches on a CdTe (001) substrate[27]. Thereafter a PbTe nanowire was grown and the shadow walls are used to angle deposit superconductor Pb on the nanowire. This report is the closest to a scalable reliable method to fabricate such structures. However, the HSQ method has severe limitations on the height and aspect ratios of the shadow walls that one can fabricate. This in turn requires the nanowires to be extrememly close to the walls for a shadow wall, thus limiting flexibility to form larger networks. In addition, the junctions fabricated were all in greater than 500nm. Fabricating the nanowire trenches here might also pose a problem because of the resist profile around a tall structure has a significant height gradient. Therefore the exposure in the EBL will be non-uniform and will lead to inaccurate dimensions. Other versions of this last report include using selective area grown InP walls grown on (111)A InP substrate[28] , as shadow

walls and subsequently fabricating nanowire trenches in close proximity to the walls for the next SAG growth step for the nanowires. This report although very creative is limited by the choice of substrates, parasitic growth on the walls and the poor aspect ratios of the shadow walls. In addition, complex crystal facets that will naturally form on the shadow walls will need to be considered and will further limit the applicability of this technique.

In this work, a fully scalable and completely customizable shadow wall technique is reported for InAs SAG on InP (001) substrates. Here, the shadow wall templates are fabricated fully before initiating any growth steps. The nanowire is grown using chemical beam epitaxy and thereafter, the sample is in-situ transferred to the interconnected MBE system containing a cold stage and effusion cells for evaporating superconductors aluminum and tin. The superconductors are deposited with a shadowing angle and result in superconducting islands

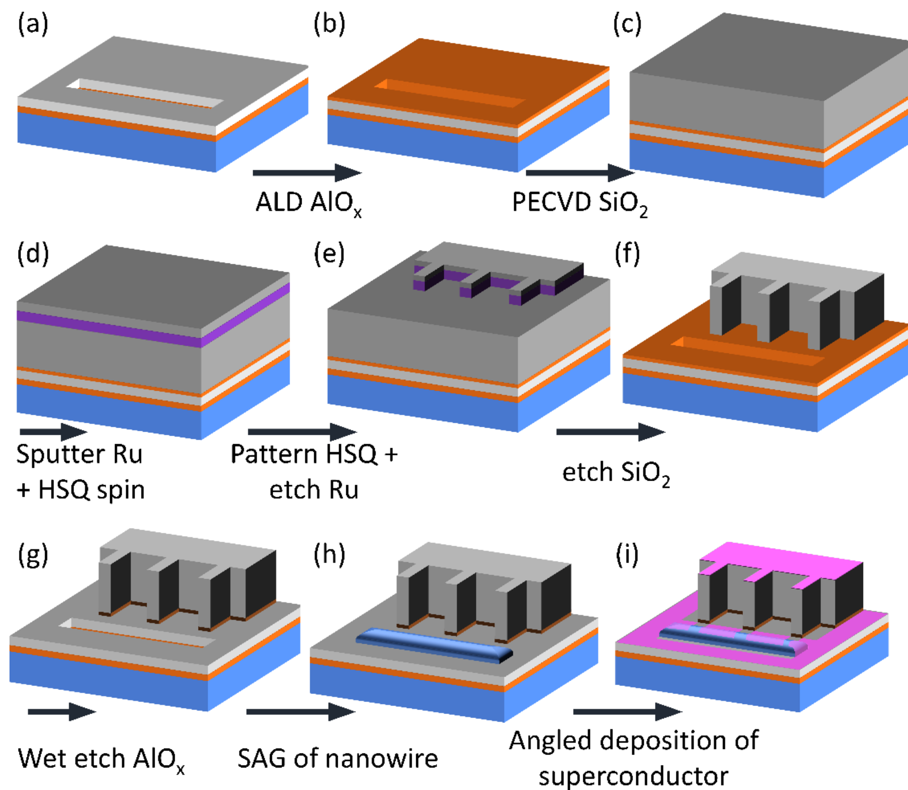

Figure 5.27 : Fabrication steps to form shadow wall templates with SAG trench.

that are ~100nm thick. The fabrication of the selective area growth shadow wall template is described below.

First, a InP(001) substrate is masked with a 6nm ALD deposited AlOx layer and a 30nm PECVD deposited SiO2 layer. The AlO_x layer as mentioned before protects the surface of the InP from plasma damage as well as non-volatile fluorine residues from dry etches. Following this, alignment marks are patterned using EBL and the SiO_2 is etched using a $CHF_3/CF_4/O_2$ etch in an inductively coupled plasma chamber. The AlO_x is removed under the etched SiO_2 using a wet etch in AZ300MIF (a developer that etches aluminum containing compounds). Following this, using the SiO_2 hard mask, the InP is etched by reactive ion etching in a Methane/Hydrogen/Argon chemistry. All the deposited dielectrics are etched away by performing a buffered HF etch and the 6nm of ALD AlO_x and 30nm of PECVD SiO_2 is redeposited. This forms the dielectric mask layer for the SAG of the naowires and it is crucial to select PECVD as the deposition technique for this step to minimize the parasitic growth. Using the alignment marks, the naowire trenches are now exposed in the EBL and the SiO_2 layer is etched in the same chemistry as before in an ICP chamber. The AlO_x layer is not etched. A 20nm AlO_x layer is deposited using ALD on top of the sample. This is followed by a 650nm layer of SiO_2 deposited using PECVD and a 150nm layer of Ru deposted using sputtering. HSQ is spun as a resist on top and the shadow wall designs are exposed in the EBL. Following the development of the HSQ in TMAH, the HSQ (now SiO_2 after electron beam exposure) mask is used to etch the Ru layer in an oxygen environment. Thereafter, the Ru (and the exposed HSQ on top) is used as a mask to etch the SiO_2 shadow walls. This etch is performed using a CHF_3/CF_4 recipe. This etch produces near vertical sidewalls and results in high aspect ratio shadow walls with very narrow fingers. The etch is observed in real time using a

Intellimetrics Laser End point detector and the etch rate drops sharply when the AlO_x layer unde the SiO_2 layer starts etching, at which point the etch is stopped. Once the shadow walls are fully etched, the remaining Ru mask is etched off using an oxygen ICP and thereafter the AlO_x layer is wet etched in AZ300MIF. A significant overtech (30-40%) is required to ensure that the AlO_x is removed from the narrow trenches. This completes the fabrication of the shadow wall templates. Before loading into the CBE chamber three cycles of digital etch (UV Ozone oxidation of exposed InP inside the trenches followed by wet etch in dilute HCl) is performed. This was found to improve nanowire growths inside the nanowire trenches.

The nanowires grown for these experiments are InAs/InP (buffer)/InP (substrate). The InP buffer growth separates the interface of the substrate from the actual transport channel. Residues and damages at that interface therefore have less effect on the actual tranpsort characteristics of the device. The growth of both the InP buffer and the InAs channel were

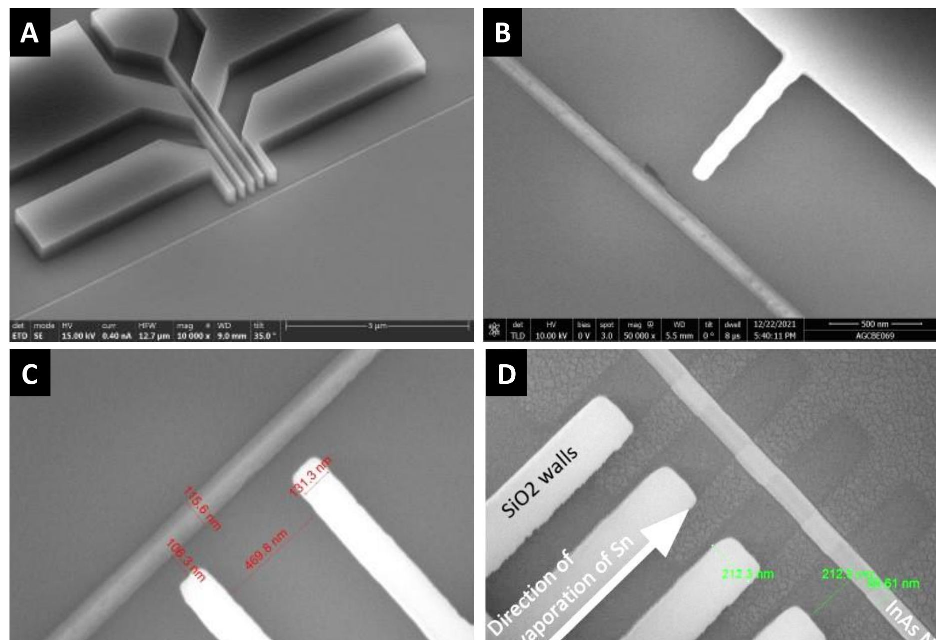

Figure 5.28 : Shadow wall templates with SAG InAs nanowires and shadowed deposition of tin. (A-D) shows various geometries and tin shadows.

performed at 520°C (calibrated using the appearance of the (2x4) reconstruction of InP). For the InP growth, TMI (0.5 torr) and PH_3 (18 torr) were used and growth time was 8 minutes. For InAs growth TMI (0.5 torr) and AsH_3 (12 torr) were used and growth time was 3 minutes. Before initiating the buffer layer growth 3 minutes were spent at 520°C under PH_3 overpressure. A 3 minute anneal under PH_3 was performed after the growth of the buffer layer to smoothen the surface. A 10" As flush was performed while switching the group-V precursors before turning on the TMI for the InAs growth. Following the growth of the nanowires, the samples were transferred into the superconducting deposition stage. The sample was kept in contact with the liquid nitrogen cooled cold stage for 1 hour for the temperature of the sample to equilibriate. Tin was deposited at a growth rate of 2A°/s from an effusion cell maintained at a thermocouple temperature of 1100 °C. After the deposition of the tin the sample was quickly transferred in-situ to the dielectric deposition chamber and 3nm of electron beam evaporated AlOx was deposited with sample rotation covering it uniformly. This AlOx layer prevents the superconductor from oxidising.

The sample was inspected using scanning electron microscopy to ensure the yield of the nanowires and the superconductor deposition. Device fabrication is subsequently performed using EBL and the tin in areas farther away from the naowire are etched using a 1:50 dilute HCl etch. Therafter contacts using normal metals (Ti/Au) are put down using standard liftoff techniques.

Preliminary cryogenic transport measurements with a superconductor-normal-superconductor 2 terminal device reveal the presence of super-current in the InAs nanowires that is tunable with an inplane magnetic field. A side gate also can tune the superconducting gap but cannot completely pinch off the device due to gate leakage issues.

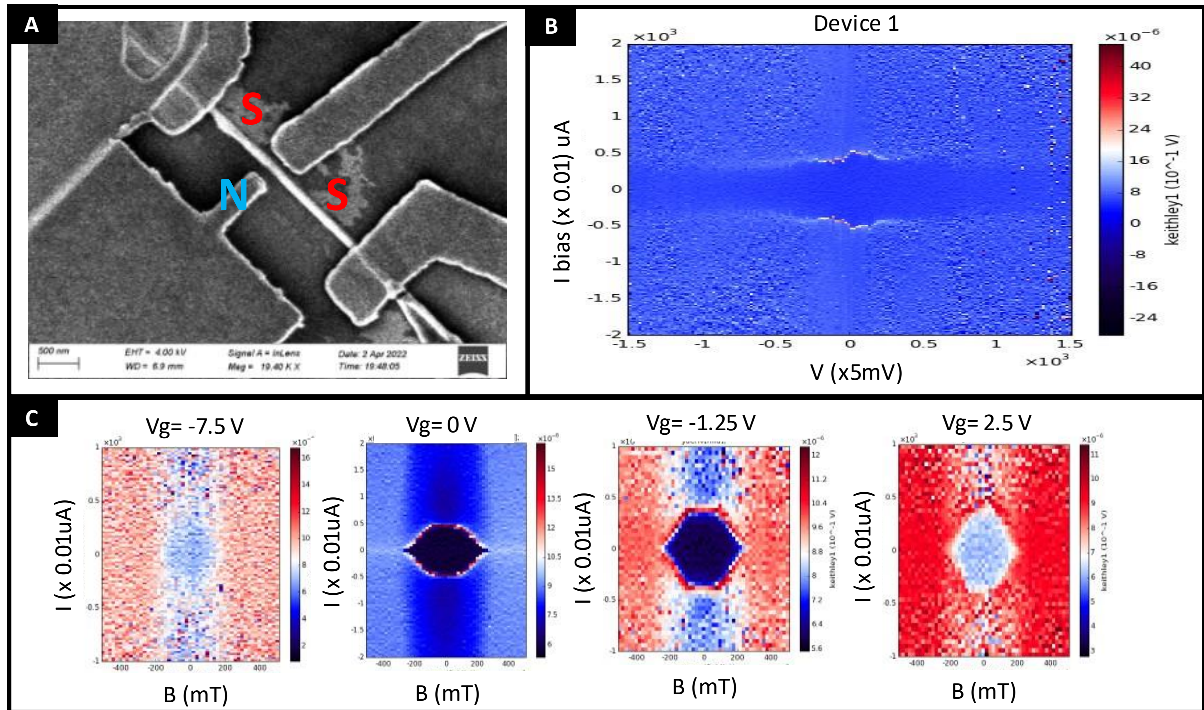

Figure 5.29 : (A) Fabricated SNS device with shadow wall sample (B) I-V curve demonstrating supercurrent (C) tuning of supercurrent with magnetic field at different side gate voltages (Vg).

Summary:

Shadow-wall SAG nanowire templates can provide a scalable platform to fabricate nanowires of arbitrary materials and deposit superconductors at predefined positions on the wire while maintaining a pristine superconductor-semiconductor interface. This can enable a number of cryogenic transport experiments without any limitations in the choice of

superconductors, nanowire materials, choice of substrates to grow on and the length of the shadow desired (that can be tuned easily by the height of the shadow wall). In this work, the fabrication of the template geometry exhibiting high aspect ratio shadowing structures, growth of nanowires as well as characterization using low-temperature transport measurements is established successfully. Future directions will involve experimenting with novel device geometries and newer materials (ferromagnets/ superconductors/ channel semiconductors).

References:

[1] E. Majorana, "Teoria simmetrica dell'elettrone e del positrone," *Il Nuovo Cimento (1924-1942) 1937 14:4*, vol. 14, no. 4, pp. 171–184, Sep. 2008, doi: 10.1007/BF02961314.

[2] J. Alicea, Y. Oreg, G. Refael, F. von Oppen, and M. P. A. Fisher, "Non-Abelian statistics and topological quantum information processing in 1D wire networks," *Nature Phys.*, vol. 7, no. 5, pp. 412–417, 2011, doi: 10.1038/nphys1915.

[3] J. D. Sau, D. J. Clarke, and S. Tewari, "Controlling non-Abelian statistics of Majorana fermions in semiconductor nanowires," *Phys. Rev. B*, vol. 84, no. 9, p. 094505, Sep. 2011, doi: 10.1103/physrevb.84.094505.

[4] A. Y. Kitaev, "Fault-tolerant quantum computation by anyons," *Ann. Phys.*, vol. 303, no. 1, pp. 2–30, 2003, doi: 10.1016/s0003-4916(02)00018-0.

[5] M. Sato and S. Fujimoto, "Majorana Fermions and Topology in Superconductors," 2016, doi: 10.7566/JPSJ.85.072001.

[6] A. Y. Kitaev, "Unpaired Majorana fermions in quantum wires," *Physics-Uspekhi*, vol. 44, no. 10S, p. 131, Oct. 2001, doi: 10.1070/1063-7869/44/10S/S29.

[7] R. M. Lutchyn, J. D. Sau, and S. das Sarma, "Majorana fermions and a topological phase transition in semiconductor-superconductor heterostructures," *Physical Review Letters*, vol. 105, no. 7, p. 077001, Aug. 2010, doi: 10.1103/physrevlett.105.077001/figures/3/medium.

[8] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, "Signatures of majorana fermions in hybrid superconductor-semiconductor nanowire devices," *Science (1979)*, vol. 336, no. 6084, pp. 1003–1007, 2012, doi: 10.1126/science.1222360.

[9] A. Das, Y. Ronen, Y. Most, Y. Oreg, M. Heiblum, and H. Shtrikman, "Zero-bias peaks and splitting in an Al–InAs nanowire topological superconductor as a signature of Majorana fermions," *Nature Physics 2012 8:12*, vol. 8, no. 12, pp. 887–895, Nov. 2012, doi: 10.1038/nphys2479.

[10] J. Chen *et al.*, "Ubiquitous non-Majorana zero-bias conductance peaks in nanowire devices," *Physical Review Letters*, vol. 123, no. 10, p. 107703, Sep. 2019, doi: 10.1103/PHYSREVLETT.123.107703/FIGURES/4/MEDIUM.

[11] J. Jung *et al.*, "Universal Platform for Scalable Semiconductor-Superconductor Nanowire Networks," *Advanced Functional Materials*, vol. 31, no. 38, p. 2103062, Sep. 2021, doi: 10.1002/ADFM.202103062.

[12] P. Aseev *et al.*, "Ballistic InSb Nanowires and Networks via Metal-Sown Selective Area Growth," *Nano Letters*, vol. 19, no. 12, pp. 9102–9111, Dec. 2019, doi: 10.1021/ACS.NANOLETT.9B04265/SUPPL_FILE/NL9B04265_SI_001.PDF.

[13] R. L. M. Op het Veld *et al.*, "In-plane selective area InSb–Al nanowire quantum networks," *Communications Physics 2020 3:1*, vol. 3, no. 1, pp. 1–7, Mar. 2020, doi: 10.1038/s42005-020-0324-4.

[14] P. Aseev *et al.*, "Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks," *Nano Letters*, p. acs.nanolett.8b03733, 2018, doi: 10.1021/acs.nanolett.8b03733.

[15] S. Mauthe *et al.*, "High-speed III-V nanowire photodetector monolithically integrated on Si," *Nature Communications 2020 11:1*, vol. 11, no. 1, pp. 1–7, Sep. 2020, doi: 10.1038/s41467-020-18374-z.

[16] Z. Wang *et al.*, “Room-temperature InP distributed feedback laser array directly grown on silicon,” *Nature Photonics 2015 9:12*, vol. 9, no. 12, pp. 837–842, Oct. 2015, doi: 10.1038/nphoton.2015.199.

[17] Y. Y. Hhh *et al.*, “Bufferless 1.5 µm III-V lasers grown on Si-photonics 220 nm silicon-on-insulator platforms,” *Optica, Vol. 7, Issue 2, pp. 148-153*, vol. 7, no. 2, pp. 148–153, Feb. 2020, doi: 10.1364/OPTICA.381745.

[18] K. Tomioka and T. Fukui, “Recent progress in integration of III–V nanowire transistors on Si substrate by selective-area growth,” *Journal of Physics D: Applied Physics*, vol. 47, no. 39, p. 394001, Sep. 2014, doi: 10.1088/0022-3727/47/39/394001.

[19] N. Gogneau *et al.*, “One-step nano-selective area growth (nano-SAG) of localized InAs/InP quantum dots: First step towards single-photon source applications,” *Journal of Crystal Growth*, vol. 310, no. 15, pp. 3413–3415, Jul. 2008, doi: 10.1016/J.JCRYSGRO.2008.04.019.

[20] F. Krizek, “Semiconductor Nanowire Networks Grown By Molecular Beam Epitaxy Vapor-Liquid-Solid,” *Phd. Thesis*, 2018.

[21] von Dipl-Phys Oliver Bierwagen, C. Markschies, C. Limberg Gutachter, W. T. Masselink, R. Fornari, and G. J. Salamo, “Growth and anisotropic transport properties of self-assembled InAs nanostructures in InP”.

[22] Q. Hang *et al.*, “Role of molecular surface passivation in electrical transport properties of InAs nanowires,” *Nano Letters*, vol. 8, no. 1, pp. 49–55, Jan. 2008, doi: 10.1021/NL071888T/ASSET/IMAGES/MEDIUM/NL071888TN00001.GIF.

[23] S. A. Studenikin, G. Granger, A. Kam, A. S. Sachrajda, Z. R. Wasilewski, and P. J. Poole, “Nonlinear magnetotransport phenomena in high-mobility two-dimensional electrons

in InGaAs/InP and GaAs/AlGaAs," *Physical Review B - Condensed Matter and Materials Physics*, vol. 86, no. 11, p. 115309, Sep. 2012, doi: 10.1103/PHYSREVB.86.115309/FIGURES/8/MEDIUM.

[24] I. v. Kulkova, S. Kadkhodazadeh, N. Kuznetsova, A. Huck, E. S. Semenova, and K. Yvind, "High-quality MOVPE butt-joint integration of InP/AlGaInAs/InGaAsP-based all-active optical components," *Journal of Crystal Growth*, vol. 402, pp. 243–248, 2014, doi: 10.1016/J.JCRYSGRO.2014.06.026.

[25] D. J. Carrad *et al.*, "Shadow Epitaxy for In Situ Growth of Generic Semiconductor/Superconductor Hybrids," *Advanced Materials*, vol. 32, no. 23, p. 1908411, Jun. 2020, doi: 10.1002/ADMA.201908411.

[26] S. Heedt *et al.*, "Shadow-wall lithography of ballistic superconductor–semiconductor quantum devices," *Nature Communications 2021 12:1*, vol. 12, no. 1, pp. 1–9, Aug. 2021, doi: 10.1038/s41467-021-25100-w.

[27] Y. Jiang *et al.*, "Selective area epitaxy of PbTe-Pb hybrid nanowires on a lattice-matched substrate," *Physical Review Materials*, vol. 6, no. 3, p. 034205, Mar. 2022, doi: 10.1103/PHYSREVMATERIALS.6.034205/FIGURES/4/MEDIUM.

[28] J. Jung *et al.*, "Universal Platform for Scalable Semiconductor-Superconductor Nanowire Networks," *Advanced Functional Materials*, vol. 31, no. 38, p. 2103062, Sep. 2021, doi: 10.1002/ADFM.202103062.

VII. Silicon fin based Merged Element Transmon

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ii. Circuit QED

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VII A. Introduction

When we look at the current challenges in computing, the most important problems are of course in scaling and reducing power consumption while maintaining or improving performance - as discussed in depth in the previous chapters. However, there exists a class of computational problems which cannot be calculated either efficiently (polynomial time) or at all by even the most powerful supercomputer in existence [1]. To this end, quantum computers can mitigate this issue potentially resulting in a tremendous impact for computing, hardware security, communication as well as computationally intensive combinatorial problems such as protein folding [2]. As a result, the construction of efficient qubits and the control and readout of individual quantum systems is the topic of intense research in scientific communities as well

as industries. This chapter focuses on the use of nanostructures to improve the scalability and coherence times of a transmon qubit. Unlike previous chapters, here we use a top-down technique to fabricate the quantum device. While this introduces some challenges when dealing with the extreme aspect ratio nanostructures, the top-down technique simultaneously has some clear advantages that make it suitable for fabricating such devices. These are described in the following sections. Before that a brief introduction to quantum computing is provided along with a brief summary of the different qubit architectures relevant to this work.

VII B. A brief introduction to quantum computing

A quantum bit (qubit) is the quantum mechanical equivalent of a classical bit which is the basic unit of information. In a classical bit, information is stored as a 0 or 1. In contrast, a qubit can be in an arbitrary superposition state of two states. The state of a qubit can therefore be represented as a wavefunction $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where α and β are probabilities of finding the qubit in state $|0\rangle$ (ground state) or $|1\rangle$ (excited state), with the condition that $|\alpha|^2 + |\beta|^2 = 1$. The qubit state is usually visualized using a Bloch sphere representation[3]. The qubit eigenstate energies have a separation of $\hbar\omega$ where $\frac{\omega}{2\pi}$ is the qubit transition frequency. The design of qubits should follow DiVincenzo criteria. These state that to build a quantum computer one must have a scalable physical system with well characterized qubit, the ability to initialize the state of the qubits to a simple fiducial state, long relevant decoherence times, a "universal" set of quantum gates and

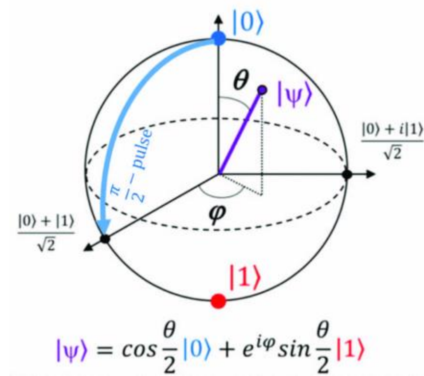

Figure 7.1 : The Bloch sphere provides an useful means to visualize the state of a single qubit and operations on it (reprinted from[3] with permission)

a qubit-specific measurement capability. Based on these criteria, several different physical qubits have been implemented including superconducting qubits, quantum dots, photonic systems, ultra-cold atoms, trapped ions, color centers in high bandgap materials and NMR systems. It is important to note the third criteria involves long decoherence times and will be a topic of focus in this work.

Qubit coherence is a strictly non-classical property that exists between two quantum states, when there is a definite phase relationship between them. Loss of it (i.e. quantum decoherence) happens due to the qubit coupling to the environment and can occur through various pathways. Two special cases are "relaxation" and "dephasing". Relaxation times refer to how fast the qubit decays or "relaxes" from an excited state to a ground state. This relaxation is given by T_1 and arises from energy loss from the qubit into the environment. Dephasing given by T_2 means a loss of phase coherence. In this, the qubit state rotates about the Z-axis in the Bloch sphere picture. To perform a large number of qubit operations without losing coherence, increasing the T1 and T2 times of qubits is one of the main focus in the community.

Among the various qubit implementations, superconducting qubits have emerged as one of the top contenders for constructing a reliable gate-based quantum computer as have been demonstrated by several research groups. Superconducting qubits are fabricated from inductors capacitors and Josephson junctions. Using circuit Quantum electrodynamics (cQED) these simple circuit elements can create complicated qubit networks that are fully controllable. Superconducting qubits have various device architectures and among them a transmon is the most popular implementation. In the next sections a brief overview of the individual elements and qubit architectures is provided.

VII B (ii). Josephson junctions

Two superconductors placed on both sides of a thin insulating layer together form a Jospehson junction. The superconducting wavefunction decays through the insulating barrier and allows Cooper pairs to tunnel through the barrier. The current flowing through the junction is related to the phase difference $\Phi = \theta_1 - \theta_2$, (each superconductor wavefunction can be represented by a Ginzburg-Landau wavefunction $\Psi(r) = \rho(r)e^{i\theta(r)}$) between the two superconductors by the relation $I = I_C sin\Phi$, where I_C is the critical current. The time evolution of phase difference with an applied voltage is given by $\frac{d\,(\Delta\Phi)}{dt} = \frac{2eV}{\hbar}$. The energy stored in a JJ is given by $\int I_s V\, dt = \int I_s \left(\frac{\hbar}{2e}\right) d(\Delta\Phi) = const. - E_J \cos(\Delta\Phi)\,, where\ E_J = \frac{\hbar I_C}{2e}$. The charging energy (arising from the capacitance of the metal-insulator-metal junction) is given by $E_{CJ} = \frac{e^2}{2C_J}$. The product of the critical current and the normal state resistance can be expressed as $I_C R_n = \frac{\pi\Delta}{2e}\tanh\left(\frac{\Delta}{2k_B T}\right)$, *where* Δ is energy gap of superconductor at T=0K. The JJ thus exhibits a non-linearity, which can be used to make dissipation-less non-linear inductors for superconducting qubits.

VII B (iii). Circuit Quantum Electro dynamics

A macroscopic circuit can be described by a small number of input parameters. We define a magnetic flux variable Φ as $\Phi(t) = \int_{-\infty}^{t} V(\tau)d\tau$ as the time integral of the voltage V across a circuit element and charge Q as $Q(t) = \int_{-\infty}^{t} I(\tau)d\tau$ as the time integral of the current flowing through a circuit element. Considering a simple LC resonator, with parallel inductor and capacitors, using Kirchoff's law we can write the sum of currents at one of the nodes as

$$I_L + I_C = 0 = \frac{\Phi}{L}(current\ through\ inductor\ I_L) + \frac{dQ}{dt}(current\ through\ capacitor\ I_C)$$

$$\frac{\Phi}{L} + C\frac{d^2\Phi}{dt^2} = 0$$

The Lagrangian for this circuit is $\boldsymbol{L} = \frac{1}{2}LI^2 - \frac{Q^2}{2C} = \frac{1}{2}\frac{\Phi^2}{L} - C\frac{\dot{\Phi}^2}{2}$

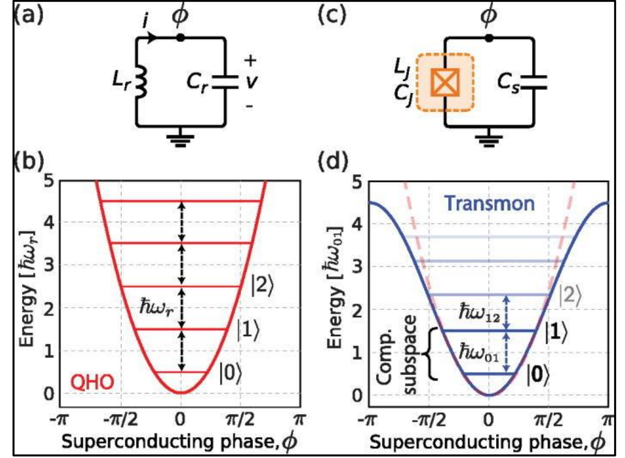

Figure 7.2 (a) Circuit for a parallel LC-oscillator. (b) Energy potential for the QHO (a), where energy levels are equidistantly spaced $\hbar\omega_r$ apart. (c) Josephson qubit circuit, with nonlinear inductance L_J (d) sinusoidal energy potential which yields non-equidistant energy levels.(reproduced from [4] with permission from AIP publishing)

The Hamiltonian for this is given by $H = \frac{1}{2C}Q^2 + \frac{1}{2L}\Phi^2$. Using the creation and annihilation operators $\hat{a}$ and $\hat{a}^\dagger$ with $[\hat{a}, \hat{a}^\dagger] = 1$, the Hamiltonian transforms to $H = \hbar\omega_r\left(\hat{a}^\dagger\hat{a} + \frac{1}{2}\right)$, where $\omega_r = \frac{1}{\sqrt{LC}}$. This is a quantum harmonic oscillator. However, since the energy spacings between consecutive energy states are equal, exciting from the ground state to the first excited state is uncontrolled since it leads to spurious excitements from n to (n+1) state. This is why the inductance of the circuit is replaced with a non-linear element i.e. a JJ making the energy spacings different and subsequently forming a qubit. The modified Hamiltonian is $H = 4E_C(n)^2 - E_J cos\phi$, where $E_C = \frac{e^2}{2C_{total}}$, $C_{total} = C_{self} + C_{shunt}$, and $n = \frac{Q}{2e}$ is the reduced charge. This makes the energy-phase relation non-parabolic and this forms the basis of a superconducting qubit.

VII C. Superconducting qubits

Superconducting qubits often dubbed as artificial atoms, have a number of different architectures contining capacitors and josephson junctions in various loops. Here we will

discuss three of the most relevant architectures, the Cooper pair box, the Transmon and the merged element transmon.

VII C.(i). Cooper pair box

A Cooper pair box contains a josephson junction with a small capacitance in parallel. The Hamiltonian of the system is given by

$$H = 4E_C\left(n - n_g\right)^2 - E_J cos\phi$$

Where n is the integer number of excel Cooper pairs across the JJ, n_g is the dimensionless offset charge between the islands, the charging energy $E_C = \frac{e^2}{2C}$ and E_J/E_C is typically of order unity. A gate electrode controls n_g. The charge dispersion $\frac{dE_m}{dn_g}$ for a CPB is large away from integer and half integer values of n_g making it susceptible to charge noise (as is the problem in the regime $\frac{E_J}{E_C} \leq 1$) . Coherence times of a CPB typically are less than $1\mu s$.

VII C.(ii). Transmon

A transmon is a CPB in the limit $\frac{E_J}{E_C} \gg 1$. To make the charging energy E_C small, the junction is shunted by a large capacitor, $C_S \gg C_J$. In the transmon regime the charge dispersion of the mth energy level is expressed as $\epsilon_m \cong E_C \frac{2^{4m+5}}{m!} \sqrt{\frac{2}{\pi}} \left(\frac{E_J}{2E_C}\right)^{\frac{m}{2}+\frac{3}{4}} e^{-\sqrt{\frac{8E_J}{E_C}}}$, which leads to an exponential suppression of charge noise as $\frac{E_J}{E_C}$ is increased. Qubit frequency is given by $\hbar\omega_{01} \cong \sqrt{\frac{E_J}{8E_C}} - E_C$ and is usually in the 3-6 GHz range. The superconducting phase Φ has a small spread and acts as a good quantum number. The second term of the Hamiltonian when expanded $E_J cos\phi = \frac{1}{2}E_J\phi^2 - \frac{1}{24}E_J\phi^4 + \Theta(\phi^6)$) contains a negative power of 4 term which effectively reduces the anharmonicity of the energy landscape and makes the qubit more

susceptible to noise. Therefore, a large $\frac{E_J}{E_C}$ is maintained that exponentially suppresses charge noise and only weakly changes anharmonicity making it a workable device [4].

VII D. Towards merged element transmons with Si fins

The invention of the transmon qubit has fueled the rapid development of quantum-information research over the past decade [5], and landmark breakthroughs have been achieved with this technology[6] . Modern transmons are typically based on some variant of a small, thermally oxidized $Al/AlO_x/Al$ tunnel junction in parallel with a large shunt capacitor. A variety of methods exist for defining the Josephson junctions (JJs) to obtain a nonlinear inductance, such as Dolan bridges [7], the Manhattan shadow evaporation process[8] and overlap designs[9], [10] .

However, these devices are difficult to scale for a couple of reasons. First, the associated shunt capacitors are typically defined as planar structures grown on a low-loss substrate. While very low-loss substrates (i.e., intrinsic, float-zone silicon (i-Si)) with loss tangent in the low 10^{-7} range can be obtained [11], it is well known that the interfaces and

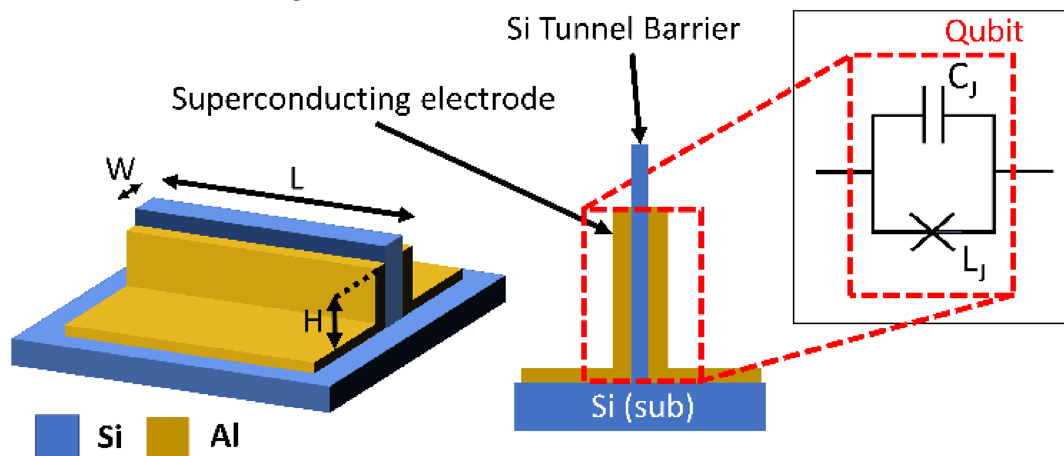

Figure 7.3 : 3D schematic of the FinMET and cross-section with corresponding circuit diagram of MET (inset) (reproduced from [34] with permission from AIP publishing)

surfaces of the shunt capacitor participate significantly in the total loss [12], [13]. In general, while it has been observed that increasing the size of the shunt capacitor can dilute the high loss contributions [14], this results in very large structures, with dimensions of the order of 100s of micrometers. This is problematic for scaling up to systems with many qubits and warrants capacitors with lower form factors. Second, the frequency allocations of transmons using thermally oxidized aluminum have a significant spread [15]. While there have been advances on this front using post-processing, i.e. laser-annealing of individual devices [16], this remains a significant obstacle to large-scale integration of transmons. To this end, better control of the tunnel-barrier thickness and interfaces in the fabrication process is desired.

Recently, an alternative approach to scaling these circuits was demonstrated [17], i.e. the merged-element transmon (MET). The MET minimizes the transmon qubit size and radiation while providing an avenue to potentially reduce losses due to surfaces and interfaces. This design entails engineering the junction itself to satisfy the transmon requirements for frequency, anharmonicity, and charge noise by merging the external shunt capacitor and the JJ inductance into a single element. This design is constructed from a superconductor–insulator-superconductor trilayer where the insulator is made from a dielectric material that has a low barrier height and may even be a semiconductor at room temperature. This design has several advantages over the traditional transmon. First, the MET allows a significant reduction, on the

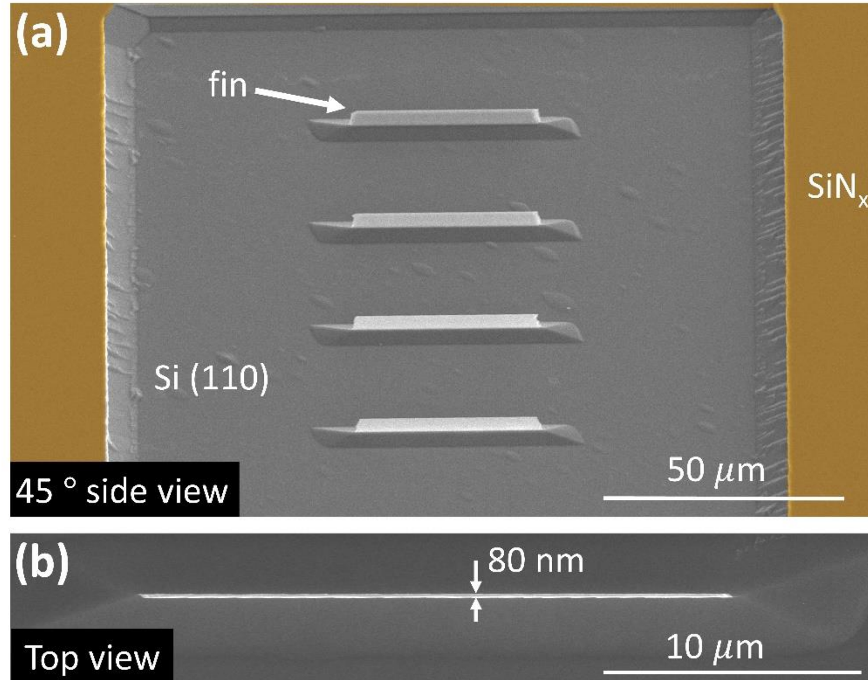

Figure 7.4 : Images of Si fins (a) 4 fins structures, 30 μm long x 2.3 μm tall and 80nm thick etched into a Si surface, including the trenched area around them (b) top view of a fin that is 30um long and 80nm thick(reproduced from [34] with permission from AIP publishing)

order of 10^4, in the device area [17]. Second, the resulting small qubit dimensions effectively suppress unwanted radiation and qubit-qubit coupling through direct interactions or box modes. Third, the MET frequency should be less susceptible to the variation in lithography because the associated capacitive and inductive contributions toward the qubit frequency cancel out to first order [5], [17]. Moreover, one may choose a low-barrier-height material as the junction tunnel barrier. This enables the use of a relatively thick tunnel barrier that may reduce the percentage variation in junction inductance, potentially alleviating the frequency allocation problem.

The energy-level transitions of a MET device, from two-tone spectroscopy measurements confirmed that the MET is indeed operating in the transmon qubit regime [17]. An in-depth

TLS-loss analysis identified the lossy amorphous silicon tunnel barrier and surrounding interfaces as the major limiting factor for the qubit relaxation time. Subsequently, Mamin *et.al.* (and the IBM team) demonstrated METs with coherences on up to 41 and 234 μs , using as-grown- and annealed-AlOx overlap junctions respectively [18].

While the MET demonstration from Ref [18]. confirmed the possibility of obtaining long coherence times in selected devices, the extreme oxidation and annealing conditions resulted in significant frequency spread for the devices. This is reminiscent of conventional transmons and is most likely due to several problems. First, the tunneling critical current varies exponentially with the tunnel barrier thickness, which is difficult to control in a 2 nm thick tunnel barrier formed by thermal oxidization. In addition, there are tunneling hotspots due to the barrier being structurally and chemically inhomogeneous, resulting in only a small percentage of the 2 nm thick AlO_x barrier actually contributing to the tunneling [19]. Second, the critical current can be affected by atomic-level defects in and around the barrier and wiring [20]. These can cause two-level-system spectral features that are detrimental to the operation of the devices. This illustrates the importance of developing a more robust method of defining the tunnel junction. Specifically, we note that a low barrier height, crystalline tunnel barrier can mitigate this problem because it can be thicker, making monolayer scale thickness variations less significant.

Here, first, we propose the concept of a FinMET device that can overcome a number of the problems discussed above. This process capitalizes on the fact that crystalline Si fins can be formed on the surface of a wafer using an anisotropic wet etch (Figure 7.1). These Si fins act as tunnel barriers for the MET. The fin walls can, in principle, be atomically flat, parallel, and engineered to be a very specific thickness. For amorphous-Si barriers, for example, the small

band gap compared to that of AlO_x results in a low tunnel-barrier height [17] . This allows the use of a relatively thick fin, on the order of 5-10 nm, leading to a natural extension of the MET to a more scalable geometry.

In addition to being used as a junction, the fin geometry also allows the fabrication of low-loss parallel plate silicon capacitors with a significant reduction in utilized area on chip. Such capacitors can be used in conjunction with conventional Josephson junctions to improve coherence times of conventional trasnmons.

In this work, as first steps towards realizing a FinMET device, we demonstrate both the fabrication of high aspect ratio Si fins and the self-aligned process to deposit superconductors on such fins. Subsequently, we pattern these Al-Si-Al fin capacitors into resonator circuits and perform microwave measurements at dilution fridge temperatures. The transport clearly demonstrates the presence of working fin capacitors and their integrability into traditional superconducting qubit fabrication processes. These scalable techniques are unique in that both capacitive elements and METs can be formed from the Si substrate resulting in reduction in both form-factor and losses leading to improved qubit scalability.

Fin fabrication and structural characterization

The fin-based devices will have parallel-plate electrodes that can be optically defined, fabricated with standard processing techniques, and capacitively coupled through the low-loss substrate in order to form cells for VLSI circuits. In this case, it is critical to have low loss,

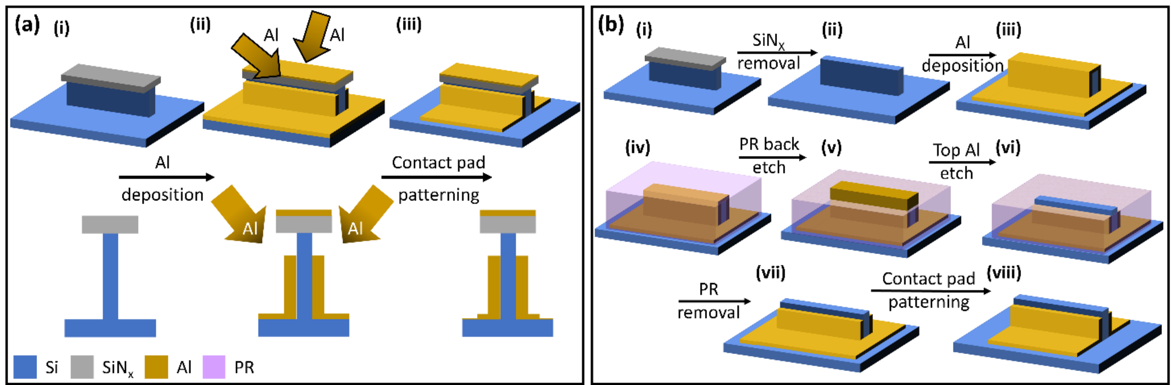

Figure 7.5 : Schematics of (a) self-aligned process and (b) planarization process with process A being followed in this work (reproduced from [34] with permission from AIP publishing)

epitaxial interfaces for the fin-metallization layer. This can be achieved using careful surface cleaning and growth methods, as shown by Place, et al. [21].

Fin fabrication : Based on the modeling from Ref [17], the optimal dimensions for the FinMET will require Si fin structures on the order of 5-10 nm thick with areas of approximately 10μm^2. Structures of such extreme aspect ratios are on the cutting edge of modern fin technologies [22].

The FinMET devices are comprised of a Si fin [22],[23] with superconducting electrodes grown on both the surfaces of the fin, effectively forming a horizontal superconductor-semiconductor-superconductor junction, as illustrated in Figure 7.3. The Si fin is formed by top-down etching of a commercial intrinsic Si substrate, which are commonly grown using float-zone technique and exhibit high resistance and low loss. To achieve atomically flat surfaces, we start with a Si(110) substrate and use anisotropic wet etching to fabricate Si fins with smooth (111) surfaces.

For the anisotropic wet etch, a SiNx hard mask is used. The SiNx layer is deposited using a low-pressure chemical vapor deposition technique which results in a high density, low stress nitride layer on top of the silicon substrate. This mask is lithographically defined using electron beam lithography (EBL) and plasma based dry etching. Alternatively, there exist methods based on SiNx deposited on step edges [24] that can form SiNx masks with similar dimensions using only photolithography.

Before the wet etch to define the fin, the sample is cleaned under a $C_4F_8/SF_6/CF_4$ Si etching chemistry in a plasma based dry etcher for 30 seconds to remove the top damaged layer from the previous dry etch for the SiN_x mask. This was found to considerably improve the cleanliness of the substrate and the uniformity of the wet etch. The wet etch is subsequently performed using potassium hydroxide (KOH) at 87°C. Figure 7.4 shows fin structures defined on a Si(110) substrate. Fin mask widths were varied from 100nm to 1um for test samples. The undercutting from the wet etch is considerable (~50-80nm). The thinnest fins that were reliably fabricated without much optimization of process parameters were approximately 80nm (with a length and height of 100um and 3um respectively).

Further thinning of the fins can then be achieved, if necessary, by timing an additional wet etch and/or subsequent atomic-layer-digital-etching (ALE). The ALE process is typically achieved by oxidizing the Si(111) surface using O_2 plasma at room temperature to form an oxide layer that is approximately 5-7nm thick. This oxide can then be etched away using HF and the process repeated to achieve the desired fin thickness. The second envisioned process to thin the fin involves using atomic layer etching with a O_2, HF, and $Al(CH_3)_3$ chemistry [25]. A final wet etch in KOH can then be used to regain the smooth Si(111) surface followed by a HF dip to remove any oxides, prior to Al metal deposition.

By using the intrinsically parallel crystallographic {111}-faces that are exposed by the anisotropic etch, the tunnel junction can be expected to have well-defined, homogeneous tunneling currents. In addition, the low-tunnel-barrier-height material can be much thicker than standard junction material and thus mass-fabricated with better margins.

Fin Metallization: Metallization of the fins can be accomplished by cleaning the exposed Si{111}-faces and then epitaxially growing a superconducting metal, such as Al. Prior to Al growth, a buffered HF etch followed by high temperature annealing of the Si fin is expected to result in a pristine interface, thus optimizing coherence. Additionally, since the bottom edge is surrounded by low-loss substrate a reduced participation of the Al-air exposed interface is expected.

Two different process flows can be followed, either self-aligned or planarized, as illustrated in Figure 7.5. Both processes start by etching Si fins as described previously, using a SiN_x hard mask and a combination of dry and wet etches.

The first process flow involves retention of the SiNx hard mask that was initially used to etch down the Si fins. Using the overhang in the SiNx on top of the fin, an angled deposition of aluminum can lead to a break in the metal layer at the top of the fin. This shadow-evaporation technique therefore enables direct creation of a fin capacitor using a self-aligned process. This eliminates the need to etch off Al from the top of the fin to electrically disconnect the pads on either side of the fin (Figure 7.5b). Contact pads can then be patterned using optical lithography.

The second possible process flow, planarization, (Figure 7.5b) involves removing the SiN_x hard mask and then depositing a layer of aluminum onto the fins. Back-etching of a subsequent

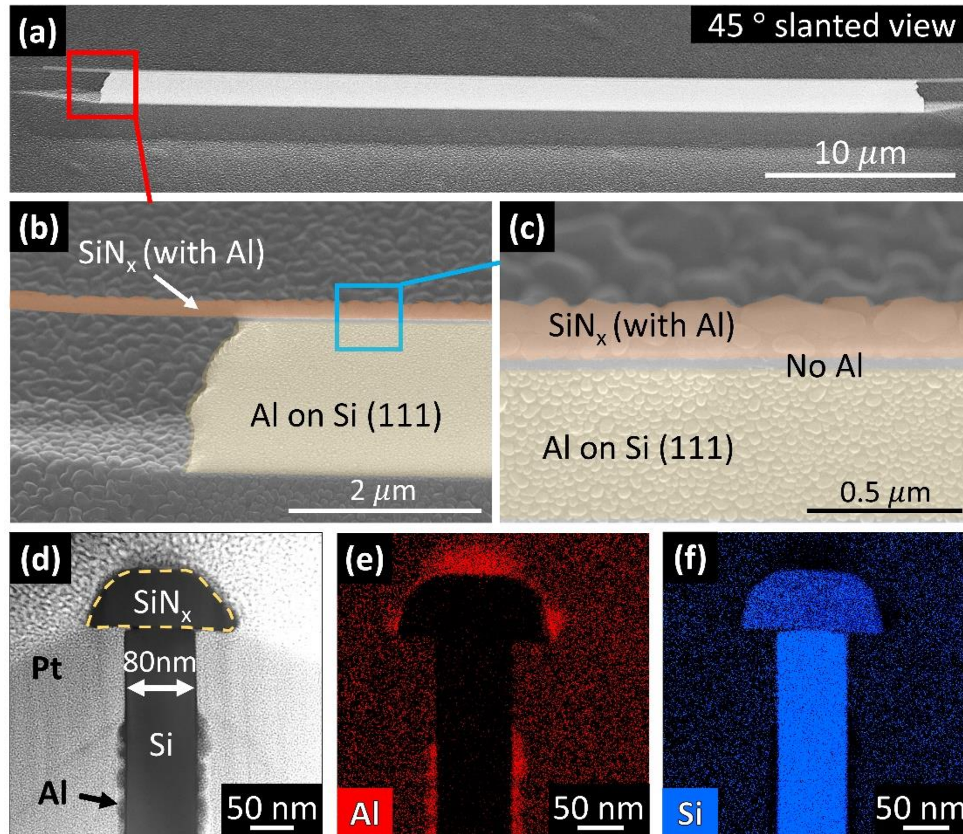

Figure 7.6: Metallized fin structure illustrating the self-aligned process and growth of Al on the Si{111} surfaces with a SiN_x hard mask. (a) side view of the fin, (b) shows zoomed in area of (a) with the SiNx hard mask on top of the fin, extending out to the left, (c) shows a zoomed in area of (b) with the area where the Al is shadowed.(d) High angle dark field scanning transmission electron microscopy image of a fin cross-section with SiN_x hard mask and shadow deposited Al. (e) and (f) shows energy-dispersive x-ray scans highlighting the Al and Si areas respectively (reproduced from [34] with permission from AIP publishing)

resist layer, either by dry etching or chemical mechanical polishing (CMP), can thereafter be used to expose the metal at the top of the fin and a wet or dry etch is used to remove the top aluminum. Contact pads would then be patterned in a way similar to the previous process flow. Figure 7.6 shows fin structures coated with Al, as described below.

In this work, we employed the first, self-aligned method. Fins were fabricated according the the above recipe and the Al was shadow deposited with an effusion cell in a molecular beam epitaxy chamber. The substrate temperature was maintained close to 0°C. Smoother Al films can be grown by performing the deposition in a cryogenic cold stage maintained at -196 °C following a process similar to Ref [26]–[29]. Connection to other parts of the circuit, for example superconducting resonators and wiring, can be accomplished using the Al pads on the sides of the fins using standard processing techniques.

Microwave measurements : Lumped element (LE) resonators were made using fin capacitors having widths greater than 200nm, meander inductors, and interdigitated capacitors (IDCs). These LE resonators were used to demonstrate feasibility of integration of fins in superconducting circuits and to characterize fabricated fins in the capacitive regime. The concept of the LE design is depicted in Figure 7.7. The design consists of eight LE resonators inductively coupled to a single 50 Ohm coplanar waveguide feedline in a standard ‘hanger’ arrangement [30].

To characterize the fin capacitors and minimize uncertainties due to capacitance of metallized leads, fins are incrementally added between the fingers of the IDC as shown in Figure 7.7. The meander inductor and other IDC parameters are kept the same while the number of fins in each LE resonator is varied. In this way, the resonant frequencies of the LE resonators are separated, and capacitance of the fins may be determined experimentally.

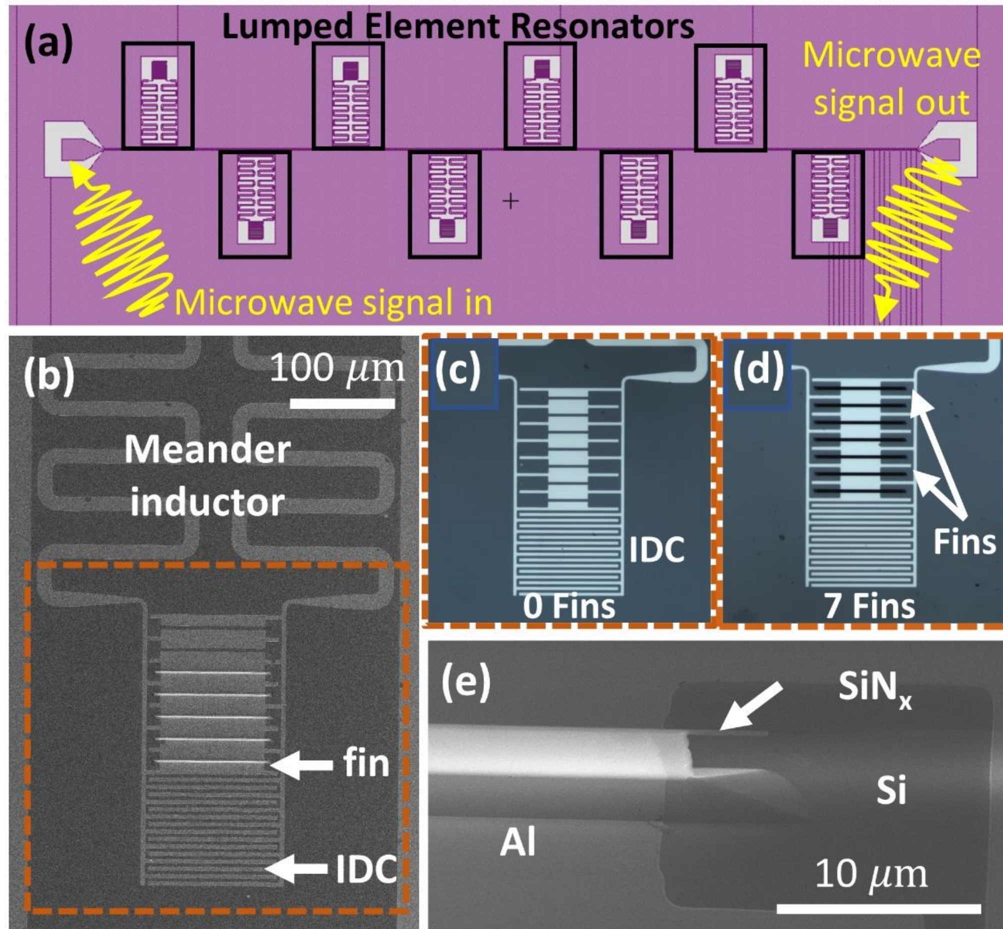

Figure 7.7: (a) Mask layout for frequency multiplexed lumped element resonator design. (b) SEM illustrating how fins are incorporated into the interdigitated capacitor (IDC) with a meander inductor. (c-d) Optical micrographs of resonators with zero and 7 fins . (e) shows aluminum patterned around 100 µm long fins(reproduced from **[34]** with permission from AIP publishing)

3μm tall fins having lengths of 120um and patterned widths of 300nm and 400nm were fabricated on a 50.8mm diameter Si(110) wafer using the process outlined in this work. The fin capacitor height and width are set during fin formation while the fin capacitor length is lithographically defined in the metallization (superconductor) layer using optical lithography.

Following fin formation, the wafer was etched in 6:1 BHF for 2 minutes to remove surface oxide and immediately loaded into high vacuum for Al deposition. 30nm of Al was deposited using e-beam evaporation on each side of the fins using deposition angles of +/-25^0 to obtain a uniform Al coating on each side of the fins with a self-aligned break in the Al near the top of the fin due to the overhang of the silicon nitride mask. Following Al deposition, the test resonator circuits were defined using direct-write photolithography and wet etching. The wafer was diced into 7.5mm x 9.5mm die which were then packaged and cooled to 35mK for microwave measurements in a dilution refrigerator.

Figure 7.8 (a) shows resonant frequency dependance on the number of fins included between the IDC fingers in each LE resonator. Three different dies were measured where each die incorporates nominally identical fins and where the fin dimensions are varied between dies. Figure 7.8(b) shows C_n/C_0 plotted vs number of fins incorporated in the IDCs for each of the three dies measured. Here C_n is the capacitance of a LE resonator with n fins, and C_0 is the capacitance of the LE resonator with no fins. The linear trend in the data shown in Figure 7.8 (b) is consistent with the expectation that each fin adds a set capacitance to the resonator, with the interpolated slope equal to $\Delta C/C_0$, where ΔC is the added capacitance from a single fin and C_0 is the capacitance of the LE resonator without any fins added.

We also simulated the capacitor part of the LE resonator with COMSOL® Electrostatics [31]. In these simulations, fin dimensions were chosen based on SEM micrographs. The simulation results were found to be in good agreement with experiment and are included in Figure 7.8 (b). The fin dimensions found to result in the best fit are indicated in Fig.7.8. For these fits, the fin capacitor length was kept constant at 100 μm (or 50 μm) , the fin height was kept constant at 3.55 μm and the thickness was extracted from least square fitting (319 nm for

nominally 400nm thick fin and 219nm for nominally 300 nm thick fin). For these dimensions, the fin capacitance per unit length along the fin was found to be ~1.3 fF/µm for 319 nm wide fin and 1.8 fF/µm for the 219 nm wide fins. These values are in close agreement with the estimates obtained from a parallel plate geometry. In addition, the single-photon internal quality factors of one- and six-fins combined with the IDCs as shown in Figure 7.7 are determined to be 8.4 x 10^4 and 1.8 x 10^5 respectively. Following Ref.[32] and based on simulations of capacitance of the combined IDC-fin capacitors, we estimate the single-fin loss to be on the order of ~3 x 10^{-7}. This is a promising demonstration of Si fins as an improvement over traditional thin-film capacitors and its potential development into FinMETs .

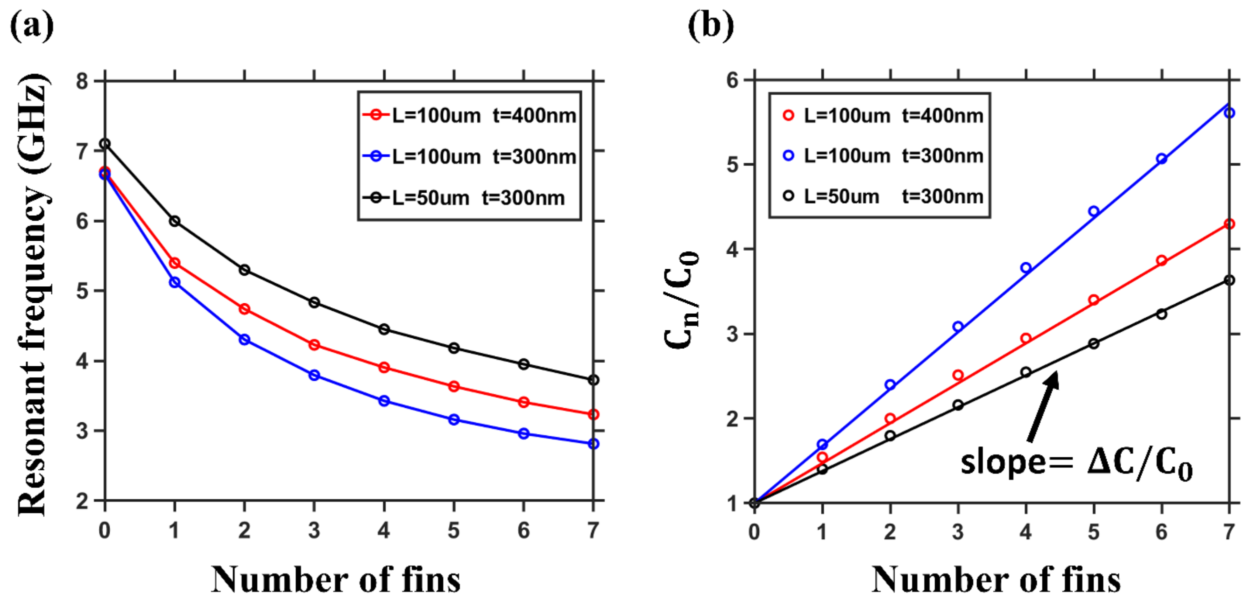

Figure 7.8: (a) Measured resonant frequency vs the number of fins in each interdigitated capacitor. (b) Capacitance ratio vs the number of fins (circles) along with fits (straight lines) from COMSOL simulations. Fits in (b) are for 219 and 319 nm thicknesses for nominally 300 and 400 nm thick fins, respectively(reproduced from [34] with permission from AIP publishing)

VII E. Discussion and Summary :

The use of amorphous-AlOx Josephson junctions for quantum computing transmon applications is challenged by frequency allocation, frequency stability, spurious two-level states (TLS) and loss issues. In addition, the large size of shunt capacitors required to dilute the TLS losses at surfaces and interfaces severely limits the scalability.

In order to transition to a robust and more scalable technology, a significant effort on the front-end is required in order to bootstrap a completely new junction fabrication process and device design. To this end, we have proposed and demonstrated one of the necessary elements of a new FinMET technology. These include the fin structures needed to develop a more scalable system and reduce footprint. Although the fin thicknesses used in this work are not low enough to demonstrate tunneling, working low-loss fin capacitors integrated with superconductor resonator circuitry have been demonstrated and characterized. Next steps include integration of these capacitors with tunnel junctions to form qubits with reduced footprint and demonstration of tunnel junctions in the fins to form the proposed FinMET device.

To achieve tunneling through the silicon fins the fin thicknesses need to be approximately 5-10 nm. Structures of such extreme aspect ratios are on the cutting edge of modern fin technologies [22]. Thinning of the fins can then be achieved, by timing an additional wet etch and/or subsequent digital etching. The digital etching process is typically achieved by oxidizing the Si(111) surface using O_2 plasma at room temperature to form an oxide layer that is approximately 5-7nm thick. This oxide can then be etched away using HF and the process

repeated to achieve the desired fin thickness. The second envisioned process to thin the fin involves using atomic layer etching (ALE) with a O_2, HF, and $Al(CH_3)_3$ chemistry [25]. A final wet etch in KOH can then be used to regain the smooth Si(111) surface followed by a HF dip to remove any oxides, prior to Al metal deposition.

The entire process can be also performed using photolithography by using SiNx deposited on step edges[24] that can form SiNx masks with similar dimensions. This can result in a more reliable wafer-scale fabrication of fin-based qubit devices.

To deposit the side superconductors, in addition to the process demonstrated, the second proposed process flow uses planarization (Fig. 7.5 (b)). This involves removing the SiN_x hard mask and then depositing a layer of aluminum onto the fins. Back-etching of a subsequent resist layer, either by dry etching or chemical mechanical polishing (CMP), can thereafter be used to expose the metal at the top of the fin and a wet or dry etch is used to remove the top aluminum. Contact pads would then be patterned in a way similar to the previous process flow.

While this is feasible to demonstrate at the small scale, the importance of these developments is that it should be possible to scale up significantly by decreasing the yield variation and material defects, based on existing Si-fin infrastructure and expertise in the field.

In conclusion, in this work, we first propose and outline a new geometry to define Si fin based self-aligned superconductor/Si/superconductor trilayer structures to form fin merged element transmons (FinMETs). Following this, we successfully fabricate, and measure low-loss resonators consisting of Al/Si/Al fin capacitors. This also establishes the compatibility of this technology with conventional qubit or novel [33] qubit fabrication platforms. Further thinning of the Si barrier layer will enable the subsequent realization of FinMET devices.

References:

[1] M. A. Beck, "HYBRID SUPERCONDUCTING QUANTUM COMPUTING ARCHITECTURES," 2018.

[2] A. Robert, P. K. Barkoutsos, S. Woerner, and I. Tavernelli, "Resource-efficient quantum algorithm for protein folding," *npj Quantum Information 2021 7:1*, vol. 7, no. 1, pp. 1–5, Feb. 2021, doi: 10.1038/s41534-021-00368-4.

[3] F. Jazaeri, A. Beckers, A. Tajalli, and J. M. Sallese, "A Review on quantum computing: From qubits to front-end electronics and cryogenic mosfet physics," *Proceedings of the 26th International Conference "Mixed Design of Integrated Circuits and Systems", MIXDES 2019*, pp. 15–25, Jun. 2019, doi: 10.23919/MIXDES.2019.8787164.

[4] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "A quantum engineer's guide to superconducting qubits," *Applied Physics Reviews*, vol. 6, no. 2, p. 021318, Jun. 2019, doi: 10.1063/1.5089550.

[5] J. Koch *et al.*, "Charge-insensitive qubit design derived from the Cooper pair box," *Physical Review A - Atomic, Molecular, and Optical Physics*, vol. 76, no. 4, 2007, doi: 10.1103/PhysRevA.76.042319.

[6] F. Arute *et al.*, "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, no. 7779, pp. 505–510, Oct. 2019, doi: 10.1038/s41586-019-1666-5.

[7] G. J. Dolan, "Offset masks for lift-off photoprocessing," *Applied Physics Letters*, vol. 31, no. 5, 1977, doi: 10.1063/1.89690.

[8] M. v. Costache, G. Bridoux, I. Neumann, and S. O. Valenzuela, "Lateral metallic devices made by a multiangle shadow evaporation technique," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 30, no. 4, 2012, doi: 10.1116/1.4722982.

[9] X. Wu, J. L. Long, H. S. Ku, R. E. Lake, M. Bal, and D. P. Pappas, "Overlap junctions for high coherence superconducting qubits," *Applied Physics Letters*, vol. 111, no. 3, 2017, doi: 10.1063/1.4993937.

[10] A. Stehli *et al.*, "Coherent superconducting qubits from a subtractive junction fabrication process," *Applied Physics Letters*, vol. 117, no. 12, 2020, doi: 10.1063/5.0023533.

[11] W. Woods *et al.*, "Determining Interface Dielectric Losses in Superconducting Coplanar-Waveguide Resonators," *Physical Review Applied*, vol. 12, no. 1, 2019, doi: 10.1103/PhysRevApplied.12.014012.

[12] D. S. Wisbey *et al.*, "Effect of metal/substrate interfaces on radio-frequency loss in superconducting coplanar waveguides," *Journal of Applied Physics*, vol. 108, no. 9, 2010, doi: 10.1063/1.3499608.

[13] G. Calusine *et al.*, "Analysis and mitigation of interface losses in trenched superconducting coplanar waveguide resonators," *Applied Physics Letters*, vol. 112, no. 6, 2018, doi: 10.1063/1.5006888.

[14] J. M. Gambetta *et al.*, "Investigating surface loss effects in superconducting transmon qubits," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 1, 2017, doi: 10.1109/TASC.2016.2629670.

[15] J. M. Kreikebaum, K. P. O'Brien, A. Morvan, and I. Siddiqi, "Improving wafer-scale Josephson junction resistance variation in superconducting quantum coherent circuits," *Superconductor Science and Technology*, vol. 33, no. 6, 2020, doi: 10.1088/1361-6668/ab8617.

[16] J. B. Hertzberg *et al.*, "Laser-annealing Josephson junctions for yielding scaled-up superconducting quantum processors," *npj Quantum Information*, vol. 7, no. 1, 2021, doi: 10.1038/s41534-021-00464-5.

[17] R. Zhao *et al.*, "Merged-Element Transmon," *Physical Review Applied*, vol. 14, no. 6, 2020, doi: 10.1103/PhysRevApplied.14.064006.

[18] H. J. Mamin *et al.*, "Merged-Element Transmons: Design and Qubit Performance," *Physical Review Applied*, vol. 16, no. 2, 2021, doi: 10.1103/PhysRevApplied.16.024023.

[19] L. J. Zeng *et al.*, "Direct observation of the thickness distribution of ultra thin AlOx barriers in Al/AlOx/Al Josephson junctions," *Journal of Physics D: Applied Physics*, vol. 48, no. 39, 2015, doi: 10.1088/0022-3727/48/39/395308.

[20] S. Schlör *et al.*, "Correlating Decoherence in Transmon Qubits: Low Frequency Noise by Single Fluctuators," *Physical Review Letters*, vol. 123, no. 19, 2019, doi: 10.1103/PhysRevLett.123.190502.

[21] A. P. M. Place *et al.*, "New material platform for superconducting transmon qubits with coherence times exceeding 0.3 milliseconds," *Nature Communications*, vol. 12, no. 1, 2021, doi: 10.1038/s41467-021-22030-5.

[22] M. L. Chen *et al.*, "A FinFET with one atomic layer channel," *Nature Communications*, vol. 11, no. 1, 2020, doi: 10.1038/s41467-020-15096-0.

[23] P. S. Finnegan, A. E. Hollowell, C. L. Arrington, and A. L. Dagel, “High aspect ratio anisotropic silicon etching for x-ray phase contrast imaging grating fabrication,” *Materials Science in Semiconductor Processing*, vol. 92, 2019, doi: 10.1016/j.mssp.2018.06.013.

[24] V. Jovanovic, T. Suligoj, and L. Nanver, “Crystallographic Silicon-Etching for Ultra-High Aspect-Ratio FinFET,” *ECS Transactions*, vol. 13, no. 1, 2008, doi: 10.1149/1.2911512.

[25] A. I. Abdulagatov and S. M. George, “Thermal Atomic Layer Etching of Silicon Using O2, HF, and Al(CH3)3 as the Reactants,” *Chemistry of Materials*, vol. 30, no. 23, 2018, doi: 10.1021/acs.chemmater.8b02745.

[26] R. W. Simmonds *et al.*, “Josephson junction materials research using phase qubits,” in *Quantum Computing in Solid State Systems*, 2006. doi: 10.1007/0-387-31143-2_11.

[27] B. M. McSkimming, A. Alexander, M. H. Samuels, B. Arey, I. Arslan, and C. J. K. Richardson, “Metamorphic growth of relaxed single crystalline aluminum on silicon (111),” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 35, no. 2, 2017, doi: 10.1116/1.4971200.

[28] L. Aballe, C. Rogero, P. Kratzer, S. Gokhale, and K. Horn, “Probing interface electronic structure with overlayer quantum-well resonances: Al/Si(111),” *Physical Review Letters*, vol. 87, no. 15, 2001, doi: 10.1103/PhysRevLett.87.156801.

[29] H. Liu, Y. F. Zhang, D. Y. Wang, M. H. Pan, J. F. Jia, and Q. K. Xue, “Two-dimensional growth of Al films on Si(1 1 1)-7 × 7 at low-temperature,” *Surface Science*, vol. 571, no. 1–3, 2004, doi: 10.1016/j.susc.2004.08.011.

[30] C. R. H. McRae *et al.*, “Materials loss measurements using superconducting microwave resonators,” *Rev. Sci. Instrum. 91, 091101*, 2020, doi: 10.1063/5.0017378.

[31] “COMSOL Multiphysics® v. 6.0. www.comsol.com. COMSOL AB, Stockholm, Sweden”.

[32] C. R. H. McRae *et al.*, “Dielectric loss extraction for superconducting microwave resonators,” *Applied Physics Letters*, vol. 116, no. 19, May 2020, doi: 10.1063/5.0004622.

[33] A. Gyenis *et al.*, “Experimental Realization of a Protected Superconducting Circuit Derived from the 0 - π Qubit,” *PRX Quantum*, vol. 2, no. 1, p. 010339, Jan. 2021, doi: 10.1103/PRXQUANTUM.2.010339/FIGURES/16/MEDIUM.

[34] A.Goswami et.al. “Towards merged-element transmons using silicon fins: The FinMET”

Appl. Phys. Lett. 121, 064001 (2022)

VIII. Summary and Future Directions

Semiconductor nanostructures constitute an important path forward to fabricate the next generation of electronic, optical and quantum devices. For example, the high aspect ratios of such nanostructures can enable scaling, high-density packing and improved electrostatic control of electronic transistors, resulting in smaller and more power-efficient devices [1]–[5]. The optical and electronic confinement in these nanostructures can also be harnessed for efficient light trapping, compact light sources and detectors for integrated photonic devices[6]–[8] . Finally, semiconductor nanostructures exhibit one-dimensional electron transport [9]–[11], and can form quantum light sources [12] - thus finding wide applications in building quantum nano-electronic devices.

The wide-scale potential applications of semiconductor nanostructures are primarily limited by the ability to fabricate these nanostructures with high enough material qualities, that can meet the required benchmarks in terms of electrical and optical performances. To this end, this dissertation explored both bottom-up and top-down techniques to fabricate scalable defect-free nanostructures for a wide variety of applications in low-power electronics and quantum devices. Here, by harnessing the advantages of selective area bottom-up growth as well as top-down lithography, nanostructures of the desired shape, size, electrical and optical properties were demonstrated, to satisfy the application in hand. In this regard, going beyond silicon as the material of choice is sometimes important since other materials (for example III-V semiconductors) can offer vastly superior performances for the desired applications. However, this brings in challenges of integration and cost-effectiveness for large-scale production, which

remain outstanding problems in the field. Despite this, nanostructures can deliver a clear advantage for the next generation of device technologies. In the following paragraphs, both the work performed in this thesis as well as some of the outstanding challenges and future directions for each project in this dissertation have been summarized.

A. Project 1 : Confined epitaxial lateral overgrowth (CELO)

Summary of work done: The first work in this thesis uses selective area growth (SAG) and confined epitaxial lateral overgrowth (CELO) as the primary techniques to build nanostructures at pre-defined positions on the sample. For this, primarily III-V semiconductors such as indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs) and gallium arsenide (GaAs) were explored. Using transmission electron microscopic techniques, the facets and defects in horizontal InP CELO nanostructures were first studied. Growth conditions (specifically growth temperature, group V/III ratios and template orientations) that result in defect-free nanostructures were identified. Subsequently, heterostructures and ultra-thin lateral quantum-wells were demonstrated in this geometry and low-temperature magneto-transport measurements were performed to extract material parameters in these growths. This work provided a comprehensive study of the optimum growth conditions and fabrication processes, required to scalable-y build high-quality CELO nanostructures. In the future, this can be used for fabricating heterostructure tunnel-junction based low-power electronic devices.

Future directions: The future work using CELO can have several different directions. One of the current major applications of CELO is to aid in the integration of III-V electronic and optical devices on silicon [13]–[20]. CELO has also been explored as an effective tool for building integrated photonic devices[17], [19], [20]. To this end, creating defect-free materials

is of utmost importance since defects can lower mobilities and also act as recombination centers, thus degrading both electronic and optical device performances respectively. Although significant progress has been made in this direction, controlling crystal phases (zincblende and wurtzite), eliminating dislocations and antiphase defects in small nanostructures remain as open challenges for a wide range of III-V materials. Apart from the challenges in defect and crystal facet control, currently the yield of CELO grown devices on a chip still remains low. Typically, considerable amount of variations are observed in the template geometries, junction lengths and defect densities, which lead to a spread in device performaces. A methodical comprehensive study is required to improve this yield, such that densely integrated circuits of such CELO devices can be fabricated, networks of such in-plane devices can be grown, and basic III-V circuits integrated on silicon can be demonstrated. This is critical to improving the usability of CELO for future scalable processes. Finally, one of the most exciting future directions in CELO, is to explore other nonconventional materials beyond III-V materials. Although there have been efforts to use templates fabricated from non-dielectric materials such as tungsten, very few reports of CELO grown non III-V nanostructures exist. Growing oxides, Heusler materials or even 2D materials using CELO can lead to very interesting results. The greatest advantage in these is that, it significantly reduces the number of post processing steps needed to fabricate devices out of the grown materials and that might prove particularly useful for materials that are prone to damage from etching processes.

B. Project 2 : Selective area growth of in-plane nanowires

Summary of work done: In the second part of this dissertation , selective area growth of in-plane semiconductor nanowires was studied. Such nanowires, in conjunction with s-wave superconductors are particularly attractive to study a wide range of one-dimensional electronic

transport effects at cryogenic temperatures, with potential applications in fabricating topological quantum hardware. First, the reliable growth of such nanostructures using chemical beam epitaxy was explored primarily for InP, InAs and InGaAs. The effects of including a buffer layer were studied and InP/InGaAs/InP quantum wells in nanowires were demonstrated. In addition, *in-situ* superconductor deposition techniques were developed using shadow template fabrication that resulted in high quality interfaces between the semiconductor and superconductor. This is crucial to achieving improved proximitized superconducting gaps in the semiconductor nanowire and probing the presence of topological quasiparticles in such hybrid nanowires. In summary, improvements in the qualities of SAG grown nanowire-superconductor hybrid nanostructures were demonstrated which can prove critical to exploring the physics of low-dimensional and low-temperature behaviors of electrons for future quantum hardware.

Future directions: Selective area grown in-plane nanowires using III-V materials have been explored widely for quantum electronic devices and optical components such as in-plane lasers. However, heterostructures in nanowires with widths in the range of 50-500nm have not been extensively explored. The work in this thesis, dealing with heterostructures demonstrates that carefully designing multi-layer quantum-wells can vastly improve the electronic and optical qualities of these SAG nanowires. More work in growing heterostructures in such nanowires is required. In addition, similar to CELO, identifying growth conditions and template geometries particularly aimed to improve nucleation, faceting and lowering defects in these structures are critical for future heterogeneously integrated SAG devices.

C. Project 3 : Superconducting capacitors and transmon devices based on high aspect ratio silicon fins

Summary of work done: The final part of this thesis explored a top-down lithographical approach to fabricate extreme aspect-ratio capacitors using silicon fins and aluminum electrodes. Such capacitors can be particularly useful for building high coherence superconducting qubits, due to its ability to use low-loss bulk float-zone grown silicon as the dielectric material – which can lower the dielectric losses in a qubit. Resonator measurements using microwave excitations at millikelvin temperatures were demonstrated that exhibit expected capacitor like behaviors from these fins and also a higher quality-factor compared to the current planar qubits. TEM measurements also demonstrated the high quality of the nanostructures and the successful self-shadowed superconductor deposition technique.

Future directions: The future work in this project will involve two parts. First, single fin capacitors coupled to a conventional $Al/AlO_x/Al$ junction needs to be demonstrated. If these devices exhibit a higher coherence time, it will serve as a direct proof to validate the usefulness of the improved capacitor design with a lower loss dielectric material. Second, approaches to reliably make the fins thinner and approach the tunneling regime need to be explored. In this respect digital etching using repeated oxidation and etching of the oxides or atomic layer etching techniques can be studied. These two immediate efforts can potentially enable both the improving of the coherence times of current superconducting qubits as well as the demonstration of the actual fin merged element transmon (FinMET) qubit, that has been

proposed in this dissertation. In the future, such approaches to use nanostructured capacitors can also be explored for materials beyond silicon.

References:

[1] H. Sakaki, "Scattering suppression and high-mobility effect of size-quantized electrons in ultrafine semiconductor wire structures," *Jpn J Appl Phys*, vol. 19, no. 12, pp. L735–L738, 1980, doi: 10.1143/JJAP.19.L735.

[2] H. Lueth, "Semiconductor nanostructures: a new impact on electronics," *Appl Surf Sci*, vol. 130–132, pp. 855–865, Jun. 1998, doi: 10.1016/S0169-4332(98)00166-4.

[3] C. Zhang and X. Li, "III-V nanowire transistors for low-power logic applications: A review and outlook," *IEEE Trans Electron Devices*, vol. 63, no. 1, pp. 223–234, Jan. 2016, doi: 10.1109/TED.2015.2498923.

[4] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature 2011 479:7373*, vol. 479, no. 7373, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[5] C. Y. Huang *et al.*, "3-D self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued moore's law scaling," *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2020-December, pp. 20.6.1-20.6.4, Dec. 2020, doi: 10.1109/IEDM13553.2020.9372066.

[6] Y. Zhang, J. Wu, M. Aagesen, and H. Liu, "III–V nanowires and nanowire optoelectronic devices," *J Phys D Appl Phys*, vol. 48, no. 46, p. 463001, Oct. 2015, doi: 10.1088/0022-3727/48/46/463001.

[7] B. Zhao, T. R. Chen, and A. Yariv, "The Extra Differential Gain Enhancement in Multiple-Quantum-Well Lasers," *J. Watson Sr. Laboratories of Applied Physics*, vol. 4, no. 2, pp. 128–95, 1992.

[8] F. Priolo, T. Gregorkiewicz, M. Galli, and T. F. Krauss, "Silicon nanostructures for photonics and photovoltaics," *Nature Nanotechnology 2014 9:1*, vol. 9, no. 1, pp. 19–32, Jan. 2014, doi: 10.1038/nnano.2013.271.

[9] S. Vaitiekėnas, Y. Liu, P. Krogstrup, and C. M. Marcus, "Zero-bias peaks at zero magnetic field in ferromagnetic hybrid nanowires," *Nature Physics 2020 17:1*, vol. 17, no. 1, pp. 43–47, Sep. 2020, doi: 10.1038/s41567-020-1017-3.

[10] J. Wang *et al.*, "Interplay between superconductivity and ferromagnetism in crystalline nanowires," *Nature Physics 2010 6:5*, vol. 6, no. 5, pp. 389–394, Mar. 2010, doi: 10.1038/nphys1621.

[11] Y. Liu *et al.*, "Semiconductor-Ferromagnetic Insulator-Superconductor Nanowires: Stray Field and Exchange Field," *Nano Lett*, vol. 20, no. 1, pp. 456–462, Jan. 2020, doi: 10.1021/ACS.NANOLETT.9B04187/SUPPL_FILE/NL9B04187_SI_001.PDF.

[12] M. v Rakhlin *et al.*, "InAs/AlGaAs quantum dots for single-photon emission in a red spectral range OPEN," vol. 8, p. 5299, 2018, doi: 10.1038/s41598-018-23687-7.

[13] M. Borg, H. Schmid, K. E. Moselund, D. Cutaia, and H. Riel, "Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si," *J Appl Phys*, vol. 117, no. 14, Apr. 2015, doi: 10.1063/1.4916984.

[14] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, and H. Riel, "Complementary III-V heterojunction lateral NW Tunnel FET technology on Si," *Digest of*

Technical Papers - Symposium on VLSI Technology, vol. 2016-Septe, no. 619509, pp. 1–2, 2016, doi: 10.1109/VLSIT.2016.7573444.

[15] M. Sousa, S. Mauthe, B. Mayer, S. Wirths, H. Schmid, and K. E. Moselund, "Monolithic Integration of III-V on Si Applied to Lasing Micro-Cavities: Insights from STEM and EDX," *Proceedings of the IEEE Conference on Nanotechnology*, vol. 2018-July, pp. 1–4, 2019, doi: 10.1109/NANO.2018.8626223.

[16] C. Convertino *et al.*, "InGaAs FinFETs directly integrated on silicon by selective growth in oxide cavities," *Materials*, vol. 12, no. 1, Dec. 2018, doi: 10.3390/ma12010087.

[17] S. Wirths *et al.*, "Room-Temperature Lasing from Monolithically Integrated GaAs Microdisks on Silicon," *ACS Nano*, vol. 12, no. 3, pp. 2169–2175, 2018, doi: 10.1021/acsnano.7b07911.

[18] H. Schmid *et al.*, "Template-assisted selective epitaxy of III-V nanoscale devices for co-planar heterogeneous integration with Si," *Appl Phys Lett*, vol. 106, no. 23, Jun. 2015, doi: 10.1063/1.4921962.

[19] S. Mauthe *et al.*, "High-speed III-V nanowire photodetector monolithically integrated on Si," *Nature Communications 2020 11:1*, vol. 11, no. 1, pp. 1–7, Sep. 2020, doi: 10.1038/s41467-020-18374-z.

[20] S. Mauthe *et al.*, "InP-on-Si Optically Pumped Microdisk Lasers via Monolithic Growth and Wafer Bonding," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 6, 2019, doi: 10.1109/JSTQE.2019.2915924.

IX. Appendix

IX A. Scanning electron microscopy

Scanning electron microscopy (SEM) projects and scans a focused beam of electrons over a surface. The electron interaction with the sample generally produces secondary electrons, backscattered electrons and X-rays. Secondary electrons (SE) are produced from inelastic interactions, when an incident electron excites an electron in the sample and loses some of its energy in the process. Back-scattered electrons (BSE) are generated when the electrons are elastically scattered and reflected back. BSE signals are dependent on the atomic weight of the element and provides Z contrast. These signals are collected by multiple detectors and reconstructed to form a real space image of the sample. The interaction volume depends on the energy of the electron beam used. Therefore, a higher energy beam penetrates more into the sample and images inner depths of the sample. The resolution achievable is usually in the range of 10nm with very careful alignment.

IX B. X-ray diffraction

X-ray diffraction is ana analytical tool that helps image the reciprocal lattice of a crystalline compound and is an invaluable feedback tool for epitaxial growth. The reciprocal lattice is very simply the Fourier transform of the real space lattice. The technique of XRD involves shooting a beam of X-rays (typically Cu K-alpha wavelength) at a sample and measuring the reflection from the elastically scattered beams that constructively or destructively interfere. The detectable reciprocal points depend on the structure factor of the compound, and the angle of incidence of the X-ray beam for a fixed wavelength and can be calculated theoretically through an Ewald sphere construction. One of the most common uses

for XRD is to determine the lattice parameters of a crystalline (or polycrystalline) compound. For ternary or quaternary element this directly provides an insight into the chemical composition of the compound and thus acts as a feedback for epitaxial growth.

IX C. Transmission electron microscopy (TEM)

A standard transmission electron micrscopy measurement involves passing an accelerated beam of electrons through a very thin sample and measuring the transmitted electrons using various detector configurations. In general the a TEM consists of an electron gun where the generated electrons are accelerated typically in the range 100-300keV. The two most commonly used electron sources are

(1) Thermionic electron gun : thermionic emission from W or LaB_6 crystal when heated with an electric current.

(2) Field emission gun (FEG) where the electrons are extracted from the sharp tip of a W needle by applying an electric field. Typically produces electron beams with higher coherence.

Post generation, the electrons are focused by a condenser system that contains a series of magnetic lenses and apertures. The beam can be made parallel (for TEM mode) or convergent (for scanning TEM) by changing the lens settings. The electron beam then passes through the sample which sits in high vacuum in a goniometer stage with precise control of X,Y,Z movements along with rotation. Below the sample an objective lens generates the image (of both the specimen and the diffraction pattern depending on where it is focused). The image can be switched between a bright field and a dark field image by selecting either the central beam on the optic axis or particular diffraction beams by using an aperture in the back focal

plane of the objective lens. The final image can be viewed on a phosphor viewing screen directly or through a CCD camera (and imaged).

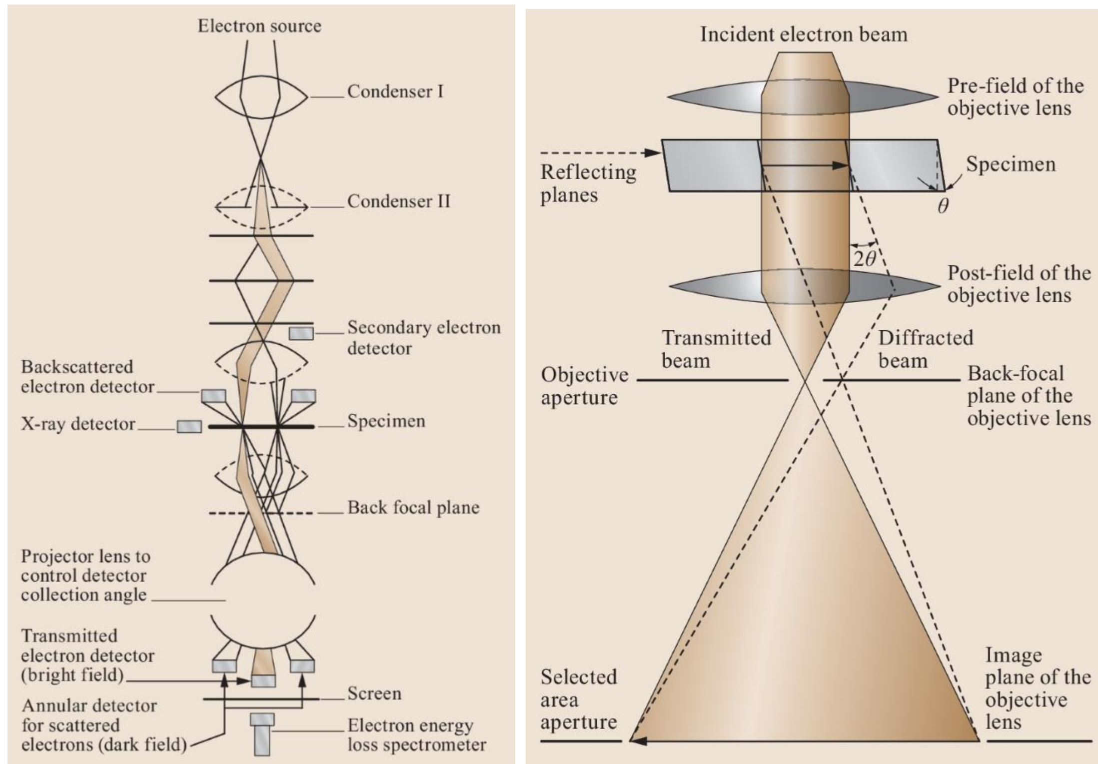

Figure 9.1: The optics column of a standard TEM (left) and schematic of ray paths (right) (reprinted with permission from [1]).

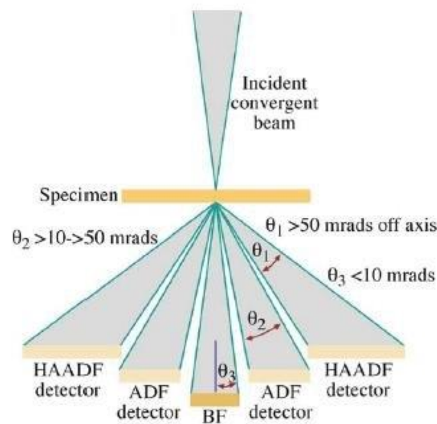

Figure 9.2. Schematic diagram of HAADF detector setup along with other detectors (image adapted from [2]).

For Scanning TEM or STEM, the convergent beam interacts with the sample and generates signals which are recorded for each spot and reconstructed into an image. The Bright Field (BF) detector detects the beam along the microscope optic axis. The annular dark field (ADF) detector is a ring shape detector with collection angles in the range of 10-50 mrad and detects electrons scattered into small angles. The high angle annular dark field (HAADF) detector is similar to the ADF but detects electrons scattered at higher angles (>50mrad). The HAADF detector detects electrons that are mostly from incoherent scattering events and the contrast heavily depends on the atomic number (Z) .

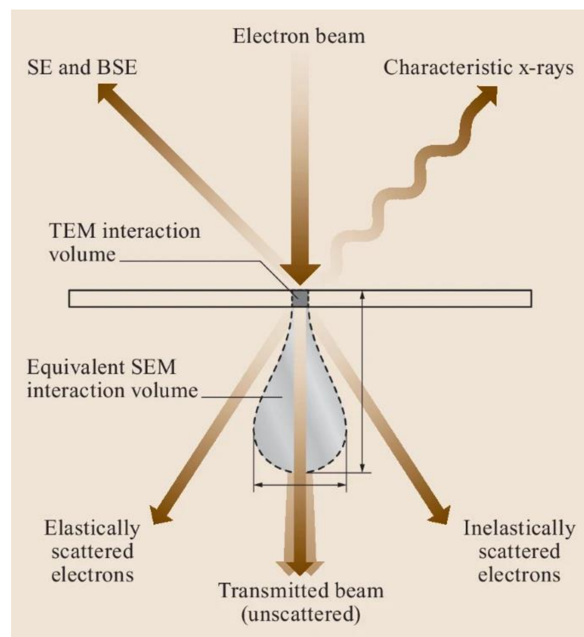

Figure 9.3 Schematic showing the most important electron-matter interactions arising during the interaction of an electron beam with a specimen. If the sample thickness is small enough to allow at least a part of the electrons to pass through, then certain signals below the sample are observable (image reprinted with permission from [1])

When interacting with a thin sample, the convergent electron beam generates a multitude of signals. Elastic interactions (no energy loss from electrons into sample) contribute to the direct beam with minimal deviation from its path. When an electron interacts strongly with the nucleus of the sample atoms, they are scattered much more dramatically. Electrons that scatter into the direction from which they arrived are labelled as back scattered electrons. This scattering is strongly dependent on the nuclear charge and as a result is dependent on the atomic number Z (i.e. heavier elements generate more signal {$\propto Z^2$} and appear brighter as a rule of thumb also known as Z contrast). In amorphous compounds with no clear order, incoherent scattering occurs. If a crystalline lattice is probed, coherent scattering takes place and Bragg diffraction results from constructive or destructive interference from diffracted beams.

IX D. Energy Dispersive X-ray spectroscopy

Energy dispersive X-ray spectroscopy (EDX or EDS) is an analytical technique to determine elemental composition of a compound. When electron beams interact with a sample they produce bremsstrahlung (breaking) radiation and characteristic X-rays. The bremsstrahlung process is caused by deceleration of the electrons by the nucleus and the subsequent emission of the electron energy as X-rays. This forms a skewed bell shaped background in the detector (low energy X-rays are absorbed in the sample). The characteristic X-rays are formed when the incoming electron removes an electron from the inner shell of the sample atoms. The vacancy is quickly filled by a higher energy electron from the outer shell by emitting X-rays or Auger electrons (by transferring the energy to emit another electron from the outer shell). The X-ray emitted has a wavelength that is determined by the energy spacings between the shells of the atom and is therefore dependent on the atomic number of the element. A crystal spectrometer is used to separate the X-rays into their different wavelengths and the

intensities measured by gas proportional counter (or a Si /Ge chip that generates electron-hole pairs when the X-rays hit the chip). Thus, a signal intensity vs wavelength plot can be generated that contains the ratios of the individual elements of the sample. A more comprehensive discussion can be found on [3].

IX E. Chemical beam epitaxy (CBE) manipulator maintenance

The substrate heater for the CBE manipulator shorted resulting in inadequate and uneven heating of the sample block and the inability to reach temepratures above 250-300 C. Therefore the manipulator needed to be taken out of the system. The CBE uses PH3 and AsH3 precursors which are highly toxic compounds. In addition, due to the use of cracked phosphorus in the chamber, the cryo-shield and chamber walls are coated with phosphorus,

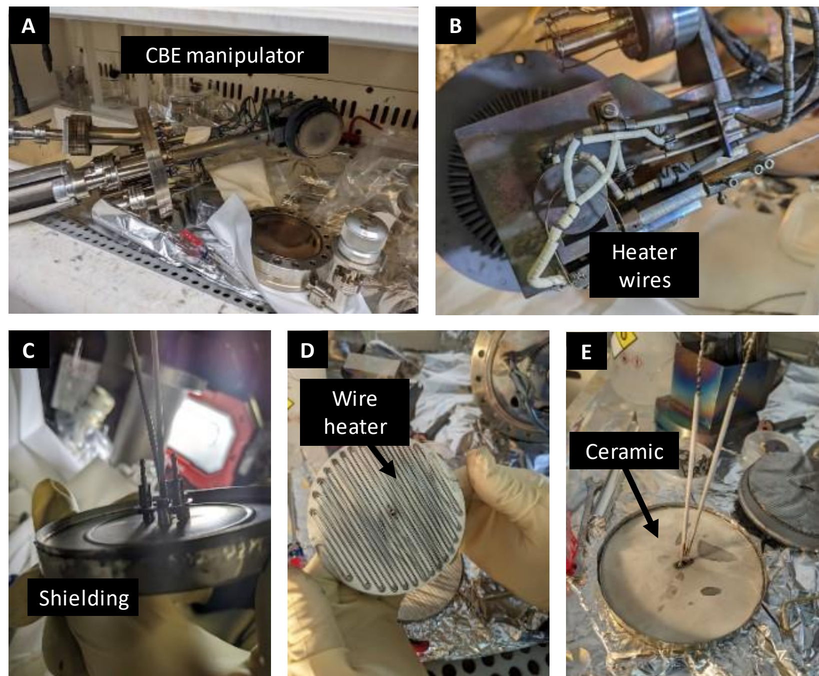

Figure 9.4 : (A) the CBE manipulator (B) the ceramic shielding on the heater wire (C) shielding around the heater wire (D) The wire heater that buckled and shorted (E) Ceramic on top of the heater wire.

which is inflammable in contact with oxygen. To vent the system safely, the chamber was baked to about 130°C for over a week to get most of the deposition out of the walls. During chamber vents, a gas mask needs to be worn which is maintained at a high positive pressure with air being pumped through gas lines from an external room. During the vent, the chamber is first vented with nitrogen and kept vented for a few hours. Thereafter the manipulator was

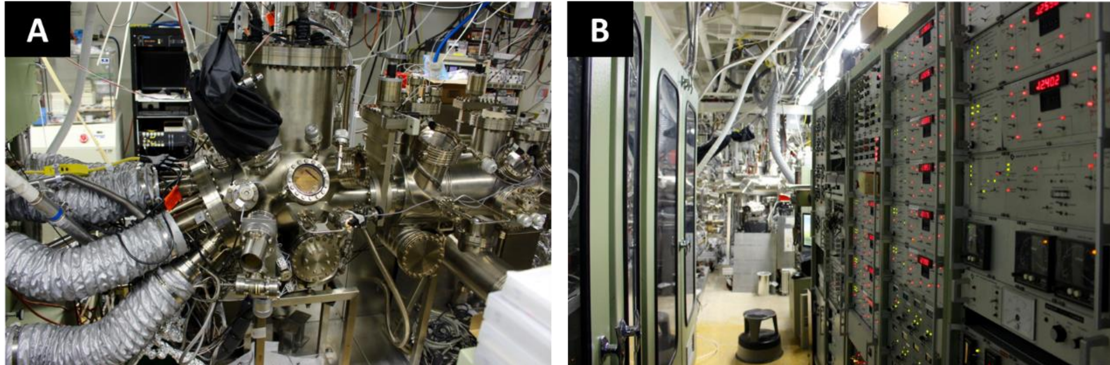

Figure 9.5 : (A) the CBE system (B) CBE gas cabinet (left) and control electronics racks (right)

taken out, and the ports blanked. The exact point of the short was not clearly understood but a new Ta wire was coiled against a jig to make a new heater and installed carefully. Extra ceramic shieldings were installed to ensure lower chances of shorting. Then the manipulator was reassembled and put back into the chamber. The chamber was thereafter baked for almost two weeks till it reached a low base pressure.

9f. Reflection high energy electron diffraction (RHEED)

RHEED refers to reflection high energy electron diffraction. In MBE or CBE, RHEED can be used as a real time monitoring for the growth. It involves a high energy beam of electrons in the range 5-40keV reflecting off the surface of the growing sample at glancing incidence (1-3°). The de Broglie wavelength of these electrons is in the range 0.17-0.06A and the beam only samples the first few atomic layers of the sample. Using kinematic diffraction analysis of the

incident beam and its interaction with the sample reciprocal space one can map the surface unit cell of the sample.

Kinematic theory of diffraction can be described as follows. Since the absolute magnitude of atomic amplitudes of scattering of electrons is very small, the intensities of the scattered beam will, in the presence of a limited number of scattering centers (atoms), be small compared with the intensity of the primary beam. Thus, it is possible to ignore the loss of energy of the primary beam in the course of its "expenditure" in the formation of coherently scattered radiation. One may also ignore the coherent scattering of secondary beams, which, acting in their tum as primary beams, give rise to new diffracted beams, and so on. As the volume of coherent scattering increases, i.e., the number of scattering centers increases, the intensities of the secondary beams will increase, and the description of the processes taking place must be based on the dynamical theory of scattering. In this theory, energy interrelationships are taken into account and, generally speaking, all beams are taken as qualitatively equivalent to the primary beam and to one another [4].

For a lattice with real space lattices of sizes a,b, c, the reciprocal space is defined by vectoes $a^* = \frac{2\pi h}{a}$, $b^* = \frac{2\pi h}{b}$ and $c^* = \frac{2\pi h}{c}$. Each point in the reciprocal space is characterized by a vector $\frac{2}{2\pi} = G = ha^* + kb^* + lc^*$ having its origin at the point (0,0,0). For orthogonal unit cells, the condition for diffraction by a crystal are given by $s = 2\pi G$; $k = k_0 + s = k_0 + 2\pi G$. For any given position of the crystal, the intersection of these points on the reciprocal space with the Ewald sphere (incident beam in reciprocal space) gives rise to a detectable reciprocal space point. The Ewald sphere has a radius of $\frac{1}{\lambda}$.

X-ray diffraction has a wavelength (Cu K-α) of approximately 1-2A, which is comparable to unit cell distances (5-10A). Therefore, the Ewald sphere only cuts a few of the reciprocal

space points and a limited number of peaks are visible. In electron diffraction, the wavelengths are in the order of 0.05A. Therefore, in the reciprocal space, the Ewald sphere radius is large and appears almost flat with respect to the unit cell reciprocal space points. As a result most points become visible and the resulting pattern is almost a section of the reciprocal lattice. The following are some examples of the unit cell and their reciprocal lattices.

Using the Bragg equation, the distance between the sample and the RHEED screen and the crystal structure, one can calculate the atom periodicities in the solid surface region by measuring the diffraction spot spacings.

For diffraction on smooth surfaces, RHEED patterns usually consist of streaks. When the uppermost crystal layer is considered as the layer that the electron beam interacts with, it is essentially a 2D layer where the reciprocal space is represented by rods in a direction normal to the surface. Th intersection of the Ewald sphere and the rods happen along their length, resulting in streaks instead of dots. Thus, RHEED gives a direct insight into solid surfaces.

The surface of a solid is always different from the bulk material due to rearrangements of atoms on the surface. Surfaces can rearrange into symmetric patterns. A (m x n) reconstruction for a crystalline material for example GaAs (100) typically refers to a unit mesh that is m x n times larger than the underlying bulk structure. Such surfaces may be centered referred to as c(m x n) (such as c(2x8)) or rotated with respect to the principal axes of the underlying bulk and then indicated by the rotation angle such as $(\sqrt{19}x\sqrt{19})R23.4°$.

References :

[1] J. McKinley, “Electron and Ion Beam Characterization of Glass. In: Musgraves, J.D., Hu, J., Calvez, L. (eds) Springer Handbook of Glass. Springer Handbooks (2019). Springer, Cham. DOI : 10.1007/978-3-319-93728-1_27

[2] S. Hussain. “Structural and optical characterization of green-yellow light emitting devices with high indium concentrated (In,Ga)N quantum wells”. Physics. Univeristé Nice Sophia Antipolis”, 2014

[3] Dr C B Boothroyd “Microanalysis in the electron microscope” http://fy.chalmers.se/~f10mh/Halvarsson/EM_intro_course_files/EDX%20intro.pdf

[4] Helmut Sitter and Marian A. Herman “Molecular Beam Epitaxy: Fundamentals and Current Status”