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Background Digital Calibration Techniques for High-Speed,

High Resolution Analog-to-Digital Data Converters

A dissertation submitted in partial satisfaction of the requirements

for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Yun-Shiang Shu

Committee in charge:

>   Professor Bang-Sup Song, Chair
>   Professor Chung-Kuan Cheng
>   Professor Miroslav Krstic
>   Professor Larry Larson
>   Professor Paul Yu

2008

The Dissertation of Yun-Shiang Shu is approved, and it is acceptable in quality and

form for publication on microfilm:

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<div align="right">Chair</div>

University of California, San Diego

2008

To my father, mother, and sisters

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Vita

1997	B.S. Electrical Engineering National Taiwan University, Taipei, Taiwan
1999	M.S. Electrical Engineering National Taiwan University, Taipei, Taiwan
2000-2002	Design Engineer ALi Corp., Taipei, Taiwan
2003-2007	Research Assistant University of California, San Diego, La Jolla, CA
2004, 2006	Summer Intern Conexant Systems, Inc., Palm Bay, FL
2008	Ph.D. Electrical Engineering University of California, San Diego, La Jolla, CA

Publications

Y.-S. Shu and B.-S. Song, "A 15b-linear, 20MS/s, 1.5b/stage pipelined ADC digitally dalibrated with signal-dependent dithering," *IEEE J. Solid-State Circuits,* Feb. 2008.

Y.-S. Shu, B.-S. Song, and K. Bacrania, "A 65nm continuous-time $\Delta\Sigma$ modulator with 81dB DR and 8MHz bandwidth auto-tuned by pulse injection," *ISSCC Dig. Tech. Papers,* Feb. 2008

Y.-S. Shu and B.-S. Song, "A 15b-linear, 20MS/s, 1.5b/stage pipelined ADC digitally calibrated with signal-dependent dithering," *Symp. VLSI Circuits Dig. Tech. Papers,* Jun. 2006, pp. 270–271.

Y.-S. Shu and W.-S. Feng, "Design and implementation of a double-sampled bandpass delta-sigma Modulator," Master Thesis, National Taiwan University, June 1999

ABSTRACT OF THE DISSERTATION

Background Digital Calibration Techniques for High-Speed,

High Resolution Analog-to-Digital Data Converters

by

Yun-Shiang Shu

Doctor of Philosophy in Electrical Engineering

(Electronic Circuits and Systems)

University of California, San Diego, 2008

Professor Bang-Sup Song, Chair

A high-speed, high-resolution analog-to-digital converter (ADC) is a key

component in broadband communication transceivers, video imaging systems, and

instrumentation. As the ADC speed increases with the advances in IC fabrication

technology, the ADC resolution is still limited by the non-ideal effects of the circuits,

such as device inaccuracy, component mismatch, and finite device gain. A recent trend

for enhancing the resolution is to calibrate the non-ideal effects in background with the aid of digital signal processing. These techniques are preferred since the calibration accuracy is not limited by the accuracy of the analog components, and the calibration tracks the variations of process, voltage and temperature without interrupting ADC's normal operation.

This dissertation describes the background calibration techniques for three high-speed, high-resolution ADCs using different architectures: pipelined, floating-point, and continuous-time (CT) $\Delta\Sigma$. For pipelined ADCs, a background digital calibration technique with signal-dependent dithering scheme is proposed to overcome the dither magnitude and measurement time constraints with the existing fixed-magnitude dithering. A 15-b, 20-MS/s prototype ADC achieves a spurious-free dynamic range (SFDR) of 98 dB and a peak signal-to-noise plus distortion ratio (SNDR) of 73 dB. The chip is fabricated in 0.18-μm complementary metal-oxide-semiconductor (CMOS) process, occupies an active area of 2.3 x 1.7 mm^2, and consumes 285 mW at 1.8 V.

The concept of signal-dependent dithering is also applied to a floating-point ADC (FADC) to calibrate the gain and offset errors in the variable gain amplifier

(VGA) stages. A digitally-calibrated 10~15-b 60-MS/s FADC adjusts its quantization steps instantly depending on the sampled input level and enhances the integral non-linearity (INL) from 24 to 0.9 least significant bit (LSB) at a 15-b level for small input signals. The chip is fabricated in 0.18-μm CMOS process, occupies 3.5 x 2.5 mm^2, and consumes 300 mW at 1.8 V.

In the CT ΔΣ architecture, the active filter is calibrated by injecting a binary pulse dither and nulling it with an LMS algorithm. The proposed technique calibrates the filter time-constant continuously with crystal accuracy, while the conventional master-slave approaches use additional analog components which limit the calibration accuracy. A 3rd-order 4-b prototype in 65-nm CMOS occupies 0.5 mm^2 and consumes 50 mW at 1.3 V. It achieves a dynamic range (DR) of 81 dB over an 8-MHz signal bandwidth with a 2.4 V$_{pp}$ full-scale range. Signal-to-noise ratio (SNR) and SNDR at −1 dBFS are 76 and 70 dB, respectively.

Chapter 1

Introduction

1.1 Motivation

Wireless communication applications have been a major driver for the development of high-speed and high-resolution analog-to-digital converters (ADCs). ADCs with very high dynamic range and high sampling rate can simplify system design, reduce overall cost, and maximize receiver sensitivity. Many other applications, such as instrumentation and imaging also benefit from higher-speed and high-performance ADCs. Switched-capacitor pipelined architecture has been a consistent choice to meet both requirements on speed and resolution. In general, pipelined ADCs are attractive in applications where the required bandwidth is too high for oversampling $\Delta\Sigma$ ADCs and the required resolution is too high for flash ADCs. Recently, $\Delta\Sigma$ ADCs using continuous-time (CT) loop filters have achieved conversion

rates up to 40 MHz with a 13-b resolution. Although pipelined ADCs exhibit better performance, CT $\Delta\Sigma$ ADCs are attractive due to the build-in anti-aliasing filtering and the potential to be low-voltage, low-power designs.

The resolution of pipelined ADCs is mainly limited by the inter-stage gain error resulting from capacitor mismatch and finite operational amplifier (opamp) gain. Pseudo random noise (PN) dithers have been used to measure the inter-stage gain errors in the background and to calibrate them digitally. By injecting PN dithers into a pipelined stage, the gain error in the signal path can be obtained by correlating the digital output with the same PN sequence. However, existing PN dithering schemes suffer from signal range reduction when a large dither is injected, and need long signal de-correlation time when high measurement accuracy is required. For any background digital calibration to be practical, it should make a less impact on the circuit and system performance, and constantly track the inter-stage gain error variation due to the variations in process, voltage, and temperature (PVT).

CT $\Delta\Sigma$ ADC performance is also affected by the PVT variation. One of the critical issues is the inaccurate filter time constant, which is set by the absolute RC values which has 20~30% variations. In most cases, the CT filter is calibrated in the

background using master-slave approaches. The filter time-constant variation in a replica filter is calibrated first without interrupting the main filter's normal operation, and then the main filter is adjusted accordingly. However, the calibration accuracy is limited by the mismatch between the main filter and its replica circuits. For CT $\Delta\Sigma$ ADCs, a filter time-constant calibration technique with better accuracy is needed to further mitigate the design tradeoff between performance and stability and to make the MASH-type modulator practical.

1.2 Research Goal

This research seeks to address and solve the issues in the existing background digital calibration techniques for pipelined ADCs and investigate different ADC architectures for high-speed, high-resolution applications. A more general goal of this research is to discover a common calibration scheme applicable to various ADCs. In the context of these goals, some key research results are summarized below:

◆ The measurement time and dither magnitude constraints in the fixed-magnitude PN dithering schemes are investigated.

◆ Signal-dependent dithering is proposed to allow injecting of a large dither

without reducing the signal range and to keep the signal-to-dither ratio low; therefore, both constraints associated with the fixed-magnitude dithering are greatly relaxed.

◆ Signal-dependent dithering is also applied to a high-speed, high-resolution FADC for gain and offset calibration. The FADC effectively reduces the quantization error and enhances the ADC linearity by 5 b for small input signals.

◆ An automatic tuning technique with pulse injection is proposed to calibrate the filter time-constant in a 3rd-order 4-b CT $\Delta\Sigma$ modulator. Highly accurate calibration is achieved. The same technique can be applied to tune CT filters in MASH-type $\Delta\Sigma$ modulators

1.3 Thesis Organization

Chapter 2 provides a brief overview of the non-linearity error in pipelined ADCs and the constraints of background gain measurement by PN dithering. In Chapter 3, a digital background calibration scheme based on signal-dependent dithering is proposed and applied to an 1.5b/stage pipelined ADC. Chapter 4 describes a digitally-calibrated FADC with background gain and offset calibration. An automatic

tuning technique is proposed to calibrate the filter time-constant of a CT $\Delta\Sigma$ modulator

in Chapter 5. Chapter 6 concludes the presentation of this research and gives

recommendations for future work.

Chapter 2

Background Digital Calibration of Pipelined ADCs

2.1 Introduction

The resolution of the pipelined ADC is limited by the inter-stage gain error resulting from capacitor mismatch and finite opamp gain in the multiplying DAC (MDAC). As fine-line lithography advances, even 14-b level performance has been achieved without calibration by carefully matching capacitors in the multi-bit first-stage MDAC but still using high-gain opamps [1], [2]. A recent trend is to digitally calibrate both capacitor mismatch and opamp finite gain errors simultaneously in the background [3]–[14]. The digital background calibration is preferred to other high-resolution techniques because it can track long-term process variations, and the digital power and area overhead diminishes as CMOS technology is

scaled down. For any background calibration to be useful, it is necessary that its impact on analog circuits be minimized, and the calibration cycle be made short.

The pseudo-random noise (PN) pulse sequence has been used in background calibration for error randomization and detection [7]–[19]. PN-modulated errors or dithers can be measured by correlating them digitally with the same PN sequences. In the digital domain, the measurement process is simply the digital sign change by the PN followed by the accumulation for averaging (low-pass filtering). In most cases, capacitor mismatch errors can be PN-modulated by switching circuit configurations [15]–[17]. However, to measure the total gain error contributed by both capacitor mismatch and finite opamp gain, a PN-modulated dither needs to be injected into the same gain path for gain measurement, but it can be subtracted later digitally [7]–[12], [18]. However, with a large un-correlated signal present, it is difficult to detect a small PN-modulated error. In particular, a prohibitively large number of samples should be accumulated when the number of bits resolved per stage is low [9]. Moreover, the signal magnitude needs to be reduced so that the signal plus dither may not exceed the full-scale range of the MDAC [7]–[10], [18].

In Section 2.2 the ADC non-linearity error resulting from capacitor mismatch

and finite opamp gain is explained. Section 2.3 describes the concepts of digital calibration and the background error measurement by PN dithering. The constraints of PN dithering is discussed in Section 2.4.

2.2 Non-Linearity Error of a Pipelined ADC

A pipelined ADC consists of several low-resolution stages as shown in Figure 2.1. In each stage, after the input is sampled and quantized by the sub-ADC, the residue is amplified to fit into the next stage's full range using a switched-capacitor MDAC [21]. Since the comparator offsets in the sub-ADC can be digitally corrected using a redundant bit [22], the ADC performance relies only on the accuracy of the amplified residue.
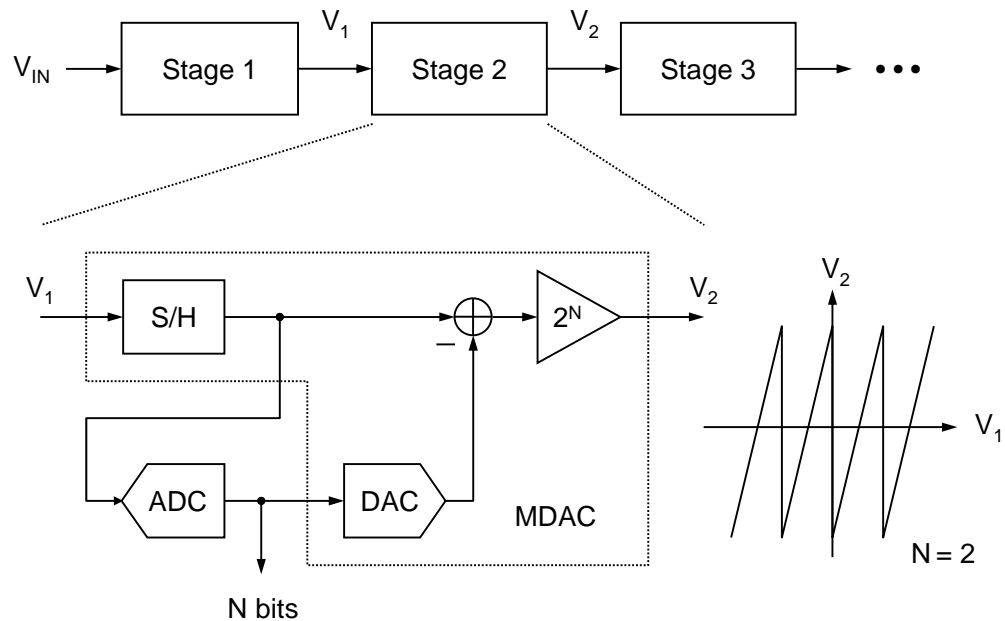
Figure 2.1: Pipelined ADC block diagram.

Figure 2.2 shows a tri-level MDAC in two phases. The input signal is sampled on both capacitors during the sampling phase. In the amplification phase, one of the capacitors is switched to the opamp output, and the other to $\pm V_{REF}$ or 0 depending on the sub-ADC output bit, b. Consequently, the sampled input is amplified by a gain of 2, and bV_{REF} is subtracted as shown in the residue plot of Figure 2.2 (c), where the comparator thresholds of the sub-ADC are set to $\pm 1/4$ V_{REF}.
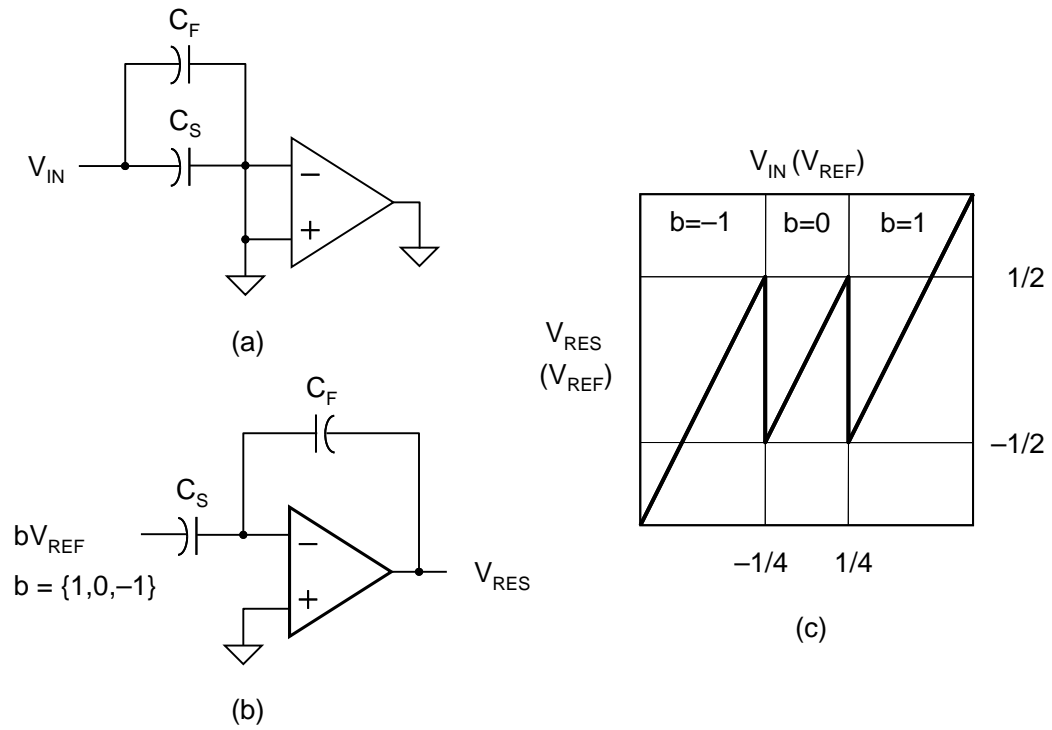
Figure 2.2: Tri-level MDAC. (a) Sampling phase.
(b) Amplification phase. (c) Residue plot.

In practice, the amplified residue is affected by two major non-ideal factors, α and δ, which result from capacitor mismatch and finite opamp gain, respectively, and becomes

$$V_{RES} = (1+\delta)[(2+\alpha)V_{IN} - (1+\alpha)bV_{REF}].\qquad(2.1)$$
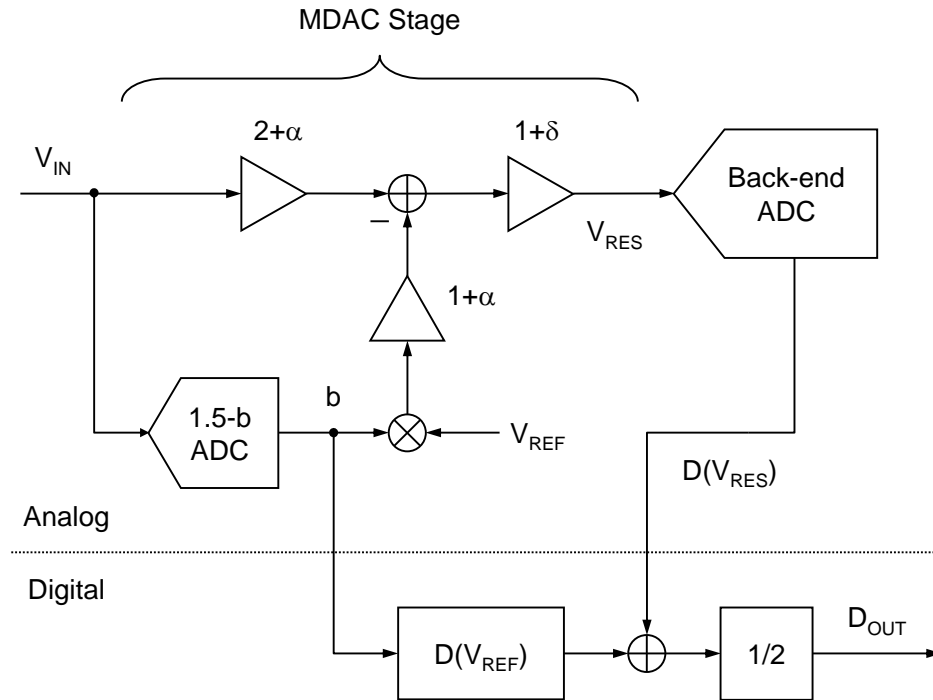
Figure 2.3: Model of a pipelined ADC with non-ideal factors.

Using (2.1), the MDAC stage can be modeled as shown in Figure 2.3. The residue, V_{RES}, is further digitized by the later ADC stages. The digital output, D_{OUT}, is obtained by adding the digital V_{REF}, $bD(V_{REF})$, to the digitized residue, $D(V_{RES})$, and then divided by 2 so that what is subtracted in the MDAC can be restored digitally. However, the analog bV_{REF} subtracted in (1) is affected by both α and δ, and therefore, it does not match with the ideal digital V_{REF}, $bD(V_{REF})$. Figure 2.4 shows how this mismatch affects the pipelined ADC's linearity. In this example, $(1+\alpha)(1+\delta)V_{REF}$ is subtracted in the analog domain, but the ideal $D(V_{REF})$ is added in the digital domain

when the sub-ADC output bit is 1. As a result, a mismatch error occurs at the comparator threshold point, and is translated into the non-linearity of the ADC.
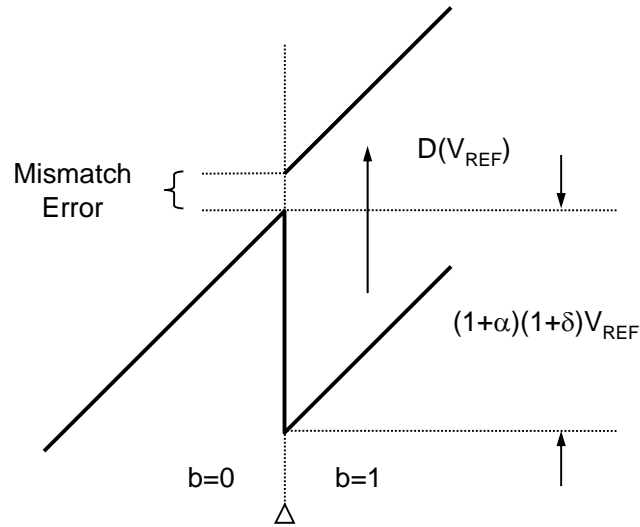
Figure 2.4: Non-linearity error in pipelined ADC.

2.3 Background Digital Calibration

2.3.1 Digital Calibration Concept

The mismatch between the analog V_{REF} and the digital $D(V_{REF})$ can be eliminated by either reducing the non-ideal factors in the analog domain or by adjusting $D(V_{REF})$ or $D(V_{RES})$ in the digital domain. The analog implementation usually requires capacitor trimming [23], capacitor error-averaging [24]–[26], or

capacitor shuffling [16], [27] to reduce the capacitor mismatch error α and uses high-gain opamps to get rid of the low-gain effect δ. Such analog methods increase the circuit complexity, especially in the opamp design at low supply voltages. However, in the digital implementation, only the digital $D(V_{REF})$ needs to be adjusted to match the non-ideal analog V_{REF} [28], [29]. For this, the analog V_{REF} should be measured accurately with the back-end ADC. The digital calibration concept is explained in Figure 2.4. While $(1+\alpha)(1+\delta)V_{REF}$ is subtracted in the MDAC, the digital value of $D[(1+\alpha)(1+\delta)V_{REF}]$ is added back instead of the ideal $D(V_{REF})$ to eliminate the mismatch error. Even after this calibration, the overall gain slope error remains, but the gain slope correction is not necessary since the ADC transfer function is linear. Note that the mismatch error can also be eliminated by gain slope adjustment, but digital multipliers are required. In such a case, the digitized residue, $D(V_{RES})$, in Figure 2.3 need to be multiplied by $1/(1+\alpha)(1+\delta)$ before the ideal $D(V_{REF})$ is added. Digital calibration may increase the complexity of the digital circuitry, but the overhead is minimal in deep submicron CMOS chips.
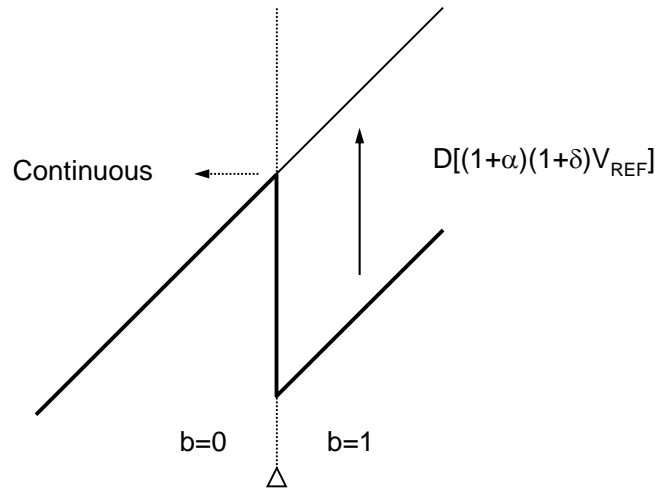
Figure 2.5: Digital calibration concept.

2.3.2 Background Gain Measurement with PN Dithering

Figure 2.6 explains the gain measurement scheme by PN dithering, where the gain errors of $(1+\alpha)$ and $(1+\delta)$ are combined as $(1+\varepsilon)$. To measure this gain of the V_{REF}, a well-defined PN-modulated calibration signal, V_{CAL}, which is a usually a fraction of V_{REF}, is added to the input, V_{IN}. The PN is a zero-mean sequence of 1 and -1. After multiplied by the same PN and V_{REF}/V_{CAL}, the digital output becomes

$$\frac{V_{IN}}{V_{CAL}} PN(1+\varepsilon)V_{REF} + PN^2(1+\varepsilon)V_{REF} \qquad (2.2)$$
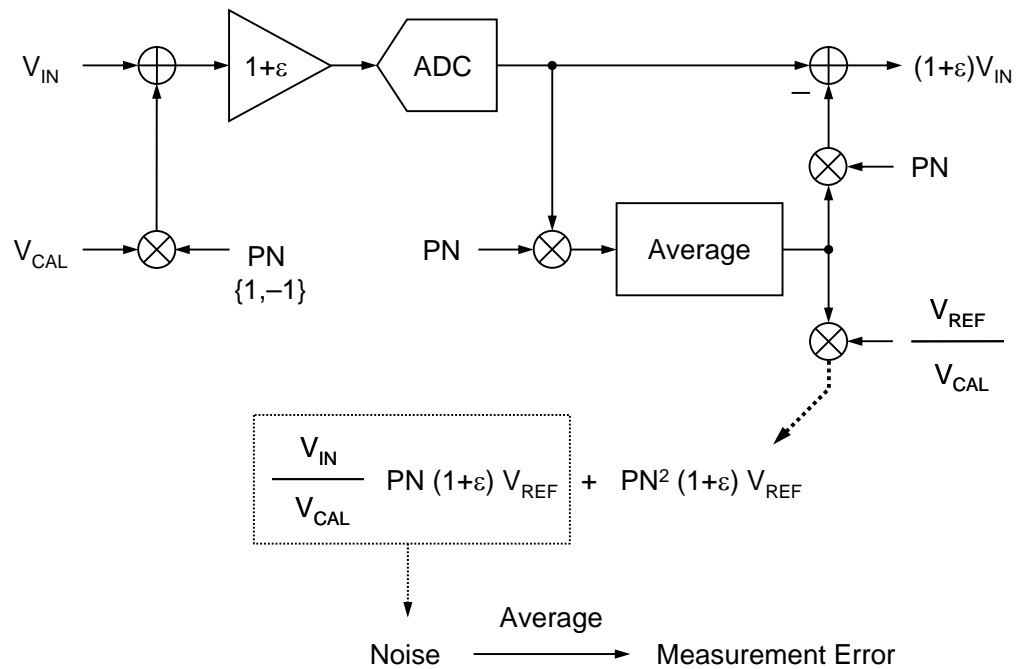
Figure 2.6: Principle of background gain measurement with PN dithering.

Note that the input signal, V_{IN}, is modulated by PN and translated into a noise, but the PN-modulated calibration signal is correlated by the same PN sequence and becomes a DC value of $(1+\varepsilon)V_{REF}$ since $PN^2 = 1$. Therefore, the gain of V_{REF} is obtained by low-pass filtering the output given by (2.2). However, since the bandwidth of the low-pass filter is limited, the noise-like PN-modulated V_{IN} remains as a measurement error after low-pass filtering. The simplest digital low-pass filter is an accumulator that averages a large number of samples. Ideally, the measurement error approaches zero if infinitely many samples are averaged. However, as the number of

samples is limited in practice, V_{IN}/V_{CAL}, which is the signal-to-dither ratio, should be

kept as small as possible in order to minimize this residual measurement error.

Figure 2.7 shows how the gain measurement is performed in one 1.5-b stage in

the pipelined ADC, where the measurement function is enclosed inside the dotted

rectangle. The subtracted bV_{REF} is multiplied by the gains of $(1+\alpha)$, $(1+\delta)$, and

quantized by a non-ideal back-end ADC with a gain of $(1+\gamma)$. The PN-modulated V_{CAL}

is injected to measure the gain of the V_{REF}. After the PN correlation, accumulation for

averaging, and multiplication by V_{REF}/V_{CAL}, the digital value of

$D[(1+\alpha)(1+\delta)(1+\gamma)V_{REF}]$ is obtained. Therefore, all errors resulting from capacitor

mismatch, finite opamp gain, and the non-ideal back-end ADC can be grouped and

calibrated as one gain error. Once calibrated, the ADC performance will be only

limited by the non-linearity of the opamp and non-linear signal-dependent charge

injection in sampling.
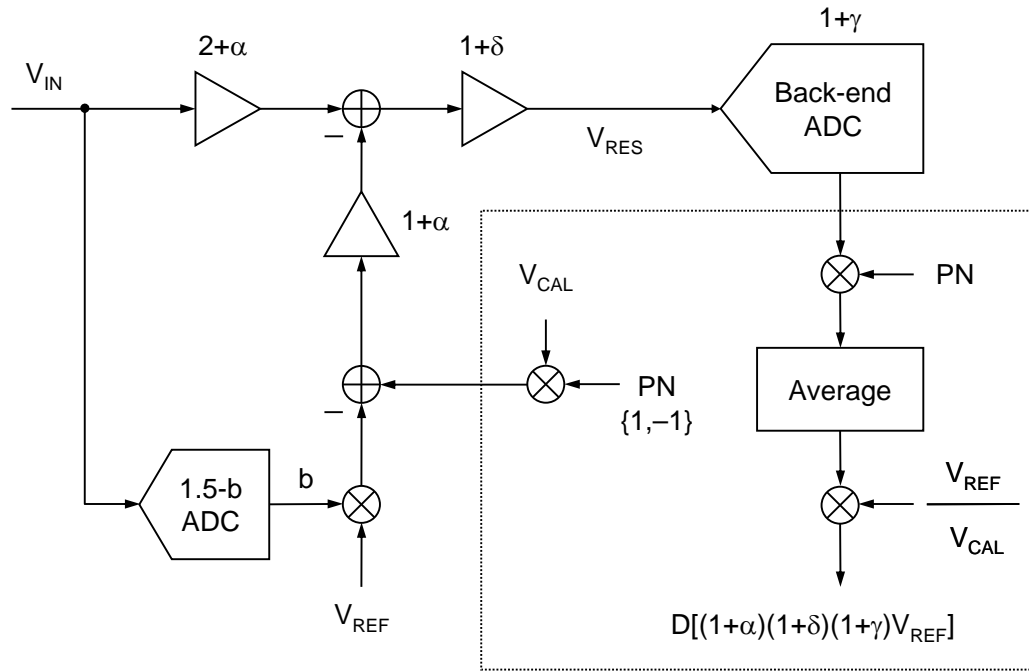
Figure 2.7: Background gain measurement of an MDAC stage.

2.4 Constraints of PN Dithering

The background calibration by PN-modulation or dithering has two constraints. One is the measurement time constraint, and the other is the dither magnitude constraint. The measurement time constraint originates from the tradeoff between the measurement accuracy and the averaging time. Figure 2.8(a) shows the measurement error given by (2.2) after averaging 2^{20} samples, where both V_{IN}/V_{CAL} and V_{REF} are set to 1. The simulation is repeated 1000 times with a 2 V_{pp} sinusoidal input. In the output

histogram, 99% of the measurement errors are smaller than 2^{-10}, which is a 10-b

accuracy. Figure 2.8(b) demonstrates the relation between the measurement accuracy

and the numbers of samples averaged. Note that four times more samples should be

averaged to get one more bit of measurement accuracy. This is true if the

PN-modulated V_{IN}/V_{CAL} in (2.2) is treated as a white noise since the standard

deviation of a white noise is reduced by the square root of 2 as the number of

averaging samples is doubled. The result in Figure 2.8(b) implies that 2^{30} samples

should be averaged for 15-b accuracy, and it takes almost one minute to complete one

measurement if the ADC works at 20 MS/s.
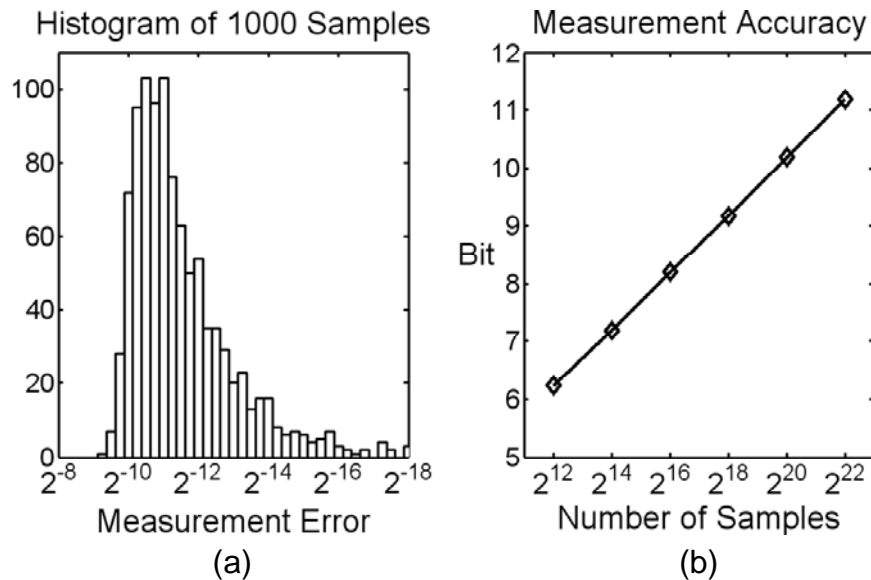
Figure 2.8: (a) Histogram of measurement error after averaging 2^{20} samples. (b)
Measurement accuracy vs. number of samples averaged.

The dither magnitude constraint results from the tradeoff between the dither magnitude and the signal range. Figure 2.9(a) explains the dither magnitude constraint with a large PN-modulated dither, where the full scale is normalized from -1 to 1. The signal range is reduced accordingly to keep the total signal plus dither within the full-scale range. This leads to the reduction of the effective number of bit (ENOB). The signal range reduction is not desirable in a system where the signal-noise ratio (SNR) is dominated by the thermal noise. For example, switched-capacitor circuits will need capacitors of twice the size to suppress the kT/C noise by 3 dB, thus resulting in a significant area and power penalty. Although a smaller dither, as shown in Figure 2.9(b), makes the signal range larger, it takes much longer time to achieve the same accuracy since the ratio of V_{IN}/V_{CAL} in (2.2) is large. This relation between the signal range and the measurement time makes it even more difficult to find a solution that satisfies both constraints.
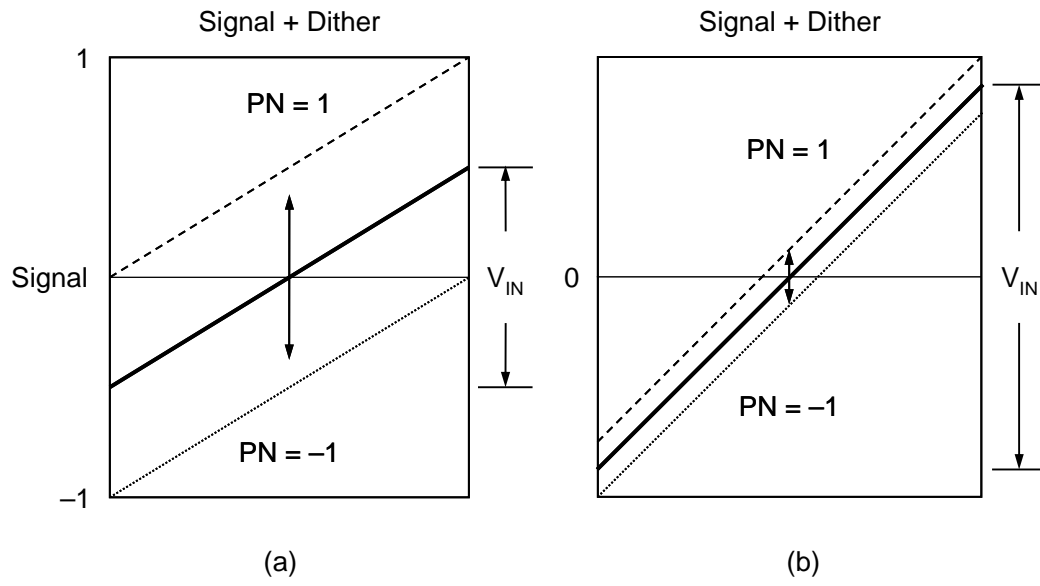
Figure 2.9: Fixed-magnitude PN dithering. (a) Large dither. (b) Small dither.

Chapter 3

A 15-b linear, 20-MS/s Pipelined ADC Digitally Calibrated with Signal-Dependent Dithering

3.1 Introduction

A signal-dependent dithering scheme is proposed to overcome these measurement time and dither magnitude constraints present in the previous fixed-magnitude PN dithering. In the signal-dependent dithering [20], dithers of different magnitudes are selectively used depending on the signal level so that the signal-to-dither ratio can be minimized, and thereby both constraints are significantly relieved. When applied to a 1.5-b/stage pipelined ADC, the inter-stage gain error of the standard tri-level MDAC is measured with 15-b accuracy within a practical number of measurement cycles of 2^{26}. Dither is injected by adding two comparators

and splitting the unit capacitor into two in each pipeline stage. The proposed digital background calibration method calibrates all gain errors resulting from capacitor mismatch, finite opamp gain, and other sources in one step with no strict requirements imposed on analog components and without using digital multipliers or dividers [5]−[8].

Section 3.2 and Section 3.3 present the proposed signal-dependent dithering scheme and the modified tri-level MDAC, respectively. The background calibration technique used in this design is explained in Section 3.4. Section 3.5 discusses the circuit implementation, and the experimental results are summarized in Section 3.6.

3.2 Signal-Dependent Dithering

A signal-dependent dithering scheme is proposed to relieve both the measurement time and dither magnitude constraints. The dither magnitude is adjusted depending on the signal level. For example, the signal is divided into three sub-ranges as shown in Figure 3.1(a). A dither of $+2/3$ or $-2/3$ is injected depending on the PN value in the middle range. When the signal is higher than $+1/3$, no dither is injected if PN = 1, but a dither of $-4/3$ is injected if PN = -1. When it is lower than $-1/3$, dithers

of +4/3 and 0 are injected if PN = 1 and −1, respectively. As a result, the signal plus

dither is equivalent to a smaller signal, which is between ±1/3, with a large

fixed-magnitude dither of 2/3 as shown in Figure 3.1(b). This implies that the ratio of

V_{IN}/V_{CAL} in (2) is smaller and the measurement accuracy is higher. That is, the

signal-dependent dithering scheme shortens the measurement time and achieves the

same level of measurement accuracy while permitting a large dither to be injected with

a full-scale signal. Note that the signal-to-dither ratio V_{IN}/V_{CAL} can be further reduced

if the signal range is divided into more sub-ranges. In the signal-dependent dithering,

the PN-correlated component in the output stays constant although different

magnitude dithers are added. In practice, the difference of the outputs for two cases of

PN = 1 and −1 should be generated by the same hardware in order to emulate the

fixed-magnitude PN dithering. The comparator thresholds and the dither magnitudes

should be set properly so that the signal can stay within the full-scale range regardless

of the comparator offsets.
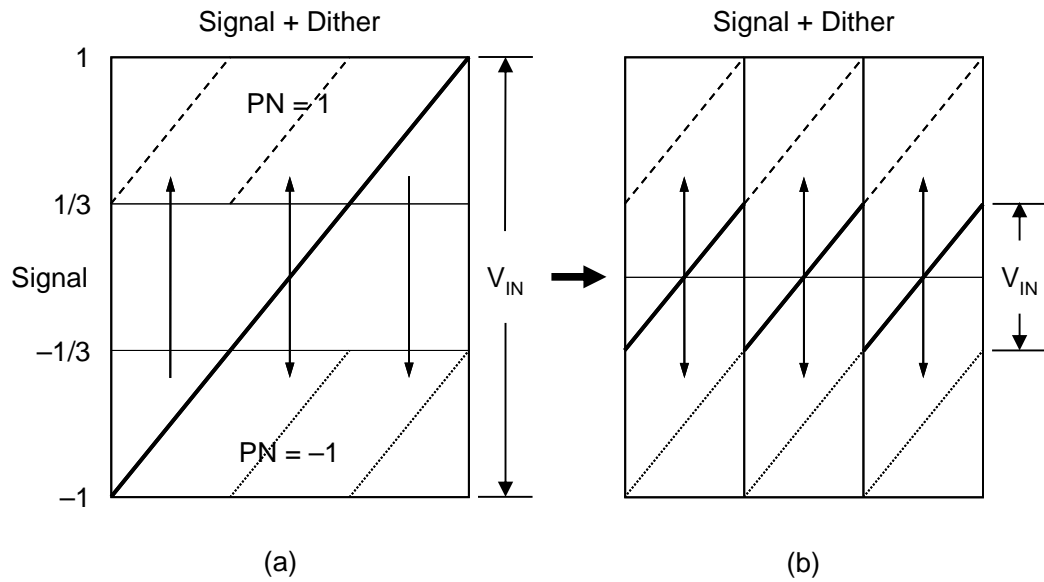
Figure 3.1: Signal-dependent dithering. (a) Three sub-ranges.
(b) Equivalent fixed-magnitude PN dithering.

The benefits of the signal-dependent dithering are apparent if the fixed-magnitude dithering case with a dither of 1/4, which is a compromise between Figure 2.9(a) and Figure 2.9(b), is compared to the signal-dependent dithering case shown in Figure 3.1(a). First, since the dither of 1/4 reduces the signal range to 3/4, the ENOB with Figure 3.1(a) is about 0.5-b better. Second, the ratio of V_{IN}/V_{CAL} decreases from 3 to 1/2 in the signal-dependent dithering. This improves the measurement accuracy further by 2.5 bits. Therefore, the dithering scheme in Figure 3.1(a) gives 3 more bits of accuracy and can shorten the measurement time by $1/4^3$. That is, one measurement cycle that would otherwise take one minute to complete can

now be completed in one second.

The dithering scheme used in [13], [14] is very similar to the proposed signal-dependent dithering. The sub-ADC and sub-DAC resolve one more bit to produce two different residues. Both designs use a multi-bit first stage to achieve a 12-b calibrated resolution. In [13], the inter-stage gain and non-linearity errors are calibrated by detecting the difference between the two residues. In [14], digital outputs are averaged so that the estimated gain and non-linearity parameters can converge after a certain number of steps. The proposed signal-dependent dithering lowers the signal-to-dither ratio by dividing the input range into more sub-ranges, and the inter-stage gain error is measured together. This low signal-to-dither ratio is an important feature when calibrating a high-resolution ADC with a low-resolution first stage. For example, calibrating a 1.5-b first stage requires more accuracy than calibrating a multi-bit first stage. Therefore, a large number of output samples were averaged [9]. Although using a multi-bit first stage can somewhat relax the calibration accuracy requirement, calibrating both multi-bit DAC mismatch and residue amplifier gain error increases the complexity of the calibration algorithm [8], [12].

3.3 Signal-Dependent Dithering for Tri-Level MDAC

Figure 3.3 shows the modified residue plot of a tri-level MDAC for dithering. The comparator thresholds in the sub-ADC are shifted from $\pm 1/4$ V_{REF} to $\pm 3/8$ V_{REF}. Signal-dependent dithers are injected between $\pm 3/8$ V_{REF}, and two more comparators are added with thresholds at $\pm 1/8$ V_{REF}. No dither is injected when signal is high for simplicity. This does not delay the calibration time significantly as will be explained later. A dither magnitude of $-V_{REF}$, $-1/2$ V_{REF}, 0, $+1/2$ V_{REF} or $+V_{REF}$ is chosen depending on the PN values and the signal level as shown in Figure 3.1(a). The comparator thresholds and dither magnitudes are set to have room for comparator offsets. As a result, the signal plus dither between $\pm 3/8$ V_{REF} is in effect a large fixed-magnitude dither of $1/2$ V_{REF} with a small signal within the range of $\pm 1/4$ V_{REF} as shown in Figure 3.3. The signal-to-dither ratio of V_{IN}/V_{CAL} is reduced to $1/2$. By averaging the output samples while the input stays within $\pm 3/8$ V_{REF}, 99% of the measurement errors are smaller than 2^{-14} when 2^{26} samples are averaged. If referred to the input after divided by the residue gain of 2, it corresponds to a 15-b accuracy.

b = −1   b = 0   b = 1

V_{RES}
(V_{REF})

3/4

−3/4

−3/8   3/8
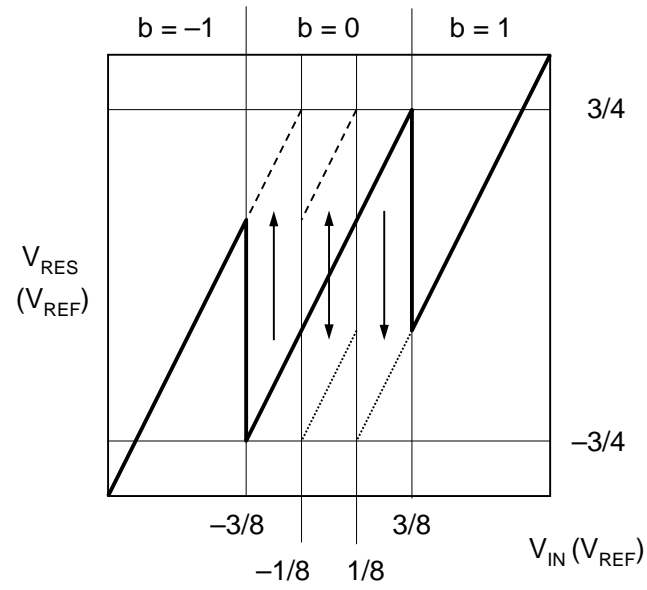
−1/8   1/8

$V_{IN} (V_{REF})$

Signal-Dependent Dithering		
$V_{IN} (V_{REF})$	PN = −1	PN = +1
−1 ~ −3/8	0	0
−3/8 ~ −1/8	0	+ V_{REF}
−1/8 ~ 1/8	−1/2 V_{REF}	+1/2 V_{REF}
1/8 ~ 3/8	− V_{REF}	0
3/8 ~ 1	0	0

Figure 3.2: Modified residue of an MDAC stage for signal-dependent dithering.
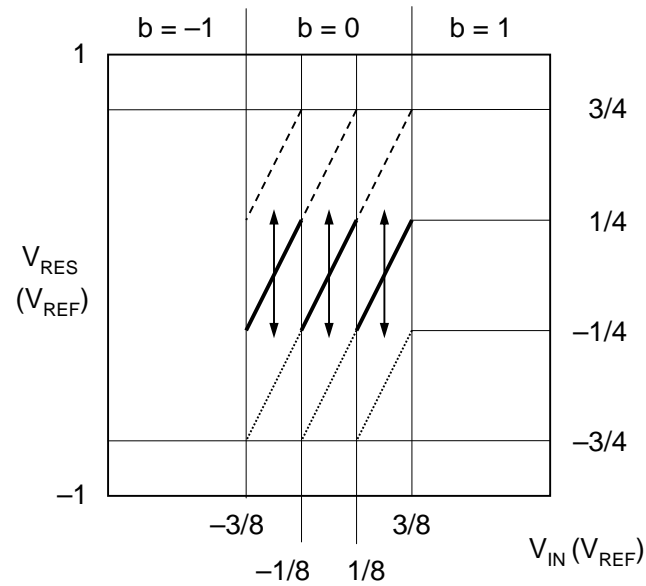
Figure 3.3: Equivalent fixed-magnitude PN dithering of modified MDAC stage.

The standard tri-level MDAC modified for signal dependent dithering by adding two more comparators and splitting a capacitor into two is shown in Figure 3.4. Dithers are injected by controlling the switches according to the comparator outputs and PN values. Both C1 and C2 are switched between $-V_{REF}$ and 0 for the signal range from $-3/8$ to $-1/8$ V_{REF}, and between 0 and $+V_{REF}$ for the signal range from $+1/8$ to $+3/8$ V_{REF} if PN is 1 and -1, respectively. When the signal lies in the middle range, C1 and C2 are alternately switched to $-V_{REF}$ if PN= 1 and $+V_{REF}$ if PN= -1 to inject a dither of 1/2 V_{REF} equally through two capacitors. The mismatch between the two split capacitors contributes to noise after randomized and spread over the Nyquist band.

However, it is below the noise level of the system and is not subtracted digitally in this design.
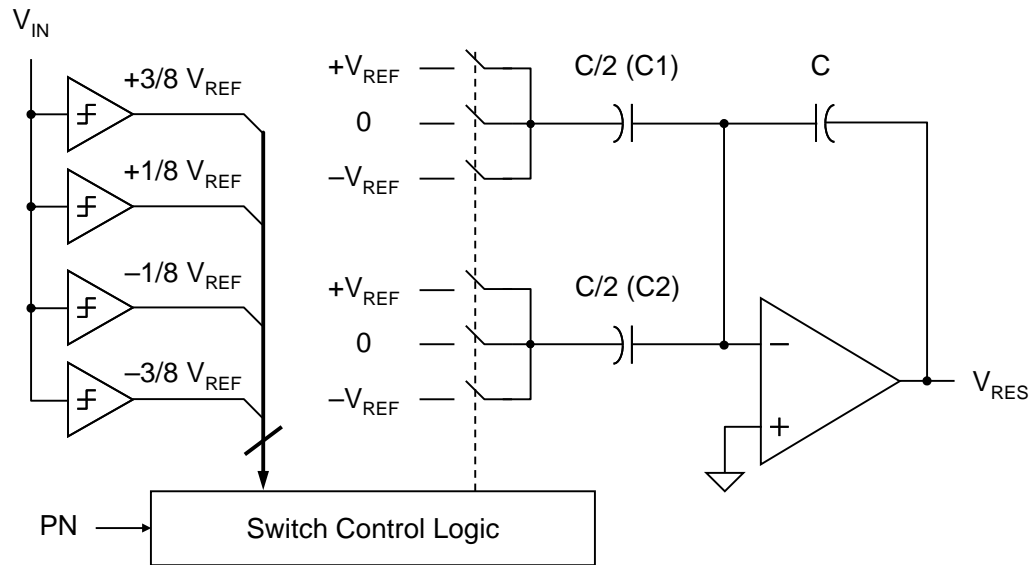
Figure 3.4: MDAC residue amplifier for signal-dependent dithering.

The proposed tri-level MDAC shown in Figure 3.4 has the following features:

(1) Large dithers are used without sacrificing the signal range. (2) The signal de-correlation time is greatly shortened due to the low signal-to-dither ratio, V_{IN}/V_{CAL}.

(3) No additional capacitor is used for dithering, and the analog performance is not affected. (4) Switch control logic does not delay opamp settling. (5) Two more comparators are added in each pipeline stage.

One major concern regarding the proposed signal-dependent dithering scheme

in Figure 3.3 is that the calibration time varies with the signal condition since no dither

is injected when the signal is high. Dithering for the full-range signal is possible as

shown in Figure 3.5 with additional comparators added. For example, if the signal is

larger than +5/8 V_{REF} and PN $= -1$, the residue can be $2 V_{IN} -2 V_{REF}$ although an

additional capacitor or a reference voltage of $2 V_{REF}$ should be used for that.
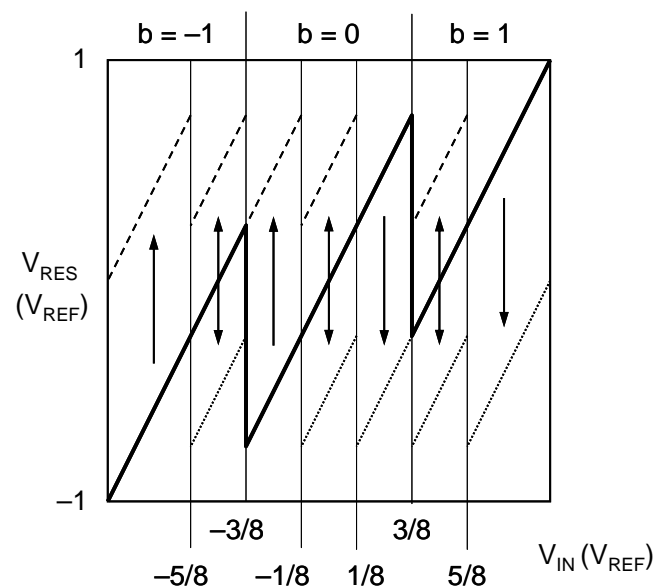
Figure 3.5: Modified residue of an MDAC stage restored to full signal range dithering.

However, numerical analysis of the calibration time based on the proposed

scheme shown in Figure 3.3 indicates that only the dithering of the first stage is

sensitive to the input condition while the later stages are not because the inputs of the

later stages are randomized by the previous stages. The proposed signal-dependent

dithering still offers a substantial saving in the measurement time with low circuit complexity unless the signal stays at a high level all the time. It is noted that the residue plot shown in Figure 3.3 is similar to the residue plot used in [11] except for the range between $\pm 1/8$ V_{REF}. However, in [11], dither is injected before the sub-ADC by randomizing the comparator thresholds. The signal-to-dither ratio is still high since all output samples are averaged. A two-channel ADC architecture is used to cancel the PN un-correlated input signal, and therefore, it introduces the mismatch problem between the two channels.

3.4 Background Digital Calibration

The pipelined ADC with the proposed calibration scheme is illustrated in Figure 3.6. The DV_{REF}'s are adjusted to match the analog V_{REF}'s added/subtracted in the MDAC stages. In this example, the dither is injected into the stage2 and subtracted digitally from the signal path. The digitized residue of the stage2 is PN-correlated and then multiplied by V_{REF}/V_{CAL} to measure and update the DV_{REF2} as drawn with the thick lines. The calibration proceeds from the rear stages to the front repeatedly in order to measure errors with the calibrated back-end ADC. All multipliers in Figure

3.6 are implemented with adders and shifters. The digital circuitry for the PN

correlation is shared by all stages.
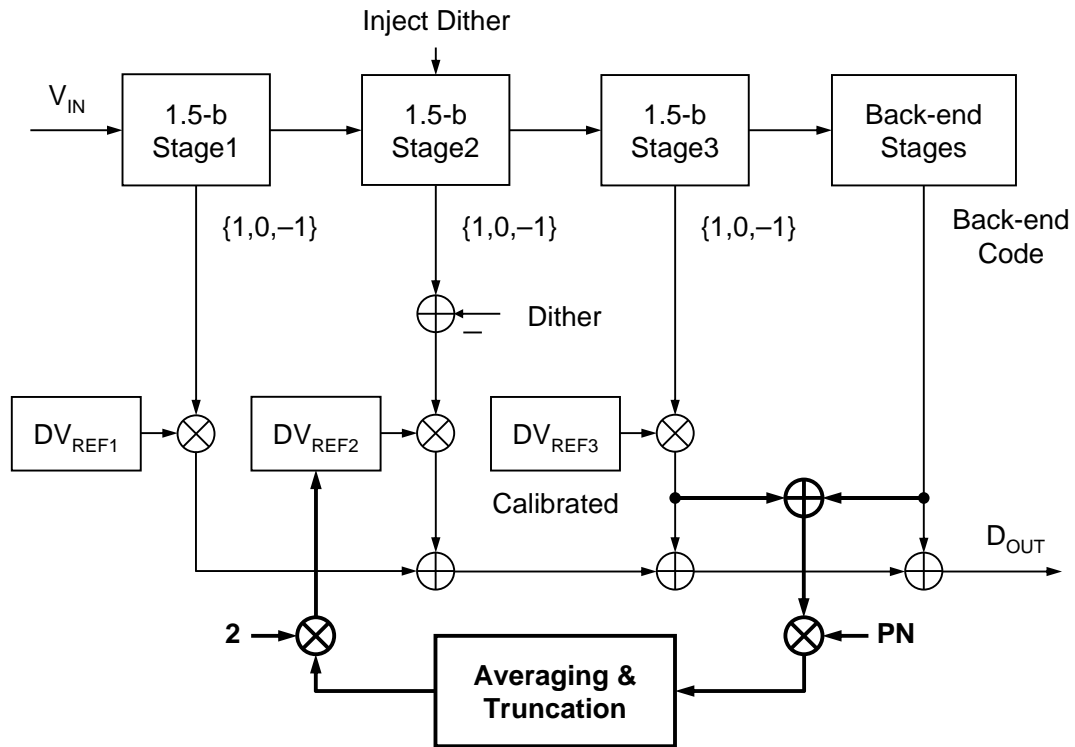
Figure 3.6: 1.5-b/stage pipelined ADC calibrated with dithering.

Since the non-ideal effects in the back-end stages are less critical, the

calibration accuracy in the later stages can be lowered gradually to shorten the

calibration time. The un-calibrated back-end ADC can be modeled as a linear ADC

with a gain error. Offset has no effect on the error measurement since the offset

becomes a white noise after it is spread by the PN sequence. In system simulations

including all circuit non-idealities such as capacitor mismatch, finite opamp gain, and

comparator and opamp offsets, the calibration achieves an SNDR of 96 dB and an

SFDR of 114 dB by averaging 2^{26} samples per stage.

3.5 Circuit Implementation

3.5.1 ADC Architecture

The proposed ADC has one S/H, 14 1.5-b stages, and a 3-b flash as shown in

Figure 3.7. The digital output is 16-b with a redundant bit to reduce the digital

truncation error. The comparator outputs in each stage are connected to the digital

logic. The digital encoding, digital correction, digital calibration, and also the PN

sequence generator functions are all integrated in the digital logic. It provides each

pipeline stage with the PN value and the calibration enable signal.
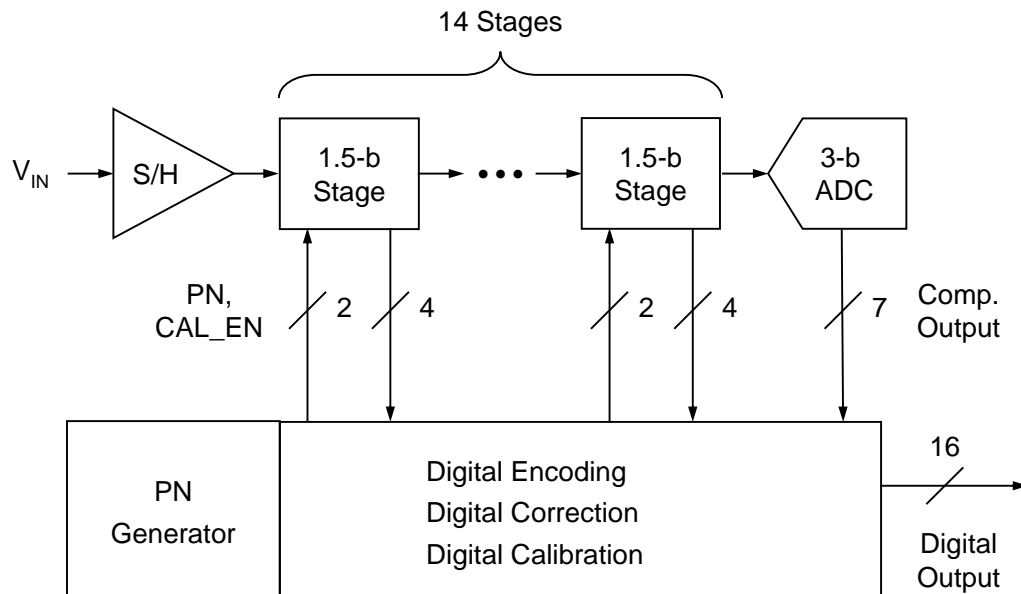
Figure 3.7: ADC block diagram with digital calibration.

3.5.2 Operational Amplifier

Since all gain errors in the signal path can be simultaneously calibrated with the proposed calibration method, the circuit implementation should ensure that all components are linear enough to achieve high SFDR. Figure 3.8 shows the opamp used in both the S/H and MDAC. A 2-stage Miller-compensated opamp is chosen for a large output swing. The opamp gain is designed to be high enough to neglect its non-linearity but not to slow down its speed since the finite opamp gain error can be calibrated. The length of NMOS transistors in the signal path is minimized to meet the

high-speed requirement. Simple boosting amplifiers are added to compensate for the

gain reduction due to the short channel effect. The length of PMOS transistors is

chosen to be longer than the minimum length for high output resistance. Simulation

results show that the gain of this opamp is 95 dB. The flip-around S/H is used in this

design, and the tri-level MDAC is modified for dithering as shown in Figure 3.4. The

S/H and MDAC have simulated loop gains of 94 dB and 87 dB, respectively, and

achieve16-b linearity with a 2-V_{pp} input signal. The simulated closed-loop bandwidths

of the S/H and MDAC are 360 MHz and 300 MHz, respectively. They are designed

high enough to settle with 16-b accuracy at 50 MS/s. Note that the MDAC settling

error is also calibrated if it is linear, and fast settling is not necessary if the settling

behavior is purely exponential with a fixed time constant without any slew limit.
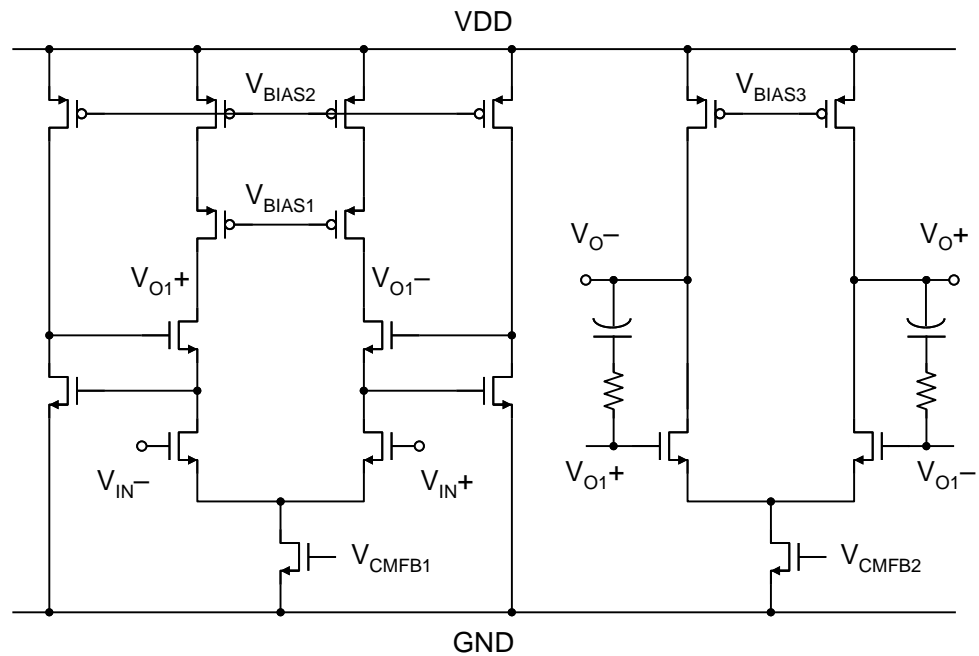
Figure 3.8: Operational amplifier for S/H and residue amplifier.

3.5.3 Switch

Bootstrapped switches [30] are used in the signal path. In high-speed circuits,

as switch gets larger, the amount of charge injection increases. The bootstrapped

switch provides a lower and more linear on-resistance, and contributes to a smaller

and more linear signal-dependent charge injection, which can be also calibrated along

with the gain error. Its parasitic capacitance is mainly the junction capacitance since its

boosted gate voltage follows the drain and source voltages. The drawback is that it

needs a large capacitor to boost its gate to a high voltage. Therefore, only the switches

in the S/H stage in this design use a large boosting capacitor to achieve high linearity while the switches in the MDAC are boosted with smaller capacitors.

3.5.4 Digital Logic

In the digital circuits, 2^{26} samples are averaged to guarantee a calibration accuracy of a 15-b level as discussed. No measurement accuracy is scaled for later stages in this design for simplicity. The word length of the DV_{REF}'s is 21 bits so that the accumulated truncation error can be smaller than the measurement error.

3.6 Experimental Results

The prototype chip is fabricated in a 0.18-µm CMOS process. The die photograph shown in Figure 3.9 occupies an active area of 2.3 x 1.7 mm^2. The digital calibration algorithm is fully implemented on the prototype chip. The digital logic occupies 0.6 mm^2. The area only for calibration is smaller than that since the digital area also includes the digital encoding and digital correction functions. The sampling capacitors in the S/H and stages 1 ~ 4 are set to 2 pF, and the kT/C noise limits the SNR of the ADC to be −76 dB. Stages 5 ~ 14 are scaled down by half to save chip

power and area. The highly-linear differential sinusoidal input is obtained by using a synthesized signal generator followed by a band-pass filter and a single-ended-to-differential converter. The clock signal is generated by a low-jitter pulse generator.
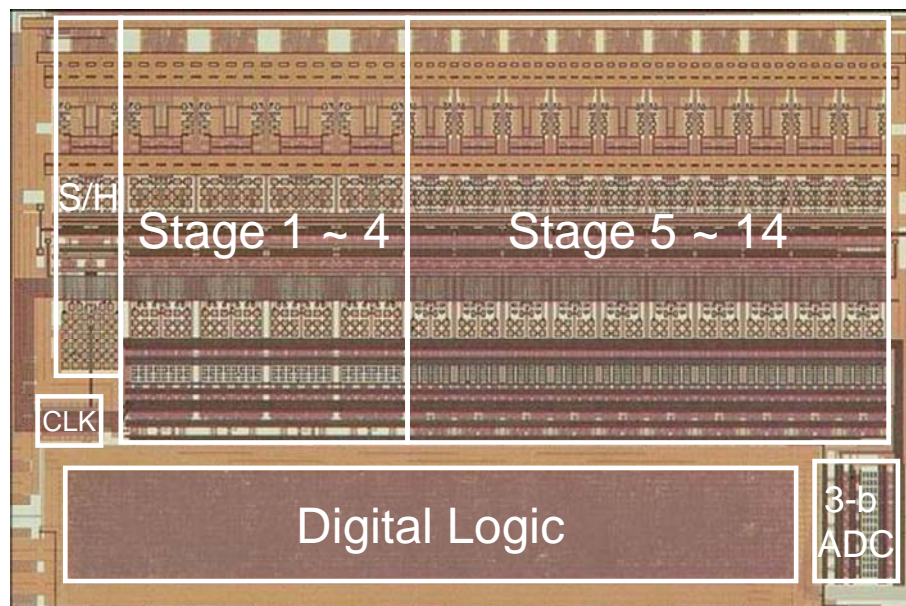
Figure 3.9: Die photograph.

Figure 3.10 shows the measured INL at a 15-b level before and after calibration measured at 20 MS/s. The INL error jumps significantly at the comparator threshold points before calibration. The largest INL jump is from the first stage. After the first 6 stages are calibrated, the INL errors are greatly reduced and improved from

25 LSB to 1.3 LSB.
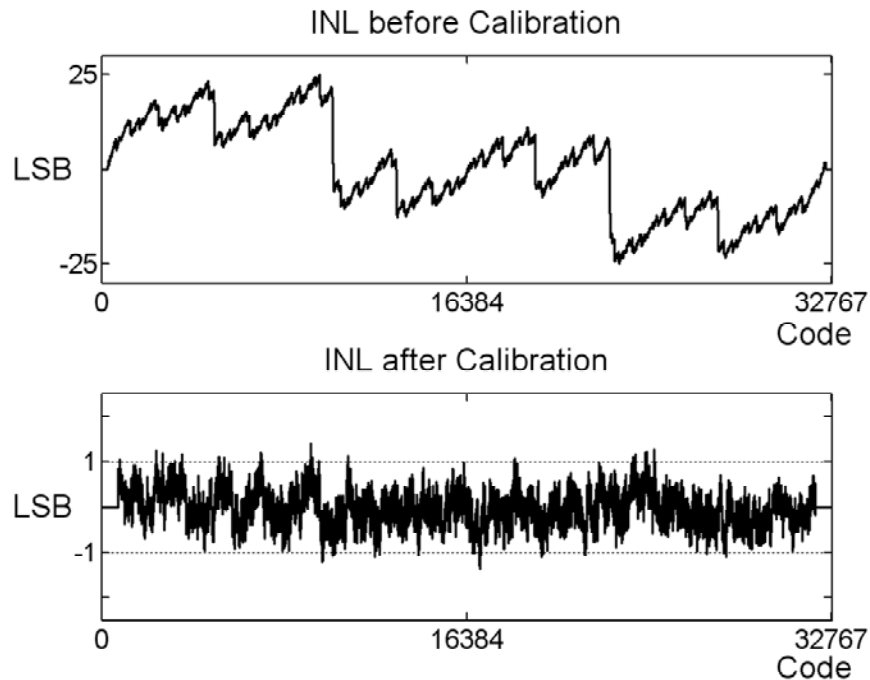
Figure 3.10: Measured INL at 15-b level.

Figure 3.11 shows the FFT spectrum of a 14.5-MHz input sampled at 20 MHz. The SFDR, total harmonic distortion (THD), and SNR, before calibration, are 69 dB, −67 dB, and 61 dB, respectively. The ENOB is about 10 bits. After calibration, the SFDR, THD, and SNR are improved to 98 dB, −92 dB, and 71 dB, respectively. The ADC linearity is improved to 15 bits while the SNDR is mainly limited by the kT/C noise. Experimental results imply the clock jitter is less than 2 psec.
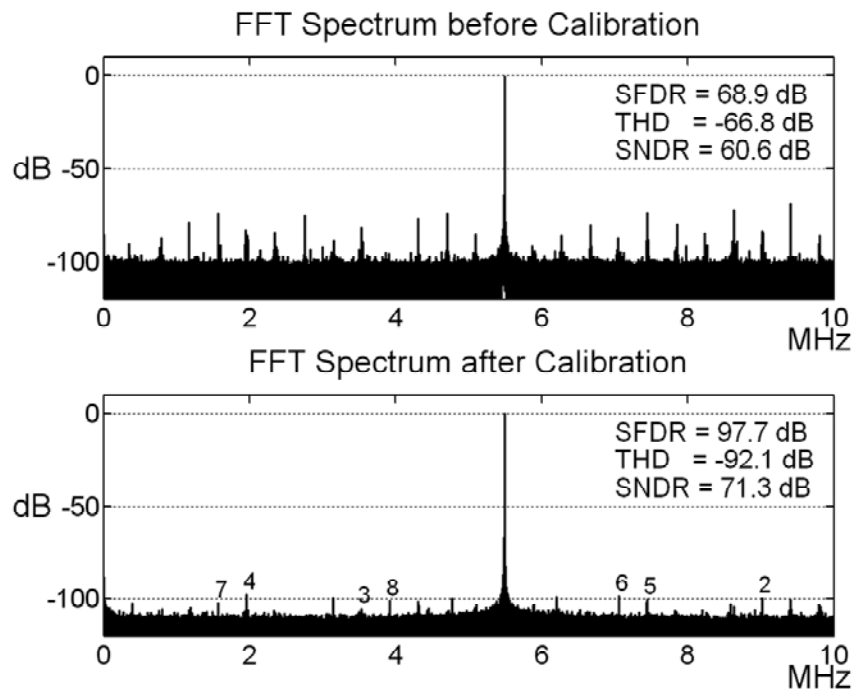
Figure 3.11: Measured FFT spectrum with 14.5-MHz input @ 20 MS/s.

It takes 45 sec to calibrate the first 6 stages while averaging 2^{26} samples per stage with a full-scale sinusoidal input at 20 MS/s. The calibration time is reduced to 38 sec if the input is uniformly distributed over the full signal range since the sinusoidal signal gives less number of samples at low signal levels. If the calibration is performed without input, it takes 20 sec to average 6×2^{26} samples at 20 MS/s. Note that this calibration time difference is not significant, considering the fact that the number of samples required to average grows exponentially if the signal-to-dither ratio is higher. The calibration time can be further saved by gradually scaling down the

measurement accuracy. For example, by scaling 0.5-b accuracy per two stages, it can be reduced to 24 sec with a random input. Higher sampling rate is also effective in shortening the calibration time.

Figure 3.12(a) shows the ADC performance at 20 MS/s with varying input frequencies up to 14.5 MHz. The SFDR and THD stay constant at about 95 dB and −90 dB, respectively. The peak SNDR reaches 73 dB with 1-MHz input. Figure 3.12(b) shows the ADC performance with varying sampling frequencies up to 50 MS/s. The SFDR stays higher than 95 dB up to 20 MS/s and starts to degrade slightly beyond 30 MS/s. The conversion rate in the measurement is mainly limited by the kick-back and charge-injection when switching the input sampling capacitor because the bonding wire inductance of the test package is larger than expected. As a result, measurements at a higher sampling rate of 50 MS/s are limited to 12 b.
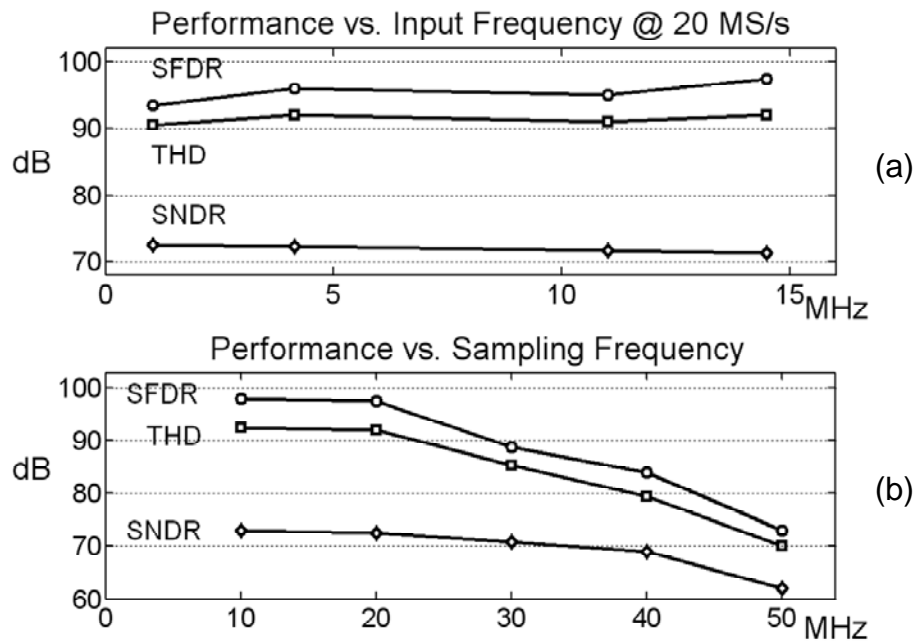
Figure 3.12: (a) Measured performance vs. input frequency sampled @ 20 MS/s.
(b) Measured performance vs. sampling frequency.

The measured performance at 20 MS/s is summarized in Table 3.1, where a

comparison with a digitally-calibrated 1.5-b/stage pipelined ADC [9] is included. The

previous work loses 25 % of the signal range and averages 2^{31} samples per stage. It

took 8.95 minutes to calibrate 5 stages at 20 MS/s while achieving less calibration

accuracy than this work. The proposed signal-dependent dithering exhibits a clear

advantage in both calibration accuracy and time. The digital logic of this work

consumes 5 mW. Assuming that the digital power consumption is proportional to the

sampling frequency and supply voltage, the digital power for calibration of this

prototype is lower than that of [8], [9], which are also calibrated digitally in the

background to 15-b linearity using on-chip digital logic.

Table 3.1: Summary of Measured Performance and Comparison with State-of-Art

	This Work	JSSC '05
Technology	0.18-μm CMOS	0.25-μm CMOS
Supply Voltage	1.8 V	2.5 V
Resolution	15 b	15 b
Conversion Rate	20 MS/s	40 MS/s
Signal Range	2 V_{pp}	3/4 x 2.1 V_{pp}
Equivalent Dither Magnitude	±1/2	±1/8
Average Samples	6×2^{26}	5×2^{31}
Calibration Time @ 20 MS/s	45 sec.	8.95 min.
INL @ 15-b	1.3 LSB	2 LSB
SFDR	98 dB	93.3 dB
THD	−92 dB	
Peak SNDR	73 dB	73.5 dB
Active Area	2.3 x 1.7 mm^2	3.8 x 3.6 mm^2
Digital Area	0.6 mm^2	1.5 mm^2
Power Analog/ Digital	275/5 mW	350/20 mW

3.7 Summary

A digital background calibration scheme with signal-dependent dithering is applied to a 1.5-b/stage pipelined ADC based on the standard tri-level MDAC pipeline stage. This technique allows the injection of a large dither without reducing the signal range while keeping the signal-to-dither ratio low. The proposed method calibrates all gain errors resulting from capacitor mismatch, finite opamp gain, and other sources in one step with no strict requirements imposed on analog components. It overcomes both the measurement time and dither magnitude constraints found in the fixed-magnitude PN dithering schemes. Highly accurate calibration up to above 15-b resolution is demonstrated to be feasible within a practical amount of time without paying significant penalty in circuit complexity and die area.

3.8 Acknowledgement

Chapter 4

A 10~15-b, 60-MS/s Digitally Calibrated Floating-Point ADC

4.1 Introduction

A floating-point architecture offers an alternative way to quantize a signal with a high resolution using a standard ADC [31]–[36]. In applications such as imagers, high resolution is not required to quantize mostly white or bright levels, but to resolve dim or dark levels, extremely high resolution and monotonicity are needed. One common approach to enhance the dynamic range is to use a variable gain amplifier (VGA) [33]–[35]. It amplifies the input within different magnitude ranges to full scale before A/D conversion. Thereby, the equivalent quantizer resolution is higher when input is smaller. It is desirable if the front-end VGA gain can be instantly set

depending on the magnitude of the sampled input [33], [34] rather than responding slowly due to the servo gain feedback [35], [36]. A switched-capacitor VGA can switch the gain quickly as the signal magnitude changes and can achieve a high data rate [34]. However, it suffers from capacitor mismatch, finite opamp gain, and opamp offset. The gain and offset errors in the different gain ranges cause non-monotonicity or missing codes at the boundaries where the VGA gain switches [37], [38]. This work describes a 10~15-b FADC, where the VGA offset and gain errors are digitally calibrated in the background. Signal-dependent dithering is used to shorten the calibration time without sacrificing the signal range. A modified clock scheme avoids using an S/H stage and lead to a lower noise floor. The sampling rate reaches 60 MHz as the IC packaging strategy is improved from the design described in Chapter 3.

After reviewing the floating-point architecture in Section 4.2, the switched-capacitor VGA is described in Section 4.3. Section 4.4 introduces the background digital offset and gain calibration schemes. The signal-dependent dithering for the VGA is presented in Section 4.5. Section 4.6 covers the circuit implementation, and the experimental results are summarized in Section 4.7.

4.2 Floating-Point Architecture

Figure 4.1 shows a concept of a 10~15-b FADC example with a VGA and a digital divider. The VGA partitions the input into several ranges and amplifies the input signal in each range to the full scale level of a 10-b ADC. The divider restores the correct digital output which is amplified by the VGA. The VGA has a total of six gain values: 1, 2, 4, 8, 16, and 32 to make a 5-b exponent. The 10-b mantissa is the output of the 10-b ADC. When the gain is set to 1, the 10-b ADC takes the same range as the input. Therefore, in this lowest gain setting, the resolution is 10-b. On the other hand, when all gains are set high, the input is amplified by a gain of 32, and the resolution is enhanced by 5 b (2^5) to 15-b.

In practice, the boundaries of the input ranges should be set properly so that the amplified input always stays within the ADC input range regardless of the comparator offset variations. Also, an opamp with a very high open-loop bandwidth is required in the switched-capacitor amplifier to achieve a VGA gain as large as 32.

Analog VGA

| V_IN | x1, x2, x4,
x8, x16, x32 | 10-b
ADC |

Digital Divider

| $\dfrac{1}{1,2,4,8,16,32}$ | D_OUT |

15 b

VGA Output

15b FADC Output

Gain Range

x1 : x x x x x x x x x x 0 0 0 0 0
x2 : 0 x x x x x x x x x x 0 0 0 0
x4 : 0 0 x x x x x x x x x x 0 0 0
x8 : 0 0 0 x x x x x x x x x x 0 0
x16 : 0 0 0 0 x x x x x x x x x x 0
x32 : 0 0 0 0 0 x x x x x x x x x x

10 b

15 b

Digital Output
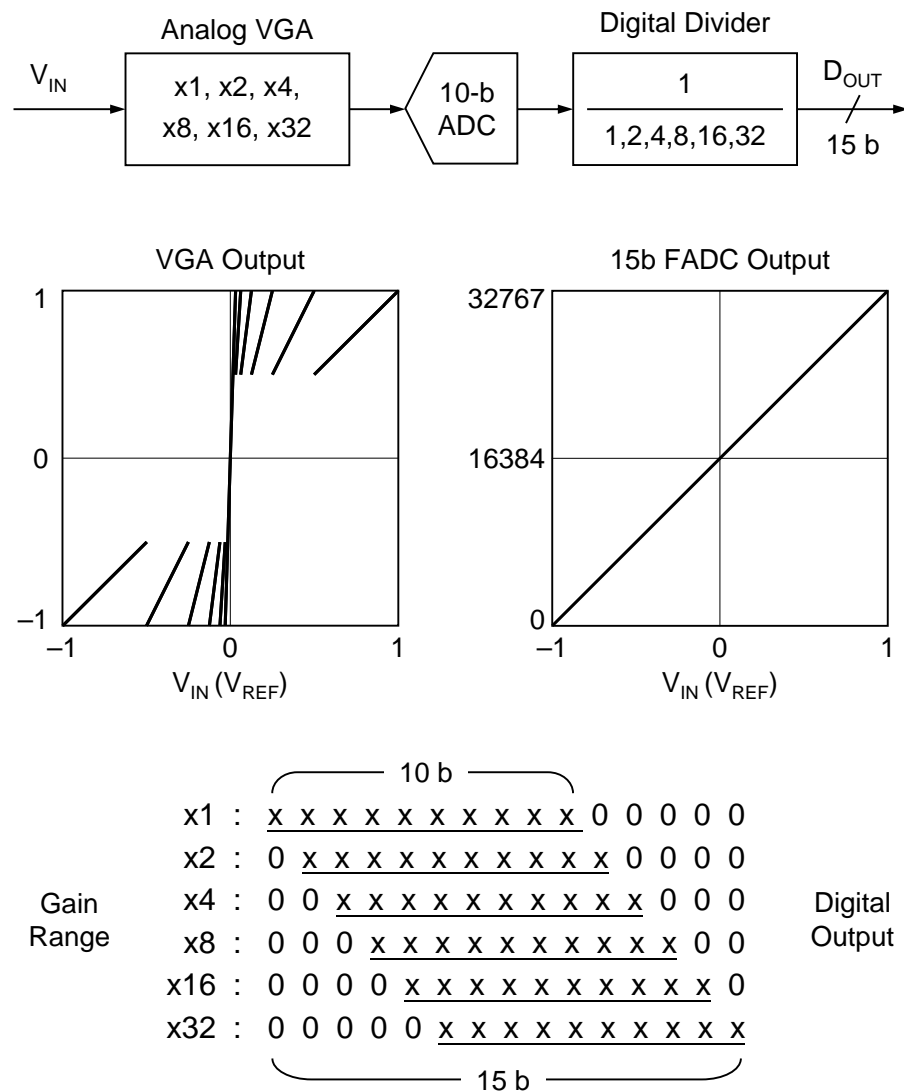
Figure 4.1: 10~15-b FADC architecture

4.3 Switched-Capacitor VGA Stages

Figure 4.2 shows a VGA divided into three cascaded stages to reduce the

comparator offset and opamp bandwidth requirements [34]. In the first two gain stages,

the gain is switched between 4 and 1 when the input level crosses the boundaries at

±0.2V_REF. Similarly, the third stage has two gain settings of 2 and 1 switched at

±0.4V_REF.
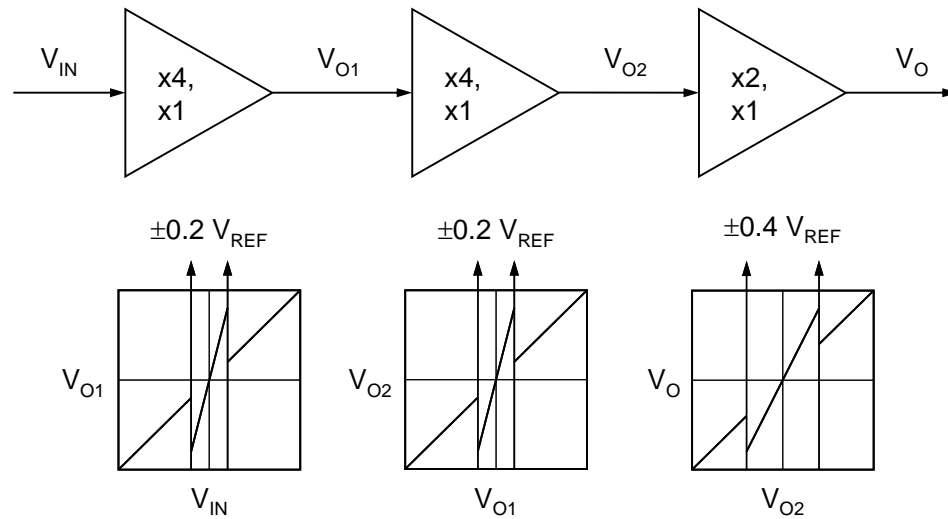
Figure 4.2: Cascaded VGA stages.

The VGA gain values of 1, 2, 4, 8, 16, and 32 are the combinations of gains

obtained by the three cascaded stages as shown in Table 4.1.

Table 4.1: VGA Gain Combinations

Gain	1	2	4	8	16	32
VGA1	x 1	x 1	x 4	x 4	x 4	x 4
VGA2	x 1	x 1	x 1	x 1	x 4	x 4
VGA3	x 1	x 2	x 1	x 2	x 1	x 2

The overall VGA residue plot and the VGA gain ranges are shown in Figure 4.3. With three cascaded stages, the requirement on the comparator offset is relaxed from ± 0.00625 to ± 0.05 V_{REF}, and the required opamp bandwidth is reduced by 1/8. The relaxed requirements also reduce the total power consumption although the VGA is implemented with three stages.
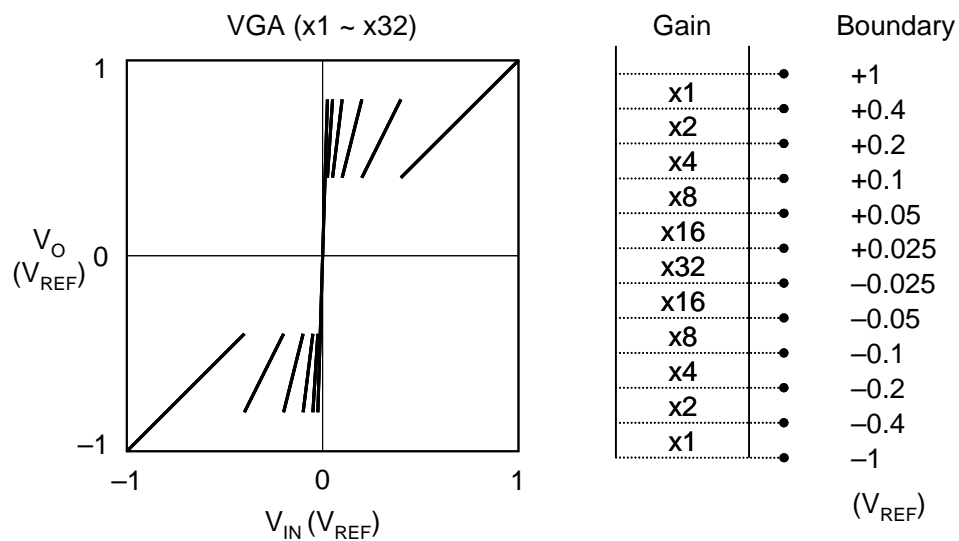
Figure 4.3: VGA residue plot and gain ranges.

Similar to the MADC in a pipeline ADC, a switched-capacitor VGA suffers from the gain error resulting from capacitor mismatch and finite opamp gain. Besides, the offset in a VGA stage varies with different gain settings while the MDAC has a

constant output offset. Figure 4.4 illustrates the non-linearity of an FADC caused by the VGA gain and offset errors [37]. The VGA in Figure 4.4 has different gain errors of ε_1 and ε_2 and offsets of V_{OS1} and V_{OS2} as the gain is set to 1 and 2, respectively. After dividing the VGA gain digitally, large step errors occur at the gain-range boundaries. The step errors cause missing code or non-monotonicity and degrade the linearity of the FADC. In this work, these step errors are digitally calibrated in the background. Once calibrated, the FADC linearity is only limited by the back-end ADC.
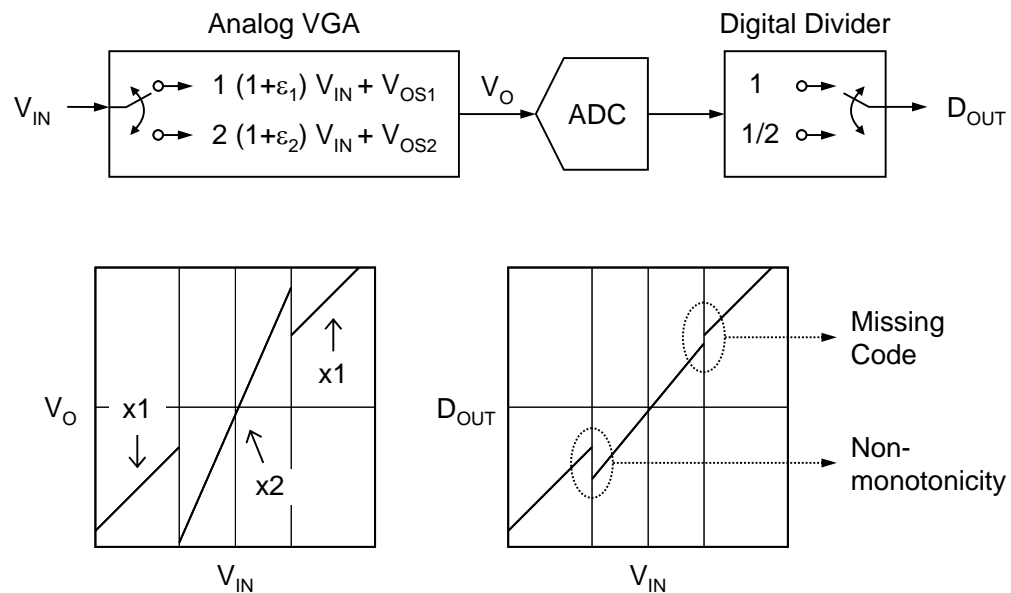
Figure 4.4: VGA gain and offset errors.

4.4 Background Digital Calibration

4.4.1 Background Offset Calibration

Figure 4.5 shows the principle of background offset calibration. The non-ideal effects of a VGA stage are modeled by a gain error ε plus an offset V_{OS}. The offset is measured by chopping the input with a zero-mean pseudo-random pulse sequence PN_O and averaging the output [39]. The input V_{IN} is translated into a noise, which approaches zero after a large number of samples are averaged. The output signal is then subtracted by the measured offset and chopped by the same PN_O again to restore the input signal.
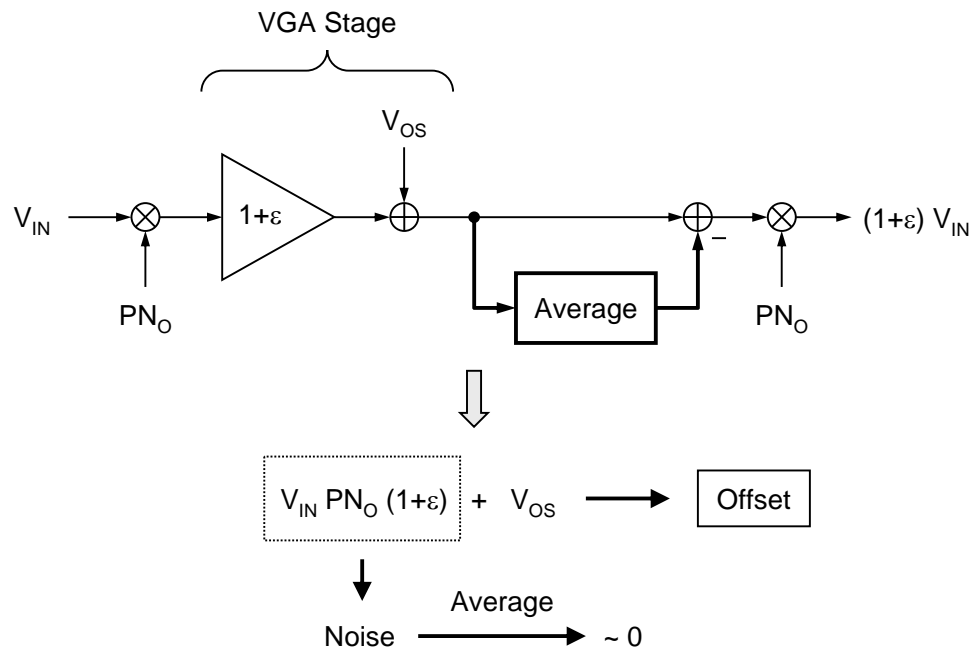
Figure 4.5: Background offset calibration.

4.4.2 Background Gain Calibration

The principle of background gain calibration is presented in Figure 4.6. Similar to the gain measurement scheme described in Section 2.3.2, the gain error, $1+\varepsilon$, is measured by injecting a PN_G-modulated calibration signal, V_{CAL}, into the signal path. After correlating the output with the same PN_G and multiplying by V_{REF}/V_{CAL}, the value of $(1+\varepsilon)$ is obtained as shown with the thick lines. The dither is subtracted from the output, and the gain error is corrected after the signal is multiplied by $1/(1+\varepsilon)$.
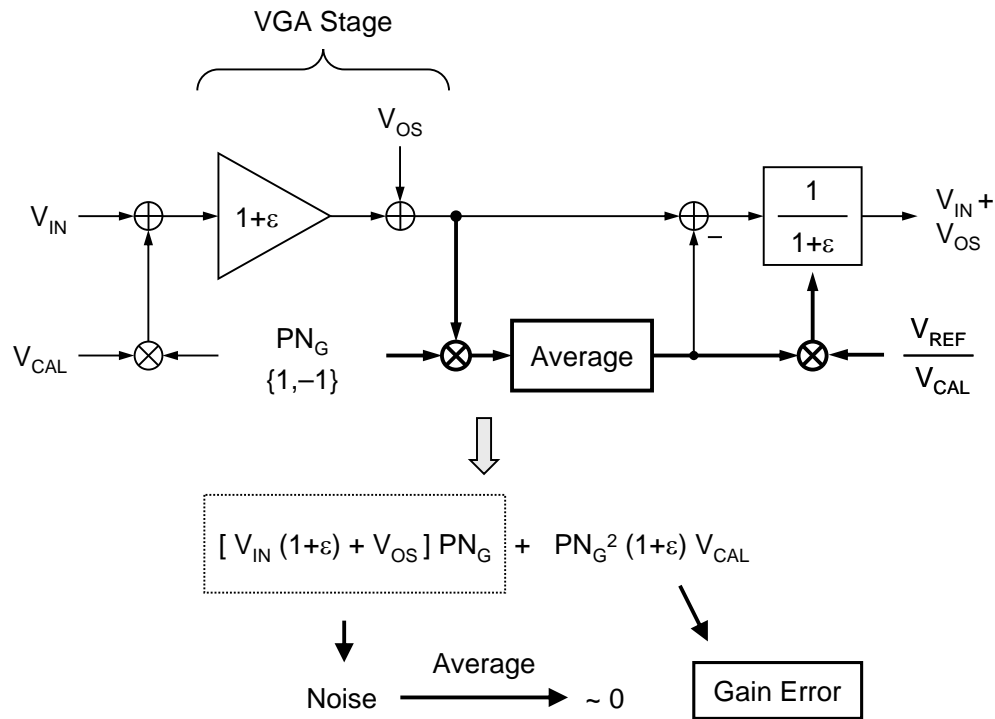
Figure 4.6: Background gain error calibration.

Note that the step error in a pipeline stage described in Chapter 3 is calibrated by only shifting the digital output since the signals in all ranges have the same gain error. In a VGA stage, the gain error changes with the gain setting. Gain correction is needed to linearize the FADC transfer function so that the signals in different range have the same gain. Ideally, the remaining gain error is zero after calibration. However, in practice, if V_{CAL} is not accurately generated and has an error of $(1+\gamma)$, it leads to an overall slope change of $1/(1+\gamma)$, but this doesn't affect the FADC linearity. Compared to a pipeline stage, a precise V_{CAL} is critical to calibrate the step error accurately.

4.4.3 Calibration of a VGA stage

Figure 4.7 shows a digital-calibrated VGA stage. Assume that the VGA and the back-end ADC have gain errors of α and β, respectively, and have an offset of V_{OS}. The offset error is measured by chopping the input by PN_O, and the gain error is measured by injecting a PN_G-modulated dither, V_{CAL}, into the signal path. The offset and V_{CAL} components are then removed from the output, and the signal is divided by $G(1+\alpha)(1+\beta)$ and chopped by PN_O again. The digital divider can be realized with a multiplier by approximating the divider ratio of $1/(1+\varepsilon)$ by $(1-\varepsilon)$ to simplify the digital logic and reduce chip area [8].
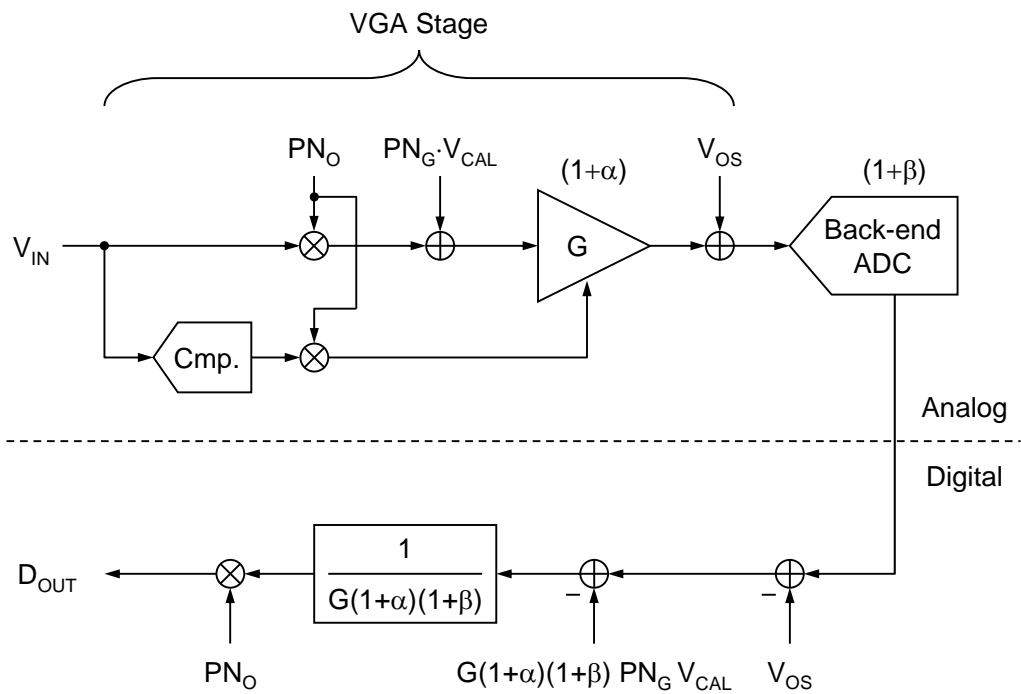
VGA Stage

Figure 4.7: Digital-calibrated VGA stage.

As the VGA gain varies with the signal magnitude, the errors in the different gain ranges are measured separately using individual digital accumulators to average the output samples. To avoid inaccurate offset measurement, the signal goes through the comparator should be chopped at the comparator output instead of the input so that the comparator offsets are randomized by PN_O.

4.5 Signal-Dependent Dithering

The signal-dependent PN dithering scheme is applied to the background gain

calibration. It has the advantage of using a large dither that shortens the calibration time without sacrificing the signal range, which solves a common problem in the fixed-magnitude dithering scheme [20]. The signal-dependent PN dithering modifies the residues of the VGA stage1 and 2 as shown in Figure 4.8. One more comparator is added at 0 V to divide the input into more ranges. The dither of $\pm V_{CAL}$, $\pm 1/2 V_{CAL}$, or 0 is injected depending on the input level. The calibration voltage V_{CAL} is set to about $4/5 V_{REF}$ in order to allow sufficient. room for the comparator offset to vary. As a result, the residue is equivalent to $-2/5 \sim 2/5 \pm 2/5 \ V_{REF}$ when gain is 4, and is equivalent to $-3/5 \sim 3/5 \pm 2/5 \ V_{REF}$ when gain is 1. The signal-to-dither ratios are reduced to 1 and 3/2, respectively, while a full signal swing is reserved.
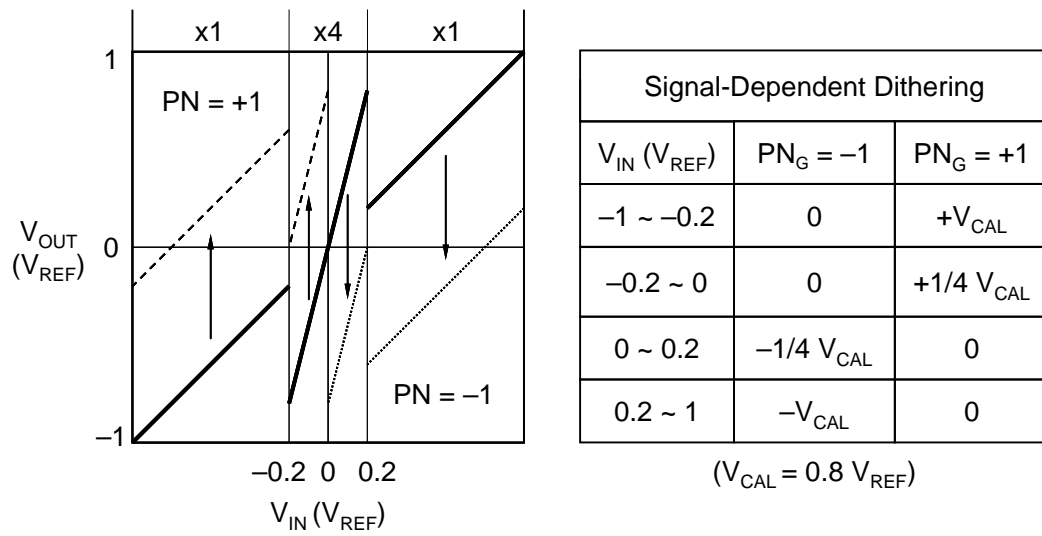
Figure 4.8: Residue plot of VGA stage1 and 2 with signal-dependent dithering.

The modified residue plot of the VGA stage3 is shown in Figure 4.9. One more

comparator is added at 0 V. The dither of $\pm V_{CAL}$, $\pm 1/2$ V_{CAL}, or 0 is injected depending

on the input level. The signal-to-dither ratios are also 1 and 3/2 when gain is 2 and 1,

respectively.

	x1	x2	x1
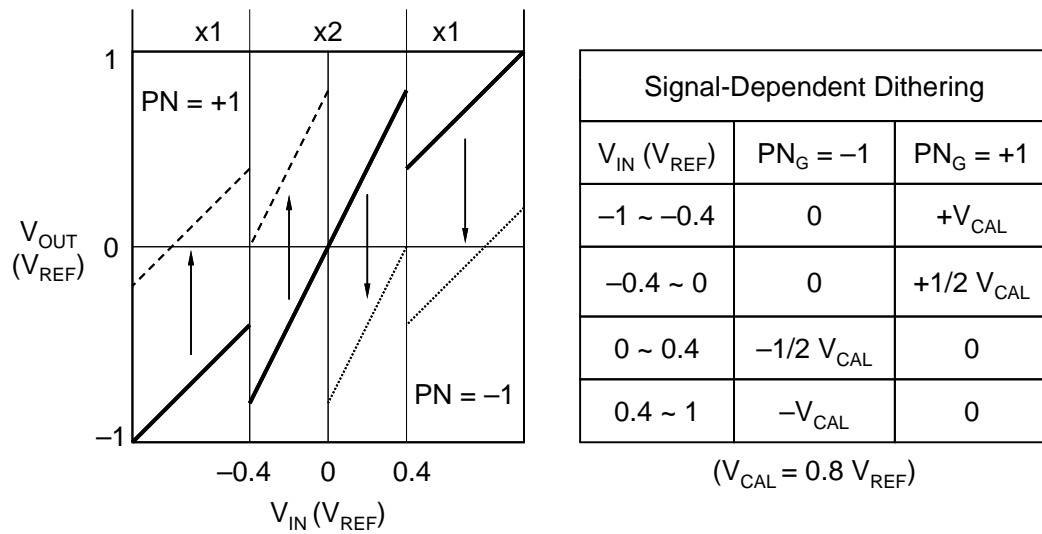
Figure 4.9: Residue plot of VGA stage3 with signal-dependent dithering.

Figure 4.10 shows a switched capacitor VGA stage in the sampling and amplification phases. During the sampling phase, the sampling capacitor is switched between $\pm V_{IN}$ according to PN_O, and the feedback capacitor is reset to zero. In the amplification phase, the sampling capacitor is switched to zero. The feedback capacitor is switched to the opamp output when the gain is 1, and only one of the n feedback capacitors is switched to the opamp output when the gain is n.

(a)

(b)
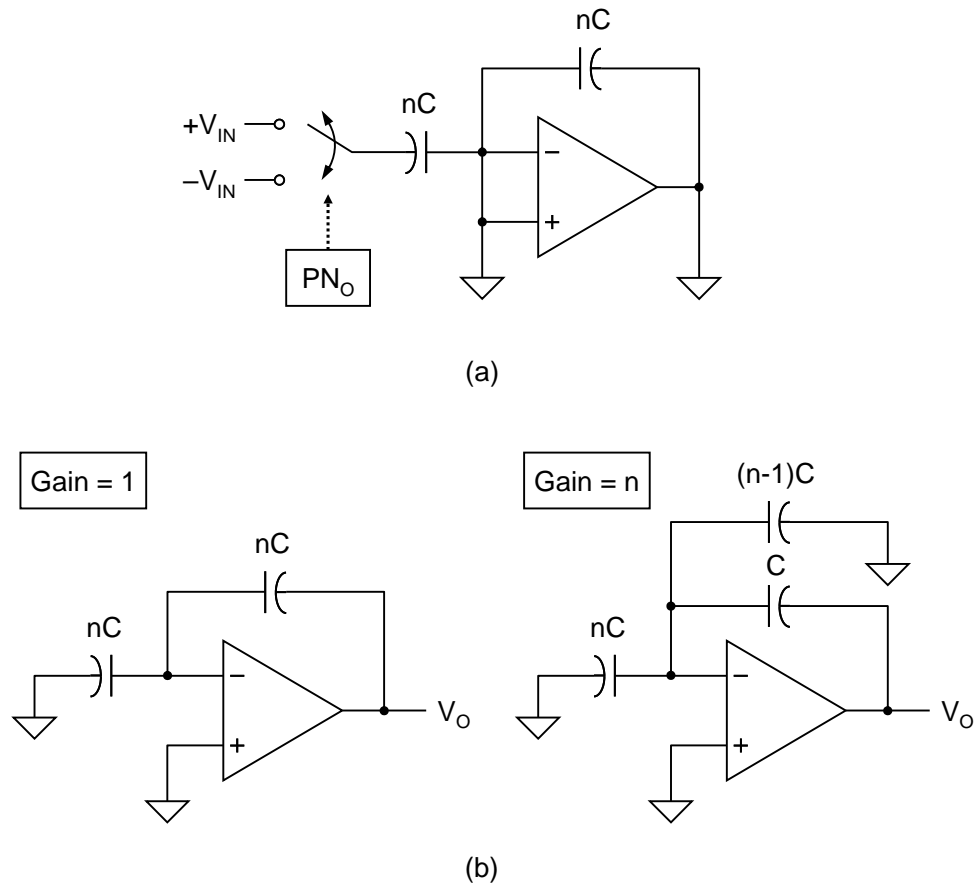
Figure 4.10: Switched-capacitor VGA stage. (a) Sampling phase with input chopping. (b) Amplification phase when gain=1 and gain=n.

The dither is injected in the amplification phase by switching all the sampling capacitor to $\pm V_{CAL}$ or 0 according to PN_G values and the comparator outputs if the gain is 1 as shown in Figure 4.11(a). When the gain is set to n, only one of the n sampling capacitors is switched to $\pm V_{CAL}$ or 0 as shown in Figure 4.11(b). The gain error contributed by each of the n sampling capacitor is combined to generate the actual gain error.
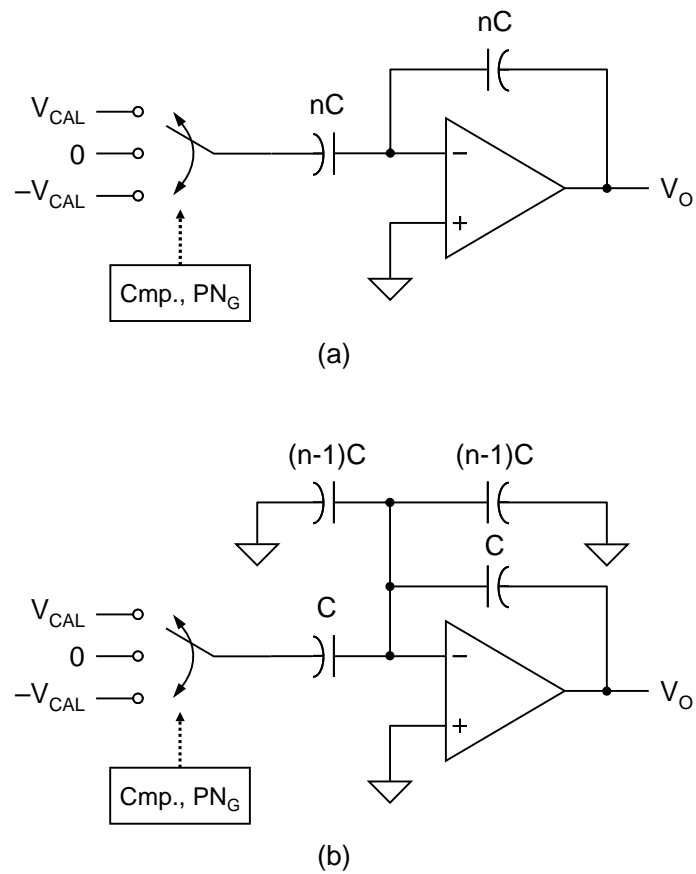
Figure 4.11: VGA gain stage in amplification phase with PN dithering.
(a) Gain=1. (b) Gain=n.

4.6 Circuit Implementation

4.6.1 ADC Architecture

Figure 4.12 shows the FADC block diagram. The proposed FADC has three

VGA stages, 9 1.5-b pipeline stages, and a 3-b flash. The digital output is 15-b. The

comparator outputs in each stage are connected to the digital logic. The digital

encoding, digital correction, digital calibration, and also the PN sequence generator

functions are all integrated in the digital logic. It provides each VGA stage with the

PN values and the calibration enable signals.
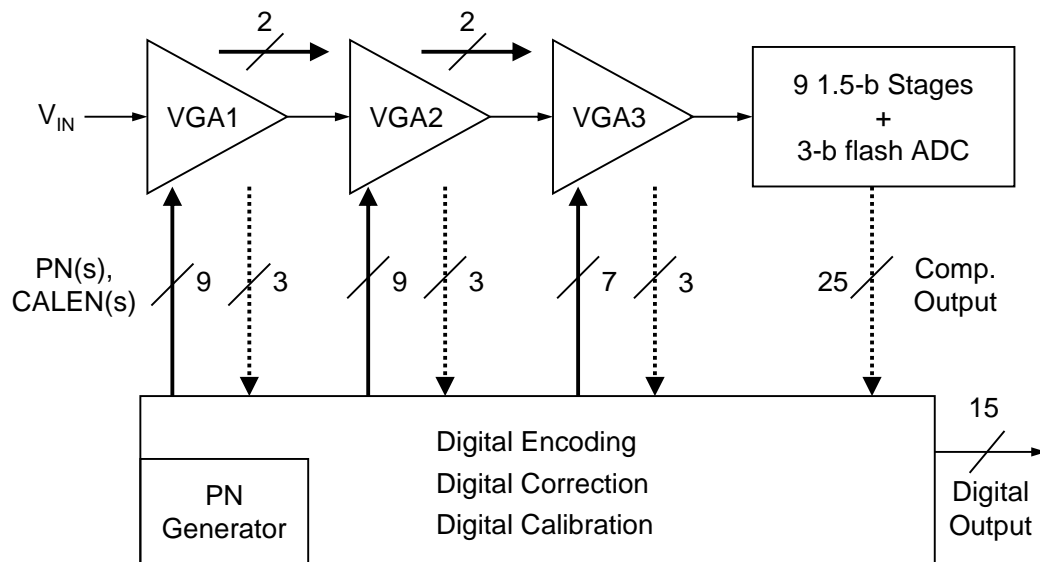
Figure 4.12: Floating-point ADC block diagram with digital calibration.

VGA stage 1 and 2 pass the information of their dither magnitudes to VGA

stage 2 and 3, respectively. The dither injected in the preceding stage is subtracted

before the VGA gain is set so that the gain selection is not be affected by the dither

injected in the preceding stage. This dither subtraction is realized by switching the

sampling capacitor to $\pm V_{CAL}$ or 0 and by adding the dither back digitally.

4.6.2 Operational Amplifier

One common problem in a switched-capacitor VGA is that its closed-loop bandwidth varies with the gain setting. The closed-loop bandwidth is set by the opamp unity-gain bandwidth and the feedback factor, which is determined by the circuit configuration. Generally, a high gain configuration leads to a small feedback factor and slows down the settling behavior. When the circut is configured to have low gain, the loop tends to get unstable.

In this work, the same Miller-compensated two-stage opamp described in Section 3.5 is used in both the VGA and pipeline stages. Nevertheless, in a VGA stage, the value of the Miller capacitor varies according to the VGA gain. Figure 4.13 shows the opamp used in a VGA stage. The Miller capacitor is connected when the VGA gain is low and disconnected when the gain is high to change the opamp unity-gain bandwidth. Therefore, the variation of the feedback factor is compensated by varying the opamp unity-gain frequency, and a constant close-loop bandwidth is realized. During the sampling phase, the Miller capacitors are connected for the charges on them to be reset.
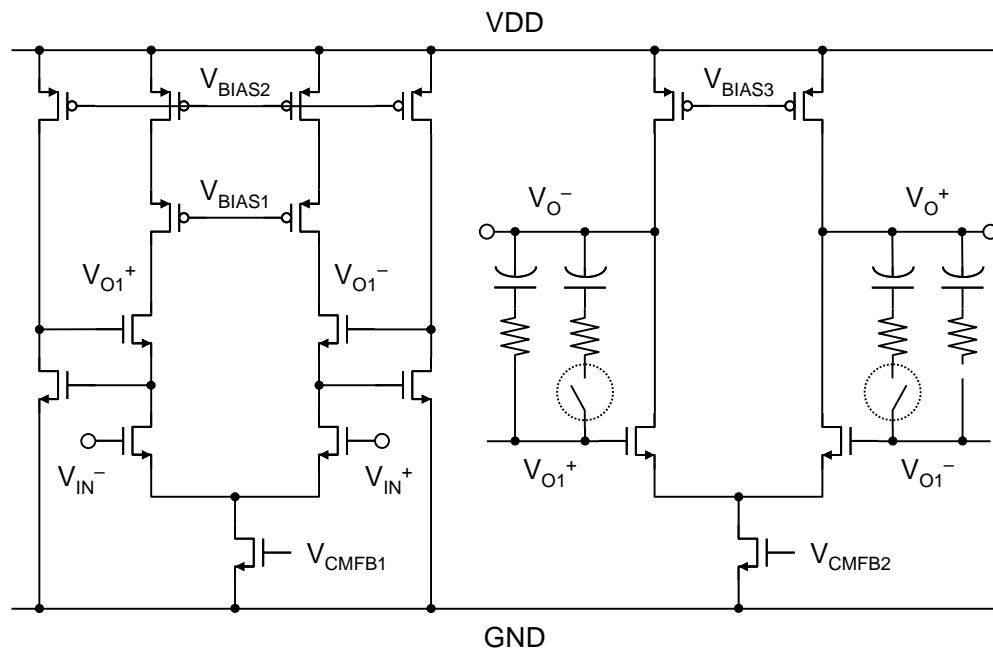
Figure 4.13: Operational amplifier for VGA stages.

4.6.3 Sampling without S/H

ADCs with switched-capacitor pipelined architecture often include an input sample-and-hold amplifier (S/H) to avoid sampling mismatches between the switched-capacitor amplifier and the comparators in the first stage [40]. However, an S/H with sufficiently high linearity and low noise would consume a large amount of current. In this work, a modified clocking scheme is used to avoid the sampling mismatch so that an S/H is not required.

Figure 4.14 explains the sampling mismatch between the amplifier and the

comparator. The RC sampling network in the amplifier adds a phase delay to the input signal. In the comparator, the phase delay is contributed by both the RC network and the pre-amp. If the phase delays in the two paths are not the same, the signal sampled in the amplifier is different from the signal sampled in the comparator. This sampling mismatch exhibits as a comparator offset and may affect the system performance as the phase delay gets larger with higher input frequency.
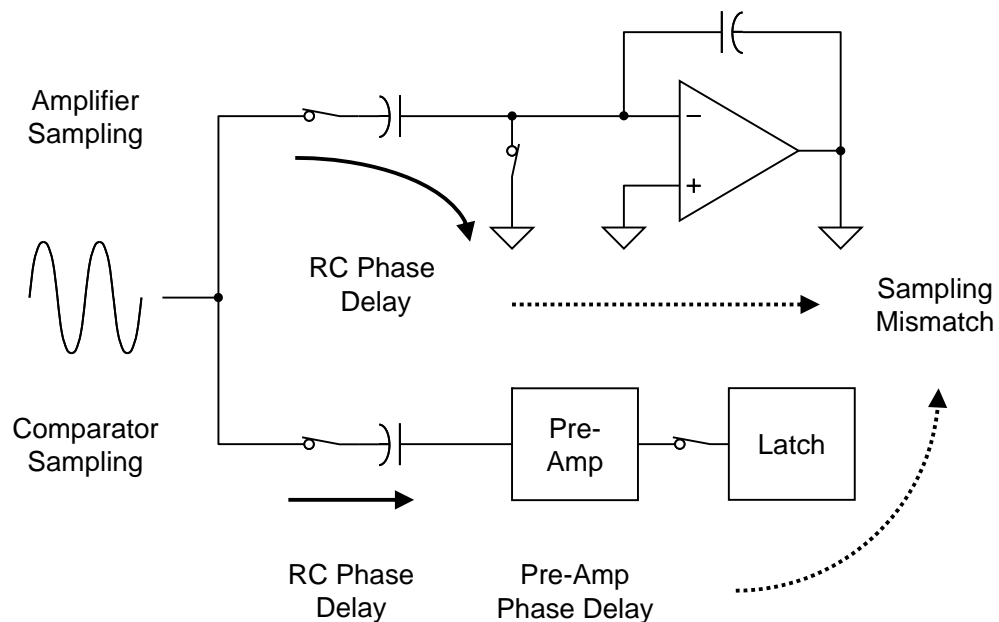
Figure 4.14: Sampling mismatch without S/H stage.

To match these two delays usually requires a very high-speed pre-amp, which is difficult to achieve and leads to a low pre-amp gain. A modified clock scheme for

the comparators of VGA stage1 is shown in Figure 4.15. The normal sampling time is divided into two clock phases to separate the phase delays caused by the RC network and the pre-amp. During the first phase, the comparator samples the signal with a scaled replica sampling network of the amplifier. Therefore, the signals sampled in the comparator and the amplifier are the same. During the second phase, the sampled signal is then amplified by the pre-amp to suppress the input-referred latch offset. The modified clock scheme imposes a tradeoff between sampling accuracy and comparator offset. Long sampling time increases the sampling accuracy but also increases the comparator offset. Short sampling time leads to less comparator offset but more sampling error.
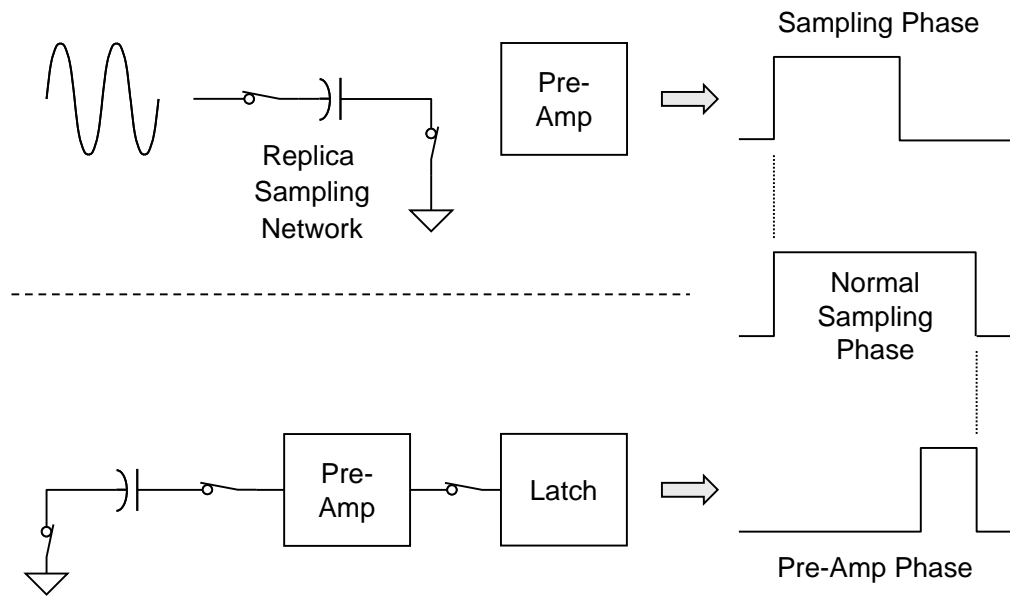
Figure 4.15: Modified sampling phase in VGA stage1.

Figure 4.16 shows a clock generator with adjustable sampling time used to optimize the performance. The sinusoidal input has a frequency twice that of the sampling frequency, and is amplified by a digital buffer to generate a pulse signal. The pulse signal is then fed into a frequency divider to provide the main clock for the circuits.

Note that the duty cycle of the pulse is affected by the DC offset of the sinusoidal input, but the duty cycle of the clock signal after the frequency divider is not. The clock phases for VGA stage1 are then generated by the pulse and the main clock. The sampling time is set by the duty cycle of the pulse, which is adjustable by

the input DC offset.

External Sinwave   Digital Buffer   Frequency Divider   Main Clock

2 F$_S$

1/2

F$_S$

VGA Stage1 Sampling Phase
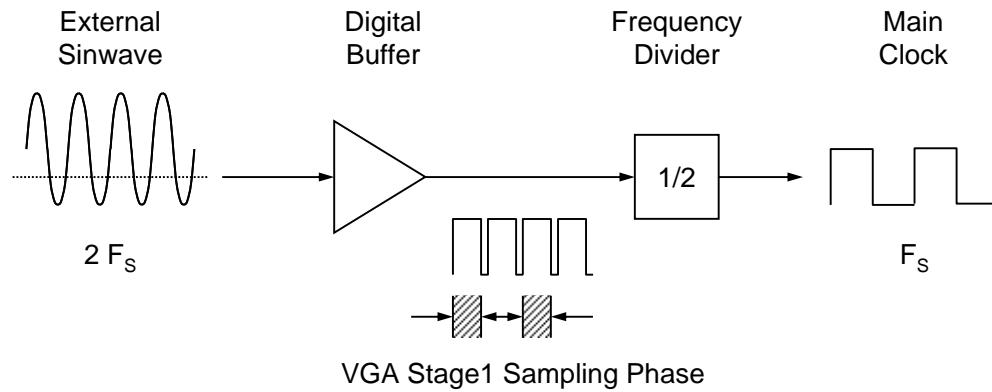
Figure 4.16: Modified clock generator.

4.7 Experimental Results

The prototype fabricated in 0.18-μm CMOS occupies an active area of 3.5 x 2.5 mm^2, and consumes 270 mW at 1.8 V. The digital calibration algorithm is entirely implemented on-chip. The digital logic occupies 1.5 mm^2. The die photo is shown in Figure 4.17.
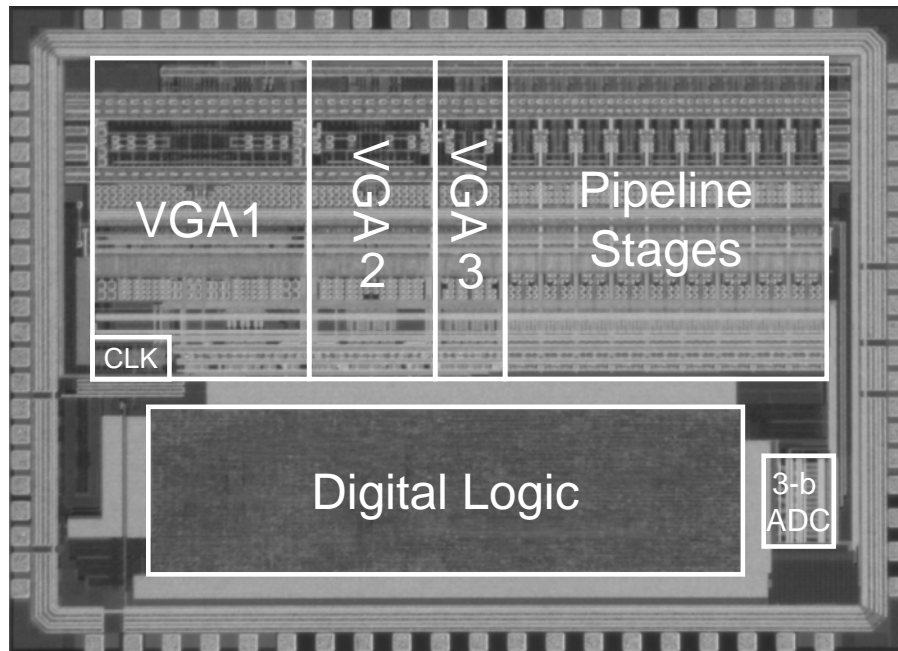
Figure 4.17: Die photo.

The gains and offsets for all VGA stages are measured and calibrated. Each measurement accumulates 2^{26} samples to ensure an accuracy of 15 bit. The calibration proceeds from VGA stage3 to the front repeatedly. Figure 4.18 shows the measured DNL and INL at a 15-b level when sampling at 60 MS/s before and after calibration. In both cases, the DNL decreases as the input signal becomes smaller. The INL before calibration shows large steps at the VGA gain-range boundaries. After calibration, the step errors are greatly reduced, and are only limited by the 10-b back-end ADC, which has a measured INL of ±24 LSB at a 15-b level. The INL after calibration indicates that the FADC effectively enhances the INL to ±0.9 LSB within the gain range of 32.
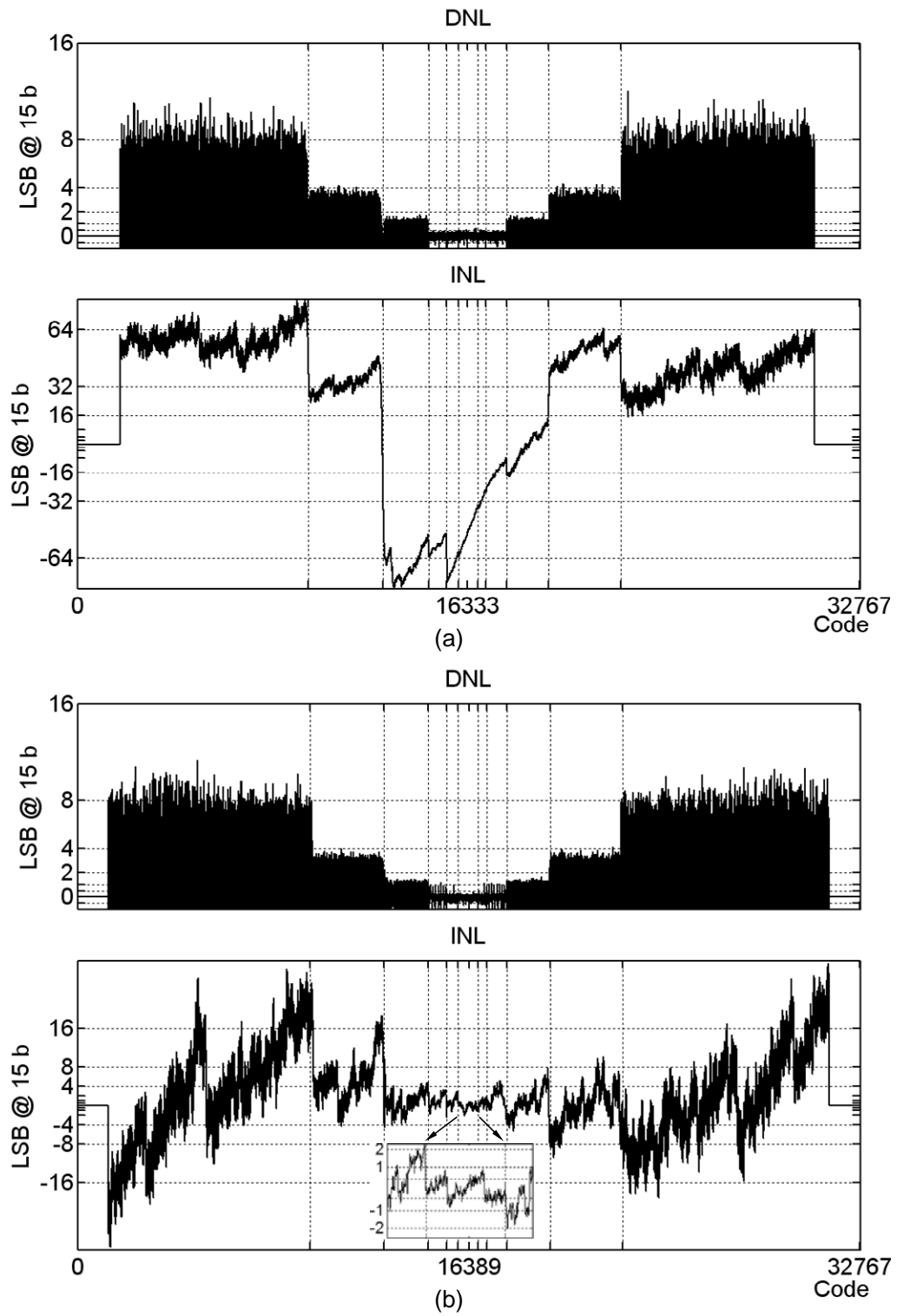
Figure 4.18: Measured DNL and INL. (a) Before calibration. (b) After calibration.

The INL in every gain range is mainly the replica of the linearity of the back-end ADC. This is also proven in the measured SFDR and SNDR by varying the input amplitude as shown in Figure 4.19. The FADC exhibits an uniform SFDR over the gain ranges after calibration. Without calibration, the SFDR and the SNDR are limited by the harmonics resulting from the large step errors at the boundaries. The SNDR after calibration is equivalent to that of an ideal 10-b ADC. It remains constant as the SNDR of the ideal 10-b ADC while the input amplitude decreases, and is finally dominated by the -80 dB thermal noise floor in the VGA stage1.
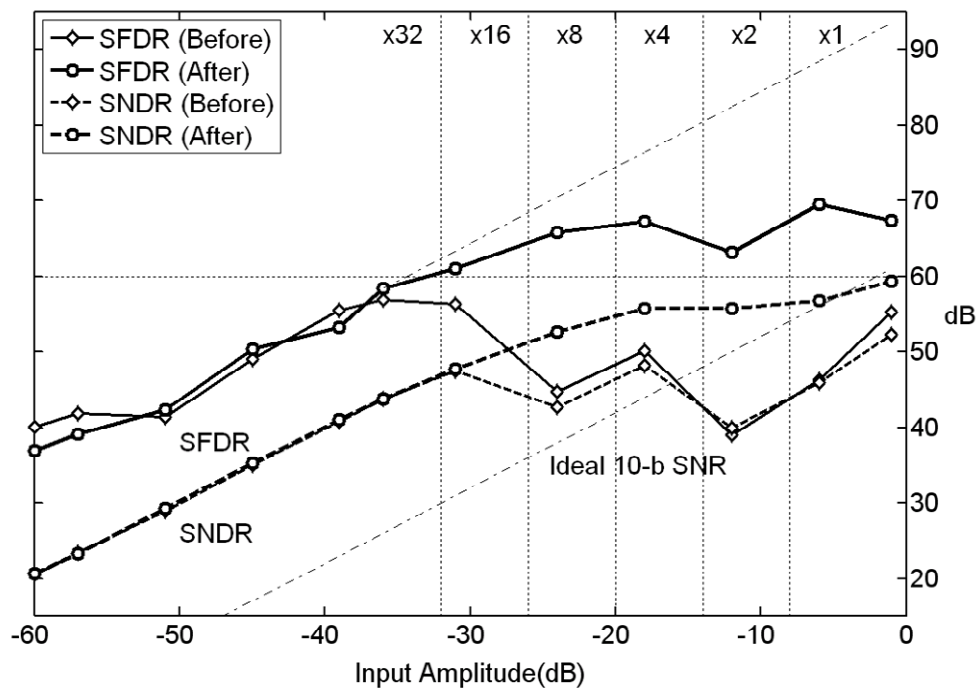
Figure 4.19: Measured performance vs. input amplitude with 29MHz input @60MS/s.

Figure 4.20(a) shows the ADC performance with varying sampling frequencies up to 70 MS/s. The SFDR and SNDR stays higher than 65 and 60 dB up to 60 MS/s, respectively. Figure 4.20(a) shows the ADC performance at 60 MS/s with varying input frequencies up to 65 MHz. The SFDR stay above 65 dB, and the peak SNDR decreases slightly with the input frequency.
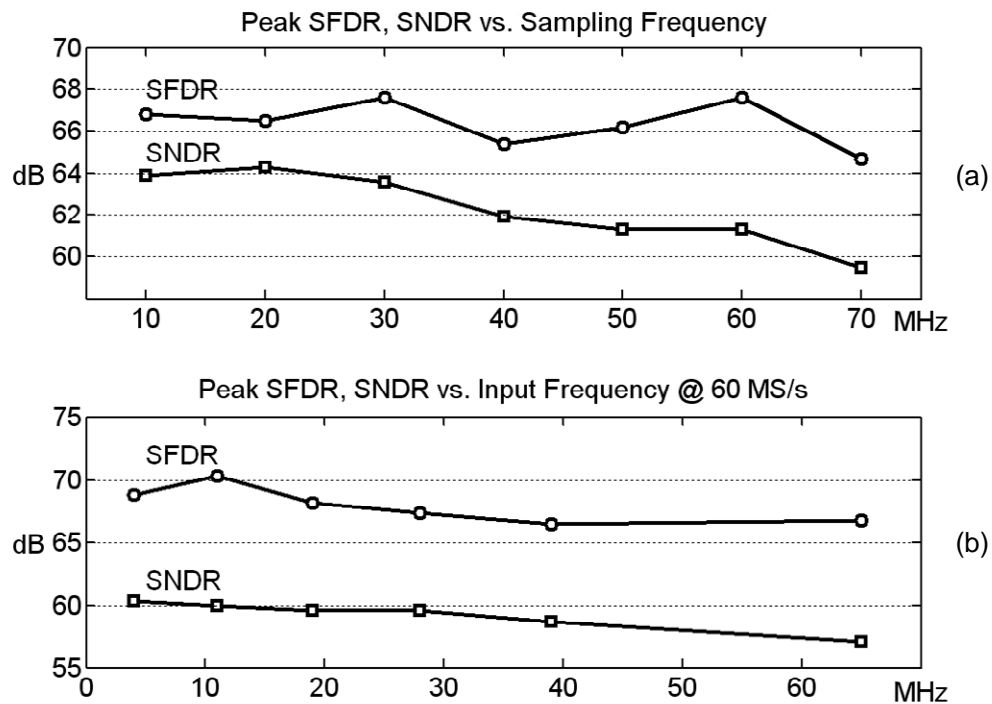
Figure 4.20: (a) Measured performance vs. sampling frequency. (b) Measured performance vs. input frequency @ 60 MS/s.

The measured performance at 60 MS/s is summarized in Table I. A comparison with the 15-b pipelined ADC described in Chapter 3 is included. The designs of the

analog components for both works are almost the same. This work achieves a higher conversion rate than the 15-b pipelined ADC after the non-ideal effects of the bonding wires are considered. Triple bonding is applied to the critical input, reference voltage, and power pins. The signal swing is higher since high resolution is not required when signal is large. This work has a lower noise floor. The noise contributed by the S/H stage is avoided, and the noises of the back-end stages are suppressed by the VGA gain. The digital logic occupies a larger area due to the digital multipliers. The FADC achieves a better performance when the input signal is small.

Table 4.2: Summary of Measured Performance

	Floating-Point ADC	Pipelined ADC
Technology	0.18-μm CMOS	0.18-μm CMOS
Supply Voltage	1.8 V	1.8 V
Resolution	10~15 b	15 b
Conversion Rate	60 MS/s	20 MS/s
Reference Voltages	1.5V / 0.3V	1.4V / 0.4V
Signal Range	2.4 V_{pp}	2 V_{pp}
INL@15-b	24 ~ 0.9 LSB	1.3 LSB
Peak SFDR	70 dB	98 dB
Noise Floor	−80 dB	−73 dB
Active Area	2.5 x 3.5mm^2	2.3 x 1.7 mm^2
Digital Area	1.5 mm^2	0.6 mm^2
Total Power	300 mW	285 mW

4.8 Summary

A floating-point ADC which extends the dynamic range without increasing the effective number of bits, and achieves a high conversion rate using the switched-capacitor pipelined architecture is presented. The FADC adjusts its quantization steps instantly depending on the sampled input level. Its linearity is

improved by the digital background calibration technique, which calibrates the gain and offset errors of the VGA stages. Signal-dependent dithering is also applied to the VGA stages to overcome the constraints of fixed-magnitude dithering. A modified clock scheme relaxes the requirement on an S/H stage and leads to a low noise floor. The techniques used in this work can also be applied to other switched-capacitor pipelined ADCs. After gain and offset calibration, the ADC is suitable for time-interleaved applications.

Chapter 5

A 65-nm Continuous-Time $\Delta\Sigma$ Modulator with 81-dB DR and 8-MHz Bandwidth Auto-Tuned by Pulse Injection

5.1 Introduction

In the digital wireless SOC environment, CT $\Delta\Sigma$ ADCs have been widely used for I/Q quantization due to the built-in anti-aliasing function and the insensitivity to the input sampling error. They are suitable for low-voltage, low-power applications and also offer higher-frequency performance than switched-capacitor modulators as no critical opamp settling is required. CT modulators with low oversampling ratio (OSR) have achieved DRs greater than 75 dB in a 20-MHz band [41], [42], which is comparable to the performance of pipelined ADCs. However, they suffer from

inaccurate active filtering as the filter time constants are set by the RC and C/Gm

values which vary by as much as ± 20~30%. CT filters have been tuned manually or

by using master-slave approaches mostly limited by the accuracy of analog

components. This chapter presents an exact time-constant auto-tuning method using an

LMS algorithm. With a binary pulse dither injected into the loop at the input of the

quantizer, the filter time constant can be calibrated continuously with crystal accuracy

until the correlated residual pulse dither disappears in the digital output.

After reviewing the basics of CT $\Delta\Sigma$ modulators in Section 5.2, the design

issues resulting from inaccurate filter time constant are discussed in Section 5.3. In

Section 5.4, an automatic time-constant tuning scheme based on pulse injection is

proposed. Section 5.5 covers the circuit implementation, and the experimental results

are summarized in Section 5.6.

5.2 Continuous-Time $\Delta\Sigma$ Modulator

5.2.1 Continuous-Time vs. Discrete-Time

A $\Delta\Sigma$ modulator consists of a loop filter, a quantizer, and a feedback

digital-to-analog converter (DAC). The loop filter can be either a discrete-time (DT) or CT filter as shown in Figure 5.1 (a) and (b). In DT ΔΣ modulators, the signal is sampled at the input, and anti-aliasing filtering is required before sampling. The DT filter, H(z), is usually realized with a switched-capacitor filter. Its characteristics are accurately set by the capacitors ratios. However, the sampling frequency of DT ΔΣ modulators is limited by the opamp settling requirement. The data conversion rate beyond the MHz level is hard to achieve when the OSR is high.

(a)

(b)
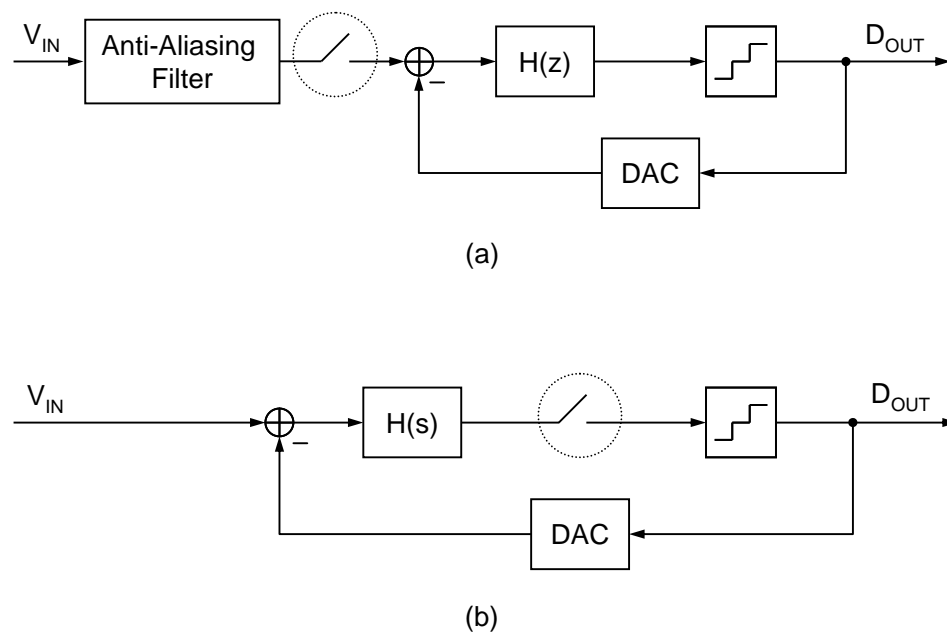
Figure 5.1: (a) Discrete-time ΔΣ modulator. (b) Continuous-time ΔΣ modulator.

In CT ΔΣ modulators, the signal is sampled inside the loop as shown in Figure

5.1(b). As a result, the in-band sampling error is suppressed by the noise transfer function (NTF) along with the quantization noise. Considering the sampling aliasing as a sampling error, the NTF also performs anti-aliasing filtering. This results in a power saving at the system level, where the requirement on anti-aliasing filter is greatly relaxed. Also, high performance sampling network is not required. This feature relaxes the demand for highly linear switches and is suitable for low-voltage design. In CT $\Delta\Sigma$ modulators, the sampling frequency is no longer limited by the opamp settling. Conversion bandwidth up to MHz with high resolution can be achieved [43].

5.2.2 Design Issues of CT $\Delta\Sigma$ modulator

CT $\Delta\Sigma$ modulators suffer from several problems in the DAC feedback path since the DAC output is considered as a continuous signal in CT $\Delta\Sigma$ modulators rather than a sampled signal in DT $\Delta\Sigma$ modulators. These issues include: (1) clock jitter, (2) comparator metastability, and (3) static and dynamic non-linearity of DAC. Since the DAC output error can be modeled as an additional signal at the input, it passes through the modulator without any suppression.

The output waveform of the DAC is determined by the quanitzer output and

the pulse shaping of the DAC. The quantizer output is affected by both clock jitter and comparator metastability, which modulate the DAC pulse width and result in additional noises [44]. The problem caused by clock jitter can be mitigate by using an on-chip low jitter clock source [41] or properly shaped DAC pulse, which is less sensitive to the jitter [45], [46]. The effect of comparator metastability can be eliminated by latching the comparator output with a half cycle delay. However, it introduces extra loop delay and decreases the loop stability [47].

The static non-linearity of the DAC results from the mismatch between the DAC cells. Dynamic element matching has been used to randomize the mismatch and linearize the DAC output [48]. For current steering DACs, current cell calibration can effectively improve the static linearity up to 14 b [49], [50]. Like most of the high-speed, high-resolution DACs, the feedback DAC also suffers from the dynamic non-linearity while switching the DAC cells at high frequency. Nevertheless, since the DAC resolution in $\Delta\Sigma$ modulators is usually less than 5 b, and the signal frequency is relatively low compared to the sampling frequency, the DAC cells are not switched as frequently as in nyquist rate DACs.

5.3 Inaccurate filter time constant

One of the critical issues in the design of CT $\Delta\Sigma$ modulators is the inaccurate filter time constant due to variations in process, voltage, and temperature (PVT). The time constant of a CT filter is set by the absolute RC or C/Gm values. However, both the resistor and capacitor values can vary by more than 25% in modern CMOS technologies. Inaccurate active filtering either degrades the DR or makes the modulator unstable. This effect is even more significant in high-order, low-OSR designs. By lowering the OSR, the signal band can be widened, but the in-band zeros of the NTF should be optimally placed to maximize the DR [51].

Figure 5.2 demonstrates the effect of inaccurate time constant. The two curves shows the simulation results of a 3rd-order 4-b $\Delta\Sigma$ modulator (OSR=16) with two different sets of filter coefficients. If the filter coefficients are chosen to maximize the DR, the performance stays high within a small time-constant variation range and easily goes unstable. If the filter coefficients are chosen so that the DR stays constant within a wider time-constant variation range, the performance of the modulator is sacrificed. It is noted that the design of filter coefficients is a tradeoff between performance and stability. With the presence of time-constant variation, it is more

difficult to meet both requirements at the same time.

Performance vs. Time-Constant Variation
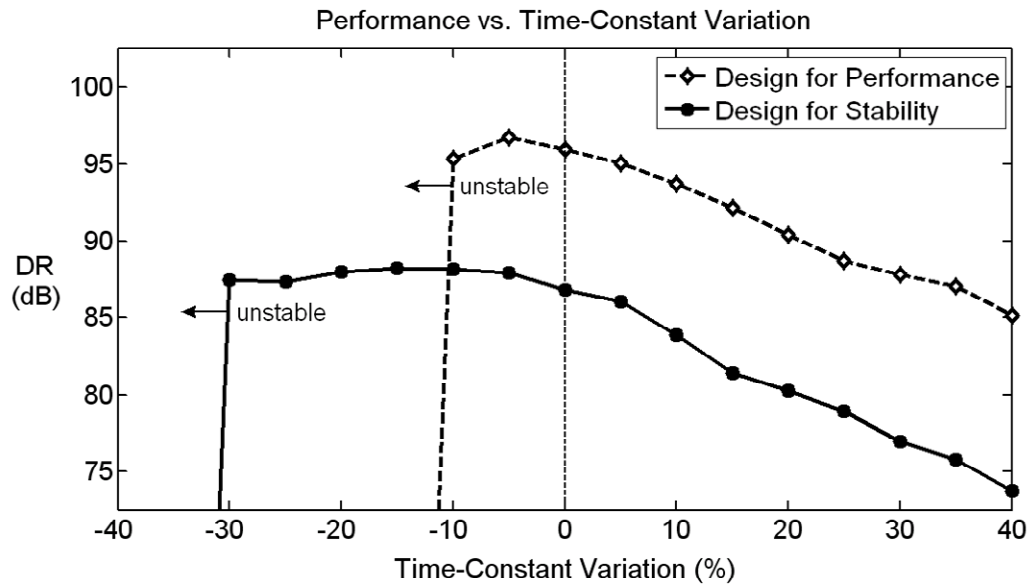
Figure 5.2: Simulated DR vs. time-constant variation.

5.4 Automatic Time-Constant Tuning by Pulse Injection

5.4.1 Existing Time-Constant Tuning Techniques

The time constant of CT filters have been tuned directly or indirectly [52]–[59].

Direct tuning is performed in foreground. The filter output is compared to a known

signal, and a tunable component in the filter is adjusted accordingly. This method can

calibrate the time constant accurately but interrupts the filter's normal operation while

calibrating. In indirect tuning, the time constant can be calibrated in the background.

This technique is mostly realized with master-slave approaches. The time constant of a

slave filter, which is a replica of the master filter, is tuned separately. The tunable

component in the master filter is then set according to that in the slave filter. This

approach requires additional analog components, and the mismatch between the

master and slave filters limits the time constant tuning accuracy to about 5% [56].

5.4.2 NTF Zero Detection by Pulse Injection

In this work, an automatic time-constant tuning technique is proposed. The

filter time constant can be calibrated continuously with crystal accuracy. This

technique is based on a simple fact that any tone inside the loop will be nulled at the

NTF zero frequency (f_{zero}). Figure 5.3 shows this principle of detecting the NTF zero

location using a single tone. Assume that a sinusoidal f_{zero} tone is injected at the input

of the quantizer. It becomes a part of the quantization noise, and is then filtered by the

same NTF [60].
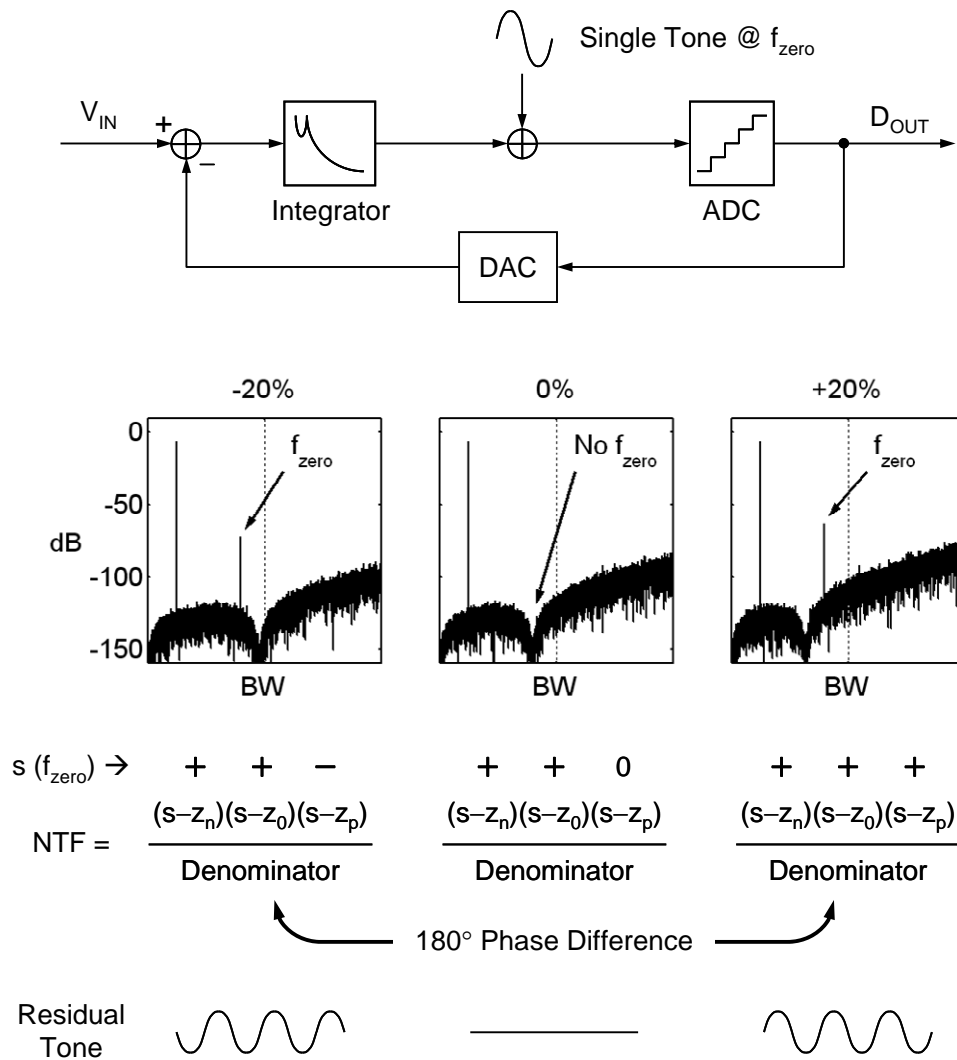
Figure 5.3: Tone injection to detect the zero in the NTF.

Ideally, the injected tone should disappear completely and doesn't affect the digital output. However, if the location of the NTF zero is not perfectly aligned with f_{zero}, a residual tone appears as shown in Figure 5.3 by the simulated examples with different filter time constants. Note that the zero frequency is lower than the injected

tone frequency when the RC value is too large, and is higher than the tone frequency when it is too small. This results in a 180°-phase difference of the residual tone output after the injected tone is filtered by the NTF. The NTF zero variation can be detected digitally by correlating this residual test tone in the modulator output.

Figure 5.4 illustrates the system block diagram for f_{zero}-tone correlation and detection. A small binary pulse dither is used instead of the sinusoidal tone in Figure 5.3. It is generated by dividing the sampling clock so that its frequency is accurately set by the sampling frequency. The correlation between the residual binary pulse in the digital output and the delayed version of the injected pulse is performed, and the output is accumulated. Since the binary pulse dither is injected, its harmonic tones and out-of-band noise at the harmonic frequencies are mixed down to DC, and affect the accuracy of the correlation detection. Therefore, an IIR filter is required to suppress the harmonics of the injected binary pulse so that the harmonic mixing and noise aliasing can be avoided. The delay block is to match the total fixed phase shift of the NTF and the IIR filter. Using the proper delay can minimize the correlation time, but inaccuracy in the amount of delay doesn't affect the detection result.

The simulated accumulator outputs with different time-constant variations are

also shown Figure 5.4. A small input signal is used in the simulation so that the accumulator output doesn't affected by the correlated signal term. The accumulator output changes its polarity with the polarity of the time-constant variation, and stay zero when the f_{zero} tone is perfectly align with the NTF zero. Therefore, the CT filter can be tuned based on the sign of accumulator output. The slope of the accumulator output is proportional to the magnitude of the residual tone, which is determined by the NTF inaccuracy.
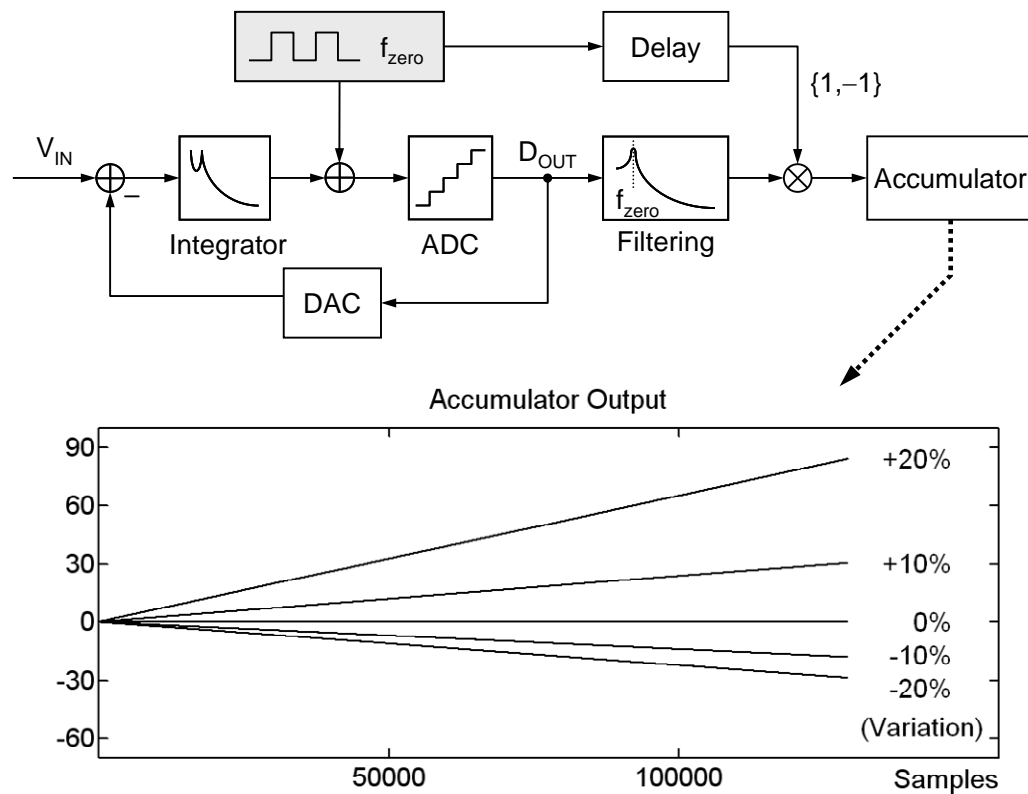
Figure 5.4: Detection of time-constant variation using pulse sequence.

Note that the correlated signal term is significant in the accumulator output, when the input signal is large. Figure 5.5 shows simulated modulator output spectrum and the accumulator output with an input signal spread over the signal band. The large out-of-band tones in the spectrum are the harmonics of the injected pulse. In the accumulator output, the correlated signal term varies. After a large number of samples are accumulated, its variation is relatively small compared to the correlated residue tone. The variation range of the correlated signal term should be carefully estimated so that the sign of the accumulator output can be defined properly. This implies the higher the slope of the accumulator output, the shorter the tuning time. Also, the calibration accuracy increases as more correlated output samples are accumulated.
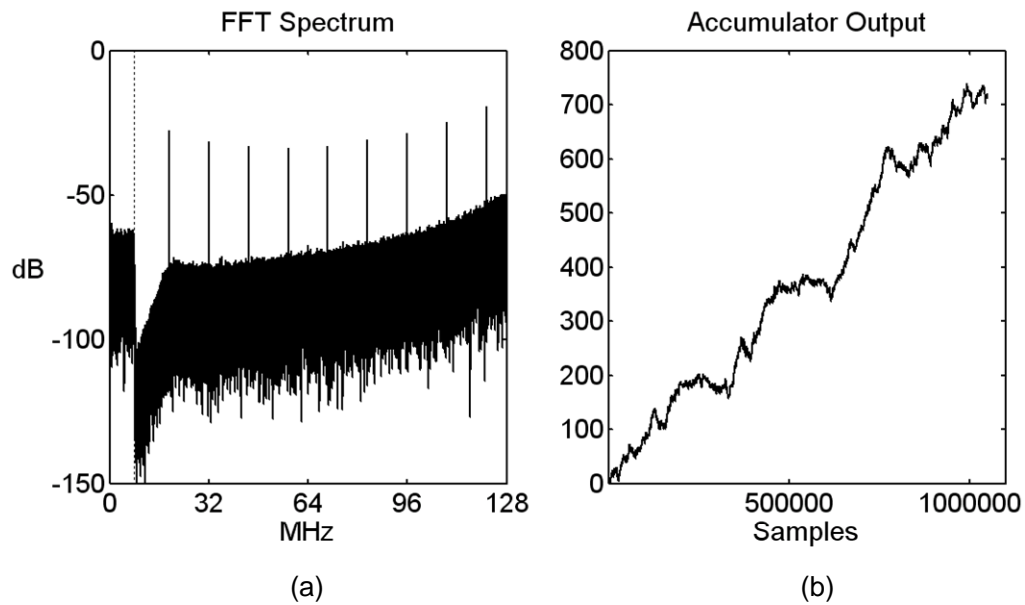
Figure 5.5: Simulation results with a large input signal spread over the signal band. (a) Modulator output spectrum. (b) The accumulator output.

5.4.3 Noise Cancellation in MASH-Type ΔΣ Modulators

The proposed automatic tuning technique can also be applied to MASH-type ΔΣ modulators using a test tone as shown in Figure 5.6. For an ideal MASH-type ΔΣ modulator, any pulse signal injected before the quantizer of a cascade stage is measured by the following stage and cancelled digitally by the noise cancellation filter (NCF). The frequency of the injected tone can be either in-band or out-of-band. The magnitude of residue tone is determined by (NTF–NCF), which is zero in the ideal case. As the NTF changes with inaccurate filter time constant, the residue tone appears

and exhibits different polarity as the time constant varies toward different directions.

The digital correlation function is the same as in the single-loop $\Delta\Sigma$ modulator case.

Since the performance of MASH-type $\Delta\Sigma$ modulators heavily relies on the function of

noise cancellation [51], the proposed scheme is attractive because highly accurate

calibration can be achieve by accumulating a large amount of output samples.
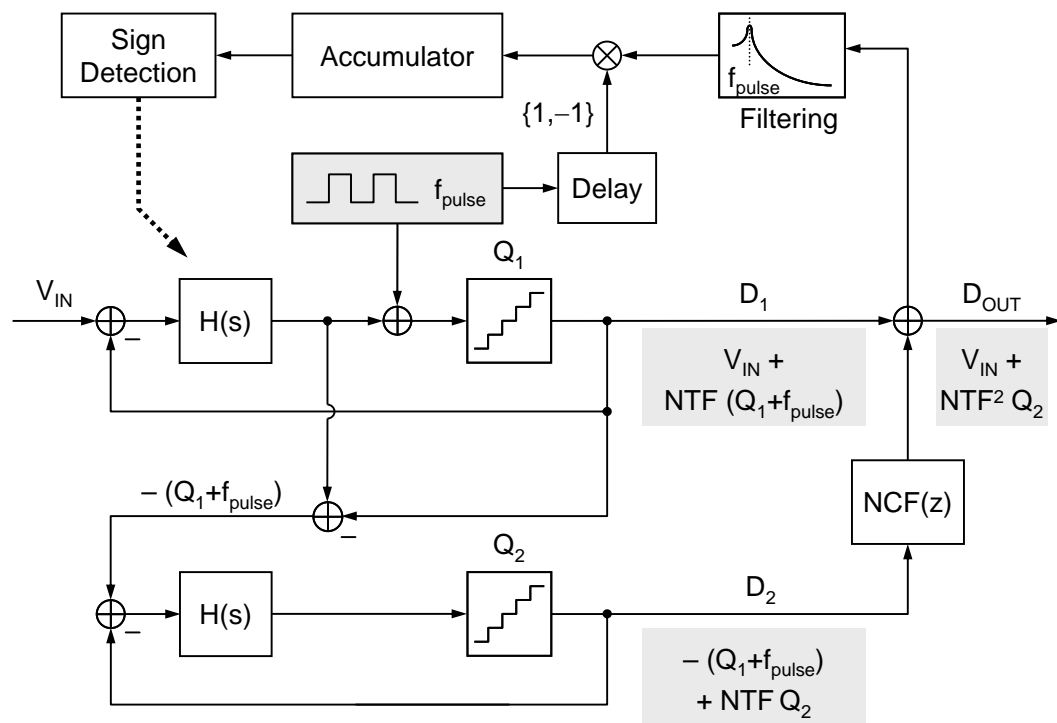
Figure 5.6: Time-constant calibration for CT MASH-type $\Delta\Sigma$ modulator.

5.5 Circuit Implementation

5.5.1 System Architecture

Figure 5.7 illustrates the system block diagram with the proposed LMS servo feedback loop for f_{zero}-tone correlation and detection. The modulator uses a 3rd-order feed-forward architecture. The NTF has one zero at DC and a pair of conjugate in-band zeros at 4/5 of the signal bandwidth. The pulse frequency f_{zero} is accurately generated after dividing the sampling clock by 2·OSR·5/4. The digital output is filtered by the IIR filter and then correlated with the same delayed pulse. In this design, the time constant is calibrated according to the sign bit of the accumulator by trimming the 6-b binary-weighted capacitor array with an incremental step size of 1.25%.

Figure 5.7: CT ΔΣ modulator and time-constant calibration block.

5.5.2 Analog Circuit Implementation

There are three practical continuous-time filter structures: active RC, Gm-C, and MOSFET-C filters. Active RC filters have better linearity and larger signal swing. Gm-C filters usually can operate at higher frequency with less power consumption. MOSFET-C filters have continuous time-constant tunability but are not linear with low supply voltage. In the design, the loop filter is realized with an active RC filter to have large signal swing at 1.3V supply. The time constant of the active RC filter is

adjusted by the capacitor arrays as shown in Figure 5.8.
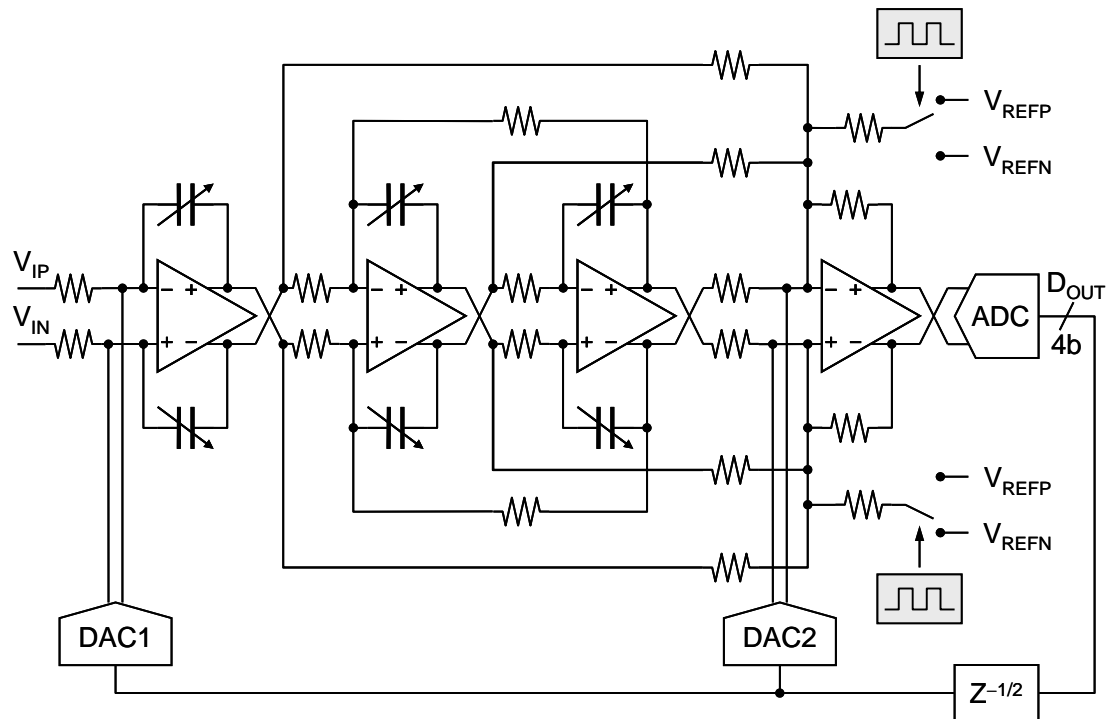
Figure 5.8: 3rd-order 4-b CT ΔΣ modulator and pulse dither injection.

Multi-bit nonreturn-to-zero (NRZ) DAC pulse shaping is used to reduce clock

jitter sensitivity. The 4-b quantizer output is latched with a half-clock delay to solve

the comparator metastability problem. This extra loop delay is compensated for by the

quantizer feedback DAC2. Both DAC1 and DAC2 are realized with

thermometer-coded current steering DAC with 15 current cells each. No dynamic

element matching or current cell calibration is applied to improve the DAC linearity.

A binary pulse dither is injected by switching an additional current into the

opamp current summing node. It is realized with two more resistors and four switches.

The proposed automatic time-constant tuning technique uses less analog components

than the master-slave approaches and imposes no strict requirements on the additional

components.

The opamp used in the integrators and the summing circuits is shown in Figure

5.9. A two-stage Miller-compensated structure is adopted for large output swing and

low output impedance. The non-dominate poles are designed high enough to avoid

excess phase delay in the loop. The simulated DC gain is 65 dB with resistive load.

The simulated integrator linearity reaches 95 dB with a 1 V_{pp} output swing.
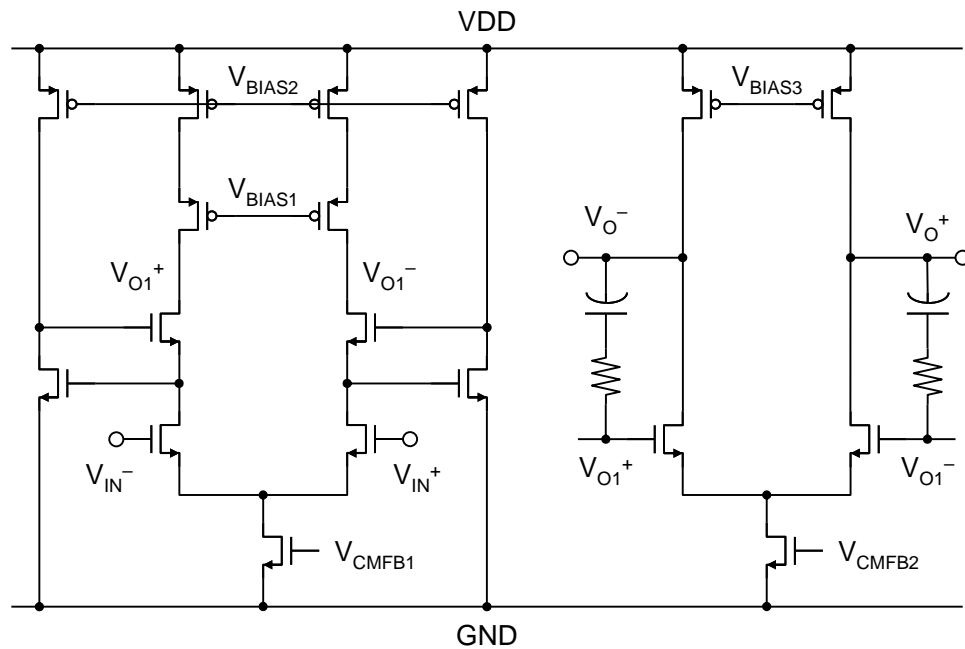
Figure 5.9: Operational amplifier for integrators and summing circuits.

5.5.3 Digital Functions

In this design, the standard digital functions of filtering, correlation, and accumulation are realized in the program. Figure 5.10 shows the IIR filter and its frequency response for harmonic filtering. The IIR filter consists of two identical digital resonators with resonate frequency around f_{zero}. The filter coefficients are carefully chosen so that no multiplier is required in the digital logic. Note that this IIR filter not only suppresses the harmonics of the injected pulse, but also amplifies the injected tone at f_{zero} to shorten the correlation time.
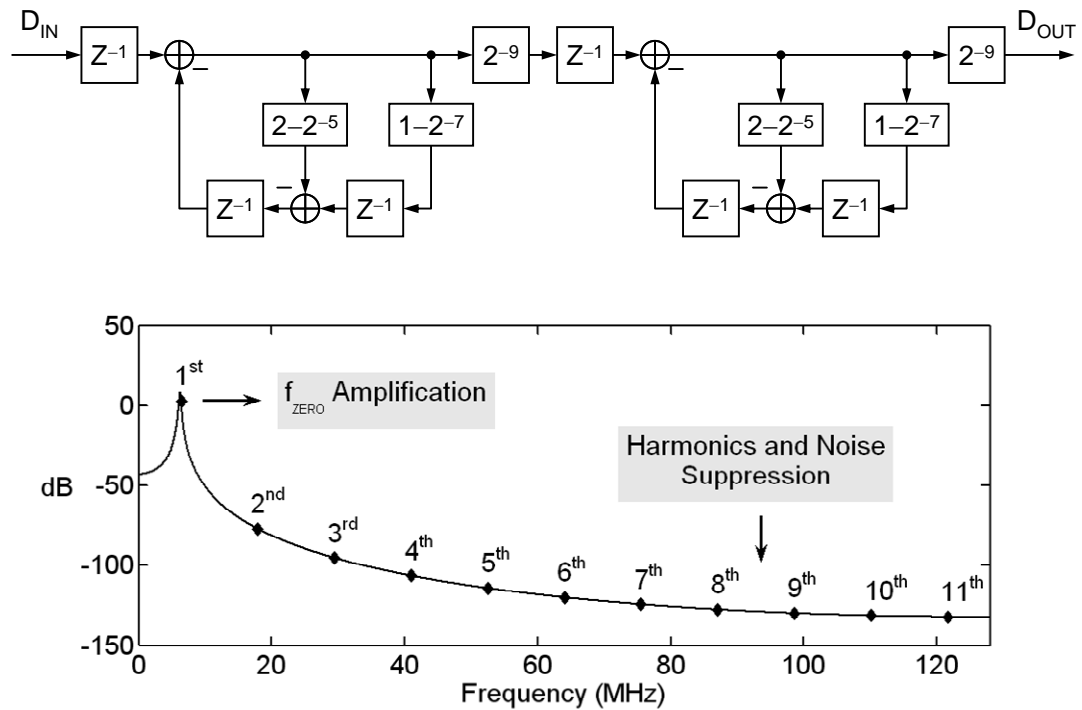
Figure 5.10: IIR filter and its frequency response for harmonic filtering.

5.6 Experimental Results

The prototype is implemented in 65-nm CMOS and occupies 0.5 mm^2. The chip photo is shown in Figure 5.11. The sampling frequency is 256 MHz (OSR=16), and the total power consumption is 50 mW from a 1.3V supply. The full-scale signal range is 2.4 V$_{pp}$, which is scaled down by 1/2 in the chip. A binary pulse dither of 1/8 V$_{REF}$ is used.
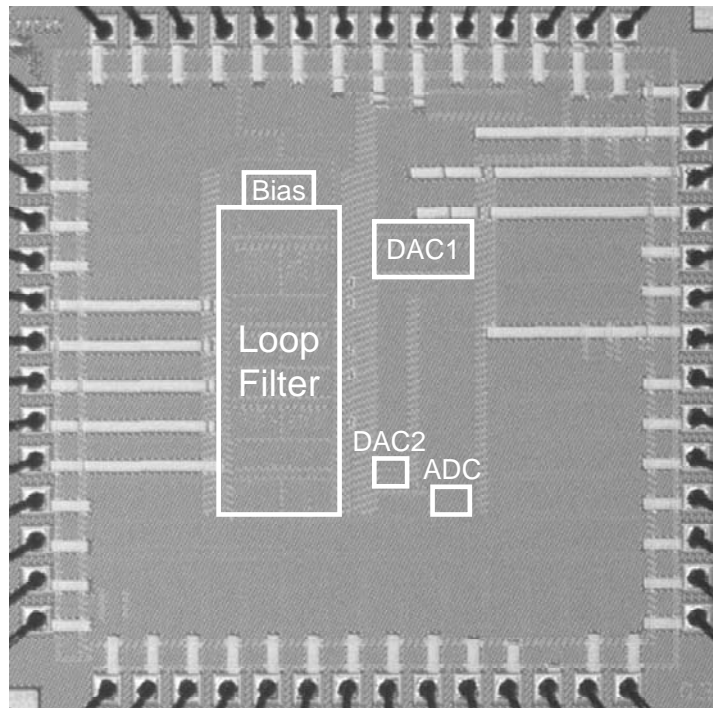
Figure 5.11: Die photo.

Figure 5.12 shows the measured residual tone, accumulator output, and DR with different capacitor trimming percentages. When the capacitor value is trimmed to −7.5%, the residual dither tone reaches the minimum value of −92 dB, the accumulator output crosses zero, and the DR reaches a peak value of 81 dB within an 8-MHz band. When trimmed by more than −35%, the modulator becomes unstable. Note that the accumulator still performs correctly although the modulator becomes unstable. However, if the RC value is far off, the results are erroneous. To avoid them, initial capacitor values can be set higher than the desired values. The accumulator

output shown in Figure 5.12 is measured by accumulating 2^{17} samples. It takes

0.5msec at a sampling frequency of 256 MHz. A large pulse dither can shorten the

calibration time but reduces the DR of the modulator. After the time-constant tuning, a

small residual tone still survives due to the tuning accuracy limited by the finite

capacitor trim step. A smaller dither can be used if such a residual tone is not

acceptable.
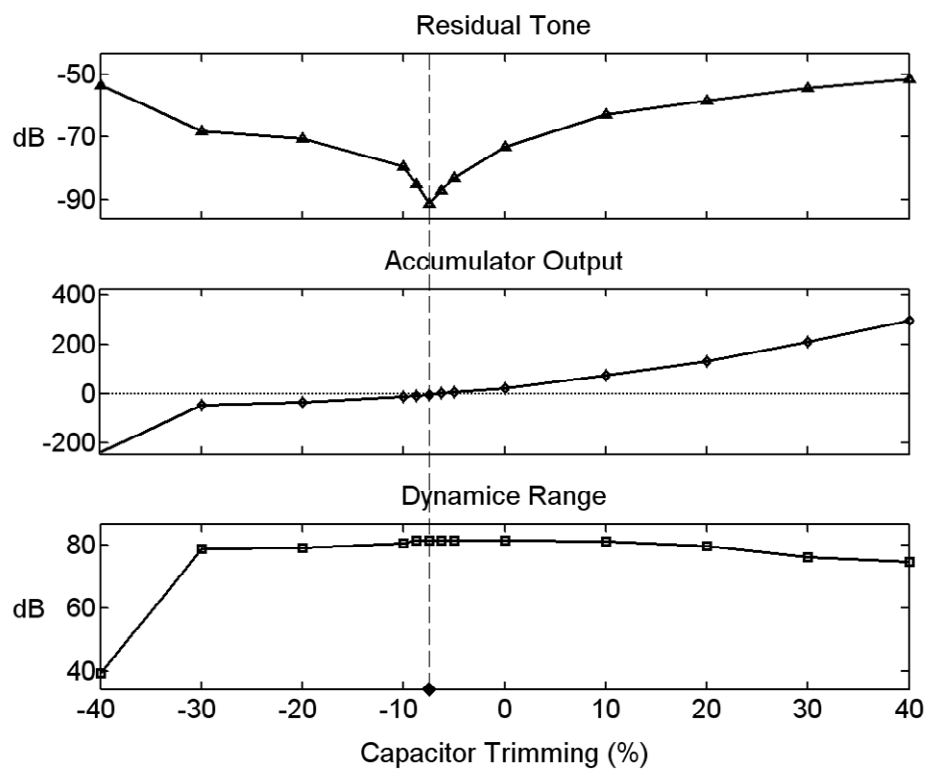
Figure 5.12: Measured residual tone, accumulator output, and DR vs. capacitor value.

Figure 5.13 shows the measured output spectrum with a small input before and

after calibration. The NTF is corrected, and the residual tone at f_{zero} is significantly

reduced.
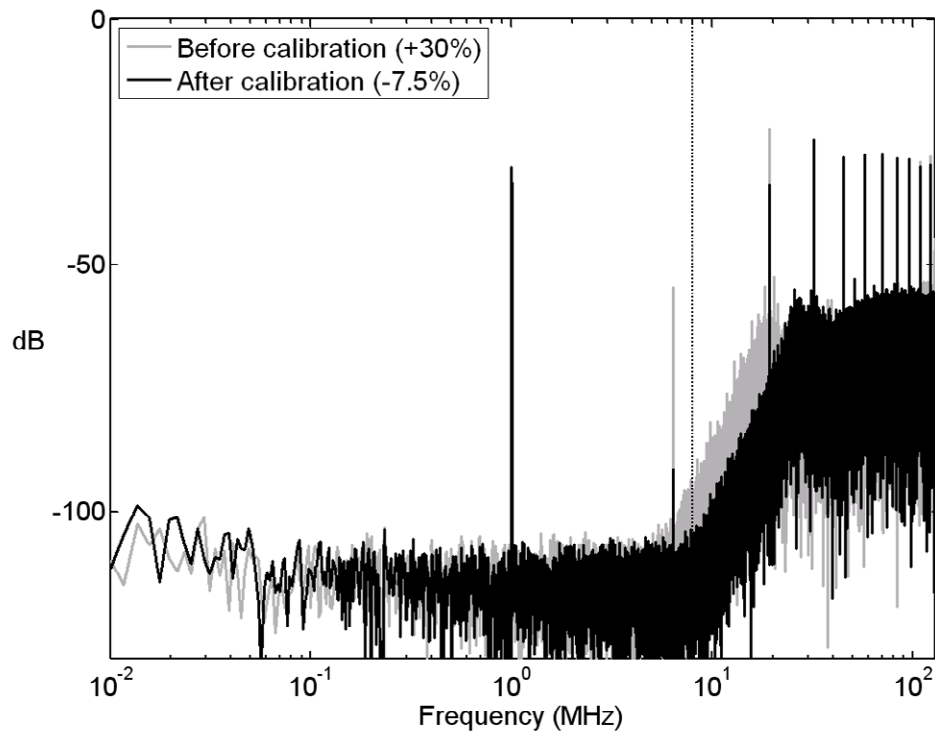
Figure 5.13: Measured output spectrum before/after calibration.

The measured SNR and SNDR versus input signal level with 1-MHz input are

shown in Figure 5.14. The CT $\Delta\Sigma$ modulator achieves 81 dB DR. The peak SNR is 76

dB with -1 dB input. The peak SNDR is 70 dB, which is limited by the linearity of the

feedback DAC.
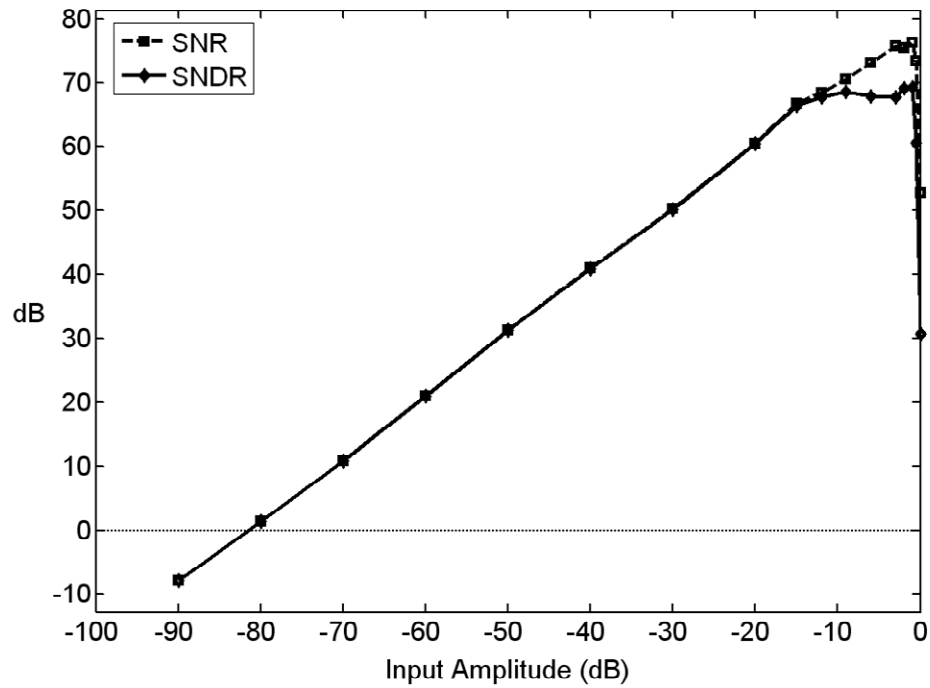
Figure 5.14: Measured SNR/SNDR vs. signal level.

The measured performances are summarized in Table 6.1, where comparisons with two state-of-art designs are included. A master-slave approach is used in [41] to calibrate the filter time constant in a single-loop $\Delta\Sigma$ modulator. An Off-line calibration technique is developed in [42] to tune the filter time constant in a CT MASH-type $\Delta\Sigma$ modulator with a resolution of 1%. This work achieves similar performance compared to the other two designs, but has lower signal bandwidth, which is limited by the speed of the comparators.

Table 5.1: Summary of Measured Performance and Comparison with State-of-Art

	This Work	ISSCC '06 [41]	ISSCC '07 [42]
Technology	65-nm CMOS	130-nm CMOS	90-nm CMOS
Architecture	Single-loop low-pass	Single-loop low-pass	MASH-type band-pass
Time-Constant Calibration	Pulse injection	Master-slave	Off-line
Sampling Frequency	256 MHz	640 MHz	340 MHz
Signal Bandwidth	8 MHz	20 MHz	20 MHz
Oversampling Ratio	16	16	17 (Quadrature)
Peak SNR	76 dB	76 dB	71 dB
Peak SNDR	70 dB	74 dB	69 dB
Dynamic Range	81 dB	80 dB	77 dB
Input Range (diff.)	(2.4/2) V_{pp}	1.6 V_{pp}	1 V_{pp}
Power Consumption	50 mW	20 mW	56 mW
Power Supply	1.3 V	1.2 V	1.2 V
Active Area	0.5 mm^2	1.2 mm^2	0.5 mm^2

5.7 Summary

An automatic time-constant tuning technique with pulse injection is applied to a 3rd-order CT $\Delta\Sigma$ modulator. Time-constant variation is detected digitally by

correlating the residue pulse in the output. This technique tracks process, voltage, and temperature variations continuously without using additional replica circuits. Highly accurate calibration can be achieved by accumulating a large amount of output samples. This same technique can also be applied to tune CT filters in MASH-type $\Delta\Sigma$ modulators using an out-of-band test tone.

5.8 Acknowledgement

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Chapter 6

Conclusions and Future Work

6.1 Conclusions

Background digital calibration techniques are demonstrated in three high-speed, high-resolution ADCs. They are all based on the same error measurement approach consisting of injecting test signals and correlating them at the digital output. The errors are calibrated either digitally or by capacitor trimming in the analog domain. The key research results are summarized below:

◆ The measurement time and dither magnitude constraints in the fixed-magnitude PN dithering schemes are investigated. They are greatly relaxed by the proposed signal-dependent dithering scheme.

◆ Signal-dependent dithering allows injecting a large dither without reducing the signal range while keeping the signal-to-dither ratio low to shorten the calibration

time.

◆ A digital background calibration scheme with signal-dependent dithering is applied to a 1.5-b/stage pipelined ADC. Highly accurate calibration up to above 15-b resolution is demonstrated to be feasible within a practical amount of time without paying significant penalty in circuit complexity and die area.

◆ Signal-dependent dithering is also applied to a high-speed, high-resolution FADC for VGA gain and offset calibration. The FADC adjusts its quantization steps instantly depending on the sampled input level and effectively enhances the ADC linearity by 5 b for small input signals.

◆ The gain and offset calibration scheme can be applied to the S/H stage in an ADC. After calibration, the ADC is suitable for time-interleaved architecture for high-speed applications.

◆ An automatic time-constant tuning technique with pulse injection is proposed and applied to a 3rd-order 4-b CT $\Delta\Sigma$ modulator. Highly accurate calibration can be achieved by accumulating a large amount of output samples. This same technique can also be applied to tune CT filters in MASH-type $\Delta\Sigma$ modulators

◆ A comparison of the three ADCs is shown in Table 6.1.

Table 6.1: Comparison of the three ADCs.

	Pipelined ADC	Floating-Point ADC	CT $\Delta\Sigma$ modulator
Process	0.18-μm CMOS	0.18-μm CMOS	65-nm CMOS
Supply Voltage	1.8 V	1.8 V	1.3 V
Conversion Rate	20 MHz	60 MHz	16 MHz
Signal Range	2 V_{pp}	2.4 V_{pp}	2.4/2 V_{pp}
Calibration Strategy			
Non-Ideal Effects	Cap. mismatch, finite opamp gain	Cap. mismatch, finite opamp gain, circuit offset	Filter time-constant
Measurement Approach	PN dithering	PN dithering, PN chopping	Pulse injecting
Calibration Method	Digital output shift	Digital output shift and slope correction	Capacitor trimming
Linearity Performance			
Peak SFDR	98 dB	75 dB	72 dB
Linearity	15 b 1.3 LSB	10~15 b 0.9 LSB @ 15 b	12 b
Linearity Improvement	Step error calibration	Gain and offset calibration	
Remaining Non-Linearity	Sampling non-linearity	Back-end ADC non-linearity	Current DAC non-linearity
Noise Performance			
Noise Floor	−73 dB	−80 dB	−81 dB
Noise Sources	kT/C, kT/Gm	kT/C, kT/Gm	kTR, kT/Gm
Noise Improvement		No S/H stage, VGA gain stages	Oversampling, RC calibration

6.2 Recommended Future Work

As highly accurately calibration for pipelined ADCs is proven to be practical, the calibration time can be further shorten by injecting signal-dependent dithers in full signal range as proposed in Section 3.3 and/or by increasing the sampling rate. To achieve higher sampling rate, the non-ideals effects resulting from the IC package, which forms the interface between the chip and the board, need to be examined carefully. The design challenges include accurate input sampling, clean power supply and reference voltages, and low-noise digital output waveform.

Time-interleaved architecture can also be used to increase the sampling rate. As the gain and offset mismatch between the ADCs can be calibrated, the remaining problem of sampling mismatch between the ADCs needs to be further investigated.

For the CT $\Delta\Sigma$ modulator in Chapter 5, DACs with current cell calibration can improve the linearity, and comparators with higher speed can increase the conversion rate. Also, it is beneficial to apply the proposed automatic time-constant tuning scheme to MASH-type CT $\Delta\Sigma$ modulators, since MASH-type CT $\Delta\Sigma$ modulators have less severe stability problems but require highly accurate time-constants for noise cancellation.

References

[1] W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 7931–1936, Dec. 2001.

[2] A. M. A. Ali, C. Dillon, R. Sneed, A. S. Morgan, S. Bardsley, J. Kornblum, and L. Wu, "A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1848–1855, Aug. 2006.

[3] U.-K. Moon and B.-S. Song, "Background digital calibration techniques for pipelined ADCs," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 2, pp. 102–109, Feb. 1997.

[4] S.-U. Kwak, B.-S. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1866–1875, Dec. 1997.

[5] O. E. Erdogan, P. J. Hurst, and S. H. Lewis, "A 12-b digital-background-calibrated algorithmic ADC with −90-dB THD," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1812–1820, Dec. 1999.

[6] X. Wang, P. J. Hurst, S. H. Lewis, "A 12-bit 20-Msample/s pipelined analog-to-digital converter with nested digital background calibration," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1799–1808, Nov. 2004.

[7] E. Siragusa and I. Galton, "Gain error correction technique for pipelined analog-to-digital converters," *Electron. Lett.*, vol. 36, pp. 617–618, Mar. 2000.

[8] E. Siragursa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[9] H.-C. Liu, Z.-M. Lee, and J.-T. Wu, "A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1047–1056, May. 2005.

[10] P. Bogner, F. Kuttner, C. Kropf, T. Hartig, M. burian, and H. Eul, "A 14b 100MS/s digitally self-calibrated pipelined ADC in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 224–225.

[11] J. Li and U.-K. Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 9, pp. 531–538, Sep. 2003.

[12] K. Nair and R. Harjani, "A 96dB SFDR 50MS/s digitally enhanced CMOS pipeline A/D converter," *ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 456–457.

[13] B. Murmann and B. E. Boser, "A 12-b 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[14] J. P. Keane, P. J. Hurst, S. H. Lewis, "Background interstage gain calibration technique for pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 1, pp. 32–43, Jan. 2005.

[15] I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 185–196, Mar. 2000.

[16] P. C. Yu, S. Shehata, A. Joharapurkar, P. Chugh, A. Bugeja, X. Du, S. U. Kwak, Y. Papantonopoulous, and T. Kuyel, "A 14b 40Msample/s pipelined ADC with DFCA," *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 136–137.

[17] S.-T. Ryu, S. Ray, B.-S. Song, G.-H. Cho, and K. Bacrania, "A 14-b linear capacitor self-trimming pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2046–2051, Nov. 2004.

[18] J. Ming and S. H. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1489–1497, Oct. 2001.

[19] R. Jewett, K. Poulton, K.-C. Hsieh, and J. Doernberg, "A 12b 128Msample/s ADC with 0.05LSB DNL," *ISSCC Dig. Tech. Papers*, Feb. 1997, pp. 138–139.

[20] Y.-S. Shu and B.-S. Song, "A 15b-linear, 20MS/s, 1.5b/stage pipelined ADC digitally calibrated with signal-dependent dithering," *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2006, pp. 270–271.

[21] B.-S. Song, S.-H. Lee, and M. F. Tompsett, "A 10-b 15-MHz CMOS recycling two-step A/D converter," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1328–1338, Dec. 1990.

[22] S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 954–961, Dec. 1987.

[23] T. Takemoto, M. Inoue, H. Sadamatsu, A. Matsuzawa, and K. Tsuji, "A fully parallel 10-bit A/D converter with video speed," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1133–1138, Dec. 1982.

[24] B.-S. Song, M. F. Tompsett, and K. R. Lakshmikumar, "A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1324–1333, Dec. 1988.

[25] H.-S. Chen, B.-S. Song, and K. Bacrania, "A 14-b 20-Msamples/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 997–1001, Jun. 2001.

[26] Y. Chiu, P. R. Gray, and B. Nikolic, "A 14-b 12-MS/s CMOS pipelined ADC with over 100-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2139–2151, Dec. 2004.

[27] P. C. Yu and H.-S. Lee, "A 2.5-V 12-b 5-Msample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1854–1861, Dec. 1996.

[28] S.-H. Lee and B.-S. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, Dec. 1992.

[29] A. N. Karanicolas, H.-S. Lee, and K. L. Bacrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, Dec. 1993.

[30] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[31] S. Sharma, G. Otomo, K. Tsukamoto, and T. Miyata, "A floating-point A/D converter uses low resolution DAC to get wide dynamic range," *Int. J. of Electronics*, vol. 64, pp. 787–794, May 1988.

[32] J. Yuan and J. Piper, "Floating-point analog-to-digital converter," *Proc. of IEEE ICECS*, vol. 3, pp. 1385–1388, Sep. 1999.

[33] F. Chen and C. S. Chen, "A 20-b dynamic range floating-point data acquisition system," *IEEE Trans. Ind. Electron.*, vol. 38, pp. 10–14, Feb., 1991.

[34] D. U. Thompson and B. A. Wooley, "A 15-b pipelined CMOS floating-point A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 299–303, Feb. 2001.

[35] V. Z. Groza, "High-resolution floating-point ADC," *IEEE Trans. Instr. and Meas.*, vol. 50, pp. 1822–1829, Dec. 2001.

[36] V. Groza, M. Debski, "Self-calibrating differential predictive floating-point analog-to-digital converter," *IEEE Trans. Instr. and Meas.*, vol. 50, pp. 1604–1606, May 2003.

[37] J. Piper and J. Yuan, "Realization of a Floating-point A/D converter," *Proc. of IEEE ISCAS*, vol. 1, pp. 404–407, May 2001.

[38] J. Piper and J. Yuan, "Design considerations of a floating-point ADC with embedded S/H," *Proc. of IEEE ISCAS*, vol. 6, pp. 6166–6169, May 2005.

[39] S. M. Jamal, D. Fu, N. C.-J. Chang, P. J. Hurst, and S. H. Lewis, "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, Dec. 2002.

[40] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 318–325, Mar. 2000.

[41] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, E. Romani, A. Melodia, and V. Melini, "A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz signal bandwidth and 12b ENOB," *ISSCC Dig. Tech. Papers*, pp. 62–63, Feb., 2006.

[42] L. J. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, and H. Termeer, "A 56mW CT quadrature cacaded ΣΔ modulator with 77dB DR in a near zero-IF 20MHz band," *ISSCC Dig. Tech. Papers*, pp. 238–239, Feb., 2007.

[43] S. Yan, E. Sanchez-Sinencio, "A continuous-Time ΣΔ modulator with 88 dB dynamic range and 1.1MHz signal bandwidth," *ISSCC Digest of Technical Papers*, pp.62–63, Feb. 2003.

[44] J. A. Cherry, W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 6, pp. 661–676, Jun. 1999.

[45] S. Luschas and H.-S. Lee, "High-speed ΣΔ modulators with reduced timing jitter sensitivity," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 11, pp. 712–720, Nov. 2002.

[46] R. van Veldhoven, "A tri-mode continuous-time ΣΔ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2069–2076, Dec. 2003.

[47] J. A. Cherry, W. M. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," IEEE Trans. Circuits Syst. II, vol. 46, no. 4, pp. 376–389, Apr. 1999.

[48] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 753–762, Dec. 1995.

[49] D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, "A self-calibration technique for monolithic high-resolution D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1517–1522, Dec. 1989.

[50] R. T. Baird and T. S. Fiez, "A low oversampling ratio 14-b 500-kHz delta–sigma ADC with a self-calibrated multibit DAC," *IEEE J. Solid-State Circuits*, vol. 31, pp.

312–320, Mar. 1996.

[51] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta–Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1997.

[52] Y. Tsividis and J. O. Voorman, *Integrated Continuous-Time Filters*. New York: IEEE Press, 1993.

[53] T. Viswanathan, S. Murtuza, V. Syed, J. Berry, and M. Staszel, "Switched-capacitor frequency control loop," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 4, pp. 775–778, Aug. 1982.

[54] Y. Tsividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C filters in VLSI," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 1, pp. 15–29, Feb. 1986.

[55] M. Banu and Y. Tsividis, "Fully integrated active RC filters in MOS technology," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 644–651, Dec. 1983.

[56] U. Moon and B. Song, "Design of a low-distortion 22-kHz 5th-order Bessel filter," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1254–1264, Dec. 1993.

[57] H. Khorramabadi and P. R. Gray, "High-frequency CMOS linear continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 6, pp. 939–948, Dec. 1984.

[58] V. Gopinathan, Y. Tsividis, K. Tan, and R. Hester, "Design consideration for high frequency continuous-time filter and implementation of an anti-aliasing filter for digital video," *IEEE J. Solid-State Circuits*, vol. 25, no. 12, pp. 1368–1378, Dec. 1990.

[59] J. Khoury, "Design of a 15-MHz CMOS continuous-time filter with on-chip tuning," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1988–1997, Dec. 1991.

[60] P. Kiss, J. Silva, A. Wiesbauer, A. Wiesbauer, T. Sun, U.-K. Moon, J. T. Stonick, and G. C. Temes, "Adaptive digital correction of analog errors in MASH ADC's—Part II: Correction using test-signal injection," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 7, pp. 629–638, Jul. 2000.