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Authors

Johnson, RP
DeWitt, J
Macafee, S
[et al.](#)

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A Fast Tracker Data Acquisition System for pCT

Robert P. Johnson, Joel DeWitt, Scott Macafee, Hartmut F.-W. Sadrozinski, *Senior Member, IEEE*,
David Steinberg, Andriy Zatserklyaniy

Abstract— We present a data acquisition design for a silicon-strip tracking system being constructed as part of a pre-clinical prototype scanner for proton computed tomography (pCT), capable of measuring one to two million proton tracks per second. The front end of the system is based on our ASIC design that handles 64 consecutive channels, including logic for control, calibration, buffering, and zero suppression. Each IC outputs a cluster list for each trigger, and a set of field programmable gate arrays merges those lists and builds the events to be sent to the data acquisition computer.

I. INTRODUCTION

Proton Computed Tomography (pCT [1]) holds promise to improve treatment planning for hadron therapy [2] by imaging the tissue in front of and inside the tumor with the same particles as used in the treatment. That will eliminate errors inherent in translating X-ray attenuation data into proton stopping power. However, implementation of pCT requires the proton trajectories and ranges to be measured one particle at a time. To accomplish that in an acceptable clinical time frame will require a tracking system that can measure the order of a million protons per second.

We are building such a system [3] to operate in the proton-synchrotron beam of the Loma Linda University Medical Center [4]. There the protons will arrive in bunches spaced at 120 ns intervals. Due to limitations of the energy detector, which unlike the tracker cannot handle multi-track events, we are interested only in single-proton bunches. That limits the practical trigger rate to about 1 MHz, for which about 7.5% of the acquired events will contain more than one proton. Our system design can accommodate trigger rates up to about 2 MHz, but with corresponding increases in the percentage of events with multiple protons.

Silicon strip detectors are nearly ideal candidates for the tracking portion of a pCT system. The relatively high cost per cm^2 of the sensors (relative to plastic scintillators, for example) is more than offset by their high performance, reliability, stability, and ease of assembly. Furthermore, the sensor cost would be a minor portion of the overall cost of a clinical system. Silicon strip detectors offer the following attractive characteristics, demonstrated in very large systems such as the Fermi-LAT Gamma-ray Space Telescope [5] and the CERN LHC tracking detectors:

- Near 100% efficiency for particle detection with essentially zero noise occupancy.
- Inherently fine spatial resolution.
- All solid-state, with simple calibration that is stable over time periods of many years.
- Compact and easy assembly using standard industry processes, with excellent mechanical stability.

II. DATA ACQUISITION ARCHITECTURE

Figure 1 gives an overview of the pCT tracker data acquisition. A pair of x,y layers precedes the subject to be imaged, and a second pair follows, to provide measurements of the entering and exiting proton trajectories. Twelve dozen ASICs are needed, and each of 8 FPGAs handles the data flow, as well as control, of 12 or 24 ICs. The FPGAs are mounted on the same printed circuit boards as the ASICs, as indicated in Figure 2. Each has a separate output serial link connecting to the event builder. The serial communications are made via LVDS, and 100 megabits/second is adequate speed.

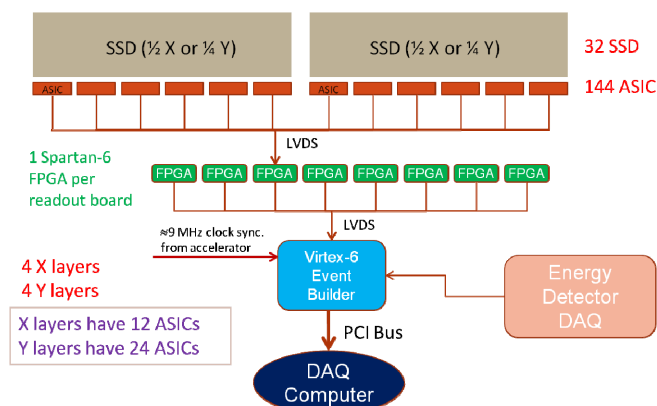


Figure 1. Overview of the pCT data acquisition.

The readout is triggered, by the energy detector and tracker, for ease of synchronization and event building, with ample buffering at the front end to minimize dead time. Eight layers of silicon strip detectors are read out by 144 64-channel ICs, each with a 100 Mbit/s link to an FPGA on the same board. The events of interest are sparse, with only a single proton passing through the tracker. An event data packet flowing from a front-end board to the event builder FPGA will typically consist of a single cluster (electronic-noise hits will be very rare and contribute negligibly to the data volume), so 100 Mbit/s capability on those data links is sufficient. The final link of an event to the computer will need to handle up to

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The authors are with the Santa Cruz Institute for Particle Physics and the Physics Department of the University of California at Santa Cruz, Santa Cruz, CA 95064, (telephone: 831-459-2125, e-mail: rjohnson@ucsc.edu).

about 1 Gbit/s. Either the event builder will be installed into the computer's PCI bus, or it will be linked by Ethernet.

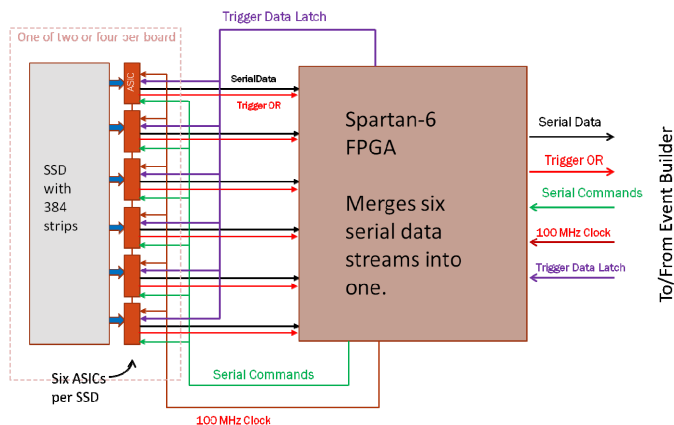


Figure 2. Simplified block diagram of a tracker readout board.

III. FRONT-END ASIC

Our existing prototype pCT instrument is based on front-end ASICs designed by the first author for the Fermi-LAT gamma-ray telescope [6], which has been operating flawlessly in orbit since June of 2008. That system design, with nearly 900,000 channels, emphasized low power and was intended to trigger at rates of a few kHz, using amplifiers with a two microsecond time constant. The new ASIC design, optimized for pCT, builds upon the Fermi-LAT experience but differs in several important aspects, mostly related to speed.

The common features are

- 64 channels, with a low-noise charge-sensitive amplifier and discriminator on each channel. The amplifiers are always live, acquiring data at all times, in particular during event readout.
- Buffering of up to four events, to transform the stochastic event arrival time into a smooth output data flow, thus minimizing dead time.
- An internal calibration system that allows an arbitrary set of channels to be pulsed with an externally specified input charge.
- A threshold that is common to the 64 channels but can be set by external command.
- An asynchronous output pulse that is the logical-OR of all channels, to be used as a trigger input (the Fermi-LAT tracking system is self triggering [7]).
- Programmable mask registers that can decouple individual channels from the trigger and/or data flow.
- A command interpreter that allows each IC to be individually configured by external digital commands.
- Serial LVDS input/output.

The following features have been incorporated into the new design to enhance the capability for pCT:

- Faster integration and CR/RC pulse shaping, with a selection between 200 ns versus 400 ns peaking times.
- Polarity selection, so that the chip could work on both sides of a double-sided silicon-strip detector.

- High and low gain selection (60 mV/fC and 15 mV/fC), to optimize the readout dynamic range for the higher ionization of protons exiting versus entering the subject.
- A digital one-shot on each channel, to detect the rising edge from the discriminator and output a short pulse of fixed (programmable) length, followed by a 32-sample deep storage pipeline (implemented in RAM) to hold the pulses pending a trigger decision. This is to ensure that protons in separate beam pulses will be kept separate in the data stream.
- Four parallel event processors that reduce the 64-bit channel hit list down to a zero-suppressed serial-encoded cluster list. The output stream specifies the starting channel of each cluster and the cluster length.

The pCT ASIC was manufactured in the TSMC 250 nm mixed-mode process (CM025 [8]), with the first chips received in September 2012. The analog circuitry runs at 3.3 V and 2.0 V, using 1.3 mW of power per channel. The digital circuitry runs at 2.5 V and uses 2.3 mW per channel at 100 MHz.

IV. ASIC TEST RESULTS

The ASIC is fully functional and suitable for operation in the pCT system, with excellent noise and channel-matching performance. It operates continuously at 100 MHz with no observable digital interference of the charge-sensitive amplifiers. The channel-to-channel threshold uniformity is excellent (2.5% rms variation across 64 channels), such that all channel thresholds may be set by a single DAC with no compromise of the efficiency or noise performance.

We measured the amplifier noise for the 200 ns peaking-time setting by using the internal calibration system to inject charge into selected channels while scanning the threshold across the transition from 100% efficiency to 0%. The efficiency curves were fit to complementary error functions, from which the noise sigma was determined. The measurements were done with disconnected channels, with channels connected to a single detector 9-cm strip (~11 pF), and with channels connected to two detector strips connected in series. The equivalent noise charge, averaged over channels, was

$$ENC = 282 + 34.7 \times C \text{ electrons}$$

with C in picofarads. For the longest strips in our pCT system, 18 cm (~22 pF), this corresponds to 1050 electrons ENC, compared to the 60,000 electron (9.5 fC) most probable signal from 250 MeV protons. This noise performance is better than needed for our pCT system, but the chip was designed also to work with thinner detectors and longer strips in a larger and more advanced system.¹

A more direct indicator of the noise performance comes from looking at the noise occupancy, measured by taking a million randomly timed triggers for each threshold setting, with 18 cm strips connected to the channels. The results are shown in Figure 3. Clearly we have a wide range for the

¹ The detectors now in use were left over from the Fermi-LAT project. Their thickness and strip pitch were optimized for that system.

threshold setting that will guarantee 100% efficiency for protons with zero hits from electronics noise.

Our demonstrated excellent ASIC signal-to-noise performance offers multiple important advantages to the pCT system. Only beam-related particles will make hits in the detectors, so there will be no electronic-noise hits present to confuse pattern recognition and increase the data volume. Furthermore, even the smallest proton signals will be far above threshold, thus minimizing time jitter of the threshold crossings and ensuring that all hits can be captured within the planned 100 ns window with efficiency very close to 100%. This is crucial, as the loss of even a single proton hit would make the event unusable for CT. The 100% hit efficiency will also allow us to treat the small (500 micrometer) gaps between detectors, as well as possible isolated dead detector strips, in a simple way. A missing hit in a single layer will indicate that the proton passed through such a gap, thus localizing it nearly as well as is accomplished by a hit strip.

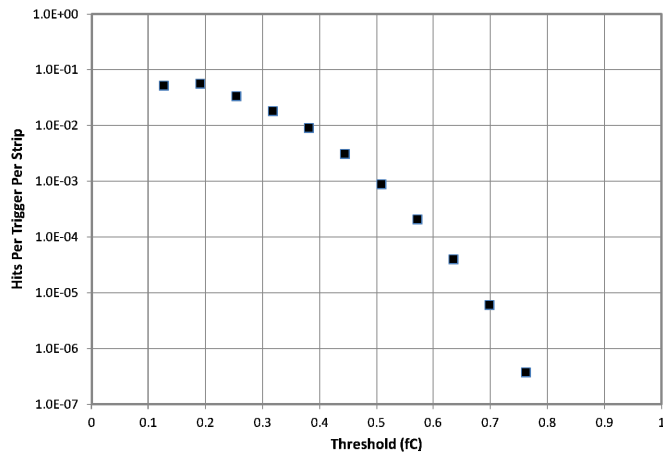


Figure 3. The noise occupancy measured from channels connected to 18 cm strips (~ 22 pF). Each point was measured from a million randomly timed triggers, each with a 150 ns window (a parameter that is adjustable on the chip).

V. DATA ACQUISITION SIMULATIONS

The pCT system has not yet been assembled and operated in an intense beam, but based on the excellent ASIC test results, in particular the negligible noise occupancy, together with Verilog simulations of the tracker data acquisition system, we have made reliable predictions of the system performance. The Verilog simulations were based on the schematic-extracted netlist of the ASIC, together with prototype data-acquisition code designed to run on the tracker-board FPGA (and already demonstrated to work on a test board that includes an FPGA, six ASICs, and silicon-strip sensor). The 9-MHz LLUMC proton-accelerator beam structure was simulated with a Poisson-distributed number of protons per beam pulse, for a total proton rate of 1.27 million per second, with at least one proton in each of 13% of the beam pulses. The detectors were simulated with hits distributed uniformly across the active area, with one or two strips per cluster. Random noise hits were pessimistically added at an occupancy of 10^{-4} per strip per trigger. The ASICs and the data acquisition were pessimistically simulated with a 60 MHz

clock and 60 Mbps LVDS data transfer rates from ASIC to FPGA, as well as from FPGA to event builder.

The resulting dead-time fraction was 6%, with the front-end buffers occupied as shown in the table below. That yielded a trigger rate of 1.04 MHz, for which 7.5% of the triggered events had more than one proton (and therefore would not be usable). With a 100 MHz clock the simulated dead time dropped to a negligible level under the same assumptions.

TABLE I. SIMULATED BUFFER OCCUPANCY (60 MHz CLOCK)

Number of Buffers Occupied	Fraction of Simulation Time
0	10.6%
1	27.1%
2	32.0%
3	21.9%
4	8.3%

CONCLUSION

The pCT tracker system is a work in progress that will be completed and tested in the coming year. We already have in hand the ASICs, which we have shown to satisfy all of the requirements of the project, and we have verified by simulation that the system design will deliver the high trigger and data rates demanded by the preclinical prototype pCT scanner.

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