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Title

Hierarchical In-Network Processing

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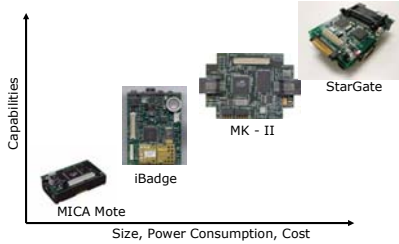
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Hierarchical In-Network Processing

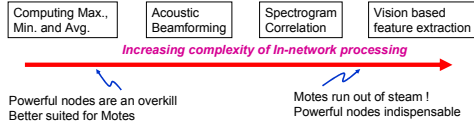
Ram Kumar, Vlasios Tsiatis, Mani B Srivastava
 Networked and Embedded Systems Lab (NESL) – <http://nesl.ee.ucla.edu>

Introduction: Exploit the heterogeneity

Diversity in Sensor Node Platforms



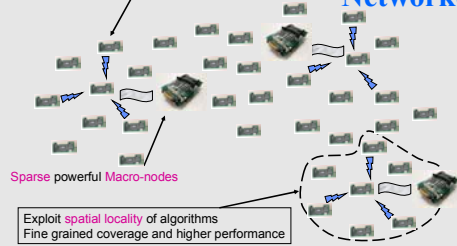
Why heterogeneous systems ?



- **Solutions ?**
 - Reconfigurable sensor nodes
 - FPGA: High standby power consumption is a show stopper
 - Stacked Arch.: PASTA Node USC/ISI – High cost of individual nodes, prohibitively expensive
 - **Exploit the heterogeneity of the sensor node platforms !**

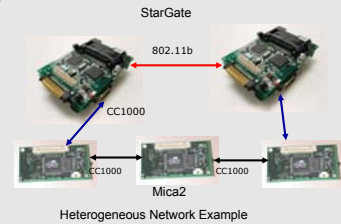
Problem Description: Heterogeneous Sensor Networks

Dense resource constrained Micro-nodes



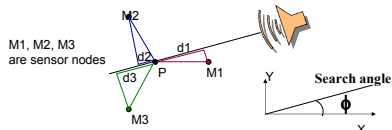
Networked System Architecture Design Challenges

- **Energy efficient application partitioning and mapping**
 - Influenced by the architecture for nodes
 - Complexity of mapped tasks
- **Determining the optimal network composition**
 - Number of macro-nodes and micro-nodes
 - Latency of data transfer is critical
 - Cost vs. performance trade-offs
- **Self-configuration mechanism**
 - Cluster micro-nodes based on proximity to macro-node
 - Offload computation onto the macro-node in the cluster



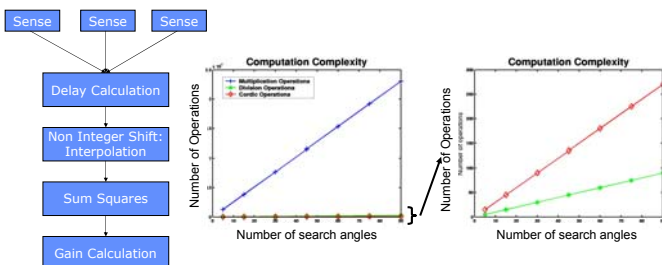
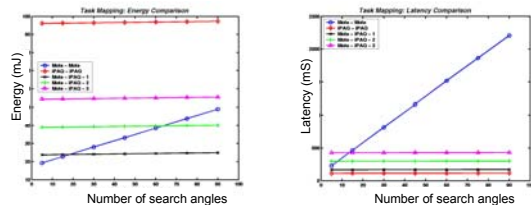
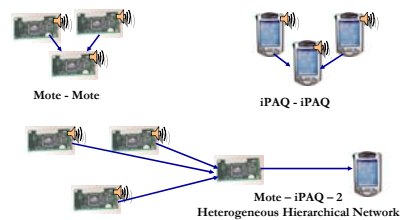
Proposed Solution: Hierarchical organization of Acoustic Beamforming application

Target Tracking Application

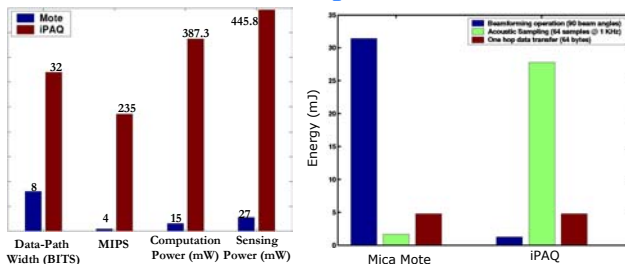


- Parametric, **Time-domain Line of Bearing** computation
- Sound source located **far away** from the sensor nodes
- Sensor nodes try estimate the **angle of arrival** of signal
- **Accuracy depends on number of search angles**
 - More search angles implies better accuracy

LOB Energy and Latency Measurements



Architecture Comparisons



Node Density Effects

