UNIVERSITY OF CALIFORNIA, SAN DIEGO

Low Power High Performance Interconnect Design and Optimization

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in
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by

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2009

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Chair

University of California, San Diego

2009

DEDICATION

To my family.

TABLE OF CONTENTS

Signature Page . . . iii

Dedication . . . iv

Table of Contents . . . v

List of Figures . . . vii

List of Tables . . . viii

Acknowledgements . . . ix

Vita, Publications, and Fields of Study . . . xi

Abstract of the Dissertation . . . xiii

I Introduction . . . 1
1. Interconnect Design Challenges . . . 1
2. Related Works . . . 5
A. Repeated On-chip RC Wires . . . 5
B. On-chip Transmission Line . . . 6
C. Off-chip Transmission Line . . . 7
3. Eye Diagrams . . . 8
A. Dissertation Outline . . . 9

II On-chip repeated RC wire . . . 11
1. Backgrounds . . . 11
A. Wire characteristics . . . 11
B. Repeater characteristics . . . 13
2. Delay modeling . . . 15
3. Power modeling . . . 17
4. Evaluation metrics . . . 18
5. Optimization of different design goals . . . 18
A. Definition of design goals . . . 18
B. Evaluation procedure . . . 19
C. Analysis of min-d procedure . . . 19
6. Experiments . . . 20
A. Experimental setup . . . 21
B. Optimal wire configuration . . . 22
C. Metric evaluation . . . 27
7. Summary . . . 35

III On-Chip Transmission Line . . . 39
1. Introduction . . . 39
A. Basic theory of transmission Line . . . 39
B. Existing works . . . 42
2. Our signaling scheme using on-chip transmission line . . . 43
A. Wire modeling . . . 43
B. Driver and receiver design and modeling . . . 47
C. Evaluation metrics . . . 49
3. Problem formulation and optimization framework . . . 50
A. Problem formulation . . . 50
B. Optimization framework . . . 51
4. Experimental results . . . 53
A. Experimental setup . . . 54
B. Comparison of the transmission line and the repeated RC wires 54
5. Summary . . . 64

IV Off-Chip Transmission Line . . . 66
1. Introduction . . . 66
2. Equalization topologies and schemes . . . 69
A. Equalization topologies . . . 69
B. equalization schemes . . . 70
3. Analysis and comparison of the equalization topologies . . . 72
A. RL structure . . . 73
B. RC structure . . . 74
C. T-junction structure . . . 76
D. Comparison . . . 78
4. Problem formulation and optimization framework . . . 79
A. Problem formulation . . . 80
B. Optimization framework . . . 82
5. CPU-memory links in IBM POWER6 system . . . 83
6. Experimental results . . . 84
A. Experimental setup . . . 84
B. Optimization results without size limits . . . 85
C. Optimization results with size limits . . . 98
7. Summary . . . 105

V Conclusions . . . 110
1. Summary of contributions . . . 110
2. Future work . . . 111

Bibliography . . . 112

LIST OF FIGURES

Figure I.1: Delay of metal 1 and global wiring versus gate(10FO4 delay) 2
Figure I.2: Energy per bit of metal 1 and global wiring versus gate (10FO4 energy per bit) 3
Figure I.3: Delay energy product of metal 1 and global wiring versus gate (100FO4 delay energy product) 3
Figure I.4: Bandwidth of metal 1 and global wiring 4
Figure I.5: A representative eye diagram 9

Figure II.1: A simple wire capacitance model 12
Figure II.2: Test circuit for measuring the transistor output resistance 14
Figure II.3: RC model of the test circuit, (a) Rising delay, (b) Falling delay 14
Figure II.4: Delay model of the repeated RC wire 15
Figure II.5: Optimal wire widths 23
Figure II.6: Optimal repeater sizes 24
Figure II.7: Optimal repeater intervals 25
Figure II.8: Overview of normalized delay 28
Figure II.9: Normalized delay at 22nm technology 29
Figure II.10: Overview of normalized power 31
Figure II.11: Normalized power at 22nm technology 32
Figure II.12: Overview of bandwidth 33
Figure II.13: Bandwidth at 22nm technology 34
Figure II.14: Overview of bandwidth over power 36
Figure II.15: Bandwidth over power at 22nm technology 37

Figure III.1: RLGC model of a transmission line segment 40
Figure III.2: The proposed signal scheme for global communication: (a) one stage structure; (b) transceiver structure 44
Figure III.3: The cross section of the differential stripline we use 45
Figure III.4: Double-tail sense amplifier [54] 48
Figure III.5: The optimization framework 52
Figure III.6: Normalized delay comparison between repeated RC wire and the proposed on-chip T-line 55
Figure III.7: Normalized energy per bit comparison between repeated RC wire and the proposed on-chip T-line 55
Figure III.8: Normalized throughput comparison between repeated RC wire and the proposed on-chip T-line 56
Figure III.9: $delay_n$ of different wire spacing for min-d at 45nm technology 60
Figure III.10: $delay_n * power_n$ of different wire spacing for min-dp at 45nm technology 61

Figure III.11: $delay_n^2 * power_n$ of different wire spacing for min-ddp at 45nm technology . . . 62
Figure III.12: Throughput of different wire spacing at 45nm technology 63

Figure IV.1: A channel with equalizers at the driver and the receiver . 67
Figure IV.2: The frequency response of the equalizer, the channel w/ and w/o equalization . . . 68
Figure IV.3: Constant-R ladder: input impedance is R when $z_1 z_2 = R^2$ 68
Figure IV.4: equalization components: (a) T-junction (b) R-C (c) R-L 70
Figure IV.5: Transfer function of the channel . . . 72
Figure IV.6: block diagrams of equalizer at (a)driver, (b)receiver 73
Figure IV.7: Transfer functions of RL, channel w/ and w/o using RL . 74
Figure IV.8: Transfer functions of RC, channel w/ and w/o using RC . 75
Figure IV.9: Transfer functions of T-junction, channel w/ and w/o using T-junction . . . 77
Figure IV.10: Optimization flow . . . 82
Figure IV.11: Structure of the CPU-memory link . . . 84
Figure IV.12: Transfer functions of solutions in Table IV.4 . . . 90
Figure IV.13: Step response (0 to 8ns) of solutions in Table IV.4 . . . 91
Figure IV.14: Step response (3ns to 4ns) of solutions in Table IV.4 . . . 92
Figure IV.15: Transfer functions of solutions in Table IV.5 . . . 93
Figure IV.16: Step responses of solutions in Table IV.5 . . . 94
Figure IV.17: Transfer functions of solutions in Table IV.6 . . . 95
Figure IV.18: Step responses of solutions in Table IV.6 . . . 96
Figure IV.19: Transfer functions of solutions in Table IV.7 . . . 97
Figure IV.20: Step responses of solutions in Table IV.7 . . . 98
Figure IV.21: Eye diagrams of M+M . . . 101
Figure IV.22: Eye diagrams at input port . . . 102
Figure IV.23: Eye diagrams at TXPKG . . . 103
Figure IV.24: Eye diagrams at port RXPKG . . . 104
Figure IV.25: Eye diagrams at output . . . 105
Figure IV.26: Transfer functions of different schemes . . . 106
Figure IV.27: Step responses of different schemes . . . 107
Figure IV.28: Step responses between 3ns and 4ns of different schemes . 107
Figure IV.29: Input impedances of different schemes . . . 108
Figure IV.30: Eye diagrams at higher data rate . . . 108
Figure IV.31: Eye diagrams at output with crosstalk effect . . . 109

LIST OF TABLES

Table I.1: Single-chip packages technology trend for high performance applications [34] 4

Table II.1: Technology data for repeated RC wire experiments 21

Table III.1: Design parameters 46
Table III.2: The latency of transceiver (unit: ps) 54
Table III.3: The power of transceiver (unit: uW) 54

Table IV.1: Usages of topologies 71
Table IV.2: Groups of schemes according to the matching conditions . 72
Table IV.3: Optimization variables for each component 80
Table IV.4: Optimization results of Group 1 without size limit 86
Table IV.5: Optimization results of Group 2 without size limit 87
Table IV.6: Optimization results of Group 3 without size limit 88
Table IV.7: Optimization results of Group 4 without size limit 89
Table IV.8: Optimization results of Group 1 and 2 with size limit . . . 99
Table IV.9: Optimization results of Group 3 and 4 with size limit . . . 100
Table IV.10: Sensitivity comparison 104

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L. Zhang, W. Yu, H. Zhu, A. Deutsch, G. A. Katopis, D. M. Dreps, E. Kuh, C-K Cheng, "Low Power Passive Equalizer Optimization Using Tritonic Step Response", *Proceedings of IEEE/ACM Design Automation Conference (DAC 2008)*

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ABSTRACT OF THE DISSERTATION

Low Power High Performance Interconnect Design and Optimization

by

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Professor Chung-Kuan Cheng, Chair

As technology scales, interconnect planning has been widely regarded as one of the most critical factors in determining the system performance and total power consumption. As the result of shrinking dimension, on-chip wires are getting more resistive, and the delay is becoming larger comparing to gate delay. On the other hand, the self capacitance of wires does not scale with feature size, and as wiring density grows, the total coupling capacitance increases, which results in substantial increment of interconnect power consumption. Meanwhile, off-chip interconnect is also becoming a limiting factor for system performance since the growth of chip's I/O bandwidth has been outpaced by the growth of communication. To meet the performance challenge, the per-pin interconnect bandwidth must be further improved with given power budget.

For on-chip interconnect, buffer insertion has been adopted to reduce the signal delay. However, the added buffers require extra power consumption and increase routing complexity. In this dissertation, we investigate a set of interconnect performance metrics, optimize the repeated on-chip wires under different design goals and compare the performance metrics of optimum results. The quantitative delay-energy trade-offs for different design goals are demonstrated.

Even with repeaters, nominal on-chip global wires still can not keep up with the pace of gate scaling. We propose a high speed signaling scheme using transmission line properties to address the performance issue. The transmission

line allows the signal to travel at the speed of light in the medium. The signal toggles as wave instead of enforced electronic charges and thus saves power. However, the inter-symbol interference (ISI) limits the communication bandwidth. We use passive compensation to alleviate the ISI and develop an optimization flow for a given technology and wire dimension. We compare the nominal repeated wires with the transmission lines under different design goals.

For off-chip serial links, we propose a set of passive equalization schemes to enhance the performance with low power consumption. We apply the schemes to the CPU-memory links using IBM POWER6 system as a test vehicle. An optimization flow is devised to optimize the parameters of the equalizers. We derive the performance improvement and power consumption of the proposed schemes. We also demonstrate the sensitivities to the variations of RLC parameters and noise.

I

Introduction

I.1 Interconnect Design Challenges

The importance of interconnect has dramatically risen over the last twenty years. For chip designers, they have experienced the migration from gate-centric design to interconnect-centric design, which was caused by the big gap between the scaling of transistors and wires. Before 1990s, on-chip wires could be treated as pure capacitive loads of logic gates because the wire resistance and the RC constant is negligible. As technologies advances, both transistor size and wire size are shrinking. Comparing to the decreasing gate delay, the wire resistance and its contribution to the wire RC constant can be no longer ignored. According to the report from International Technology Roadmap for Semiconductor (ITRS) [34] we generate the delay, energy per bit, delay energy product and bandwidth comparisons of local and global wire versus gates in Fig. I.1 through I.4. For the wires with repeater insertion, the repeater is added to minimize the total latency ([4], [39]). For gates, we consider 10-stage FO4 delay and power to demonstrate the value typical to combination logics. We observe that local wire has the largest delay if we do not consider wire length scaling. However, 1mm wire length is very common for global wires. Even with repeaters, global wires still become slow comparing to logic gates after 32nm. Meanwhile, inserting repeaters almost doubles the wire

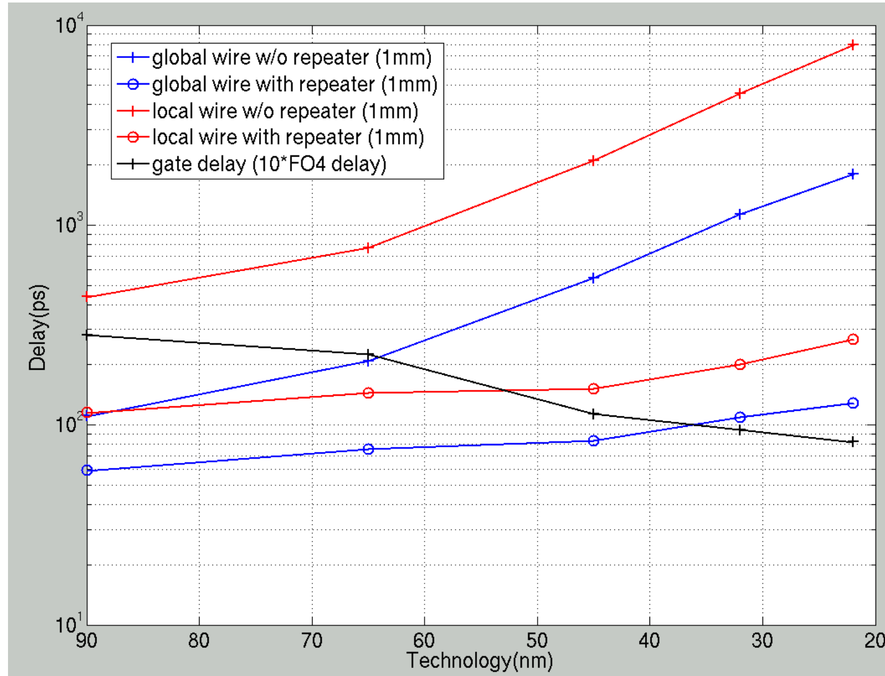

Figure I.1: Delay of metal 1 and global wiring versus gate(10FO4 delay)

power consumption, as shown in Fig. I.2, and it also has extra cost on chip area. Generally speaking, wires are more expensive than gates in terms of power and delay energy product. In [44], Magen et al. found that interconnect power alone accounted for half the total dynamic power of a 0.13um microprocessor that was designed for power efficiency. Designers need to understand how to manage the delay-power trade-offs of repeated RC wires as technology scales. Fig. I.3, I.4 illustrate the delay energy product and bandwidth of global and local wires for reference.

On-chip transmission line attracts intensive research focus in resent years as typical repeated RC wires are not sufficient to support future high-speed microprocessors. Transmission lines allow the signal to travel at the speed of light in the medium, and the signal toggles as wave instead of enforced electronic charges so that power consumption can be reduced. However, transmission lines suffer from the inter-symbol interference (ISI) when frequency goes higher, which can be a limiting factor for pushing ultra-high bandwidth on-chip communication. In order

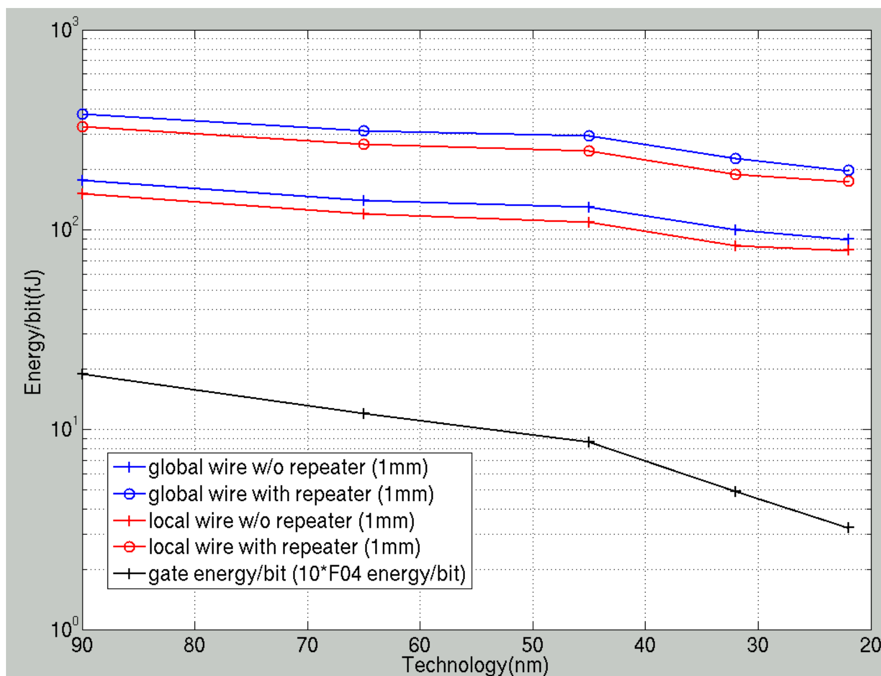

Figure I.2: Energy per bit of metal 1 and global wiring versus gate (10FO4 energy per bit)

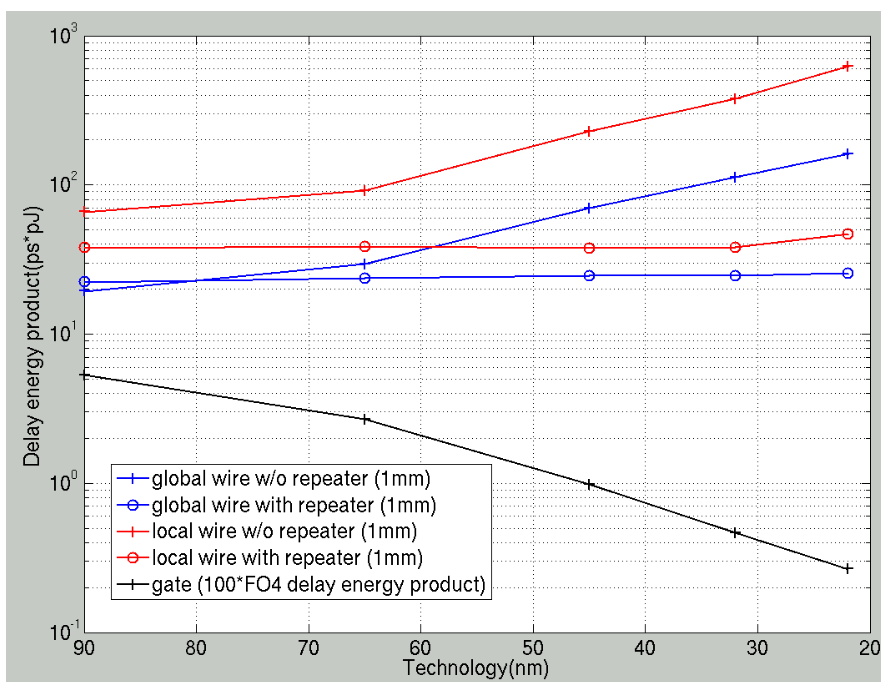

Figure I.3: Delay energy product of metal 1 and global wiring versus gate (100FO4 delay energy product)

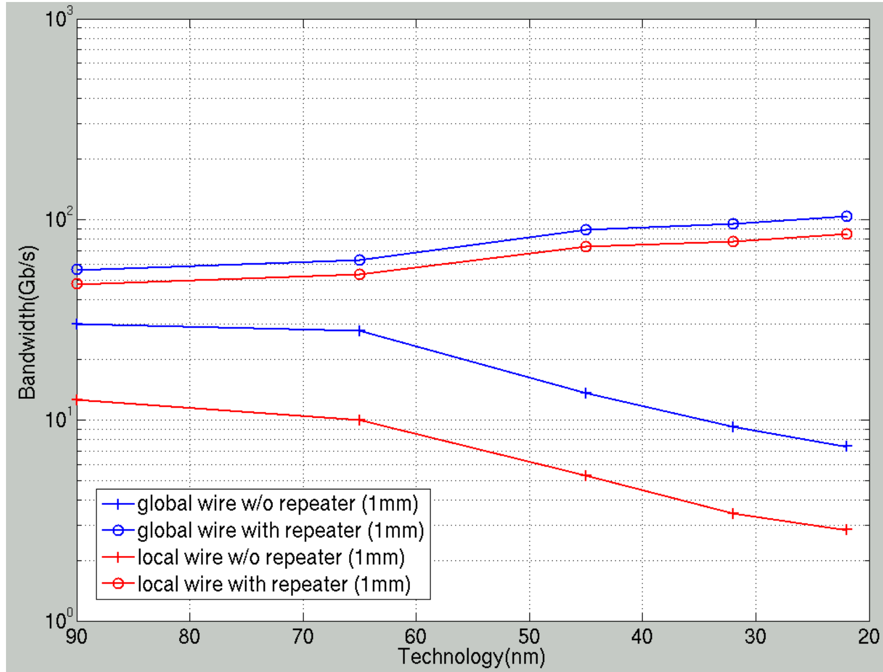

Figure I.4: Bandwidth of metal 1 and global wiring

Table I.1: Single-chip packages technology trend for high performance applications [34]

year	2005	2007	2010	2013	2015
Technology node(nm)	90	65	45	32	22
Package pincount	3000	3371	4015	4736	6191
Cost per pin(cents/pin)	1.78	1.71	1.61	1.51	1.21
Maximum power (Watts/mm^2)	0.54	0.61	0.64	0.64	0.46

to make transmission lines competitive in practice, the performance and power efficiency of drivers and receivers need to be improved. Like the repeaters in RC wires, extra transceivers can be inserted to make the on-chip transmission lines scale with technology. A unified optimization framework including both wires and transceivers is needed to improve the bandwidth.

As the device density and operating frequency of integrated circuit (IC) are growing rapidly, the demand for high-bandwidth off-chip communication is imposing an ever great challenge to system designers, which follows the prediction

of Rent's rule [42]: $B \propto n^p f$, in which B is the bandwidth required by a component, n is the number of devices in the component, f is the operating frequency and p is a "constant" depending on the type of component, typically in range of 0.4 to 0.8. According to the ITRS report [34](Table. I.1), the number of chip I/Os has been doubled, but the increment speed still can not bring the growing gap between I/O bandwidth demand and I/O bandwidth available. To continuously scale the overall digital system performance, the per-pin interconnect bandwidth must be further improved with reasonable power budget.

I.2 Related Works

I.2.A Repeated On-chip RC Wires

Repeater insertion technique was proposed first by Bakoglu and Meindl in 1985 ([6]), and they derived the delay expression for repeated RC wire and the optimal number and optimal size of repeaters to minimize the total latency ([6], [5]). [39], [46] discussed the closed form expression for minimum latency based on different transistor models.

However, people found that minimum delay repeater insertion consumes large chip area and burns a lot of power, which motivates researchers to determine the metrics in interconnect design so as to better understand the trade-offs between different metrics. [19], [45], [62] considered the area and power consumption when optimize the wires. An optimal repeater insertion technique to reduce the total power dissipation was explored in [26], [7]. There are also works focusing on tapered-buffer repeater insertion [2] and misaligned repeater insertion [65]. For the energy-delay optimization, much work [10], [59], [70] has been done from the gate level to the architecture level optimization. [10], [59] focused on finding the energy-delay trade-offs on devices via gate sizing, supply voltage and threshold voltage optimization, while [70] concentrates on evaluating the energy-delay trade-offs both in circuit and architectural level by defining hardware intensity.

Besides latency, bandwidth, or throughput (i.e. the number of bits per second) is considered an important metrics of wire performance in recent years. The idea of wave-pipelining is adopted for repeated global wires so that multiple signals are running on the wire and therefore throughput is greatly enhanced. [66] exploited techniques to design timing and synchronization circuits that tolerate the wire delay variation, and [16] derived an analytical expression to calculate the throughput of the wave-pipelined interconnects.

I.2.B On-chip Transmission Line

As signaling frequency keeps soaring, the transmission line effect can be no longer ignored for long and fat global wires, and the conventional RC model results in substantial underestimation of both crosstalk and delay. [14], [17]and [35] presented several methods to characterize the importance of transmission line effects. Due to skin effect, proximity effect and return current distribution, the wire characteristics (i.e., attenuation, phase velocity and characteristic impedance) are strongly frequency dependent and this makes the wire modeling more complex.

To alleviate the ISI, resistive termination is used in many on-chip transmission line schemes([63], [23]) to obtain higher bit-rate by suppressing DC voltage magnitude. [23]derived a simple terminator expression for maximum bandwidth, while [63] gave an expression for maximum eye opening. However, there is a static current flowing through the termination resistor that introduces static power dissipation and therefore a trade-off between the bandwidth and power exists.

Due to attenuation, the received signal at the far end of transmission line is usually a low-swing signal, and special receiver circuitry is used to recover it back to full-swing. The delay and power of driver/receiver contributes to the overall system performance and power, therefore carefully design is needed. [30] and [31] use current mode logic(CML) driver followed by an inverter chain at both receiver and driver sides, while [36] used differential amplifier and a single CMOS inverter as driver and receiver.

As an important approach to reduce the ISI, the idea of equalization has been widely used and various equalization schemes have been developed for off-chip communication channels. Equalization can be realized at driver side (usually referred as pre-emphasis) and receiver side. Both seek to either emphasize the high-frequency components in transmitted signal or to de-emphasize the low frequency components in received signal. Equalizers can be implemented with active or passive components. As chip frequency keeps increasing, equalizers are also used for on-chip interconnects to push the communication bandwidth. In [55], a simple and robust pulse-width pre-emphasis was adopted as driver to increase throughput with little overhead of power consumption. [40] proposed an optimization framework to optimize the active equalizers at driver and receiver sides.

I.2.C Off-chip Transmission Line

Off-chip high speed links have raised much research interest in both industry and academia due to the critical need for off-chip bandwidth. Interconnections between chips are moving from traditional multi-drop buses, such as Peripheral Component Interface (PCI) [48], to point-to-point links, such as PCI-express, RapidIO interconnect [53] and Redwood parallel interface [52]. The reason is that multi-drop buses suffer from impedance mismatches which limit the switching frequencies, and the capacitive loading and stub effects which limits the bus scalability. As apposed to multi-drop buses, point-to-point links provide tight control of electrical parameters of the bus and therefore enable higher operating frequencies. Moreover, point-to-point links can more easily employ techniques such as equalization to improve bandwidth further.

Point-to-point links can be serial links or parallel buses. Parallel buses can provide higher bandwidth by increasing clock frequency or the width of the bus, and it has lower latency because the drivers and receivers are simple. However, the number of pins available limits the bus width, and routing can be challenging since signal trace lengths have to precisely match the length of clock trace. Compared

with parallel buses, serial links use fewer pins and avoid the trace-matching problem by embedding clock into data stream. By doing this, the component costs and board layout complexity are reduced. One of the disadvantages of serial links is the large latency introduced by complex transceivers, serialization/deserialization, encoding/decoding and clock recovery.

Various equalization techniques have been used for off-chip interconnects more than a decade. For active equalization, FIR (Finite Impulse Response) filters are generally used ([60], [15], [22], [24], [21]), and the filters can be optimized for a given communication channel. However, active equalizers face significant challenges due to increasing power consumption and latency. Passive equalizers are attractive alternative solution because they minimize the extra power consumption and latency ([57], [61]). Passive equalizers can be implemented on-chip, on-package or on-board. On-chip equalizers can incorporate tunability, but use significant chip area. On-board equalizers use discrete components but increase the component cost and consume board area. On-package equalizers can avoid the shortcomings of the other two approaches by using dedicated package layers and lithography to build the passive components.

I.3 Eye Diagrams

Eye diagrams will be used throughout the rest of the dissertation and therefore, we discuss the definition of eye diagrams in this section. Eye diagrams are the most commonly accepted method to quantitatively describe the signal integrity. It is formed by overlapping the time domain waveform of a signal with multiple symbol periods, and it is given the name of eye diagram because the shape appears like a human eye. Fig. I.5 illustrates a representative eye diagram, in which the **eye opening** is defined as the voltage difference between the minimum high level voltage and the maximum low level voltage, and the **jitter** is the timing difference between the fastest and slowest arrival time at half of supply voltage.

Eye diagrams provide a straightforward demonstration of the impacts of

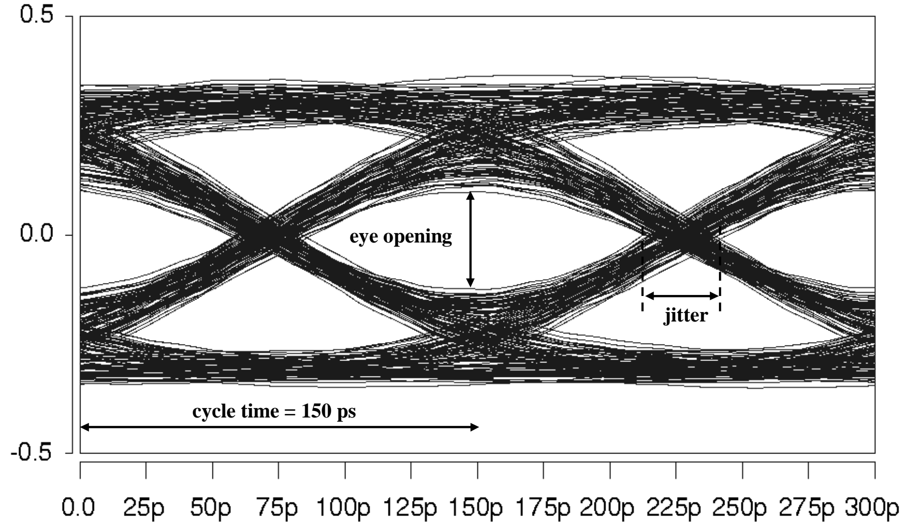

Figure I.5: A representative eye diagram

inter-symbol interference and noise upon the received signal quality and how to determine the sensing time of a specific receiver with certain input voltage margin requirement.

To generate the eye diagram by circuit simulation, input stimulus with pseudo random bit sequence (PRBS) is usually used. The bit length should be long enough, often several hundreds or thousands of bits, to capture the eye pattern in the worst case, which makes the simulation very time consuming. When the system of interest is a linear time invariant (LTI) system, superposition holds and pulse response([11]) or step response([67], [69]) can be utilized to derive the worst case eye.

I.3.A Dissertation Outline

Chapter II takes a close look at the repeated RC wires. We consider three design goals of minimizing delay, delay power product and delay-sqare power product. We define metrics of normalized delay, normalized power and normalized bandwidth to measure the performance of different wires. We show that how different design goals affect the wire performance, and how the wire performance scales with technologies.

Chapter III proposes a novel on-chip signaling scheme using transmission line. A parallel RC circuit is used at driver side to compensate the attenuation at high frequency. A double-tail sense amplifier followed by an inverter chain is used as transceiver. We use Sequential Quadratic Programming method to optimize the proposed signaling scheme under different design goals across five technologies and we compare the transmission line scheme with repeated RC wires in terms of latency, power and bandwidth.

In Chapter IV, a set of simple and effective passive equalizer are proposed. We employ the equalization schemes to the CPU-memory link of IBM POWER6 system and observe significant performance improvement with little power overhead. We also analyze and compare different schemes in terms of eye-opening, jitter and power. We demonstrate that our approach is not sensitive to RLC variations and robust to noise.

Chapter V concludes the dissertation and discusses possible future directions.

II

On-chip repeated RC wire

In this chapter we take a close look at the repeated RC wires. First we introduce basic definitions and parameters fundamental to RC wire characterization. Then we discuss the deterministic factors for repeated RC wire performance. We consider three design goals of minimizing delay, delay power product and delay-square power product. We define metrics of normalized delay, normalized power and normalized bandwidth to measure the performance of different wires. We show how different design goals affect the wire performance, and how the wire performance scales with technologies.

II.1 Backgrounds

II.1.A Wire characteristics

Generally speaking, wires on ICs are pieces of metal which have very low resistivity. However, as the wire dimension (wire thickness and wire width) shrinks dramatically, the wire resistance plays an important role. If we assume current flows through the wire uniformly, and the wire has a rectangular cross section, then the wire resistance per unit length is:

$$r_w = \frac{\rho}{wt} \qquad \text{(II.1)}$$

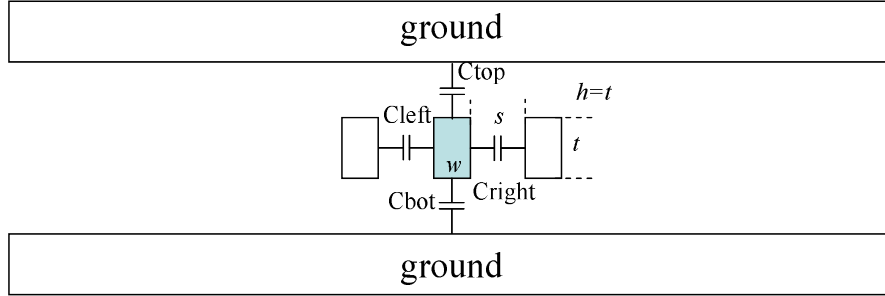

Figure II.1: A simple wire capacitance model

where ρ is the resistivity of the wiring material, and w, t are wire width and thickness, respectively. The resistivity of copper is $2.2u\Omega cm$. For the 90nm technology in [34], minimum global wire width is $w = 150nm$ and thickness is $t = 330nm$. The corresponded r_w is $444k\Omega$ per meter, or 0.44Ω per micron.

In manufacture, copper is encapsulated by a thin barrier layer to avoid diffusing into the surrounding oxide which results higher resistivity of the material. Moreover, electrons inelastically scatter off lattice bonds at the edges of wires, and this reduces the mean free path of electrons, which also increases the resistivity. The effective resistivity included in [34] considers both effects into account.

Wires also have capacitance since charges must be added to change the wires potential. A very simple capacitance model is shown in Fig. II.1 where a wire is surrounded by ground plans on top and bottom, and two neighbor wires at left and right. Thus, four parallel-plate capacitors can be used to model the wire total capacitance.

$$c_w = c_{top} + c_{bot} + c_{left} + c_{right} = 2c_{top} + 2c_{right} \tag{II.2}$$

in which we assume the top and bottom, left and right are symmetric. By the definition of parallel-plate capacitor, we have

$$c_{top} = \epsilon \frac{w}{h}, c_{right} = \epsilon \frac{t}{s} \tag{II.3}$$

where ϵ is the dielectric constant of the material. More often, wire pitch $p = w + s$ is used instead of wire spacing, and if we assume the dielectric height between

ground and wire equals the wire thickness, the above relations can be written as

$$c_{top} = \epsilon \frac{w}{t}, c_{right} = \epsilon \frac{t}{p - w} \tag{II.4}$$

and the total capacitance is

$$c_w = \epsilon (\frac{2w}{t} + \frac{2t}{p - w}) \tag{II.5}$$

When the adjacent wire switches in an opposite direction, c_{left} and/or c_{right} double since twice charges are needed to establish the new potential on the center wire. If the adjacent wire switches in the same direction, then c_{left} and/or c_{right} equal zero. (II.5) presents the capacitance for average case, which means neighbor wires don't switch to worsen or improve the coupling.

This relation is simple but it doesn't consider all the fringing effects. For accurate calculation, (12) through (15) in [58] can be used, which has less than 5% error compared to RC extraction results.

II.1.B Repeater characteristics

Repeater, or called inverter, is a non-linear device. Circuit simulation is needed to have its accurate timing waveform. When only delay is concerned in interconnect evaluation, RC delay models ([64]) is very useful. These models approximate the nonlinear transistor characteristics with and average resistance and capacitance over the switching range of the gate. There are three parameters in the switch level RC delay model of a repeater: the input gate capacitance c_{gate}, the output resistance r_d, and the output diffusion capacitance c_d. Usually diffusion capacitance is assumed to equal gate capacitance. All these parameters are related to the transistor size (the ratio of the gate width to the gate length). If a unit transistor has gate capacitance c_0 and output resistance r_0, a transistor of s times unit width has gate capacitance sc_0 and output resistance r_0/s.

As technology develops, both channel length and gate oxide thickness are reduced by the same factor, consequently the gate capacitance per micron maintains a constant around $c_g = 1.75pF/um$ [39]. To determine the output

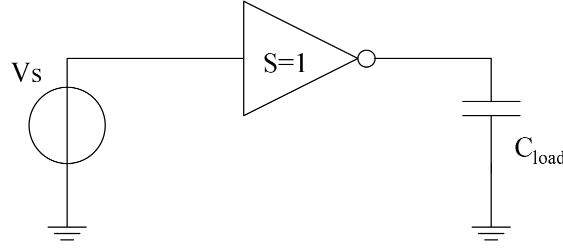

Figure II.2: Test circuit for measuring the transistor output resistance

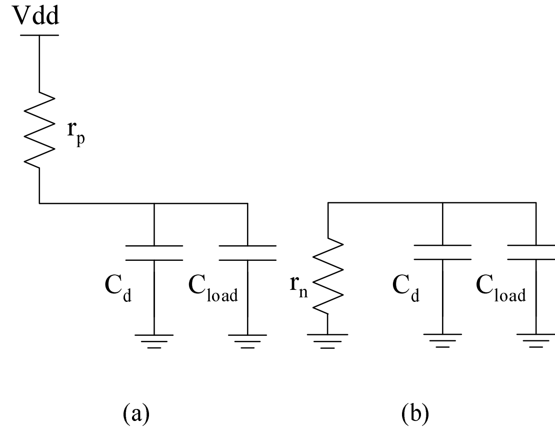

Figure II.3: RC model of the test circuit, (a) Rising delay, (b) Falling delay

resistance, one needs to simulate a transistor driving a known capacitance and measure the RC constant.

Fig.II.2 shows the test circuit used in our work for measuring the transistor output resistance. A minimum-sized inverter is connected to an ideal voltage source with digital pulse output (The period of the pulse waveform is adjusted to be long enough so that the inverter output is a near ideal pulse output). A load capacitance C_{load} is driven by the inverter. The equivalent circuit illustrating the RC model of the test circuit is given in FigII.3. When the output is high, PMOS transistor connects Vdd to the output. Otherwise, NMOS transistor connects the output to the ground. r_p is the PMOS output resistance, and r_n is the NMOS output resistance, c_d is the diffusion capacitance.

If we choose the value of load capacitance as C_{load} and $10C_{load}$, and we measure the rising/falling delay in both cases, we can have the following equations

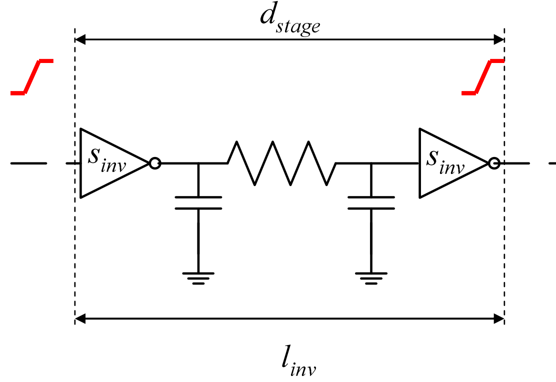

Figure II.4: Delay model of the repeated RC wire

based on Elmore delay model [20]:

$$delay_{rise1} = r_p(c_d + C_{load}) \quad \text{(II.6)}$$

$$delay_{rise2} = r_p(c_d + 10C_{load}) \quad \text{(II.7)}$$

$$delay_{fall1} = r_n(c_d + C_{load}) \quad \text{(II.8)}$$

$$delay_{fall2} = r_p(c_d + 10C_{load}) \quad \text{(II.9)}$$

By subtracting II.7 from II.8, and II.9 from II.9, the terms $r_p c_d$ and $r_n c_d$ can be eliminated. Since the value of C_{load} is known, r_p and r_n can be readily solved.

II.2 Delay modeling

In this section we consider the delay modeling of the repeated RC wire. We focus on uniform wires, which means the wire width and wire pitch are constant. We also assume that repeaters are inserted at equal intervals, and repeaters, including driver and receiver, are of the same size.

Fig.II.4 demonstrates two repeaters (with size s_{inv}) on the wire, and the π-model of the wire between the two repeaters. We denote the delay from input of the left repeater to the input of the right repeater d_{stage}, and the wire length of the segment l_{inv}.

Based on Elmore delay model [20],

$$d_{stage} = r_d(c_d + r_w c_w l_{inv}^2 + c_{gate}) + r_w l_{inv}(c_w l_{inv} + c_{gate}) \quad \text{(II.10)}$$

To make the above expression show the impact of repeater size and technology explicitly, we define several parameters. First we denote $w_0 = 2technode$ as the min-sized NMOS gate width, and $c_{nmos} = c_g w_0$ as the min-sized NMOS gate capacitance for a certain technology. Second, we assume that the P/N ratio of transistor width in the repeater is g, and the ratio of diffusion capacitance to gate capacitance is f. Thus,

$$c_d + c_{gate} = s_{inv}(f(1+g)c_{nmos} + (1+g)c_{nmos}) = s_{inv}(1+f)(1+g)c_{nmos} \quad \text{(II.11)}$$

and

$$r_d = \frac{r_0}{s_{inv}} \quad \text{(II.12)}$$

Therefore the d_{stage} can be rewritten as

$$d_{stage} = (1+g)(1+f)r_0 c_{nmos} + r_w c_w l_{inv}^2 + \frac{r_0 c_w l_{inv}}{s_{inv}} + (1+g) r_w c_{nmos} s_{inv} l_{inv} \quad \text{(II.13)}$$

However, [6] shows that this expression overestimate the delay, and two constants a and b related to the transistor switching model are needed for correction. If switchings occur at half of the voltage swing, $a = 0.4$, $b = 0.7$ and the stage delay is

$$d_{stage} = b(1+g)(1+f)r_0 c_{nmos} + a r_w c_w l_{inv}^2 + \frac{b r_0 c_w l_{inv}}{s_{inv}} + b(1+g) r_w c_{nmos} s_{inv} l_{inv} \quad \text{(II.14)}$$

(II.14) is also derived by [39] and [4].

In this work, we are more interested in the wire latency that normalized to wire length, which is the latency introduced by the wire configuration but not the total wire length. We define the normalized delay as

$$\begin{aligned} \boldsymbol{delay_n} &= \frac{d_{stage}}{l_{inv}} = \frac{b(1+g)(1+f)r_0 c_{nmos}}{l_{inv}} \\ &\quad + a r_w c_w l_{inv} + \frac{b r_0 c_w}{s_{inv}} + b(1+g) r_w c_{nmos} s_{inv} \end{aligned} \quad \text{(II.15)}$$

II.3 Power modeling

For the single wire stage shown in Fig.II.4, the power consumption includes the following components. First is the power consumed by the metal wire:

$$p_{wire} = c_w l_{inv} v_{dd}^2 \tag{II.16}$$

where v_{dd} is the supply voltage for a certain technology. Here the power refers the energy consumed on each bit transmitted by the wire. Second is the power consumed by the driver, which includes dynamic power, short circuit power and leakage power. dynamic power can be estimated by

$$p_{dyn} = (1 + f)(1 + g)c_{nmos} s_{inv} v_{dd}^2 \tag{II.17}$$

which is the energy needed to charge the transistor gate and diffusion capacitance. The work in [47] shows that the short circuit power is roughly 10% of the dynamic power regardless of technology scaling. The leakage current at 25°C is provided in [34], however as temperature goes up, the leakage current increases exponentially. To explore the importance of leakage effect, we use the temperature of 100°C to perform Hspice simulations. For 90nm technology, we measure the leakage current of a NMOS transistor with zero gate voltage, and supply voltage at drain, and we find that at 100°C, leakage current becomes 30 times of the value at 25°C in [34]. We assume this relation holds for all technologies we concern, and we define the leakage power factor as

$$\eta_{leak} = \frac{p_{leak}}{s_w p_{dyn}} = \frac{I_{leak}}{s_w (1 + f)(1 + g) c_{nmos} v_{dd} f_{clock}} \tag{II.18}$$

in which, s_w is the switching factor, I_{leak} is the leakage current, f_{clock} is the clock rate. We need the clock rate because leakage power is static power and the dynamic power is the energy consumed per bit. Note that when the P/N ratio and temperature is given, η_{leak} is only determined by technology.

Combining all the above components, the total power for a single stage is written as

$$p_{stage} = (c_w l_{inv} + (1.1 + \eta_{leak})(1 + f)(1 + g) c_{nmos} s_{inv}) v_{dd}^2 \tag{II.19}$$

Similarly with the delay modeling, we are more interested in the power that is normalized to wire length, which is defined by the following equation:

$$\boldsymbol{power_n} = \frac{p_{stage}}{l_{inv}} = (c_w + \frac{(1.1 + \eta_{leak})(1+f)(1+g)c_{nmos}s_{inv}}{l_{inv}})v_{dd}^2 \qquad \text{(II.20)}$$

II.4 Evaluation metrics

We have defined two metrics in the last two sections: normalized delay $\boldsymbol{delay_n}$ and normalized power $\boldsymbol{power_n}$. The normalized delay measures the wire latency per unit length, and the normalized power describes the energy consumption per bit per unit length of the wire. Another important metric is the communication bandwidth, which can be define as:

$$\boldsymbol{bandwidth} = \frac{1}{delay_n \times pitch} \qquad \text{(II.21)}$$

Bandwidth measures the speed and the capacity of wire communication. We further define

$$\boldsymbol{bandwidth/power} = \frac{1}{delay_n \times pitch \times power_n} \qquad \text{(II.22)}$$

which shows the communication efficiency in terms of power. Note that for a given pitch, with the definition of *bandwidth*, the maximization of *bandwidth* and *bandwidth/power* is equivalent to the minimization of the $delay_n$ and $delay_n \times power_n$.

II.5 Optimization of different design goals

II.5.A Definition of design goals

Different designs may have different goals, such as minimizing latency, maximizing bandwidth or minimizing the energy per bit. Interconnect design should conform the overall system design goal to achieve true optimization. To represent some of the typical design goals, we define the following three objective

functions: $\boldsymbol{delay_n}$, $\boldsymbol{delay_n \times power_n}$, $\boldsymbol{delay_n^2 \times power_n}$. We explore performance in the context of each objective function for a range of wire configurations, and note how the design goal influences the perception of the "best" configuration.

II.5.B Evaluation procedure

We define procedures of minimizing $delay_n$, $delay_n \times power_n$ and $delay_n^2 \times power_n$ as min-d, min-dp and min-ddp. Our evaluation process is as follows. For a given objective function and process technology, a range of wire pitch from minimum metal width to 1.2um is selected. We sweep the pitch in step of 10nm from the lower to upper bound. At each step, we find the optimal w, s_{inv} and l_{inv} by numerical search so that the given objective function is minimized. With this optimal wire configuration, metrics at that pitch value are evaluated.

II.5.C Analysis of min-d procedure

For minimizing $delay_n$, the optimal w, s_{inv} and l_{inv} have closed-form expressions [4] [44]. We include the analysis for completeness.

To minimize $delay_n$, we take its derivatives with respect to s_{inv} and l_{inv}, and let them equal zero:

$$\begin{aligned} \frac{\partial delay_n}{\partial s_{inv}} &= -\frac{br_0c_w}{s_{inv}^2} + b(1+g)r_wc_{nmos} = 0 \\ \frac{\partial delay_n}{\partial l_{inv}} &= -\frac{b(1+g)(1+f)r_0c_{nmos}}{l_{inv}^2} + ar_wc_w = 0 \end{aligned} \tag{II.23}$$

Solve these two equations to obtain the s_{inv} and l_{inv} that minimize the $delay_n$ (we label the solutions as s_{inv_mind} and l_{inv_mind}):

$$\begin{aligned} l_{inv_mind} &= \sqrt{\frac{b(1+g)(1+f)r_0c_{nmos}}{ar_wc_w}} \\ s_{inv_mind} &= \sqrt{\frac{r_0c_w}{(1+g)r_wc_{nmos}}} \end{aligned} \tag{II.24}$$

By plugging in (II.24) back to (II.15,II.20), the minimum delay and the corresponding power can be derived:

$$
\begin{aligned}
delay_{n_mind} &= 2(\sqrt{a(1+f)}+\sqrt{b})\sqrt{(1+g)br_0c_{nmos}r_wc_w} \\
power_{n_mind} &= (1+(1.1+\eta_{leak}\sqrt{\frac{a(1+f)}{b}}))c_wv_{dd}^2
\end{aligned} \tag{II.25}
$$

To derive the wire width w corresponding to minimum delay, we employ (II.25) and (II.5), take the derivative of $delay_{n_mind}$ with respect to w, and make it equal to zero. We then have

$$
w_{mind} = \frac{1}{2}pitch \tag{II.26}
$$

which is the default wire width used in most of on-chip wire designs. It is reasonable because the primary concern of most chip designs is to reduce the latency when power is not an issue. However, as technology scales system becomes more power hungery and power management is critical. When power consumption enters the objective function, the wire width is no longer half of the wire pitch, as we will see in the following sections.

II.6 Experiments

Based on the delay and power models discussed in SectionII.2 and II.3, we perform numerical experiments of the repeated RC wires under five technologies: 90nm, 65nm, 45nm, 32nm and 22nm with three different design goals defined in SectionII.5.A. Different performance metrics are also evaluated and discussed. Our evaluation process is as follows. For a given objective function and a process technology, a range of wire pitch from minimum metal width to 3.0 um is selected. This range exceeds the practical range used for global wires in all technologies. We sweep the pitch in step of 10nm from the lower to upper bounds. At each step, we find the optimal w, s_{inv} and l_{inv} by numerical search so that the given objective function is minimized. With this optimal wire configuration, metrics at that pitch value are evaluated.

Table II.1: Technology data for repeated RC wire experiments

year	2005	2007	2010	2013	2015
Technology node(nm)	90	65	45	32	22
Data from ITRS [34]					
Wiring pitch[1](nm)	300	210	135	96	75
Aspect ratio	2.2	2.3	2.4	2.5	2.6
Resistivity[2] (Ω-cm)	2.53	2.73	3.10	3.52	3.93
Voltage supply(volt)	1.1	1.0	1.0	0.9	0.9
Dielectric constant	3.1	2.9	2.6	2.4	2.1
Data from Hspice simulation					
r_0[3]($k\Omega$)	7.61	8.46	6.14	7.20	9.18
η_{leak}[4]	4.98%	11.68%	17.43%	15.30%	10.05%

[1] The wiring pitch is the minimum global wiring pitch.

[2] The conductor effective resistivity includes scattering effect and a conformal barrier

[3] r_0 is the output resistance of minimum size repeater

[4] (η_{leak} is the leakage power factor at 100°C.)

Section II.6.A summarizes technology data and implementations used in our experiments. The optimal wire configurations and corresponding metrics are shown and discussed in Section II.6.B and II.6.C respectively. We discuss the results from three perspectives: (1) spreading from 90nm to 22nm technology nodes, values at minimum pitches are compared, (2) values at the same technology node with a range of pitches are compared, and (3) values of 22nm technology are shown.

II.6.A Experimental setup

We list the technology related data in Table II.1. Row 4 to 8 are copied from ITRS report [34], and Row 10 and 11 are derived from Hspice simulation based on a predictive technology model [1].

We implement Matlab programs (Matlab 7.5) to find the optimal wire width, repeater size and repeater interval for given technology and objective func-

tion.

II.6.B Optimal wire configuration

The optimal wire widths, inverter sizes and inverter distances under different objective functions and technologies are shown in Fig.II.5 to Fig.II.7.

We have several observations regarding the optimized wire configurations.

Wire width:

At minimum pitch, the $w/pitch$ ratio is 0.5, 0.3 and 0.2 for min-d, min-ddp and min-dp respectively(Fig.II.5). The ratio of min-d matches our analysis in Section II.5.C. For min-ddp and min-dp, narrower wire is better because power is taken into consideration.

Inverter size:

(1) For the same technology node with a range of pitches, we can derive analytical expression for min-d procedure by using (II.5,II.1,II.24,II.26) and the assumption $h = t$. Noting that r_0 and c_{nmos} are constant under the same technology, the result is

$$s_{inv_mind} \propto \sqrt{r_0 c_w/(r_w c_{nmos})}\sqrt{t^2 + 0.25p^2} \qquad \text{(II.27)}$$

This explains why the inverter size increases linearly near the min-pitch range in Fig.II.6 (The same approach is used in other variables and metrics evaluations.)

(2) For min-ddp and min-dp procedures, comparing values for different technologies at the minimum pitch vs. values at the same technology node with a range of pitches, we can also observe similar trends but they are much less drastic.

(3) For 22nm technology node and at the min-pitch, the inverter size of min-ddp is 45% of that of min-d, and the inverter size of min-dp is 29% of that of min-d.

Inverter distance:

(1) For the same technology node with a range of pitches, inverter distance increases as pitch grows(Fig.II.7). The analytical expression can be derived from

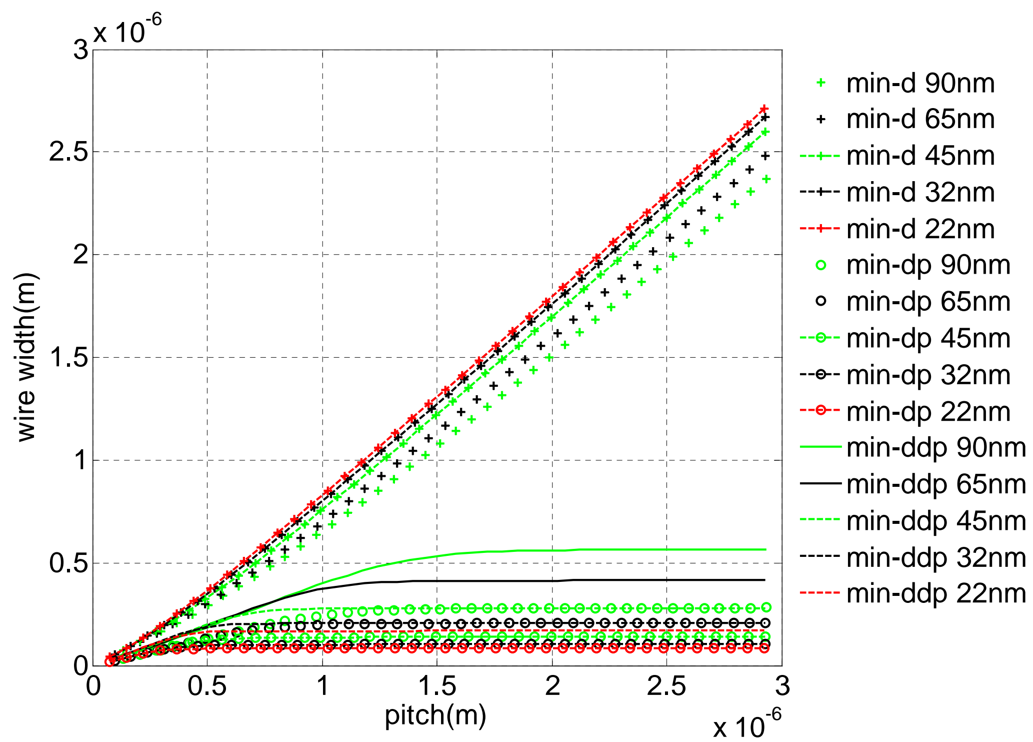

Figure II.5: Optimal wire widths

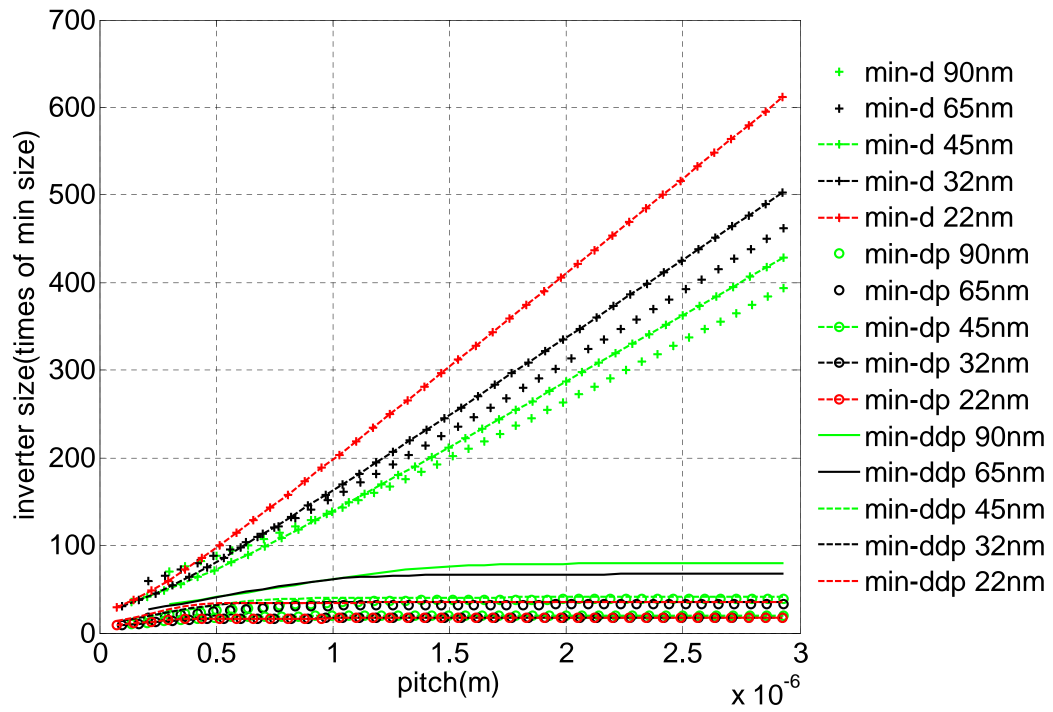

Figure II.6: Optimal repeater sizes

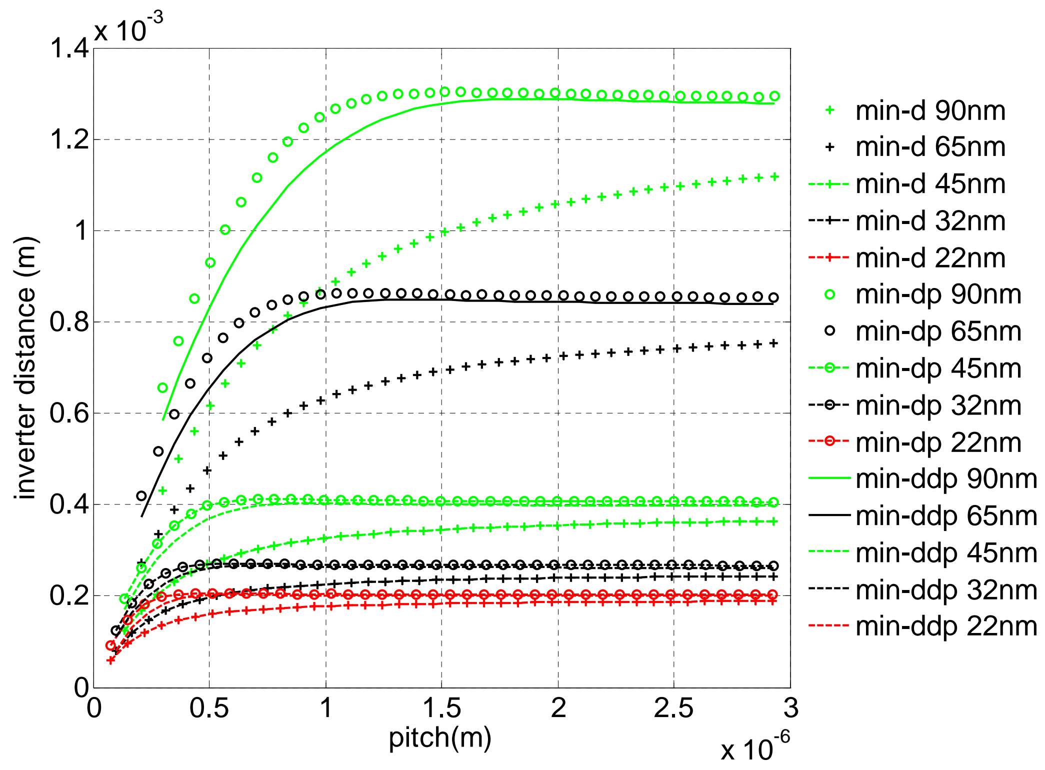

Figure II.7: Optimal repeater intervals

(II.5,II.1,II.24,II.26):

$$l_{inv_mind} \propto \sqrt{c_{nmos} r_0/(r_w c_w)} \propto \sqrt{1/(4/p^2 + 1/t^2)} \tag{II.28}$$

(2) For min-ddp and min-dp procedures, comparing values for different technologies at the minimum pitch vs. values at the same technology with a range of pitches, we can also observe similar trends.

(3) Generally, the inverter distance of min-dp and min-ddp are 110% to 140% of that of min-d.

Capacitance ratio c_{gate}/c_{wire}:

Once the wire width, repeater size and interval are determined, the capacitance ratio of gate to wire is also determined:

$$\frac{c_{gate}}{c_{wire}} = \frac{(1+f)(1+g)c_{nmos}s_{inv}}{c_w l_{inv}} \tag{II.29}$$

For min-d procedure, it is easy to find that

$$\frac{c_{gate_mind}}{c_{wire_mind}} = \sqrt{a(1+f)/b} = 1.07 \tag{II.30}$$

This result is verified in our experiment, and matches the result in [39]. This means the optimum wire configuration results in a particular c_{gate}/c_{wire} value, regardless of the wire pitch and technology. In other words, the most important thing for optimizing the RC repeated wire is to decide how to distribute the capacitance between gates and metal wires. For min-dp and min-ddp, the c_{gate}/c_{wire} value depends on technology but not on wire pitch, because the leakage power relates to technology. $c_{gate_minddp}/c_{wire_minddp}$ is 0.48∼0.50, and $c_{gate_mindp}/c_{wire_mindp}$ is 0.30∼0.32.

If we formulate the cost of repeater as s_{inv}/l_{inv}, which is how many minimal size repeaters need to be inserted per unit wire length, then we find that from technology 90 nm to 22 nm, the costs of repeater are $10^5\times$(16.28, 23.08, 29.17, 37.50, 50.00) respectively. Therefore, repeater insertion becomes more and more expensive as technology advances. Increasing pitch induces a linear increase in wire width, inverter size and inverter distance in min-d, but has much less effect on min-dp and min-ddp.

II.6.C Metric evaluation

In this section, we discuss the trends of delay, power, bandwidth, and bandwidth over power with respect to wire pitch and technology under different design goals.

Normalized delay:

(1) Spreading through 90 nm to 22 nm technology nodes at the min-pitch, the normalized delay increases as shown in Fig. II.8. At 90 nm technology, the min-pitch min-d $delay_n$ is 100 ps/mm, while at 22 nm technology, the min-pitch min-d $delay_n$ increases to 210 ps/mm, which is more than doubled. At the first glance, it may appear unreasonable that newer technology has larger delay. The reason is that the normalized delay does not consider the wire length scaling throughout different technologies. Local and intermediate wires scale with feature size but global wires don't, and in this scenario the normalized delay comparison makes more sense.

(2) For the same technology node with a range of pitches, the trend can be derived by adopting (II.5,II.1,II.25,II.26):

$$delay_{n_mind} \propto \sqrt{c_{nmos} r_w c_w} \propto \sqrt{\frac{1}{(4p^2)} + \frac{1}{t^2}} \qquad \text{(II.31)}$$

which makes $delay_n$ decrease (Fig.II.8). As pitch further increases, delay becomes insensitive to pitch. Such a change of trend leads to the definition of a saturating pitch: the pitch at which the decrease rate of delay becomes smaller than a threshold rate. Increasing pitch can not effectively reduce $delay_n$ when the pitch is larger than the saturating pitch. Here, we pick the threshold rate as $0.03s/m^2$ which means $delay_n$ decreases 30ps/mm when pitch increases 1 micron.

(3) At saturating pitch, the delay of min-dp is about 140% of that of min-d, and the delay of min-ddp is about 115% of that of min-d.

(4) Saturating pitch scales with technology.

(5) At the 22 nm technology node as shown in Fig. II.9, saturating pitch is 0.4∼0.5 um, and the delay of min-d is about 55 ps/mm, while the speed of light

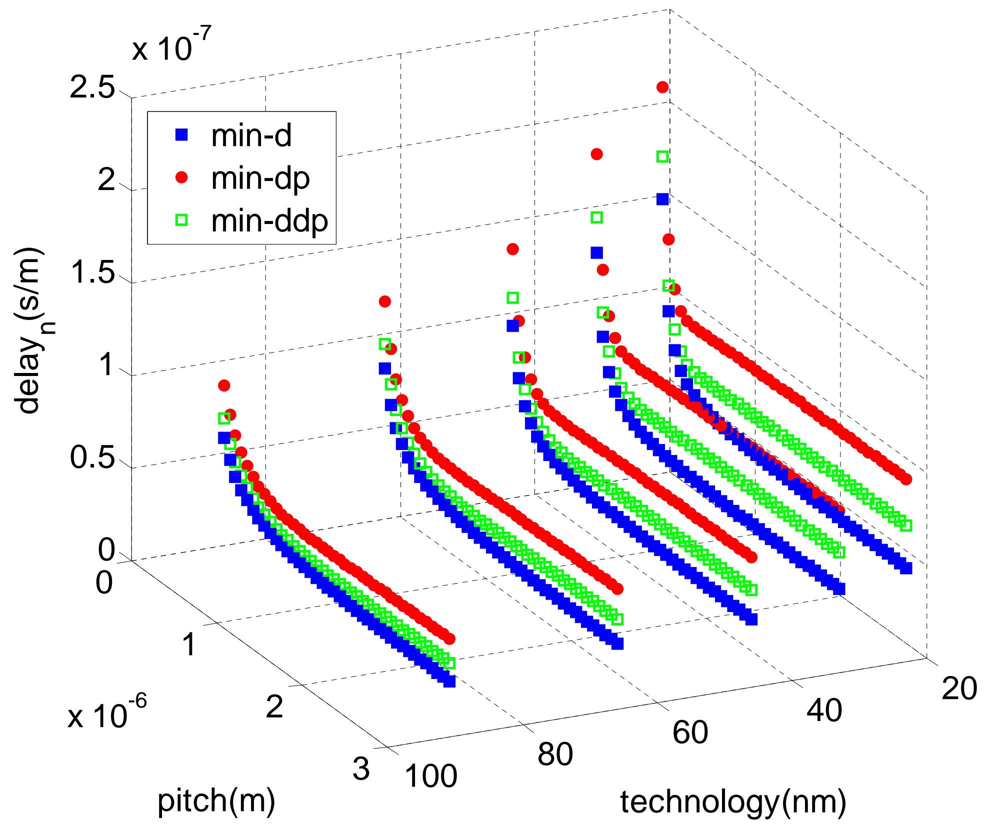

Figure II.8: Overview of normalized delay

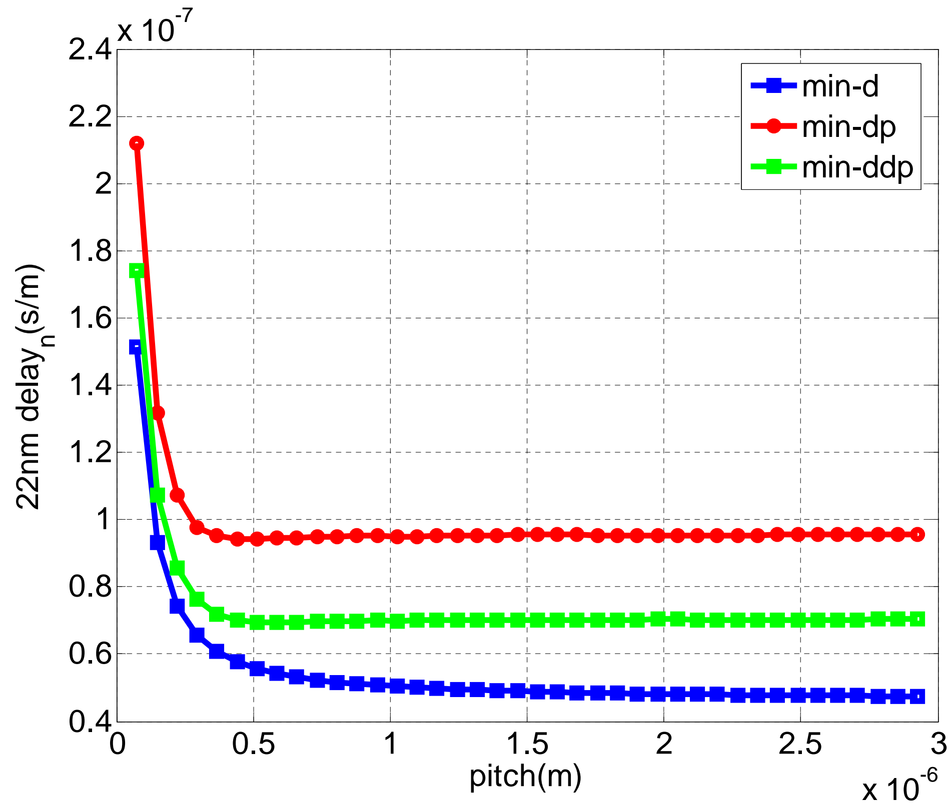

Figure II.9: Normalized delay at 22nm technology

is 6 ps/mm.

Normalized power:

(1) Spreading through 90 nm to 22 nm technology nodes at min-pitch, power decreases (Fig.II.10) due to lower supply voltage. As the voltage drops from 1.1V to 0.9 V, the min-pitch power also drops from 610 fJ/mm to 320 fJ/mm. Smaller technology can bring around 50% power reduction at min-pitch.

(2) For the same technology node with a range of pitches, optimal pitch for min-d power can be derived analytically using (II.5,II.1,II.20,II.26):

$$power_{n_mind} \propto \eta_{leak} c_w v_{dd}^2 \propto (\frac{2t}{p} + \frac{p}{2t}) \eta_{leak} v_{dd}^2 \qquad \text{(II.32)}$$

Power decreases since coupling capacitance c_c dominates ground capacitance c_s near min-pitch. At larger pitch area, with wire width increasing relatively faster, larger c_w enables wire to consume more power.

(3) For min-ddp and min-dp in the higher pitch range, the trend is almost constant (Fig.II.10). The reason is that neither wire capacitance nor inverter capacitance change much for these objective functions (Fig.II.5-II.7), which implies wire spacing is not quite effective for power saving.

(4) At optimal pitch, compared with min-d, min-ddp reduces power by 40%∼50%, and min-dp by around 60%. Further, the optimal pitch scales with technology. The power at minimum pitch is around 1.2x∼1.5x of that at optimal pitch.

(5) At the 22 nm technology node(Fig. II.11, the optimal pitch is around 0.15 um, and the power is about 0.25 pJ/mm for min-d, 0.1 pJ/mm for min-dp, and 0.12 pJ/mm for min-ddp at optimal pitch. At min-pitch, the power is about 0.31 pJ/mm, 0.12 pJ/mm, 0.15 pJ/mm for min-d, min-dp and min-ddp respectively.

Bandwidth:

(1) Spreading through 90 nm to 22 nm technology nodes at min-pitch, bandwidth increases as technology advances.

(2) For the same technology node with a range of pitches, the trend is clear: *bandwidth* almost inversely proportional to pitch because of the definition

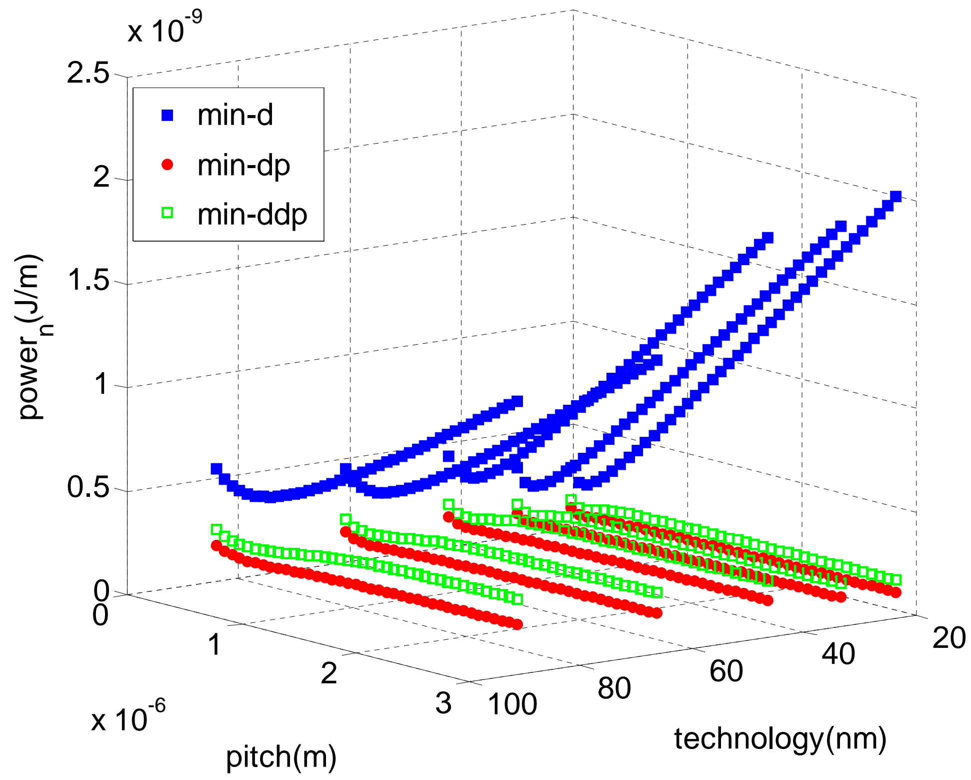

Figure II.10: Overview of normalized power

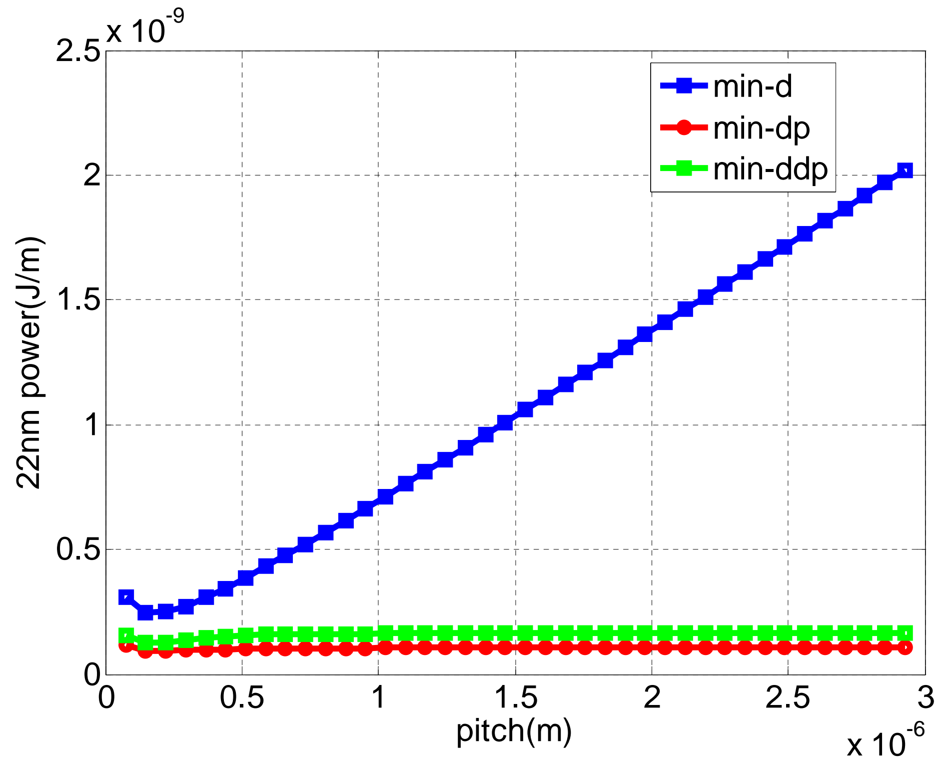

Figure II.11: Normalized power at 22nm technology

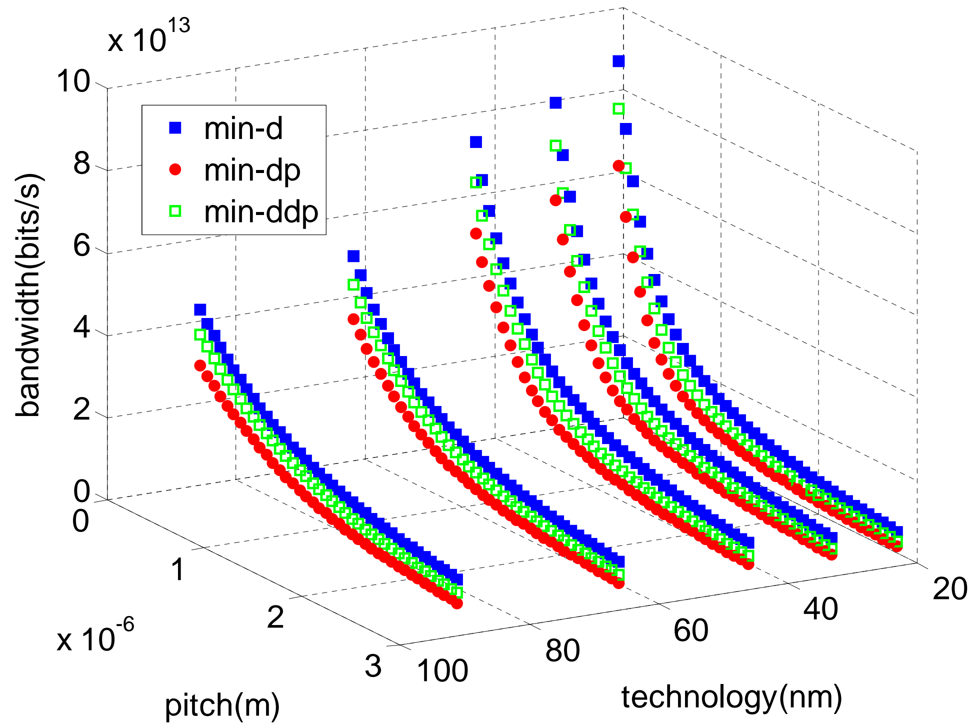

Figure II.12: Overview of bandwidth

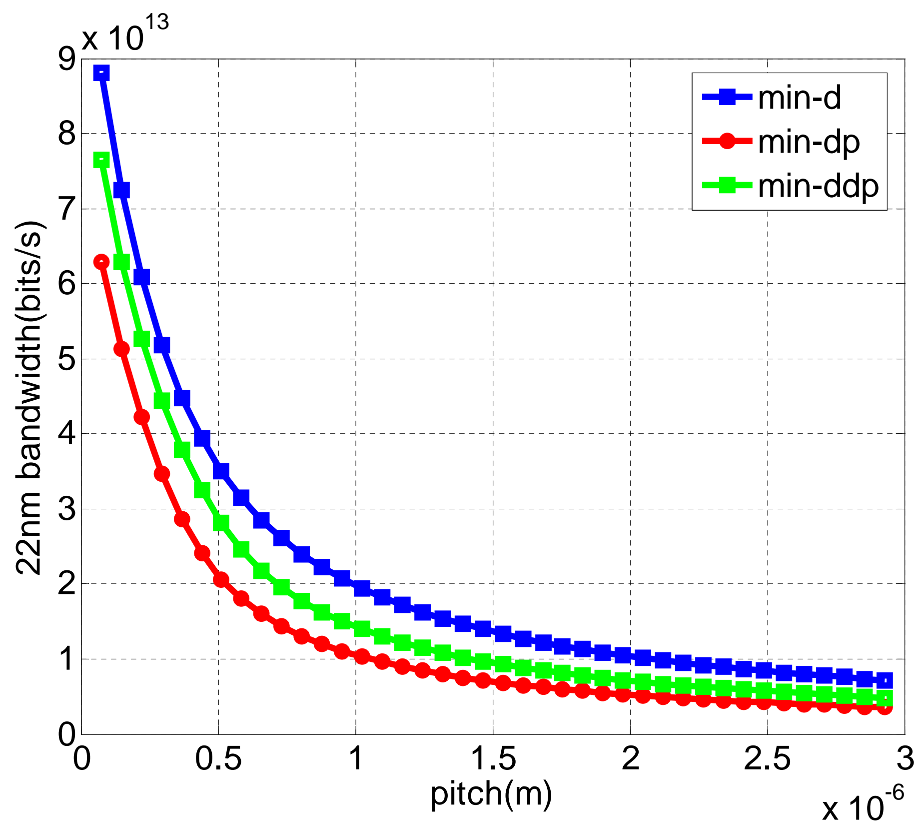

Figure II.13: Bandwidth at 22nm technology

of *bandwidth* is proportional to $1/pitch$.

(3) The min-d procedure results in the best *bandwidth* (Fig.II.12). The reduction of *bandwidth* for min-ddp is around 15%, and for min-dp is around 30%.

(4) Min-d enjoys the highest bandwidth of 90bits/ps at the minimum pitch for the 22 nm technology, as indicated in Fig. II.13.

Bandwidth over power:

(1) Spreading through 90 nm to 22 nm technology nodes at min-pitch, Fig. II.14 shows that the *bandwidth/power* increases significantly, and newer technology is more sensitive to the pitch variation.

(2) For the same technology node with a range of pitches, the trend can be inferred easily from the optimal pitch of $power_n$ and the decrease of *bandwidth*.

(3) Optimal pitch scales with technology, and min-dp has the greatest value for this metric (Fig.II.14).

(4) As shown in Fig. II.15, the *bandwidth/power* of min-dp at the optimal pitch(0.15 um) for 22 nm technology, is $540 bits \times mm/(pspJ)$, which is 67% larger than min-d, and is around 8% larger than min-ddp. At min-pitch, the min-dp's *bandwidth/power* is $530 bits \times mm/(pspJ)$, which is 83% larger than min-d and 8% larger than min-ddp. On average, *bandwidth/power* at optimal pitch is larger than that at min-pitch by around 1%~3%.

II.7 Summary

We studied the optimized wiring strategies for three objective functions, and evaluated their effects on four design metrics. Our observations are as follows:

(1) The repeater to wire capacitance ratio depends only on the objective function and technology, and remains constant when wire pitch changes.

(2) At min-pitch, the width pitch ratios of wire for different objective functions are different: the ratio is 0.5 for minimizing delay, 0.3 for minimizing delay^2-power product and 0.2 for minimizing delay-power product.

(3) Among the commonly used objective functions studied, min-ddp shows

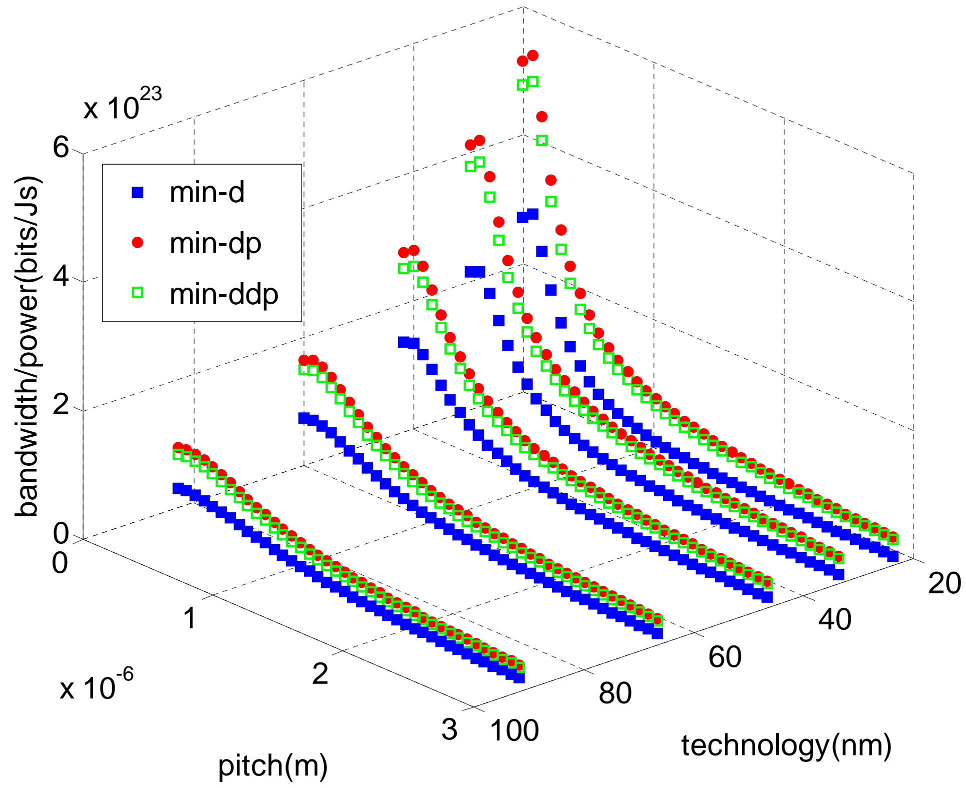

Figure II.14: Overview of bandwidth over power

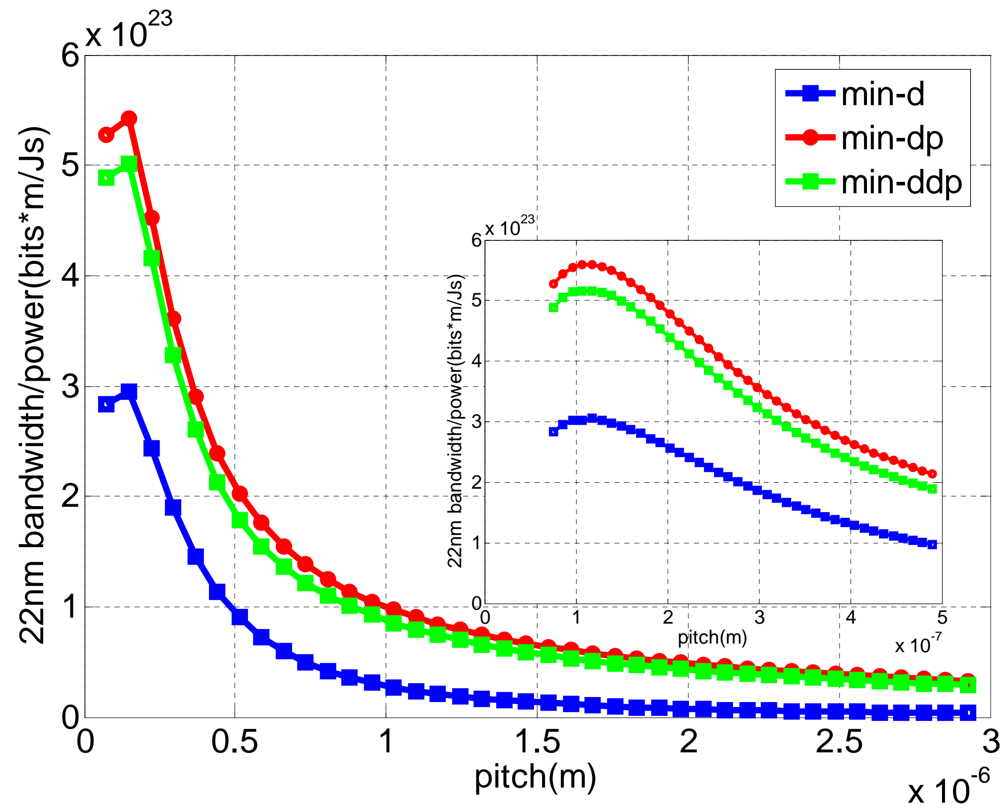

Figure II.15: Bandwidth over power at 22nm technology

a better trade-off between delay and power compared with min-d. It reduces $power_n$ by 50%, increases $bandwidth/power$ by 60%, while the cost is 15% increase in $delnay_n$ and 15% reduction in $bandwidth$. In contrast, min-dp reduces $power_n$ by 60% and increases $bandwidth/power$ by more than 70%, but the costs on $delay_n$ and $bandwidth$ are over 30%.

(4) Each metric has its own optimal pitch region, and the region scales down with technology. At 22 nm technology node, for $bandwidth$, the optimal pitch is at min-pitch, while for $power_n$ and $bandwidth/power$, it is around 2x min-pitch, and for $delay_n$, it is no more than 0.5 um.

Repeated RC wire is still used most widely in current chip design. Analysis and numerical evaluation in this work give favorable pitch values for different metrics and depict how different design goals choose different trade-offs between delay versus power: to choose different c_{gate}/c_{wire}. The delay^2-power product acquires much power saving with relative low cost in wire speed.

Chapter 2 includes the content of one published paper, “Repeated On-Chip Interconnect Analysis and Evaluation of Delay, Power, and Bandwidth Metrics under Different Design Goals”, by L. Zhang, H. Chen, B. Yao, K. Hamilton, C-K Cheng, in Proceedings of IEEE International Symposium on Quality Electronic Design in 2007. The dissertation author was the primary investigator and author of this paper.

III

On-Chip Transmission Line

We summarize the on-chip signaling scheme using transmission line we proposed in this chapter. First we give a brief introduction on basic transmission line theory, and then we review some existing on-chip transmission line works. Next we demonstrate our signaling scheme including the wires and the driver and receiver designs, and the optimization framework we developed. Finally we compare the on-chip transmission line with the repeater RC wires we discussed in the previous chapter.

III.1 Introduction

III.1.A Basic theory of transmission Line

We include the basic theory of transmission [51] for completeness of this chapter. The most fundamental equations are the telegrapher's equations of the transmission line. The homogenous lines are treated as cascaded infinitesimal RLGC segments, as shown in Fig. III.1. The R, L, G, C are per unit length electrical properties defined as follows:

- R = series resistance per unit length, in Ω/m.
- L = series self loop inductance per unit length, in H/m.

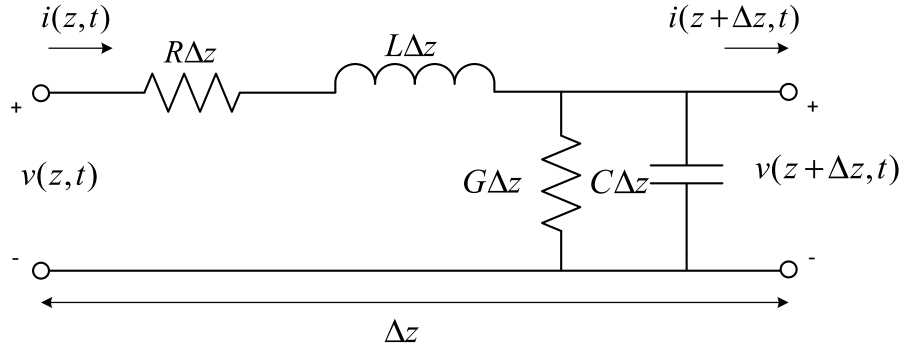

Figure III.1: RLGC model of a transmission line segment

- G = shunt conductance per unit length, in S/m.
- C = shunt capacitance per unit length, in F/m.

The voltage and current on the transmission line are waves traveling along the wire, and they are both functions of distance z and time t, and follow the telegrapher's equations:

$$\begin{aligned}\frac{\partial V(z,t)}{\partial z} &= -RI(z,t) - L\frac{\partial I(z,t)}{\partial t} \\ \frac{\partial I(z,t)}{\partial z} &= -GV(z,t) - C\frac{\partial I(z,t)}{\partial t}\end{aligned} \tag{III.1}$$

Assuming sinusoidal steady-state condition, by solving the above equations we can get the expressions of the incident wave that travels in the $z+$ direction:

$$V^{+}(z) = V_0^{+}e^{-\gamma z} = V_0^{+}e^{-\alpha z - j\beta z} \tag{III.2}$$

where

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{III.3}$$

is the complex propagation constant. From (III.2) we see that the amplitude of the traveling wave is $A(z) = V_0^{+}e^{-\alpha z}$. Thus α is called *attenuationconstant*, since 1 volt input will attenuate to $e^{-\alpha}$ volt after traveling one unit distance. Similarly β is called the *phaseconstant*, because βz gives the phase of the voltage wave at location z. The velocity of the traveling wave is

$$v = \frac{\omega}{\beta} \tag{III.4}$$

The **characteristic impedance** of the line is defined as the ratio of voltage to current on any point of the line:

$$Z_0 = \frac{V^+(z)}{I^+(z)} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{III.5}$$

The transmission line supports waves in both $z+$ and $z-$ directions. So the general solution to (III.1) is

$$V(z) = V^+(z) + V^-(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{III.6}$$

Typical on-chip global interconnects are very lossy. The series resistance of the global interconnects is usually at the order of $10\Omega/mm$. On the other hand, the silicon dioxide is a very good insulator, whose loss tangent is only 0.00068. Therefore, for on-chip transmission lines, the shunt conductance can be treated as zero. Under these conditions, on-chip transmission lines could operate in either RC region or LC region, depending on the frequency of interest.

RC Region:

When the frequency ω is low, we have $\omega L \ll R$ and $G \approx 0$. (III.3) simplifies to

$$\gamma = \alpha + j\beta = \sqrt{j\omega RC} = \sqrt{\frac{\omega RC}{2}} + j\sqrt{\frac{\omega RC}{2}} \tag{III.7}$$

Hence

$$\begin{aligned} \alpha &= \sqrt{\frac{\omega RC}{2}} \\ v &= \frac{\omega}{\beta} = \sqrt{\frac{2\omega}{RC}} \end{aligned} \tag{III.8}$$

We see that in RC region, both the attenuation constant and phase velocity are functions of the frequency. For on-chip interconnect, this $\omega L \ll R$ condition is usually satisfied up to 10GHz.

LC Region:

If the frequency keeps increasing such that $\omega L \gg R$, and $G \approx 0$, then (III.3) can be written as

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L) j\omega C} = \frac{R}{2\sqrt{L/C}} + j\omega\sqrt{LC} \tag{III.9}$$

Thus

$$\begin{aligned} \alpha &= \frac{R}{2\sqrt{L/C}} = \frac{R}{2Z_0} \\ v &= \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\epsilon_r}} \end{aligned} \tag{III.10}$$

where c_0 is the speed of light in free space and ϵ_r is the dielectric constant. We see that in LC region, if neglecting the variation of R and L, both attenuation and phase velocity are independent of frequency. This result provides the theoretic foundation for the work [12] and [38], which seek to modulate the low-frequency content to the LC region.

III.1.B Existing works

On-chip global signaling using transmission line has attracted intensive research focus in recent years. Comparing with repeated RC wires, transmission line delivers signals with speed of light in the medium. It also consumes much less power since the wave propagation eliminates the full swing charge and discharge on wire and gate capacitance. However the inter symbol interference (ISI) can be a barrier for performance, and various approaches have been proposed to deal with it.

Adding a resistive termination is an effective approach to reduce the ISI because by doing so, the DC voltage of the received signal is suppressed and the saturation time is greatly shortened. [23] and [63] derived the analytical formula for the optimal termination resistance. [13] and [68] proposed a surfliner scheme that intentionally inserting shunt resistors along the wire to minimize the distortion and therefore reduce the ISI. [40] adopted active equalization schemes to alleviate the ISI.

To have better understanding of on-chip transmission line performance, [31] predicted the bit-rate of different wire length for future technologies, and [30], [36] compared the performance of transmission line to RC wire.

III.2 Our signaling scheme using on-chip transmission line

In this section, we describe our on-chip transmission line signaling scheme (Fig. III.2(a)), which consists of a parallel RC equalizers, differential wires, termination resistance and transceivers. The transceivers compose of a sense amplifier and an inverter chain. We adopt parallel RC circuit at the driver side to compensate the attenuation in high frequency components given the fact that on-chip transmission line is very lossy. The RC circuit appears as a short circuit for high frequency components and boosts the high frequency response magnitude. For a given wire, the values of R_d, C_d and the termination resistance R_l determine the eye-opening and are optimized in our optimization flow (Section III.3.B). Two identical transceivers, which include a double-tail SA followed by a differential inverter chain as indicated in Fig. III.2(b), are used at both the driver and receiver sides to recover the signal back to full-swing.

III.2.A Wire modeling

Two parameters need to be considered in modeling the wires. One is the critical wire length distinguishing lumped-element region and distributive-element region [37]:

$$L_{critical} = \left| \frac{0.25}{\sqrt{(R + j\omega L)(j\omega C)}} \right| \tag{III.11}$$

When the wire length exceeds the critical length, the wire should be modeled as distributive element. The other parameter is the corner frequency f_{LC} distinguishing RC region and LC region, which is defined as:

$$f_{LC} = \frac{1}{2\pi} \frac{R_{DC}}{L} \tag{III.12}$$

where R_{DC} is the DC resistance of the wire. When the operating frequency is lower than the corner frequency, the wire works in RC region. Otherwise, it works in LC region.

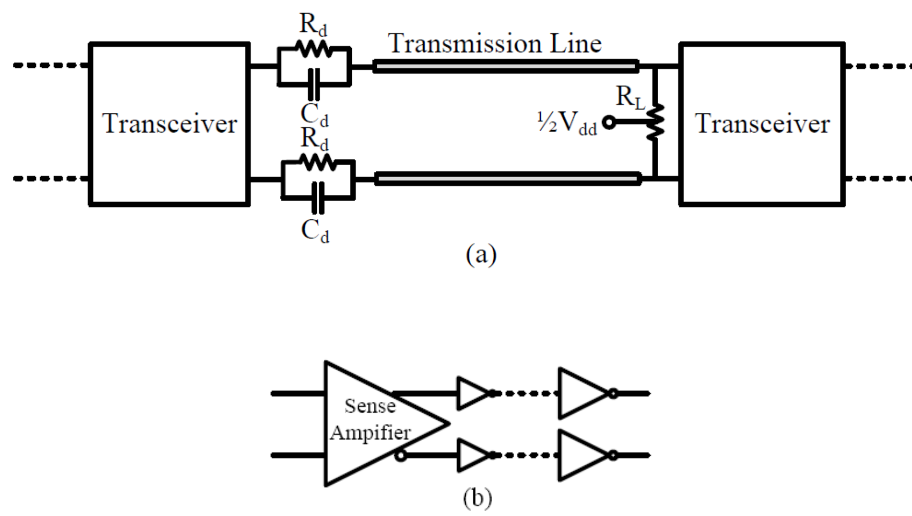

Figure III.2: The proposed signal scheme for global communication: (a) one stage structure; (b) transceiver structure

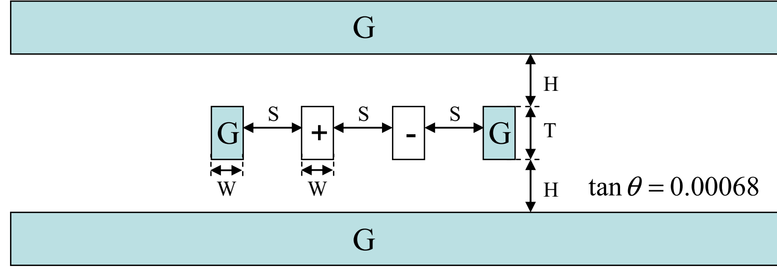

Figure III.3: The cross section of the differential stripline we use

We use the differential stripline as shown in Fig. III.3. We restrict the wire thickness T versus wire width W (i.e., the aspect ratio) to be 2 according to ITRS [34] report, and we define the vertical clearance $H = T$ for simplicity. We also assume that the ground wires has the same width as signal wires, and the spacing between ground and signal wires is identical to the spacing between the two signal wires. We choose 5mm wire length to represent typical on-chip global communication distance. The output of the wires connect to a sense amplifier, which samples the output voltage and amplify it. We want to make the wire dimension as small as possible so that the wiring density is maximized and sense amplifier still can sense the signals. Next we show how to derive the wire dimension.

As the aspect ratio is determined, the wire resistance is a function of wire thickness that

$$R = \frac{2\rho}{T^2} \tag{III.13}$$

We assume the sense amplifier has input threshold voltage V_{min}, and the input voltage level is 1V, then the attenuated voltage for a single wire can be no less than V_{min}:

$$e^{-\alpha l} \geq V_{min} \tag{III.14}$$

Since transmission lines are low-pass filters and the attenuation constant α increases as frequency grows up. If the wires operate between RC and LC region (We will verify that later), the attenuation constant should satisfy

$$\alpha \leq \frac{R}{2Z_0} = \frac{\rho}{T^2 Z_0} \tag{III.15}$$

according to (III.10). Plugging (III.15) into (III.14), we can have the lower bound of wire thickness that satisfies the signal sensing constraint:

$$T \geq T_{min} = \sqrt{\frac{2\rho l}{-Z_0 ln V_{min}}} \qquad \text{(III.16)}$$

To minimize the wire dimension, we choose $T = T_{min}$.

Table III.1: Design parameters

Design Parameters		Technology Node				
		$90nm$	$65nm$	$45nm$	$32nm$	$22nm$
ITRS	dielectric constant ϵ_r	3.1	2.9	2.6	2.4	2.1
	copper resistivity $\rho(\mu\Omega \cdot cm)$	2.53	2.73	3.10	3.52	3.93
	min. global wire pitch	300	210	135	96	75
	aspect Ratio	2.2	2.3	2.4	2.5	2.6
SA	r_0[1](kΩ)	7.61	8.46	6.14	7.20	9.18
	Cycle time T_c(ps)	150	90	50	30	20
	work frequency f_{op}^2(GHz)	6.7	11.1	20	33	50
	sensing threshold voltage $V_{min} = 25mV$					
Wire	$T_{min}(\mu m)$	0.90	0.94	1.00	1.08	1.14
	$L_{critical}^2(\mu m)$	179	186	196	205	219
	$f_{LC}^2(GHz)$	26.25	25.96	26.04	25.35	25.41
	W=0.5T,S=0.5T,T,1.5T,2T,H=T					

[1] The output resistance of minimum-sized CMOS inverter

[2] $f_{op} = 1/T_c$

[3] parameters are computed assuming that $S = 0.5T$.

We list the T_{min} with $V_{min} = 25mV$ for each technology in Row 7 of Table III.1. This table contains three types of design parameters, the data from ITRS [34] report (dielectric constant, resistivity of copper, minimum global wiring pitch and wire aspect ratio), the parameters we calculated (T_{min}, $L_{critical}$ and f_{LC}), and the data we obtained by performing circuit simulation (r_0, the cycle time of sense amplifier and the work frequency).

For each technology and a given wire thickness, larger spacing increases Z_0, reduces the attenuation and generates better eye. Therefore we vary S so that $S = 0.5T, T, 1.5T, 2T$ to observe the performance change. It can bee observed that f_{LC} keeps constant because when wire spacing is fixed to half of wire thickness, the wire inductance does not change much and the wire resistance is tuned to be very

similar by selecting the lower bound T. The operating frequency of the channel is determined by the cycle time of the sense amplifier, and comparing it to the corner frequency of the wire, we can see that the wire works at RC region at technologies of 90 nm to 45 nm and shifts into LC region for 32 nm and 22 nm. When wire spacing increases, the corner frequency decreases since L drops, which pushes the wire towards or into LC region further. At the same time, $L_{critical}$ is much smaller than the wire length (5mm), hence distributive element model is necessary.

The wire delay can be modeled as

$$D_{wire} = T_{flight} + T_c \tag{III.17}$$

The first term is the time-of-flight, which is the time of signal traveling from the wire input to the output. The second term is the cycle time of sense amplifier and that is the time from the signal arriving time to the signal sensing time.

For a given wire dimension and an operating frequency, the average total power of the wire with RC equalizer and R_l is a function of variables R_d, C_d, R_l and R_s. We model the relationship using the following polynomial function:

$$P_{wire} = \sum_{k=1}^{n} a_k R_s^i R_d^j C_d^p R_l^q, \quad \text{for all } i+j+p+q \leq N \tag{III.18}$$

The number of terms n is determined by the order N. We run circuit simulations to collect the power values for different variables combinations, and we use min-square-error curve fitting method to find the coefficients a_k. We found that when $N = 4$, the error is less than $\pm 6\%$ which is small enough for the optimization task.

III.2.B Driver and receiver design and modeling

The structure of transceiver is shown in Fig. III.2, which is a sense amplifier driving an inverter chain. We adopt a state-of-the-art sense amplifier structure called double-tail latch-type sense amplifier proposed by [54] in our design. This scheme achieves fast decisions by adopting strong positive feedback in the second stage and compared with other possible sense amplifier choices, this scheme could

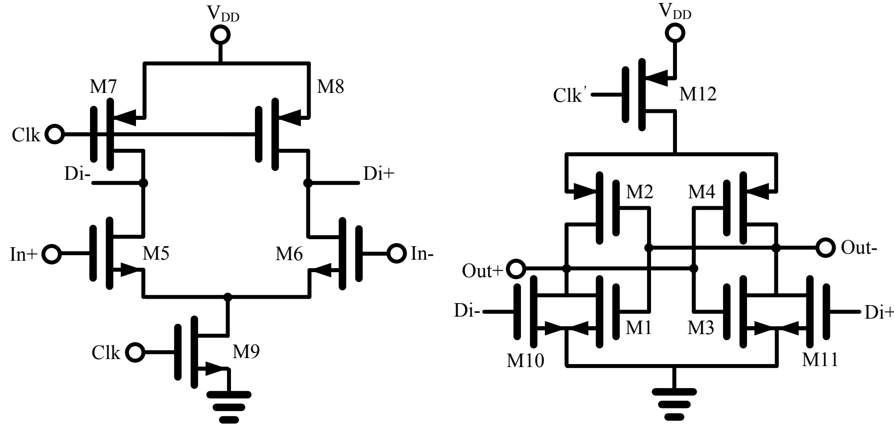

Figure III.4: Double-tail sense amplifier [54]

provide more flexibility for designer to balance the trade-offs of performance metrics, which is suitable for on-chip interconnect application. In our application, we tune the size of transistors in the double-tail scheme to minimize the sense amplifier delay for a given technology.

Sense amplifier with reasonable delay can only drive small capacitive load, while the output resistance of transceiver or driver can not be too large, normally in the range between $Z_0/2$ and Z_0. Thus, a number of cascaded inverters are needed to achieve the low output resistance. In our design, the number of inverters is fixed to 6 and the size ratio is constant:

$$\frac{s_2}{s_1} = \frac{s_3}{s_2} = ... = \frac{s_6}{s_5} \qquad \text{(III.19)}$$

Once the first and last stage size s_1, s_6 are determined, the size of every inverter can be derived. When only s_6 is known, which is the case for a single iteration of the optimization (Section III.3.B, we sweep s_1 so as to minimize the total latency of the transceiver.

Our simulation results show that, with $\Delta V_{in} = 50mV$ for the sense amplifier input voltage and transceiver output resistance$R_s = 50\Omega$, the minimum delay and power of transceiver are 87.08 ps and 0.52 mW at 90 nm, and as technology scales to 22 nm, the delay and power decrease to 5.61 ps and 0.04 mW. Whereas the power consumed on the wire is around 2 mW at 90 nm and doesn't scale with

technology when wire length is fixed. Therefore, the total power consumption is dominated by wire power, and when we optimize the transceiver, we can only minimize transceiver latency.

We model the transceiver using non-linear fitting method. Input parameters are the received signal swing ΔV_{in} and the transceiver output resistance R_s. We use the following two expressions for the transceiver delay and power fitting:

$$D_{TX}(\Delta V_{in}, R_s) = a_1 \Delta V_{in}{}^{a_2} + a_3 R_s{}^{a_4} + a_5 \quad \text{(III.20)}$$

$$P_{TX}(\Delta V_{in}, R_s) = \frac{b_1 + b_2 \Delta V_{in} + b_3 R_s}{1 + b_4 ln \Delta V_{in} + b_5 ln R_s} + b_6 \quad \text{(III.21)}$$

where $a_i(i \leq 5), b_i(\leq 6)$ are the fitting coefficients, which are determined based on delay and power data from circuit simulations. The fitting errors of delay and power are within $\pm 2\%$ and $\pm 5\%$, respectively, which are small enough for the optimization task.

III.2.C Evaluation metrics

Metrics definitions of on-chip transmission line

Similar to the case of studying repeated RC wire, we define the metrics of normalized delay, normalized power, delay power product and bandwidth to evaluate the on-chip transmission line performance from different perspectives. The normalized delay is

$$delay_n = \frac{D_{wire} + D_{TX}}{wirelength} \quad \text{(III.22)}$$

in which D_{wire} is defined by (III.17) and D_{TX} is defined by (III.20). In our experiments, the wire length is 5mm.

The normalized power is

$$power_n = \frac{Energy/bit}{wirelength} = \frac{P_{wire} + P_{TX}}{f_{op} \times wirelength} \quad \text{(III.23)}$$

The working frequency of transmission line is determined by the bandwidth of the transceiver, especially the sense amplifier, whereas the frequency of repeated

RC wire is determined by the latency since one bit is transmitted only after the previous bit reaches destination.

The bandwidth is defined as

$$bandwidth = \frac{f_{op}}{wirepitch} \quad \text{(III.24)}$$

which is the amount of data that can be transmitted for a given cross area in a given period.

Bandwidth definition of repeated RC wire

The definitions of the normalized delay and the normalized power of repeated RC wires in the evaluation of this study is the same as those defined by (II.15, II.20) in Chapter II. They have the same units as the delay and power of transmission line (III.22, III.23). The bandwidth definition of transmission line has the unit of $bit/(second * meter)$, which implicitly assumes the communication distance is 5 mm, and counts the number of bits being transmitted per unit wiring pitch. To be consistent with transmission line, we redefine the bandwidth of repeated RC wire as

$$bandwidth = \frac{1}{delay_n \times 5mm \times wirepitch} \quad \text{(III.25)}$$

III.3 Problem formulation and optimization framework

III.3.A Problem formulation

We formulate the optimization problem as a constrained non-linear programming problem, and adopt Sequential Quadratic Programming (SQP) method([8]) to solve it. The design goals include minimizing delay, minimizing delay-power product and minimizing delay^2-power product, which are referred as **min-d**, **min-dp** and **min-ddp** respectively. The optimization variables are R_s, R_d, C_d and R_l.

For a given technology node and a given wire dimension, the formulation can be written as:

$$min \quad f = f_0 + ae^{(V_0 - V_{eye})} \tag{III.26}$$

$$\begin{aligned} s.t. \quad & R^s_{min} \leq R_s \leq R^s_{max} \\ & 0 \leq R_d \leq R^d_{max} \\ & 0 \leq C_d \leq C_{max} \\ & 0 \leq R_l \leq R^l_{max} \end{aligned} \tag{III.27}$$

where f_0 is the design objects that we want to minimize, and it can be delay, delay-power product or delay^2-power product. a and V_0 are constants. We add the exponential term to handle the constraint on the eye opening at the far end of transmission line. When the eye opening V_{eye} is smaller than V_0, the exponential term dominates and forces the flow to find a larger V_{eye}, otherwise the f_0 term dominates and the design goal will be minimized. Each variable has the lower and upper bound constraints on its value. Considering the manufacture ability, $C_{max} = 15pF$. In our application, $R^s_{max} = 80\Omega$ is the upper bound of source resistance that the wire can be treated as transmission line and $R^s_{min} = 10\Omega$ is the lower bound to avoid super large inverter size. $R^d_{max} = R^l_{max} = 500\Omega$.

III.3.B Optimization framework

The overall optimization framework is shown in Fig. III.5. The inputs are technology node and wire dimensions. Based on these design parameters, we then build the wire model and transceiver stage model, respectively. For the wires, we employ the 2D field solver to generate RLGC tabular model, which is used in SPICE simulation. For the transceiver model, we do the optimization by sweeping the first inverter size s_1 and fit the simulation data into non-linear functions as mentioned in Section III.2.B.

In each iteration of optimization, we compute the wire delay and power using (III.17) and (III.18). We simulate the step response of T-Line for the given

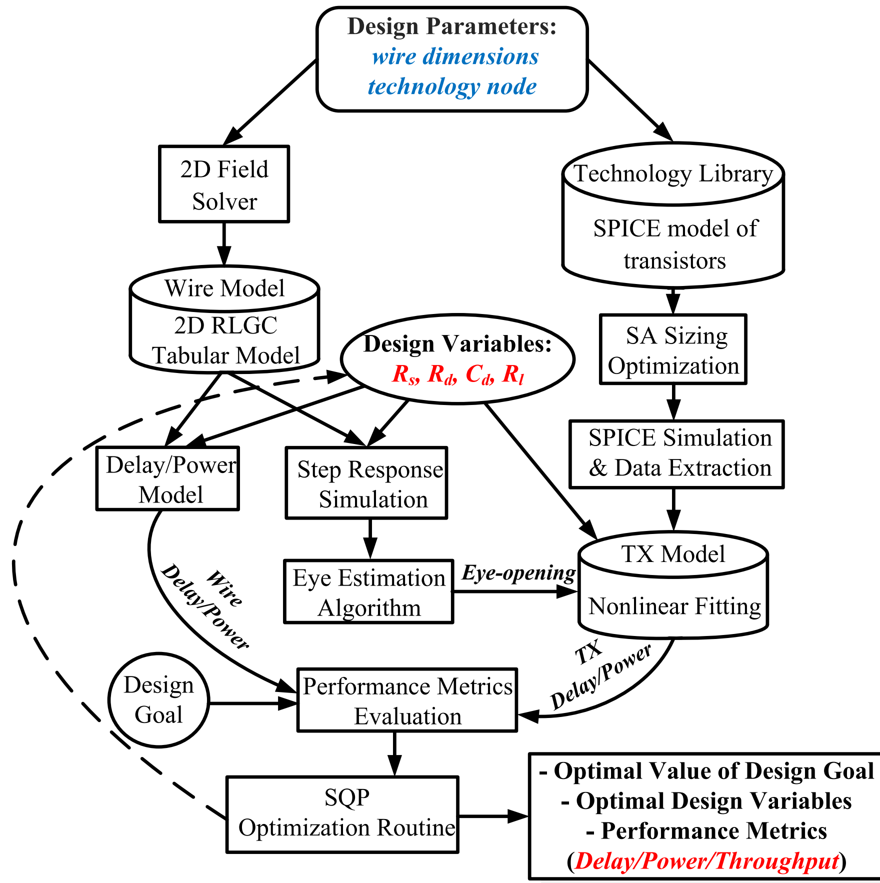

Figure III.5: The optimization framework

design variables, and then use [56] to estimate the eye opening, which is the input signal swing ΔV_{in} of the following transceiver stage. With the ΔV_{in} and R_s, delay and power of transceiver stage are derived according to (III.20) and (III.21). The cost function is evaluated based on different design goals by combining the delay and power of both wires and transceivers, and the SQP routine performs the optimization by evaluating the cost function. The flow outputs optimal values of design variables in terms of optimal design goal, and also provides the performance metrics, including delay/power/throughput at this optimal situation.

The relation between cost function and variables is complex and there is no closed-form solution. We use Sequential Quadratic Programming(SQP) to solve it, which is the state of the art nonlinear programming method, and has been implemented in Matlab. Based on the work of [8] [29] [49] [50], the method closely mimics Newton's method for constrained optimization. At each iteration, a quasi-Newton updating method is used to derive the approximated Hessian of the Lagrangian function, which is then used to generate a QP subproblem, whose solution is used to obtain a search direction for a line search procedure. The SQP method relies on gradient information and maybe sensitive to the starting point.

III.4 Experimental results

We optimize the proposed signaling scheme with the flow discussed in Section III.3.B under three different design goals: **min-d**, **min-dp** and **min-ddp**. For each design goal, we further study wires with 4 different spacings as shown in Table III.1. We also compare the performance scaling of on-chip transmission line to the repeated RC wires that are optimized in Chapter II for the three design goals.

Table III.2: The latency of transceiver (unit: ps)

Technology	90nm	65nm	45nm	32nm	22nm
min-d	76.38	50.59	23.45	14.70	5.14
min-dp	78.28	52.77	24.41	15.05	5.27
min-ddp	78.28	52.13	23.96	14.76	5.19
min-pitch	78.08	51.61	26.76	16.90	6.77

Table III.3: The power of transceiver (unit: uW)

Technology	90nm	65nm	45nm	32nm	22nm
min-d	383.6	237.4	142.2	65.7	32.4
min-dp	385.7	243.9	143.3	65.6	32.5
min-ddp	385.7	242.5	143.1	65.7	32.5
min-pitch	385.7	241.1	212.6	232.2	463.5

III.4.A Experimental setup

For repeated RC wire, the results obtained in Chapter II are adopted and verified with Hspice simulation using the predictive transistor model [1].

For transmission line, we use the 2D EM solver CZ2D in EIP tool suite from IBM [32] to extract the frequency dependent RLGC tabular model for the wires using the dielectric constant ϵ_r, the resistivity ρ_{Cu}, and the wire dimensions listed in Table III.1. Due to the accuracy limitation of HSPICE, PowerSPICE [33] is used to generate step response and to measure the power for transmission lines. Linear regression method in Matlab is used to obtain the power model.

The predictive transistor model [1] is also used to simulate the transceiver delay and power with HSPICE. Nonlinear regression method in Matlab is adopted to generate the delay and power model for the transceiver.

III.4.B Comparison of the transmission line and the repeated RC wires

The latency, energy per bit and the throughput comparisons of the two signal schemes under three design goals are given in Fig. III.6 through Fig. III.8.

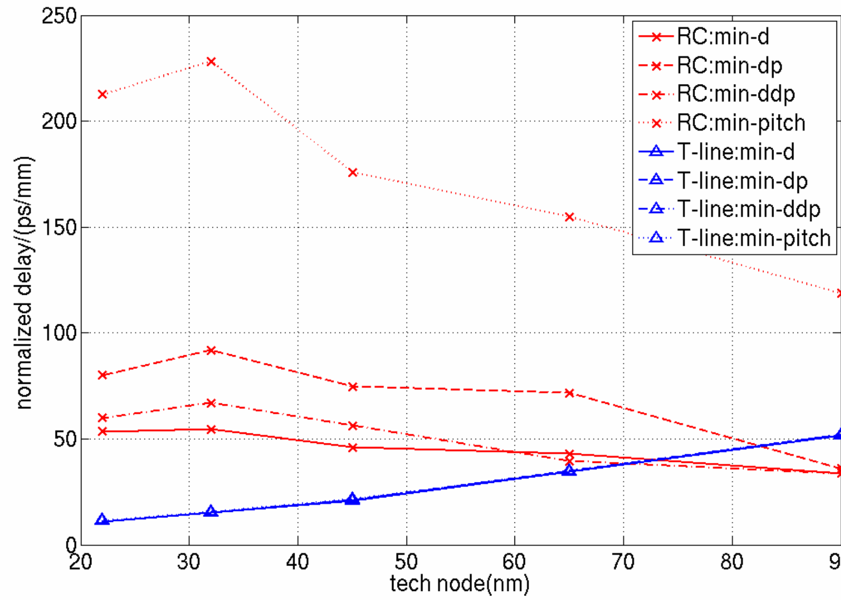

Figure III.6: Normalized delay comparison between repeated RC wire and the proposed on-chip T-line

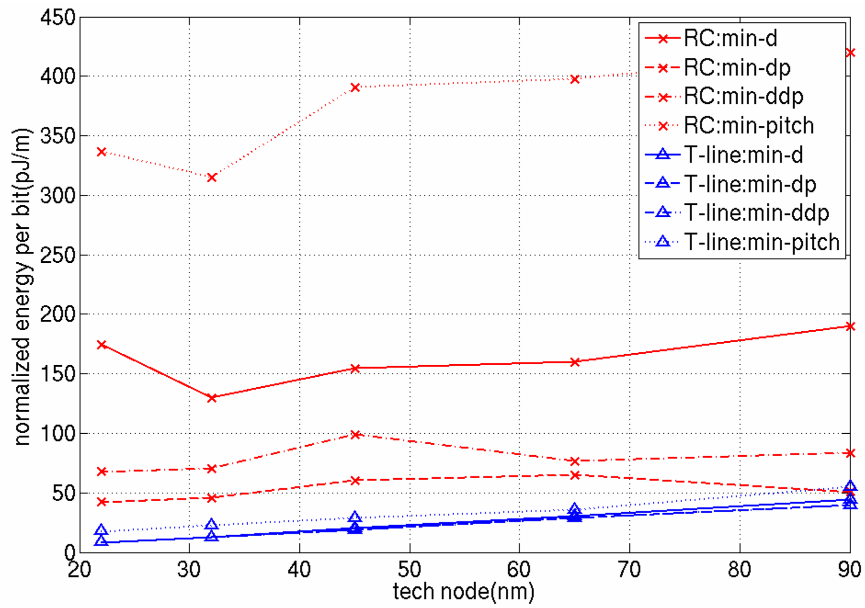

Figure III.7: Normalized energy per bit comparison between repeated RC wire and the proposed on-chip T-line

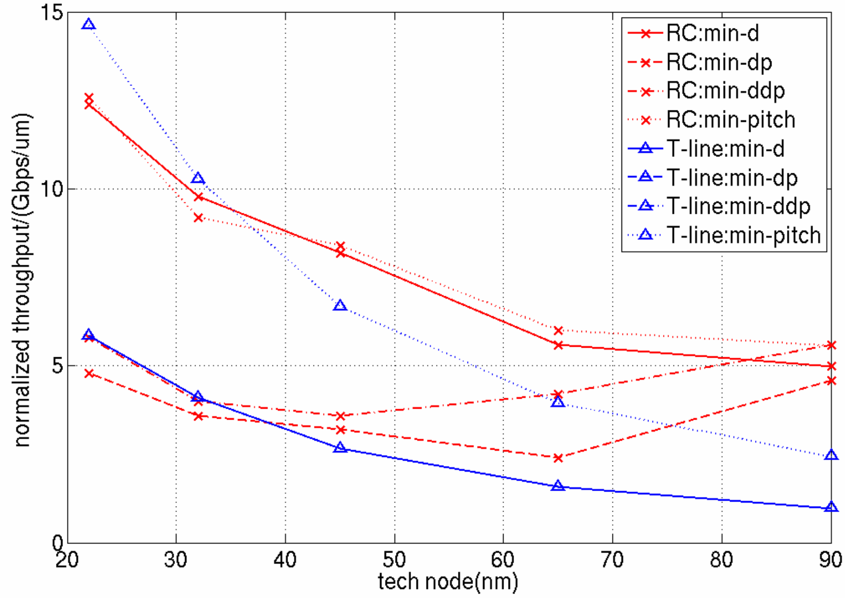

Figure III.8: Normalized throughput comparison between repeated RC wire and the proposed on-chip T-line

Table. III.2 and III.3 show the transceiver delay and power. Besides the three design goals, we also show the performance of min-d at minimum pitch, which is labeled as **min-pitch**.

Latency comparison

From Fig. III.6, we can see that design goal has very little impact on T-Line latencies, while the latency of repeated RC wire is strongly correlated with design goals. For T-Line, as technology scales, the normalized latency shrinks accordingly, but for RC wire, the normalized latency rises up more or less as technology advances.

For T-Line, the latency has three components: time of flight T_{flight}(only depends on technology since the wire length is fixed to 5mm), cycle time T_c and transceiver latency. As technology advances, T_{flight} reduces slowly as dielectric constant gets smaller. T_c is only determined by the bandwidth of SA since we use the same SA sizing for a given technology. T_c decreases as a result of faster SA

switching speed when technology scales. The transceiver latency varies with design goal, because different designs may find different optimal R_s, which determines the last inverter size in the inverter chain, and therefore affects the sizing of the whole inverter chain. Generally speaking, we found in our experiments that the variations of transceiver latency (Table. III.2) are insignificant comparing with total latency. For example, at 90 nm technology, the time of flight for the 5 mm wire is around 30 ps, and the cycle time is 150 ps. For different design goals, transceiver latency ranges from 70 ps to 80 ps, which makes total latency varies from 250 ps to 260 ps. The corresponding $delay_n$ changes from 50 ps/mm to 52 ps/mm. We can also observe from Table. III.2 that as technology scales, transceiver latency improves as a result of faster device switching. For these three reasons, the latency of T-Line shows decreasing trend with technology.

Very different from T-Line, the latency of repeated RC wire (Fig. III.6)is strongly affected by design goals, and as technology shrinks, latency increases. When the design goal is min-d, pitches that are much larger than min-pitch are selected and therefore the wire resistance and coupling capacitance can be reduced significantly, and the latency can drop to lower than 50 ps/mm for 90 nm and 65 nm technologies. At 90 nm technology, the minimum pitch of wire is 300 nm while the min-d optimization select 1.2 μm pitch, the width and spacing increase around 4 times. At minimum pitch, the wire resistance and coupling capacitance are high due to small wiring width and higher A/R, which result very large latency (above 200 ps/mm for 32 nm and 22 nm technologies). As technology advances, wire pitch decreases and A/R grows, consequently wire becomes much more resistive and more heavily coupled, which results larger latency.

Comparing RC wire and T-Line in terms of latency under three design goals, T-Line has larger latency only at 90 nm (roughly 50 ps/mm versus 35 ps/mm, which is 1.5X). The newer the technology, the more advantageous the T-Line in terms of normalized latency.

Power consumption comparison

As shown in Fig. III.7, the energy per bit of T-Line is much lower than RC wire, and it decreases as technology advances, since the energy per bit is inverse proportional to the working frequency (III.23), and the frequency f_{op} increases as technology shrinks (Table. III.1). The power consumption of transceiver is insignificant compared to the power consumed on the metal wires and resistors (R_{load} and R_d). For example, at 90 nm technology, the transceiver consumes around 400 uW power, while the total power dissipation is 1.5 mW to 1.8 mW according to different design goals. Table. III.3 also demonstrates that the transceiver power is decreasing with technology scaling as well. Fig. III.7 tells us that design goals only have a minor effect on the T-Line power consumption: min-pitch dissipates slightly higher power than other design goals.

As apposed to T-Line, the energy per bit of RC wire is strongly coupled with design goals and the value is much higher than T-Line. For example, under the min-dp design goal, the energy per bit of RC wire varies from twice (90 nm) to 4.3X (22 nm) of T-Line, and for 90 nm technology, the energy per bit ranges from more than 400 pJ/m for min-pitch to around 50 pJ/m for min-dp.

Throughput comparison

From Fig. III.8, we can observe the trend of the normalized throughput of T-Line and RC wire. At 90 nm technology, RC-wire has higher throughput than T-Line, while at 22 nm, T-Line with min-pitch enjoys the highest throughput of around 15 Gbps/μm, RC wires with min-pitch and min-d have throughput of 12-13 Gbps/μm. With other design goals, the throughput of T-Line and RC wire are similar, which is around 5-6 Gbps/μm.

According to the definition of (III.24), the normalized throughput of T-Line relies on the cycle time (which is the reciprocal of operating frequency) and the wire pitch, which is $3W + 3S$ according to the differential wire structure illustrated in Fig. III.3. As discussed above, T_c is determined by technology regardless of the

design goal, therefore, for the same design goal, the normalized throughput only depends on the wire pitch.

As we will show in Section III.4.B, the wires with the largest spacing $S = 2T$ give all the optimal design goals, which result that the three design goals have the same throughput for a given technology (Fig. III.8, and the min-pitch has higher throughput since $S = 0.5T$ in this case. According to Table. III.1, the wire thickness is slightly increasing, since the the resistivity of copper rises as technology scales and we want to keep the wire resistance constant. This trend makes the T-Line pitch grows from 90nm to 22nm, which has negative effect on the throughput. On the other hand, the cycle time T_c shrinks drastically, and therefore improves the throughput by 6X from 90 nm to 22 nm (Fig. III.8).

Comparing with T-Line, min-d and min-pitch RC wire always have higher throughput than min-dp and min-ddp design goals. This is because without signal pipelining, the throughput of RC wire relies on the latency rather than operating frequency. Under the design goals of min-dp and min-ddp, the throughput of RC wires decreases slightly from 90nm to 45nm technology. The reason is to minimize power dissipation, these two design goals prefer to use smaller repeaters with larger intervals, and to reduce the coupling capacitance, to use wires with wider pitch and narrower width, which result larger delay. Before 45 nm technology, RC wire with min-dp and min-ddp have substantial advantage comparing to T-Line with min-d, min-dp and min-ddp. After 45 nm technology, their throughputs are very close, and at 22 nm, the throughput of T-Line is even slightly higher than RC wire, which tells us that as technology scales, T-Line becomes more appealing in terms of maximizing throughput.

Performance comparison of different wire spacing

Fig. III.9 through Fig. III.12 show the effect of wire spacing upon different design goals and throughput at 45 nm technology. For the normalized delay, normalized delay power product and delay^2 power product, the optimal values are

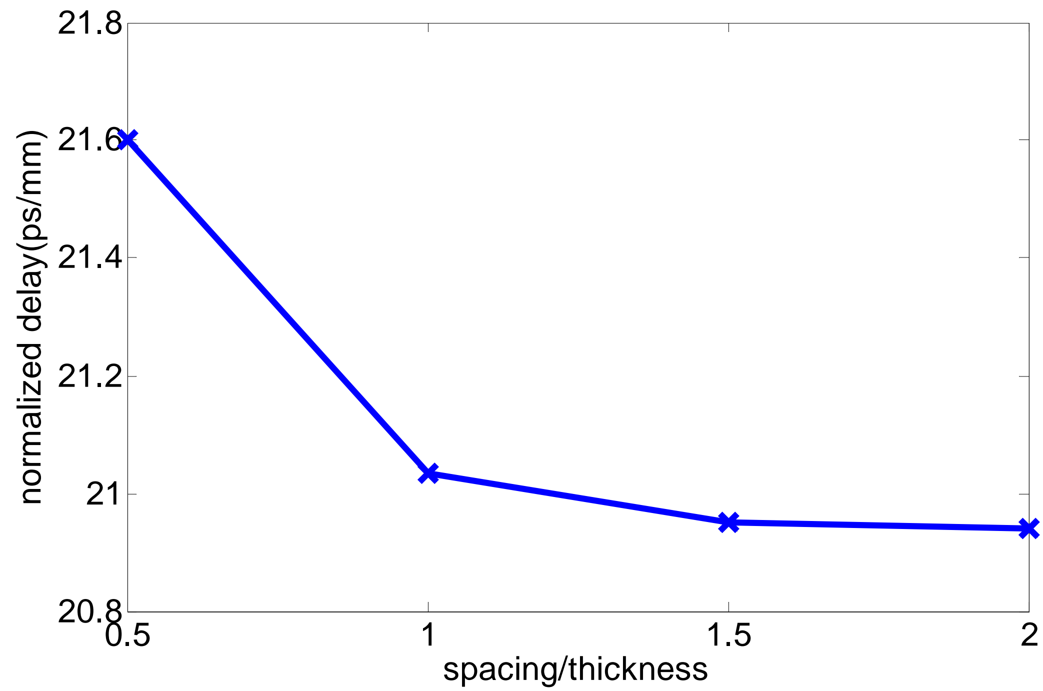

Figure III.9: $delay_n$ of different wire spacing for min-d at 45nm technology

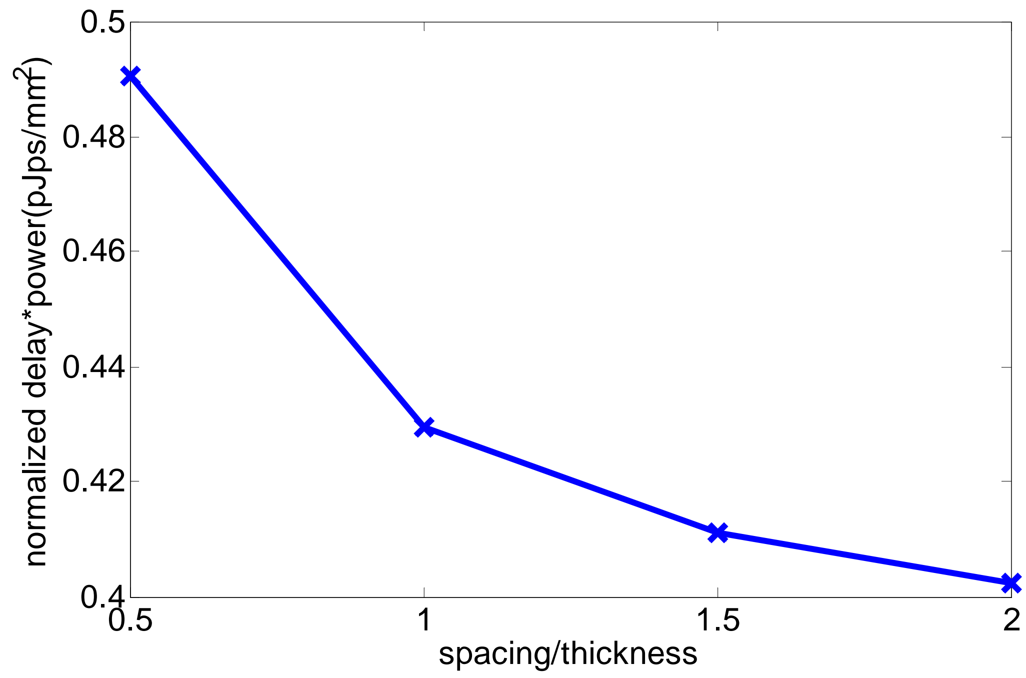

Figure III.10: $delay_n * power_n$ of different wire spacing for min-dp at 45nm technology

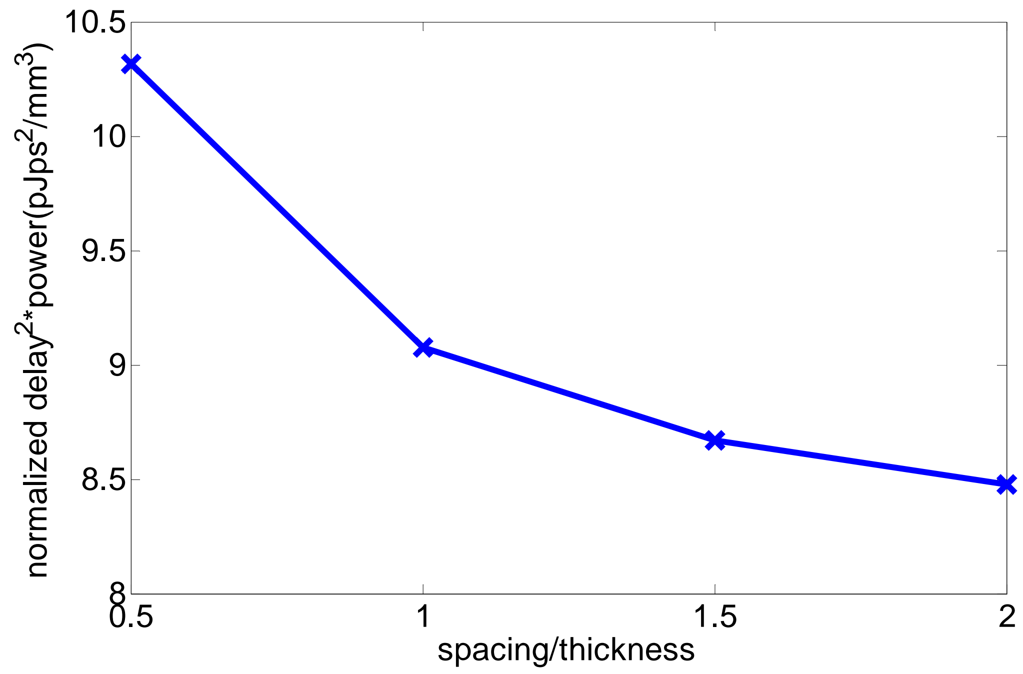

Figure III.11: $delay_n^2 * power_n$ of different wire spacing for min-ddp at 45nm technology

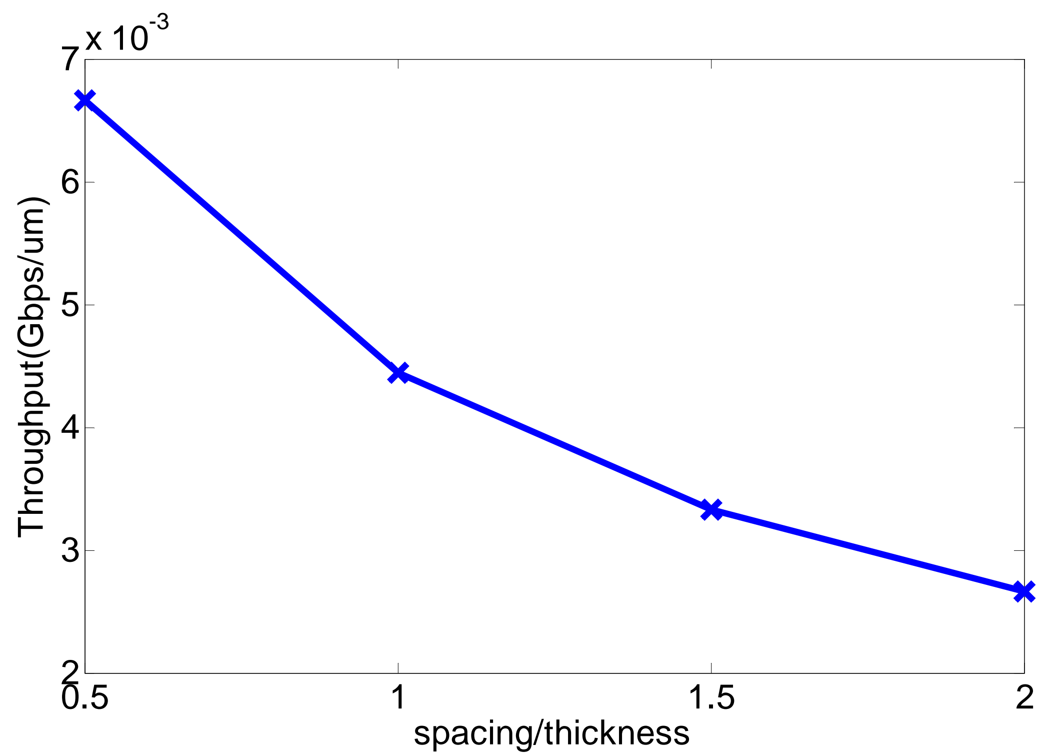

Figure III.12: Throughput of different wire spacing at 45nm technology

achieved when $S = 2T$. The reason is because larger spacing gives higher Z_0, which reduces the attenuation along the wire. Consequently, to satisfy the given eye opening constraint in our optimization flow, larger R_s is used since higher voltage drop on source can be tolerated. Larger R_s results in lower transceiver delay because it reduces the fan out of inverter chain, and it also gives lower power consumption on both transceiver and wires at the same time. Thus, wires with large spacing have optimal design goals. However, large spacing reduces the throughput, as illustrated in Fig. III.12, and there are trade-offs between different design goals and the desired throughput.

III.5 Summary

In this chapter, we propose a high performance on-chip global signaling with passive compensation. We use a parallel RC circuit at driver side to compensate the attenuation in high frequency components. We use a double-tail sense amplifier(SA) followed by an inverter chain as transceivers. We use Sequential Quadratic Programming (SQP) method([8]) to optimize the proposed signaling scheme under different design goals accross five technologies and we compare our scheme with the repeated RC wire in terms of latency, power and bandwidth. Our experimental results show that at the technology node 22 nm, proposed signaling scheme could reduce the normalized delay 80%-95%, the normalized energy consumption by 50%-94% comparing with repeated RC wires. The highest throughput is improved by 20%. At 22 nm, the normalized latency is 10 ps/mm, the energy per bit is 20 pJ/m, and the throughput is around 15 Gbps/μm.

Our contributions include: 1) an on-chip global signaling scheme with passive compensation, 2) an optimization flow based on Sequential Quadratic Programming (SQP) method that optimizes the scheme for a given technology and wire dimension, 3) comparison between the proposed on-chip T-Line scheme and repeated RC wire under the design goal of minimum delay, minimum delay power product and minimum delay^2 power product at different technologies.

Chapter 3 includes the content of one published paper, "High Performance On-Chip Differential Signaling Using Passive Compensation for Global Communication", by L. Zhang, Y. Zhang, A. Tsuchiya, M. Hashimoto, C-K Cheng, in Proceedings of IEEE Asian and South Pacific Design Automation Conference in 2009. The dissertation author was the primary investigator and author of this paper.

IV

Off-Chip Transmission Line

We describe the off-chip signalling scheme with equalization we investigated in this chapter. The basic transmission line theory was included in Chapter III and omitted in this chapter. We begin from introducing the basic idea of passive equalization, and then review existing works. Next we show the equalization topologies we adopt in our work, and analyze and compare their frequency responses and reflections. Thirdly discuss the problem formulation and the optimization framework we use to optimize the equalization schemes. Afterward, we introduce the CPU-memory links in IBM POWER6 system, which we used as test case, and finally we show the experimental results.

IV.1 Introduction

The power and performance of packaging level interconnects have become crucial for optimized system performance. While multi-core architectures increase the on-chip computing processing capability, inter-chip communication bandwidth must expand to accommodate this processing demand. Meanwhile, minimizing signaling power is becoming an ever greater challenge since many conventional approaches that improve performance increase the system power consumption, therefore, a low power signaling scheme is necessary.

An important approach to combating inter-symbol interference(ISI) is

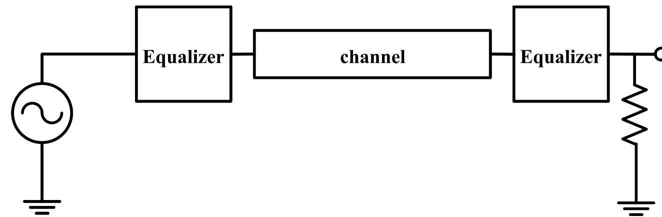

Figure IV.1: A channel with equalizers at the driver and the receiver

equalization. Equalization can be active or passive. Active equalization can achieve high bit rate but faces great challenges of increasing power consumption and latency, as mentioned in I.2.C. Passive equalization has much lower power overhead but uses significant chip or board area. In this chapter, we focus on passive equalization technique.

Passive equalizers can be used at the driver or receiver sides of the channel, as shown in Fig. IV.1. The equalizers may connect to ground or not. Generally, the channel acts as a low pass filter(the black line in Fig. IV.2), and therefore, high

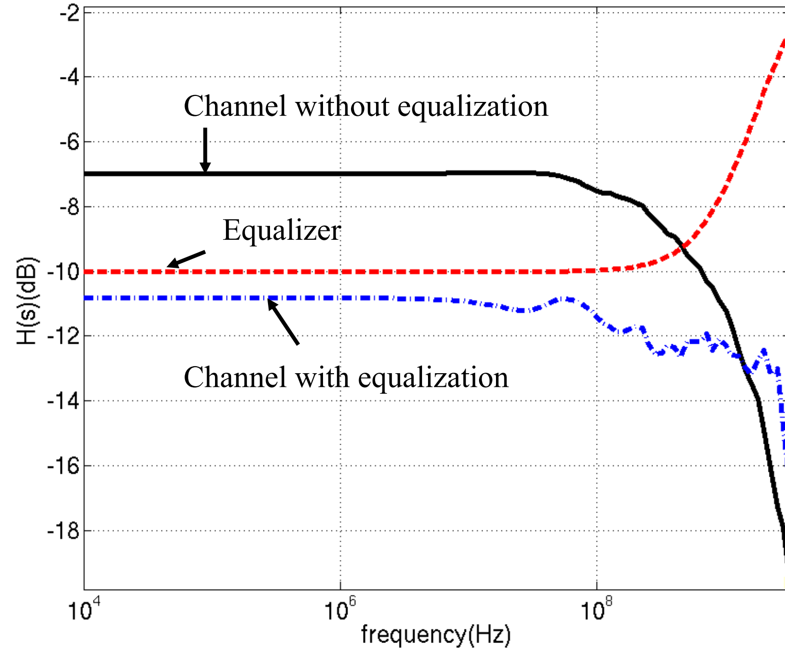

Figure IV.2: The frequency response of the equalizer, the channel w/ and w/o equalization

frequency components have larger attenuation then low frequencies. To compensate the high frequency loss, high pass filter (band pass filter in practice) can be inserted before or after the channel to boost up the high frequencies, as the red line in Fig. IV.2 indicated. The frequency response after equalization (the blue line) has much higher bandwidth comparing to the one without equalization. Consequently, the channel performance is greatly enhanced with passive equalization technique.

In 1920's, the concept of equalization was introduced in [3], [9]. In [41], a

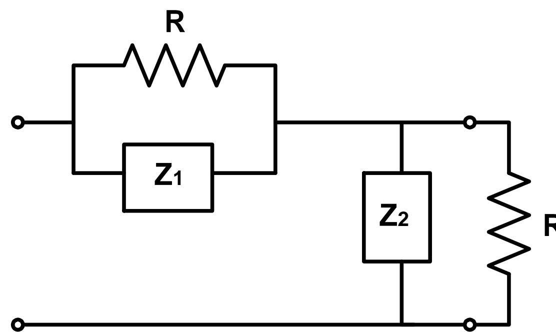

Figure IV.3: Constant-R ladder: input impedance is R when $z_1 z_2 = R^2$

constant-R ladder network (Fig. IV.3) was described, which behaved as an equalizer. The ladder satisfies the condition $z_1 z_2 = R^2$. When it is terminated with resistance R, its input impedance is R as well, therefore, multiple ladders can be cascaded.

In 2005, an adaptive passive equalizer based on a RLC T-junction network was introduced and had better power efficiency than active equalizers [61]. Shin et al. from Intel proposed three passive equalizers in [57] for the driver side. The equalization schemes include T-junction and parallel R-C, and have demonstrated that 90 mV eye opening at 10 GHz is feasible for a 19-inch long differential pair with 1.2 V supply voltage on actual measured hardware. [28] uses passive equalization to eliminate the ringings in mismatched termination condition. Because there are high frequencies in the ringings, equalizers with low pass filter property are adopted. Guo et al. analyzed the equalization schemes using inductor and high-impedance line at the receiver side in [27]. They optimized and implemented the schemes for an ideal PCB trace with length of 38 inches, where the eye opening ranged from 170 mV to 190 mV with 0.8 V supply voltage and 5 Gbps data rate.

IV.2 Equalization topologies and schemes

IV.2.A Equalization topologies

There are three basic topologies we used in this work: T-junction, R-C and R-L, as shown in Fig. IV.4. To preserve the constant R property, the RLCG components in T-junction satisfy:

$$\frac{R}{G} = Z_0^2, \frac{L}{C} = Z_0^2 \tag{IV.1}$$

We don't use the Ladder structure in our work because Ladder is equivalent to T-junction in terms of transfer function at both driver and receiver side, but consumes more power than T-junction when used at driver side. Our analysis

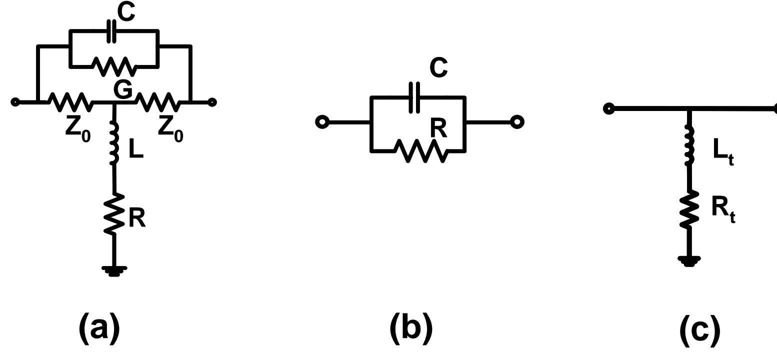

Figure IV.4: equalization components: (a) T-junction (b) R-C (c) R-L

shows that the power ratio of Ladder and T-junction when used at driver side can be written as:

$$\frac{POWER_{Ladder}}{POWER_{T-junction}} = \frac{2(1+r)Z_0 + (1+r)R_w}{2(1+r/2)Z_0 + R_w} \tag{IV.2}$$

where Z_0 is the characteristic impedance, R_w is the wire DC resistance, and r is defined as:

$$r = \frac{R_d(Z_0R_d + R_dR_w + R_wZ_0)}{Z_0^2(R_d + Z_0(Z_0 + R_w)/(2Z_0 + R_w))} \tag{IV.3}$$

in which R_d is the resistor in parallel with capacitor in T-junction, and in parallel with Z_1 in Ladder (we assume T-junction and Ladder have the same R_d for equivalence analysis). Given the fact that $r > 0$, the ratio in (IV.2) is always greater than 1.

IV.2.B equalization schemes

The three types of lumped elements can be used at both sides of the channel, and the T-junction can be implemented on-chip and off-chip because of matching. We summarize and label the usages of the components in Table IV.1. Column 3 shows the source resistance when the topology is used at driver side, while Column 4 gives the load resistance when the topology is inserted at receiver. For RL, the R_S is not available because RL is never used at driver side, and the R_{load} is infinity because RL serves as load itself and no extra load is needed. For RC, the source output resistance is considered so we use a 10 Ω resistor to represent

Table IV.1: Usages of topologies

Label	Topology	R_s at driver side	R_{load} at receiver side
M	match (no equalizer)	Z_0	Z_0
S	RL	NA	Infinity
P	RC	10Ω	R_L
T_m^c	On-chip T-junction	Z_0	Z_0
T_m^p	Off-chip T-junction	Z_0	Z_0
T_u^c	On-chip T-junction	10Ω	R_L
T_u^p	off-chip T-junction	10Ω	R_L

it, and the load resistance is a value to be determined. For on-chip and off-chip T-junction, we explore both the matched (labeled as T_m^c and T_m^p) and mismatched cases (labeled as T_u^c and T_u^p). In the matched case, both R_s and R_{load} are Z_0 while for mismatched, the condition is the same as RC. The matched structure without any equalizer is given label M for reference simplicity.

Given these seven basic topologies, there are many different schemes combining different components at driver and receiver side. We group the schemes according to the matching conditions at both sides, as shown in Table IV.2. For example, schemes in Group 1 have matched driver and receiver. It incudes $M+M$ (match at driver + match at receiver), $M+T_m^c$ (match at driver + on-chip T-junction at receiver), $M+T_m^p$ (match at driver + off-chip T-junction at receiver), T_m^c+M, $T_m^c+T_m^c$, $T_m^c+T_m^p$, T_m^p+M, $T_m^p+T_m^c$, $T_m^p+T_m^p$. The total number of schemes in Group 1 is nine. Following the same combination rule, the number of schemes in Group 2, 3 and 4 are nine, twelve and twelve.

Matching conditions determine the groups since the matching conditions have a predominant effect on the eye-diagram. With matched driver or receiver, there will be at most a slight reflection when the signal is propagating and therefore, the jitter is small. With mismatched driver or receiver, there exist reflections affecting the height of the eye.

Table IV.2: Groups of schemes according to the matching conditions

Group	topologies at driver side	topologies at receiver side
G1	matched: M, T_m^c, T_m^p	matched: M, T_m^c, T_m^p
G2	un-matched: P, T_u^p, T_u^c	matched: M, T_m^c, T_m^p
G3	matched: M, T_m^c, T_m^p	un-matched: P, T_u^p, T_u^c, S
G4	un-matched: P, T_u^p, T_u^c	un-matched: P, T_u^p, T_u^c, S

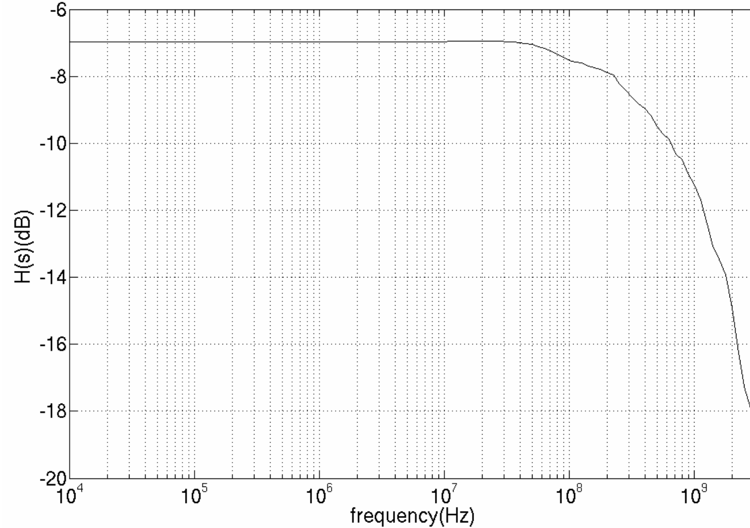

Figure IV.5: Transfer function of the channel

IV.3 Analysis and comparison of the equalization topologies

In this section, we briefly analyze and compare the topologies that are adopted in these schemes. The basic transmission line theory is included in Chapter III, and the s-parameter and output voltage are derived for each topology. Fig. IV.5 demonstrates the transfer function of the channel when no equalizer is used. The 3dB bandwidth is 0.65GHz. In the following analysis, we assume that at the driver, the equalizer input connects to a Z_g and the output is terminated with Z_0, as shown in Fig. IV.6(a), and at the receiver, the equalizer input connects to a Z_0 and the output is terminated with a Z_L, as shown in Fig. IV.6(b).

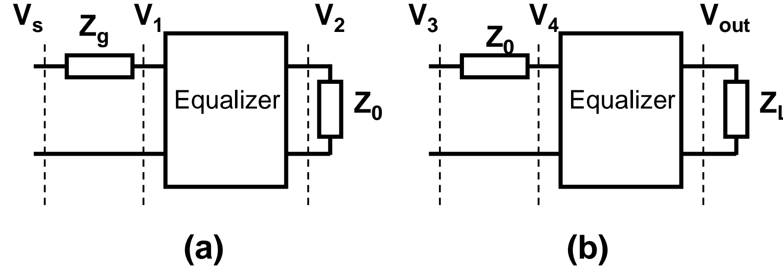

Figure IV.6: block diagrams of equalizer at (a)driver, (b)receiver

IV.3.A RL structure

The S matrix of RL can be written as:

$$S_{RL} = \begin{bmatrix} \Gamma_0 & 1+\Gamma_0 \\ 1+\Gamma_0 & \Gamma_0 \end{bmatrix} \tag{IV.4}$$

where

$$\Gamma_0 = \frac{\frac{Z_{RL}+Z_0}{Z_{RL}Z_0} - Z_0}{\frac{Z_{RL}+Z_0}{Z_{RL}Z_0} + Z_0} \tag{IV.5}$$

and $Z_{RL} = R + sL$ is the impedance of serial RL circuit. RL circuit is used only at receiver end and there is no extra load connected, therefore, the reflection coefficient coming from output of RL circuit is 1. Hence, the input impedance looking from input to RL circuit is

$$Z_{in}^{RL} = Z_{RL}, \tag{IV.6}$$

and the output voltage is

$$V_{out} = \frac{Z_{RL}}{Z_{RL} + Z_0} V_3. \tag{IV.7}$$

Fig. IV.7 shows the transfer function of RL in red dash line (assume the RL is connected to a voltage source with $Z_g = Z_0$), the transfer function of the channel without and with using RL in black line and dash dot blue line, respectively. The RL structure is a high pass filter, therefore, the 3dB bandwidth of channel output increases to 2.65 GHz after equalization.

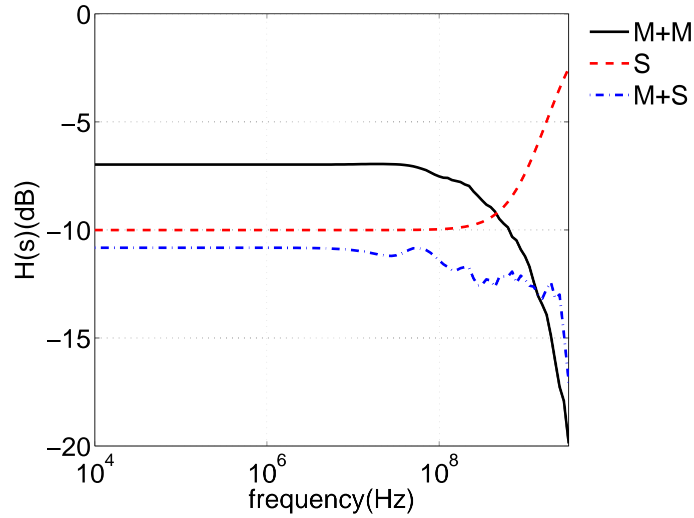

Figure IV.7: Transfer functions of RL, channel w/ and w/o using RL

IV.3.B RC structure

The S matrix of RC can be written as:

$$S_{RC} = \begin{bmatrix} \Gamma_0 & (1+\Gamma_0)\frac{Z_0}{Z_{RC}+Z_0} \\ (1+\Gamma_0)\frac{Z_0}{Z_{RC}+Z_0} & \Gamma_0 \end{bmatrix} \quad \text{(IV.8)}$$

where $\Gamma_0 = \frac{Z_{RC}}{Z_{RC}+2Z_0}$ is the input reflection coefficient looking into RC when the output of RC is terminated with Z_0, and $Z_{RC} = \frac{R}{sRC+1}$.

RC at receiver side

In this case, the load reflection is

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \quad \text{(IV.9)}$$

and the input reflection is

$$\Gamma_{in}^{RC} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = 1 - \frac{2Z_0(1-\Gamma_L)}{2Z_0 + (1-\Gamma_L)Z_{RC}}, \quad \text{(IV.10)}$$

The input impedance can be written as

$$Z_{in}^{RC} = Z_{RC} + Z_L = Z_0\frac{1+\Gamma_L}{1-\Gamma_L} + Z_{RC} \quad \text{(IV.11)}$$

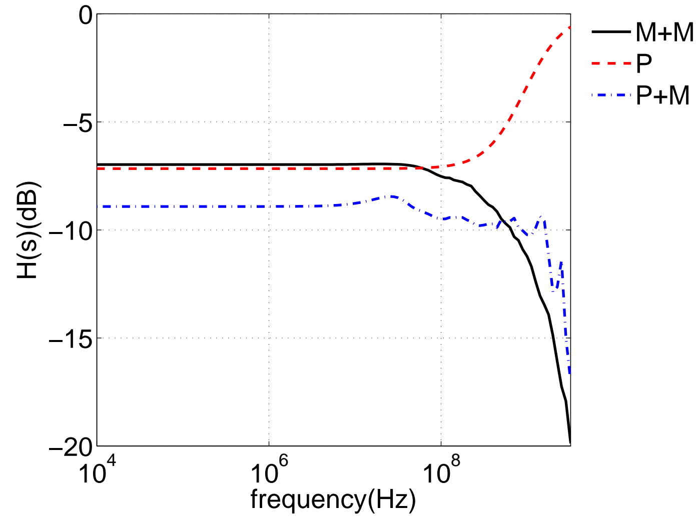

Figure IV.8: Transfer functions of RC, channel w/ and w/o using RC

The output voltage is

$$V_{out}^{RC} = \frac{Z_L}{Z_{RC} + Z_L + Z_0} V_3 \tag{IV.12}$$

RC at driver side

Since we assume a matched transmission line, the load reflection $\Gamma_L = 0$, and the input reflection is

$$\Gamma_{in}^{RC} = s_{11} = \frac{Z_{RC}}{Z_{RC} + 2Z_0}. \tag{IV.13}$$

The input impedance of RC is

$$Z_{in}^{RC} = Z_{RC} + Z_0. \tag{IV.14}$$

The voltage V_2 can be written as

$$V_2^{RC} = \frac{Z_0}{Z_{in} + Z_g} V_s. \tag{IV.15}$$

Fig. IV.8 shows the transfer function of RC in red dash line (assume the RC is connected to a $Z_L = Z_0$), the transfer function of the channel without and with using RC in black line and dash dot blue line, respectively. Similar to RL, the

RC structure is a high pass filter, and the 3dB bandwidth of output increases to 1.87 GHz when RC is used at the driver. Although the bandwidth has be greatly improved by using RL and RC, the output response has zigzags in high frequency. That is because these two topologies are not matched and introduce reflections.

IV.3.C T-junction structure

The S matrix of T-junction is

$$S_T = \begin{bmatrix} 0 & \frac{Z_2}{Z_0+Z_2} \\ \frac{Z_2}{Z_0+Z_2} & 0 \end{bmatrix} \tag{IV.16}$$

where $Z_2 = R + sL$. Notice that s_{11} and s_{22} of T-junction are zero because when matched, T-junction has no reflection and behaves as Z_0.

T-junction at receiver side

When the load impedance is R_L, the load reflection Γ_L is the same as (IV.9), and the input reflection is

$$\Gamma_{in}^T = s_{12}s_{21}\Gamma_L = (\frac{Z_2}{Z_0 + Z_2})^2\Gamma_L. \tag{IV.17}$$

The input impedance is

$$Z_{in}^T = \frac{1 + \Gamma_L(\frac{Z_2}{Z_2+Z_0})^2}{1 - \Gamma_L(\frac{Z_2}{Z_2+Z_0})^2} Z_0. \tag{IV.18}$$

The transfer function without considering reflection is

$$H_T = \frac{V_{out}^+}{V_4^+} = s_{21} = \frac{Z_2}{Z_0 + Z_2}. \tag{IV.19}$$

Considering reflection V_{out}^-, the voltage at output is

$$V_{out}^T = V_3 \frac{s_{21}}{2}(1 + \Gamma_L). \tag{IV.20}$$

For components T_m^c, T_m^p and T_u^p, $\Gamma_L = 0$ and $V_{out} = V_3 s_{21}/2$. For component T_u^c, the output voltage is determined by termination resistance.

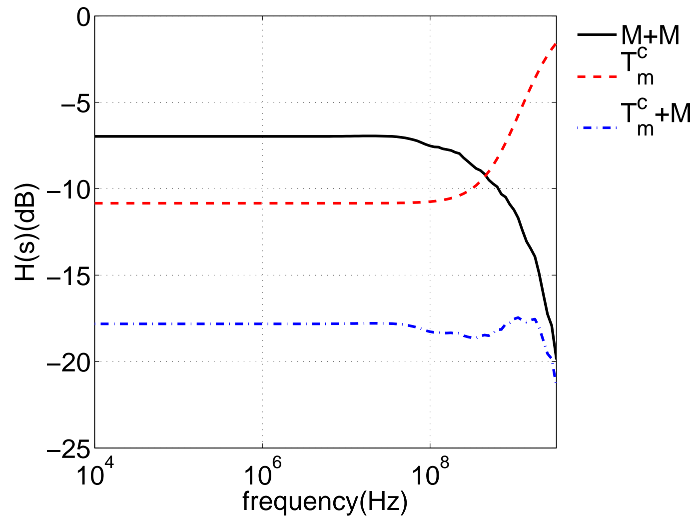

Figure IV.9: Transfer functions of T-junction, channel w/ and w/o using T-junction

T-junction at driver side

In this case, both the Γ_L and Γ_{in} are zero, and

$$Z_{in}^T = Z_0. \tag{IV.21}$$

Therefore, the voltage at output of T-junction is

$$V_2^T = \frac{s_{21}Z_0}{Z_0 + Z_g}V_s. \tag{IV.22}$$

For components T_m^c, T_m^p and T_u^p, $Z_g = 50\Omega$, hence $V_2 = V_s s_{21}/2$. For component T_u^c, $Z_g = 10\Omega$, and $V_2 = V_s\frac{5s_{21}}{6}$.

Fig. IV.9 shows the transfer function of T-junction in red dash line (assume the T-junction is connected to a $Z_L = Z_0$), the transfer function of the channel without and with using T-junction in black line and dash dot blue line, respectively. T-junction also acts as a high pass filter, and the 3dB bandwidth of output increases to 3.05 GHz when T-junction is used at the driver. Because when connects to $Z_g = Z_0$, T-junction behaves as a characteristic impedance from both sides, it significantly reduces the reflections introduced by the channel discontinuities. Therefore, the output response is very smooth comparing to the cases of

using RC and RL, and it enjoys the highest bandwidth as well.

IV.3.D Comparison

In this section, we compare the output voltages and input reflections of different structures and summarize the results into three claims.

Claim 1. At driver side, RC has larger output voltage than T-junction when $Z_2 Z_{RC} = Z_0^2$.

Having $Z_2 Z_{RC} = Z_0^2$, the driver side output voltage of T-junction in (IV.22) can be rewritten as

$$V_2^T = \frac{Z_0}{Z_0 + Z_g + Z_{RC} + \frac{Z_g Z_{RC}}{Z_0}} V_s, \tag{IV.23}$$

while the driver side output voltage of RC is

$$V_2^{RC} = \frac{Z_0}{Z_0 + Z_g + Z_{RC}} V_s \tag{IV.24}$$

according to (IV.15). Therefore, by having an extra term $Z_g Z_{RC}/Z_0$ in the denominator, V_2^T is always smaller than V_2^{RC}. Based on the definition of Z_{RC}, we know that when complex frequency $s \to 0$, $Z_{RC} \to R_d$ and $V_2^T < V_2^{RC}$. When $s \to \infty$, $Z_{RC} \to 0$ and $V_2^T = V_2^{RC} = Z_0 V_s/(Z_g + Z_0)$. It indicates that when used at driver side, T-junction structure has stronger ability to compensate the high frequency loss of the channel.

Claim 2. At receiver side, RC and RL have larger output voltage than T-junction when $Z_2 Z_{RC} = Z_0^2, Z_{RL} Z_{RC} = Z_0^2$.

Substituting Z_2 with Z_0^2/Z_{RC}, the output voltage of T-junction in (IV.20) becomes

$$\begin{aligned} V_{out}^T &= V_3(1 + \Gamma_L)\frac{s_{21}}{2} \\ &= V_3(1 + \Gamma_L)\frac{Z_0}{2Z_0 + 2Z_{RC}}, \end{aligned} \tag{IV.25}$$

and the output voltage of RC in (IV.12) is

$$V_{out}^{RC} = V_3(1 + \Gamma_L)\frac{Z_0}{(1 - \Gamma_L)Z_{RC} + 2Z_0}. \tag{IV.26}$$

Since $\Gamma_L \geq -1$, the denominator of V_{out}^{T} always has larger magnitude than the denominator of V_{out}^{RC}. Therefore, RC always has larger output than T-junction when used at receiver side. Substituting Z_{RL} with Z_0^2/Z_{RC}, the output voltage of RL in (IV.7) becomes

$$V_{out}^{RL} = \frac{Z_0}{Z_{RC} + Z_0} V_3. \tag{IV.27}$$

Since $(1 + \Gamma_L)/2$ is always smaller than 1, RL always has larger output than T-junction. When s changes from 0 to infinity, Z_{RC} reduces from R_d to 0 and the magnitude of $V_{out}^{T} = V_{out}^{RC} = V_3(1 + \Gamma_L)/2$, and $V_{out}^{RL} = V_3$, which indicates RL circuit has larger output voltage for high frequency.

Claim 3. At receiver side RC has larger input reflection than T-junction when $Z_2 Z_{RC} = Z_0^2$.

We can rewrite (IV.10)

$$\Gamma_{in}^{RC} = \Gamma_L + \frac{(1 - \Gamma_L)^2 Z_{RC}}{2Z_0 + (1 - \Gamma_L) Z_{RC}} \tag{IV.28}$$

which means the RC structure amplifies the load reflection. In contrast, (IV.17) shows that the input reflection of T-junction is always smaller than the load reflection, which means the T-junction has the ability to reduce reflections and alleviate discontinuity effects.

IV.4 Problem formulation and optimization framework

From the discussion in Section IV.3, it can be seen that the equalizer parameters determine the scattering parameters and influence the input impedance and output voltage. Therefore, for a given channel, there exists optimal values of these RLC parameters in terms of the eye-opening and jitter.

Table IV.3: Optimization variables for each component

Label	at driver side	at receiver side
M	none	none
S	NA	R_t, L_t
P	R_d, C_d	R_t, C_t, R_L
T_m^c	R_d, C_d	R_t, L_t
T_m^p	R_d, C_d	R_t, L_t
T_u^c	R_d, C_d	R_t, L_t, R_L
T_u^p	R_d, C_d	R_t, L_t, R_L

IV.4.A Problem formulation

Since we want to maximize eye-opening and minimize jitter, we define the cost function as

$$f(x) = -V_{eye} \times (T_c - jitter) \tag{IV.29}$$

in which x stands for the optimization variables, T_c is the cycle time. V_{eye} and $jitter$ are the worst case eye-opening voltage and timing jitter respectively. The cost function $f(x)$ reflects the white area in the eye diagram when the eye is a quadrangle, which is valid in the experiments.

The variables in our optimization include all the independent RLC parameters in the equalizers and the R_L. The number of variables varies when different schemes are being optimized, as shown in Table IV.3. For instance, for $T_m^c + M$ scheme, the variables are R_d and C_d at driver side, which determine the RC values in the parallel branch of T-junction. For $T_m^c + T_u^c$ scheme, there are five variables.

The problem formulation can be written as

$$\begin{aligned} min \quad & f(x) \\ s.t. \quad & 0 \leq R_t \leq R_{max} \\ & 0 \leq R_d \leq R_{max} \\ & 0 \leq R_L \leq R_{max} \\ & 0 \leq C_d \leq C_{max} \\ & 0 \leq L_t \leq L_{max} \\ & 0 \leq C_t \leq C_{max} \end{aligned} \tag{IV.30}$$

where R_{max}, C_{max} and L_{max} are upper-bounds for the variables.

For a given scheme and a set of variables, generating the eye diagram using circuit simulation with pseudo-random bit sequence (PRBS) is very time consuming, especially when employed in an iterative optimization flow. A peak-distortion analysis method was proposed in [11] to estimate the worst-case eye-opening voltage, which regards a general input bit sequence as the composition of unit pulse signals. Then for a linear time-invariant (LTI) system, the quality of eye diagram can be analyzed with the system's unit pulse response. The saturated ramp signal (also called step signal) is more fundamental than the unit pulse signal, because the pulse can be produced by a rising step and a falling step signals. In [69] and [67], the eye-opening voltage and timing jitter were estimated from the system's step response. However, their methods made assumptions on the step response's waveform. An accurate prediction method based on step response is established in [56], which is suitable for a general step response waveform and considers asymmetric signal transition.

For the design of CPU-memory links, the step-response based method is suitable for the prediction of V_{eye} and jitter, and the step responses include more physical intuition for optimizing the equalizers. With each given scheme and a set of variables, the step response is generated by HSPICE transient simulation. Afterwards, the method in [56] is used to predict the worst-case eye-opening and

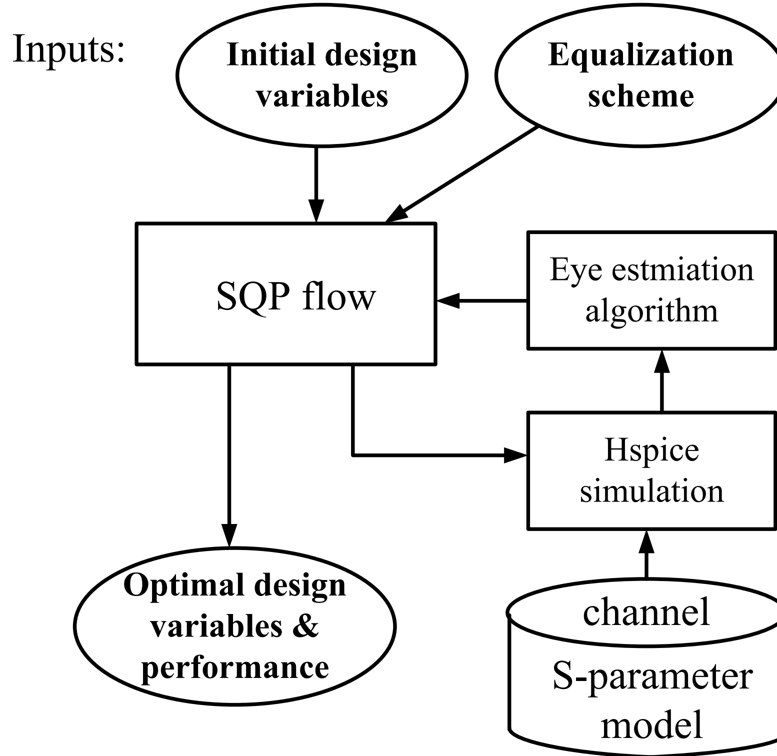

Figure IV.10: Optimization flow

jitter. Because of the quick saturation of step-response waveform, the eye diagram prediction consumes much less time.

IV.4.B Optimization framework

The relation between cost function and variables is complex and there is no closed-form solution. We use Sequential Quadratic Programming (SQP) method to solve it, which is the state of the art nonlinear programming method, and has been implemented in Matlab. Based on the works of [8], [29], [49], [50], the method closely mimics Newton's method for constrained optimization. At each iteration, a quasi-Newton updating method is used to derive the approximated Hessian of the Lagrangian function, which is then used to generate a quadratic programming subproblem, whose solution is used to obtain a search direction for a line search procedure. The SQP method relies on gradient information and maybe sensitive to the starting point.

The overall optimization flow is illustrated in Fig. IV.10. Inputs include the type of equalization schemes and the initial design variables. The SQP flow accepts the input information and after a number of iterations, outputs the optimal design variables and corresponding performance metrics. In each iteration of the SQP flow, first a SPICE net-list is generated according to the current design variables, and then SQP flow calls HSPICE to do circuit simulation with step input, in which the channel is described by an s-parameter model. After that, the step response is fed into the eye prediction algorithm to derive the worst-case eye-opening and jitter. Having the eye quality, SQP flow evaluates the cost function and determines the design variable values for next iteration step.

IV.5 CPU-memory links in IBM POWER6 system

We simulate the passive equalizer schemes based on the CPU-memory link of IBM POWER6^{TM} system. IBM introduced POWER6^{TM} microprocessor-based systems in 2007. The dual-core microprocessor has been fabricated in a 65 nm SOI process and contains over 700 million transistors. It can operate at over 5GHz frequency for high-performance applications and consumes less than 100 W for low power applications [25]. Due to these two modes of operation both the speed and the power are important design considerations for the POWER6^{TM} I/O circuitry and a challenge for the corresponding interconnection design.

According to [18], there are more than 800 wires coming off the processor chip dictated by system performance and scaling requirements. The total I/O bandwidth is around 300 GBps. The links between CPU and memory have bit-rate up to 3.2 Gbps/wire for single ended and 6.4 Gbps/wire for differential pair.

Each POWER6^{TM} chip includes two integrated memory controllers [43]. A memory controller supports up to four parallel channels, each of which can be connected through an off-chip interface to one to four buffer chips daisy-chained

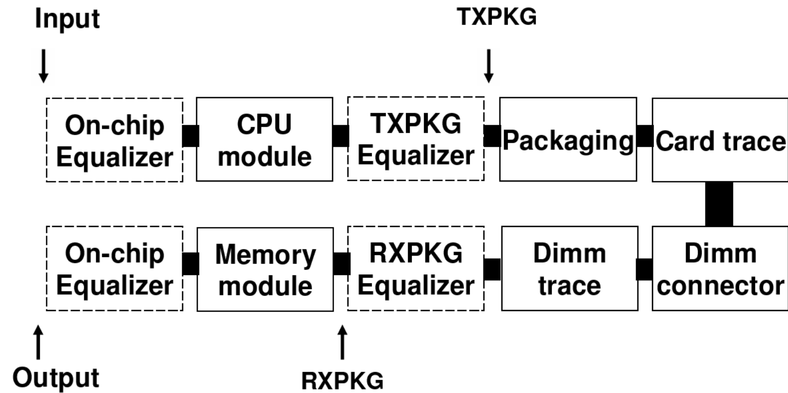

Figure IV.11: Structure of the CPU-memory link

together. A channel supports a 2-byte read datapath, a 1-byte write datapath, and a command path that operates four times faster than the DRAM frequency, which is up to 800 MHz. For some system configurations, buffer chips are mounted on the system board, through industry-standard DIMMs (dual inline memory modules) card. We use the off-chip CPU-memory links as our test case of the proposed equalizer schemes because this approach can improve the signal quality with little overhead on power consumption.

The channel is a 20 inches long differential pair, and we test with a data rate of 6.4 Gbps. The representative critical path of the channel (Fig. IV.11), from the chip carrier through card, board, to memory module is modeled and analyzed. The model takes all the fan-out, connector, and via array discontinuities into account. We observe waveforms at the input to the CPU module, at output from memory module, and two internal ports TXPKG and RXPKG, as shown in Fig. IV.11.

IV.6 Experimental results

IV.6.A Experimental setup

We model the 20-inch-long CPU-memory links with s-parameters and perform HSPICE simulation. The supply voltage is 1.1V and the bit rate is 6.4

Gbps with rise/fall time of 45 ps. We implemented the SQP optimization flow in Matlab and performed equalizer optimization. We compare the matched I/O results, in which all external and internal ports are matched with 100Ω differential impedance, with 42 different equalization schemes listed in Table IV.2 in terms of eye quality and power consumption. Table IV.4-IV.7 are the optimization results without consideration of size limit, and Table IV.8-IV.9 shows the results with size limit. The eye-openings and jitters listed in these tables are predicted worst-case values. Without size limit, the upper-bound of RLC parameters are set as $R_{max} = 500\Omega, C_{max} = 100pF, L_{max} = 100nH$. When size limit is considered, the inductor is no more than 5nH and the capacitor is no more than 15pF.

IV.6.B Optimization results without size limits

Table IV.4: Optimization results of Group 1 without size limit

Idx	Optimal solution				Performance			
	R_d	C_d	R_t	L_t or C_t	V_{eye}	$Jitter$	$3dBBW$	f
$M + M$	-	-	-	-	closed	-	0.65	-
$T_m^p + M$	56.79	4.65	-	-	0.178	22.80	2.12	-23.75
$T_m^c + M$	57.76	4.54	-	-	0.179	22.70	2.13	-23.90
$M + T_m^c$	-	-	43.28	11.35	0.179	22.68	2.13	-23.91
$T_m^p + T_m^c$	11.46	74.23	58.29	10.59	0.196	16.20	2.19	-27.50
$T_m^c + T_m^c$	11.46	74.23	58.29	10.59	0.196	15.98	2.19	-27.55
$M + T_m^p$	-	-	43.28	11.35	0.180	22.28	2.13	-24.16
$T_m^p + T_m^p$	12.43	66.23	47.76	8.16	0.195	12.46	2.33	-28.00
$T_m^c + T_m^p$	12.43	66.23	47.76	8.16	0.195	12.28	2.33	-28.03

Units for R, L and C are Ω, pF and nH.

Units of V_{eye}, $Jitter$, and BW(Bandwidth) are V, ps, and GHz.

Table IV.5: Optimization results of Group 2 without size limit

Idx	Optimal solution				Performance			
	R_d	C_d	R_t	L_t or C_t	V_{eye}	$Jitter$	$3dBBW$	f
$P+M$	64.11	4.02	-	-	0.121	49.62	1.87	-24.76
T_u^c+M	79.63	2.98	-	-	0.263	37.66	2.64	-31.25
T_u^p+M	78.62	2.90	-	-	0.277	35.30	2.67	-33.58
$P+T_m^c$	27.75	3.22	64.48	17.52	0.260	34.52	1.98	-31.66
$T_u^c+T_m^c$	41.80	2.79	99.33	31.53	0.265	31.03	2.62	-33.14
$T_u^p+T_m^c$	45.78	2.36	101.11	31.45	0.270	27.42	2.65	-34.84
$P+T_m^p$	27.58	3.11	60.42	16.65	0.259	33.69	2.61	-31.74
$T_u^c+T_m^p$	37.52	2.78	84.69	25.29	0.264	30.97	2.62	-33.08
$T_u^p+T_m^p$	74.92	1.71	150.67	100	0.268	18.05	2.79	-37.08

Units for R, L and C are Ω, pF and nH.

Units of V_{eye}, $Jitter$, and BW(Bandwidth) are V, ps, and GHz.

Table IV.6: Optimization results of Group 3 without size limit

Idx	Optimal solution					Performance			
	R_d	C_d	R_t	L_t or C_t	R_L	V_{eye}	$Jitter$	$3dBBW$	f
$M+P$	-	-	75.90	$4.92(pF)$	53.10	0.156	45.03	1.89	-17.37
T_m^c+P	57.67	4.68	0	$23.68(pF)$	57.67	0.186	24.62	2.13	-24.48
T_m^p+P	57.67	4.68	0	$23.68(pF)$	57.67	0.183	24.87	2.13	-24.09
$M+T_u^p$	-	-	32.70	9.13	99.20	0.209	28.50	2.39	-26.65
$T_m^p+T_u^p$	10.44	87.34	40.96	8.03	96.4	0.219	18.38	2.44	-30.23
$T_m^c+T_u^p$	9.94	92.36	40.54	8.15	99.6	0.220	18.18	2.45	-30.38
$M+S$	-	-	23.12	3.71	-	0.222	46.81	2.56	-24.30
T_m^p+S	18.82	33.03	33.84	3.27	-	0.252	31.09	2.61	-31.54
T_m^c+S	38.30	8.47	51.07	2.83	-	0.252	30.94	2.41	-31.58
$M+T_u^c$	-	-	15.07	3.26	348.06	0.242	31.50	3.16	-30.22
$T_m^p+T_u^c$	9.64	99.61	29.45	5.06	499.93	0.262	25.81	2.75	-34.23
$T_m^c+T_u^c$	9.64	99.61	29.45	5.04	499.93	0.263	25.51	2.75	-34.37

Units for R, L and C are Ω, pF and nH.

Units of V_{eye}, $Jitter$, and BW(Bandwidth) are V, ps, and GHz.

Table IV.7: Optimization results of Group 4 without size limit

Idx	Optimal solution					Performance			
	R_d	C_d	R_t	L_t or C_t	R_L	V_{eye}	$Jitter$	$3dBBW$	f
$P+P$	64.21	3.93	0.01	1.72(pF)	47.06	0.230	48.59	1.87	-24.81
T_u^c+P	67.85	2.39	26.66	26.96(pF)	53.56	0.264	28.79	2.72	-33.62
T_u^p+P	81.25	1.80	25.24	27.22(pF)	57.94	0.267	22.56	2.80	-35.71
$P+T_u^p$	20.95	0.52	17.92	5.32	162.48	0.264	43.40	2.76	-29.76
$T_u^c+T_u^p$	43.06	2.70	94.50	32.17	59.23	0.271	32.18	2.63	-33.62
$T_u^p+T_u^p$	39.54	2.40	79.31	59.48	23.16	0.277	29.32	2.65	-35.16
$P+S$	58.00	4.12	46.73	2.13	-	0.280	48.23	1.99	-30.27
T_u^c+S	60.21	3.95	45.49	1.98	-	0.311	43.65	2.71	-35.06
T_u^p+S	64.32	3.36	43.82	2.14	-	0.328	41.67	2.79	-37.57
$P+T_u^c$	18.64	0.87	17.06	3.74	363.08	0.313	40.47	2.70	-36.20
$T_u^c+T_u^c$	43.07	2.69	94.63	32.12	59.30	0.271	32.42	2.63	-33.56
$T_u^p+T_u^c$	39.76	2.35	79.12	22.54	60.60	0.276	30.14	2.65	-34.80

Units for R, L and C are Ω, pF and nH.

Units of V_{eye}, $Jitter$, and BW(Bandwidth) are V, ps, and GHz.

Table IV.4-IV.7 give the optimization results for 42 schemes. Optimal variable values and the corresponding eye heights and jitters at output ports, 3dB bandwidth and cost function f are given for each scheme. Fig. IV.12 through IV.20 illustrate the transfer functions and step responses of different schemes in each group. In Fig. IV.15, IV.17, IV.19, IV.26, the legends at right hand side are arranged according to the DC magnitude of the transfer function. For example in Fig. IV.15, scheme $P+M$, which has the largest DC transfer function, is on top of the legend list, scheme $T_u^p + T_m^p$ is at the bottom since it has the smallest DC transfer function. In Fig. **??**, **??**, IV.16, IV.18, IV.20, IV.27 and IV.28, the legends are organized according to the DC voltage level after the transition.

We notice that adopting equalizers opens the eye with V_{eye} ranges from 0.12V to 0.31V, and generally speaking, matched components generate smaller jitter while unmatched components produce larger eye due to reflection. We compare different schemes group by group in the following subsections.

Schemes in Group 1

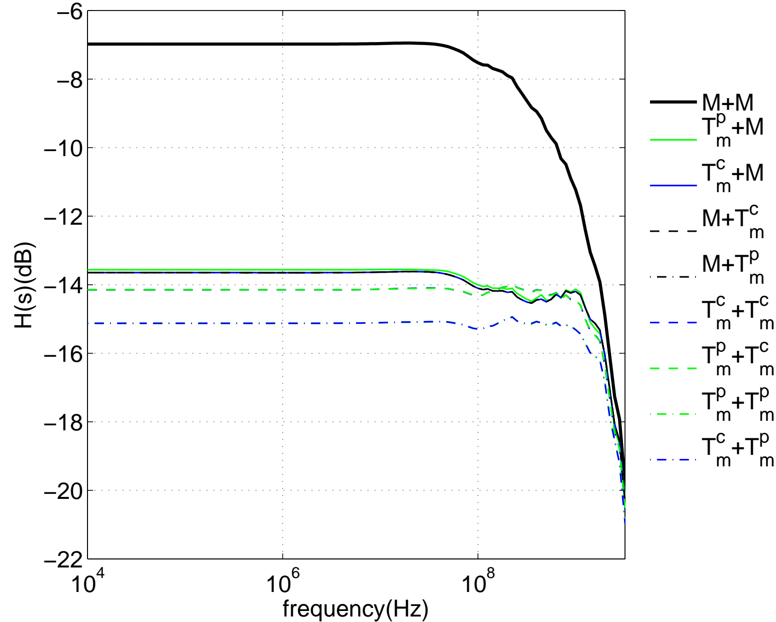

Figure IV.12: Transfer functions of solutions in Table IV.4

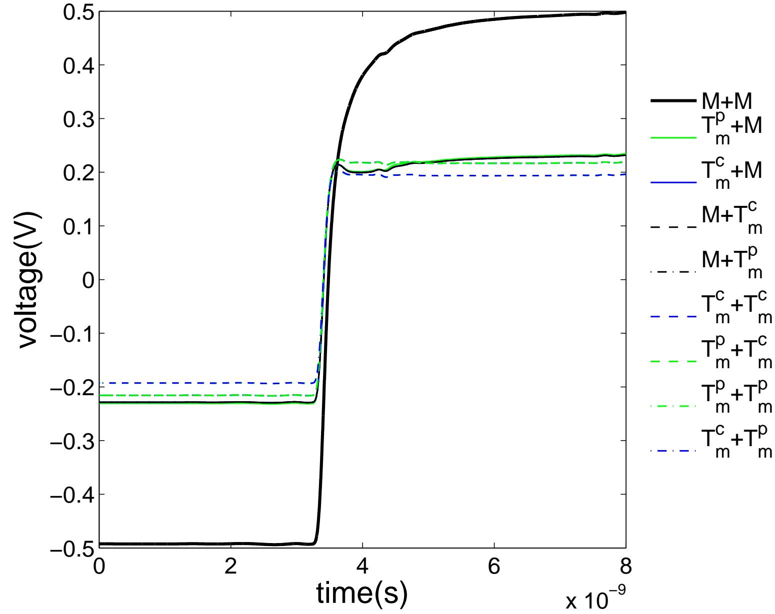

Figure IV.13: Step response (0 to 8ns) of solutions in Table IV.4

It can be observed from Table IV.4 that schemes in Group 1 fall into three categories according to the number of equalizers they use. If no equalizer is used (scheme $M + M$), there is no eye. If only one equalizer is used (schemes $T_m^c + M$, $T_m^p + M$, $M + T_m^c$ and $M + T_m^p$), the eye opening is from 178mV to 180mV and the jitter is 22-23ps. If two equalizers are used, the eye opening can reach 195mV or 196mV with jitter smaller than 17ps.

With the condition of matching, T_m^c is equivalent to T_m^p when used at driver side(IV.22, IV.20). At receiver side, we notice that T_m^p is slightly better than T_m^c in terms of jitter by comparing schemes $T_m^p + T_m^c$ with $T_m^p + T_m^p$, and schemes $T_m^c + T_m^c$ with $T_m^c + T_m^p$. The reason is that by inserting a T-junction structure between Dimm trace module and Memory module, off-chip T-junction has better ability to alleviate the discontinuities of the channel and therefore, reduce the reflections and the jitter.

Fig. IV.12 shows the transfer functions of different schemes, We see that with no equalizer the transfer function of the link is flat up to 30MHz, if one equalizer is used the corresponding transfer function decreases at 100MHz albeit

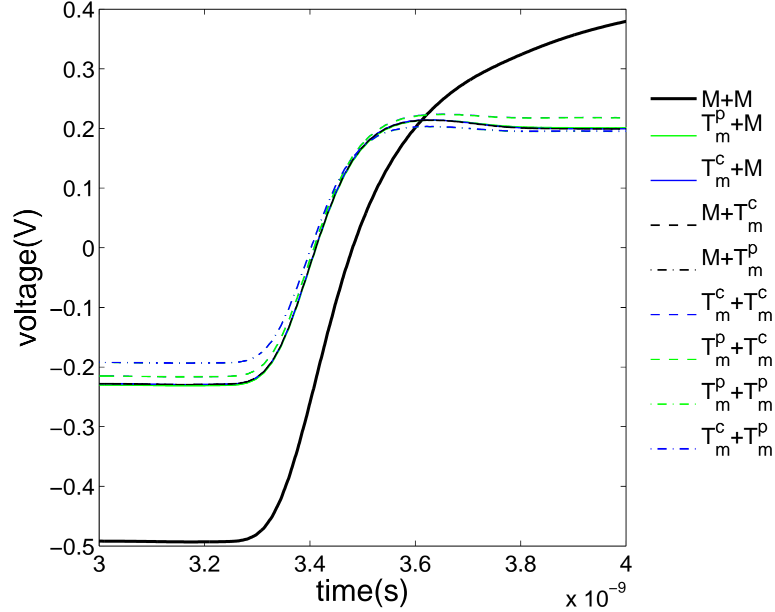

Figure IV.14: Step response (3ns to 4ns) of solutions in Table IV.4

with a significant reduction in magnitude as shown in Fig. IV.12. Two equalizers result in a further magnitude reduction of the transfer function of this link but they maintain a flat response up to 1GHz. This explains the eye-opening difference when different number of equalizers are used. It can also be seen that T_m^p at receiver side has a lower and flatter frequency response than T_m^c at receiver side, which tells us that T_m^p has smaller jitter.

Fig. IV.13, IV.14 present the step responses of schemes in Group 1. It can be seen that the DC voltage with one equalizer is larger than that with two equalizers, while the slew rate of rise edges of these two cases are very similar. As a result, it needs longer time for the schemes with one equalizer to get saturated, therefore, eye opening is slightly reduced.

The observations from Group 1 can be summarized as follows.

- Using T_m^c or T_m^p at both sides is better than using at one side only. If only one T-junction is used, the eye-opening is about 180 mV, the jitter is around 23 ps. If two T-junctions are used, the eye-opening is about 195 mV, the jitter is from 12 ps to 16 ps.

- T_m^c and T_m^p are equivalent when used at driver side.

Schemes in Group 2

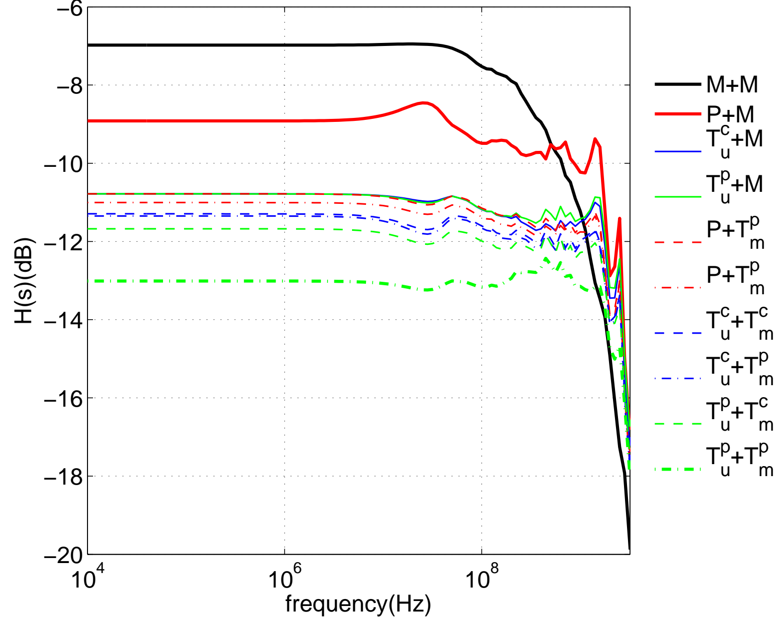

Figure IV.15: Transfer functions of solutions in Table IV.5

In Group 2, unmatched driver side equalizer can be P, T_u^c and T_u^p while the matched receiver side equalizer can be M, T_m^c and T_m^p. Based on the analysis of Group 1, we can expect that at receiver side, T_m^c and T_m^p are very similar and they are better than M. This trend can be observed in Table. IV.5.

By examining Table. IV.5, we find that in terms of parameter values and eye quality, (1) $T_u^c + M$ is similar to $T_u^p + M$, (2) $P + T_m^c$ is similar to $P + T_m^p$, (3) $T_u^c + T_m^c$, $T_u^p + T_m^c$ are similar to $T_u^c + T_m^p$.

Table. IV.5 also shows that for the same receiver side structure, T_u^p is very similar and slightly better than T_u^c, and T_u^c is better than P. T-junctions have larger eyes and lower jitters than RC because based on Claim 2 and (IV.23), T-junctions have smaller frequency response than RC at low frequency, which means RC has higher DC voltage level and needs longer time to get saturated. This can be observed in Fig. IV.15. When frequency goes up, the difference of

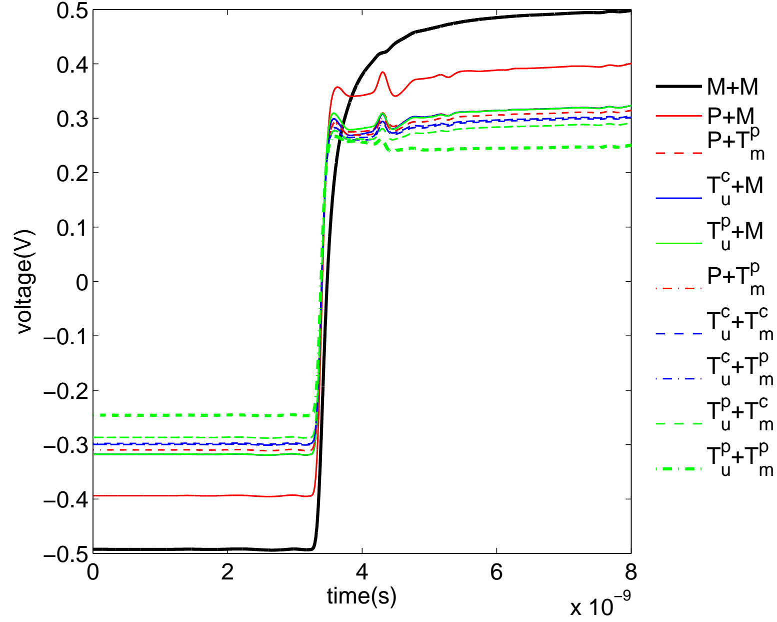

Figure IV.16: Step responses of solutions in Table IV.5

their transfer function approaches zero, which makes T-junction have a flatter total transfer function and better eye. The difference of using T_u^p and T_u^c at driver side comes from the difference of source resistance. In T_u^p, $Z_g = 50\Omega$ and in T_u^c, $Z_g = 10\Omega$. Therefore, the frequency response at DC of an off-chip T-junction is smaller, and its total transfer function over all frequency range is flatter.

The observations from Group 2 can be summarized as follows.

- At driver side, T-junctions are better than P.(Eye-opening is improved by more than 5 mV, and jitter is reduced by 7-15 ps.)
- At receiver side, T-junctions are better than matched.

Schemes in Group 3

In Group 3, matched equalizers (M, T_m^c and T_m^p) are used at driver side, and unmatched equalizers (P, S, T_u^c and T_u^p) are used at receiver side. Similarly to Group 2, it is observed in Table IV.6 that at driver side, T_m^c and T_m^p are very similar and they are better than M.

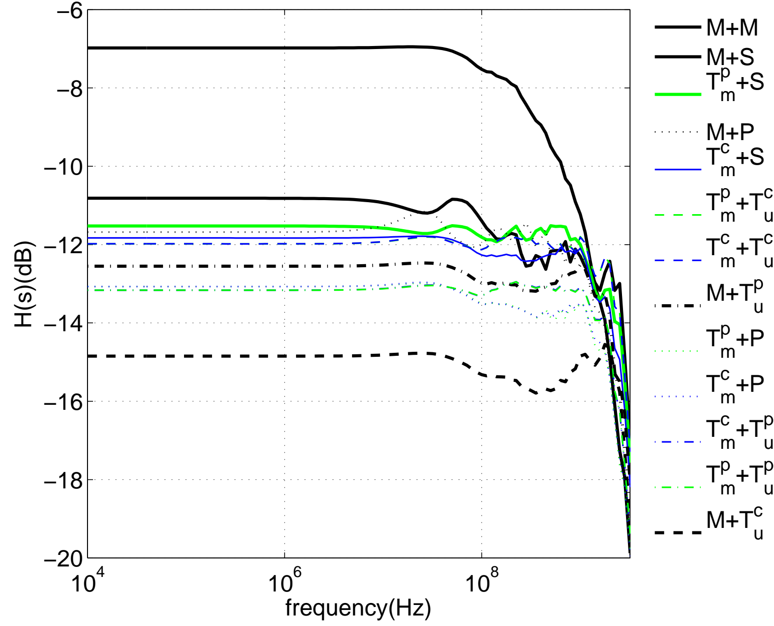

Figure IV.17: Transfer functions of solutions in Table IV.6

According to the parameter values and eye quality, schemes can be further grouped as: (1) $T_m^c + P$ is similar to $T_m^p + P$, (2) $T_m^p + T_u^p$ is similar to $T_m^c + T_u^p$, (3) $T_m^p + Sp$ is similar to $T_m^c + S$, (4) $T_m^p + T_u^c$ is similar to $T_m^c + T_u^c$.

Fig. IV.17 shows the frequency responses of these twelve schemes. It can be seen that, generally speaking, with different driver structure, the transfer functions of T_u^c and T_u^p are quite flat, which makes their eye better than other structures. Comparing the transfer functions of $M + T_u^c$ and $M + T_u^p$, $M + T_u^p$ has larger magnitude at low frequency and begins to drop after 1GHz, while $M + T_u^c$ has smaller DC magnitude and the drop starts around 2GHz, and its magnitude at 3.2GHz(which is half of the operating frequency) is larger than $M + T_u^p$. This explains that $M + T_u^c$ has a larger eye-opening. For the cases of T_m^c and T_m^p at driver side, it also can be seen that T_u^c has larger magnitude than T_u^p at 3.2GHz.

The transfer functions of $M + P$ and $M + S$ have fluctuation beyond 30MHz, which reduces the eye-opening and increases jitter. For $T_m^c + P$, $T_m^c + S$, $T_m^p + P$ and $T_m^p + S$, the variation on transfer functions gets smaller, therefore, both eye and jitter are improved.

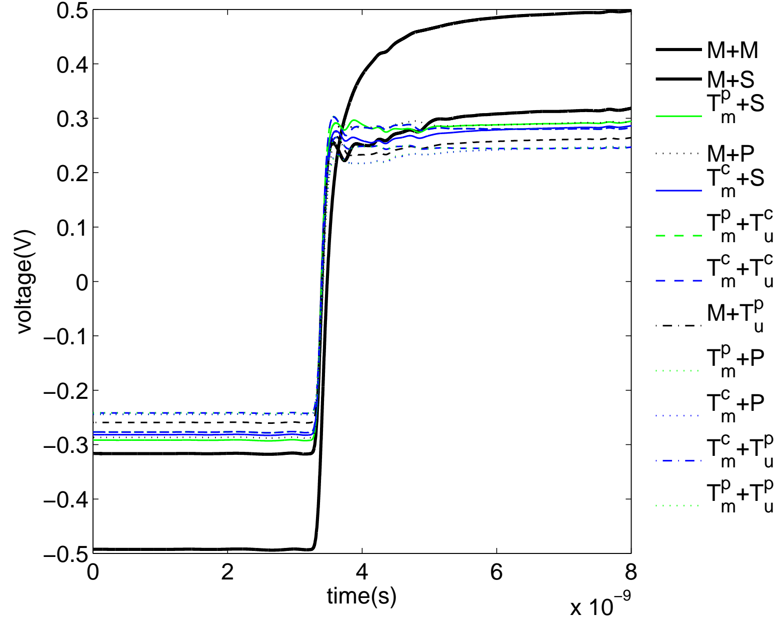

Figure IV.18: Step responses of solutions in Table IV.6

The observations from Group 3 can be summarized as follows.

- At driver side, T-junctions are better than M. (Eye-opening is improved by 20-30mV, jitter is reduced by 6-20ps.)
- At receiver side, P has the smallest eye opening (Below 190 mV).
- At receiver side, T_u^c has the largest eye opening (Above 240 mV).
- At receiver side, T_u^p has the smallest jitter (Between 18-28 ps).
- At receiver side, S has the largest jitter (Between 25-31 ps).

Schemes in Group 4

Both driver side and receiver side are unmatched for the schemes and therefore reflections affect the performance in Group 4. Structures T_u^p, T_u^c and P are used at both sides, but S is used only at receiver side. Similar with Group 2, T_u^p is slightly better than T_u^c at driver side. When P is at driver side, the jitter is

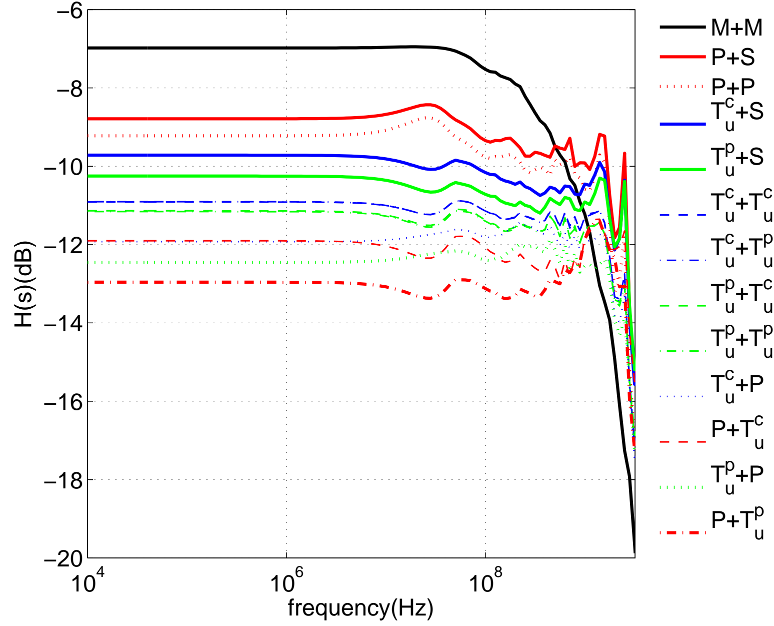

Figure IV.19: Transfer functions of solutions in Table IV.7

large since the transfer functions exhibit local maxima and minima at 10MHz and 100MHz, respectively(Fig. IV.19).

Similar to the previous groups, by observing the parameter values and eye quality, we can group the schemes as follows: (1) $T_u^c + P$ is similar to $T_u^p + P$, (2) $T_u^c + T_u^p$ is similar to $T_u^p + T_u^p$, (3) $T_u^c + S$, $T_u^p + S$ and $T_u^c + T_u^c$ are similar to $T_u^p + T_u^c$.

With the same driver side structure, Table. IV.7 shows that structure S has large jitter on average because S has larger reflection and higher DC voltage (Fig. IV.20). The eye-opening of P is small comparing to S since according to Claim 1, its DC voltage is lower while the reflection is obvious. We can also find that schemes $T_u^c + T_u^p$, $T_u^p + T_u^p$, $T_u^c + T_u^c$ and $T_u^p + T_u^c$ are very similar. As we will see in Table. IV.10, because of relative large reflection, schemes in Group 4 are the most sensitive to parameter variations.

The observations from Group 4 can be summarized as follows.

- At driver side, P has large jitter. (Between 40-48ps)
- At receiver side, P has the smallest eye opening. (Between 230-267 mV)

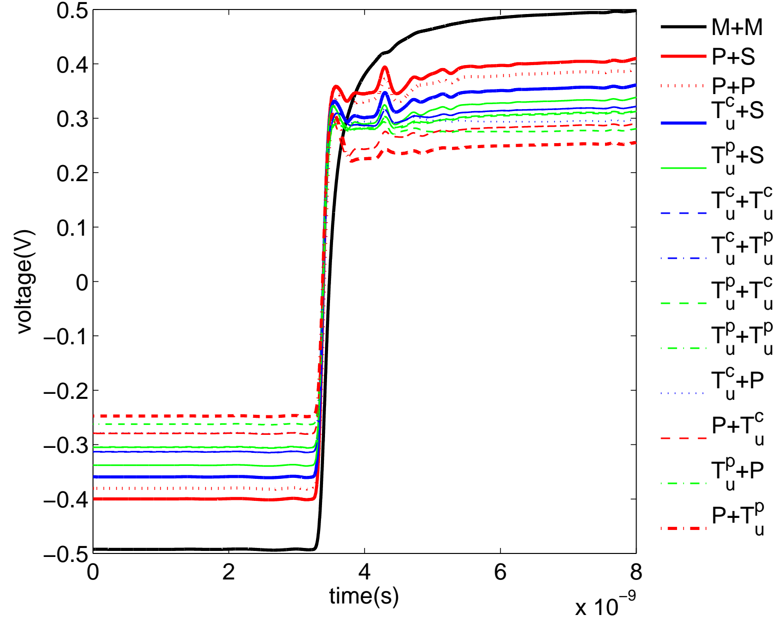

Figure IV.20: Step responses of solutions in Table IV.7

- At receiver side, S has the largest jitter. (Between 41-48 ps)
- Schemes $T_u^c + T_u^p$, $T_u^p + T_u^p$, $T_u^c + T_u^c$ and $T_u^p + T_u^c$ are very similar.

Summary

After analyzing these four groups, we can have the following conclusions. (1) Schemes in Group 1 have lower jitter due to the matching condition at both sides. (2) Schemes in Group 4 have larger eye-opening due to reflections. (3) When used at driver side, structure T_m^c is very similar to T_m^p. (4) When used at receiver end, structure T_m^c has slightly lower jitter than T_m^p, and structure T_u^c is very similar to T_u^p. (5) When used at receiver end, structure P has smaller eye-opening, while S has larger jitter.

IV.6.C Optimization results with size limits

Table IV.8: Optimization results of Group 1 and 2 with size limit

Idx	Optimal solution				Performance				
	R_d	C_d	R_t	L_t or C_t	V_{eye}	$Jitter$	$3dBBW$	Power	f
$M+M$	-	-	-	-	closed	-	0.65	7.86	-
$M+T_m^c$	-	-	20.50	5.00	0.168	29.39	3.03	7.86	-21.21
$T_m^c+T_m^c$	0.006	1.66	20.12	4.96	0.168	29.87	3.05	7.86	-21.23
$P+T_m^c$	31.87	4.16	33.67	5.00	0.219	45.16	2.80	7.96	-24.17
$P+M$	64.11	4.02	-	-	0.232	49.62	1.87	6.74	-24.76
$T_u^p+T_m^c$	119.09	1.93	499.91	5.00	0.242	33.53	2.96	15.75	-29.67
T_u^p+M	98.39	2.00	-	-	0.257	29.91	2.74	15.59	-32.47

Units for R, L and C are Ω, pF and nH.

Units of V_{eye}, $Jitter$, Power and BW(Bandwidth) are V, ps, mW and GHz.

Table IV.9: Optimization results of Group 3 and 4 with size limit

Idx	Optimal solution					Performance				
	R_d	C_d	R_t	L_t or C_t	R_L	V_{eye}	$Jitter$	$3dBBW$	Power	f
$M+P$	-	-	176.44	1.89(pF)	83.53	0.146	50.55	2.28	6.20	-15.39
T_m^c+P	136.46	1.96	0.07	0.96(pF)	69.31	0.178	35.17	3.15	10.43	-21.50
$M+S$	-	-	23.12	3.71	-	0.222	46.81	2.65	8.32	-24.30
T_m^c+S	100.01	2.0	53.84	2.47	-	0.196	31.33	3.06	10.38	-24.47
$M+T_u^c$	-	-	15.53	3.75	204.38	0.236	32.52	3.21	7.81	-29.24
$T_m^c+T_u^c$	0	0	15.13	3.35	458.32	0.250	32.67	3.17	7.79	-30.93
$P+P$	64.21	3.93	0.01	1.72(pF)	47.06	0.230	48.59	1.87	6.77	-24.81
$P+S$	58.00	4.12	46.73	2.13	-	0.280	48.23	1.99	6.97	-30.27
$T_u^p+T_u^c$	59.88	1.5	33.98	4.84	257.82	0.271	38.49	3.07	15.37	-32.00
T_u^p+P	99.5	2.0	0	0.59(pF)	51.13	0.258	29.44	2.75	15.60	-32.77
$P+T_u^c$	18.64	0.87	17.06	3.74	363.08	0.313	40.47	2.97	8.77	-36.20
T_u^p+S	106.71	1.97	49.67	2.22	-	0.302	35.66	3.10	15.66	-36.39

Units for R, L and C are Ω, pF and nH.

Units of V_{eye}, $Jitter$, Power and BW(Bandwidth) are V, ps, mW and GHz.

In this section, the results with considering physical size limit of the parameters are discussed. The inductor value is no more than 5nH, while capacitor is no more than 15 pF. After the analysis in Section. IV.6.B, we know that structure T_m^p is very close to T_m^c, and T_u^c and T_u^p have very similar effects in all schemes. Thus we can simplify our experiment by merging the similar structures and reducing the number of schemes. Table IV.8,IV.9 show the optimization results of 19 schemes with size limit consideration. Besides optimal solutions, eye-openings, jitters 3dB bandwidth and cost functions, total power consumptions(col.9) are also given in the tables.

Comparing with the results in Table IV.4-IV.7, the performance of most schemes becomes worse, except for $P + M$, $M + S$, $P + P$ and $P + S$. We choose four representative schemes for further analysis: $M+T_m^c$(the smallest jitter), $M + P$(the lowest power), $P + T_u^c$(the largest eye-opening), $T_u^p + S$(the smallest cost function). Fig. IV.22- IV.25 show the eye diagrams of different schemes at each port. Fig. IV.26-IV.28 present the transfer function and step response of these schemes. The eye diagrams of $M + M$ at each port are given in Fig. IV.21 as reference.

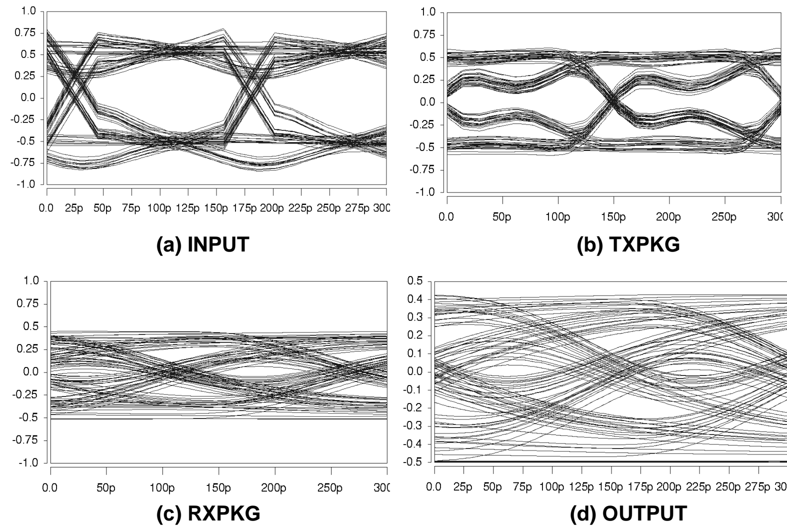

Figure IV.21: Eye diagrams of M+M

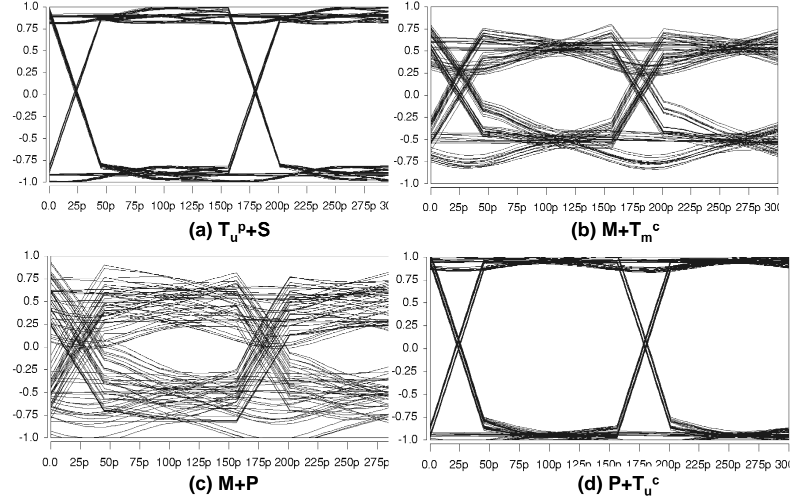

Figure IV.22: Eye diagrams at input port

Eye diagram comparison of different schemes

The eye diagrams of different schemes are compared in this section.

From Fig. IV.25 we can see that $M + T_m^c$ satisfies matching condition at both the driver and the receiver sides and has the smallest jitter. It also has the lowest DC voltage level, which can be explained by observing its transfer function in Fig. IV.26. It has the smallest magnitude and the variation is very small, which makes the jitter very small. Fig. IV.25 shows that both $T_u^p + S$ and $P + T_u^c$ have large eye opening. $T_u^p + S$ has smaller jitter than $P + T_u^c$ since its DC voltage is lower than $P + T_u^c$. Comparing the transfer function of these two schemes in Fig. IV.26, we notice that they have the same magnitude at 3.2GHz, and the DC voltage of $P + T_u^c$ is larger, which explains that the eye opening of $P + T_u^c$ is slightly larger than $T_u^p + S$. In contrast, the transfer function of $M + P$ has smaller magnitude at 3.2GHz, therefore, its eye-opening is much smaller. Fig. IV.27 shows that $M + T_m^c$ has a very flat step response after 5ns because matched driver and receiver eliminate most of the reflections, while other schemes have many small up and downs around 5ns (voltage rises up at 10ns for $M + P$) due to reflections. In Fig. IV.28, it shows that $T_u^p + S$ and $P + T_u^c$ have the most sharp rise edges which produce large eye-opening, and $M + T_m^c$ has the slowest rise edge and therefore,

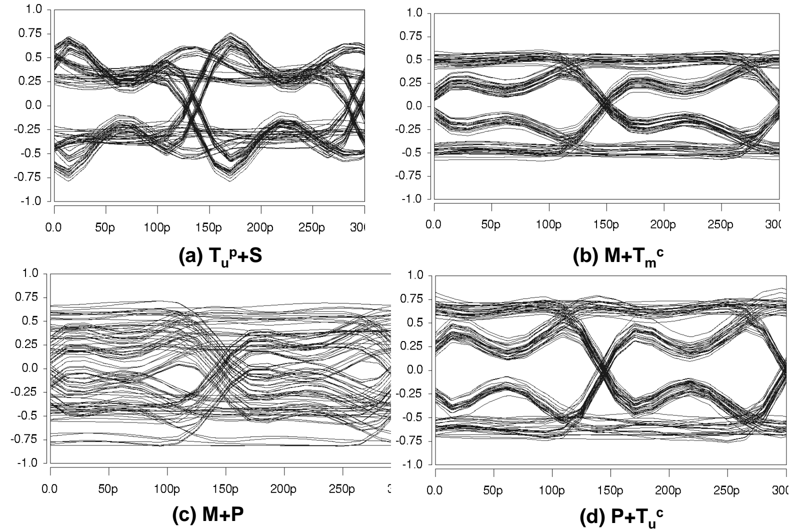

Figure IV.23: Eye diagrams at TXPKG

its eye-opening is the smallest.

Total power comparison of different schemes

Fig. IV.29 shows that the input impedance at low frequency has great impact on total power consumption. Scheme $M + P$ has the largest impedance and therefore, the lowest power consumption (6.2 mW). Similarly, $T_u^p + S$ has the highest power consumption (15.7 mW) because its impedance is the smallest.

Eye diagrams for 8 Gbps and 10 Gbps bit rate

For the four representative schemes, we perform our optimization flow with 8 Gbps and 10 Gbps bit rate and we find that the two schemes with smaller eye opening, $M + T_m^c$ and $M + P$ do not have eye at 8 Gbps. The eye diagrams of the other two schemes are shown in Fig. IV.30. Schemes $T_u^p + S$ and $P + T_u^c$ work well with the bit rate of 8 Gbps according to Fig. IV.30(a) and (c), while the data rate increases to 10 Gbps, the eye opening drops below 100 mV, which may introduce recovery problem at receiver side.

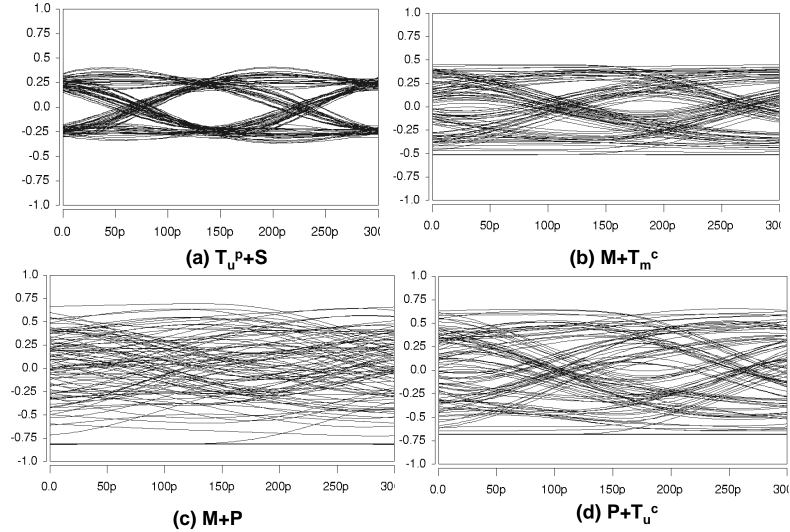

Figure IV.24: Eye diagrams at port RXPKG

Table IV.10: Sensitivity comparison

Idx	V_{eye}^{max}	V_{eye}^{min}	V_{eye} var.	J^{max}	J^{min}	$\frac{J^{min}}{T_c} - \frac{J^{max}}{T_c}$
$M + T_m^c$	0.170	0.147	14%	40.1	25.6	25.7%-16.4%
$M + P$	0.149	0.115	23%	63.7	48.0	40.8%-30.7%
$T_u^p + S$	0.308	0.228	26%	48.1	31.1	30.8%-19.9%
$P + T_u^c$	0.320	0.255	20%	56.4	36.6	36.1%-23.4%

Sensitivity comparison

To study the sensitivity of eye quality with respect to the parameters variation, we perturb the RLGC values by ±15% and record the range of eye-opening and jitter. We summarize the sensitivity comparison results in Table IV.10. The variation is calculated by dividing the minimum value with the maximum value. The fluctuation on eye opening is no more than 26%, and the variation of jitter over cycle time is no more than 13%.

Crosstalk effect

To study the crosstalk effect for the four representative schemes, we consider eight switching neighbors (four on right and four on left) with input pattern of "0101..." simultaneously, and perturb the RLCG values by ± 15%. The eye

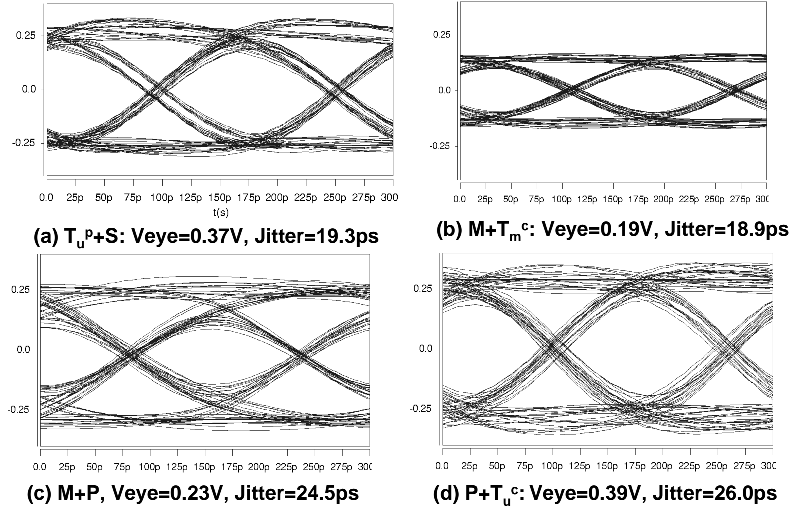

Figure IV.25: Eye diagrams at output

diagrams at output with crosstalk effect are shown in Fig. IV.31 By comparing Fig. IV.31 and Fig. IV.25, we notice that the largest variation on eye-opening and jitter are both around 10%, corresponding to scheme $T_u^p + S$. The equalization schemes are robust against crosstalk.

IV.7 Summary

A set of low power passive equalizers are proposed and optimized in this work. The equalizer topologies include T-junction, parallel RC and series RL structures. These structures can be inserted either at driver or receiver side at both the chip and package levels to improve the channel bandwidth can be improved with little extra power consumption. We investigate and compare the s parameters and reflections of these topologies, and demonstrate their effects on the total transfer function. We simulate and compare different schemes with the CPU-memory link of IBM POWER6^{TM} system with/without consideration of the physical size limit of the RLGC values.

Our experimental results show that without employing any equalizers, the eye of the output is closed at the bit rate of 6.4 Gb/s. We implement 42

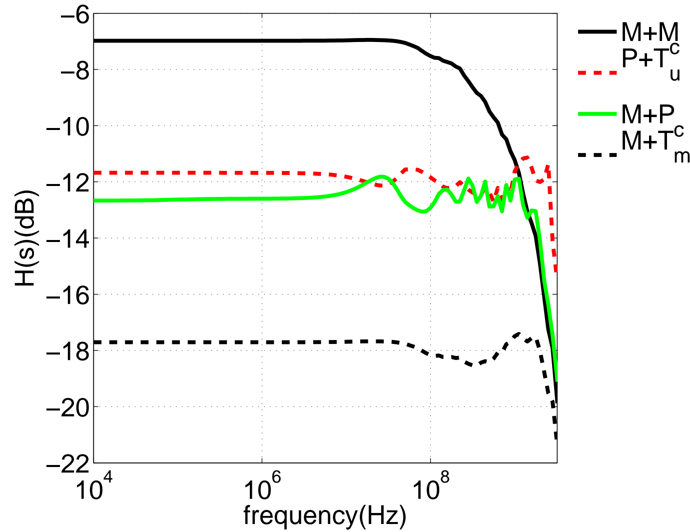

Figure IV.26: Transfer functions of different schemes

different equalizer schemes and find large variation in the predicted eye diagrams. The schemes with both the driver and receiver matched have lower jitter while the schemes with neither driver and receiver matched have larger eye-openings. With 6.4 Gb/s bit rate, the maximum eye height (scheme $P+T_u^c$) is more than 300 mV at a power cost of 8.8 mW. Scheme $M+T_m^c$ yields a minimum jitter of 29 ps at a power cost of 7.9 mW. Experimental results also demonstrate that the proposed schemes can operate with the bit rate of 8 Gb/s.

Chapter 4 includes the content of two published papers, “Low Power Passive Equalizer Optimization Using Tritonic Step Response”, by L. Zhang, W. Yu, H. Zhu, A. Deutsch, G. A. Katopis, D. M. Dreps, E. Kuh, C-K Cheng, in Proceedings of IEEE Design Automation Conference in 2008, “Low Power Passive Equalization Design for Computer Memory Links”, by L. Zhang, W. Yu, Y. Zhang, R. Wang, A. Deutsch, G. A. Katopis, D. M. Dreps, J. Buckwalter, E. Kuh, C-K Cheng, in Proceedings of IEEE Symposium on High Performance Interconnects in 2008. Chapter 4 also includes the contents being prepared for submission of Transactions on Advanced Packaging. The dissertation author was the primary investigator and author of this paper.

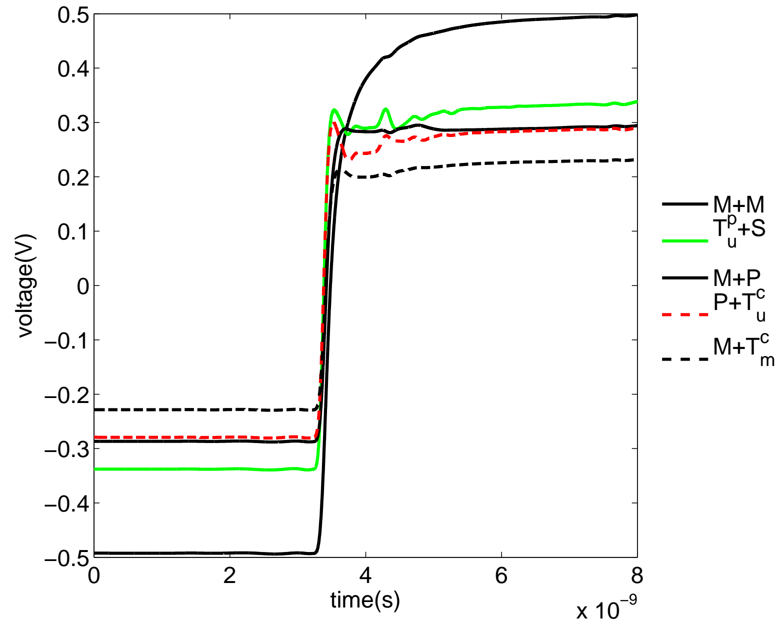

Figure IV.27: Step responses of different schemes

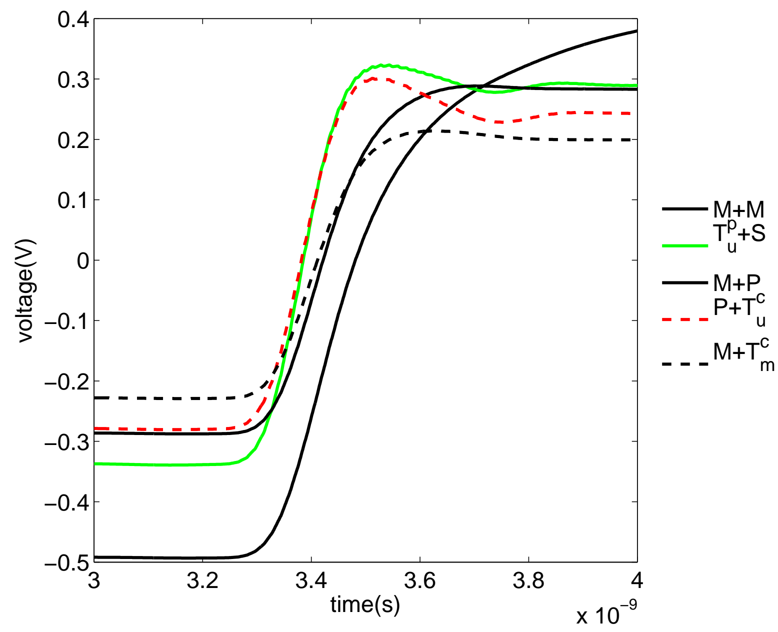

Figure IV.28: Step responses between 3ns and 4ns of different schemes

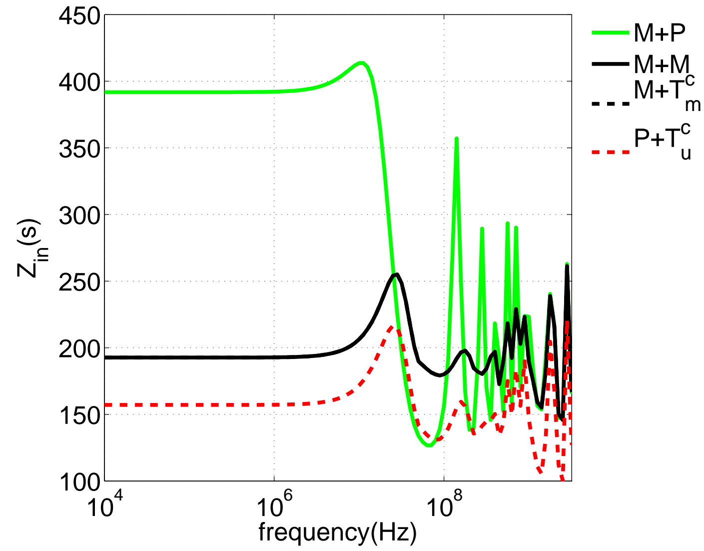

Figure IV.29: Input impedances of different schemes

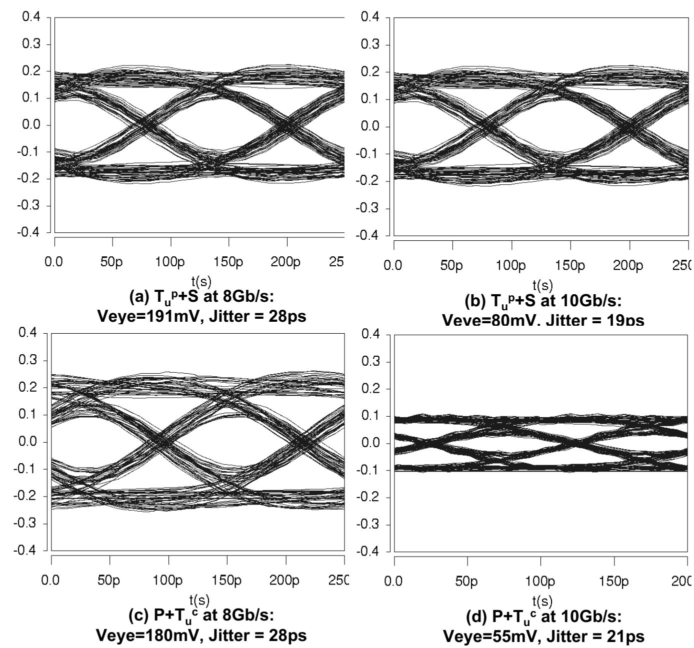

Figure IV.30: Eye diagrams at higher data rate

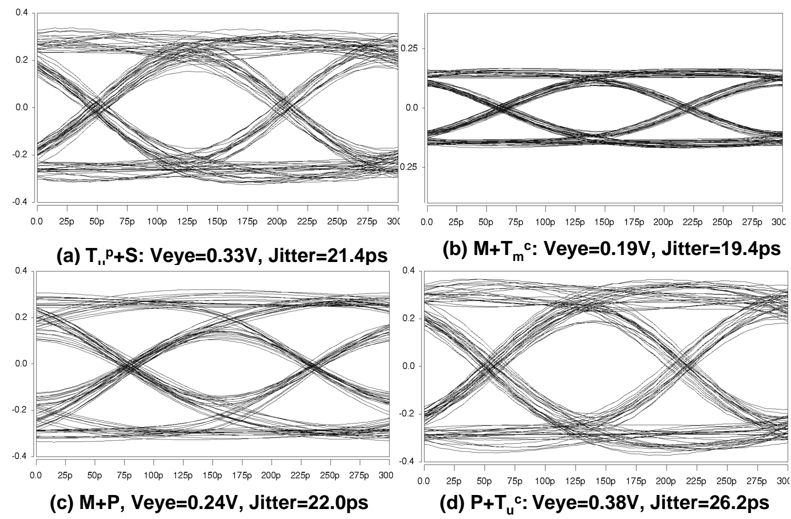

Figure IV.31: Eye diagrams at output with crosstalk effect

V

Conclusions

V.1 Summary of contributions

In this dissertation, we have focused on the design of both on-chip and off-chip high performance interconnects. We emphasized on the low power feature of the communication schemes we proposed, and we developed an optimization frame work based on SQP (Sequential Quadratic Programming) method to optimize these schemes under certain (or can be user specified) design goals.

Based on the structure of widely used repeated RC wires, Chapter II systematically optimizes the wire dimension, repeater size and repeater insertion interval assuming identical single-stage repeaters are inserted in a uniform metal wire with the same interval. The optimization is carried out with three different design goals: minimizing delay, minimizing delay$\times$power and minimizing delay$^2\times$power, and the metrics of delay, power, and bandwidth are evaluated at different wire pitches. We found that: 1) the repeater to wire capacitance ratio depends only on the objective function and technology, and remains constant when wire pitch changes; 2) each metric has its own optimal pitch region, and the region scales down with technology; and 3) among the commonly used objective functions, minimizing delay$^2\times$power shows a better trade-off between delay and power compared with minimizing delay and minimizing delay*power. At 22nm technology, the re-

peater RC wires can operate with a minimum delay of 55 ps/mm when pitch is 0.4-0.5μm, and the power cost is 0.3 pJ/mm; when delay$^2\times$power is optimized, the delay increases to 70 ps/mm at the same pitch with power cost of 0.15 pJ/mm.

In chapter III, an on-chip differential transmission line signaling scheme with passive compensation is proposed and optimized. The transceiver consists of a sense amplifier driving an inverter chain with fixed size ratio. We compare the performance of the proposed transmission line approach with the repeated RC wire across 90nm to 22nm technologies, and the experimental results indicates that the transmission line is scalable, and there are significant improvements of latency, power and throughput. At 22nm technology, the latency is 10 ps/mm, the power is 0.02 pJ/m, and the throughput is around 15 Gbps/μm (improved by 20% compared to RC wire).

Chapter IV discusses the design and optimization for off-chip transmission line using passive equalization. The equalizer topologies include T-junction, parallel RC and series RL structures. These structures can be inserted either at driver or receiver sides at both the chip and package levels to improve the channel bandwidth can be improved with little extra power consumption. We test these passive equalizers on a CPU-Memory link used in IBM POWER6 server. The experimental results show that without using any equalizer, the output eye is closed at 6.4 Gbps data rate, while equalizers are used, the maximum achievable eye opening is around 0.3 V with a power cost of only 8.8 mW (This measurement includes the power dissipated on the channel and the equalizers). It is also demonstrated that the passive equalization approach is not sensitive to variations and crosstalk.

V.2 Future work

Our study shows promising results of using on-chip transmission line for global wiring, however a number of modifications can be made based on the approach we proposed. The wires can be single-ended instead of differential, in which case modeling crosstalk effect becomes critical since single-ended wires are more

sensitive to noise. At the receiver side, amplifiers other than sense amplifier can be used to simplify the design since sense amplifier requires dedicated clock signal. Considering the substantial chip area consumed by the passive components, wires without equalization need further investigation.

For the passive equalization techniques for off-chip communication, one important future work is to model the on-chip or on-package resistor, inductor and capacitor more accurately. The Q factor and parasitic effect of these elements need to be estimated and taken into account due to the very high operating frequency. These factors are of practical interests if we are to use the equalization in real application.

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