University of California
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Identifying Mechanisms of AM-PM Distortion in Large Signal Amplifiers

A thesis submitted in partial satisfaction
of the requirements for the degree
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by

Soheil Golara

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Abstract of the Thesis

Identifying Mechanisms of AM-PM Distortion in Large Signal Amplifiers

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Master of Science in Electrical Engineering

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Professor Asad A. Abidi, Chair

We define the nonlinear dynamic phenomenon of AM to PM distortion and discuss different candidate mechanisms. Qualitative descriptions of this from of distortion are turned into expressions, and are applied to FET RF power amplifier described in the literature. Most importantly, we are able to identify the dominant mechanism of AM-PM distortion in various practical circuits, which then suggests methods of remediation. Our theory is shown to match simulations and measurements.

The thesis of Soheil Golara is approved.

Shervin Moloudi

Sudhakar Pamarti

Behzad Razavi

Asad A. Abidi, Committee Chair

University of California, Los Angeles

2015

To my parents

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I cannot think of a better supervisor to have. He is a teacher from whom I have learned the vital skill of disciplined critical thinking.

I would also like to thank Dr. Shervin Moloudi for his guidance during this thesis. I am truly thankful for his generous help and selfless dedication to the development of my work.

This thesis builds on one of Shervin's earlier unpublished works on nonlinearity of amplifier conducted at UCLA. Shervin had done an insightful work identifying the AM-PM mechanisms with descriptions which laid the foundations for my work. In his work, he had identified and explained the effect of device capacitors on AM-PM distortion. In addition, he had described the harmonics effect on phase distortion clearly. I was fortunate to access his work and learn about his viewpoints on the problem, which paved the way for my thesis.

Vita

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CHAPTER 1

Introduction

1.1 Background and aim of the research

Modern wireless communication standards use spectrally efficient linear modulation schemes that are sensitive to both amplitude and phase errors[3, 4]. Any nonlinearity in the transmitter, causes spectral regrowth and to avoid interfering with adjacent channels, we need to use highly linear power amplifier because it dominates linearity of transmitter[5].
Amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions are two significant distortion effects in PAs, causing spectral regrowth in the transmitted signal and bit errors in the received signal.

AM-AM shows itself as compression in amplifier gain, however amplitude dependent phase distortion, AM-PM, might begin to affect the linearity several dBs below the compression point [3, 6] and its measurement is more complicated and requires high-precision instruments [7].

Trade off between power efficiency and linearity, makes PA design more challenging. As we lower the amplifier output power, the amplifier becomes more linear at the expense of lower power efficiency [8]. The modulation schemes with high PAPR[1], require the power amplifier to work at power levels much lower than its saturated power, to satisfy the linearity requirements of transmitter. AM-AM and AM-PM characteristics of amplifier, show how much we need to *back off* from

[1]Peak-to-Average Power Ratio

saturated power. As we use higher order modulations, AM-AM and AM-PM will have a more serious effect on a system performance and we have to further back off. The back off can be as much as 15 or 20 dB for SSPAs and TWTAs [9]. In some applications, backing off does not adequately remove the AM-PM conversion, and it dominates the amplifier distortion [10].

CMOS is the desired technology to fully integrate the system-on-chip (SoC), and power amplifier is the most challenging block to implement in CMOS. Power amplifiers implemented in modern CMOS processes show much larger AM-PM distortion due to highly nonlinear parasitic capacitance and output resistance [11,12].

1.2 Contribution of this work

This work explains the AM-PM distortion mechanisms with simple expressions. Many efforts have been made to identify the sources of AM-PM distortion [1, 3, 13–17]. These studies have mostly relied on simulations for identifying the mechanisms. While simulations allow the designer to detect the existence of the effects at the outcome level, they do not uncover the causal processes that lead to intuition in the design process.

As a result these studies have yielded complicated expressions that mask the major effects by attempting to over-explain the phenomenon. The high number of parameters in such formulations limits the insight that could be obtained from them. The simplicity of our analysis makes it possible to capture the dominant sources that contribute to phase distortion and gain deeper intuition into what happens and why.

We have used EKV model [18,19] to explain how AM-PM distortion occurs in linear power amplifiers. Our explanation yields simple equations that reasonably match the simulation results. Although our theory is approximate, it describes the phase distortion process using first principles and successfully identifies the

dominant mechanisms in different amplifiers

Uncovering the causes of AM-PM distortion is of significant theoretical and practical importance. It allows designers to build better amplifiers and target the main factors that contribute to nonlinearity. As a result designers can efficiently determine what part of the circuit should be altered without the need for hundreds of simulation runs.

1.3 Organization of this thesis

In this thesis, AM-PM conversion is first formally defined in Chapter 2 . In Chapter 3 the EKV model of the MOSFET, which is used throughout this thesis, is briefly presented. In Chapter 4 dominant mechanisms are explained using first principles that lead to simple expressions to capture the essence of the phenomenon, and is compared with simulation. Finally in Chapter 5 the analysis is compared with measured data to validate the theory.

CHAPTER 2

Definitions

AM-PM conversion is usually studied in the context of nonlinear large signal amplifiers, but AM-PM conversion can occur in linear as well as nonlinear systems. To define AM-PM conversion and AM-PM distortion carefully, we must first define amplitude and phase of narrowband signal.

2.1 Amplitude and Phase

We look at a general band-pass (or narrow band) modulated signal that has amplitude and angle modulation. The spectrum of a narrowband signal is shown in Figure 2.1.

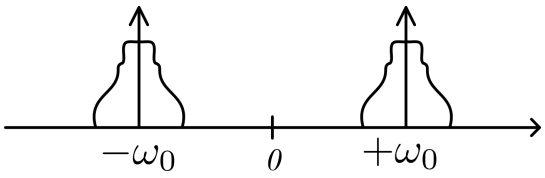


Figure 2.1: General narrow band signal in frequency domain

Figure 2.2 shows how the carrier is modulated by a signal. The carrier is represented by a phasor whose amplitude and phase are modulated[20].

Amplitude variation and phase variation are orthogonal, i.e. we can modulate amplitude without changing the phase and vice versa[1].

[1] Amplitude and phase define a rectilinear grid in the complex plane

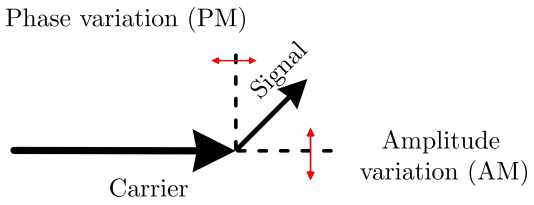


Figure 2.2: Modulated phasor

2.2 Amplitude and Phase modulation

AM is the oldest form of transmitting information on a carrier because of low cost receivers. AM signal has the form

$$f(t) = a(t)\cos(\omega_c t) \tag{2.1}$$

where

$$a(t) = 1 + A_{AM}\ s(t) > 0 \tag{2.2}$$

in order to be detected by a linear rectifier without distortion.

Fourier transform of $f(t)$, normalized to carrier for $s(t) = \cos(\omega_s t)$ is shown in Figure 2.3.

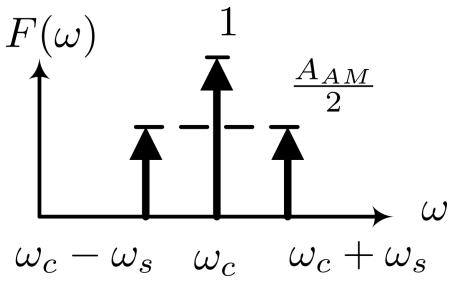


Figure 2.3: AM modulated signal in frequency domain, normalized to carrier

$a(t)$ is the envelope of the signal and $\omega_c t$ is its phase, un-modulated by ω_s.

In AM modulation, alteration takes place along radial axis. We also have the opportunity of modulating the angle (see Figure 2.2).

An angle modulated signal has the form

$$g(t) = \cos(\theta(t)) = \cos(\omega_c t + \phi(t)) = Re(e^{j\omega_c t}.e^{j\phi(t)}) \tag{2.3}$$

Instantaneous phase is $\omega_c t + \phi(t)$ and amplitude is equal to 1. The modulating signal, is proportional to $\phi(t)$.
If $\phi(t) = A_{PM} sin(\omega_s t)$ and $A_{PM} \ll 1$, $g(t)$ simplifies to

$$g(t) = \cos(\omega_c t) - A_{PM} \sin(\omega_s t) \sin(\omega_c t) \tag{2.4}$$

The spectrum of this PM modulated signal is shown in Figure 2.4.

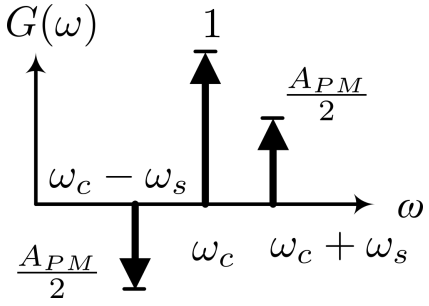


Figure 2.4: PM modulated signal in frequency domain, normalized to carrier

When we have AM and PM present simultaneously, the spectrum becomes asymmetric as shown in Figure 2.5.

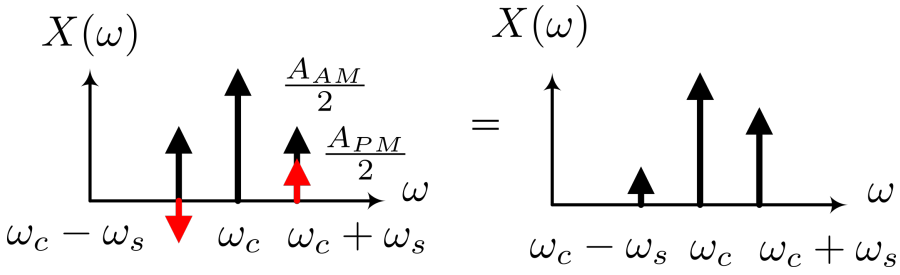


Figure 2.5: AM and PM presence simultaneously result in asymmetric spectrum

We may conclude that any spectrum asymmetric around carrier frequency contains PM. If a pure AM signal passes through the *linear* system that has

an asymmetric transfer function around ω_0, the outcome will be a signal with asymmetric spectrum which has phase variation (besides uniform phase variation of $\omega_c t$).

2.3 AM-AM and AM-PM in Transmitters

Consider a modulated signal $x(t) = a(t)\cos(\omega_c t + \phi(t))$ that passes through a memoryless nonlinear system, and assume the output can be written as:

$$y(t) = \sigma(a(t))\cos(\omega_c t + \phi(t)) \tag{2.5}$$

The function $\sigma(a)$ is the *AM-AM* characteristic of the system [21].

In a linear system, $\sigma(a) = ka$. In general, however, it is a nonlinear function. Since the phase of signal $y(t)$ is not affected by nonlinearity, the constellation points of $y(t)$ are shifted along the radius with respect to signal $x(t)$. Thus AM and PM component of modulated signal remain orthogonal.

In large signal power amplifiers and transmitters in general, amplitude variation causes phase variation as well. Assuming that output of system for input of $x(t) = a(t)\cos(\omega_c t + \phi(t))$, is equal to:

$$y(t) = a(t)\cos(\omega_c t + \phi(t) + \theta(a(t))) \tag{2.6}$$

The function $\theta(a)$ is the *AM-PM* characteristic of the system. Each constellation point is mapped to a point with the same amplitude but different phase. Therefore, the constellation is skewed rotationally. Simple rotation can be compensated by an anti-rotation $e^{-j\phi}$ but when each point is rotated by a different phase (according to its amplitude) the signal is distorted.

2.4 AM-PM conversion in asymmetrical linear system

We analyse what happens when AM signal passes through linear system whose transfer function is not symmetric around signal carrier frequency. Figure 2.6 shows a system block with input signal $V_i(j\omega_0)$ and output signal $V_o(j\omega_0)$.

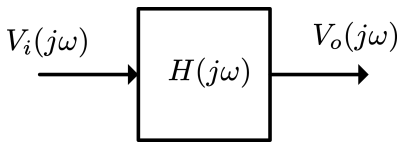


Figure 2.6: Linear system

We assume that input signal, $v_i(t)$, is AM modulated signal and can be written as:

$$v_i(t) = (1 + m\cos(\omega_s t))\cos(\omega_c t) \tag{2.7}$$

Since the system is linear, we can write output as the superposition of each different frequencies. Figure 2.7 shows the spectrum $v_i(f)$ and asymmetrical transfer function that signal is passing though.

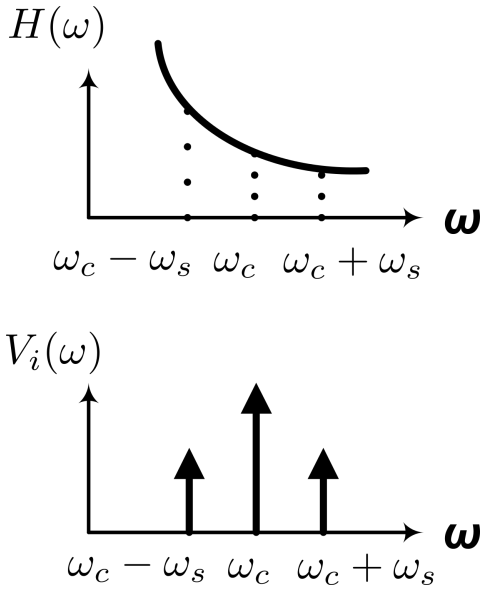


Figure 2.7: Asymmetric linear system

$$v_0(t) = |H(j\omega_0)|\cos(\omega_o t + \phi_0) + \frac{m}{2}|H(j(\omega_0+\omega_m))|\cos((\omega_0+\omega_m)t + \phi_{\omega_0+\omega_m}) + \frac{m}{2}|H(j(\omega_0-\omega_m))|\cos((\omega_0-\omega_m)t + \phi_{\omega_0-\omega_m}) \quad (2.8)$$

We define H_p and H_q as follows [22]:

$$H_p = \frac{1}{2}(H(\omega_0+\omega_m) + H(\omega_0-\omega_m)) \quad (2.9)$$

$$H_q = \frac{1}{2j}(H(\omega_0-\omega_m) - H(\omega_0+\omega_m)) \quad (2.10)$$

It easy to check that $H(\omega_0+\omega_m) = H_p - jH_q$ and $H(\omega_0-\omega_m) = H_p + jH_q$.

We define a_1, a_2, θ_1 and θ_2 so we can use them in final expression.

$$a_1^2 = |H_p|^2\cos^2\phi_p + |H_q|^2\cos^2\phi_q \quad (2.11)$$

$$a_2^2 = |H_p|^2\sin^2\phi_p + |H_q|^2\sin^2\phi_q \quad (2.12)$$

$$\theta_1 = \arctan\frac{|H_q|}{\cos\phi_q}\frac{|H_p|}{\cos\phi_p} \quad (2.13)$$

$$\theta_2 = \arctan\frac{|H_q|}{\sin\phi_q}\frac{|H_p|}{\sin\phi_p} \quad (2.14)$$

We replace these equations in equation (2.8) and then we can write:

$$v_0(t) = |H(j\omega_0)|\cos(\omega_o t + \phi_0) + m\sigma(t)\cos(\omega_o t + \gamma(t))) \quad (2.15)$$

where σ and γ are given by

$$\sigma^2(t) = a_1^2\cos^2(\omega_m t + \theta_1) + a_2^2\cos^2(\omega_m t + \theta_2) \quad (2.16)$$

$$\tan\gamma(t) = -\frac{a_2}{a_1}\frac{\cos(\omega_o t + \theta_2)}{\cos(\omega_o t + \theta_1)} \quad (2.17)$$

What is interesting in equation (2.15) is that, the output signal contains phase modulation, so AM-PM *conversion* happened, however the phase expression does not depend on amplitude. It appears as an off set and it is easy to correct it. The AM-PM distortion happens when output signal phase modulation is amplitude dependent and has a more serious effect on system performance.

CHAPTER 3

Overview of the MOSFET equivalent model

The EKV model [18, 19] is used throughout this thesis because it captures the behaviour of modern MOSFET perfectly.

We keep the model to the simplest form adequate for our analysis here. Figure 3.1 shows the cross section of an NMOS transistor.

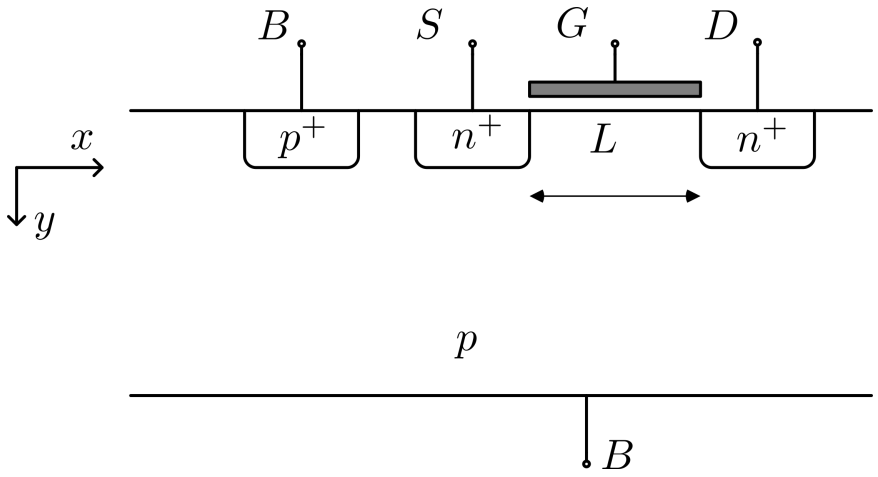


Figure 3.1: Cross section of NMOS transistor

Assuming that $V_S = V_D = 0$ and substrate is connected to ground, we have a two-terminal device which is a capacitor. As we raise V_G with respect to ground (substrate), negative charge is attracted to the surface between source and drain regions. The gate voltage at the onset of inversion, is defined as the zero bias *Threshold Voltage*, V_{t0}.

For a given gate voltage larger than threshold, raising V_S and V_D will cause mobile charge in inversion layer to diminish. Pinch-off voltage, V_P, is defined

as the equipotential channel voltage, $V_S = V_D = V_{ch}$, where inversion charge disappears. V_P depends only on gate voltage (V_G).

As we raise gate voltage beyond threshold voltage, a layer of electrons is induced at the surface of silicon, directly under the oxide. Inversion produces a continuous n-type region between source and drain and forms the conducting channel. The MOSFET in this state is said to be in *strong inversion.*

The channel conductivity in strong inversion can be modulated by increasing or decreasing gate, source, or drain voltage. For a given gate voltage, the inversion charge density, Q'_{inv}, is almost a linear function of the channel potential.

Figure 3.2 shows inversion charge density versus the channel potential for MOSFET in strong inversion.

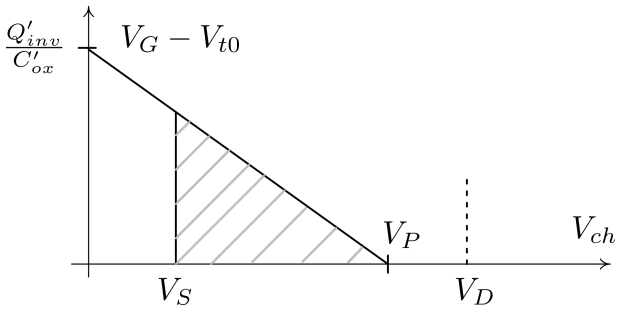


Figure 3.2: Inversion charge density versus the channel potential in strong inversion

In the Figure 3.2, drain voltage is assumed to be greater than Pinch-off voltage, and MOSFET is said to be in *saturation.* Drain current is proportional to shadowed area and constant of proportionality is equal to:

$$\beta = \mu_n C'_{ox} \frac{W}{L} \tag{3.1}$$

where μ_n is electron mobility and C'_{ox} is gate unit capacitance. W and L are aspect ratio of device. If drain voltage drops and becomes smaller than V_P, MOSFET is said be to in *triode.* For fixed gate and source voltages, as the drain voltage drops below V_P, the drain current drops as well.

Figure 3.3 shows the charge density versus channel voltage for MOSFET in triode region.

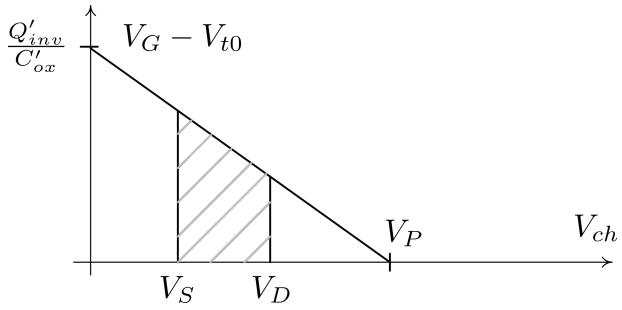


Figure 3.3: Inversion charge density versus the channel potential in strong inversion for MOSFET in triode

To find drain current, we find the area under the plot for V_{ch} from source voltage (V_S) to drain voltage (V_D), and multiply by β.

Drain current can be decomposed into a *forward current* I_F, which is integration under the curve of figure 3.3 from V_S to ∞, and *reverse current* I_R, which is integration from V_D to ∞. Therefore, we model drain current by two parallel current sources as shown in Figure 3.4.

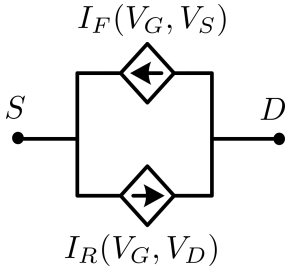


Figure 3.4: Decomposition of drain current into forward current and reverse current

The current sources are defined using the following equations:

$$I_F(t) = \begin{cases} \frac{\beta n}{2}(V_P - V_S)^2 & V_P > V_S \\ 0 & V_P < V_S \end{cases} \tag{3.2}$$

$$I_R(t) = \begin{cases} \frac{\beta n}{2}(V_P - V_D)^2 & V_P > V_D \\ 0 & V_P < V_D \end{cases} \tag{3.3}$$

Figure 3.5 shows $I_D - V_G$ characteristic for FET when $V_S = 0$. The characteristic is quadratic. It shows that when V_G is smaller than V_{t0} the current is zero. As V_G rises larger than V_{t0}, drain current increases.

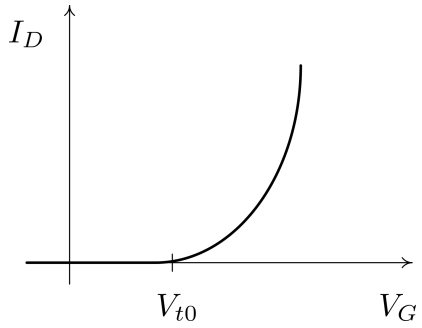


Figure 3.5: $I_D - V_G$ characteristic

Figure 3.6 shows $I_D - V_D$ characteristic for FET. It shows that, provided $V_D > V_P$, reverse current is zero and MOSFET is in saturation.
As drain voltage drops below V_P, reverse current becomes nonzero and overall drain current falls.

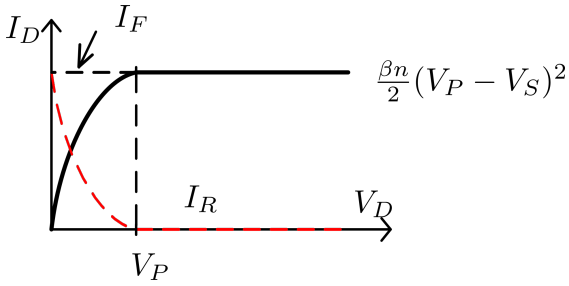


Figure 3.6: $I_D - V_D$ characteristic

CHAPTER 4

Dominant mechanisms of AM-PM distortion

In a linear system the *phase* of the output does not depend on the input *amplitude*. Also, static nonlinearity generates harmonics that are all in phase (or anti-phase). For AM-PM distortion to occur, there should exist nonlinearity *and* memory.

Figure 4.1 presents a generic FET power amplifier circuit used for our nonlinearity analysis.

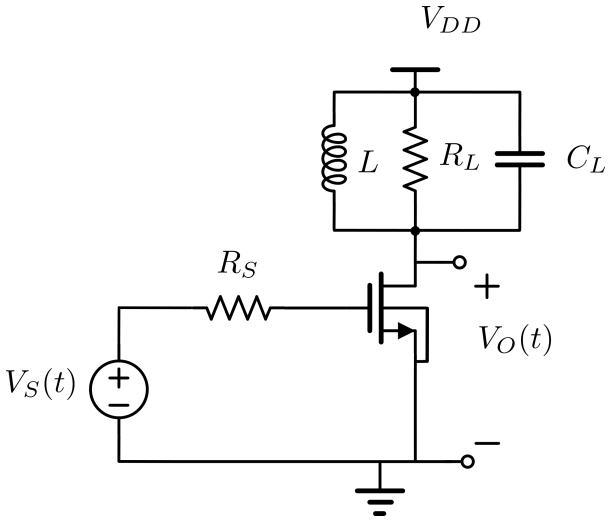


Figure 4.1: Generic linear PA circuit

The FET gate-source capacitance, C_{gs}, is nonlinear and varies with input voltage. This is a source of dynamic nonlinearity that will create AM-PM distortion. The capacitor between drain and source of FET, C_{gd}, can also generate AM-PM. The capacitor itself is nonlinear and varies with V_{GD}. However, its feedback effect across the main amplifier is the dominant mechanism of AM-PM distortion.

Device nonlinear i_D vs v_G and i_D vs v_D characteristics followed by frequency dependent load, like RC or RLC, is also a source of AM-PM distortion. It has been observed that increasing quality factor of RLC tuned tank, reduces the phase shift in drain current fundamental [23–25]. Some techniques have been proposed to reduce AM-PM in power amplifiers [11, 12, 26–28].

4.1 Nonlinear Gate Capacitance

Capacitor, C_{gs} is specified by its small-signal, or incremental, capacitance versus gate voltage with the substrate connected to ground. This is defined in terms of instantaneous charge Q and voltage V_G as follows:

$$C_{gs} = \frac{dQ}{dV_G}|_{V_G} \tag{4.1}$$

Figure 4.2 shows the typical curve for MOSFET gate capacitor at low frequencies and RF. C_{gs} depends on whether the semiconductor surface is in strong inversion, weak inversion, depletion or accumulation.

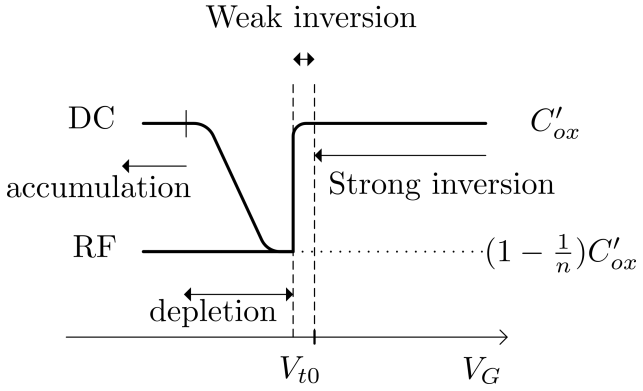


Figure 4.2: C_{gs} in different regions

We can model the MOS gate capacitor as a series combination of a fixed, voltage-independent gate oxide capacitor, C'_{ox}, and a voltage-dependent semiconductor capacitor, C'_d.

$$C'_g = \frac{C'_{ox} C'_d}{C'_{ox} + C'_d} \tag{4.2}$$

The total gate capacitance, C_g, is given by $C_g = WLC'_g$.

When the gate voltage falls below threshold voltage, there is a sharp drop in capacitance. It can be approximated with a step function (Fig. 4.3) [29].

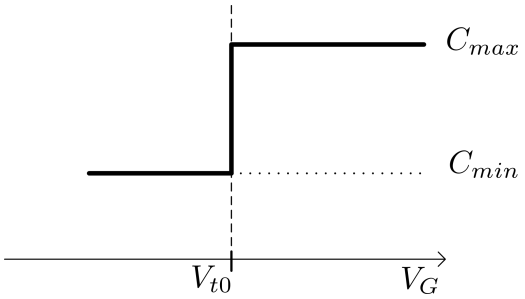
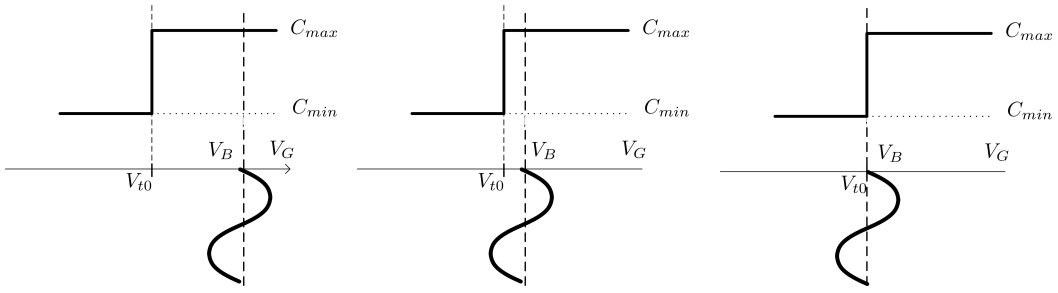


Figure 4.3: Approximate C_{gs} vs. V_G

When driven by large signals, the capacitance nonlinearity depends on where we bias the transistor. For example, for an FET amplifier biased in class A, the FET never turns off and the gate voltage always remains above threshold, hence the gate capacitor remains fixed. For class B, we assume that the gate bias is equal to the threshold voltage. If the gate voltage oscillates sinusoidally around threshold, the effective capacitance will *not* change with amplitude and there will not be a significant AM-AM or AM-PM distortion. For class AB, the FET is biased at a voltage larger than threshold, $V_B > V_{t0}$. When amplitude rises above $V_B - V_{t0}$, the small signal capacitance falls as a step function, and AM-PM distortion can occur. As amplitude rises, the effective capacitance drops, because for larger amount of cycle, the instantaneous capacitance is smaller (see Fig. 4.4).



(a) Class A (b) Class AB (c) Class B

Figure 4.4: Effect of biasing in different classes

To quantify the effect of this nonlinear capacitor, we ignore the feedback capacitor, C_{gd} and focus on the input side of amplifier shown below.

Figure 4.5 shows the input of FET power amplifier including nonlinear gate capacitor. C_{gd} is neglected for now.

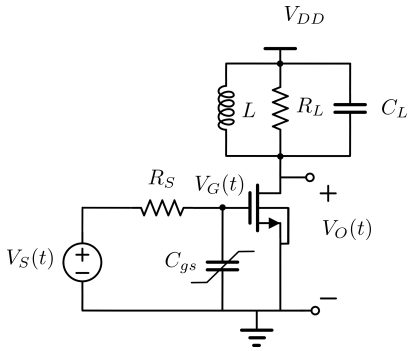


Figure 4.5: FET power amplifier with nonlinear input capacitor

Table 4.1: Parameters used in simulation of C_{gs} effect

V_{t0}	160 mV
V_B	300 mV
f_0	2 GHz
R_S	50 Ω 25 Ω
C_{min}	300 fF
C_{max}	720 fF

Table 4.1 gives the parameters used is simulation and analysis.

Input loop consists of an RC circuit with a nonlinear capacitor. We apply a tone to this RC network and find the amplitude dependent phase shift in the sinewave. Figure 4.6 shows the nonlinear RC network without the FET.

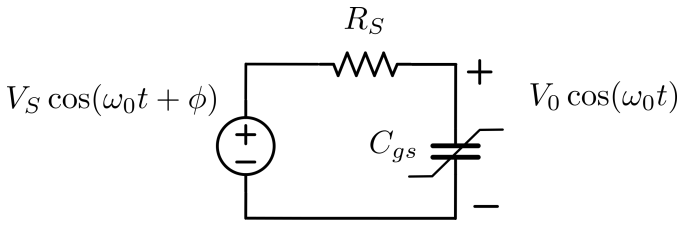


Figure 4.6: Nonlinear RC network

With the voltage $V_0\cos(\omega_0 t)$ across the capacitor, the small signal capacitance of C_{gs} varies between maximum and minimum values. The capacitance can be represented by a Fourier series:

$$C_{gs}(t) = C_{gs0} + C_{gs1}\cos(\omega_0 t) + C_{gs2}\cos(2\omega_0 t) + \dots \tag{4.3}$$

Harmonics will appear in the capacitor current. We assume voltage across capacitor is also a sinewave with a amplitude dependent phase shift $= -\phi$, relative to driving signal.

In a linear circuit, ϕ would be fixed and its value depends on the elements and frequency. But in the presence of nonlinearity, the phase is a function of amplitude as well.

Kirchhoff's laws applied to RC circuit dictate that:

$$V_s\cos(\omega_0 t+\phi) = Ri_C(t) + V_0\cos(\omega_0 t) \tag{4.4}$$

Using equation (4.1), capacitor current can be written as:

$$i_C(t) = C_{gs}(V_G)\frac{d(V_G)}{dt} = C_{gs}(t)\frac{d\left(V_0\cos(\omega_0 t)\right)}{dt} = -C_{gs}(t)V_0\sin(\omega_0 t) \tag{4.5}$$

We substitute time-varying capacitor by equation (4.3) and simplify the result to find V_0 and ϕ as follows:

$$V_0 = V_s\frac{1}{\sqrt{1+\left(R_s\omega_0(C_{gs0}-\frac{1}{2}C_{gs2})\right)^2}} \tag{4.6}$$

and

$$\phi = \arctan\left(R_s\omega_0(C_{gs0} - \frac{1}{2}C_{gs2})\right) \tag{4.7}$$

Since C_{gs0} and C_{gs2} are themselves amplitude dependent, ϕ will be a function of sinewave amplitude and causes AM-PM distortion. As we change the sinewave amplitude, the phase shift varies. To complete the expression for AM-PM distortion we need to find the first and third terms in Fourier series of $C_{gs}(t)$.

In Figure 4.7, we have applied a sine-wave gate voltage to a C_{gs} nonlinearity that is approximated by a step function and shown that instantaneous small signal capacitance will be a pulse train with maximum of C_{max} and minimum of C_{min}.

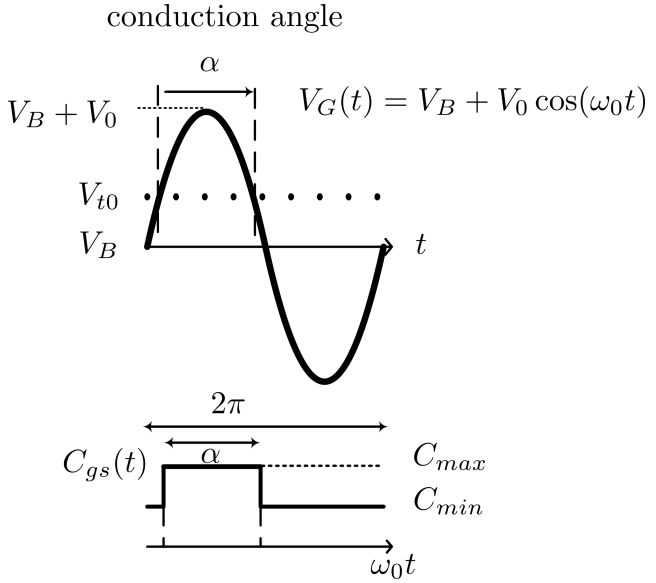


Figure 4.7: Gate signal controlling the capacitance and instantaneous capacitance versus time

The duty cycle, α, is equal to:

$$\frac{\alpha}{2} = \arccos(\frac{V_{t0} - V_B}{V_0}) \tag{4.8}$$

From the definition of Fourier series, we find first and third Fourier coefficients.

$$C_{gs0} = C_{min} + \frac{\alpha}{2\pi}(C_{max} - C_{min}) \tag{4.9}$$

and

$$C_{gs2} = \frac{C_{max} - C_{min}}{2\pi} \sin(\alpha) = \frac{C_{max} - C_{min}}{2\pi} \sqrt{1 - \left(\frac{V_{t0} - V_B}{V0}\right)^2} \tag{4.10}$$

We substitute (4.9) and (4.10) into (4.7) to find amplitude dependent phase shift, ϕ.

The result is phase shift as a function of gate voltage amplitude, V_0. Because $R_S\omega_0 C_{gs} \ll 1$, $V_s \simeq V_0$ (see (4.6)) so replacing V_0 with V_s in (4.7).

$$\phi = \arctan \left\{ R_s\omega_0 \left(C_{min} + \frac{C_{max} - C_{min}}{2\pi} (2 \arccos(\frac{V_{t0} - V_B}{V_s}) - \frac{1}{2}\sqrt{1 - (\frac{V_{t0} - V_B}{V_s})^2}) \right) \right\} 0 \tag{4.11}$$

To verify the derived expression, we plot the (4.11) and compare it with simulation. Figure 4.8 and Figure 4.9 compare the expression with simulation for $R_S = 50\Omega$ and $R_S = 25\Omega$.

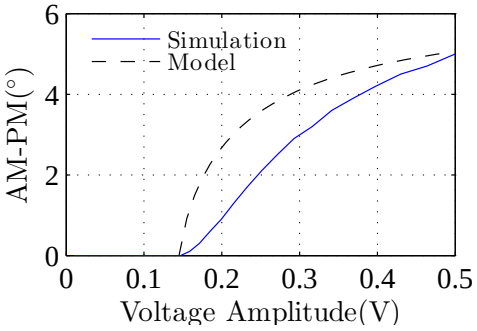


Figure 4.8: AM-PM distortion when $R_S = 50\Omega$

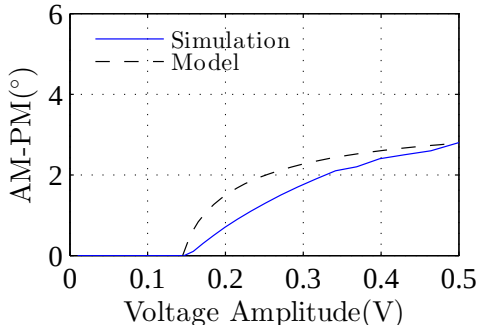


Figure 4.9: AM-PM distortion when $R_S = 25\Omega$

The important result is that the AM-PM distortion depends highly on source resistance as shown in Figure 4.10.

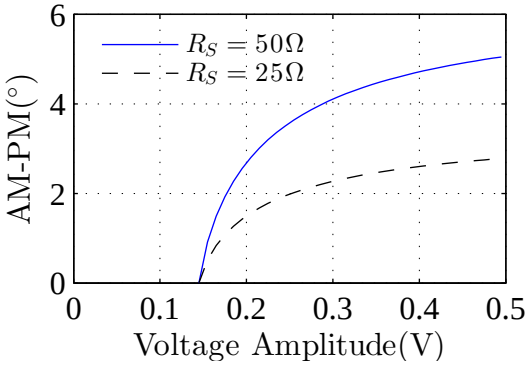


Figure 4.10: Effect of source resistance on AM-PM distortion (in the model)

For voltage amplitudes below $V_B - V_{t0}$, there is no phase shift because C_{gs} remains at C_{max}. Phase shift appears only when $V_s > (V_B - V_{t0})$.

4.2 Feedback capacitor

The feedback capacitor between drain and gate, C_{gd}, can be modelled as equivalent capacitor connected to gate (Miller effect). The value of this effective capacitor depends on voltage gain. Thus non-constant AM-AM characteristic results in a varactor effect causing AM-PM distortion.

Figure 4.11 shows FET PA with feedback capacitor C_{gd}, and ignoring C_{gs} and C_{db}.

By analysing this circuit, we derive small signal transfer function, $H_{in}(j\omega)$, from input voltage source, V_s, to input of FET, V_G.

$$H_{in} \equiv \frac{V_G}{V_S}(j\omega) = \frac{1}{1 + j\omega C_{gd} R_S R_L g_m} \tag{4.12}$$

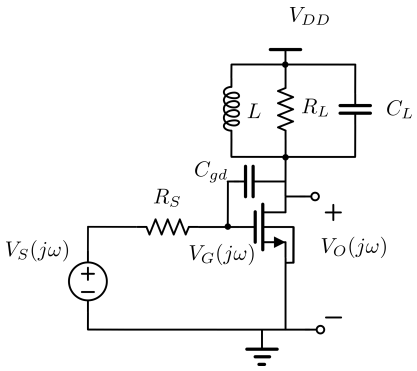


Figure 4.11: Simple power amplifier including C_{gd} capacitor

Table 4.2: Parameters used in simulation of C_{gd} effect

V_{t0}	160 mV
V_{DD}	1 V
V_B	500 mV
f_0	2 GHz
R_S	50 Ω 25 Ω
R_L	10 Ω
C_{gd}	250 fF
β	2.77 $\frac{A}{V^2}$

In a linear circuit, there is a fixed attenuation and phase shift from input voltage source to gate of FET, however in large signal FET amplifier, transconductance varies with input amplitude and the phase of $H(j\omega)$ changes.

An important step in analysing the nonlinearity of amplifier is to model the transconductance variation with amplitude. Table 4.2 gives the parameters used in analysis and simulation.

The FET is bias at class AB with a dc gate voltage of $V_B = 0.5V$. The small signal transconductance is equal to:

$$g_m = \frac{2I_D}{V_B - V_{t0}} = 0.65mS \tag{4.13}$$

and small signal voltage gain across FET, $\frac{V_o}{V_g}$, is 6.5. As we raise the input voltage, the output voltage increases but it is limited ultimately by voltage supply. In the simplest form, we can say that the output amplitude rises with input amplitude until it reaches V_{DD}, then remains fixed at V_{DD} as the input amplitude increases.

The small signal voltage gain is $A_0 = 6.5$, so when output reaches $V_{DD} = 1V$, the critical input amplitude is equal to:

$$V_C \equiv \frac{V_{DD}}{A_0} = 0.15V \tag{4.14}$$

Suppose we define large signal transconductance as follows:

$$r = \frac{V_G}{V_C} \tag{4.15}$$

$$G_m = \begin{cases} g_m & r < 1 \\ \dfrac{g_m}{r} & r > 1 \end{cases} \tag{4.16}$$

This is a piecewise linear model. The parameter r, captures the drop in transconductance and voltage gain. Figure 4.12 shows a comparison between modelled large signal transconductance and simulated large-signal transconductance. Harmonic balance simulation is performed to plot $G_m = \mid \frac{I_{D1}}{V_{G1}} \mid$.

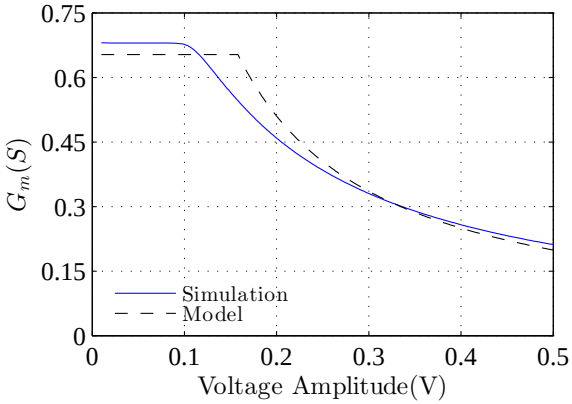


Figure 4.12: Large-signal transconductance

We replace the g_m in (4.12), by the expression for G_m in (4.16). As the input amplitude rises, the large signal transconductance drops and phase of transfer function increases. This phase shift occurs at the input loop. As the voltage gain drops, the effective capacitance seen between the gate terminal and ground becomes smaller. This is an amplitude-dependent capacitor at the input of the FET.

We substitute (4.16) into (4.12) and compare the result with simulation. Harmonic balance simulation is performed to plot $\angle I_{D1}(V_{G1})$.

We have used two different source resistors to verify our model. Figures 4.13 and 4.14 show the comparison for $R_S = 50\Omega$ and $R_S = 25\Omega$.

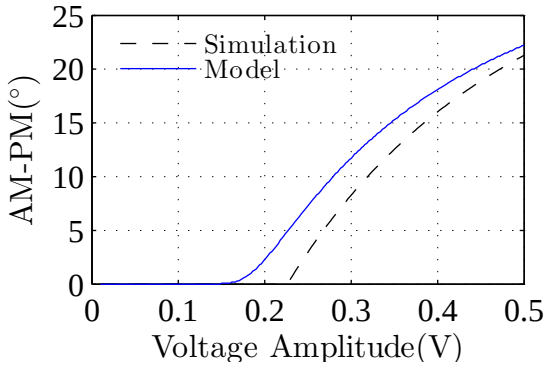


Figure 4.13: AM-PM distortion resulting from feedback capacitor, $Rs = 50\Omega$

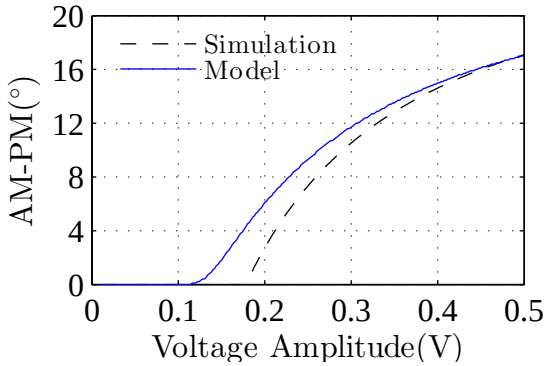


Figure 4.14: AM-PM distortion resulting from feedback capacitor, $Rs = 25\Omega$

4.3 Load impedance effect on drain current

Figure 4.15 shows FET power amplifier with RC load. Harmonic traps are used to remove second and third harmonics.

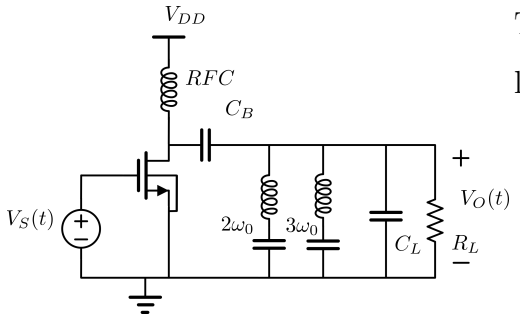


Figure 4.15: FET power amplifier

Table 4.3: Parameters used in simulation of load effect on drain current

V_{t0}	160 mV
V_{DD}	1 V
V_B	500 mV
f_0	2 GHz
R_L	10 Ω
β	2.77 $\frac{A}{V^2}$

Now we will ignore the FET capacitors and analyse the effect of a mis-tuned load. As long as the FET is in saturation region, the drain current consists of only the forward current, I_F, and its fundamental-frequency component is in-phase with input voltage. Drain current goes through the capacitive load and drain voltage will be shifted with respect to drain current.

The important point is that when the FET is pushed into triode region, the reverse current, I_R, becomes non-zero and is subtracted from forward current. Since reverse current depends on drain and gate voltages, there is a phase difference between forward current and reverse current and the total drain current will no longer be be in phase with the input voltage.

We focus on the fundamental components of forward current and reverse current, because harmonics are suppressed by the resonate traps.

Figure 4.16 shows the phasor addition of the fundamental components of the forward current and reverse current.

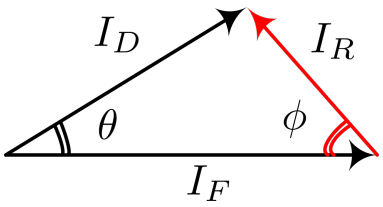


Figure 4.16: Fundamental component of drain current decomposed into forward and reverse currents

To obtain an expression for I_D, we approximate the phase shift, ϕ, in I_R, then solve for θ in Figure 4.16.

By the definition (3.3), $i_R(t)$ can be written as:

$$i_R(t) = \frac{1}{2}\beta(v_G(t) - V_{t0} - v_D(t))^2 \tag{4.17}$$

If α is the phase of the drain load impedance at the fundamental frequency and A_v is the large signal voltage gain from gate to drain, $A_v = \dfrac{V_{D1}}{V_{G1}}$, then $v_G(t)$ and $v_D(t)$ can be written as:

$$v_G(t) = V_B + V_0\cos(\omega_0 t) \tag{4.18}$$

$$v_D(t) = V_{DD} + V_0 A_v\cos(\omega_0 t + \theta + \alpha) \tag{4.19}$$

where V_B is gate voltage bias.

We can find the phase shift in reverse current by finding the time instant when the drain voltage goes through a minimum. To find drain voltage minimum we solve for $\dfrac{dv_D(t)}{dt} = 0$.

$$-V_0\omega_0\sin(\omega_0 t) + V_0 A_v\omega_0\sin(\omega_0 t + \theta + \alpha) = 0 \tag{4.20}$$

$$\sin(\omega_0 t) - A_v\sin(\omega_0 t + \theta + \alpha) = 0 \tag{4.21}$$

The root of equation above gives us phase shift in reverse current. Therefore we replace $\omega_0 t$ by $-\phi$ and simplify equation to derive ϕ.

$$\sin(-\phi) - A_v\sin(-\phi + \theta + \alpha) = 0 \tag{4.22}$$

$$-\sin\phi - A_v\left(-\sin\phi\cos(\theta+\alpha)+\cos\phi\sin(\theta+\alpha)\right)=0 \tag{4.23}$$

$$(1-A_v\cos(\theta+\alpha))\tan\phi = -A_v\sin(\theta+\alpha) \tag{4.24}$$

$$\phi = \arctan\left(\frac{\sin(\theta+\alpha)}{\frac{1}{-A_v}+\cos(\theta+\alpha)}\right) \tag{4.25}$$

We can write another equation by graphical analysis on Figure 4.16, as follows:

$$I_D\cos(\theta) + I_D\sin(\theta)\frac{1}{\tan(-\phi)} = I_F \tag{4.26}$$

We solve (4.26) and (4.25) simultaneously. We replace the ratio of I_F to I_R by parameter r, and derive equation (4.28).

$$r = \frac{I_F}{I_D} \tag{4.27}$$

$$r = \cos(\theta) - \frac{\sin(\theta)}{\sin(\theta+\alpha)}\left(\frac{1}{-A_v}+\cos(\theta+\alpha)\right) \tag{4.28}$$

Parameter r (same as in (4.15)) models the drop in transconductance and large signal voltage gain. Therefore we can write large signal voltage gain, A_v, when $r > 1$ as:

$$A_v = \frac{A_0}{r} = \frac{V_{DD}}{V_0} \tag{4.29}$$

where A_0 is the small signal gain.

We substitute (4.29) in (4.28) and re-write (4.29) as follows:

$$r\left(\sin(\theta+\alpha)-\frac{1}{A_0}\sin(\theta)\right) = \cos(\theta)\sin(\theta+\alpha)-\sin(\theta)\cos(\theta+\alpha) = \sin(\alpha) \tag{4.30}$$

We expand $\sin(\theta+\alpha)$ to sum of $\sin\theta$ and $\sin\alpha$.

$$r\left(\sin(\theta)\cos(\alpha)-\frac{1}{A_0}\sin(\theta)+\sin(\alpha)\cos(\theta)\right) = \sin(\alpha) \tag{4.31}$$

We define two parameters, B and α', to simplify (4.31).

$$\alpha' = \arctan\left(\frac{\sin(\alpha)}{-\frac{1}{A_0}+\cos(\alpha)}\right) \tag{4.32}$$

$$B = \sqrt{1 + \frac{1}{A_0}\left(\frac{1}{A_0} + 2\cos(\alpha)\right)} \tag{4.33}$$

With these definitions, we can write;

$$B\cos(\alpha') = -\frac{1}{A_0} + \cos(\alpha) \tag{4.34}$$

$$B\sin(\alpha') = \sin(\alpha) \tag{4.35}$$

We substitute (4.32) and (4.33) into (4.31) to derive following equation for θ:

$$\theta = -\alpha' + \arcsin\left(\frac{1}{r}\frac{1}{B}\sin(\alpha)\right) \tag{4.36}$$

As shown in Figure 4.16, θ is phase shift in drain current, I_D, and its variation with input amplitude is AM-PM distortion. We can replace r by $A_0\dfrac{V_0}{V_{DD}}$ to find θ as a function of voltage amplitude, V_0. Figures 4.17 and 4.18 compare the expression (4.36) with simulation for two different loads. Figure 4.17 shows the comparison for the case that $Q = 0.5$, and Figure 4.18 shows the result for $Q = 1$.

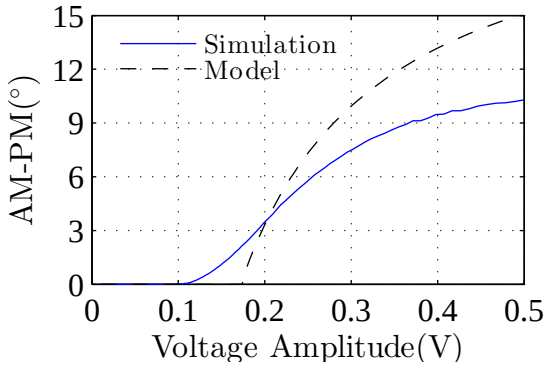


Figure 4.17: AM-PM distortion for Q=0.5

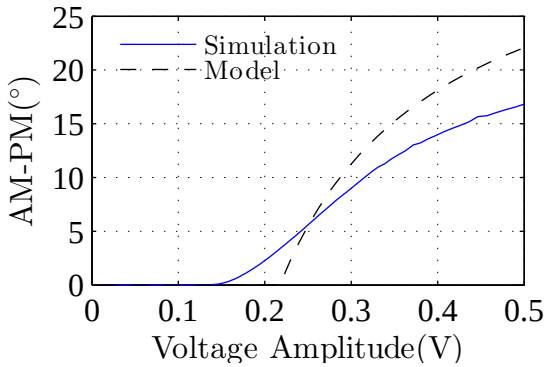


Figure 4.18: AM-PM distortion for Q=1

The abrupt behaviour comes from the assumption that the FET suddenly enters into triode region. If small signal gain, A_0, is high enough $B \simeq 1$, and $\alpha' \simeq \alpha$.

As we increase input voltage amplitude, the FET is pushed deeper into triode region (momentarily) and we observe more phase shift in fundamental component of drain current.

The reason for difference between model and simulation is that for simplicity we assumed when fundamental component of drain current reaches an amplitude $\frac{V_{DD}}{|Z(\omega_0)|}$, it remains fixed and does not increase.

4.4 Harmonics effect on drain current

Consider the linear class AB FET power amplifier shown in Figure 4.19, ignoring all device capacitors. The amplifier's load is a tank tuned to frequency of operation, ω_0, to suppress the harmonics. When tank Q is not high enough, harmonics will cause an amplitude-dependent phase shift.

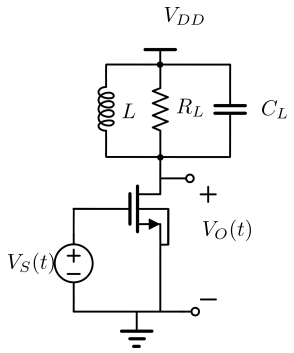


Figure 4.19: FET power amplifier with RLC load tuned to frequency of operation

Table 4.4: Parameters used in simulation of harmonics effect

V_{t0}	160 mV
V_{DD}	1 V
V_B	500 mV
f_0	2 GHz
Q	5 10
R_L	10 Ω
β	2.77 $\frac{A}{V^2}$

All harmonics of I_F are in phase with fundamental because FET nonlinear characteristics is memory-less, however we have frequency dependent load that causes harmonics to be shifted differently, according to their frequencies.

When the FET is in saturation region, $i_D(t) = i_F(t)$, $i_R(t) = 0$ and there is no phase shift in the current at the fundamental frequency since it only depends on gate voltage. However, when the FET is driven into triode, i_R appears. Since its amplitude at the fundamental frequency depends on drain voltage — not only the fundamental component of drain voltage but on all harmonics — it is not in phase with forward current and creates a phase shift at the fundamental frequency of drain current. The second (and higher) harmonics of drain current pass through the tank and they experience different phase shift compared to fundamental component. The fundamental component flows through R_L and higher harmonics through C_L.

Figure 4.20 shows distorted drain current and drain voltage. Most of the cycle, $v_D(t) > V_P$ and FET works in saturation or cut-off region. For a short period of time $v_D(t) \simeq 0$ and $i_D(t)$ is forced to drop, although the FET is in strong inversion (see Fig 3.6). When FET is pushed deeply in triode region (momentarily), a

dent appears in drain current and results in another negative peak in the current waveform (the other negative peak happens momentarily when the FET is in cut off region).

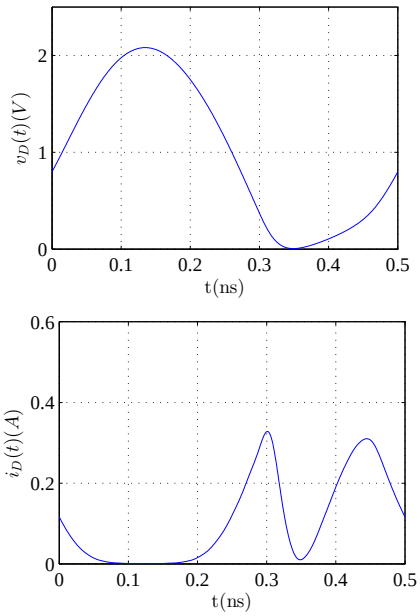


Figure 4.20: Distorted drain current and drain voltage for circuit in Figure 4.19

Table 4.5: Parameters used in simulation of distorted voltage and current

V_{t0}	160 mV
V_{DD}	1 V
V_B	500 mV
f_0	2 GHz
V_0	400 mV
R_L	10 Ω
Q	5
β	2.77 $\frac{A}{V^2}$

In the presence of tuned tank, the drain voltage remains approximately sinusoidal. The tank causes the drain voltage to shift with respect to drain current because the harmonics flow through a capacitor and experience a phase lag. At downward excursions of drain voltage, the FET is asymmetrically pushed into triode region (drain voltage is shifted with respect to drain current) and causes an asymmetric drop in drain current.

We decompose the drain current into forward current and reverse current. Forward current depends only on the gate voltage, however reverse current depends on drain voltage as well.

Reverse current is zero when FET in in saturation, it only appears when FET is pushed into triode region.

Figure 4.21 shows distorted current decomposed into forward and reverse current.

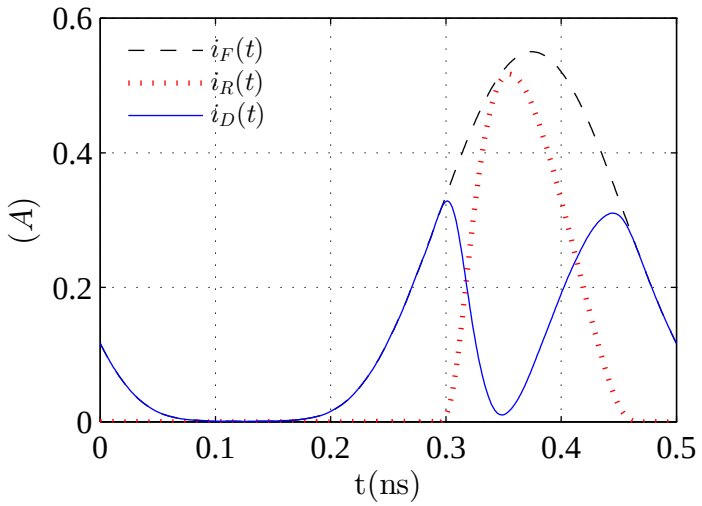


Figure 4.21: Drain current decomposition into forward current and reverse current

The feedback loop below shows the explained mechanism in which drain voltage changes the fundamental component of drain current through reverse current.

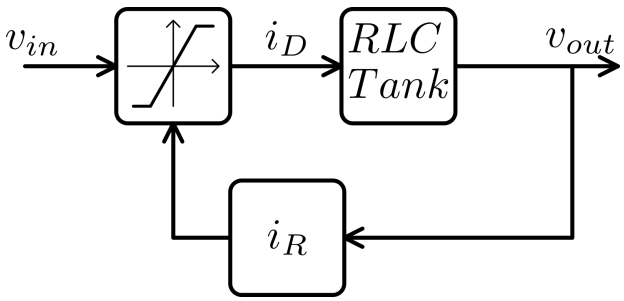


Figure 4.22: Feedback loop creates AM-PM

The forward current can be written as:

$$i_F(t) = \frac{1}{2}\beta(V_B - V_{t0} + V_0\cos(\omega_0 t))^2 = I_{F0} + I_{F1}\cos(\omega_0 t) + I_{F2}\cos(2\omega_0 t) \quad (4.37)$$

where

$$I_{F1} = \beta V_0 (V_B - V_{t0}) \tag{4.38}$$

$$I_{F2} = \frac{1}{4}\beta (V_0)^2 \tag{4.39}$$

By inspection of Figure 4.21 we propose to model the reverse current with an impulse train.

A key point is that this impulse train is shifted in time with respect to forward current and causes asymmetry in the drain current. Figure 4.23 shows the reverse current approximation with impulse. ϕ measures the phase shift in reverse current, and we will use it later to find phase shift in total current.

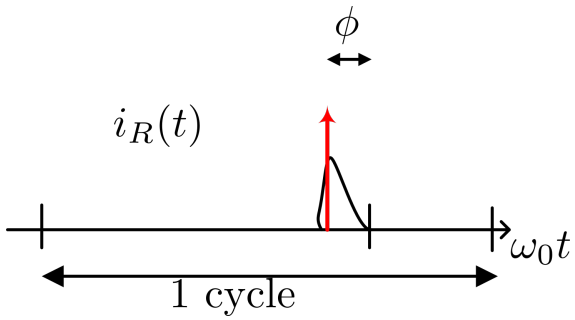


Figure 4.23: Impulse approximation of reverse current

The Fourier series for an impulse train offset from $t = 0$ by $\frac{\phi}{\omega_0}$ can be written as:

$$i_R(t) = I_{R0} + I_{R1}\cos(\omega_0 t + \phi) + I_{R2}\cos(2\omega_0 t + 2\phi) + ... \tag{4.40}$$

where $I_{R0} = I_{R1} = I_{R2} = \ldots$.

Assuming a sinusoidal voltage at the gate of FET, $v_G(t) = V_G \cos\omega_0 t$, maximum value that fundamental component of drain current, I_{D1}, reaches can be written as:

$$I_{D1}(max) = \frac{V_{DD}}{R_L} = g_m V_C = V_G \frac{g_m}{r} \tag{4.41}$$

where g_m is the small-signal FET transconductance, V_C is defined as:

$$V_C = \frac{V_{DD}}{A_0} \tag{4.42}$$

and r is defined in (4.15).

Basically, when input voltage amplitude reaches V_C, voltage gain drops because output voltage has reached the maximum level and beyond that the output amplitude remains at the same level, however the input amplitude is rising. As a result, large signal voltage gain drops with $\frac{1}{V_G}$ and parameter r is defined to capture the gain drop. Also the fundamental component of forward current is simply the amplitude V_G multiplied by small signal transconductance:

$$I_{F1} = g_m V_G \tag{4.43}$$

Figure 4.24 shows addition of fundamental component of forward current, I_{F1}, and fundamental component of reverse current, I_{R1}, as phasors.

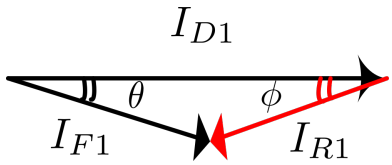


Figure 4.24: Fundamental component of drain current decomposed into forward and reverse with relative phase difference

In a tuned circuit, the harmonics are suppressed to some extent and the phase shift in reverse current and ultimately in drain current will be small. We can use the following approximations:

$$\tan(\phi) \simeq \sin(\phi) \simeq \phi \tag{4.44}$$

$$\tan(\theta) \simeq \sin(\theta) \simeq \theta \tag{4.45}$$

Thus fundamental component of drain current can be written as:

$$I_{D1} = I_{F1} - I_{R1} \tag{4.46}$$

because $\cos\theta \simeq \cos\phi \simeq 1$.

Using equations (4.41), (4.43) and (4.46) we can write:

$$I_{R1} = I_{F1}(1 - \frac{1}{r}) \tag{4.47}$$

Using (4.47), we can use phasors to find the drain current phase shift, θ, in terms of reverse current phase, ϕ.

$$\theta = \arcsin\left(\frac{I_{R1}\sin(\phi)}{I_{D1}}\right) = \arcsin\left((r-1)\phi\right) = (r-1)\phi \tag{4.48}$$

In order to solve for θ in terms of r, we need another equation to eliminate ϕ from equation above.

The angle, ϕ, is the phase shift in reverse current and we can approximate it by finding the minimum of drain voltage.

Drain voltage up to second harmonic can be written as:

$$v_D(t) = V_{DD} - I_{D1}R_L\cos(\omega t + \theta) - I_{D2}\frac{R_L}{\frac{3}{2}Q}\cos(2\omega_0 t + \beta + \alpha) \tag{4.49}$$

where Q is quality factor of the tank, β is phase of second harmonic of drain current, α is phase of tank impedance at the second harmonic equal to:

$$\alpha \equiv \angle Z(2j\omega_0) = -\arctan(\frac{3}{2}Q) \tag{4.50}$$

and magnitude of tank impedance at the second harmonic is:

$$|Z(2j\omega_0)| = \frac{R_L}{(\frac{3}{2}Q)} \tag{4.51}$$

To find minimum of drain voltage, we need to find magnitude and phase of second harmonic of drain current.

Very important point is that, second harmonic of current, itself shifts significantly respect to forward current because of its own reverse component. The reason is that second harmonic of reverse current becomes larger than second harmonic of forward current quickly as FET goes into triode. Figure 4.25 shows

second harmonic of drain current, decomposed into forward and reverse components.

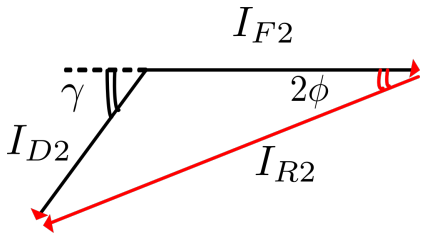


Figure 4.25: Second harmonic of drain current decomposed into forward and reverse with relative phase difference

We find minimum of drain voltage by solving $\frac{dv_D(t)}{dt} = 0$.

$$\frac{dv_D(t)}{dt} = 0 \tag{4.52}$$

$$I_{D1}\sin(\theta - \phi) + \frac{4}{3}\frac{I_{D2}}{Q}\sin(-2\phi + \pi + \gamma + \alpha) = 0 \tag{4.53}$$

$$I_{D1}\sin(\theta - \phi) + \frac{4}{3}\frac{I_{D2}}{Q}\sin(2\phi - \gamma + \alpha) = 0 \tag{4.54}$$

Since α is approximately $-\frac{\pi}{2}$ when $Q > 5$ (see (4.50)), we can further simplify the above equation as follows:

$$I_{D1}\sin(\theta - \phi) + \frac{4}{3}\frac{I_{D2}}{Q}\cos(2\phi - \gamma) = 0 \tag{4.55}$$

Since ϕ and γ have the same sign, the difference will be an even smaller angle and we can use approximation that $\cos(2\phi - \gamma) \simeq 1$ (see Figure 4.25).
With these simplifications, we derive:

$$\theta = \phi - \arcsin\frac{4}{3Q}\frac{I_{D2}}{I_{D1}} = \phi - \frac{4}{3Q}\frac{I_{D2}}{I_{D1}} \tag{4.56}$$

The second harmonic of drain current, I_{D2}, can be approximated as follows:

$$I_{D2} = I_{R2} - I_{F2} \tag{4.57}$$

because we assume that $\cos 2\phi = \cos \gamma = 1$. Also we know that

$$I_{D1} = I_{F1}\frac{1}{r} \tag{4.58}$$

and

$$I_{R2} = I_{R1} = I_{F1}(1 - \frac{1}{r}) \tag{4.59}$$

We substitute equations (4.57), (4.58) and (4.59) into equation (4.56), and derive:

$$\theta = \phi - \frac{4}{3Q}r(1 - \frac{1}{r} - \frac{I_{F2}}{I_{F1}}) \tag{4.60}$$

From (4.38) and (4.39), the ratio $\frac{I_{F2}}{I_{F1}}$, is equal to:

$$\frac{I_{F2}}{I_{F1}} = \frac{1}{4}\frac{rV_x}{V_B - V_{t0}} \tag{4.61}$$

By replacing equation (4.61) into (4.60), we can write θ in terms of r:

$$\theta = -\frac{4}{3Q}r\frac{1 - \frac{1}{r} - \frac{r}{4}\frac{V_x}{V_B - V_{t0}}}{1 + \frac{1}{r-1}} \tag{4.62}$$

Equation (4.62), is AM-PM distortion as a function of r and is valid when $Q > 5$. Figures 4.26 and 4.27 compare the above expression with simulation for two different cases.

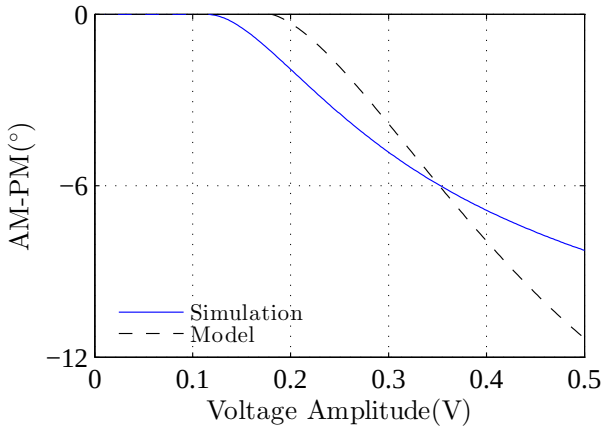


Figure 4.26: AM-PM distortion when Q=5

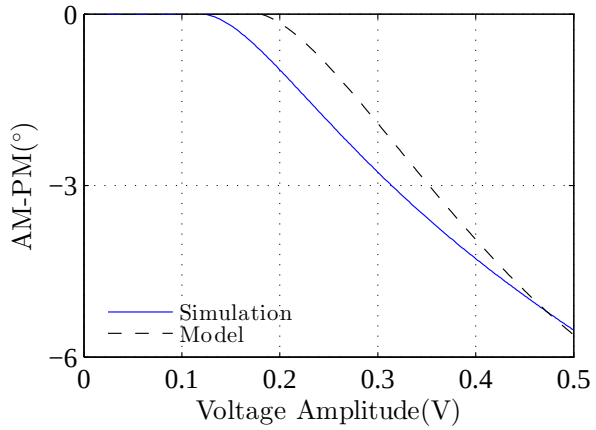


Figure 4.27: AM-PM distortion when Q=10

As can be seen in Figure 4.28, tank with higher quality factor reduces the phase shift, since it suppresses harmonics more.

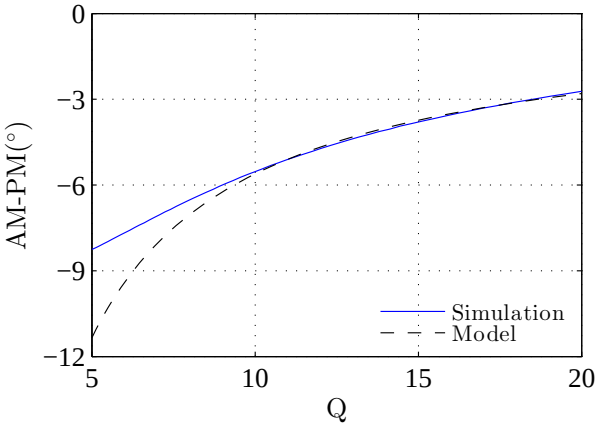


Figure 4.28: Sweeping Q when input amplitude=500 mV

For smaller values of Q, expression departs from simulation results because we assumed harmonics flow entirely through the capacitor.

CHAPTER 5

Verification with Measurement

in order to verify our theory with measured AM-PM data, we have done an extensive literature review to find measurement data on AM-PM distortion. Among all the publications with reported measured AM-PM, we only could find two examples that provide sufficient details about the circuit so we can apply our theory to their measurement to explain how AM-PM occurs. There were some parameters that we needed to deduce to re-produce their results.

5.1 15-W 900MHz PA

The measured AM-AM and AM-PM characteristics are reported for a 15-W 900-MHz GaN HEMT PA prototype [1].

We apply our theory to explain their AM-PM data. We need to design input and output matching networks to re-construct the measured data, since details of matching networks are not provided and we need them to analyse the amplifier.

Voltage supply of the power amplifier is $V_{DD} = 28V$ and the maximum output power is $P_{max} = 41dBm$. As a starting point we calculate the transferred resistance that is seen at the drain of device as follows:

$$R = \frac{V_{DD}^2}{2P_{out}} \tag{5.1}$$

We connect this resistor to drain of device and using s-parameters of the FET [30] provided by manufacturer, we calculate input impedance. We terminate the input side of device with a matched impedance and calculate the output

impedance. We can add a proper reactance to resistive load that we started with, and do the same calculations again to find output and input terminations.

Figure 5.1 and Figure 5.2 show the layout and simplified PA circuit.

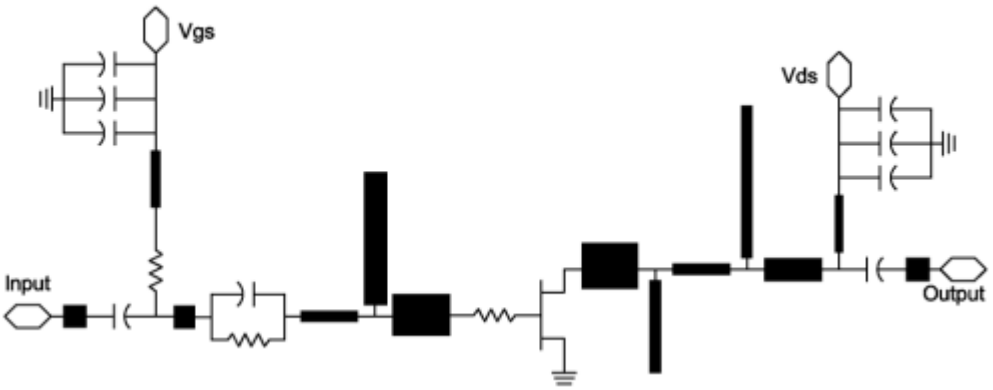


Figure 5.1: Layout of power amplifier (from [1])

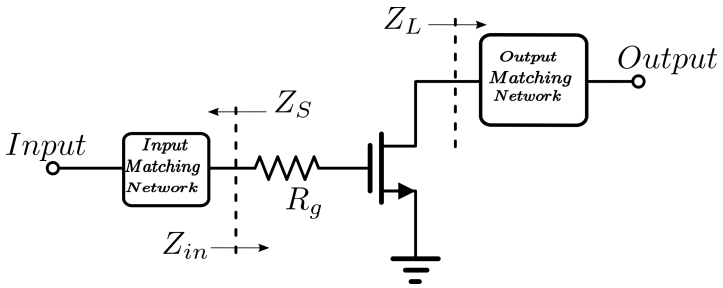


Figure 5.2: Simplified PA circuit

We start the analysis by looking at C_{gs} and C_{gd} as dominant sources of AM-PM distortion. Figure 5.3 shows the input of power amplifier including nonlinear capacitor, C_{gs}, and effective capacitance, $C_{gd}(1-A_v)$. C_{gs} is a nonlinear capacitor that varies with input voltage. The gain of the amplifier changes with input amplitude, so does the effective capacitance $C_{gd}(1-A_v)$.

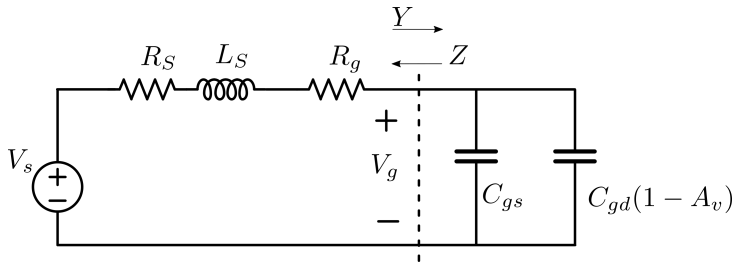


Figure 5.3: Input loop of power amplifier circuit

$$H_{in}(j\omega) \equiv \frac{V_g}{V_s}(j\omega) = \frac{1}{1 + ZY} \tag{5.2}$$

where $Z = Z_s + R_g$ (see Figures 5.2 and 5.3), and Y is gate input admittance of FET that is approximately capacitive and can be written as:

$$Y = j\omega(C_{gs} + C_{gd}(1 - A_v)) \tag{5.3}$$

In small signal operation there is a fixed phase shift from input voltage source to the gate of FET, however as input amplitude rises, the admittance Y varies and phase shift changes. In addition to AM-PM distortion generated at the input side of transistor, the load with nonzero reactance will generate AM-PM distortion when device is pushed into triode region.

We take a few points from figure shown in [1] to plot measured AM-PM distortion shown in Figure 5.4.

Phase of $H(j\omega)$ as function of input amplitude gives the AM-PM distortion generated by capacitors. This distortion appears in V_{gs} and it is plotted in Figure 5.4. The phase shift in V_{gs} is the dominant mechanism of AM-PM distortion of the amplifier.

As input amplitude rises and the amplifier output saturates, the voltage gain drops and the transistor enters into triode. The non-zero reactance at the load causes additional phase shift at higher power levels. Using (4.36) and AM-AM

curve for the amplifier, we calculate the additional phase shift and add it to phase shift in V_{gs}. The result is plotted in Figure 5.4.

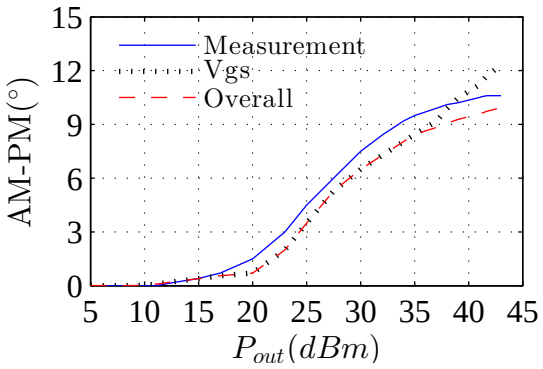


Figure 5.4: Comparison between measured AM-PM and analytic model

Table 5.1: Parameters used in analysis of the 15-W PA

V_{t0}	-3.5 V
V_{DD}	28 V
V_B^*	-3 V
R_L^*	15 Ω
$\angle Z_L^*$	-15 °
C_{min}	6 pF
C_{max}	10 pF
C_{gd}	0.345 pF
Z^*	15 + 12j Ω
A_0^*	18

(∗) These values are not provided in the paper or datasheet and we deduced them.

The V_{gs} curve in Figure 5.4 shows the phase shift in V_{gs} caused by C_{gs} and C_{gd}. The overall curve shows the phase shift from the input to the output. The difference between overall curve and V_{gs} curve is additional phase shift because of mis-tuned load.

Dominant mechanisms of AM-PM distortion are input varactor effect, C_{gs}, and feedback capacitor, C_{gd}. The amplifier for a power range that it is measured in [1], remains out of saturation and effect of mis-tuned load is small. As the FET is pushed deeper in triode region, mis-tuned load generates more phase shift. In the next section we discuss an example that FET gain drops by $15dB$ and mis-tuned load dominates.

To compare effect of two capacitors, we fix C_{gs} in our model to only look at C_{gd}. Also, we fix the voltage gain in our model to only consider input varactor

effect. We plotted these two cases in Figure 5.5.

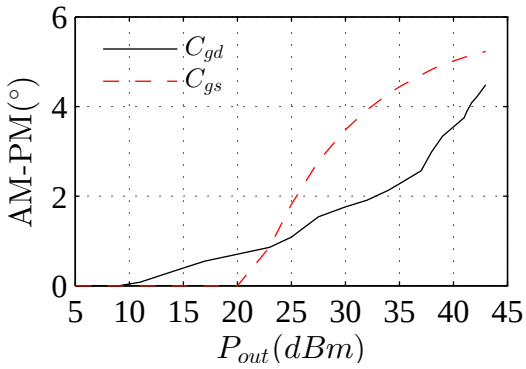


Figure 5.5: Comparison between AM-PM generated by input varactor and feedback capacitor (using the model)

The analytic comparison above, shows that effect of two capacitors are comparable. The effect of C_{gd} depends on gain variation. As voltage gain drops, the effective capacitance goes down. When $(1 - A_v)C_{gd} < C_{gs}$ the drop in voltage gain does not generate significant phase shift. Phase shift because of C_{gs} appears when $V_G > (V_B - V_{t0})$. Since the AM-PM distortion begin to affect the amplifier linearity below the P_{1dB}, the backing-off from peak power is not enough [9, 10].

5.2 900MHz HEMT PA

Measured AM-PM distortion characteristic is reported for a power amplifier using GaN HEMT device [2]. The power amplifier is not tuned at the drain to the input frequency but it has an RC load.

Figure 5.6 shows the simplified PA circuit presented in the paper.

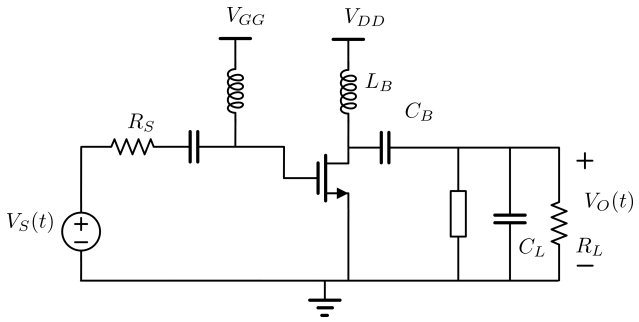


Figure 5.6: PA circuit with RC load (from [2])

Figures 5.7 and 5.8 are measured AM-AM and AM-PM reported in [2].

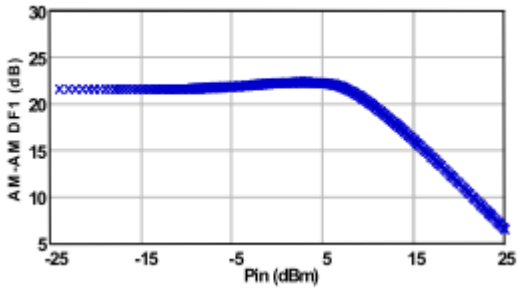


Figure 5.7: Measured AM-AM characteristic of amplifier (from [2])

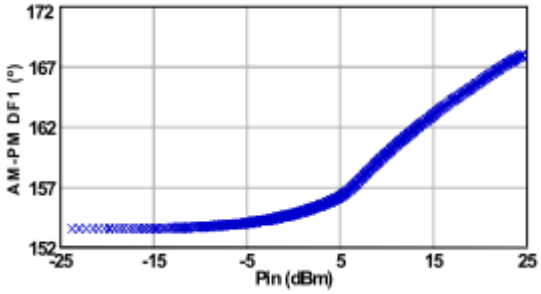


Figure 5.8: Measured AM-PM characteristic of amplifier (from [2])

Device equivalent model including device capacitors, small signal transconductance and channel length modulation are measured and reported [31]. Load impedance at the drain of intrinsic device, at fundamental frequency is $Z_L(j\omega_0) = 13.2 - 5.2j\ \Omega$.

There will be significant phase shift because of the mis-tuned load. The phase of load impedance at the fundamental frequency of $900MHz$ is $\alpha = -21.5°$ and from AM-AM characteristic plot we observe $15dB$ gain drop.

We use (4.36) to predict phase shift resulting from mis-tuned load. We recall that equation here:

$$\theta = -\alpha' + \arcsin(\frac{1}{r}\frac{1}{B}\sin(\alpha)) \tag{5.4}$$

The voltage gain across device can be calculated as $A_v = g_m|Z_L(j\omega_0)| = 15.6dB$ and we can calculate $\alpha' = -18.4°$ and $B = 1.15$ from (4.32) and (4.33). The parameter r corresponds to drop in gain, and in this case varies from 1 to 5.5.

Figure 5.9 shows equation (5.4) plotted versus input power.

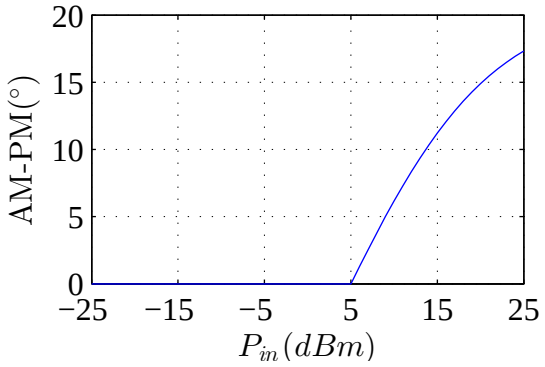


Figure 5.9: AM-PM distortion resulting from mis-tuned load using (5.4)

Input varactor, C_{gs}, and feedback capacitor, C_{gd}, can generate phase shift. Similar to the analysis presented in previous section, we write small signal transfer function from input voltage source to input of intrinsic device in order to approximate phase shift at the input side of transistor (see (5.2)).

Figure 5.10 shows plotted expression for phase shift due to input varactor and feedback capacitor. We have used (5.2) and parameters in Figure 5.2.

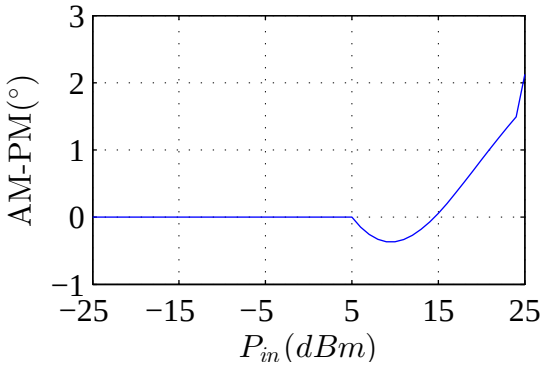


Figure 5.10: AM-PM distortion resulting from feedback capacitor and input varactor

We add two phase expressions to get an estimate for overall phase shift. Figure 5.11 shows the addition of nonlinearity sources and compares it with measured AM-PM.

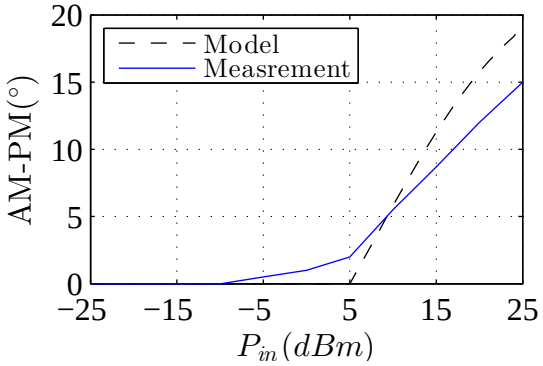


Figure 5.11: Comparison between measured AM-PM and the model

Table 5.2: Parameters used in analysis of the 900MHz HEMT PA

g_m	0.33 mS
Z_L	16.3 $\angle -25°$ Ω
V_{t0}	-4.3 V
V_{DD}	6 V
V_B	0 V
C_{min}	1.5 pF
C_{max}	3.5 pF
C_{gd}	0.4 pF
Z_s	40 $\angle -19°$ Ω

The model is close enough to measurement and it proves that dominant machanism of AM-PM distortion in the amplifier is mis-tuned load. The amplifier gain drops by 15 dB and the FET enters deep triode region momentarily at high input

power levels. As the FET is pushed deeper in triode region, the reverse current increases and phase of total current shifts.

5.3 90nm CMOS PA

We have simulated a simple power amplifier using 90nm CMOS as shown in Figure 5.12, similar to circuit we analysed in Chapter 4.

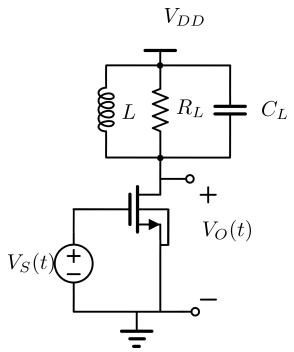


Figure 5.12: Simple power amplifier circuit

Table 5.3: Parameters used in analysis of the 90nm CMOS power amplifier

g_m	0.47 mS
R_L	20 Ω
V_{t0}	0.2 V
V_{DD}	1 V
Q	5 10
V_B	0.5 V
W/L	2400u/0.4u

The value of load resistor is set to $R = 20\Omega$. C_L and L are tuned to $100MHz$ for convenience. The FET size is designed to give a voltage gain of $A_v = 17.5dB$.

Since a voltage source is connected directly to the gate of FET, the varactor effect is removed. The frequency is chosen low to ignore C_{gd} feedback.

Load of FET is tuned using a RLC tank. We change the tank quality factor to study the effect of harmonics on generated AM-PM distortion.

We have applied the analysis presented in Chapter 4 to our circuit and compared the simulation result with analytic expression for two different loads.

Recall (4.62):

$$\theta = -\frac{4}{3Q} r \frac{1 - \frac{1}{r} - \frac{r}{4}\frac{V_C}{V_B - V_{t0}}}{1 + \frac{1}{r-1}} \tag{5.5}$$

where $V_B = 0.5V$ and $V_{to} = 200mV$.

V_C is defined as the input voltage amplitude that output voltage amplitude reaches the maximum and can be calculated using voltage gain across FET, $V_C = \frac{V_{DD}}{A_0}$. The parameter r, corresponds to drop in voltage gain (see (4.15)). Figure 5.13, compares the simulated phase shift with model for RLC tank with quality factor of 5, and Figure 5.14 shows the results for quality factor of 10.

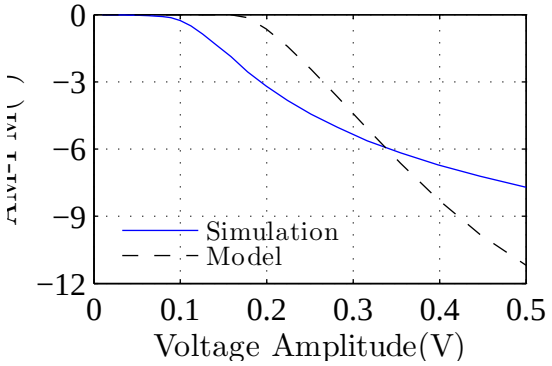


Figure 5.13: AM-PM distortion when Q=5

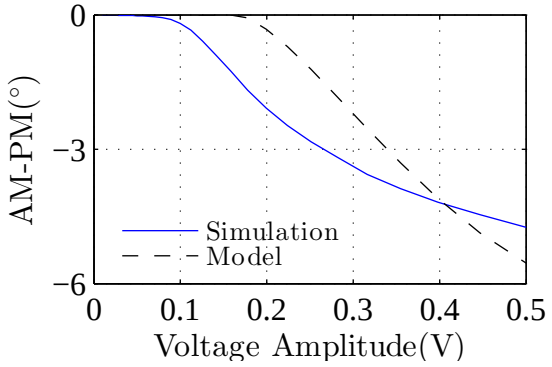


Figure 5.14: AM-PM distortion when Q=10

Tank quality factor has a significant effect on phase distortion. As we increase

Q, the phase distortion decreases.

The effect of Q on phase distortion is also observed in [23] and our model can explain their observation.

CHAPTER 6

Conclusion

This thesis provided a simple model for AM-PM distortion in large signal amplifiers. The dominant mechanisms are described qualitatively and simple expressions are derived. High complexity of previous models make it difficult to understand and calculate the phase distortion, however the simplicity of this model, offers insight into the AM-PM distortion phenomenon. Once the dominant source of distortion is identified, it can be fixed easily instead of doing hundreds of simulation runs.

The EKV model proved to be very useful in the modeling of the nonlinearity effects. The introduction of forward current and reverse current in EKV model, helped us separate different effects that happen in an amplifier.

Device capacitors are found to be source of AM-PM distortion. The AM-PM distortion due to capacitors depends on source resistor and voltage gain variation. The phase shift due to capacitors might begin to affect the performance below the P_{1dB} and backing off the amplifier is *not* enough to satisfy linearity requirements of modern modulation schemes.

Load impedance when output matching is out of resonance generates AM-PM distortion as the amplifier saturates. It is explained that this distortion mechanism depends strongly on output matching and the non-zero output reactance. If this mechanism dominates the amplifier nonlinearity, either output matching should be improved or the amplifier should back off from peak power.

In addition, if the amplifier is tuned but the quality factor is low, harmonics

generate AM-PM distortion as the voltage gain drops. Although the mechanism is very complicated, our theory explained it very effectively and the end result shows that it depends mostly on two parameters, tank quality factor and gain drop. To eliminate phase distortion caused by low Q tank, the harmonics should be removed at the drain of transistor, not at the antenna. Besides improving the tank Q, backing off the amplifier lowers the distortion as well.

The model proved to be successful in explaining measured AM-PM distortion of different power amplifiers in the literature.

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