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# **Patterned, Low-Temperature Growth of Transition Metal Dichalcogenides for Low Resistance Raised Contacts**

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## **ABSTRACT**

**Transition metal dichalcogenide (TMD) monolayers are promising channel materials for next-generation electronic devices. A challenge is the high contact resistance between monolayer TMDs and metal contacts, especially for holes. In this regard, raised source/drain contacts are promising. However, the direct, patterned growth of raised contacts at CMOS-compatible temperatures remains largely unresolved. We present plasma-free selenization and sulfurization of metal-oxides at substrate temperatures down to 400 °C, compatible with back-end-of-line (BEOL) thermal budgets. To achieve growth at such temperatures, gas-phase chalcogen precursors are first thermally activated at 950 °C. Films grown on single-crystal monolayer TMDs exhibit high crystal quality as confirmed by transmission electron microscopy. Raised contacts on WSe<sub>2</sub> monolayers fabricated using this approach yield a low hole contact resistance of 0.3 kΩ·μm after chemical doping. This process is shown to be applicable to growing various TMDs, including WS<sub>2</sub>, MoSe<sub>2</sub>, MoS<sub>2</sub>, PtSe<sub>2</sub>, and NbS<sub>2</sub>.**

Transition-metal dichalcogenide (TMD) monolayers have gained widespread interest for their potential applications for the next-generation electronics.<sup>1–3</sup> TMD-based transistors have been reported to display high carrier mobility, large on-off ratios, and low subthreshold swings.<sup>4–6</sup> Their intrinsic physical properties such as dangling-bond-free surfaces and atomically-thin nature facilitate scaling of the transistors to sub-5nm channel lengths.<sup>7</sup> Moreover, many of the TMDs have high effective mass and low in-plane dielectric constants, which make it feasible to have low source-to-drain tunneling leakage currents, suitable for low power applications.<sup>8–10</sup>

A key challenge impeding the adoption of monolayer TMD transistors is high contact resistance, primarily due to the high Schottky barrier formed at the metal–monolayer TMD interface, especially for the *p*-type devices.<sup>11</sup> To resolve this issue, numerous techniques have been developed, including the use of special transfer techniques to create ideal van der Waals contacts,<sup>5,12,13</sup> aggressive dopants for highly doped regions near the contacts,<sup>14</sup> and semimetal interlayers for more favorable metal-semiconductor band alignment.<sup>15</sup> Still, many of these techniques require process steps such as special transfer procedures difficult to scale, high-temperature treatments beyond the back-end-of-line (BEOL) thermal budget of 400 °C, or the use of materials that are incompatible with conventional complementary metal-oxide-semiconductor (CMOS) processes.

Meanwhile, studies indicate that achieving low contact resistance may be more readily achievable for thicker, few-layered TMD flakes compared to their monolayer counterparts<sup>16</sup> as thicker TMDs have smaller bandgaps and more favorable band alignment between the conduction/valence band edges and metal work functions.<sup>17</sup> This understanding has motivated the exploration of raised source/drain contacts to enhance carrier injection from metal contacts into multilayered TMDs.<sup>18</sup> This method, a well-established silicon-based technique for minimizing parasitic contact resistance,<sup>19</sup> allows for improved current flow while preserving a monolayer TMD as the channel layer, which is essential for ultra-scaled transistors.

Consequently, this approach has been adopted in various TMD-based field-effect transistors (FETs) with multilayer TMD beneath the metal source/drain contacts, demonstrating reduced contact resistance, particularly when the channel is defined by sequential layer-by-layer oxidation etching.<sup>18</sup> However, selective growth of multilayer TMDs on monolayer TMDs is highly desirable, as etching processes can introduce unintended damage to the TMD channel.

While the synthesis of high-quality TMDs often requires temperatures exceeding the BEOL thermal budget,<sup>20,21</sup> several innovative methods have demonstrated large-scale growth with high carrier mobilities at BEOL compatible temperatures.<sup>22–24</sup> Moreover, area selectivity was also shown to be feasible with trench shaped SiO<sub>2</sub> on HfO<sub>2</sub>.<sup>25</sup> However, gas backflow techniques are inherently unstable and extremely difficult to control with precision, leading to difficulties in scale to larger productions. Plasma-assisted processes can limit TMD quality and risk causing plasma-induced damage to the film. Growth method using monolayer graphene as a template carries a risk of introducing residual carbon at the critical interface. Employing SiO<sub>2</sub> trench-shaped masks to grow single crystalline TMD, while effective, inherently constrains design flexibility due to the necessity of the size and the distances required between the trenches.

Here, we present low-temperature (down to 400 °C) patterned growth of TMDs which can be made to be located between the monolayer channel and the metal contacts by single step lithography. As an exemplary application, the process is used as raised source/drain contacts for monolayer WSe<sub>2</sub>. The same process could be applied to fabricate a wider range of raised source/drain contacts for different TMDs. The process involves selective selenization of pre-patterned transition metal oxide films beneath metal electrodes using our low-temperature (LT) growth method. A hot zone, kept at 950 °C, was implemented to ‘activate’ the chalcogen species before reaching the substrate, enabling WO<sub>x</sub> to be converted to WSe<sub>2</sub> at relatively low substrate temperatures near 400 °C. This LT growth method was demonstrated for various TMDs and resulted in high-quality films as evidenced by Raman. Highly crystalline WSe<sub>2</sub> was verified

using high resolution transmission electron microscopy (HRTEM) imaging with templated growth of the converted films on top of single-crystalline exfoliated monolayer WSe<sub>2</sub>. Raised source/drain contacts were created using the LT method through the lateral conversion<sup>26</sup> of WO<sub>x</sub> evaporated in between exfoliated WSe<sub>2</sub> and rhodium source/drain metal. The contact resistance of this raised source/drain device structure was extracted using transfer length method (TLM), which was calculated to be 0.3 k $\Omega$ · $\mu$ m upon doping with AuCl<sub>3</sub>. Moreover, we successfully fabricated a top-gate monolayer WSe<sub>2</sub> FET with raised source/drain displaying a switching behavior and an on/off current ratio greater than 10<sup>6</sup>.

## Results and Discussions

The schematic in Figure 1a illustrates the overall setup of our LT growth process, which uses a two-zone furnace to selenize an evaporated transition metal or transition metal oxides without requiring the substrate to be at a high temperature. In the two-zone furnace, the gasses first flow from upstream, crossing the hot zone at 950 °C (activation T) before reaching the substrate placed downstream in the cooler zone at 400 °C (substrate T). The hot zone promotes the source chalcogen gas to have higher kinetic energy and reactivity, while the substrate, whose surface is covered with thin films of transition metal or transition metal oxides, is kept at a cooler, BEOL-compatible temperature.

We hypothesized that the hot zone would lead to dissociation of the gas-phase selenium precursor (H<sub>2</sub>Se), and that the resulting reactive species would react with the metal oxide in the cooler part of the reactor (400 °C). To understand if TMD growth in this setup is thermodynamically feasible, we calculated the equilibrium gas composition as a function of temperature for a H<sub>2</sub>Se: Ar mixture (5:95, 1 bar) as shown in Figure 1b.

We anticipate that shorter-chain allotropes of selenium, such as Se<sub>2</sub>, will be predominantly found at temperatures exceeding 800 °C compared to lower temperatures with H<sub>2</sub>Se fully dissociating at the temperatures shown in the figure. Prior studies have established

that shorter-chain sulfur allotropes, including  $S_2$  and  $S_3$ , exhibit significantly higher reactivity than their longer, cyclic counterparts, such as  $S_8$ .<sup>27</sup> Consequently, we expect selenium allotropes to demonstrate a similar trend, given that selenium and sulfur participate in many analogous chemical reactions<sup>28,29</sup> and share comparable molecular structures, namely, the prevalence of shorter chains for  $Se_{2-3}$  and cyclic structures for  $Se_{5-8}$  as some of their representative molecular structures shown in Figure 1c.<sup>30-32</sup> Therefore, we expect a large formation of shorter-chain selenium and sulfur allotropes in the upstream region of annealing furnace, which will play a critical role in converting the film on the substrate maintained at lower temperatures downstream, owing to their enhanced reactivity.

As  $H_2Se$  is likely to be fully dissociated into elemental selenium allotropes and  $H_2$  gas above room temperature at thermal equilibrium, we also conducted experiments in which evaporated elemental selenium powder was transported via forming gas (95:5  $N_2/H_2$ ) through a hot zone held at 950 °C prior to reaching the substrate, yielding comparable results. These findings support the hypothesis that shorter-chain Se allotropes, generated in the hot zone, are the critical species enabling selenization, as evidenced by the successful conversion of the film even in the absence of  $H_2Se$ .

Figure 1d highlights the method's capability for precise, selective-area growth. A 3 nm  $WO_x$  film was first pre-patterned into arbitrary sizes and shapes on a Si/SiO<sub>2</sub> substrate using standard photolithography and lift-off (left). This patterned film was then successfully selenized to  $WSe_2$  (right), using vaporized Se (from a powder source near the hot zone) while flowing 1000 sccm of forming gas. This technique enables the direct fabrication of  $WSe_2$  structures, precisely confined to desired, pre-patterned locations on a chip.

The crucial effect of the high temperature ‘activation’ zone is shown in Figure 1e. The Raman spectrum of the 2H  $WSe_2$  peak has a significantly higher intensity for a sample grown with the activation zone at 950 °C (red), compared to a sample grown without the activation zone (gray). A temperature-dependent growth study, shown in Figure S1, was conducted using

H<sub>2</sub>Se as the chalcogen precursor for conversion of WO<sub>x</sub> to WSe<sub>2</sub>. WSe<sub>2</sub> films grown with a substrate T of 400 °C and an activation T of 950 °C and a using H<sub>2</sub>Se (flow rate of 10 sccm) show markedly higher Raman peak intensity compared to films grown without the hot zone being placed at a different temperature to the substrate, even when the substrate T is substantially higher, up to 750 °C.

Notably, we observe that WSe<sub>2</sub> of different phases can be grown by simply controlling the temperature of the substrate. Figure S2 shows Raman spectra of WSe<sub>2</sub> films converted from 3 nm WO<sub>x</sub> films, with substrate temperature of 300 °C (gray), by flowing 20 sccm H<sub>2</sub>Se in 490 sccm Ar using the setup shown in Figure S3. Raman Spectra indicate that when the substrate is placed at 300 °C, peaks associated with the 1T' WSe<sub>2</sub> phase emerge in 221.8, 239.4, and 260.3 cm<sup>-1</sup>.<sup>33</sup> This contrasts with the spectrum obtained from the film converted at 400 °C shown in Figure 1d, where 2H WSe<sub>2</sub> peaks are observed.<sup>34</sup> Upon annealing at 400 °C in nitrogen for 5 min, the film grown at 300 °C undergoes a phase change, with the Raman spectrum (red) showing only peaks of the 2H WSe<sub>2</sub> phase (Figure S2). This reinforces our supposition that the film grown at 300 °C is likely from the 1T' WSe<sub>2</sub> metallic phase, since 1T' is known to be metastable and can be converted to 2H by annealing at higher temperatures.<sup>33</sup> The Raman signal intensity from the annealed sample is approximately tenfold lower than that of the directly grown sample (Figure 1e), indicating that the growth method utilizing activated Se species is more effective for producing higher quality films.

To further understand the effects of the substrate temperatures on the film growth quality, we conducted growth using elemental selenium as the chalcogen precursor, varying the substrate temperature in each case. As shown in Figure 2a, by holding the activation temperature at 950 °C and varying the substrate temperature from 140 °C to 410 °C, the Raman signal becomes sharp when the substrate reaches 410 °C, with a peak between 250 cm<sup>-1</sup> and 260 cm<sup>-1</sup> with smaller full width half maximum (FWHM) of the peak from 11.47 cm<sup>-1</sup> for WSe<sub>2</sub> grown at 340 °C down to 6.72 cm<sup>-1</sup> for WSe<sub>2</sub> grown at 410 °C. As narrower Raman peaks refer

to crystals of higher crystal quality with less disorder such as defects,<sup>35,36</sup> these results strengthen our understanding that our LT method enables growth of WSe<sub>2</sub> at lower substrate temperatures even down to 400 °C.

Figure 2b displays the X-ray diffraction (XRD) pattern of the selenized 20 nm WO<sub>x</sub> film, showing prominent peaks corresponding to the (002), (006), and (008) planes<sup>37</sup>. These peaks indicate that the WSe<sub>2</sub> film is oriented with its c-axis perpendicular to the substrate surface, forming a well-aligned, layer-by-layer structure rather than random orientations.

Figure 2c, d, and e show scanning electron microscope (SEM) images along with energy-dispersive X-ray spectroscopy (EDS) maps for W M $\alpha$  and Se L $\alpha$  signals, respectively. The Se signal appears uniformly distributed across the SEM image, indicating that the WSe<sub>2</sub> conversion occurred uniformly across the entire area rather than at isolated sites. This observation is further supported by Figure S4, which presents SEM and EDS images from four additional regions on the same chip, all exhibiting consistent Se signal uniformity. A representative EDS spectrum map is shown in Figure S5 that displays the peaks integrated for the mapping. This suggests that the conversion process is widespread and not confined to specific regions of a chip.

To further improve the crystallinity of our WSe<sub>2</sub> films, we converted WO<sub>x</sub> deposited on single-crystalline, exfoliated monolayer WSe<sub>2</sub> flakes to promote growth from templated alignment. To investigate the crystallinity of our films, WSe<sub>2</sub> was grown on Si<sub>3</sub>N<sub>4</sub> membranes to perform transmission electron microscopy (TEM) analysis. The sample was converted from 6 nm WO<sub>x</sub> using elemental Se as the chalcogen precursor. Figure 3a shows a high-resolution transmission electron microscopy (HRTEM) image, with the converted WSe<sub>2</sub> interface either directly on the Si<sub>3</sub>N<sub>4</sub> membrane (left), or on the exfoliated monolayer WSe<sub>2</sub> flake (right); the indexed fast Fourier transform (FFT) patterns are insets on each side. Figure 3b and 3c show a portion of HRTEM images of each part of the film with higher magnification, with selected area electron diffraction (SAED) pattern insets. Schematic illustrations of the layered

WSe<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> structures are shown above the TEM images. For the selenized film grown directly on the Si<sub>3</sub>N<sub>4</sub> membrane, the HRTEM image shows that the minuscule grains exist in random orientations across the whole area. In contrast, for the selenized film grown on the exfoliated monolayer, the HRTEM image reveals an extended region displaying a well-defined hexagonal lattice pattern, suggesting improved local crystallinity and templated alignment with the underlying layer. This demonstrates that a single crystalline TMD monolayer can promote templated growth to synthesize high crystal quality TMD at a low substrate temperature.

In addition, to assess the thickness limit of our synthesis process, we deposited a 235 nm WO<sub>x</sub> on Si substrate and performed EDS to understand the conversion behavior. We have observed a homogenous conversion of WO<sub>x</sub> to WSe<sub>2</sub> for about 75 nm in thickness, showing that our conversion process shows good conversion even to thicker films as displayed in the EDS spectrum of the cross section scanning transmission electron microscopy (STEM) image in Figure S6. The conversion was non-uniform on a larger scale, as localized regions exhibited complete selenization penetrating the entire 235 nm film thickness.

Figure S7 presents a comparative study of surface morphology using Atomic Force Microscopy (AFM). The images depict the SiO<sub>2</sub>/exfoliated monolayer WSe<sub>2</sub> interface at three distinct process stages: post-exfoliation, after 3 nm WO<sub>x</sub> evaporation, and post-selenization. The root-mean-square ( $R_q$ ) surface roughness on the SiO<sub>2</sub> substrate increased from 0.2 nm to 2.0 nm following the complete process. In contrast, the  $R_q$  on the exfoliated WSe<sub>2</sub> flake increased from 0.8 nm to 1.5 nm. These data indicate that the selenization process yields a significantly smoother film when formed on the exfoliated monolayer WSe<sub>2</sub> as compared to the SiO<sub>2</sub>.

A variety of TMD films were successfully synthesized utilizing the low-temperature (LT) method previously described. To elucidate the gas-phase chemistry, the equilibrium composition for a H<sub>2</sub>S:Ar mixture (5:95, 1 bar) was calculated as a function of temperature (Figure S8). These calculations reveal a trend for sulfur analogous to that previously observed

for selenium where the highly reactive, shorter-chain sulfur allotropes are the dominant species at elevated temperatures, while more stable cyclic allotropes, such as S<sub>8</sub>, are favored at lower temperatures. Optical images of the successfully grown TMD films can be seen in Figure 4a, with their corresponding Raman spectra shown in Figure 4b, c, and d. We were able to convert not only tungsten oxide, but also molybdenum oxide, niobium, and platinum to WS<sub>2</sub>, WTe<sub>2</sub>, MoS<sub>2</sub>, MoSe<sub>2</sub>, NbS<sub>2</sub>, and PtSe<sub>2</sub> using powder selenium, sulfur, and tellurium sources.<sup>38–44</sup> The growths of these different films were carried out with the powder chalcogen source being placed in the upstream of the furnace, with an activation T and substrate T of 950 °C and 400 °C, respectively, the same conditions used to grow WSe<sub>2</sub>. Further optimization, by tuning the two temperatures of the furnace for each material, may enhance the film quality of these films, as each material may favor slightly different conditions. Still, these results show that our method is not limited to certain materials but rather can be incorporated into growing many other thin films.

To demonstrate a possible application and BEOL compatibility of our LT growth method, we prepared transfer-length method (TLM)<sup>45</sup> structures for electrical measurements, outlined in the steps shown in Figure 5a. Following the patterning of the exfoliated monolayer WSe<sub>2</sub> used as the FET channel, we deposited 6 nm of WO<sub>x</sub> and 30 nm of Rh as the source/drain contacts of the FET with a single step lithography lift-off. The WO<sub>x</sub> film was then converted to WSe<sub>2</sub> following the method described above, using elemental Se with an activation T of 950 °C and substrate T of 400 °C. The effectiveness of this converted WSe<sub>2</sub> interlayer for reducing contact resistance is discussed below. The device was subsequently doped with (30 wt % gold (III) chloride (AuCl<sub>3</sub>) dissolved in HCl to minimize the contact resistance.<sup>46</sup> The optical image is shown in Figure S9 along with an SEM image of the TLM design used for testing.

Figure 5b shows the output curves of each functioning device with different channel lengths, showing that the device with the shortest channel length has current levels near 600

$\mu\text{A}/\mu\text{m}$ . The extracted contact resistance using TLM fitting is shown in Figure 5c, which is approximately  $0.3 \text{ k}\Omega\cdot\mu\text{m}$ , lower than values previously reported for monolayer  $\text{WSe}_2$  transistors doped with  $\text{AuCl}_3$ .<sup>47</sup> The high current levels show the  $\text{WO}_x$  layer buried under the Rh on the source/drain pad was converted laterally from the exposed edge of the 6 nm thick  $\text{WO}_x$  film.<sup>26</sup> The lateral conversion was confirmed as devices that did not go through the selenization step showed poor conduction even after doping, as  $\text{WO}_x$  itself is an insulating material. Moreover, another TLM structure was fabricated to test contact resistance at different gate biasing conditions. As can be seen in Figure S10, with the current doping levels, the contact resistance change was not significant from  $V_{\text{BG}} = 0 \text{ V}$  to  $V_{\text{BG}} = -15 \text{ V}$  for our case, both yielding  $0.2 \text{ k}\Omega\cdot\mu\text{m}$ . To assess environmental stability, a device with a channel length of  $0.38 \mu\text{m}$  was measured again after one day and five days of exposure to ambient air. As presented in Figure S11, the device exhibited only a negligible change in its current levels. This result indicates the stability of the fabricated device and highlights the robust nature of the raised source/drain architecture against ambient degradation.

Although there could be miniscule parts of  $\text{WO}_x$  that were not fully selenized in the contact area, we believe the effect of *p*-type doping from the residual  $\text{WO}_x$ <sup>48</sup> is very small as can be observed from the device performance in Figure S12. The device was fabricated with 30 nm Rh contact on exfoliated monolayer  $\text{WSe}_2$  with which shows very poor conductance. After 3 nm  $\text{WO}_x$  was evaporated across the device, the device shows slight improvement in conductance, but still very low current levels with less than  $1 \text{ nA}/\mu\text{m}$  for the on-current. This shows that unintentional *p*-type doping from the residual  $\text{WO}_x$  would be miniscule in our method to improve the contact properties as full 3 nm  $\text{WO}_x$  evaporation across the monolayer  $\text{WSe}_2$  channel still resulted in a very poor device behavior.

To demonstrate a device with switching behavior, a top-gate FET with raised source/drain structure was fabricated with the process steps illustrated in Figure 6a. 2 nm  $\text{WO}_x$  was selenized using powder Se source for the raised source/drain for this monolayer  $\text{WSe}_2$  FET.

Different WO<sub>x</sub> and Rh thicknesses were intentionally chosen for the device in Figure 6 compared to the TLM structure in Figure 5 to demonstrate that our method is not constrained by a narrow processing window and is effective across a range of raised source/drain dimensions. Following device fabrication, selective doping of the regions adjacent to the contacts was achieved by drop-casting a 1 wt % PtCl<sub>4</sub> dissolved in HCl solution.<sup>49</sup> The optical image of the top-gate device is shown in Figure S13. Figure 6b shows the drain current dependence on the top-gate bias (V<sub>TG</sub>) and Figure 6c shows the drain current dependence on the drain bias (V<sub>DS</sub>) of the top-gate device. As shown in the figures, the device exhibits a normalized drain current of reaching a current level near 30 μA/μm where W and L are the width and channel length of the device, respectively. The on/off ratio is greater than 10<sup>6</sup>, thereby demonstrating the practical applicability of this raised source/drain fabrication methodology for high-performing devices. The peak field-effect mobility (μ) was extracted from the device's transfer characteristics using the transconductance method, defined as  $\mu = \frac{dI}{dV_{GS}} \frac{L}{WC_{ox}V_{DS}}$ , where  $I$  is the drain current,  $V_{GS}$  is the gate bias,  $L$  is the channel length,  $W$  is the width,  $C_{ox}$  is the oxide capacitance.  $C_{ox}$  was calculated using a relative permittivity of 16 for HfO<sub>2</sub>, a value reported for films deposited by low-temperature atomic layer deposition.<sup>50</sup> This analysis yielded a peak field-effect mobility of 13.5 cm<sup>2</sup>/(V·s) at a top-gate bias of -2.39 V and a drain bias of -3 V. This mobility is comparable to values in recent reports that similarly utilize highly doped contacts to improve monolayer WSe<sub>2</sub> transistor performance.<sup>51</sup> Figure S14 presents the performance of top-gate devices subjected to shorter doping durations. These results demonstrate that sufficiently doping both the exposed monolayer WSe<sub>2</sub> channel and the raised source/drain regions is critical for achieving high current drives.

Furthermore, a device from a separate fabrication batch, featuring slightly different dimensions, is presented in Figure S15 to establish reproducibility. This device was subjected to a 30-minute PtCl<sub>4</sub> doping process to show high-performance *p*-type characteristics. It

displayed a peak field-effect mobility of  $23.9 \text{ cm}^2/(\text{V}\cdot\text{s})$  at a top-gate bias of 0.28 V, measured under a drain bias of -1 V.

## **Conclusion**

In conclusion, using our LT growth method, we were able to grow WSe<sub>2</sub> thin-films, with BEOL/CMOS-compatible substrate temperatures – at or below 400 °C – by converting WO<sub>x</sub> to WSe<sub>2</sub>. This was enabled by using a high temperature zone located upstream in the furnace tube to ‘activate’ elemental Se or H<sub>2</sub>Se. The Raman spectra from the films show that at lower substrate temperatures, near 300 °C, the 1T’ WSe<sub>2</sub> phase is observed, while at higher substrate temperatures, near 400 °C, the 2H WSe<sub>2</sub> phase is observed. The critical role of activated Se in the growth process was elucidated by comparing the Raman spectra of WSe<sub>2</sub> films grown at 400 °C with activated Se to those grown at higher temperatures without precursor activation. TEM analysis confirmed that an exfoliated WSe<sub>2</sub> template layer facilitates templated growth of the converted WSe<sub>2</sub> film. Furthermore, the versatility of this method was demonstrated through its successful application to the growth of various TMDs, including WS<sub>2</sub>, WTe<sub>2</sub>, MoS<sub>2</sub>, MoSe<sub>2</sub>, NbS<sub>2</sub>, and PtSe<sub>2</sub>, as confirmed by Raman spectroscopy. Finally, we demonstrated ultralow contact resistance between a rhodium (Rh) metal contact and an exfoliated WSe<sub>2</sub> channel. This was achieved by fabricating a transmission line method (TLM) structure incorporating a converted WSe<sub>2</sub> interlayer at the source/drain regions, subsequently doped with AuCl<sub>3</sub>. Furthermore, a switching monolayer WSe<sub>2</sub>-channeled FET featuring a raised source/drain with on/off ratio exceeding  $10^6$  was demonstrated. This work highlights the practical utility of our LT method in significantly reducing metal-monolayer TMD contact resistance.

## **Methods**

### **Low temperature conversion of transition metal oxides and pure transition metal**

Transition metal oxides such as  $\text{MoO}_x$  and  $\text{WO}_x$  or pure transition metal such as Nb and Pt were deposited by electron beam evaporation with varied thicknesses of 3 nm to 6 nm on a Si/SiO<sub>2</sub> wafer and patterned using optical lithography using a lift-off process. Using a two-zone furnace, the chip with patterned material is placed in the lower temperature zone near 400 °C, downstream of the high temperature zone at 950 °C, used to facilitate activation of the chalcogen source. The substrate temperature was precisely calibrated by positioning a thermocouple at the specific location within the quartz tube where the sample substrate chip is situated, enabling accurate control of the temperature at the sample site. Time-temperature trace of the substrate temperature is shown in Figure S16 with 490 sccm of Ar flowing during the control experiment. The conversion was carried out for 15 minutes.

Two different setups were employed for the conversion of the patterned materials. For the setup involving  $\text{H}_2\text{Se}$  as the chalcogen source, shown in Figure S2, the setup had an outer quartz tube (25 mm outer diameter, 22 mm inner diameter) with an Ar flow rate of 400 sccm, and an inner quartz tube (6.35 mm outer diameter, 4 mm inner diameter) with an Ar and  $\text{H}_2\text{Se}$  flow rate of 90 sccm and 20 sccm, respectively. The setup that employed powder source Se, S, and Te, had a 1" tube, with a flow of 1000 sccm forming gas (5%  $\text{H}_2$  in  $\text{N}_2$ ).

### **Equilibrium gas composition calculation**

Enthalpies and entropies were calculated from the tabulated heat capacity values of each chemical compound in the format of NASA-9 parametrization<sup>52–56</sup> or the Shomate equation.<sup>57</sup> The thermodynamic equilibrium conditions were calculated using CANTERA<sup>58</sup> for each temperature.

### **Material characterization**

Raman spectra were obtained by using a Horiba Labram HR evolution Confocal Raman Microscope with a 473 nm laser as the excitation source. TEM imaging and EDS analysis were

performed at the National Center for Electron Microscopy at Lawrence Berkeley National Laboratory using the FEI TitanX 60-300 and FEI ThemIS 60-300 microscopes operated at 300 kV. The cross-sectional lamella for EDS analysis was prepared using a Thermo Scios-2 DualBeam SEM/FIB system. SEM and EDS images are captured from an FEI Quanta 3D FEG (field emission gun) with the Oxford AZtec software at QB3 at Berkeley. XRD measurements were performed by X-ray diffractometer (SmartLab, Rigaku) using Cu K $\alpha$  ( $\lambda = 1.5418 \text{ \AA}$ ) radiation at a scan rate of 3°/min and step size of 0.01°.

### **Device Fabrication**

Devices were fabricated using electron beam lithography to pattern the source/drain contacts with 950 PMMA C4. After developing the pattern for source/drain electrodes for the TLM structure, WO<sub>x</sub>/Rh (6 nm/30 nm) was deposited using electron beam evaporation for the source/drain contacts and was lifted off in acetone. The source/drain for the top-gate device was fabricated in the same way with slightly different thickness of the contact layers WO<sub>x</sub>/Rh (2 nm/15 nm). The gate stack was also fabricated using electron beam lithography, where 15 nm HfO<sub>2</sub> was successfully deposited using atomic-layer deposition at 90 °C on 1.2 nm SiO<sub>x</sub> deposited with electron beam evaporation. Subsequently, WO<sub>x</sub>/Rh (2 nm/15 nm) was deposited for the gate metal using electron beam evaporation and was lifted off in acetone.

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## Supporting Information

Raman spectra of 3 nm  $\text{WO}_x$  film converted to  $\text{WSe}_2$  at different substrate temperatures using  $\text{H}_2\text{Se}$  as the chalcogen source (Figure S1), Raman spectrum of a 3 nm tungsten oxide film converted to  $\text{WSe}_2$  at 300 °C and after annealing the film for 5 min (Figure S2), Furnace setup used for converting transition metal oxides/pure transition metal to TMDs using  $\text{H}_2\text{Se}$  (Figure S3), EDS mapping of 4 different spots of  $\text{WSe}_2$  film converted from 20 nm  $\text{WO}_x$  using powder Se source (Figure S4), representative EDS mapping showing peaks of different elements (W, Se, Si, O) (Figure S5), a cross-sectional STEM image of a 235 nm thick  $\text{WO}_x$  film, captured using HAADF detector (Figure S6), AFM images of  $\text{SiO}_2$ /exfoliated  $\text{WSe}_2$  interface in between each process (Figure S7), equilibrium mole fractions of sulfur gas phase species for 5% / 95%  $\text{H}_2\text{S}$  / Ar gas at 1 bar in linear scale and log scale (Figure S8), optical and SEM image of the TLM structure shown in Figure 5 (Figure S9). Extra TLM Structure tested for contact resistance testing (Figure S10), performance of device tested for TLM in Figure S10 with  $L = 0.38 \mu\text{m}$  after being left in air for one day and five days (Figure S11), device for testing doping effects from  $\text{WO}_x$  (Figure S12), optical image of the top-gate device shown in Figure 6 (Figure S13), top-gate transistor with raised source/drain contacts on exfoliated monolayer  $\text{WSe}_2$  based on different doping time (Figure S14), top-gate transistor with raised source/drain contacts on exfoliated monolayer  $\text{WSe}_2$  with different dimensions (Figure S15), and time-temperature trace of where the sample is placed while flowing 490 sccm Ar (Figure S16).

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### **Author Contributions**

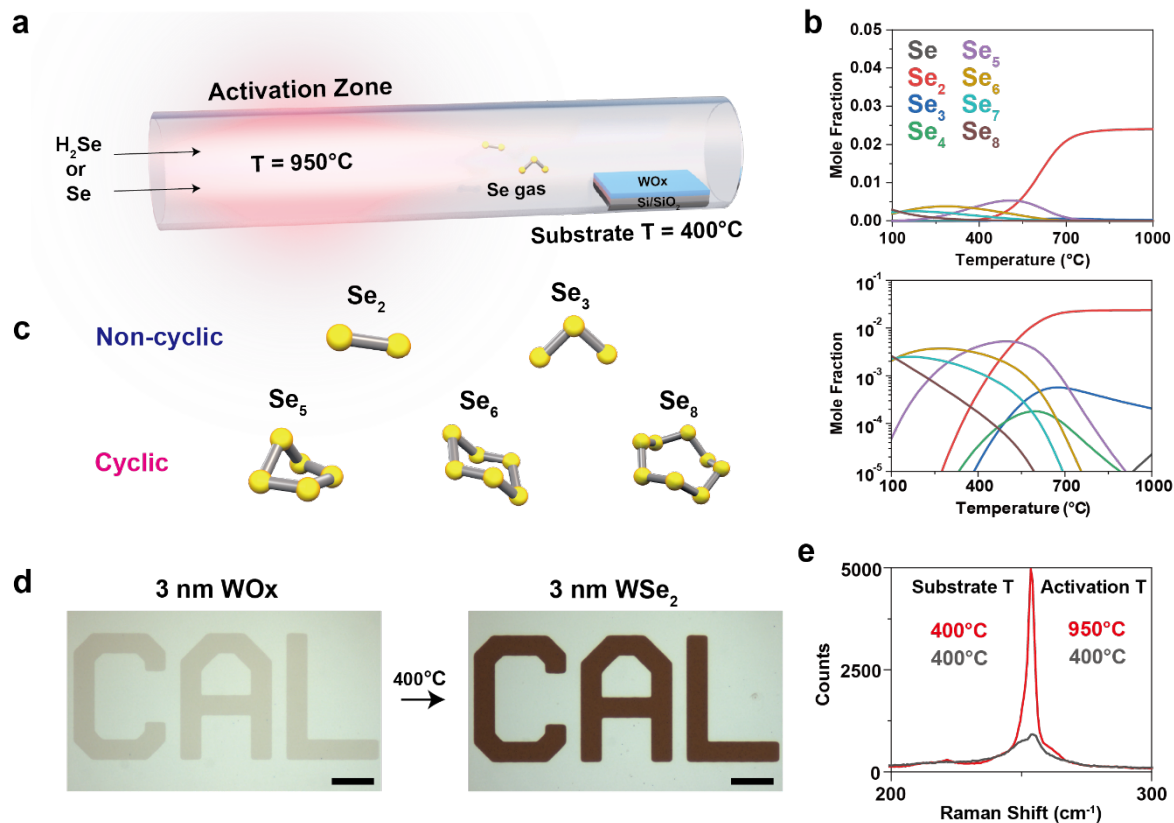
I.K. and A.J. conceived the idea for the project and designed the experiments. I.K. and D.U. fabricated the devices. I.K. and T.K. grew the materials with H<sub>2</sub>Se. I.K. performed optical characterizations. I.K., D.Z., M.J., and M.S. performed TEM measurements. I.K., D.U., and J.A. performed thermodynamic calculations. I.K., D.U., N.H., J.A., and A.J. analyzed the data. I.K. and A.J. wrote the manuscript. All authors discussed the results and commented on the manuscript.

### **Competing financial interests**

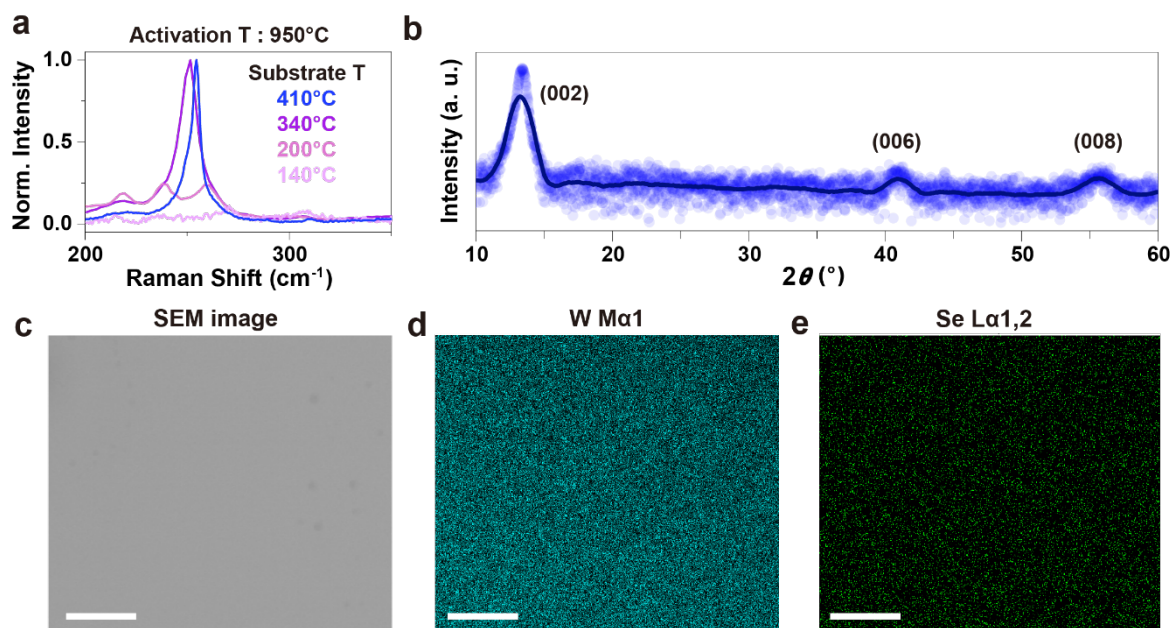
The authors declare no competing financial interest.

### **Corresponding Author**

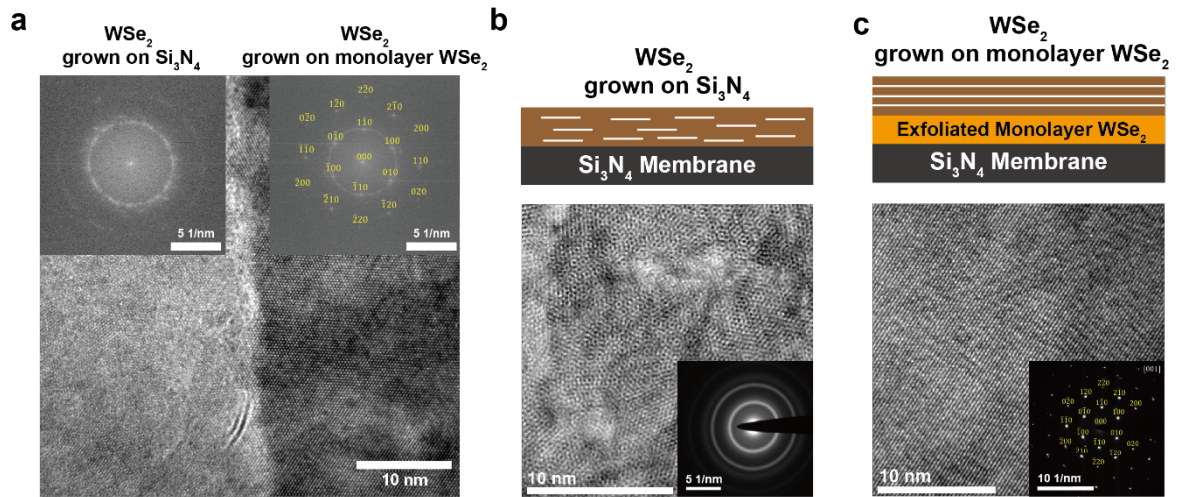
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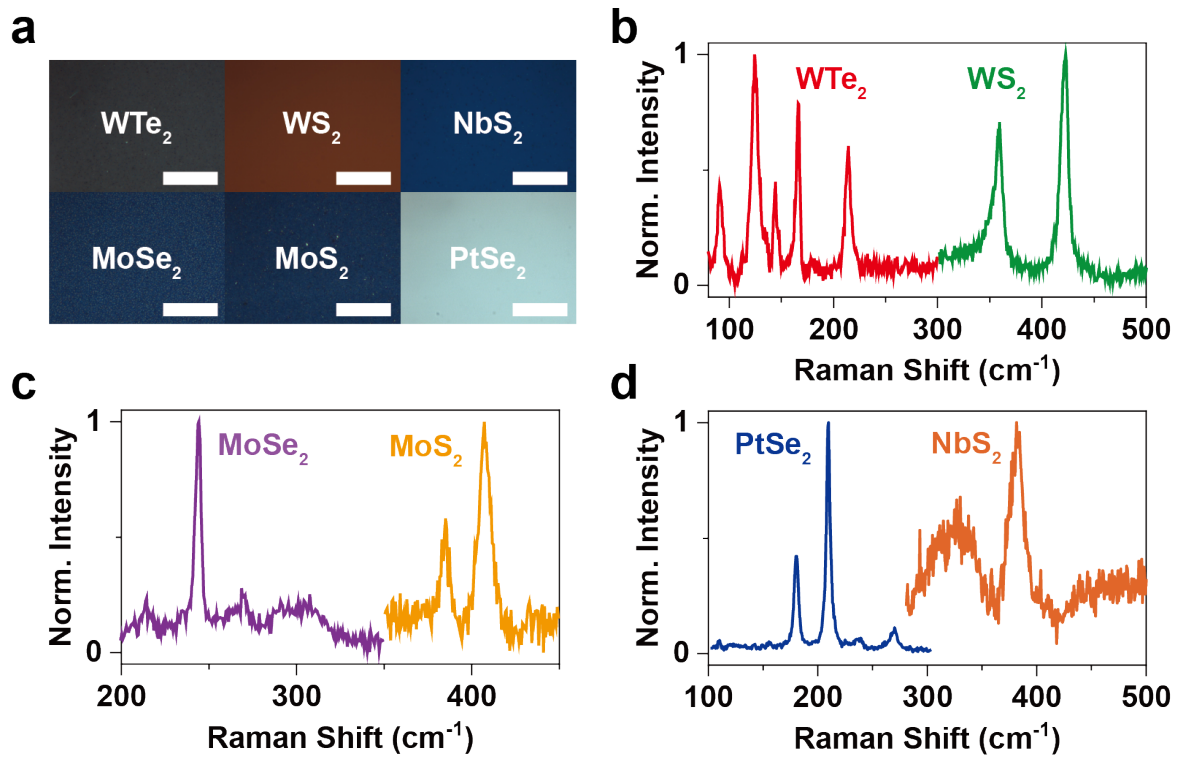
**Figure 1. Growth TMD thin films with substrates at low temperatures.** (a) Schematic illustration outlining our LT method of converting  $\text{WO}_x$  to  $\text{WSe}_2$ . Elemental Se or  $\text{H}_2\text{Se}$  is carried through the hot zone, held at 950 °C, to the cooler zone where the conversion reaction takes place at 400 °C. (b) Equilibrium mole fractions of Se gas phase species for 5% / 95%  $\text{H}_2\text{Se}$  / Ar gas at 1 bar in (top) linear scale and (bottom) log scale.  $\text{Se}_2$  is the dominant Se-containing species in this temperature regime.  $\text{H}_2\text{Se}$  is not visible in either of the plots because it appears to be fully dissociating in the temperature range shown in the figures. (c) Molecular structures of Se allotropes. Larger Se chains such as  $\text{Se}_5$ ,  $\text{Se}_6$ , and  $\text{Se}_8$  exist in cyclic chains compared to the smaller non-cyclic  $\text{Se}_2$  and  $\text{Se}_3$ . (d) Patterned 3 nm  $\text{WO}_x$  before reaction (left) and after selenization (right) using the process shown in (a). The scale bar is 30  $\mu\text{m}$ . (e) With the substrate kept at 400 °C, a significant increase in the intensity of the Raman signal is observed for samples grown with the activation zone held at 950 °C (red), compared to without the activation zone (gray). Samples in (e) were converted using  $\text{H}_2\text{Se}$ .



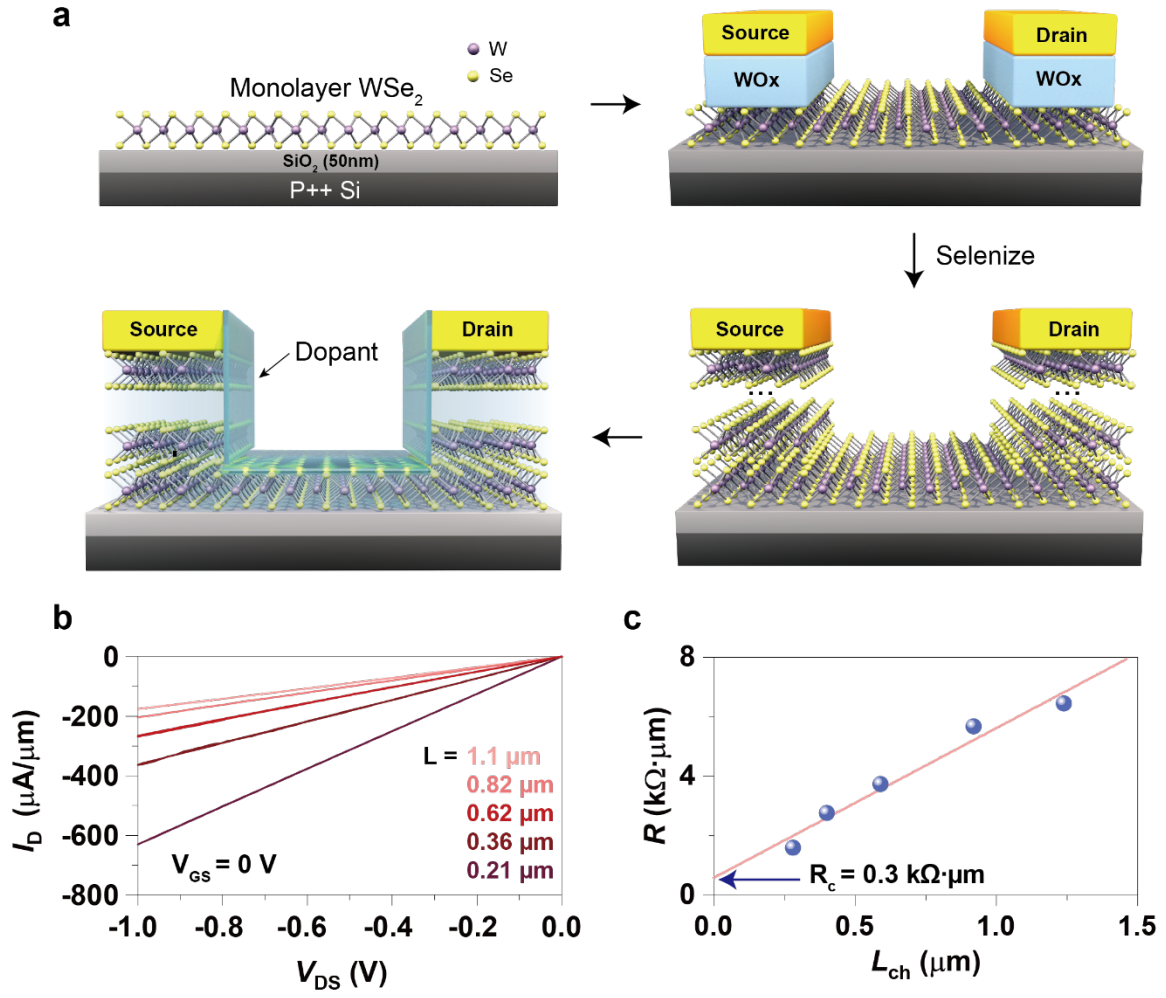
**Figure 2. Characterization of selenized  $\text{WO}_x$  thin films from elemental Se using the two-zone furnace.** (a) Raman spectra of selenized 3 nm  $\text{WO}_x$  with the activation zone held at 950 °C while the substrate temperature is altered. At lower temperatures such as 200 °C, a 1T'  $\text{WSe}_2$  Raman signal can be observed similarly as with  $\text{H}_2\text{Se}$ . (b) XRD pattern of the selenized 20 nm  $\text{WO}_x$  film. Diffraction peaks corresponding solely to the (0 0 n) planes of  $\text{WSe}_2$  are observed, indicating that the  $\text{WSe}_2$  is grown with its layered structure aligned parallel to the substrate. (c) SEM image of selenized 20 nm  $\text{WO}_x$  film. Scale bar is 50  $\mu\text{m}$ . (d) EDS of W  $\text{Ma}1$  fitted from the area shown in (c). Spectrum from W  $\text{Ma}1$  overlap with Si  $\text{Ka}1$ , hence some signal from Si could be unintentionally shown. (e) EDS of Se  $\text{La}1,2$  line from the area shown in (c).



**Figure 3. TEM images of the template assisted crystal growth of WSe<sub>2</sub> films.** (a) HRTEM image of WSe<sub>2</sub> film converted from WO<sub>x</sub> deposited directly on a Si<sub>3</sub>N<sub>4</sub> membrane (left) and WSe<sub>2</sub> converted from WO<sub>x</sub> deposited on a single-crystalline exfoliated monolayer WSe<sub>2</sub> flake on a Si<sub>3</sub>N<sub>4</sub> membrane (right). FFT patterns of each part are provided as inset on each side of the image. (b) Schematic illustration (top) and TEM image (bottom) of a WSe<sub>2</sub> film converted from WO<sub>x</sub> deposited directly on a Si<sub>3</sub>N<sub>4</sub> membrane. The lattice-resolved HRTEM image, and SAED pattern (inset), show the nanocrystalline morphology of the WSe<sub>2</sub> film. (c) Schematic illustration (top) and TEM image (bottom) of WSe<sub>2</sub> converted from WO<sub>x</sub> deposited on a single-crystalline exfoliated monolayer WSe<sub>2</sub> flake on a Si<sub>3</sub>N<sub>4</sub> membrane.

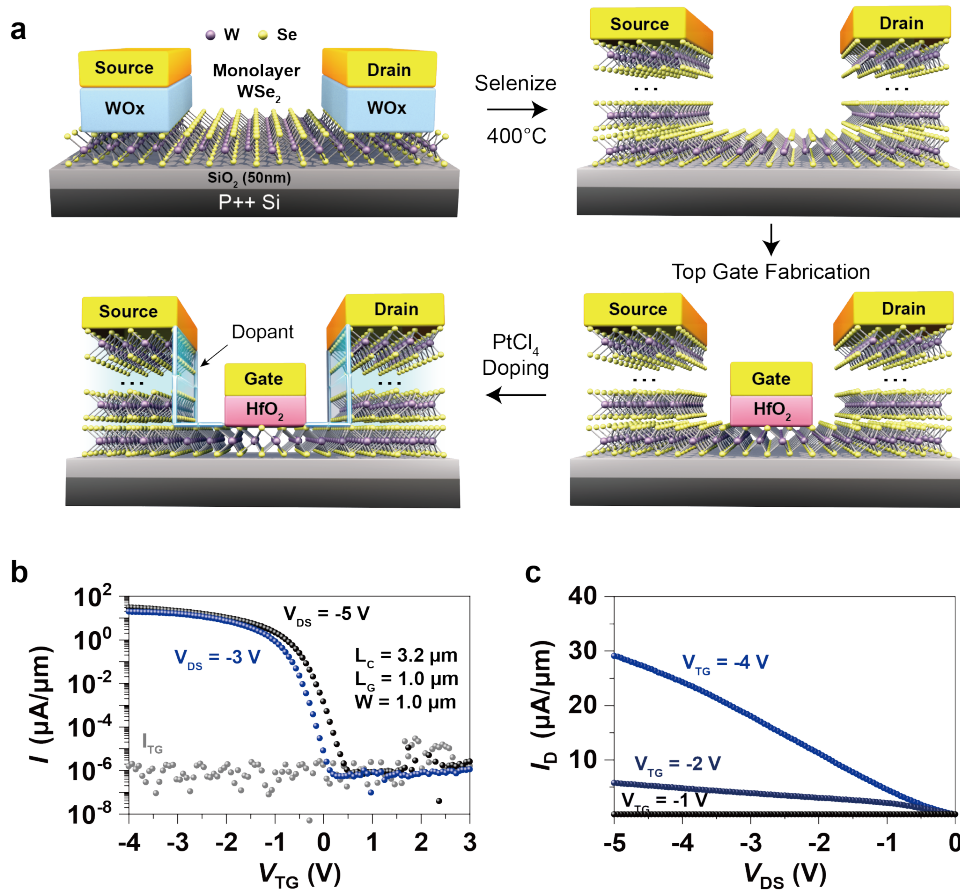


**Figure 4. TMDs grown using different transition metal/metal oxides and chalcogen species.** (a) Optical image of different transition metals and metal oxides undergone conversion using our LT method. (b), (c), and (d) Raman spectra of each of the TMDs shown in (a).



**Figure 5. Demonstration of raised source/drain contacts on exfoliated monolayer WSe<sub>2</sub>.**

(a) Fabrication steps to make raised source/drain on an exfoliated monolayer WSe<sub>2</sub> flake. First, the shape of the channel was defined using lithography to mask and etch an exfoliated monolayer flake (I). Next, 6 nm WO<sub>x</sub> and 30 nm Rh electrodes were defined by lithography and contact stack lift-off (II). The whole chip was then placed in the two-zone furnace and selenized using elemental Se (III). Finally, to mitigate the contact resistance, AuCl<sub>3</sub> was dropcasted on the device to make it highly *p*-type and to mitigate contact resistance (IV). (b) Drain current dependence on the drain bias of a TLM structure doped with AuCl<sub>3</sub> with different channel lengths. (c) Extracted contact resistance using a linear fit of the total resistance of each TLM measurement in (b).



**Figure 6. Top-gate transistor with raised source/drain contacts on exfoliated monolayer WSe<sub>2</sub>.** (a) Schematic of the top-gate transistor. Top-gate stack was made using atomic layer deposition of HfO<sub>2</sub> (15 nm) and e-beam evaporation of Rh after following the steps shown in Figure 5a for fabricating FET with raised source/drain. The device was finally doped with PtCl<sub>4</sub> for p-type doping. (b) Drain current dependence on the top-gate bias ( $V_{\text{TG}}$ ) with the back-gate grounded. Width ( $W$ ), gate length ( $L_g$ ), channel length ( $L_c$ ) of the device are shown. Top-gate leakage current ( $I_{\text{TG}}$ ) for  $V_{\text{DS}} = -5 \text{ V}$  is shown for reference. (c) Drain current dependence on the drain bias ( $V_{\text{DS}}$ ) with different top-gate biasing conditions with the back-gate grounded.