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Low Thermal Budget Process Engineering for Flexible Electronics, Sensors, and Nanoscale Patterning

by

Thomas Ryland Rembert

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Ming C. Wu
Professor Junqiao Wu

Fall 2019

Low Thermal Budget Process Engineering for Flexible Electronics, Sensors, and Nanoscale Patterning

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Abstract

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Doctor of Philosophy in Engineering – Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Tsu-Jae King Liu, Chair

Within every process of electronic device fabrication and subsequent device use, there exists an inherent temperature limitation. This limitation can be part of a particular processing step or a target specification of device operation. To determine the temperature restrictions required by a device and its fabrication, the material system and target application of the resultant device must be assessed, as the thermal budget will vary based on both of these factors. If the temperature limit imposed on a device and its process becomes low enough, measures must be taken to ensure a reduction in thermal load is met without sacrificing the integrity of the constituent materials or the final device behavior. More specifically, these measures result in the development of low temperature materials deposition techniques, devices with reduced power consumption, or low temperature in-line processing techniques. In this dissertation, I will present solutions to circumvent temperature limitations in three areas: transparent flexible electronics, small-scale gas sensors for the Internet of Things (IoT), and back-end-of-line (BEOL) processing steps of state-of-the-art integrated circuits (ICs).

First, in Chapter 2, a novel method of metal oxide material deposition for flexible thin film transistors (TFTs) will be discussed. Materials characterization indicates this material is of high quality suitable for flexible electronics, demonstrated via fabrication of fully transparent all-oxide flexible TFTs. Second, in Chapter 3, a chip-integratable pollutant gas sensor based on silicon transistors is discussed. Transistor-based gas sensing leverages IC manufacturing and enables low temperature operation, allowing for lower power consumption carbon monoxide sensors for air quality monitoring and personal pollution tracking. Lastly, Chapter 4 will present a novel low cost fully-BEOL-compatible nanoscale patterning method based on tilted ion implantation and conventional deep ultraviolet (DUV) lithography. Utilizing silicon-containing spin-on films, patterns on the order of 20 nm are achieved, providing an alternative lithographic method for state-of-the-art transistor fabrication with nanoscale features.

To those who support me, believe in me, care for me, and love me,
even when I can't do it myself

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Chapter 1

Introduction

Within every process of electronic device fabrication and subsequent device use, there exists an inherent temperature limitation. This limitation can be part of a particular processing step or a target specification of device operation. To determine the temperature restrictions required by a device and its fabrication, the material system and target application of the resultant device must be assessed, as the thermal budget will vary based on both of these factors. If the temperature limit imposed on a device and its process becomes low enough, measures must be taken to ensure a reduction in thermal load is met without sacrificing the integrity of the constituent materials or the final device behavior. More specifically, these measures result in the development of low temperature materials deposition techniques, devices with reduced power consumption, or low temperature in-line processing techniques. In this dissertation, I will present solutions to circumvent temperature limitations in three areas: transparent flexible electronics, small-scale gas sensors for the Internet of Things (IoT), and back-end-of-line (BEOL) processing steps of state-of-the-art integrated circuits (ICs).

1.1 Flexible Electronics

1.1.1 Background & Motivation

The development of low-cost, widespread consumer electronics, combined with the introduction of wearable health monitoring systems, has created a need for devices based on materials other than traditional crystalline Si used in high-performance microprocessors. Common examples of this need are seen in modern television and mobile phone display systems as well as smart watches with integrated health sensors, utilizing materials systems such as amorphous Si (a-Si), low temperature polysilicon (LTPS), organic semiconductors, and semiconducting metal oxides. Most of these technologies are implemented using the thin-film transistor (TFT) as their driving technology due to its larger processing window, relaxed material quality constraints, and reduced cost compared to traditional transistors [1]. For example, the initial commercial uses of TFTs for pixel control in displays were based on an a-Si material

platform, but the need for improvement of particular device characteristics such as the off-current (I_{OFF}) and the ratio of the on-current to the off-current (I_{ON}/I_{OFF}, on/off ratio) as well as material properties such as electron mobility (indicative of TFT switching speed, or display refresh rate) caused many industry vendors to turn to a TFT platform based on the quaternary metal oxide material indium-gallium-zinc oxide (IGZO) material system [1–3]. This switch is an example of the materials-focused research to create application-specific transistors for new electronics.

As these electronics become more integrated into our existing infrastructure, the market share for flexible electronics is projected to continually increase (Fig. 1.1). Given the diversity

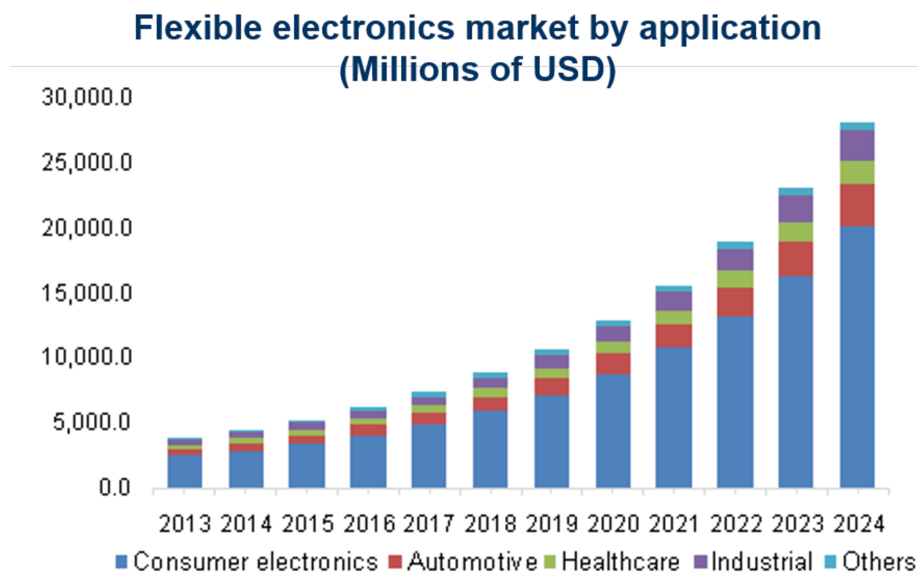


Figure 1.1: Flexible electronics market by application [4].

of applications of flexible electronics, different areas may require the use of certain materials systems or have specific processing limitations. For example, flexible electronics on thin glass substrates have a less stringent thermal budget than plastics, allowing for different material deposition methods and processing conditions, and transparent electronics require using materials with minimal optical absorbance. Semiconducting metal oxides, such as IGZO, offer both high material quality at various deposition temperatures and optical transparency in the visible wavelengths, making them a strong candidate for future flexible electronics applications.

1.1.2 Semiconducting Metal Oxides

Each of the previously referenced material systems for TFTs (a-Si, LTPS, organics, metal oxides) possesses a subset of desirable material qualities, such as mechanical flexibility and

electron mobility, and processing requirements, such as low temperature deposition and large-scale thickness uniformity, but no system offers a universal solution to TFTs or flexible electronics. Fig. 1.2 provides a qualitative comparison of some of these materials. This

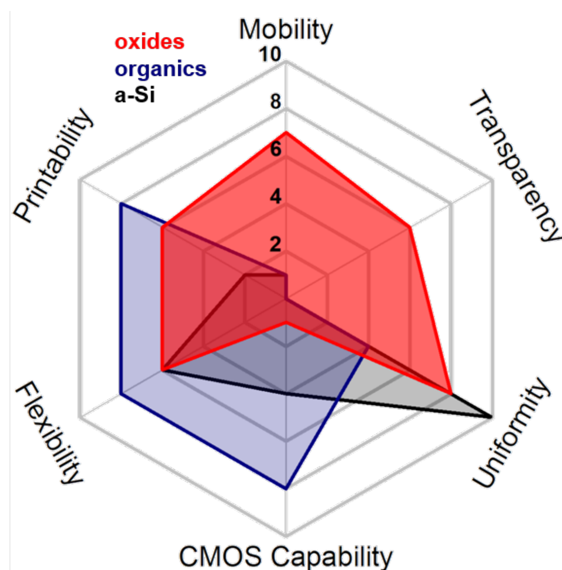


Figure 1.2: Comparison of TFT material system ratings for various material and processing properties, adapted from [3].

leads to materials selection based on the desired application. Given this work's target of high quality TFT performance for flexible transparent electronic applications, oxides are the chosen TFT channel material.

Most semiconducting metal oxides exhibit n-type behavior, making the capability of true complementary metal-oxide-semiconductor (CMOS) devices difficult, as they require both an n-type and p-type transistor. While the development of p-type oxides for TFT applications is an ongoing research direction, this issue is not addressed in this work, which instead focuses on the development of a novel n-type oxide deposition process for future integration into existing TFT systems such as displays, transparent electronics, and flexible electronics. While IGZO is the industry-favorite metal oxide TFT material, previous work on ZnO-based TFTs helped pioneer the field of oxide TFTs [1]. Additionally, given the deposition process used in this work, our process was inherently limited to a single oxide species rather than forming oxide compounds with more than one metal type.

1.1.3 Temperature Limitations

TFT Channel Material

Regardless of the chosen TFT channel material, deposition onto plastic substrates requires lower processing temperatures, leading to a degradation in material quality as compared to

a higher temperature process for the same material (i.e., loss of crystal structure with decreased deposition temperature leading to reduced electrical transport properties) [5]. While this is known to be circumvented by implementing post-deposition thermal treatment of thin films, such as an ambient air anneal step, many of these treatment processes can exceed the thermal budget restrictions of the substrate material [6–10]. This necessitates materials deposition processes that minimally reduce material quality when scaled to plastic-compatible temperatures and do not require post-deposition thermal treatment steps.

Flexible Substrate

Specifically in terms of flexible electronics, the substrate material used is mechanically deformable, which is usually achieved by means of a thin plastic material. This limits the material and processing steps further by requiring the desired TFT material to be both mechanically robust and deposited at plastic-compatible temperatures. Given mechanical bending can be improved by thinning the substrate, which also helps reduce strain on subsequent layers, the temperature stability of the plastic material arises as the limiting factor of fabrication process steps [11]. Many different plastics can and have been used as flexible substrate materials, with the most common plastics used being polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyimide (PI) (Fig. 1.3). Each plastic has its

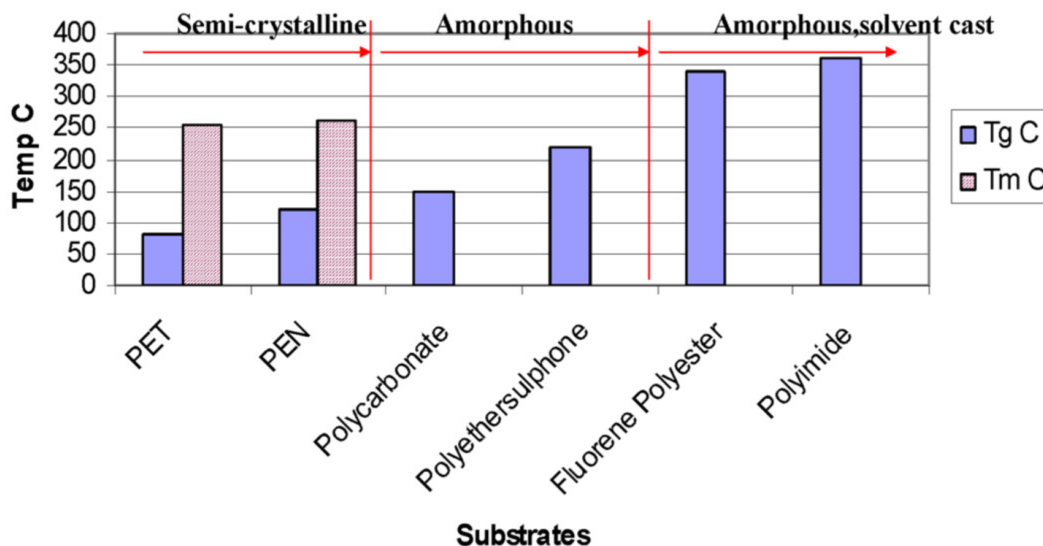


Figure 1.3: Glass transition temperatures (T_g) of common substrate materials used in flexible electronics. T_m indicates the melting point for lower-thermal-budget materials [11].

own advantages and may be a more suitable choice depending on the application or processing requirements. For example, PET is known for having high optical clarity but may suffer from surface roughness issues due to its semi-crystalline character, whereas solvent cast PI has very low surface roughness but is not fully transparent in the visible light spectrum. In

this work, spin-cast PI is used for the plastic substrate material to benchmark our novel semiconducting oxide material deposition process due to its low surface roughness.

1.2 IoT Sensors

1.2.1 Background & Motivation

With the rise of IoT, the number of connected devices is projected to continually increase, with almost the majority of device increase coming from IoT devices (Fig. 1.4). This will lead to a growing network of sensors and control systems that will require integration into existing infrastructures and consumer electronics. IoT sensors are based on a mesh of devices that

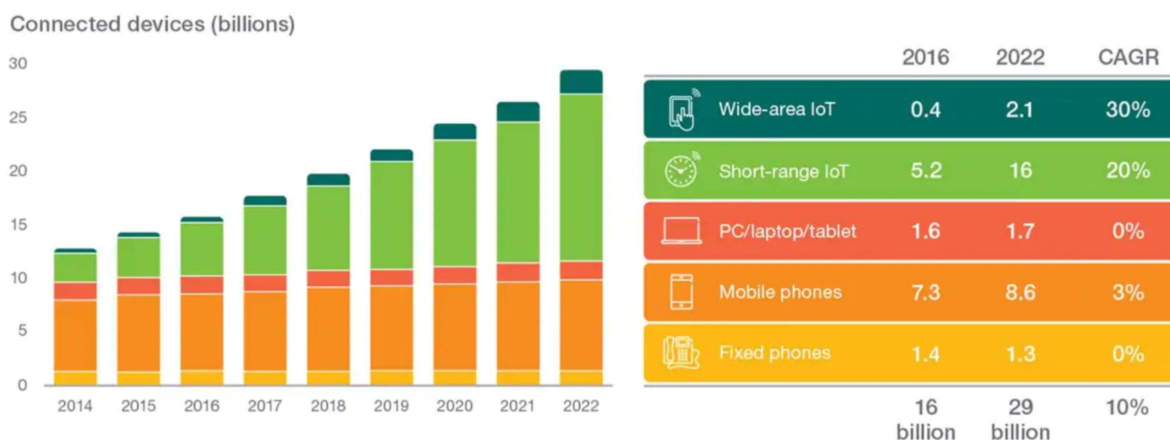


Figure 1.4: IoT connected device growth for different device types [12].

exist separate from a main user interface, transmitting sensing data to a central location for monitoring. One of the specific IoT sensors under continued development is the gas sensor. While current gas monitoring systems exist, they do not have a form factor sufficient for mobile use or require high power supplies that limit the sensor to a nearby fixed power source. Therefore, the future of IoT gas sensors requires minimal power consumption and small form factor in order to successfully integrate with mobile electronics.

1.2.2 Pollutant Gases

Among the plethora of gases to detect, one subset of interest is that of pollutant gases. These gases can affect both the natural environment in which they are being produced as well as have adverse health effects on the people who are exposed to too much pollution. The Environmental Protection Agency (EPA) has established the National Ambient Air Quality Standards (NAAQS) to identify the major pollutant gases and their respective concentration values that are not to be exceeded if air quality is to be maintained [13]. Table 1.1 indicates these values along with the National Institute for Occupational Safety and Health (NIOSH)

and Center for Disease Control (CDC) defined workplace permitted exposure limit (PEL) and immediately dangerous to life and health (IDLH) gas concentration values of the NAAQS pollutant gases: carbon monoxide (CO), sulfur dioxide (SO_2), nitrogen dioxide (NO_2), and ozone (O_3).

Table 1.1: IDLH, PEL, and air quality gas concentrations for EPA-defined pollutant gases [13, 14].

Pollutants and Exposure Levels	CO	SO_2	NO_2	O_3
IDLH	1200 ppm	100 ppm	20 ppm	5 ppm
PEL	50 ppm	5 ppm	5 ppm	0.1 ppm
NAAQS	35 ppm (1 h) 9 ppm (8 h)	0.075 ppm (1 h)	0.1 ppm (1 h)	0.07 ppm (8 h)

1.2.3 Temperature Limitations

The target sensing gas, along with the sensing mechanism of the device itself, dictates the inherent power and/or temperature limitations for successful operation. In the case of an IoT sensor, these would need to be minimized, as high power consumption would require the sensor power supply to either be large or replaced often. Gas sensors based on a chemical reaction (i.e., gas oxidation or reduction) are typically enhanced with heating, as additional heat enhances the reaction rate, leading to faster sensing. However, heating needs to be minimized in order to conserve power. Many in-home sensors may require heating of sensing elements up to 300 °C which is not practical for standalone sensors or for sensors integrated into mobile electronics. Therefore, IoT pollutant gas sensors need to implement a sensor architecture that has an inherently high sensitivity, as reducing the operation temperature will make accurate detection of low gas concentrations more difficult.

1.3 Integrated Circuit Fabrication

1.3.1 Background & Motivation

Moore's Law

The trend of Moore's Law states the number of transistors on a chip doubles every two years, fueling the continued scaling of transistors for increased device density as well as lower cost per function (Fig. 1.5) [15]. The evolution of transistors over the past few decades has seen devices reach nanometer-scale dimensions, orders of magnitude smaller than their predecessors. Scaling to such feature sizes uncovers many nonidealities in transistor behavior, such

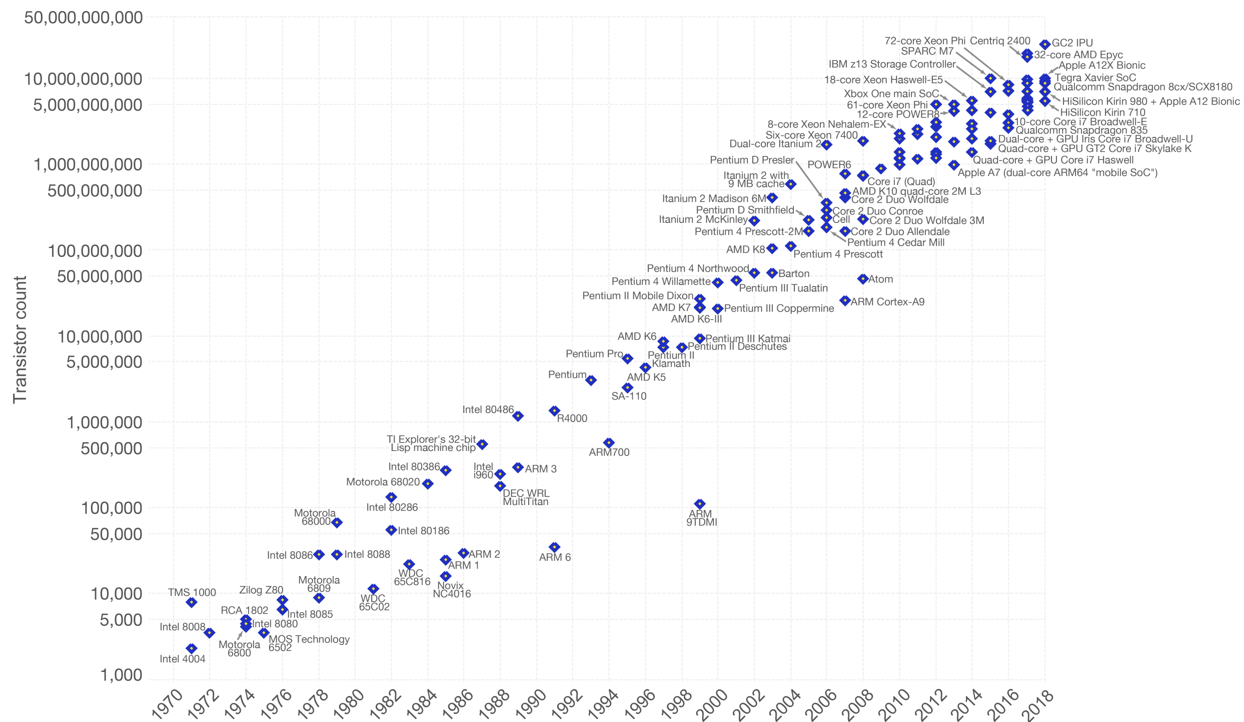


Figure 1.5: Transistor count of manufactured processors as a function of time [16].

as those seen in device performance degradation via short channel effects [17]. To circumvent this, designers have implemented novel fabrication schemes and device architectures such that these detrimental effects can be mitigated while maintaining the overall goal of increased transistor density and increased on-current [17, 18].

In addition to physical transistor dimensions, subsequent layers during fabrication, such as metal line layers, also have scaling requirements of their own. The International Roadmap for Devices and Systems (IRDS) predicts that by as early as four years from now, we will reach dimensions for which manufacturable solutions are not known (Table 1.2) [19]. While portions of the device architecture, such as transistor half-pitch, are projected to be scaled using novel transistor layouts (i.e., transitioning from fins to lateral channel gate-all-around, LGAA, to vertical channel gate-all-around, VGAA), many feature sizes of chip fabrication do not have in-place solutions. This fast-approaching need for patterning technologies with minimum feature sizes beyond current capabilities presents an immediate need for alternative lithographic approaches.

1.3.2 Patterning Technologies

While the continued scaling and novel device structures have enabled scaling of Si transistors to nanometer-scale dimensions, these processes and feature sizes are inherently limited by the patterning technologies used during fabrication. Therefore, as device dimensions con-

Table 1.2: IRDS projections for device half-pitch, physical gate length (L_G), and metal line half-pitch. DRAM, HP, and MPU stand for dynamic random access memory, high performance, and microprocessor unit, respectively. Yellow cells indicate parameters for which manufacturable solutions are known but high volume manufacturing has not been developed. Red cells indicate parameters for which manufacturable solutions are not known.

Year of Production	2017	2019	2021	2024	2027	2030	2033
DRAM min. 1/2 pitch [nm]	18	17.5	17	14	11	8.4	7.7
HP Logic physical L_G [nm]	20	18	16	14	12	12	12
MPU metal 1/2 pitch [nm]	18	14	12	10.5	7	7	7
Transistor 1/2 pitch [nm]	16	14	12	10.5	9	7	7
	(fin)		(LGAA)			(VGAA)	

tinue to shrink, so do the minimum resolutions of the utilized patterning mechanisms. The most commonly used lithography technology used in industry has been optical photolithography based on mercury lamps ultraviolet (UV) and excimer laser deep ultraviolet (DUV) light sources [20]. Over the past handful of decades, smaller feature sizes in patterned device layers have been achieved via the use of light sources with decreasing wavelengths as well as immersion-based systems to decrease the numerical aperture of the exposure tool (Fig. 1.6) [21].

In addition to optical patterning, multiple patterning or pitch-halving techniques such as self-aligned double and quadruple patterning (SADP and SAQP, respectively) used in conjunction with photolithography have been adopted by industry for further dimension scaling past the lithographic limit [22, 23]. At the same time, much progress has been made in the area of using light with wavelengths approximately an order of magnitude lower than previous exposure wavelengths, referred to as extreme ultraviolet (EUV) lithography, with single-exposure patterns on the order of 14 nm having been demonstrated [22]. The adoption of EUV lithography for high volume manufacturing is in place for existing foundries in the coming years [24].

Despite the industrial adoption of techniques such as multiple patterning and EUV lithography, each technique is not without its own challenges. Additionally, competing technologies, such as nanoimprint lithography and directed self-assembly, offer their own advantages and drawbacks for nanometer-scale patterning (Table 1.3). Common challenges among these technologies include cycle time, cost, line-edge roughness (LER), and defectivity. Thus, a future patterning technology that can achieve high-fidelity nanometer-scale patterns at low cost and processing time is requisite for further transistor scaling.

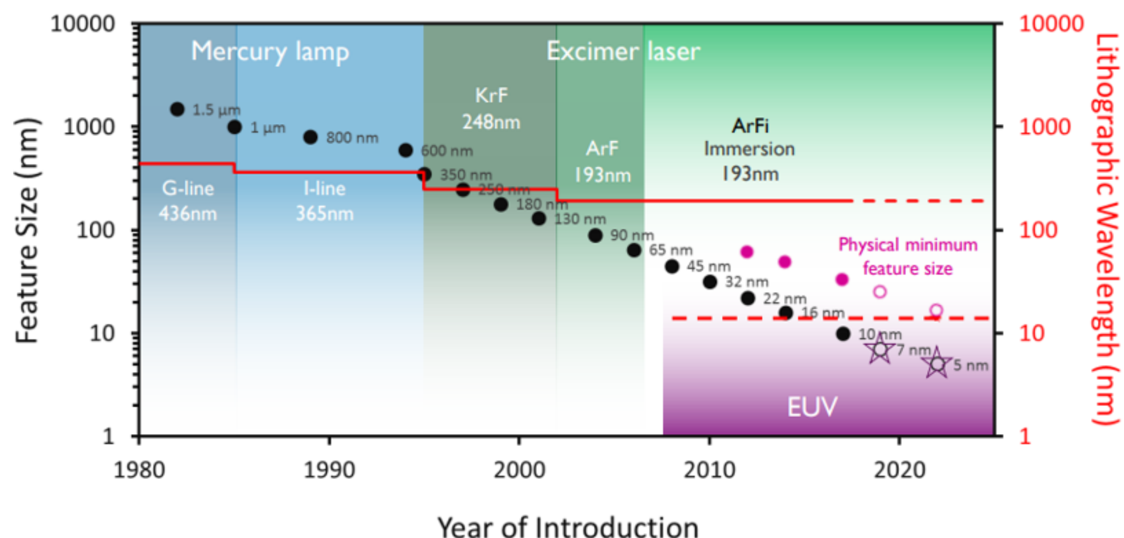


Figure 1.6: Trend in optical lithography wavelength as a function of patterned feature size [20].

Table 1.3: Comparison of patterning technologies' target feature/device and key challenges [19].

Patterning Technology	Target Feature	Key Challenges
Multiple Patterning $> 4\times$	vias, contact, cut patterns	edge placement errors, overlay, long cycle time, cost
EUV	22/24 nm half pitch contact holes, cuts; BEOL metals (18 nm)	tool uptime, defectivity, resist speed combined with LER and stochastics
Nanoimprint	20 nm line/space, 20/30 nm half pitch contact holes	defectivity, overlay, master template writing/inspection, template replication
Directed Self-Assembly	contact holes/cut levels, nanowire patterning	pattern placement, defectivity and defect inspection, design, 3D metrology

1.3.3 Temperature Limitations

BEOL Process Steps

A uniquely difficult feature to process is that of the back-end-of-line (BEOL) metal line half-pitch, as it will soon require sub-10 nm line widths and requires that all processing steps do not exceed ∼400 °C to avoid unwanted effects on underlying device layers (i.e., resistance increase of metal vias) [25]. With a BEOL-limited process temperature hundreds of degrees lower than processing steps used in the initial device layer fabrication steps, combined with the stringent requirement of low cost high-fidelity nanometer-scale patterning, an alternative low temperature fabrication process is needed.

1.4 Dissertation Structure

First, in Chapter 2, a novel method of metal oxide material deposition for flexible thin film transistors (TFTs) will be discussed. Materials characterization indicates this material is of high quality suitable for flexible electronics, demonstrated via fabrication of fully transparent all-oxide flexible TFTs. Second, in Chapter 3, a chip-integratable pollutant gas sensor based on silicon transistors is discussed. Transistor-based gas sensing leverages IC manufacturing and enables low temperature operation, allowing for lower power consumption carbon monoxide sensors for air quality monitoring and personal pollution tracking. Lastly, Chapter 4 will present a novel low cost fully-BEOL-compatible nanoscale patterning method based on tilted ion implantation and conventional deep ultraviolet (DUV) lithography. Utilizing silicon-containing spin-on films, patterns on the order of 20 nm are achieved, providing an alternative lithographic method for state-of-the-art transistor fabrication with nanoscale features.

Chapter 2

All-Oxide Transparent, Flexible Electronics

2.1 Materials for Oxide-Based Flexible TFTs

As previously discussed, metal oxides have the material quality and process capability to be utilized in high quality TFTs for consumer electronics and wearable applications. Transparent and flexible electronics represent two emerging fields that have much traction for future technological applications [26–28]. Traditional thin-film transistors fabricated from polysilicon and amorphous silicon and later from organic semiconductors and carbon nanotubes enabled the realization of large-scale flexible circuits for display and sensor applications [29–36]. More recently, the family of semiconducting post-transition metal oxides (ZnO, In_2O_3, InZnO, InGaZnO, etc.) offers an additional platform with wide energy band gaps for optical transparency over the full visible range, room temperature deposition (both solution-based and physical vapor deposition techniques) for plastic substrate compatibility, and electronic properties suitable for TFTs for transparent, flexible, and bio-related applications [6, 37–41]. However, many existing fabrication techniques for these oxide TFTs, while they are being deposited at room temperature, require higher temperature annealing steps to prime the oxide (i.e., improve crystallinity, improve stoichiometry, or calcination of solutions) for TFT use or to improve the device performance to an acceptable level [6–10]. Unfortunately, the use of higher temperatures for processing and device improvement can severely limit substrate compatibility and present challenges for integration with other components. In order to retain a wide range of substrate choices without sacrificing device performance, a low temperature fabrication scheme is needed. In this work, we demonstrate fully transparent all-oxide based ZnO TFTs with low operational voltages fabricated using a room temperature deposition method with no post-processing annealing and a maximum device processing temperature of 110 °C.

The schematic process flow for the fabrication of top-gated ZnO TFTs is shown in Fig. 2.1. ZnO TFTs are fabricated on three different substrates: i) a reference silicon wafer substrate

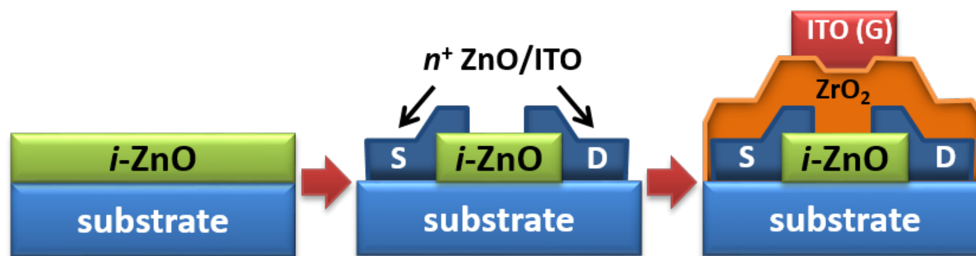


Figure 2.1: Process schematics of ZnO TFT fabrication.

with a 50 nm thick thermal oxide, ii) transparent alkali-free borosilicate glass, iii) flexible polyimide foil (Fig. 2.2). Substrates are cleaned with acetone and isopropyl alcohol and blown dry with nitrogen. Substrates are then loaded into a cathodic arc vacuum deposition chamber and pumped down to $\sim 5 \times 10^{-6}$ Torr for ZnO deposition. The filtered cathodic arc deposition for zinc oxide has originally been developed for the deposition of transparent conducing oxide films [42]. It has been shown that this deposition technology is similar to pulsed laser deposition (PLD) as it produces a flux of energetic ions. The typical Zn ion energy is 36 eV [43] which leads to local heating right at the film growth region without imposing a large heat load to the substrate. Additionally, in contrast to magnetron sputtering, negative oxygen ions are not accelerated to very high energies of several 100 eV because the arc operates at low arc voltage (the potential difference between anode and cathode is less than 40 V).

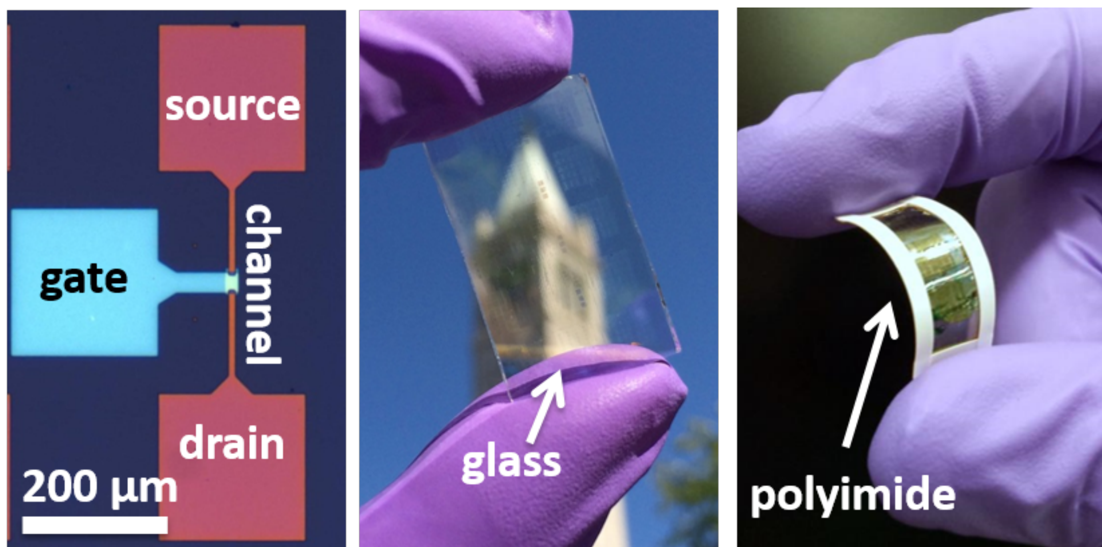


Figure 2.2: Optical microscope image of finished device on silicon (left), photograph of finished device array on glass slide (center), and photograph of finished devices on freestanding polyimide foil bent between fingers (right).

2.2 Filtered Cathodic Arc Deposition

Cathodic arc deposition (Fig. 2.3) uses a relatively low DC voltage to trigger and sustain a metal arc plasma, where the discharge current of about 50 A is concentrated in non-stationary cathode spots [44]. In contrast to the former work on AZO [42], here we use a pure (undoped) zinc (99.99%) cathode. It is surrounded by an annular grounded anode body. A permanent ring magnet is placed at the bottom part of the cathode cone: its purpose is to steer the moving arc spots around the cathode, enabling efficient material use and spreading of the heat load on the cathode. The zinc plasma generated at cathode spots streams away from the cathode into the curved macroparticle filter coil. The purpose of the coil is to guide the plasma to the substrate, which is not in line-of-sight with the cathode. In doing so, the plasma particles (electrons and ions) are separated from the microscopic but relatively massive zinc droplets, also known as "macroparticles." The coil is made of hollow, water-cooled copper tubing. It operates at a constant current of 400 A, producing a magnetic field of the order of 100 mT (more details on plasma guiding and macroparticle removal can be found in Ref. [44]). Zn ions react with oxygen dosed into the deposition chamber via a mass flow controller to form a ZnO film on the near-room-temperature substrate surface. Fig. 2.4 shows a photograph of a ZnO deposition process via filtered cathodic arc.

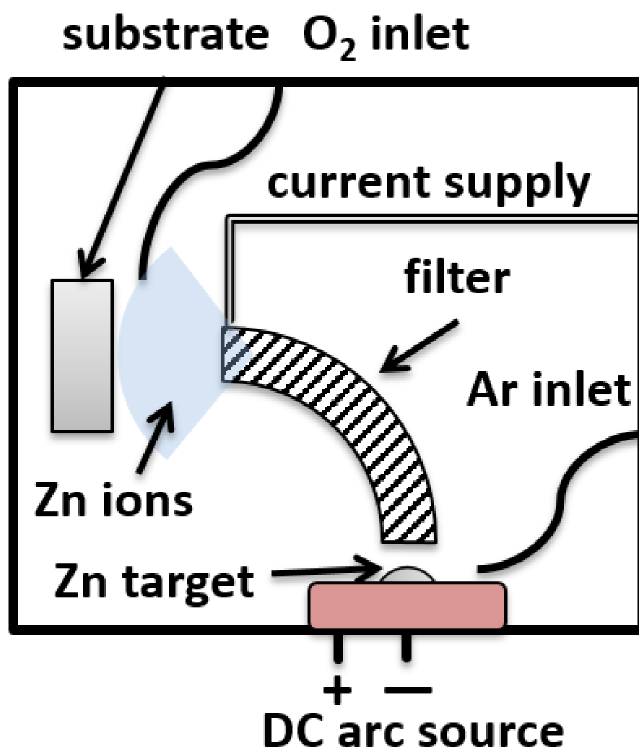


Figure 2.3: Schematic of cathodic arc deposition chamber. The permanent magnet is denoted in red.

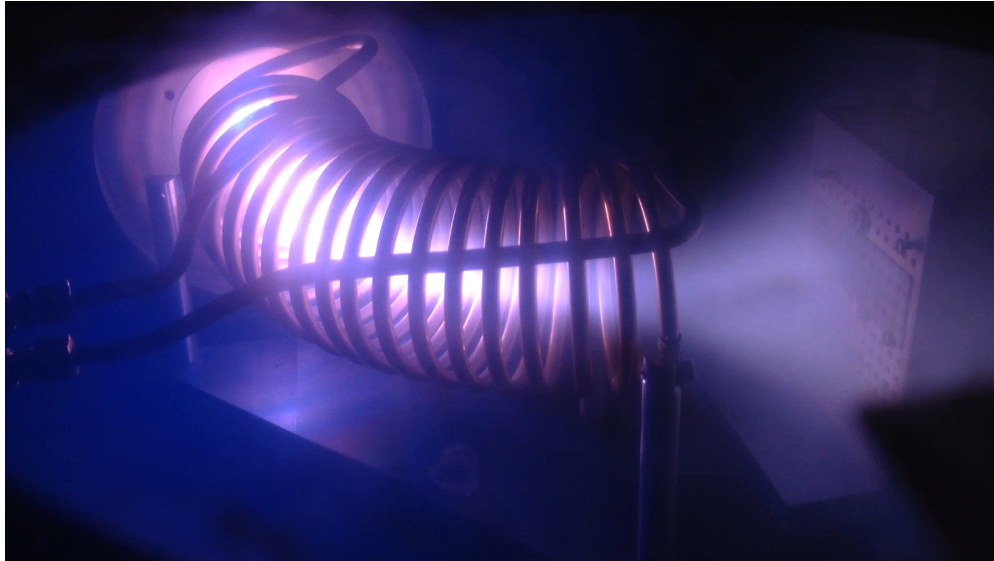


Figure 2.4: Photograph of filtered cathodic arc deposition process of ZnO thin films.

2.3 All-Oxide TFT Fabrication Process

For the start of the fabrication process, 30 nm of ZnO is deposited as the active TFT channel material onto the substrates placed 12.5 cm away from the exit of the plasma macroparticle filter coil in a 5 mTorr O_2/Ar ambient (O_2 60 sccm, Ar 20 sccm unless otherwise stated). Photolithography is used to define patterns for the source and drain electrodes via lift-off. Source and drain pads consist of 40 nm-thick degenerately doped ZnO deposited at lower O_2 partial pressure than the TFT channel ZnO (5 mTorr, O_2 20 sccm, Ar 20 sccm, room temperature), followed by 30 nm of indium tin oxide (ITO) sputtered in a 7 mTorr Ar ambient also at room temperature. A second photolithography step is performed to define the ZnO channel region of the transistors by etching in hydrochloric acid (HCl 1% for 1 s). In this process, the top ITO film on the source and drain serves as an etch stop barrier for the underlying ZnO, as the etch rate for ITO in HCl is much lower than that of ZnO [45]. A 20 nm-thick ZrO_2 top gate oxide is deposited by atomic layer deposition (ALD) at a maximum temperature of 110 °C, and subsequently patterned by photolithography. The same ITO sputtering and lift-off process is then used to define the top gate contact. Fig. 2.2 shows optical images of the devices completed on silicon, alkali-free glass, and free-standing polyimide foil, respectively.

2.4 ZnO Materials Characterization

2.4.1 Structural Characterization

X-ray Diffraction

We first explore the material properties of ZnO thin films deposited by cathodic arc. X-ray diffraction spectra (XRD) of the ZnO films for various O_2 flow rates are shown in Fig. 2.5. All

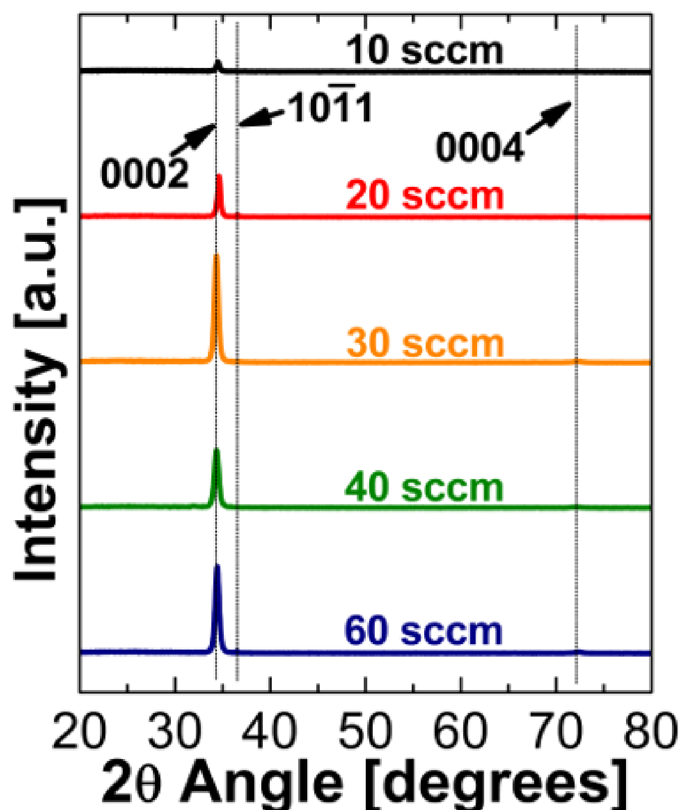


Figure 2.5: XRD spectra for ZnO films deposited at different O_2 flow rates.

films exhibit a polycrystalline hexagonal wurtzite structure and {0002} texture in agreement with literature [46]. The c-axis lattice constant extracted from the 0002 peak at 34.8° is 5.2 Å in good agreement with values for sputtered ZnO films [47]. No peaks corresponding to metallic Zn inclusions are detected. Estimating the grain size from the 0002 peak positions, 2θ, and full-width half-maximum widths, β, using the Scherrer equation

$$D(2\theta) = \frac{K\lambda}{\beta \cos 2\theta} \tag{2.1}$$

assuming a crystallite shape factor $K = 0.9$ and substituting $\lambda = 0.154$ nm for the wavelength of Cu Kα radiation, yields grain sizes between ~17–23 nm [48].

Atomic Force Microscopy

Additionally, the surface roughness of the ZnO films was characterized via atomic force microscopy (AFM). Film roughness was assessed for ZnO films deposited on glass, Si, and ∼250 µm-thick free-standing polyethylene terephthalate (PET) substrates (Fig. 2.6). The resulting measurements indicate the ZnO film is quite smooth, with the roughness of each film closely matching the roughness of its underlying substrate.

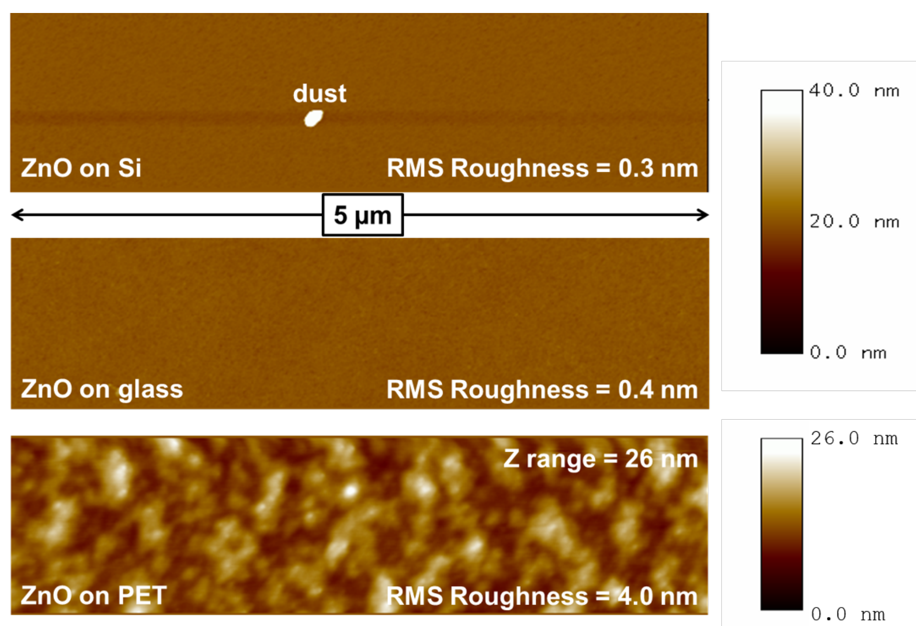


Figure 2.6: Surface roughness measurements of ZnO films deposited by filtered cathodic arc on Si (top), glass (middle), and PET (bottom).

2.4.2 Electrical Characterization

For transistor application, it is important to precisely control the conductivity of the ZnO channel to enable gate control. The carrier concentration in the ZnO film can be tuned by adjusting the O_2 flow rate during deposition as the carrier concentration of intrinsic ZnO films directly correlates with the number of oxygen vacancies [46, 49]. We chose to keep the Ar flow rate and the total deposition pressure constant (20 sccm and 5 mTorr, respectively) and vary the O_2 flow rate from 10 sccm to 35 sccm to modulate the electron concentration in the ZnO. As the O_2 flow rate is increased from 15 sccm to 35 sccm, the electron concentration drops from the mid-10^{19} cm^{-3} range to the low 10^{18} cm^{-3} range (Fig. 2.7), while the Hall mobility (second panel in Fig. 2.7) essentially remains constant between 17.3–21.2 $cm^2\,V^{-1}\,s^{-1}$, with the highest recorded mobility of 21.2 $cm^2\,V^{-1}\,s^{-1}$ being deposited at an O_2 flow rate of 15 sccm. For the higher O_2 flow rates above 35 sccm, the resistivity of the films (third panel

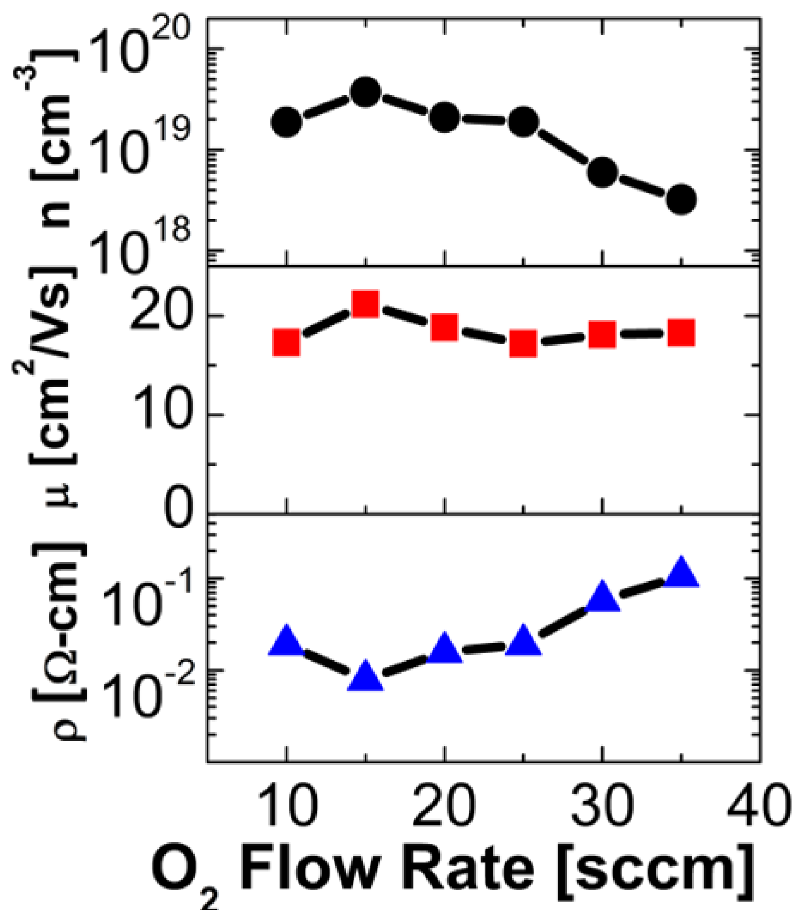


Figure 2.7: Electron concentration (n), Hall mobility (μ), and resistivity (ρ) of ZnO films as a function of O_2 flow rate.

in Fig. 2.7) increases too rapidly, rendering Hall measurements unreliable on our setup. However, the ZnO mobilities reported here appear to be some of the highest Hall mobilities for room-temperature-deposited thin film oxides for TFTs reported in literature, showing that cathodic arc deposition is reliable for producing high quality ZnO films [6, 38–40, 50, 51].

2.4.3 Optical Characterization

The ZnO films were optically characterized with transmission and reflection measurements in the visible and UV light wavelength range. Fig. 2.8 shows the optical absorption of the ZnO films as a function of wavelength for various O_2 flow rates. As the O_2 flow rate increases from 10 sccm to 30 sccm, the sub-bandgap absorption at wavelengths longer than 400 nm decreases significantly. This is caused by metallic Zn clusters becoming embedded in the film. Too low of an O_2 flow rate prevents present Zn particles from reacting with

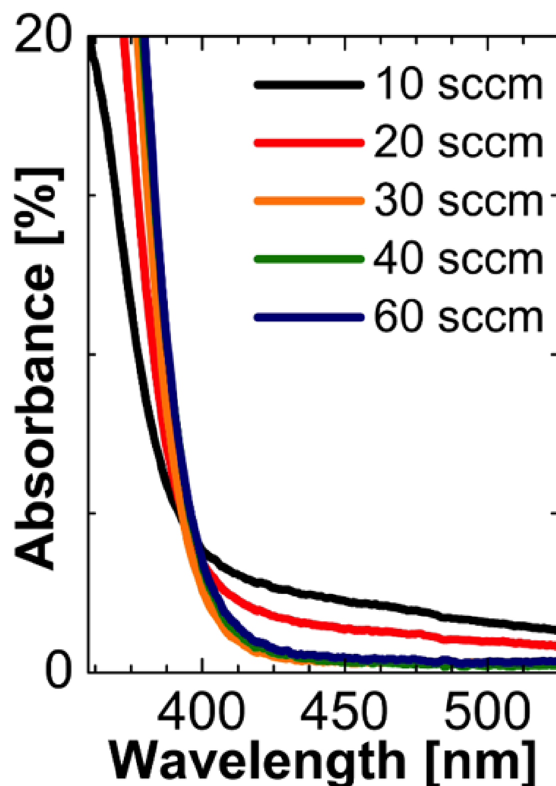


Figure 2.8: Dependence of the optical absorption of ZnO films with deposition O_2 flow rate.

the ambient oxygen, causing Zn particles to remain and provide trap states that reduce the absorption. Increasing the O_2 flow rate reduces the number of unreacted Zn particles, thusly reducing the number of trap states and decreasing the absorption. The absorbance of 30 nm ZnO films in this spectral range drops below 2%. In parallel, the absorption edge at wavelengths shorter than 400 nm shifts to longer wavelengths for increasing O_2 flow rates due to the decreasing electron concentration. This effect is attributed to the reduction of the Burstein-Moss shift, which decreases the optical bandgap as the Fermi level lowers with decreasing electron concentration. These findings are consistent with our Hall measurement results. Absorbance data for 60 sccm O_2 which is the O_2 flow rate used for the ZnO TFT channel, is practically identical to the data for 40 sccm although film resistivity further increases.

2.5 ZnO-Based All-Oxide TFT Performance

2.5.1 Alkali-Free Glass Substrate

Fig. 2.9 shows the drain to source (DS) and gate to source (GS) I_{DS}-V_{GS} transfer curves of a TFT device on alkali-free glass with channel width and length of 100 µm, operated at $V_{GS} = \pm 3\,\mathrm{V}$ and $V_{DS} = 3\,\mathrm{V}$, resulting in an on/off current ratio of $\sim 10^5$. The subthreshold slope (SS) is calculated from a linear fit (dotted line) to be SS = 204 mV dec^{-1}. The threshold voltage of $V_t = 0.36\,\mathrm{V}$ was extracted from a linear fit of $I_{DS}{}^{1/2}$ vs. V_{GS}. The saturation mobility was determined to be $\mu_{sat} = 4.5\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, calculated using the peak value of the slope of the $I_{DS}{}^{1/2}$ vs. V_{GS} plot under $V_{DS} = 3\,\mathrm{V}$ saturation operation and a capacitance-voltage (CV) extracted gate oxide capacitance of $C_{ox} = 597\,\mathrm{nF\,cm^{-2}}$. Fig. 2.9 shows the I_{DS}-V_{DS} characteristic of the device, exhibiting typical square-law behavior and reaching an on-current of almost 40 nA µm^{-1}. These values compare well with the best reported oxide

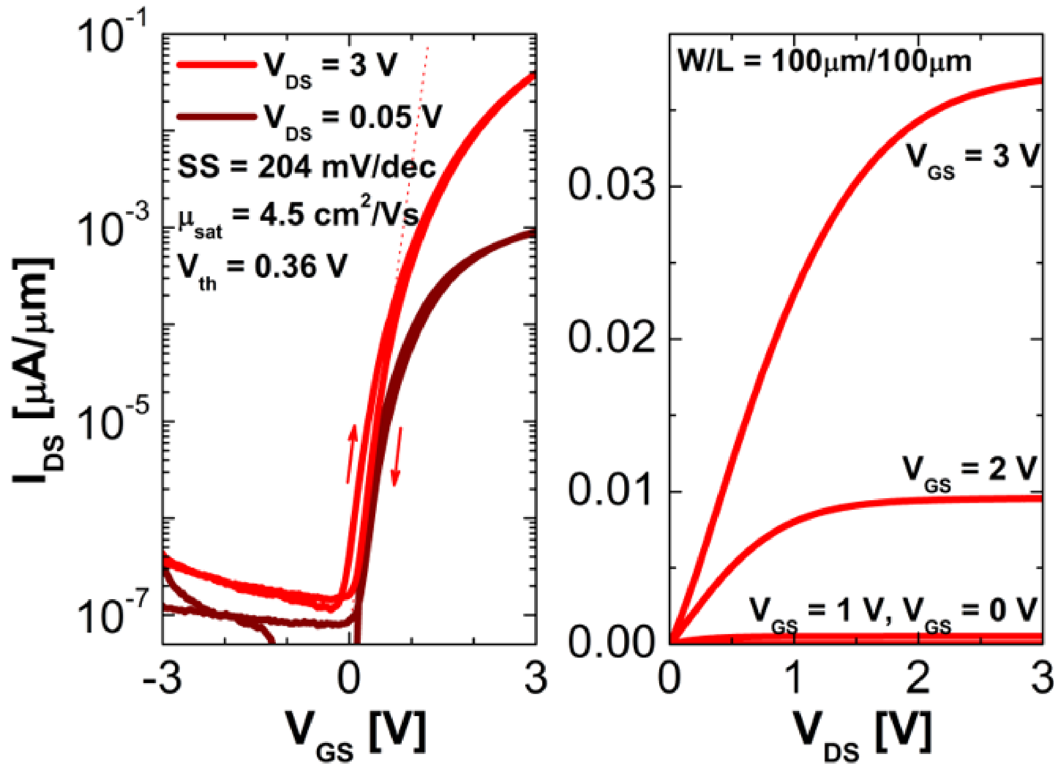


Figure 2.9: I_{DS}-V_{GS} (left) and I_{DS}-V_{DS} (right) curves for $W/L = 100\,\mu\mathrm{m}/100\,\mu\mathrm{m}$ device on alkali-free glass. The arrows on the transfer curves indicate the direction of the double sweep measurement.

low temperature TFTs in literature with SS typically in the range of one hundred to a few hundreds of mV dec^{-1} and V_t less than 1 V [51–57]. It should be noted that alkali-free glass is chosen due to impurities in other glasses, such as microscopy slides. We found that charged

ions in the glass were causing a threshold voltage shift of our devices, so alkali-free glass was used to avoid this issue. Additionally, the off-current of our devices is comparable to those reported in literature, showing that the room-temperature process is able to produce devices with just as low of an off-current as compared to those with higher temperature processes. In terms of the saturation mobility, our lower values as compared to literature can be associated with interface states between the ZrO_2 gate oxide and ZnO channel overlap capacitances between the gate and source/drain, which would cause some of the applied gate field to contribute to state filling and source/drain charges rather than channel inversion, as well as contact resistance effects. These effects can be combated by annealing or plasma treatments for the oxide interfaces and improved alignment during fabrication to reduce the overlap capacitances. Again, seeing that we are avoiding any higher temperature or post-annealing to improve the gate-channel interface, future work should look into plasma treatment to enhance the ZrO_2-ZnO interface.

2.5.2 Polyimide Substrate

The TFT fabrication process was then ported to flexible polyimide foils. Polyimide resin was spun on a temporary silicon handling wafer and cured at 300 °C for an hour before device fabrication. Fig. 2.10 shows the I_{DS}-V_{GS}transfer curve of the ZnO TFT on polyimide with channel width and length of 100 µm operated at $V_{GS} = \pm 3\,V$, exhibiting an on/off current ratio of almost 10^5, with extracted subthreshold slope, threshold voltage, and saturation mobility of $SS = 251\,mV\,dec^{-1}$, $V_t = 1.2\,V$, and $\mu_{sat} = 4.8\,cm^2\,V^{-1}\,s^{-1}$, respectively. Fig. 2.10 shows the I_{DS}-V_{DS} curves indicating expected square-law behavior with an on-current of almost $40\,nA\,\mu m^{-1}$, thus reaching identical performance characteristics to the device on glass and with those reported in literature. For each of the I_{DS}-V_{GS} curves on the two substrates, the increase in off-current at low V_{GS} operation can be attributed to gate leakage resulting from both the thin 20 nm gate oxide and the source/drain to gate overlap. The steepness of the subthreshold slope can also be restricted by trap states in the channel-oxide interface, energy band tail states of the ZnO, and contact resistance effects from the ITO contacts to the ZnO channel. The on/off ratio is 10^5 at 3 V operation, whereas other studies report ratios as high as 10^8 [52, 53]. Since the focus of this project is on low voltage operation for digital circuits, we are unable to directly compare the low voltage operation performance of some of the referenced TFTs with higher on/off ratios at higher operation voltages. This is because the referenced devices are operated at voltages of V_{GS} and V_{DS} $\geq$10 V, while ours are run at a V_{GS} and $V_{DS} = 3\,V$. Overall, the devices made on glass and polyimide show consistent, transferable and reproducible behavior, suggesting the cathodic arc deposition method to be a universally applicable technique for creating fully-transparent ZnO TFTs on a variety of substrates. Table 2.1 summarizes our results for the ZnO TFT on polyimide and compares this device to other high-performance oxide TFTs reported in literature.

Table 2.1: Comparison of this work (denoted with *) to previously reported ZnO and IGZO TFTs. V_{op} and W/L denote the operation voltage and channel size of the published device, respectively. Max T refers to the maximum temperature used during device processing, excluding substrate preparations. V_{op} refers to the gate voltage range in which the device was reported, with the accompanying V_{DS} voltage being the highest of the reported V_{op} value. It should be noted that transparency is defined as all components of the transistor, including the gate, source/drain contacts, and the substrate altogether be transparent.

Material	ZnO*	ZnO [10]	ZnO [55]	ZnO [56]	ZnO [57]	IGZO [52]	IGZO [53]	IGZO [54]
Dep. Method	CAD	PLD	sol-gel	sputtering	solution	sputtering	sol-gel	sputtering
On/off ratio	10^5	$>10^4$	10^4	$>10^4$	$>10^4$	$<10^7$	10^8	$<10^8$
V_{op} [V]	±3	−1–4	0–3	±1.5	−1–3	±20	±10	±3
SS [mV/dec]	251	250	≈ 300 (est.)	180	250	200	95.8	60
V_t [V]	1.2	2	0.7	0.1	0.1	2	2.7	0.5
μ_{sat} [$cm^2\,V^{-1}\,s^{-1}$]	3.1	0.024	3.4	0.45	22.1	11	<10.5	10
W/L	100/100	2000/50	1500/100	500/50	N/A	400/100	100/10	1000/5
Max T [°C]	110	200	280	200	150	RT	150	325
Transparent?	Yes	Yes	No	No	No	Yes	No	No
Flexible?	Yes	No	Yes	Yes	No	No	Yes	No

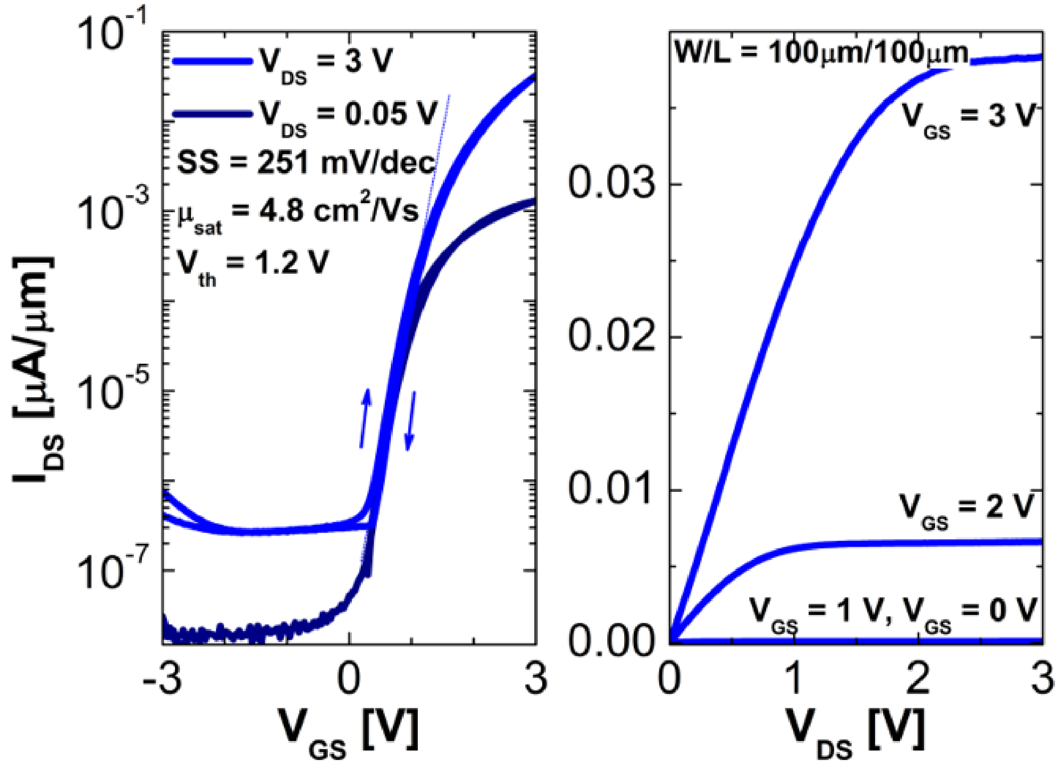


Figure 2.10: I_{DS}-V_{GS} (left) and I_{DS}-V_{DS} (right) curves for $W/L = 100\,\mu\mathrm{m}/100\,\mu\mathrm{m}$ device on polyimide. The arrows on the transfer curves indicate the direction of the double sweep measurement.

2.5.3 Performance of Bent TFT

With the focus of these TFTs being on applications in flexible electronics, bending studies are performed to get an idea of the mechanical robustness and its effect on the electrical performance of the device. To remove the polyimide from the handle wafer, the polyimide was cut around the edges and then submerged into DI water for twenty minutes. Putting the sample in water promotes self-delamination of the polymer from the substrate. This process prevents the polyimide from needing to be manually peeled off, which induces strain on the polymer, potentially cracking the fabricated devices. Once the polyimide has delaminated, the polyimide foil is laid flat, and the devices are measured to quantify possible effects from internal strain relaxation during delamination. Bending tests are then performed by wrapping the polyimide around a test tube with $r = 8\,\mathrm{mm}$ and measuring the device performance while bent. Fig. 2.11 shows the I_{DS}-V_{GS} and I_{DS}-V_{DS} curves for the $W/L = 200\,\mu\mathrm{m}/25\,\mu\mathrm{m}$ device after peeling off the handle wafer before bending and while bent. This device geometry is chosen for its higher output current values. The on-current of the device drops almost one order of magnitude during delamination, which may be attributed to defects created in the device during strain relaxation of the polyimide film upon delamination. However, while

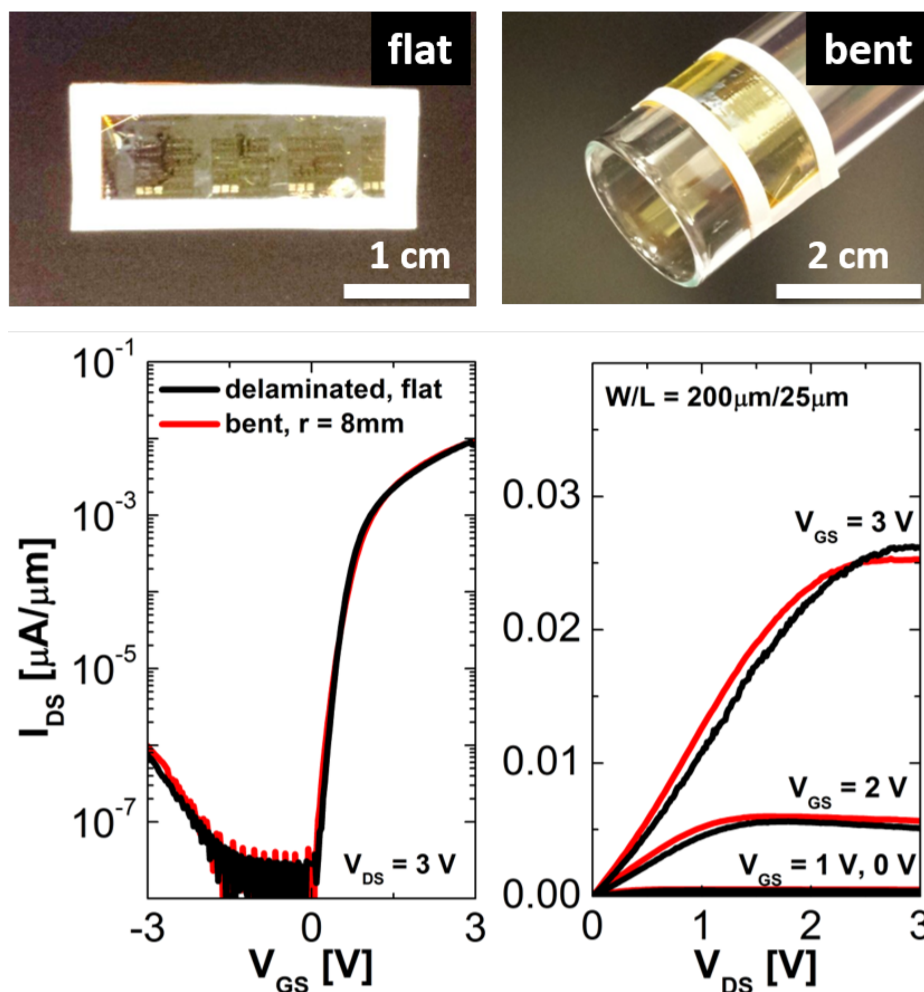


Figure 2.11: Photographs of the substrate while flat (top left) and bent (top right) around a test tube with $r = 8\,\text{mm}$. I_{DS}-V_{GS} (bottom left) and I_{DS}-V_{DS} (bottom right) curves for $W/L = 200\,\mu\text{m}/25\,\mu\text{m}$ device on freestanding polyimide (black) and bent at $r = 8\,\text{mm}$ (red).

bent at $r = 8\,\text{mm}$, there is minimal change in device performance, proving that our ZnO TFT process is not only universally applicable to various substrates but also mechanically robust for flexible electronics.

2.6 Demonstration of NMOS Inverter

Furthermore, to demonstrate the applicability of this process to integrated logic systems, we have fabricated an inverter gate. Due to these devices being solely NMOS, the inverter was constructed with a depletion-mode transistor load rather than a PMOS device or resistor. Henceforth, the transistor in which the input (V_{IN}) is passed is referred to as the "switching

transistor," whereas the depletion-mode transistor, whose gate terminal is connected to the inverter output node (V_{OUT}), is referred to as the "load transistor." The switching voltage of the inverter only depends on the V_{t} of the switching transistor since the load transistor is acting as the resistive load, so the supply voltage to the inverter (V_{DD}) was chosen to maximize the inverter noise margin. At an input voltage of $V_{\mathrm{IN}} = 0\,\mathrm{V}$, the switching transistor is off and has a much greater resistance than the load transistor. Thus, V_{OUT} tends toward V_{DD}, logic 1. Upon the onset of inversion, the switching transistor changes from the off-state to the on-state. As the switching transistor turns on, the resistance of the switching transistor becomes comparable to and then much less than that of the load transistor, causing V_{OUT} to be pulled to ground, logic 0. Fig. 2.12 shows the transfer characteristics of the inverter at $V_{\mathrm{DD}} = 2\,\mathrm{V}$ as well as an optical image and circuit schematic of the device. The contact pads have been labeled for convenience. It should be noted that the purpose of the V_{TUNE}

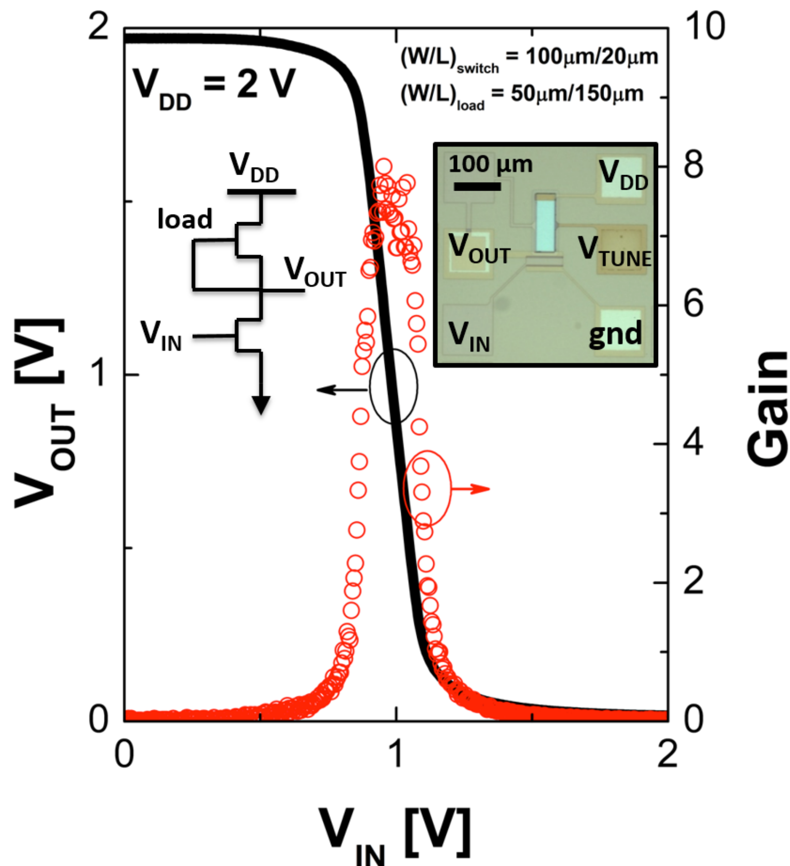


Figure 2.12: Voltage transfer curve (V_{OUT} vs. V_{IN}) and DC gain ($|\partial V_{\mathrm{OUT}}/\partial V_{\mathrm{IN}}|$) of the all-oxide NMOS inverter on polyimide under an operation voltage $V_{\mathrm{DD}} = 2\,\mathrm{V}$. The switching transistor has a $W/L = 100\,\mu\mathrm{m}/20\,\mu\mathrm{m}$, and the depletion-mode load transistor has a $W/L = 50\,\mu\mathrm{m}/150\,\mu\mathrm{m}$. Inset is a schematic representing the device layout as well as the corresponding optical image of the device with labeled contacts.

pad is to adjust the V_t of the load transistor so that it serves as a resistive load device. Also plotted is the DC gain of the inverter, defined as $|\partial V_{OUT}/\partial V_{IN}|$, which is shown to reach ≈8. Additionally, the noise margins of the inverter were extracted from the transfer curve by taking the maximum low input voltage (V_{LI}) and the minimum high input voltage (V_{HI}), corresponding to the input voltages at unity gain, and the corresponding output values of those inputs, V_{HO} and V_{LO}, respectively. The high and low input noise margins are then defined as $NM_H = V_{HO} - V_{HI}$ and $NM_L = V_{LO} - V_{LI}$, respectively. The noise margin values were calculated as $NM_H = 0.36\,V_{DD}$ and $NM_L = 0.33\,V_{DD}$.

2.7 Conclusion

2.7.1 Summary

In conclusion, a filtered cathodic arc deposition technique is demonstrated for room temperature deposition of intrinsic ZnO with electrical and optical quality suitable for transparent transistor applications. Additionally, this method of ZnO deposition has been shown to be usable in the fabrication of all-oxide fully transparent transistors on alkalki-free glass and polyimide with comparable or better electrical performance to alternative TFT platforms and existing oxide TFTs. Bending studies were performed to show the mechanical robustness of the device structure to confirm its potential use on flexible substrates. Additionally, further processing shows the material from cathodic arc deposition can be used for digital logic by creating a working inverter gate entirely out of oxides. Overall, this work demonstrates a low temperature fabrication process for ZnO TFTs enabling use in both fully transparent and flexible electronic applications.

2.7.2 Future Work

In future work, such a process could be ported to other flexible plastics with much lower thermal budget than polyimide, such as PET or PEN. Device performance improvements can be achieved by creating better channel-oxide interfaces and decrease series resistance issues, which will help with the gate control of the device and boost device mobility and on/off ratio. Additionally, lower temperature gate oxides via ALD or solution processing will be explored to lower the processing temperature to its lowest limit of 90 °C, as determined by photolithography. Previous research by colleagues should be noted for the development of an e-skin platform based on carbon nanotubes [35, 58, 59], which requires uniform TFTs for pixel backplane addressing as well as large-scale digital circuits for on-chip pixel addressing and simple data manipulation. Continued development of this ZnO device platform will enable use in future e-skin applications as an emerging flexible, large-area systems for backplanes and circuits on various flexible substrates.

Chapter 3

Silicon Transistor-Based Gas Sensors

3.1 Existing Carbon Monoxide Sensing Technology

CO is a prevalent pollutant gas that, in higher concentrations, is known to have immediate lethal effects. The danger of CO exposure is related to both the present CO concentration and exposure time. For example, according to Fig. 3.1, exposure to a CO concentration of 200 ppm for one hour is barely perceptible, whereas exposure to the same concentration over the course of eight hours can be lethal [60]. The variation in both gas concentration and exposure time shapes the sensor design space needed to appropriately detect or monitor CO gas.

For pollutant levels of CO, the minimum detection limit is close to ∼10 ppm, representing the maximum eight hour exposure limit for sensitive people groups (i.e., people with respiratory issues or those of old age) as determined by NAAQS [13]. Traditionally, metal oxide semiconductor (MOS) sensors suffer from high detection limit or require high temperature operation (≥200 °C) to detect low gas concentration values, making them good candidates for in-home detection of dangerous levels of CO but not for remote/mobile applications for consumer electronics requiring low power operation [61]. Electrochemical (EC) sensors are known for their high sensitivity and low power operation, enabling their integration into existing home monitoring electronics, but the physical form factor requiring a chamber with electrolyte solution does not allow for IC chip-level integration for mobile applications. Optical-based methods of detection such as photoionization detectors (PID) and non-dispersive infrared (NDIR) sensors have their respective gas concentration operation regimes but similarly suffer from scalability. Fig. 3.2 indicates general concentration ranges of various sensor types along with approximate gas concentration ranges for atmospheric air, work space environments, and exhaust gases.

With a target of on-chip integration for our gas sensor technology, the main issues of scalability, temperature operation, detection dynamics (including lowest detection limit and response/recovery time) need to be addressed. To accomplish this, we focus on the integration of MOS sensor capability into existing fabrication processes. More specifically,

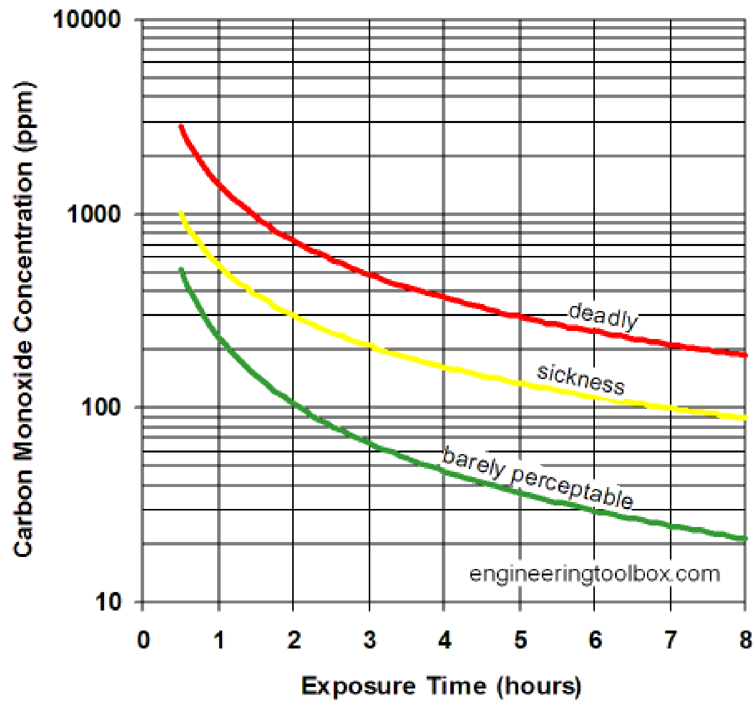


Figure 3.1: Health effects of CO exposure as a function of exposure time and CO concentration [60].

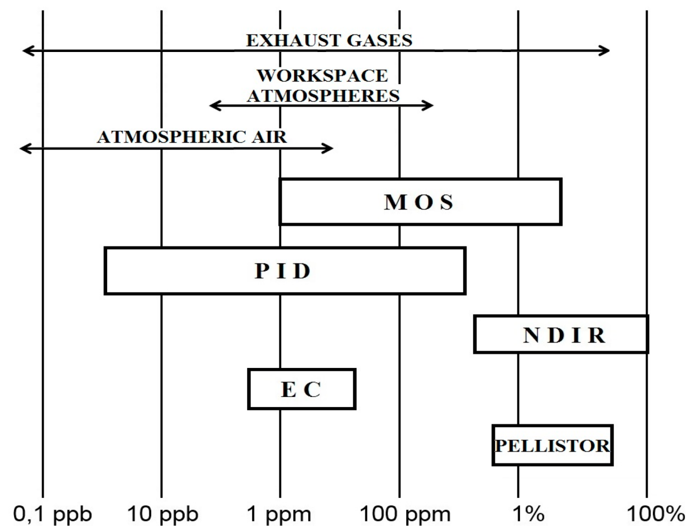


Figure 3.2: Gas sensor types as a function of detection range and corresponding atmospheric and workplace concentrations [61].

the application of metal oxides to existing transistor fabrication processes allows for direct integration of gas sensors into a chip-level package for mobile sensing.

3.2 Chemical-Sensitive FET

The development of a Si transistor-based gas sensor, referred to as a chemical-sensitive field effect transistor (CS-FET), replaces the gate oxide and metal gate elements of a transistor with a material that is chemically sensitive to a target gas, creating a traditional MOSFET that experiences current modulation via a chemically-induced process rather than a pure electrostatic potential [62]. Integrating the known low power operation and exponential current change of transistors along with the capability of metal oxide-based CO sensing provides a unique sensor design architecture allowing for high sensitivity detection at lower temperatures than existing MOS-based sensors.

3.2.1 Device Fabrication

The CS-FET design implements an ultra-thin body (UTB) Si-on-insulator (SOI) junctionless n-type transistor, with its gate stack replaced with chemically sensitive materials. Initially a 70 nm SOI wafer was thinned to a target of ∼5 nm via a dry/wet/dry oxidation process (1000 °C in atmosphere ambient) and subsequent oxide stripped by hydrofluoric acid (HF) solution. The remaining Si was then n^+-doped by spin-on phosphosilicate glass (PSG) deposition, dopant drive-in and activation anneal (960 °C for 5 s) with remaining PSG stripped by HF. Strips were then patterned into the wafer using standard i-line photolithography and anisotropic TCP dry etching. Ni source and drain contacts (50 nm) were patterned via an i-line liftoff process and annealed at 350 °C for 1 min to form nickel silicide (NiSi). Microheaters, which can be used for on-chip heating or pulsed desorption of gases to "reset" the CS-FET, are also formed by an i-line liftoff process of 20 nm Cr followed by 400 nm Au. Sensing materials can then be deposited by thermal or electron beam evaporation techniques to form the chemically-sensitive gate stack. Fig. 3.3 shows schematics, optical images, and cross-sectional transmission electron microscopy (TEM) images of a CS-FET functionalized with Pd/Au for hydrogen sulfide (H_2S) sensing [62].

3.2.2 Device Operation

CS-FET operation is based on traditional MOSFET operation in the subthreshold regime, allowing for exponential changes in current with a small change in potential at the gate material. Again, CS-FET utilizes a chemical-sensitive gate rather than an electrostatic contact, with the underlying gate dielectric simply being the native SiO_2 layer on the UTB Si strips, to achieve carrier modulation in the channel. CS-FET devices are biased with some voltage, V_{DS}, which produces a source/drain current, I_{DS}, through the Si channel. As a gas is introduced near the CS-FET, a change in I_{DS} occurs proportional to the concentration of the

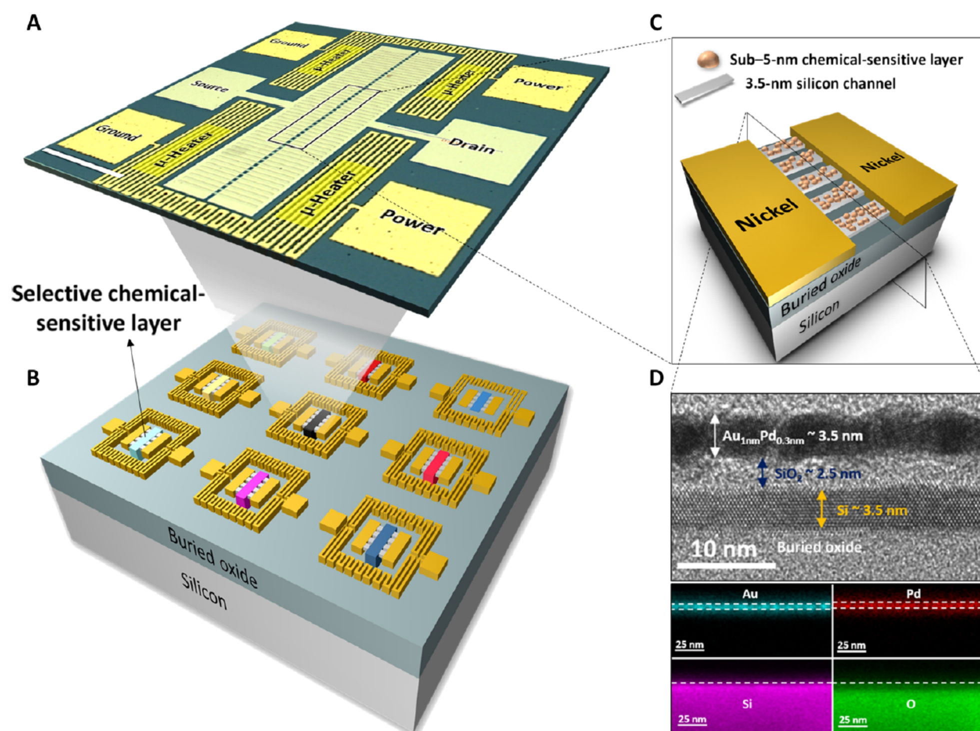


Figure 3.3: (a) Optical image of an individual CS-FET with Pd/Au sensing layer. (b) Schematic of example CS-FET chip array with different sensing layers. (c) Detailed schematic of an individual CS-FET. (d) Cross-sectional TEM image of CS-FET with associated energy-dispersive x-ray spectroscopy (EDS) [62].

gas. The mechanism for channel modulation can be the result of a change in work function of the sensing material or charge production via a chemical reaction. The effect the gas has on the change in I_{DS} current level—that is, whether I_{DS} increases or decreases—depends on the gas and its interaction with the sensing layer. Fig. 3.4 depicts the effect of H_2S exposure inducing an increase in work function of the sensing layer, shifting the V_{t} of the CS-FET, and thus increasing I_{DS} exponentially. It should be noted that, since this device is not a complete MOSFET structure due to the lack of gate metal contact, I_{DS}-V_{GS}-like characteristics are gathered by sweeping the bottom Si underneath the thick buried oxide layer, treated as a back gate and denoted V_{BS}, of the SOI wafer under different gas exposure conditions.

3.2.3 Personal Pollution Tracking

The overall vision of this project and sensing technology is the push for personal pollution tracking for mobile consumer electronics. Current methods of pollution tracking, such as those reported by government agencies and weather services, are based on stationary sensors that monitor a particular location. With a fully integrated mobile pollution tracking system, it will be possible for a user to monitor their own levels of pollutant exposure on a daily basis,

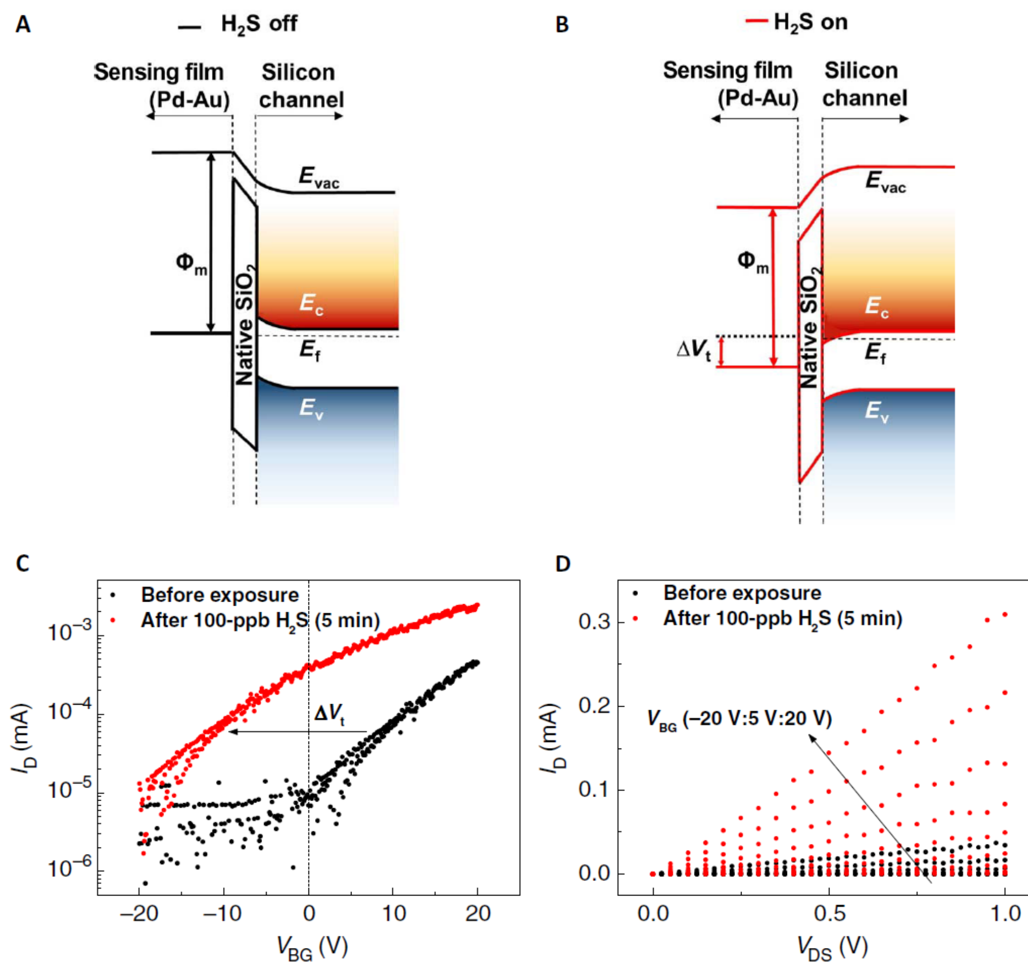


Figure 3.4: Schematics of the energy level alignments of the sensing layer work function, ϕ_{m}, vacuum energy level, E_{vac}, bottom of the Si conduction band, E_{C}, top of the Si valence band E_{V}, and the Si Fermi level energy, E_{F} before (a) and after (b) H_2S exposure. Experimental measurements of the CS-FET I_{DS}-V_{BS} (c) and I_{DS}-V_{DS} (d) before and after H_2S exposure [62].

which can in-turn be used for future health care data. As previously mentioned, this vision would be accomplished by fabricating arrays of micron-scale CS-FET devices, with different sensing layer materials per device, into a single sensing chip, allowing for the integration of small-scale sensors into existing mobile electronics such as mobile phones. This would enable selective sensing of individual NAAQS-recognized pollutant gases and provide real-time information on a person's exposure. Fig. 3.5 shows a conceptual schematic of the final project outcome.

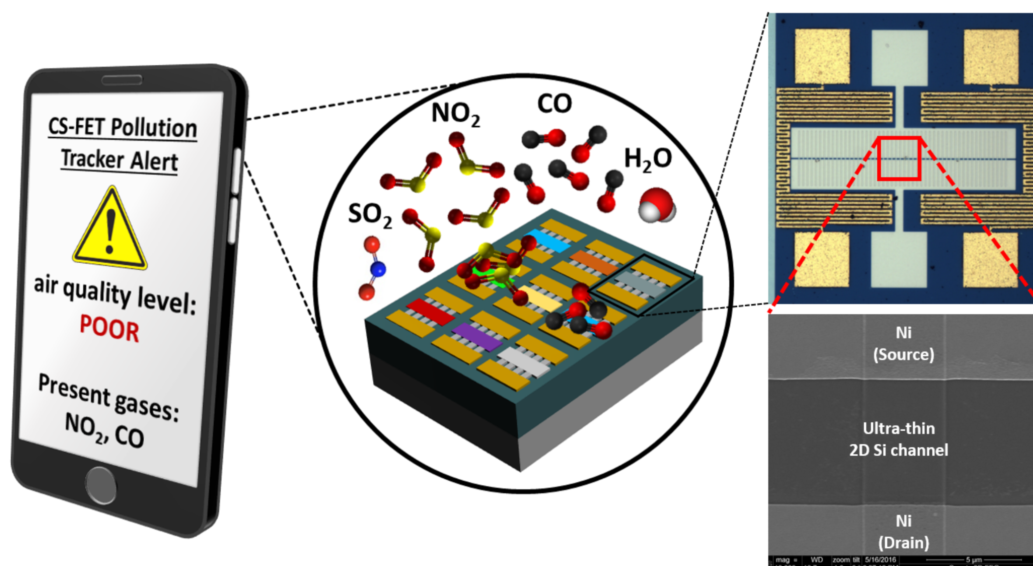


Figure 3.5: Conceptual schematic of a CS-FET array integrated into a mobile phone for personal pollution tracking.

3.3 CS-FET Carbon Monoxide Sensor

3.3.1 Materials Optimization for Peak Sensor Response

Metal Oxide Materials

The reaction of CO with heated metal oxide materials has been well-documented and is still used today for in-home MOS-type CO sensors, utilizing a heated tin oxide (SnO_2) current-carrying filament [63, 64]. Upon CO exposure, the resistance of the metal oxide changes based on the present concentration, enabling detection [65]. In addition to SnO_2, other metal oxide materials have been reported to have a response to CO exposure [64–70]. In order to screen for the material with the highest response when integrated with a CS-FET, we selected the following metal oxides for both room temperature and heated sensing tests for maximum CO response: WO_x, InO_x, AlO_x, SnO_x, and CeO_x. It should be noted that each of these materials was deposited by thermal evaporation with a target thickness of 1 nm, with such conditions typically producing substoichiometric oxide materials, denoted by the subscript "x" in each of the chemical formulas.

Sensor Response, Operation Temperature, and Platinum Catalyst Optimization

In addition to the well-documented reactivity of metal oxide materials with CO, the addition of noble metals such as Pt, Pd, and Au has been shown to increase sensor response when combined with metal oxide materials [71]. This is attributed to the "spillover effect" in which the presence of nanoscale noble metals increases the chemisorption of oxygen to the metal

oxide surface in the area surrounding the noble metal, acting as a catalyst for oxidation or reduction of a present gas [72]. For our CO sensors, we chose to implement Pt nanoparticles as our noble metal material, which was deposited by electron beam evaporation.

In order to produce nanoscale particles from evaporation, very thin layers of Pt were deposited such that the Pt could not appropriately wet onto the underlying oxide surface, causing the Pt particles to ball up. AFM images of a Si substrate exposed to this Pt evaporation, compared to a portion of the same sample that was covered with photoresist, can be seen in Fig. 3.6. Given the difficult nature of quantifying the density of Pt nanoparticles

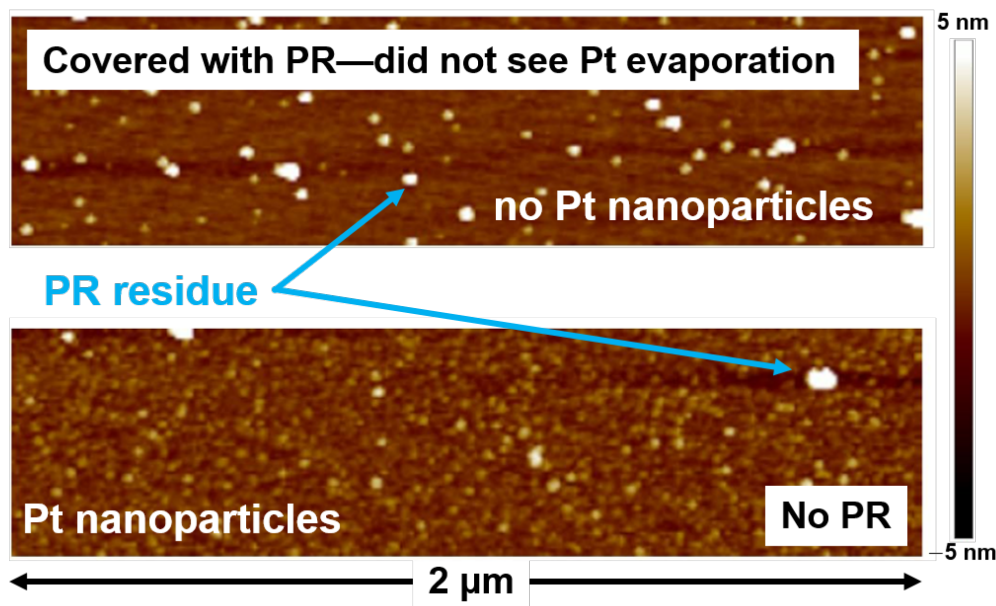


Figure 3.6: AFM images of Si samples exposed to 0.2 nm (as indicated by crystal monitor) Pt electron beam evaporation, resulting in Pt nanoparticles. A portion of the sample was covered in photoresist (PR) to prevent deposition (top), while the other portion was exposed to Pt evaporation, resulting in Pt nanoparticles (bottom).

deposited by evaporation, the amount of Pt was determined by the evaporation tool's crystal monitor. Using a very slow evaporation rate ($0.1\,\text{Å}\,\text{s}^{-1}$, also indicated by the crystal monitor) and depositing thicknesses that generate continuous films, we were able to calculate the true deposition rate. For Pt thicknesses that dewet from the underlying oxide surface producing nanoparticles ($<$1 nm), the total thickness of the deposition measured by the crystal monitor is used as an effective thickness, purely to describe the Pt nanoparticle density. Thus, a reference to a 0.2 nm Pt layer, for example, indicates the presence of Pt nanoparticles rather than a continuous 0.2 nm Pt layer.

To determine the metal oxide and Pt nanoparticle combination that produces the highest CO sensitivity, CS-FETs underwent 1 nm thermal evaporation of the aforementioned metal oxide materials, followed by a 0.2 nm Pt evaporation (as this thickness was confirmed via

AFM to produce Pt nanoparticles) (Fig. 3.7). Devices were then biased with a V_{DS} in the range of 100 mV to 5 V in order to produce a baseline current of $I_{DS} \approx 10$ nA, which was near the current noise floor of our measurement setup. To produce on-chip heating, the

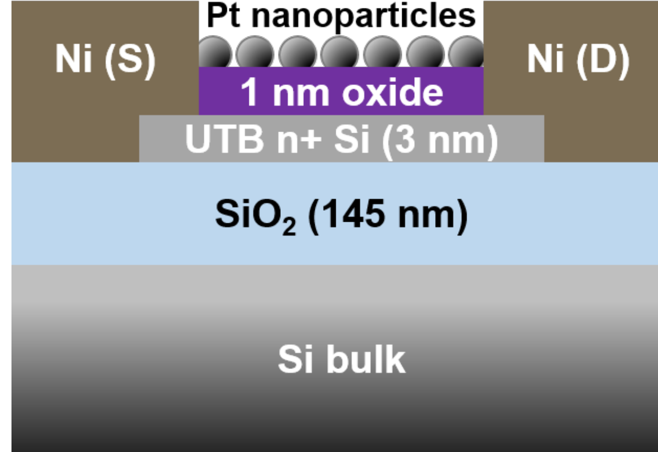


Figure 3.7: Cross-sectional schematic of the CO sensor CS-FET structure. For final device characterization, the 1 nm oxide layer is thermally evaporated WO_x.

CS-FET microheaters were biased to produce heat locally, with operation temperatures, $T_{operation}$ ranging from ∼55 °C to 95 °C. The maximum temperature was kept below 100 °C to minimize power consumption and thermal load. For devices being tested under room temperature operation, the microheaters were not used. The response of the sensor was characterized by comparing the percent current changes based on the individual devices' baseline currents, I_0, resulting in the following equation:

$$\text{sensor response} = \frac{\Delta I}{I_0} \tag{3.1}$$

where ΔI is the difference between the measured I_{DS} under gas exposure and I_0. Individual devices were exposed to 100 ppm of CO for 5 min at varied $T_{operation}$ values and their responses recorded. Fig. 3.8 shows the sensor response of each oxide CS-FET, along with a Pt-only device to indicate the presence of metal oxide is needed to produce a response. The device comprised of 1 nm WO_x + 0.2 nm Pt showed the highest response out of the screened materials, with a sensor response of nearly $\Delta I/I_0 \approx 80\%$ at a $T_{operation} \approx 95$ °C.

Next, we wanted to survey the sensor response of WO_x-based CS-FET CO sensors as a function of Pt thickness in order to optimize sensor response. This test was performed by fabricating devices with 1 nm WO_x by thermal evaporation and varied Pt thicknesses by electron beam evaporation, ranging from 0.1 nm to 1.2 nm. The tests were performed by exposing devices to 100 ppm CO for 5 min at both room temperature and $T_{operation} \approx 95$ °C (Fig. 3.9). The results indicates that sensor response, regardless of heating, decreases for Pt

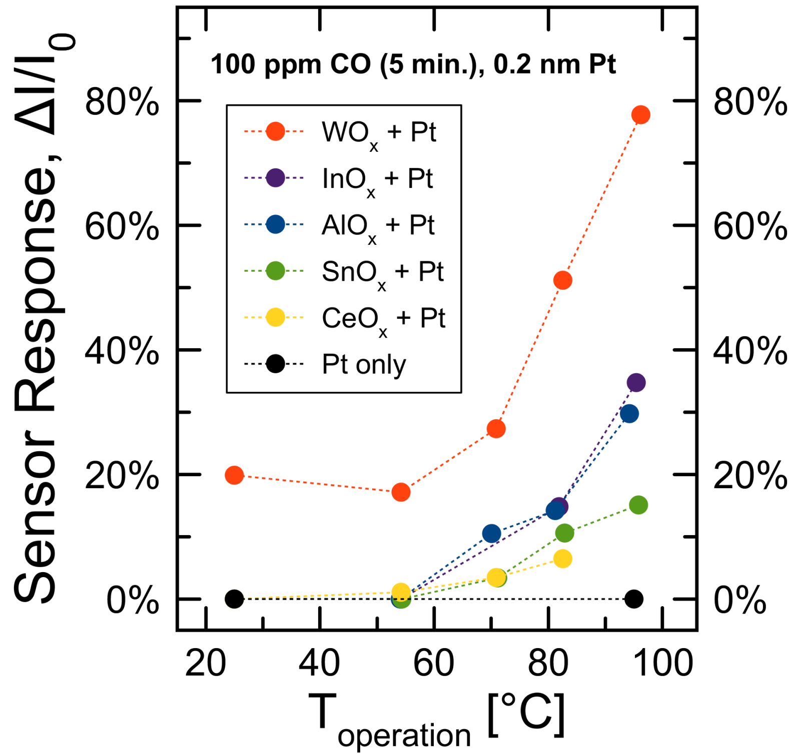


Figure 3.8: CO sensor response, $\Delta I/I_0$, as a function of operation temperature, $T_{\text{operation}}$ for different combinations of 1 nm thermally evaporated metal oxides and Pt nanoparticles.

layers > 0.4 nm. For room temperature operation, the peak average response is found to be for devices fabricated with 0.4 nm Pt, whereas the heated devices indicate a peak average response for 0.2 nm Pt. Ideally, the CS-FET-based CO sensors would be able to operate with minimal heating, ideally at room temperature with no heating, but we found that the batch-to-batch variation for such devices as the 0.4 nm Pt room temperature operation devices were too significant to reliably reproduce the sensor response. Therefore, further tests for dynamic sensing, such as varied CO concentrations and response/recovery times, were made using the sensor with the highest response that was able to be consistently reproduced both device-to-device and batch-to-batch: 1 nm WO_x + 0.2 nm Pt sensing layer at $T_{\text{operation}} = 95\,°\text{C}$.

On-Chip Microheater Temperature Calibration

The value of $T_{\text{operation}}$ is determined by the power dissipated by the on-chip microheaters. To determine this relation, the resistance of a fabricated microheater pattern was measured as a function of temperature and compared to the calculated resistance of the heater voltage supply conditions for the microheater for increasing values of applied heater voltage, V_{heater}.

To measure the change in microheater resistance as a function of temperature, fully-fabricated CS-FET devices were placed in an oven and electrically probed. The microheaters

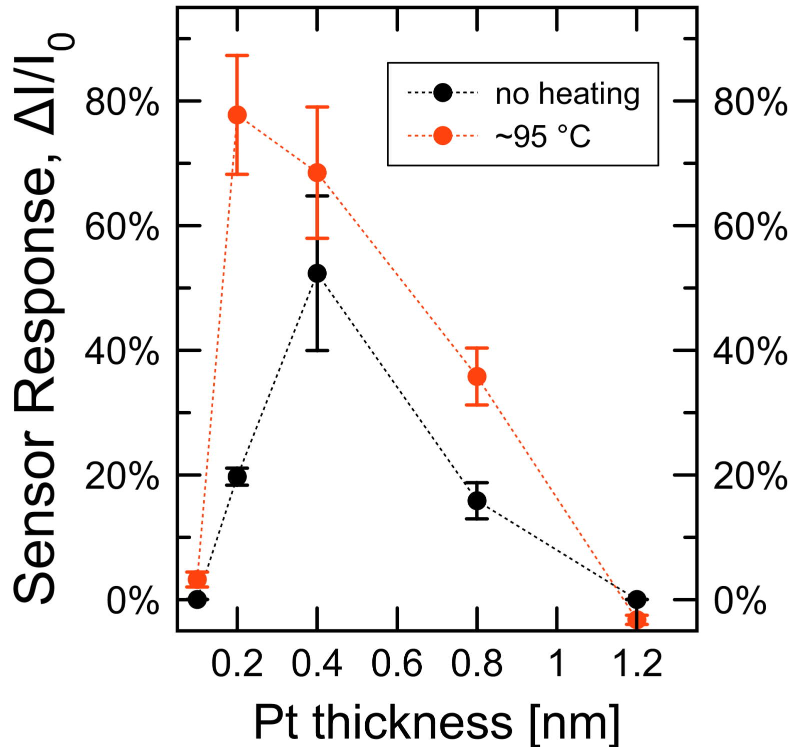


Figure 3.9: Room temperature and heated CO sensor response as a function of electron beam evaporated Pt thickness on a 1 nm WO_x layer. Devices were exposed to 100 ppm CO for 5 min.

were wire-bonded in a four-point-probe-style configuration to chip carrier contacts, which were then fed through the top of the oven and connected to a source-measure unit. The oven had a thermocouple placed near the CS-FET chip to monitor the internal temperature of the oven. The temperature of the oven was set to a a particular value, allowed to stabilize for 10 min, and the resistance of the microheater measured. The microheater was then subjected to a ±10 mA current stimulus, and its corresponding voltage drop, V_{sense}, measured, with the final resistance simply being the result of Ohm's Law: $R = V/I$. A linear approximation was then used to calibrate the resistance value as a function of surrounding temperature. Fig. 3.10 provides a schematic representation of the measurement setup and the resulting resistance vs. temperature plot for a microheater. The resistance of the microheaters was then remeasured using another on-chip microheater to provide the heating. This was accomplished by attaching a power supply to one microheater and varying V_{heater} from 1 V to 10 V in 1 V steps. For a given V_{heater}, a stabilization time of 10 min was used before probing the microheater resistance to avoid measurement errors due to temperature change. After temperature stabilization, the same four-point-probe-style measurements for determining the microheater resistance was used. Fig. 3.11 similarly shows a schematic representation of the

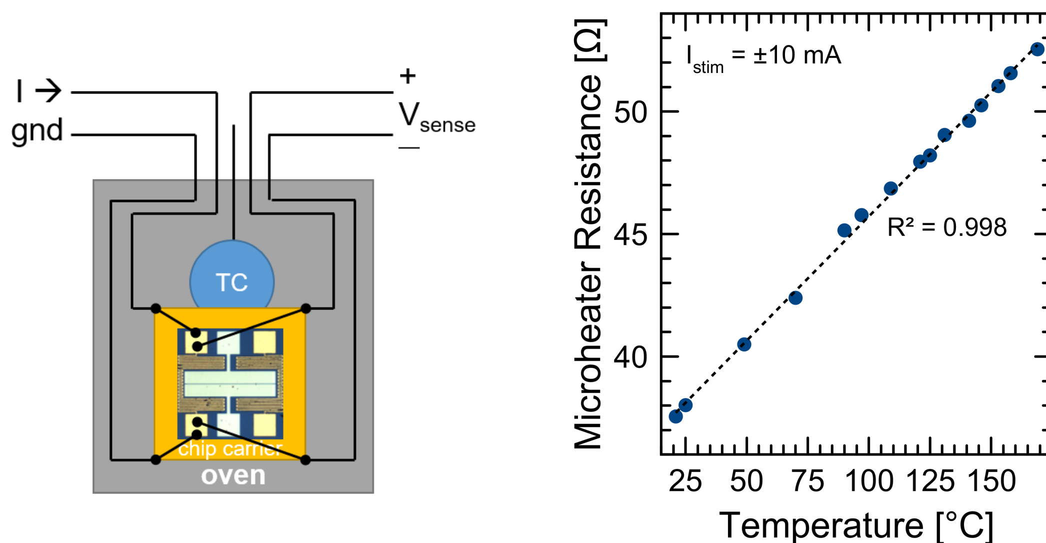


Figure 3.10: Schematic of microheater resistance measurement (left) and resulting resistance vs. temperature measurements and linear fit (right).

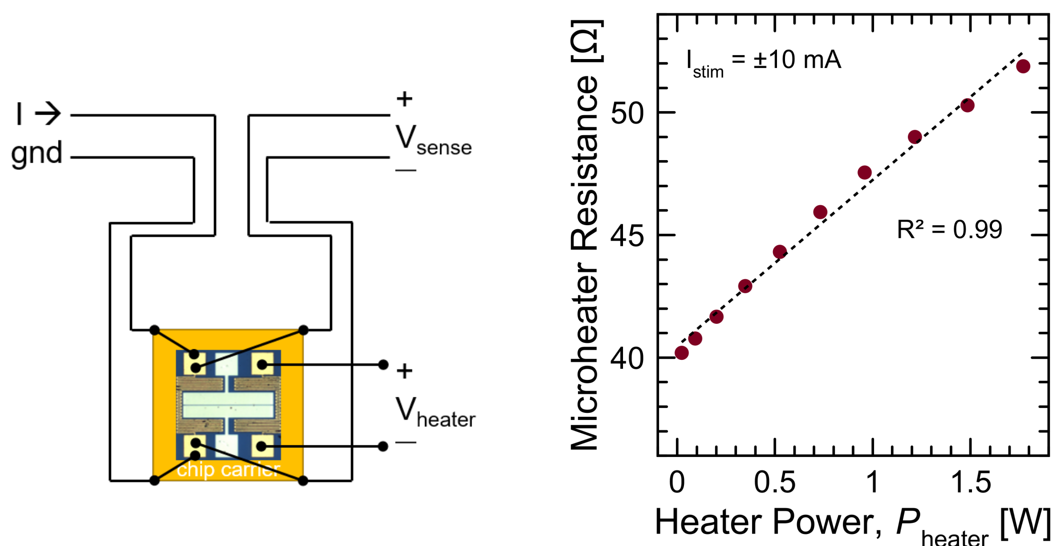


Figure 3.11: Schematic of microheater resistance measurement (left) and resulting resistance vs. heater power measurements and linear fit (right).

measurement setup and the measured microheater resistance as a function of applied microheater power (calculated using $P_{\text{heater}} = V_{\text{heater}}^2/R_{\text{microheater}}$) along with a linear fit approximation. By equating the fit lines from each of the resistance measurement experiments, we can approximate a heater power vs. temperature relation of $P_{\text{heater}}\,[\text{mW}] \approx 15\,T_{\text{operation}} - 723$.

3.3.2 CO Sensor Response

Full Range Measurement

Using the material structure and operation conditions previously described, the sensor response to varied levels of CO concentrations was characterized. The tests started with an initial concentration of 10 ppm, increasing to a peak concentration of 500 ppm, and decreasing back to 10 ppm, with all concentrations being exposed to the sensor for 10 min. Between each 10 min pulse of CO, the sensor was allowed to naturally recover to near baseline current before seeing a new pulse of gas. Each CO concentration was made by diluting a 500 ppm source bottle of CO with a dry air line. The sensor I_{DS} current was sampled every second and normalized to the average baseline current of the device in air from the hour before CO concentration tests. Fig. 3.12 shows the dynamic sensor response for these CO concentration tests, and Fig. 3.13 indicates the peak response for each CO concentration. The

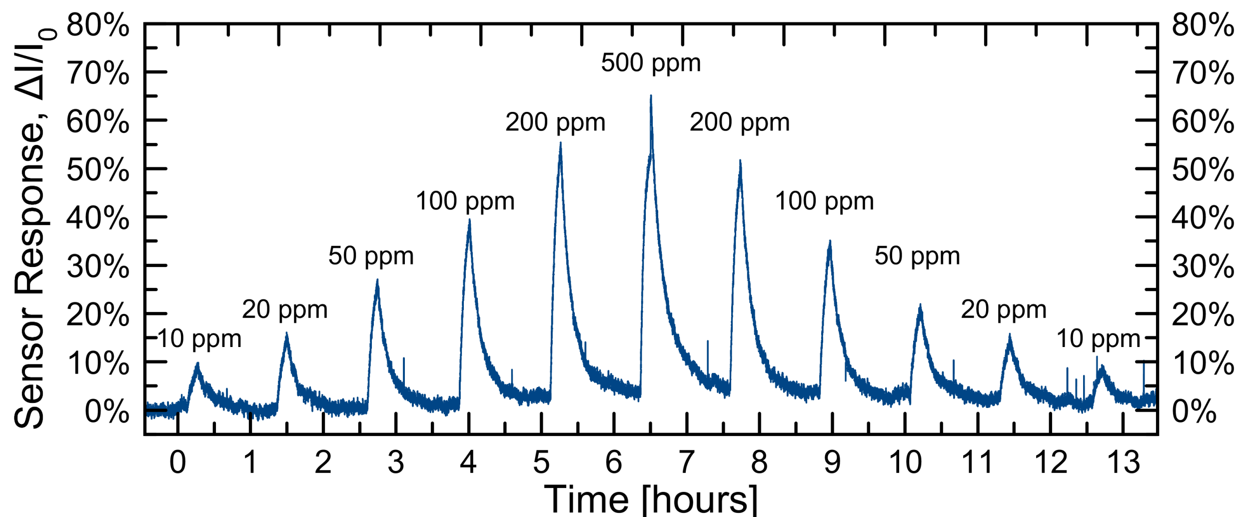


Figure 3.12: Full range dynamic CO sensor response from 10 ppm to 500 ppm for 10 min pulses at an operating temperature of $T_{\mathrm{operation}} \approx 95\,^{\circ}\mathrm{C}$.

sensor exhibits a response of nearly 10 % change from the baseline current upon exposure to 10 ppm CO, indicating the sensor can successfully respond to the NAAQS maximum eight hour secondary exposure limit of CO. With further optimization of the measurement setup, i.e., by reducing the noise floor, we suspect single digit concentrations of ppm-level CO can be easily detected, with further reductions in the noise floor potentially enabling ppb-level detection. As the CO concentration increases, the sensor exhibits a response logarithmic in nature, as indicated by the semi-log plot and dashed fit line in Fig. 3.13. Given the tested CO concentration range of 10 ppm to 500 ppm, initial evaluation confirms the ability to use this CS-FET CO sensor for monitoring levels of CO as well as concentrations near the PEL and higher, more-immediately-dangerous levels of CO—a good concentration range for mobile consumer electronics.

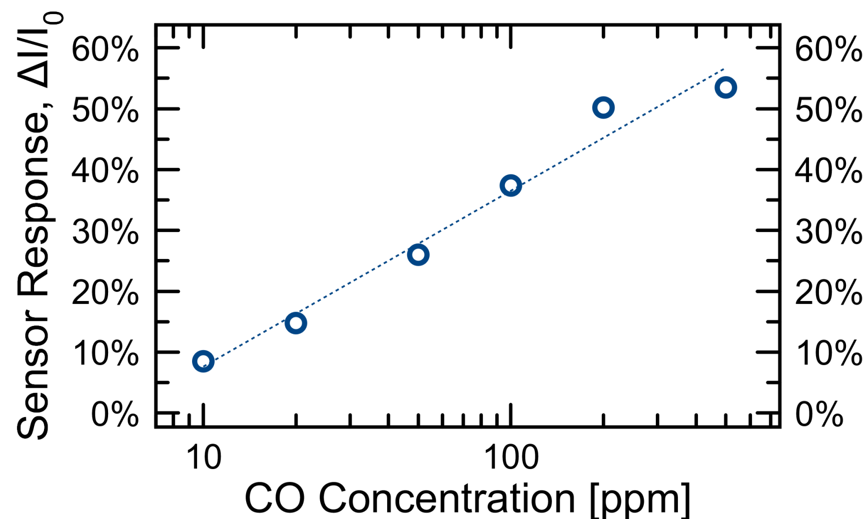


Figure 3.13: Peak sensor response as a function of CO concentration extracted from Fig. 3.12.

Response and Recovery Time

An important set of metrics for a gas sensor, especially those intended for safety-monitoring use, is the response and recovery time. For many gas sensors, these values are defined in reference to the peak response for particular concentrations. In terms of the CS-FET, we have chosen to define the response time as the amount of time to reach 90% of the peak response for a given concentration, $t_{90\%}$, and the recovery time as the amount of time needed to decrease to 50% of the peak response for the same concentration, $t_{50\%}$. In the case of a mobile pollution tracking system, the response and recovery times have more flexible constraints, as the user will most likely not be experiencing large, high-rate changes in ambient CO concentration. For our device, the $t_{90\%}$ response time is nearly constant for most CO concentrations, having times roughly in the range of 6.5 min to 7 min (Fig. 3.14). This behavior continues from 10 ppm to 200 ppm, with the response time of 500 ppm improving to ∼5.5 min. The increase in response time at 500 ppm may be attributed to the lack of setup-supplied dry air, as this CO concentration does not require any dilution from the source bottle. The $t_{50\%}$ recovery time has a wider range of values, with a minimum recovery time near 5.5 min at 10 ppm CO and slightly above 7 min for 500 ppm CO. The rough trend of increasing recovery times with increasing concentration is expected due to the WO_x/Pt surface becoming more saturated with increasing concentration, requiring more time to fully replenish CO-induced oxygen vacancies. (For a more detailed explanation of the proposed sensing mechanism, see Sec. 3.3.4.) Overall, the response and recovery times on the order of minutes is sufficient for small changes in local CO concentrations as well as for potentially more-dangerous levels ≥100 ppm.

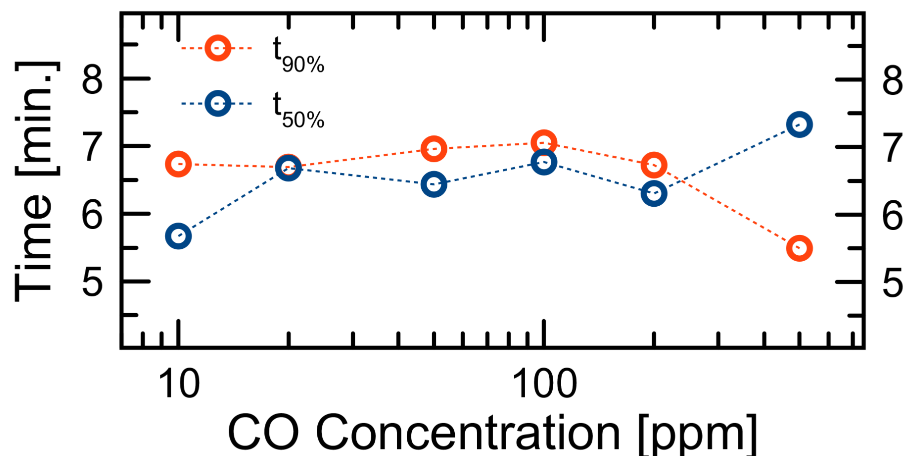


Figure 3.14: Response time, $t_{90\%}$, and recovery time, $t_{50\%}$, of the CO CS-FET as a function of exposed CO concentration (10 min).

Sensing Repeatability

The repeatability of a sensor is important for calibration of consistent, expected output response for a given gas concentration. To assess the repeatability, the CS-FET was exposed to eight consecutive 10 min pulses of 100 ppm CO, with sufficient time given between each pulse to recover to near-baseline. As shown in Fig. 3.15, the sensor response is suitably repeatable, with the difference in maximum and minimum responses being $\sim$3 %. Variations in the sensor response can be attributed to manually-induced error from CO exposure time on the order of seconds as well as effects from baseline drift, as these devices see constant V_{DS} and V_{heater} biases.

3.3.3 Sensor Selectivity

Selectivity to NAAQS Pollutants

In order for the CO CS-FET to be successfully integrated into an array of CS-FETs that detect different pollutant gases, it needs to have selective response to other gases that could be present. More specifically, in terms of NAAQS established pollutants, we have tested the CO sensor for selective response to SO_2 and NO_2 gases. Rather than a direct comparison of the same concentration of each gas, the concentration of the pollutants was adjusted to be more representative of concentrations one may expect in the ambient air and workplace. For CO, a concentration of 10 ppm was used, as this represents our target pollution tracking concentration. For SO_2 and NO_2, the chosen concentration of 5 ppm represents the PEL values for each gas. It should be noted that this an aggressive test of the CO sensor, as we have benchmarked high workplace concentrations of SO_2 and NO_2 against ambient CO concentrations affecting only sensitive people groups. The sensor response to 10 min of

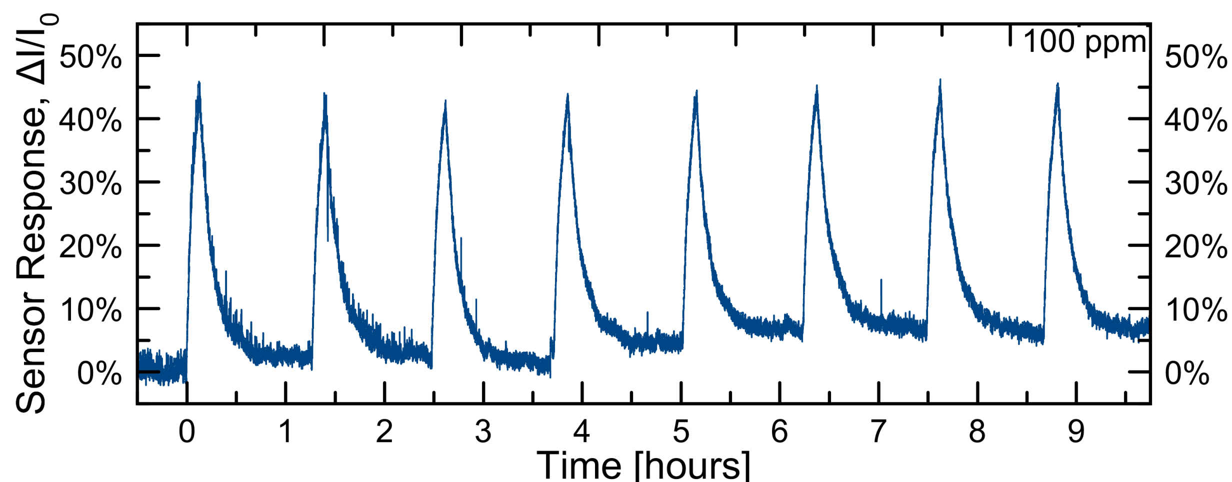


Figure 3.15: Dynamic response of the sensing repeatability of the CO CS-FET. The device was exposed to eight consecutive 10 min pulses of 100 ppm CO.

10 ppm CO was ∼8 %, which is consistent with previous measurements, while the response to 10 min of 5 ppm SO_2 and NO_2 was ∼−14 % and ∼−85 %, respectively (Fig. 3.16). While CO is commonly known as a reducing gas species, both SO_2 and NO_2 are know for being oxidizing gases, causing the sensor response to be negative. The −85 % response to NO_2 is

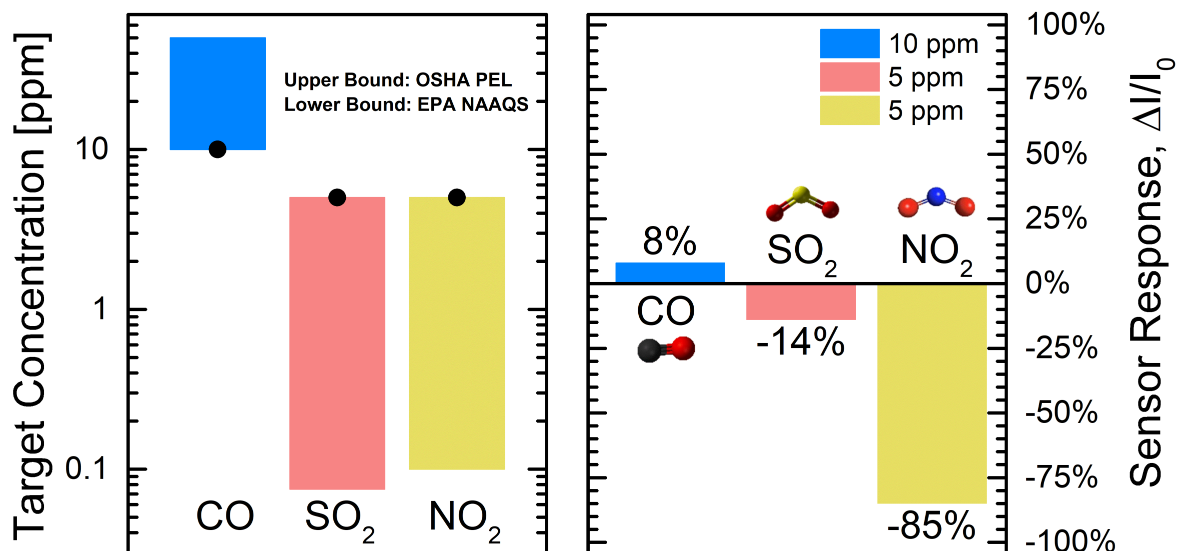


Figure 3.16: Target NAAQS gases for selectivity tests (left) and their corresponding CO sensor response after 10 min exposure (right). The dots on the target concentration graph indicate the tested pollutant gas concentrations of 10 ppm CO, 5 ppm SO_2 and 5 ppm NO_2.

not ideal, as this implies a mixture of CO and NO_2 will be difficult to selectively detect with a CO CS-FET. However, integration of the CO sensor in an array of sensors that include an NO_2 sensor that has both a stronger response to NO_2 and selectivity to CO will enable off-chip extraction of the present CO concentration.

Humidity Response

To ensure the CO sensing is, in fact, sensing CO, as well as to provide a window of operating conditions for the CO sensor, we measured the effect of CO sensing with changes in relative humidity. To increase humidity, the setup's dry air line was flown through a water bubbler, and a commercial humidity sensor was placed in the gas sensing chamber to quantify the relative humidity. The relative humidity of the chamber without additional moisture was 12 % due to the flowing of the dry air line in combination with the dry CO source cylinder. Fig. 3.17 shows the CS-FET response to 10 min exposure to 100 ppm CO for relative humidity values of 12 %, 56 % and 78 %. The sensor response to CO in the presence of moisture varies

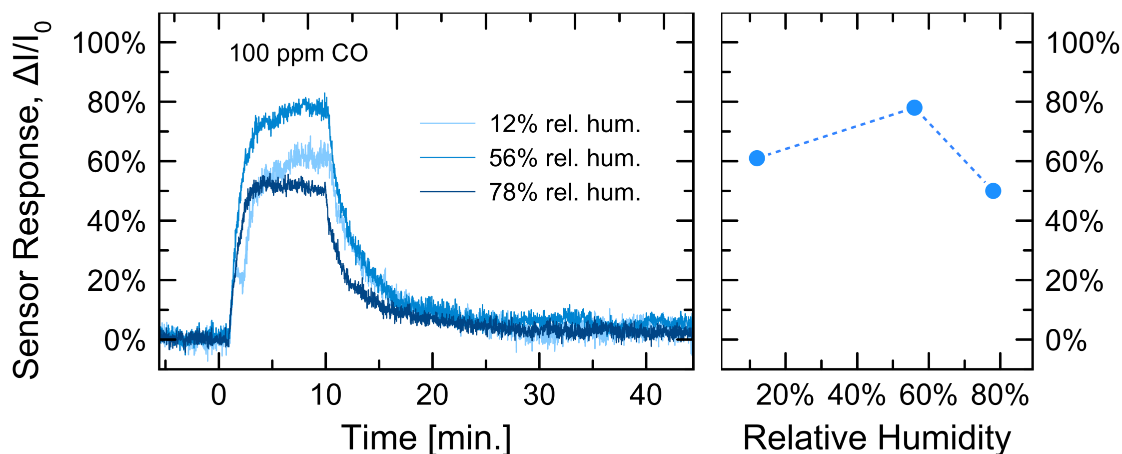


Figure 3.17: Dynamic sensor response to 100 ppm CO for 10 min in varied relative humidity levels of 12 %, 56 % and 78 % (left) and the corresponding peak sensor response for each condition (right).

from approximately 50 % to 80 %, while the CO response in a dry air ambient is ∼60 %. While it is clear the presence of moisture affects the sensor response for a particular CO concentration, the effect does not prevent CO sensing. Additionally, similar to the previously discussed integration of additional sensors, on-chip humidity sensors will allow for a similar off-chip extraction or calibration of the sensed CO concentration, allowing for more accurate and consistent measurements.

3.3.4 Proposed Sensing Mechanism

CO Oxidation on Noble Metal-Supported Oxides

The oxidation of CO to CO_2 via noble metal catalysts and underlying metal oxides with oxygen vacancies has been thoroughly studied [64, 65, 67, 68, 71–74]. Given the most commonly proposed methods of CO oxidation, we extrapolated these reactions to the sensing layer on our CS-FET device to describe the current response of the sensor—i.e., why the I_{DS} current increases for increased CO exposure.

Noble metal nanoparticles are known for the their ability to have gas molecules such as CO adsorb onto their surface as well as gather surround oxygen atoms close to the nanoparticle, the latter being an effect known as "oxygen spillover" [72]. Therefore the addition of Pt nanoparticles in our device provides for enhanced oxygen adsorption near the nanoparticle. Fig. 3.18 shows a close-up schematic of the WO_x + Pt sensing layer prior to any interaction with ambient O_2 or CO species and an accompanying energy band diagram of the WO_x layer. As a reminder, the tungsten oxide formula is written as WO_x to imply substo-

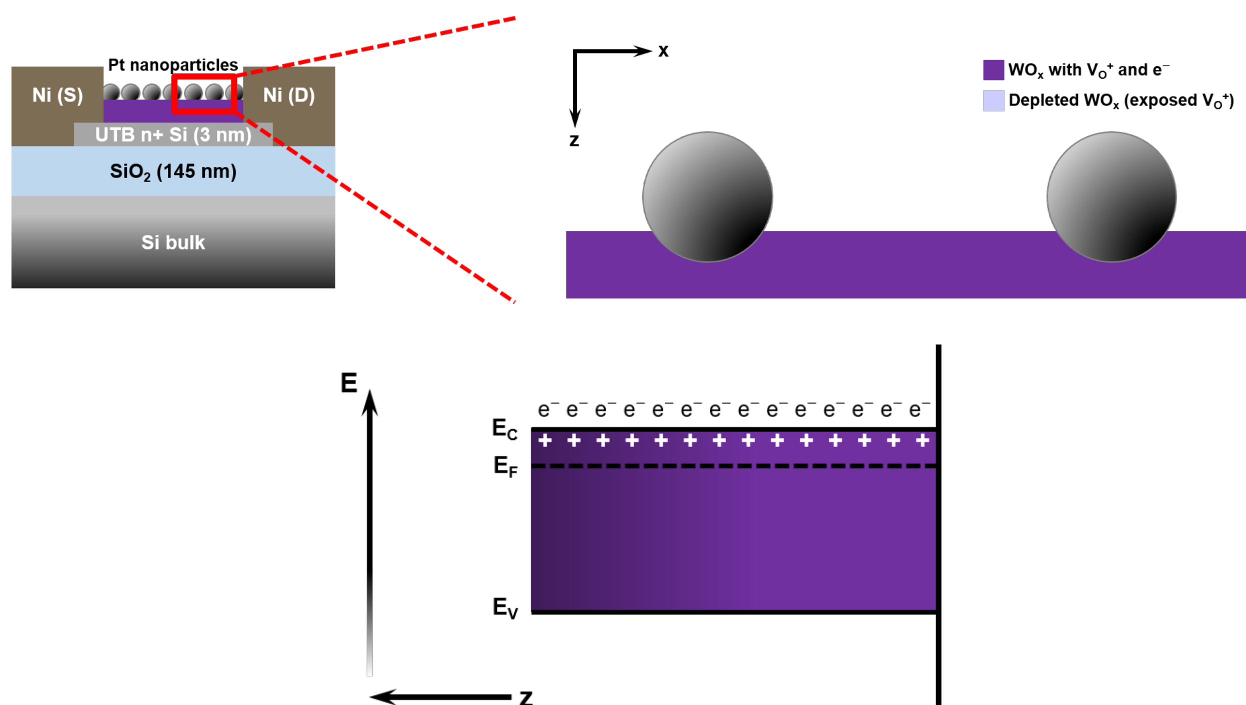
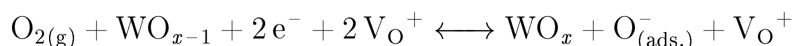


Figure 3.18: Enlarged cross-sectional schematic of the WO_x + Pt sensing layer (top) and corresponding energy band diagram of the WO_x layer (bottom). The dark purple indicates substoichiometric WO_x, and the silver spheres indicate Pt nanoparticles. In the energy band diagram, E_C, E_F, and E_V represent the conduction band minimum, Fermi level energy, and valence band maximum, respectively. Donor-like oxygen vacancies are represented by + symbols, and their corresponding free electrons indicated above as e^-.

ichiometry resulting from the thermal evaporation of the material. For many metal oxides, substoichiometry presents itself in the form of oxygen vacancies, denoted ${V_O}^+$. The +-sign represents the effect of missing oxygen lattice atoms acting as donor-like shallow dopants, providing electrons to the material and acting as a positive charge center. In the case of Fig. 3.18, the solid purple represents an as-evaporated WO_x layer, replete with both oxygen vacancies, ${V_O}^+$, and donated electrons from the vacancy, e^-. The Fermi level energy, E_F, is a result of the most energetically favorable concentration of vacancies for this material and deposition method, akin to the Fermi stabilization energy [75, 76].

Once O_2 gas is present and the oxide material is lightly heated based on $T_{\text{operation}}$, there exists another energetically favorable condition in which some of the oxygen vacancies on the WO_x surface are occupied by oxygen atoms from ambient gas. (It should be noted that a similar approach to this CO oxidation mechanism also incorporates water vapor, but this is not addressed in this proposed mechanism.) This reaction can be described as follows:



$$O_{2(g)} + WO_{x-1} + 2\,e^- + 2\,{V_O}^+ \longleftrightarrow WO_x + O^-_{(ads.)} + {V_O}^+$$

where oxygen atoms form the present O_2 gas fill an oxygen vacancy (denoted via an increase in the WO_x stoichiometry from "x−1" to "x" and reduction in ${V_O}^+$), leaving behind a negatively-charged surface-adsorbed oxygen atom, $O^-_{(ads.)}$. The negative charge results from the free electrons filling the orbital of the adsorbed oxygen atom. This reaction results in an oxygen vacancy being filled, but at the same the free electrons moving to the adsorbed oxygen depletes the surface of electrons, causing a ${V_O}^+$ charge center to be exposed. This effect is shown in Fig. 3.19, where adsorbed O^- species expose a positive depletion charge.

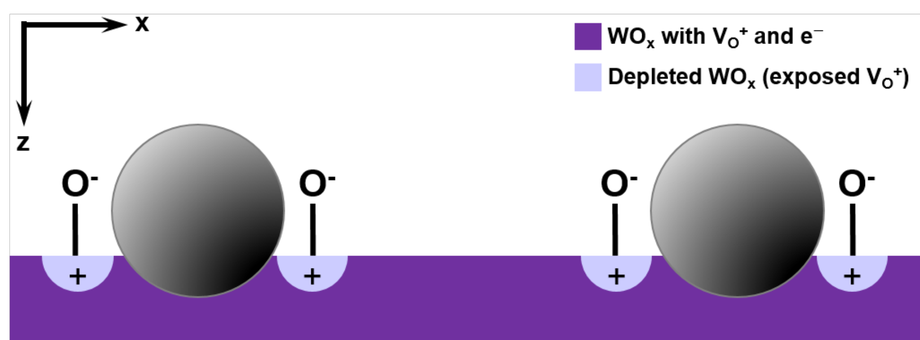
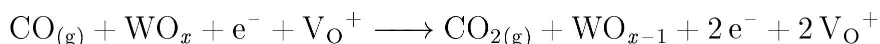


Figure 3.19: Cross-sectional schematic representation of the adsorption of oxygen atoms onto the surface of WO_x. Oxygen atoms become negatively-charged due to orbital filling by free electrons produced from oxygen vacancies. This negative surface charge locally depletes the WO_x (light purple semicircles), creating a positive space charge region of donor-like oxygen vacancies.

Upon exposure to CO, which adsorbs onto the Pt nanoparticle, the WO_x layer gives up an oxygen atom to assist in the oxidation of CO to CO_2, resulting in yet another oxygen vacancy. This reaction can be described as follows:



$$CO_{(g)} + WO_x + e^- + {V_O}^+ \longrightarrow CO_{2(g)} + WO_{x-1} + 2\,e^- + 2\,{V_O}^+$$

where the stoichiometry of the WO_x decreases and the number of oxygen vacancies increases, providing more free electrons [69]. Therefore, with increased CO presence by means of increased exposure time or increased CO gas concentration, the number of produced ${V_O}^+$ sites continues to increase. This, in turn, allows for more present O_2 molecules to follow the previous reaction, providing more negatively-charged $O^-_{(ads.)}$ species that deplete more of the surface, providing additional positive charge. A visual schematic and band diagram representation of this effect is shown in Fig. 3.20. Combining these two reactions forms

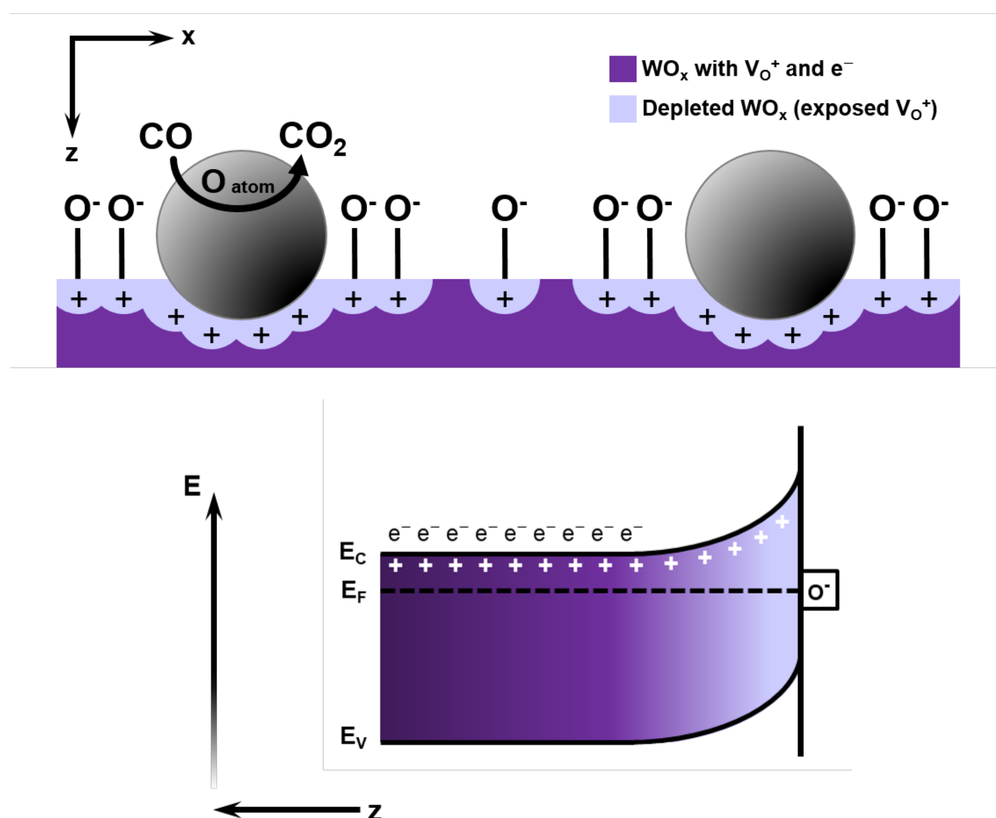
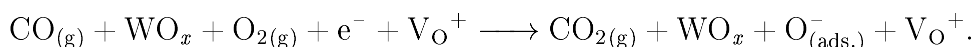


Figure 3.20: Cross-sectional schematic representation of the CO-induced increase of negatively-charged oxygen adsorption on the surface of WO_x (top) and an accompanying energy band diagram of the WO_x depicting surface depletion (bottom). As the CO oxidation creates more oxygen vacancies, more oxygen atoms adsorb and attract free electrons, depleting the surface of electrons and uncovering more depletion charge sites.

the overall chemical equation of CO oxidation by means of oxygen vacancy donation, and subsequent filling of the oxygen vacancy resulting in positive surface charge, as follows:



$$CO_{(g)} + WO_x + O_{2(g)} + e^- + {V_O}^+ \longrightarrow CO_{2(g)} + WO_x + O^-_{(ads.)} + {V_O}^+.$$

Sensor recovery can then be described as energetic relaxation to the originally favorable configuration, as illustrated in Fig. 3.19.

I_{DS}-V_{BS} of CS-FET under CO Exposure

Due to the generation of positively-charged depletion regions of exposed V_O^+ sites, an increase in CO concentration results in an increase of positive charges on the "gate stack" of the CS-FET, providing a positive bias to the transistor. This effect can be seen in Fig. 3.21, which shows schematic representations of the increase in positive gate charges upon CO exposure as well as experimental demonstration of a CS-FET I_{DS}-V_{BS} plot before and after 100 ppm CO exposure. It can be clearly seen that the I_{DS} current increases upon CO expo-

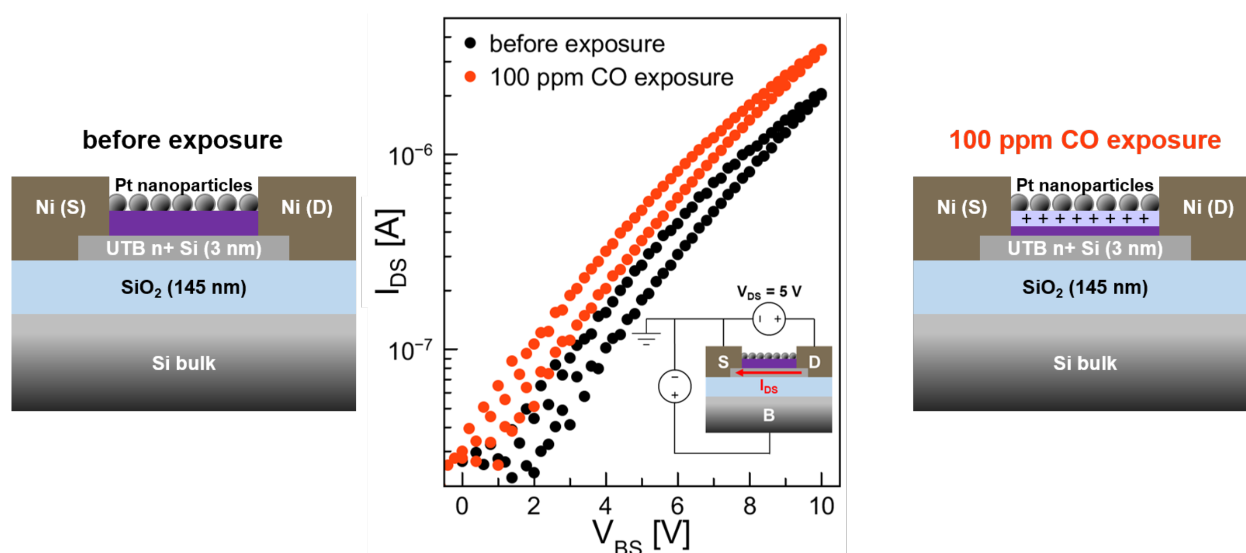


Figure 3.21: Cross-sectional schematics of the WO_x + Pt CS-FET before CO exposure (left) and after 100 ppm CO exposure, creating depletion charges (right). Experimental I_{DS}-V_{BS} curves before and after CO exposure indicate a shift in the I_{DS}-V_{BS} curve due to the presence of positive charges (center).

sure, which is indicative of the presence of positive charges on the surface of the WO_x layer. An n-type FET sees an increase in current with an increase in positive bias on the gate, thus a shift left in the corresponding CS-FET I_{DS}-V_{BS} curve indicates higher current values are being reached at a lower V_{BS} voltage, implying additional positive bias is being applied. The observed hysteretic switching behavior can be attributed to the interaction of present water vapor with the exposed metal oxide film.

3.4 Summary

3.4.1 Conclusion

Utilizing the CMOS-compatible CS-FET structure and known CO gas interaction with metal oxide and noble metal systems, we were able to demonstrate detection as low as 10 ppm of CO at device operating temperatures ∼95 °C. Lower concentrations are believed to be able to be detected with noise-reduction of the sensor measurement setup. The sensor response and recovery times were both in the 5.5 min to 7.5 min range—sufficient for all-day monitoring of local user pollution levels. The CS-FET exhibited repeatable sensing characteristics, minimal change in sensor response in the presence of large humidity changes, and partial selectivity to other pollutant gases. The mechanism for CO sensing and subsequent device I_{DS} current increase is proposed: CO oxidizes to CO_2 via oxygen atoms from the WO_x layer, and Pt-enhanced oxygen adsorption depletes the surface of carriers, exposing donor-like oxygen vacancy charge centers. This is supported by I_{DS}-V_{BS} measurements of the CS-FET before and after CO exposure. To the best of our knowledge, this represents the first demonstration of a fully-CMOS-compatible transistor-based CO sensor and one of the lowest operation temperature for CO sensing with MOS-type structures for ∼10 ppm CO concentrations.

3.4.2 Future Work

In the future, work must be done to optimize the Pt nanoparticle deposition, as it has been shown that CO adsorption can be increased by utilizing certain facets of a noble metal crystal [74]. Additionally, with further optimization of the sensing layer it may allow for even lower temperature operation, reducing power consumption. Other methods of power consumption reduction to be explored include pulsed measurements and pulsed heating of the device—all measurements of this sensor were under constant V_{DS} and heat. By evaluating the sensor response to well-timed samples of I_{DS} current for low duty cycle higher voltage heater bias pulses, it may be possible to obtain similar levels of CO detection with a decrease in average power consumption. Lastly, to realize the personal pollution tracker project, the CO CS-FET can be integrated with existing SO_2 and NO_2 CS-FETs for individual monitoring of pollutant gases.

Chapter 4

Tilted Ion Implantation for Nanoscale Patterning

4.1 Introduction

Incremental reduction of the minimum size and pitch of features in state-of-the-art integrated circuits (ICs) to allow for improvements in chip functionality and cost has driven the need to improve the resolution of IC-layer patterning techniques [77]. Photolithographic approaches using conventional deep ultraviolet (DUV) light sources require multiple exposures for a single photoresist layer (DEL) or multiple lithography+etch sequences (LELE) to achieve sub-90 nm pitch, with significant incremental cost associated with specialized resists and multi-mask alignment processes [78–81]. The development of extreme ultraviolet (EUV) light sources is aimed to improve the resolution of photolithography, alleviating the need for the aforementioned "multiple patterning" approaches, but is limited by throughput and post-development resist fidelity [24, 81, 82]. Alternative approaches such as spacer-based pattern splitting and directed self-assembly (DSA) of diblock co-polymers have been developed to increase the density of patterned features beyond the limits of photolithography; today spacer-based self-aligned double and quadruple patterning (SADP, SAQP) are used in high-volume manufacturing [83–89].

Recently it was shown that tilted ion implantation (TII) is an effective and lower-cost method for achieving features with linewidth and pitch smaller than that of preexisting masking features on the surface of a wafer [90–92]. Specifically, the masking features protect portions of an underlying SiO_2 layer from the TII, preventing damage that locally enhances the wet etch rate. The implanted portions of the SiO_2 layer are selectively removed, for positive-tone patterning [93]. In this work, silicon anti-reflection coating (SiARC) materials are investigated as an alternative to SiO_2 to achieve negative-tone sub-lithographic patterning using TII. Unlike SiO_2, SiARC films are spin-coated and contain organic functionalities that offer tunable film composition. Additionally, to further demonstrate the advantages of TII as a sub-lithographic patterning technique, Monte Carlo simulations of multiple lithog-

raphy+TII sequences to form two-dimensional (2D) patterns are presented. Specifically, two orthogonally masked TII steps are used to define sub-10 nm 2D patterns with high fidelity. The repeatability and tolerance to lithographic misalignment of this patterning approach, in addition to a Boolean method of selective patterning, are assessed.

4.2 Positive-Tone vs. Negative-Tone TII Patterning Process

The process steps for both positive-tone patterning, using SiO_2, and negative-tone patterning, using SiARC, are illustrated in Fig. 4.1. For both processes, a pre-existing mask (e.g., comprising photoresist) is used to shield portions of the TII layer from implantation. The key difference in these processes is that the implanted SiO_2 regions are removed (positive-tone), whereas the implanted SiARC regions remain after etching (negative-tone), as seen in steps 3 and 4 of Fig. 4.1. Note that for negative-tone patterning, the pre-existing mask should be removed prior to etching of the TII layer, so that the non-implanted SiARC region under the pre-existing mask features will be removed in the same etch step. Once the TII layer is etched, its resulting pattern can be transferred to the underlying IC layer.

4.3 Implantation-Induced Change in SiARC Wet Etch Rate

4.3.1 SRIM Simulations of SiARC Implantation

Negative-tone patterning is achieved by hardening the SiARC with ion implantation. To study the effect of implantation, using the concentration of vacancies as a proxy, simulations of TII into a 15 nm SiARC film on a Si substrate were performed using the Stopping and Range of Ions in Matter (SRIM) software package [94]. Fig. 4.2 shows the vacancy concentration depth profile caused by a 3 keV Ar^+ implant at a tilt angle of 15°, for Ar^+ doses of $3 \times 10^{14}\,\mathrm{cm}^{-2}$, $6 \times 10^{14}\,\mathrm{cm}^{-2}$ and $9 \times 10^{14}\,\mathrm{cm}^{-2}$. The lowest dose of $3 \times 10^{14}\,\mathrm{cm}^{-2}$ was chosen such that the peak damage concentration was $\sim 10^{22}\,\mathrm{cm}^{-3}$, which is greater than 10% of the atomic density of the SiARC, as previous experimental results indicate the onset of the wet etch rate of Ar^+-implanted SiO_2in dilute hydrofluoric acid (HF) solution to consistently occur at $\sim 3 \times 10^{21}\,\mathrm{cm}^{-3}$ [93]. Thus, the SRIM simulations used dose values such that the implant-induced vacancy concentration, serving as the quantification of damage, was maintained at this value throughout most of the SiARC film.

4.3.2 Wet Etching of Implanted SiARC Films

To study the effect of Ar^+ implantation on SiARC wet etch rate, samples were prepared by spin-coating the SiARC material onto Si wafers, followed by a 220 °C bake in air, resulting

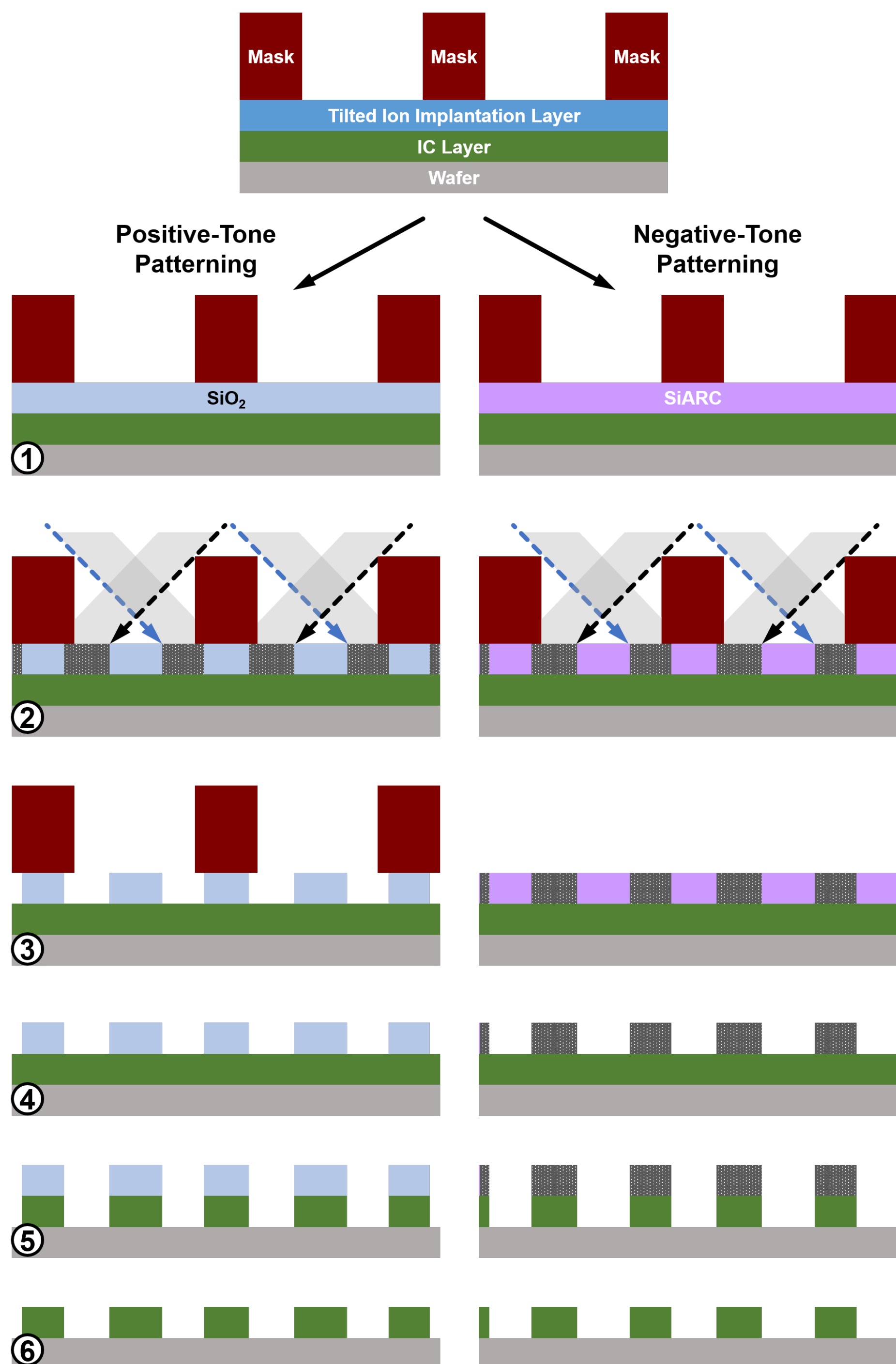


Figure 4.1: Process flow for positive-tone and negative-tone TII patterning: 1) SiO_2 TII layer for positive-tone, SiARC TII layer for negative-tone, 2) two TII steps to halve pitch, 3) etch TII layer (positive-tone) and remove mask (negative-tone), 4) remove mask (positive-tone) and etch TII layer (negative-tone), 5) etch underlying IC layer, 6) remove TII layer.

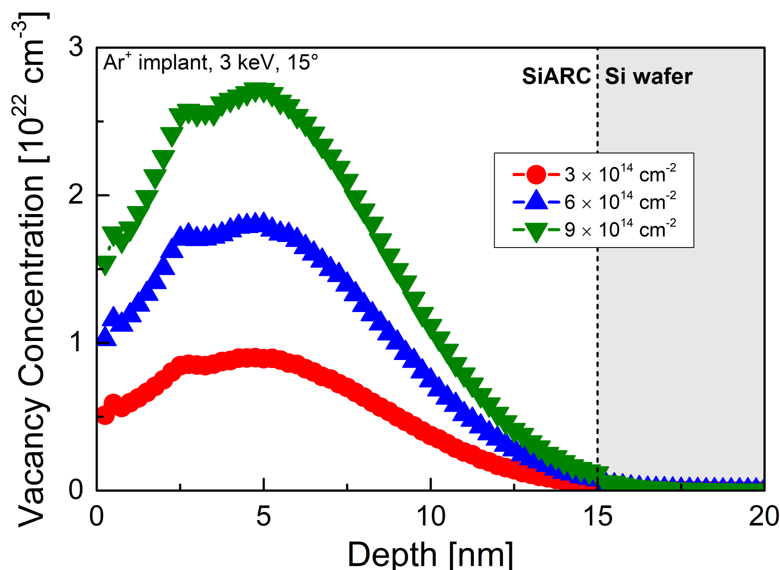


Figure 4.2: SRIM simulations of vacancy concentration depth profile for a 15 nm SiARC film on a Si substrate after a 3 keV, 15° tilt Ar^+ implant for three different implant dose values.

in films ∼15 nm thick. The wafers were then implanted with Ar^+ at an energy of 3 keV and tilt angle of 15°. Afterwards the wafers were diced into chips and etched in a 200:1 buffered HF (BHF) solution for different durations. Post-etch film thicknesses were then measured by variable angle spectroscopic ellipsometry (VASE); from these measurements the etch rate of the films could be calculated.

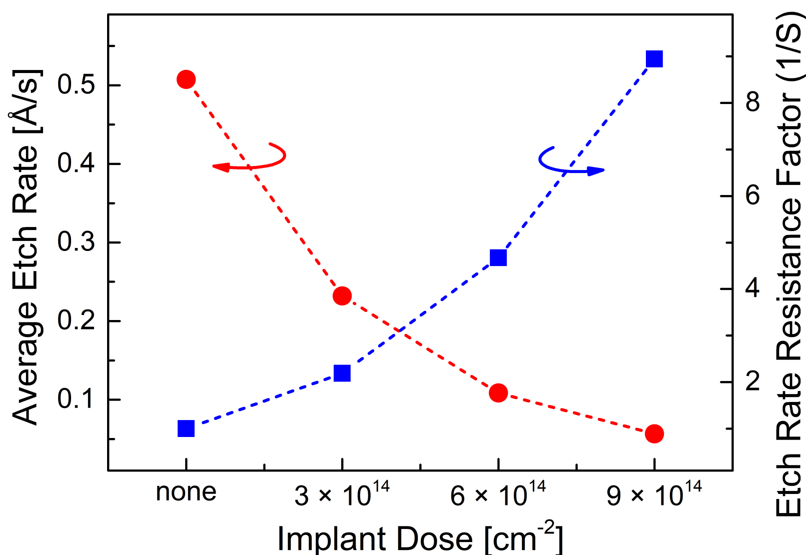


Figure 4.3: Characterization of TII-induced SiARC wet etch rate changes, in 200:1 BHF solution, for various Ar^+ implant doses.

Previous reports of wet etch rate enhancement of implanted SiO_2 layers cited an etch rate enhancement factor $S \approx 9$, meaning that the post-implant wet etch rate of SiO_2 was 9 times larger than that of non-implanted SiO_2 [91, 93]. In this work, since ion implantation decreases the SiARC wet etch rate so that $S < 1$, we cite an etch rate resistance factor (corresponding to $1/S$) to more clearly show the etch rate change for different implant doses. Fig. 4.3 plots both the SiARC wet etch rate and etch resistance factor as a function of Ar^+ implant dose, showing that a similar etch rate ($1/S \approx 9$) contrast can be achieved with SiARC as the TII material.

4.4 Sub-lithographic Nanoscale Patterning using SiARC TII Process

4.4.1 Process Flow of TII Line Patterning with SiARC

To demonstrate the viability of SiARC as a TII patterning layer, experiments were conducted to form sub-lithographic lines defined by tilted Ar^+ implantation into SiARC with pre-existing photoresist (PR) masking features. Fig. 4.4 schematically illustrates the process steps and shows corresponding cross-sectional scanning electron microscope (SEM) images. Samples were prepared as before, by spin-coating SiARC onto Si wafers, followed by a 220 °C bake in air, resulting in films ~15 nm thick. PR line patterns were then formed over the SiARC layer by spin-coating PR, exposing it using an ArF 193 nm DUV stepper, and subsequently developing it to form 165 nm-thick PR lines with line and space dimensions ranging from 200 nm to 300 nm (cf. step 1, Fig. 4.4).

Samples were then implanted with 3 keV Ar^+ at a tilt angle of 15° and dose of 9×10^{14} cm^{-2} to induce a wet etch rate contrast between implanted and non-implanted regions (cf. step 2, Fig. 4.4). Afterwards the samples underwent a 300 sec wet etch in 200:1 BHF solution (cf. step 3, Fig. 4.4) to selectively remove SiARC material from un-implanted regions, followed by a dry etch process to transfer the pattern of the SiARC layer to the underlying Si substrate. The dry etch was done using a transformer-coupled plasma (TCP) reactive ion etch (RIE) system using 200 W TCP RF power and 150 W bias RF power, under 80 mTorr pressure, flowing 100 sccm HBr, 1 sccm O_2, and 100 sccm He, for 18 sec (cf. step 4, Fig. 4.4).

4.4.2 Demonstration of Trench Patterning with TII

Because SiARC-based TII patterning is a negative-tone process, the areas that were implanted are unetched on the wafer whereas the non-implanted portions are etched, resulting in selective trench formation in the regions in which the implantation was shadowed by the PR masking features (Fig. 4.5). Sub-lithographic patterns ~44 nm wide were formed, which is close to the estimated pattern width for a TII-defined feature, x_{TII}, given the simple

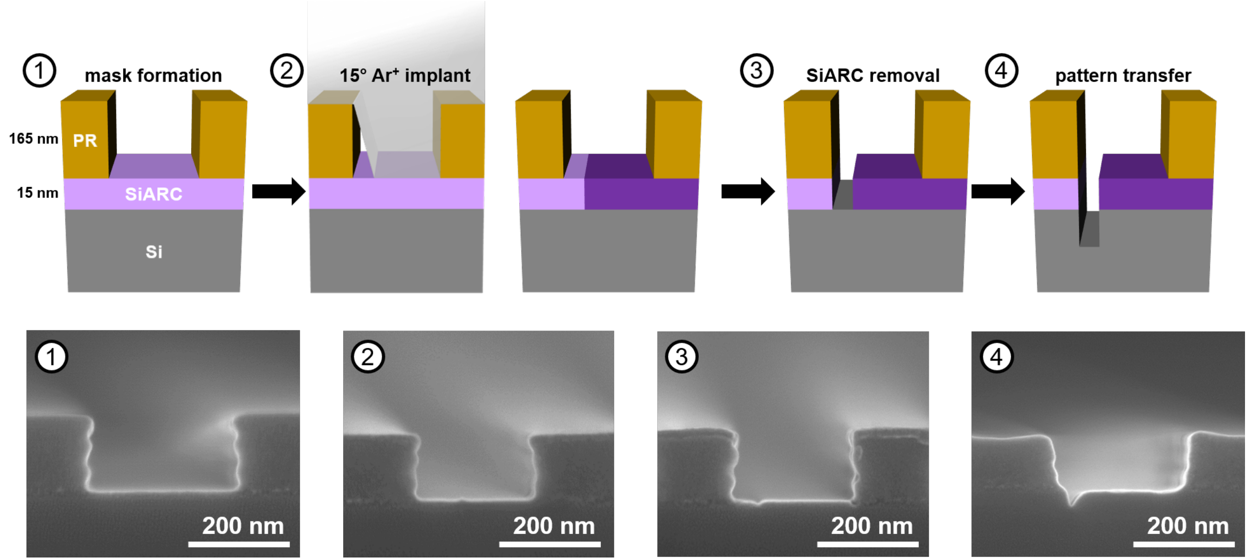


Figure 4.4: Cross-sectional process flow schematics (top) and corresponding SEMs (bottom) of SiARC-based TII line patterning. 1) PR masks are formed by DUV process, 2) implant with 3 keV Ar^+, dose $= 9 \times 10^{14}\,\mathrm{cm}^{-2}$, 15° tilt angle to decrease SiARC wet etch rate, 3) wet etch in 200:1 BHF solution to remove non-implanted SiARC regions, 4) TCP RIE dry etch in $HBr+O_2+He$ environment to transfer pattern to underlying Si substrate.

geometric relation between PR thickness, t_{PR}, and implant tilt angle, θ, as follows:

$$x_{\mathrm{TII}} = t_{\mathrm{PR}} \tan\theta \tag{4.1}$$

Due to PR shrinkage during implantation [95, 96], the shadowed region and hence the etched trench becomes tapered. This issue can be ameliorated by using a denser masking material that has minimal thickness change upon implantation.

4.4.3 Plan-View LER and Edge Deviation

To assess how well the TII-defined trench edge correlates with the edge of the PR mask, plan-view SEM images were used to measure the edge deviation between the two edges (Fig. 4.6) and their line-edge roughness (LER) (Fig. 4.7). It should be noted that the edge of the PR mask changes during both the implantation and dry etch steps, making a comparison between pre-implant PR and post-etch trench edges difficult.

Photoresist Mask and TII-Defined Edge Deviation

For the edge deviation measurements, the two edges used are the right-most edge of the PR pattern post-etch and the right-most edge of the TII-defined trench (Fig. 4.6, top right).

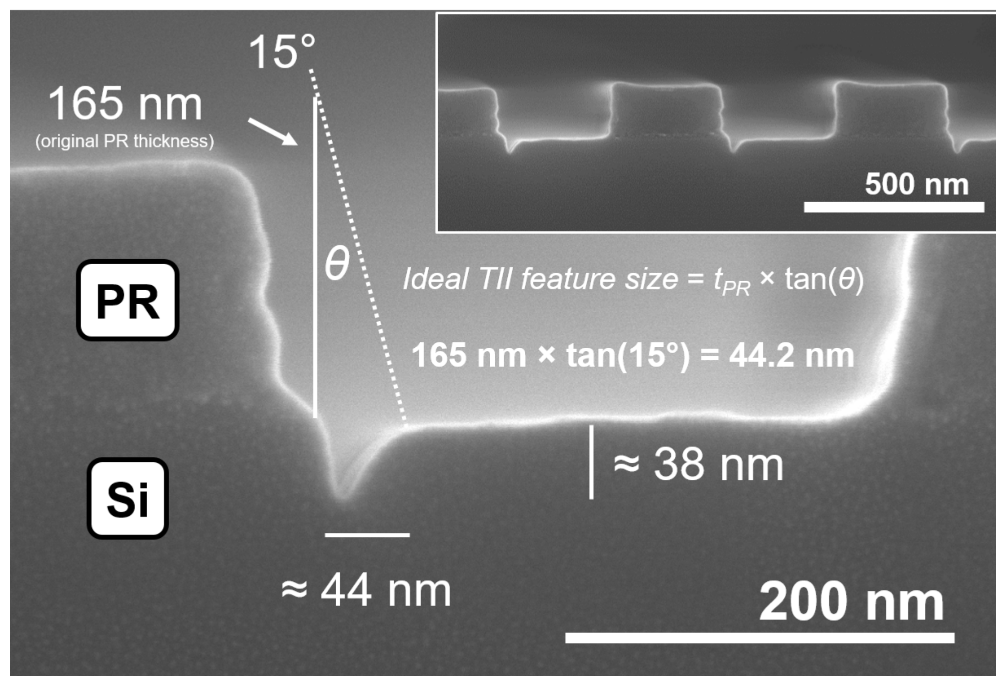


Figure 4.5: Cross-sectional SEM of the final TII-defined feature. The drawn lines representing the 165 nm-thick PR and 15° implant tilt angle are provided as visual guides. Final measurements indicate a patterned feature lateral dimension of ∼44 nm, close to the predicted feature size. Inset shows reproducible pattern formation on the side where the Ar^+ implantation was shadowed by the PR mask.

The results indicate a correlation coefficient of $r = 0.42$ (Fig. 4.6, bottom right), which is low due to the aforementioned PR erosion issue.

Power Spectral Density of TII-Defined Edge

Multiple power spectral density (PSD) analyses of the right-most edge of separate PR patterns pre-implant (n = 36) were averaged to reduce noise, resulting in an average LER of $\sigma_{\text{LER}} = 2.05$ nm. The same measurement approach was used for the right-most edge of the TII trenches (n = 52), resulting in an average LER of $\sigma_{\text{LER}} = 3.54$ nm. (All LER values reported were extracted using the SuMMIT software package [97].) While an increase in magnitude in the higher spatial frequency region is expected due to the stochastic nature of ion implantation, the observed increase is greater than anticipated due to the poor contrast between the TII-defined edge and adjacent SiARC/Si region (Fig. 4.6, left), raising the noise floor of the PSD analysis (Fig. 4.7). While both the edge deviation and TII-defined LER are not as closely correlated as desired, these values can be viewed as lower and upper bounds, respectively, of a TII process utilizing PR masking features and SiARC patterning layer.

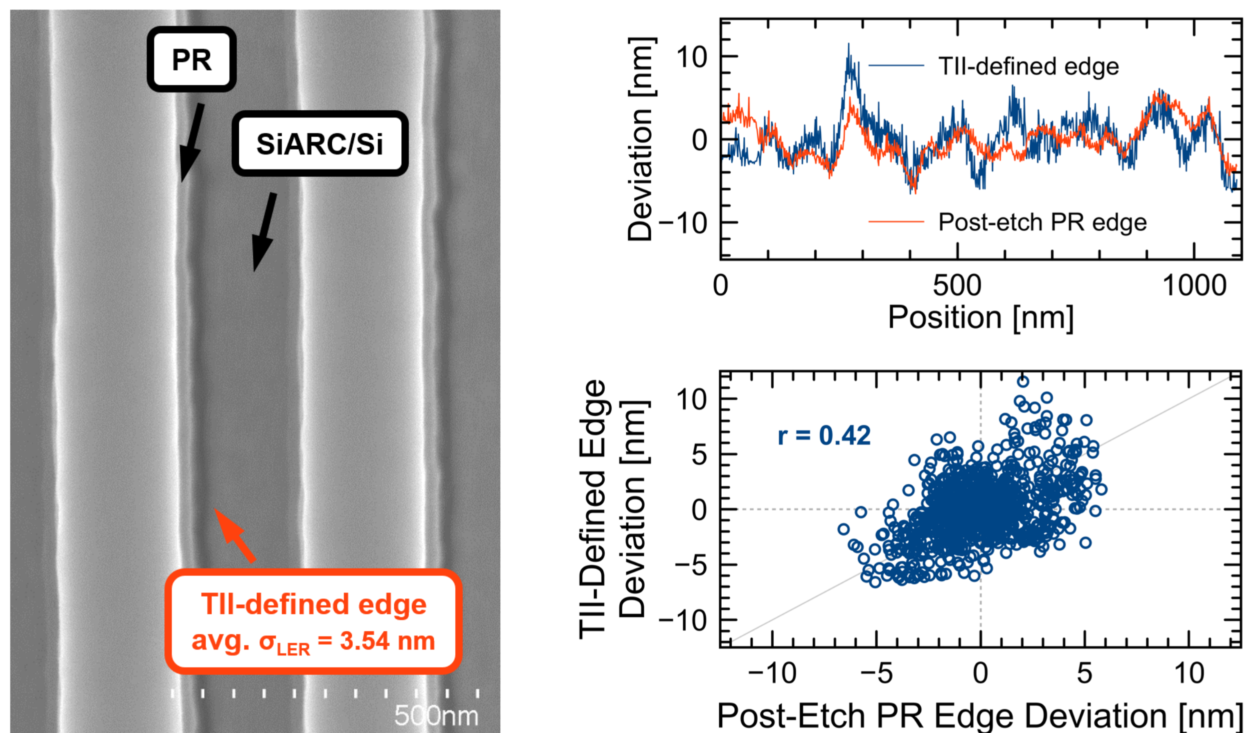


Figure 4.6: Plan-view SEM image of TII-defined feature along a PR mask line pattern, post-etch (left). Line edge deviation from the average position as a function of line pattern length (top right). Correlation between the TII-defined edge deviation and post-etch PR edge deviation (bottom right).

4.4.4 Near-20 nm Feature Patterning via SiARC TII

To achieve smaller x_{TII}, either t_{PR} or θ can be reduced, as seen from Eqn. 4.1. Here we demonstrate that smaller x_{TII} can be achieved by reducing the PR thickness from 165 nm to 80 nm, keeping θ constant. For an identical process flow (same ion implantation, wet etch, and dry etch conditions) as before, $x_{\mathrm{TII}} \approx 23$ nm is achieved with the thinner PR (Fig. 4.8). It can be expected that even smaller feature sizes would be achieved with thinner masking materials and/or smaller implant tilt angle.

4.4.5 Dual-Tone Patterning Using SiARC TII Process

Upon changing the SiARC material to a different composition, film thickness measurements as a function of BHF etch time at various Ar^+ implantation doses indicated that the SiARC etch rate initially can be enhanced with a lower implant dose (Fig. 4.9). This allows for the possibility of positive-tone patterning, rather than negative-tone patterning, using a single SiARC material simply by using different implantation doses and wet etch times.

To demonstrate this capability, experiments were performed using a 3 keV Ar^+ implant at

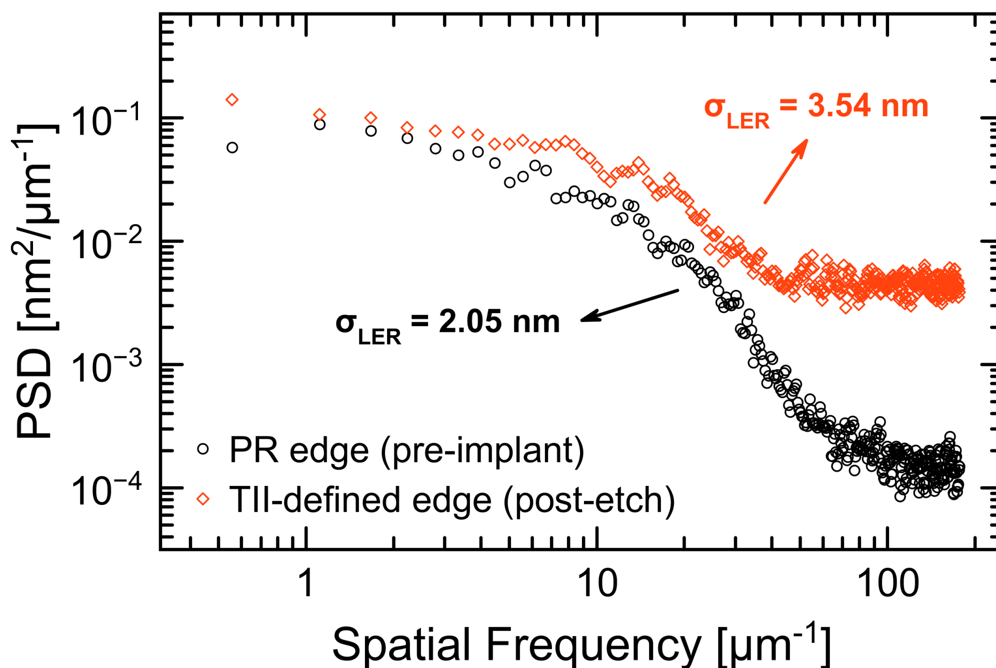


Figure 4.7: Power spectral density (PSD) comparison between DUV-patterned PR mask edges (black, circles) and TII-defined edge (red, diamonds). PR mask edge and TII-defined edge spectra and corresponding σ_{LER} values were calculated using 36 and 52 images, respectively, of lines 1.1 µm in length.

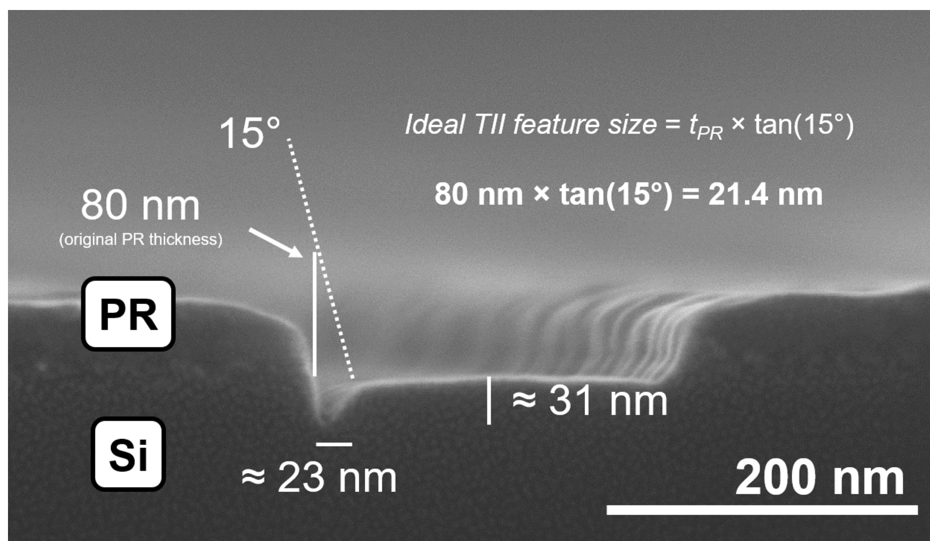


Figure 4.8: Cross-sectional SEM of TII patterning process using an 80 nm-thick PR mask, reducing x_{TII}.

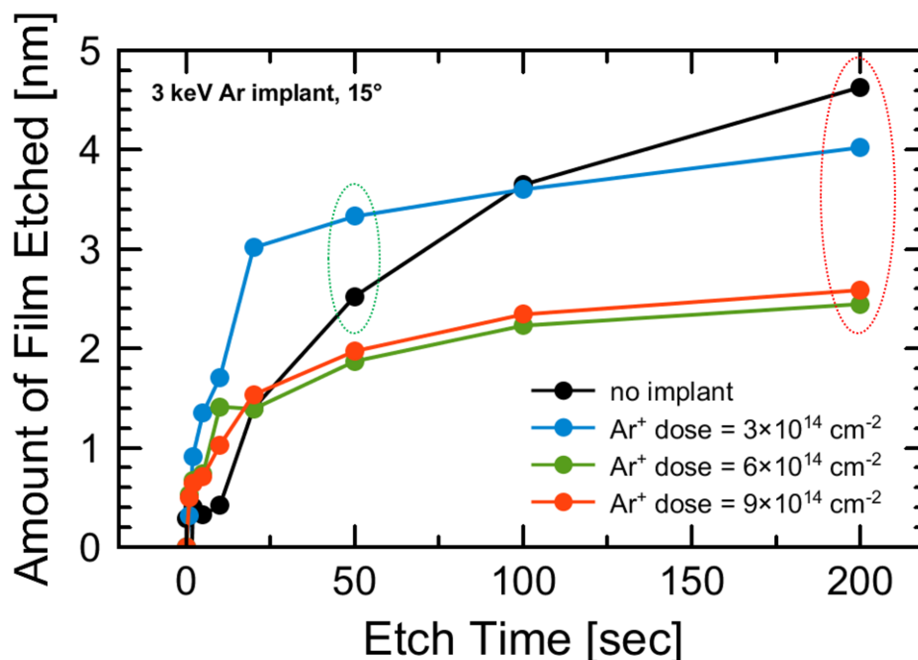


Figure 4.9: Characterization of dual-tone TII-induced SiARC wet etch rate changes, in 200:1 BHF solution, for various Ar^+ implant doses. Dashed circles represent the wet etch conditions for positive- (green) and negative-tone (red) patterning.

a title angle of 15° into a SiARC film patterned with 165 nm PR features. The positive-tone sample received a dose of $3 \times 10^{14}\,\mathrm{cm}^{-2}$ and underwent a 200:1 BHF wet etch for 50 sec, and the negative-tone sample received a dose of $9 \times 10^{14}\,\mathrm{cm}^{-2}$ and subsequent 200:1 BHF wet etch for 300 sec. Both samples then received a $HBr+O_2+He$ TCP RIE dry etch for 18 sec. For the positive-tone conditions, because the implanted regions have a faster etch rate compared to that of non-implanted regions shadowed by the PR mask, the TII-defined pattern is a step feature near the PR mask (Fig. 4.10, top). Due to the low etch rate contrast between implanted and non-implanted regions for this implant dose and wet etch time, the implanted regions exhibit a non-uniform wet etch rate, resulting in a rough surface. For negative-tone conditions, a trench feature is formed, similar to the previous data on negative-tone patterning (Fig. 4.10, bottom).

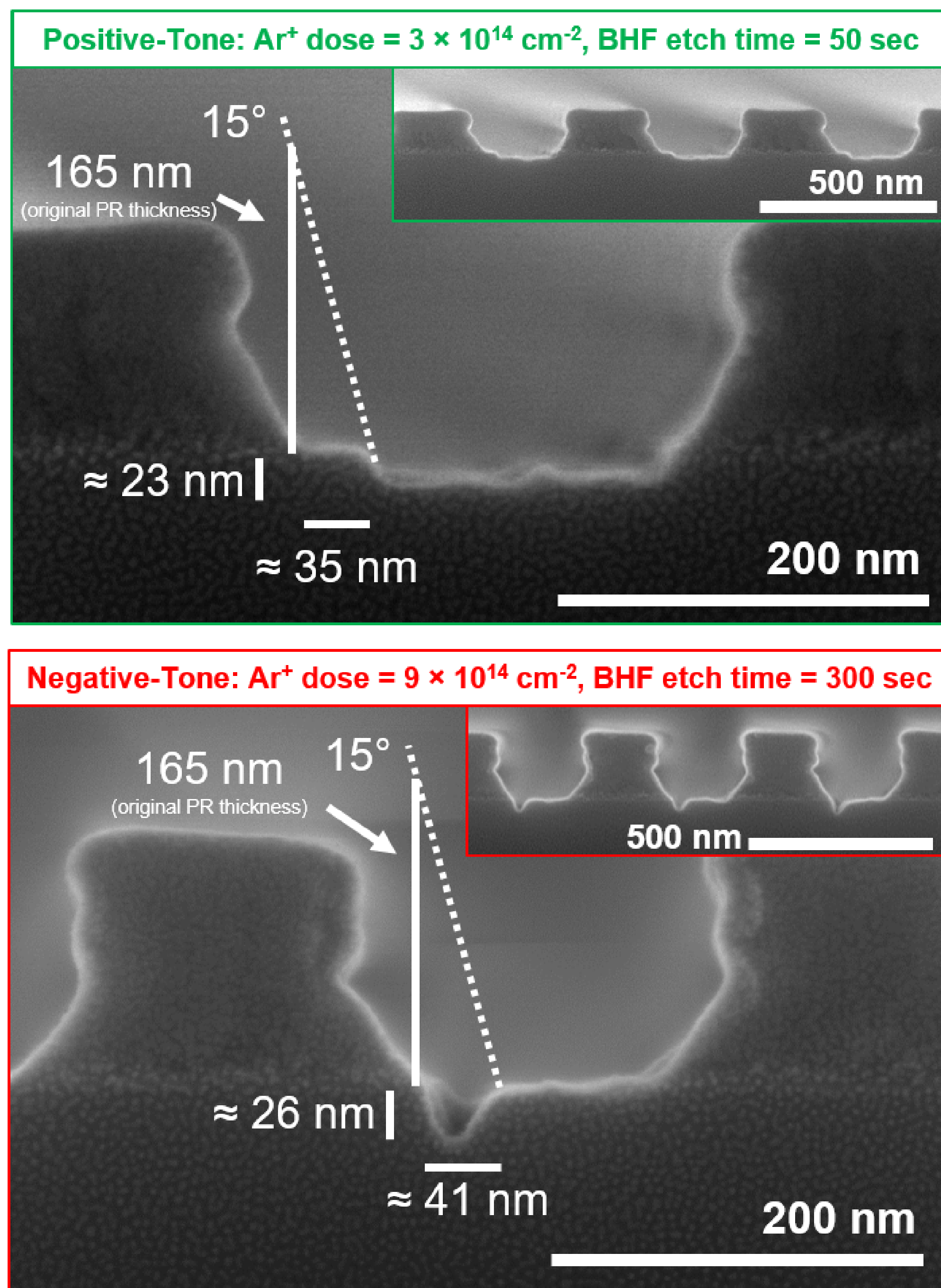


Figure 4.10: Cross-sectional SEMs of the final TII-defined features using a 50 sec wet etch for a $3 \times 10^{14}\,\mathrm{cm}^{-2}$ dose (top) and 300 sec wet etch for a $9 \times 10^{14}\,\mathrm{cm}^{-2}$ dose (bottom). The lower implantation dose induces a faster etch rate, resulting in positive-tone patterning of a step feature near the PR, while he higher implantation dose induces a slower etch rate, resulting in negative-tone patterning of a trench feature near the PR. Insets shows reproducible pattern formation on the side where the Ar^+ implant was shadowed by the PR mask.

4.5 Monte Carlo Simulations of TII Patterning

4.5.1 Two-Dimensional Patterning Concept

To date, TII patterning demonstrations have focused on creating linear features that extend in one direction. However, TII patterning also can be used to form 2D patterns by using two masking+TII steps, with the linear implanted regions extending in orthogonal directions. This would provide for further reductions in IC manufacturing cost, since more compact circuit layouts would be possible and fewer layers of metal would be needed to form the wiring on IC chips. The key to realizing this benefit is the ability to pattern 2D features with sub-lithographic minimum dimensions with good fidelity. An important aspect of the TII patterning approach is that a latent image is formed by masked ion implantation into the TII layer; this allows for multiple masked implants to be performed, to result in a composite pattern in the etched TII layer. Note that this summative patterning approach is not practical for other sub-lithographic patterning techniques such as spacer or DSA due to the non-planar topography of the sub-lithographic masking features. Fig. 4.11 shows a simulated process flow for forming a T-shaped pattern using a sequence of masked tilted 1.5 keV Ar^+ implantations (tilt angle = 25°, dose = 5×10^{14} cm^{-2}). All 2D TII simulations in this work were performed using Sentaurus Process [98].

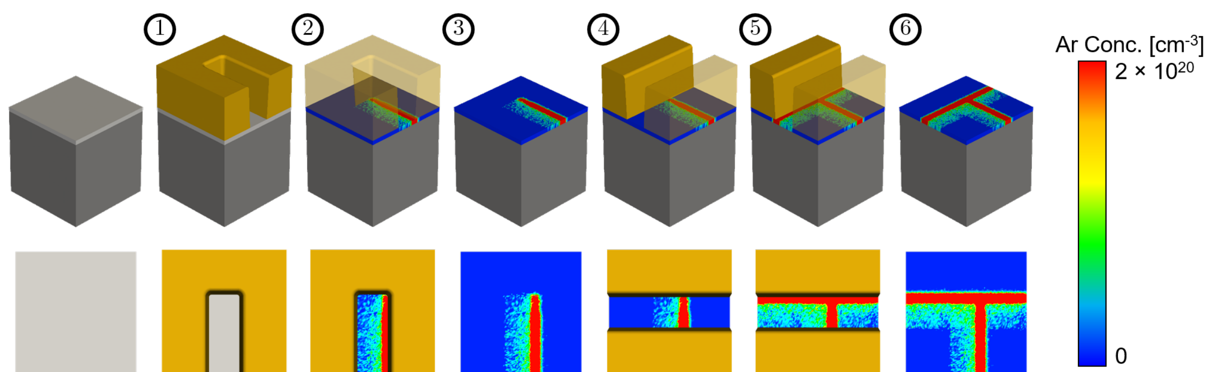


Figure 4.11: Monte Carlo simulated isometric- and plan-view images illustrating how a 2D composite latent image can be formed in the TII layer by a sequence of two masked 1.5 keV Ar^+ implants (tilt angle = 25°, dose = 5×10^{14} cm^{-2}). The Si substrate (100 nm × 100 nm) is shown in dark gray; the TII layer (5 nm thick) is shown in blue; the photoresist masks (50 nm thick) are shown in gold.

The first implant is masked by a U-shaped photoresist feature that exposes a 25 nm-wide linear region on the surface of the TII layer (Fig. 4.11, steps 1-3); the second implant is masked by a set of linear photoresist features that extend indefinitely along a direction orthogonal to the direction of the linear region previously exposed by the U-shaped photoresist mask (Fig. 4.11, steps 4-6). The resultant pattern of implanted Ar concentration in the TII layer is aligned with the edges of the masking features, and has smaller minimum feature

width. The line-width roughness seen for both implantations is due to reflection of ions off the sidewall of the masking feature [92]. The pattern of Ar concentration, which serves as a proxy for vacancy concentration, is indicative of the T-shaped pattern that would result when the TII layer undergoes an etch process step.

In order to derive the post-etch pattern, a threshold implanted Ar concentration is derived based on the Ar implant dose required to induce a vacancy concentration above the threshold value [93, 94]. In this work, an implanted Ar concentration of $2 \times 10^{20}\,\mathrm{cm}^{-3}$ is used as the threshold level; i.e., portions of the TII layer with implanted Ar concentration lower than this level are assumed to be removed during the etch process step. Fig. 4.12 shows the etched pattern of the TII layer.

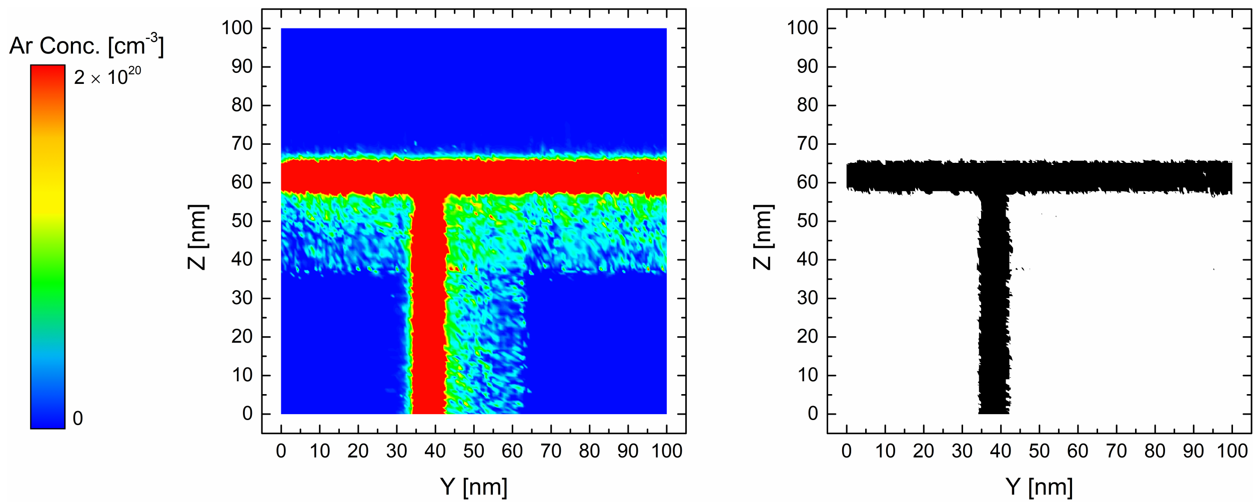


Figure 4.12: Ar concentration in TII layer after implantation (left) and the resultant pattern of the TII layer after etching, assuming that an implanted Ar concentration of $2 \times 10^{20}\,\mathrm{cm}^{-3}$ is necessary to prevent etching (right). The nominal linewidth for the image is $\sim$9 nm.

Derivation of Implant Threshold Value for Latent Image Extraction

Given that the proposed mechanism of etch rate change is via film damage, approximated by SRIM simulations calculating vacancy concentrations, a corresponding value of post-implant Ar concentration is used as a proxy. To derive this value, SRIM vacancy concentration results of the simulated implant conditions (1.5 keV implant energy, 25° tilt) into a 5 nm TII layer are used to determine the required implant dose to cause sufficient damage ($3 \times 10^{21}\,\mathrm{cm}^{-3}$). The conditions of this implant were chosen such that the vacancy concentration profile peak lies in the middle of the TII layer, 2.5 nm below the surface, which was the target depth to maximize damage uniformity throughout the depth of the film. The SRIM results for these implant conditions is shown in Fig. 4.13. To determine the dose needed for sufficient damage, the lowest vacancy concentration value from the distribution in the TII layer is used, as this guarantees the entire film will have at least $3 \times 10^{21}\,\mathrm{cm}^{-3}$ vacancies. In the

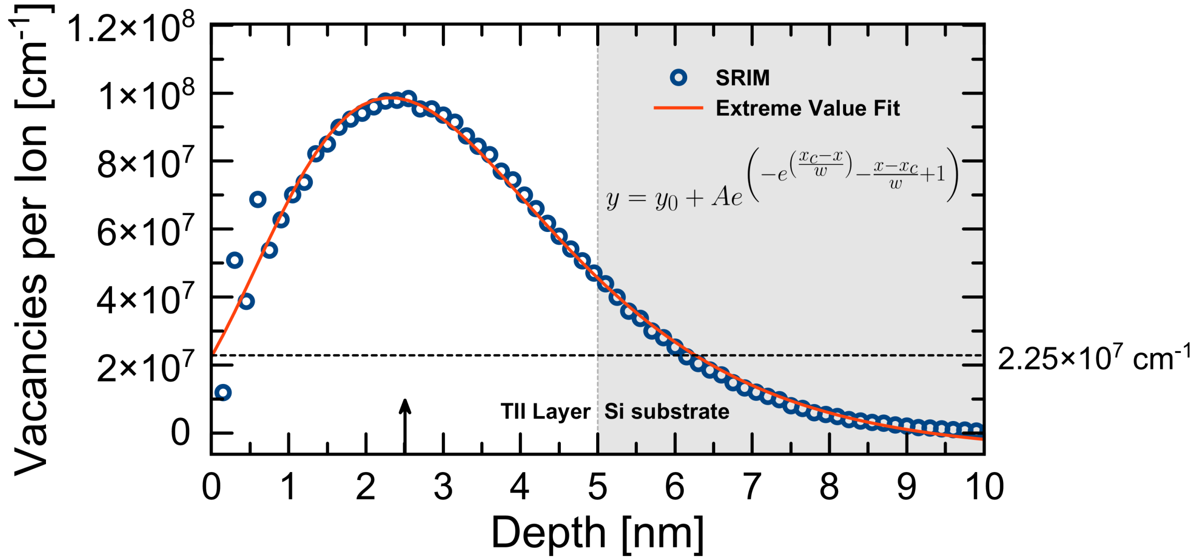


Figure 4.13: SRIM vacancy concentration distribution as a function of depth into a TII layer for a 1.5 keV Ar implantation at a tilt angle of 25° (blue circles) and corresponding extreme value distribution function fit curve (red line). The fit line (equation inset) is used to extrapolate a surface vacancy concentration, indicated by the horizontal dashed line. Latent image extraction was performed in the middle of the TII layer, indicated by the arrow at a depth of $x = 2.5$ nm.

case of our implant conditions, the vacancy concentration is lowest at the surface. SRIM results do not form a continuous distribution near the surface (see depth values <1 nm in Fig. 4.13), so a surface vacancy concentration cannot be directly extracted. To approximate the surface vacancy concentration, a fit curve of the SRIM vacancy concentration profile is use to extrapolate a y-intercept point. Due to the non-ideality of the vacancy concentration shape (i.e., it does not follow a simple Gaussian distribution), an extreme value distribution function is used (inset in Fig. 4.13). From this a surface vacancy concentration of 2.25×10^7 vacancies ion^{-1} cm^{-1} is extrapolated. Note that SRIM vacancy concentration values are reported as a one-dimensional concentration of vacancies caused per single ion. Thus, to get the required dose for a particular damage level, the following relationship is used:

$$Q\,[\text{ion cm}^{-2}] = \frac{d_{\text{th}}\,[\text{vacancies cm}^{-3}]}{v_{\text{SRIM}}\,[\text{vacancies ion}^{-1}\,\text{cm}^{-1}]} \tag{4.2}$$

where Q is the implantation dose, d_{th} is the threshold damage concentration, and v_{SRIM} is the SRIM vacancy concentration. For the extrapolated value of $v_{\text{SRIM}} = 2.25 \times 10^7$ vacancies cm^{-1} and a threshold damage concentration of $d_{\text{th}} = 3 \times 10^{21}$ vacancies cm^{-3}, the implantation dose is calculated to be $Q = 1.33 \times 10^{14}\,\text{cm}^{-2}$. (The "ion" unit is dropped as it is implied in general

implantation distribution functions.) Once a dose value is determined, the Ar implantation concentration profile, as a function of depth into the target layers x, can be calculated using the general Gaussian implantation profile equation:

$$N(x) = \frac{Q}{\sqrt{2\pi}\Delta R_{\mathrm{P}}} \exp\left(-\frac{(x - R_{\mathrm{P}})^2}{2\Delta R_{\mathrm{P}}^2}\right) \tag{4.3}$$

where R_{P} is the projected range and ΔR_{P} is the straggle. For the same SRIM simulation conditions in Fig. 4.13, the projected range and straggle of the Ar distribution are found to be $R_{\mathrm{P}} = 4\,\mathrm{nm}$ and $\Delta R_{\mathrm{P}} = 2\,\mathrm{nm}$, respectively. Using these values, along with the dose value of $Q = 1.33 \times 10^{14}\,\mathrm{cm}^{-2}$, the Ar concentration profile can be plotted (Fig. 4.14). For the

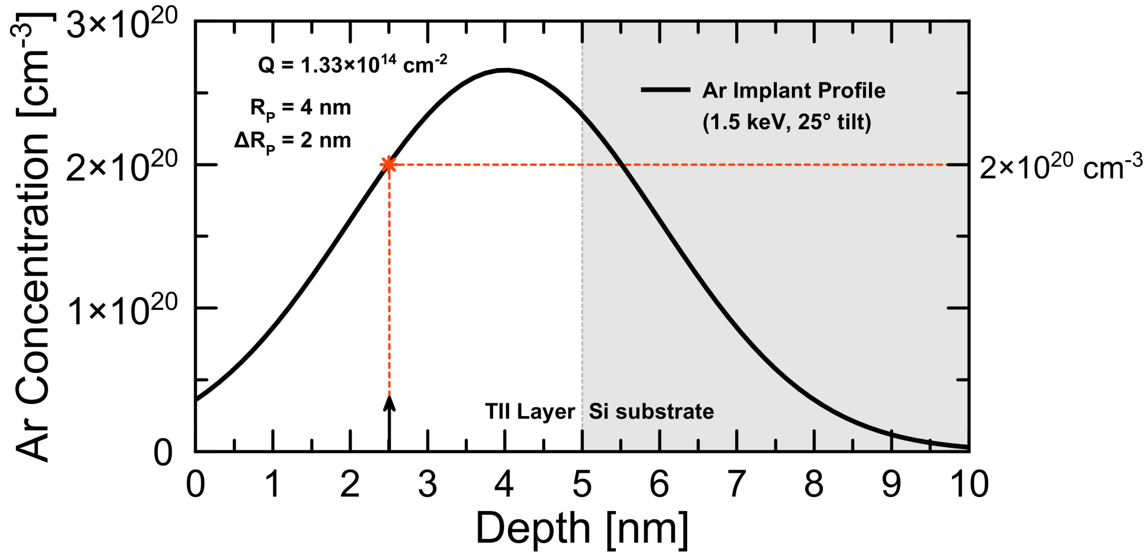


Figure 4.14: Gaussian Ar implantation concentration profile as a function of depth into a TII layer for a 1.5 keV Ar implant at a tilt angle of 25°. The values for dose, projected range, and straggle were found by SRIM to be $Q = 1.33 \times 10^{14}\,\mathrm{cm}^{-2}$, $R_{\mathrm{P}} = 4\,\mathrm{nm}$, and $\Delta R_{\mathrm{P}} = 2\,\mathrm{nm}$, respectively. Latent image extraction was performed in the middle of the TII layer, indicated by the arrow at a depth of $x = 2.5\,\mathrm{nm}$. The red dashed lines indicate the extracted Ar concentration used as the threshold for latent image formation ($2 \times 10^{20}\,\mathrm{cm}^{-3}$).

latent image extraction, slices of the TII layer were taken at a depth of 2.5 nm; thus, the Ar concentration at $x = 2.5\,\mathrm{nm}$ is used as the threshold concentration value. As shown in Fig. 4.14, this value is calculated to be $N(x = 2.5\,\mathrm{nm}) = 2 \times 10^{20}\,\mathrm{cm}^{-3}$.

It should be noted that this value is, indeed, a proxy concentration. Given the nature of the Monte Carlo simulations used, along with varied implant conditions and the stochastic variation of SRIM implantation profiles, the threshold concentration value can vary. However, for most of our implant conditions and latent image extraction, Ar concentration values between $1 \times 10^{20}\,\mathrm{cm}^{-3}$ and $2 \times 10^{20}\,\mathrm{cm}^{-3}$ were sufficient to determine latent images.

4.5.2 Repeatability of TII-Based Patterning

Given the stochastic nature of ion implantation, it is important to ensure that 2D TII patterning is repeatable. This is investigated by repeated TII Monte Carlo simulations using an unchanging set of masking features. For each set of orthogonal implantations, a latent image is extracted. These images are then averaged together, indicating the spatial variation of repeated patterning and probability of contribution to the latent image. Fig. 4.15 plots the spatial average of 50 images. Interestingly, the probability of implantation near the end of a mask opening is lower, presumably due to effects of the mask sidewall that is parallel to the direction of ion implantation.

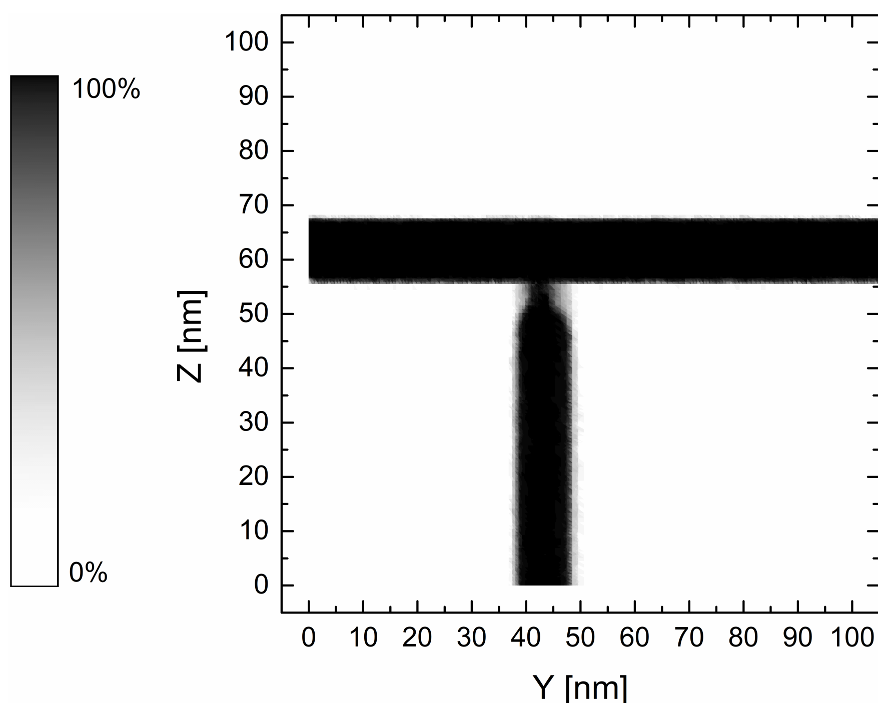


Figure 4.15: Repeatability of 2D TII patterning assessed by averaging the latent images resulting from 50 separate TII simulations using a fixed set of orthogonal masking features. Black indicates a point that is always above the concentration threshold, whereas white indicates a point that is never above the concentration threshold.

4.5.3 Effect of Mask-to-Mask Misalignment on Latent Image

2D patterning using TII requires separate masking steps for which the mask patterns cannot be reasonably expected to be perfectly aligned to each other. To assess the effect of misalignment, simulations were run such that the second mask was intentionally misaligned by varying amounts, up to +/− 25 nm. Fig. 4.16 shows the resulting patterns of implanted Ar concentration. (As before, the nominal linewidth was ∼9 nm.) Not surprisingly, the range

of misalignment is comparable to the nominal width of the extended feature at the juncture of the two implanted regions.

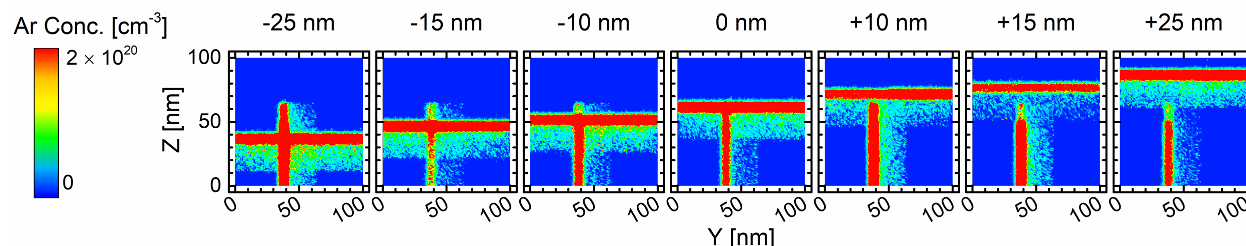


Figure 4.16: Ar concentration in TII layer after two masked implant steps, for varying degrees of overlap between the two masks. The amount of overlap is indicated above each plot. The tolerable misalignment is determined by the linewidth of the extended feature at the juncture of the two implanted regions.

4.5.4 Feasibility of Boolean Patterning

In this sub-section the possibility of forming a pattern in a TII layer defined by overlapping implanted regions is explored. We call this method Boolean patterning due to its AND-like function. Ideally, the dose for each implant is below the threshold level required to cause a significant change in the TII layer etch rate, but is at least half of this threshold level, so that regions of the TII layer that receive two implants will have significantly altered etch rate. Simulations were performed to study the formation of an etched TII layer pattern $\sim$70 nm $\times$ 70 nm square. Fig. 4.17 shows the as-implanted Ar concentration and the corresponding etched TII layer pattern, for a small range of implant dose values. The ability to form an isolated square pattern is demonstrated for a dosage window less than $10^{13}\,\text{cm}^{-2}$. With precise implant dose control, combined with high etch rate contrast for implanted vs. non-implanted regions, Boolean patterning should be possible.

4.5.5 LER Design Considerations

LER as Function of Mask Thickness, Implant Tilt Angle

Two key process parameters that determine the TII-defined feature size are the masking layer thickness and the implant tilt angle. Modification of these values, along with the pitch of the masking layer patterns, allows for a wide range of etched feature sizes to be achieved, down to the resolution limit of TII patterning. Since LER limits the precision of TII-based patterning, Monte Carlo implantation simulations were run using Sentaurus [98] to systematically investigate the combined effects of masking layer thickness and implant tilt angle on latent LER in the SiARC layer.

The simulated structure comprised a Si substrate with a 5 nm-thick TII patterning layer and preexisting masking features with a pitch of 400 nm (Fig. 4.18). This relatively large

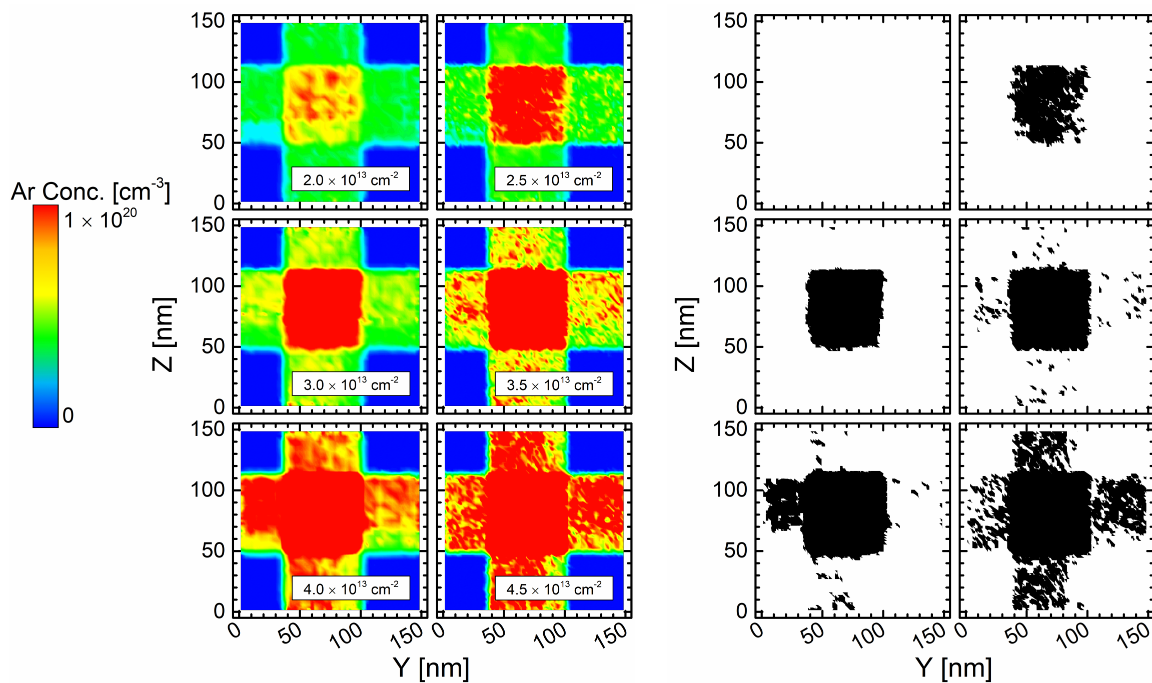


Figure 4.17: Simulation-based study of Boolean 2D patterning using overlapping Ar implantations at varying dose levels. Post-implant spatial profiles of Ar concentration (left) and their corresponding etched TII layer images (right) are shown. Dose conditions for each simulation are inset in the Ar concentration plots.

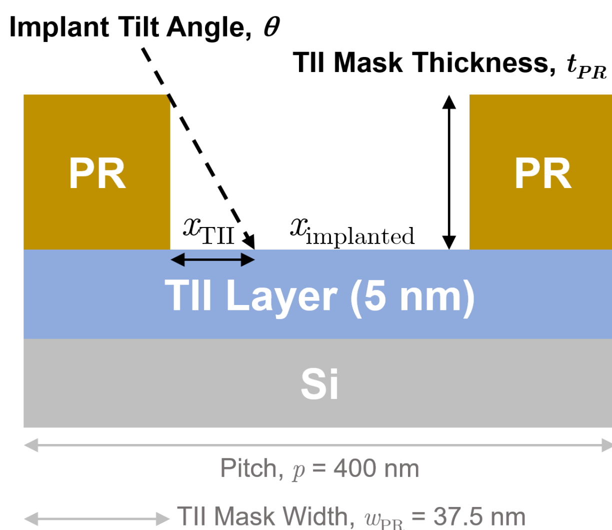


Figure 4.18: Cross-section schematic of simulated structure for TII-defined LER studies.

pitch was chosen to make negligible the effect of ion backscattering from the sidewall of the opposite (non-shadowing) preexisting masking feature [92]. The implant tilt angle was varied from 5° to 45° and the masking layer thickness was varied from 50 nm to 200 nm. The implantation species was Ar^+, with energy and dose values adjusted with the tilt angle to yield constant projected range and peak damage values based on SRIM [92]. The latent TII-defined line edge was deduced by determining the regions where the implanted dose exceeds the threshold value. Subsequently LER analysis was performed on this TII-defined line edge using the SuMMIT software package.

The simulated latent LER values show increased roughness with increasing tilt angle, consistent with the findings of a previous study [92], and additionally show minimal effect of the masking layer thickness, indicating TII-defined feature fidelity is affected primarily by the implant tilt angle (Fig. 4.19). Thus, thicker masking layers can be used to provide a wider range of possible x_{TII} feature sizes for smaller implant angles. Fig. 4.19 indicates

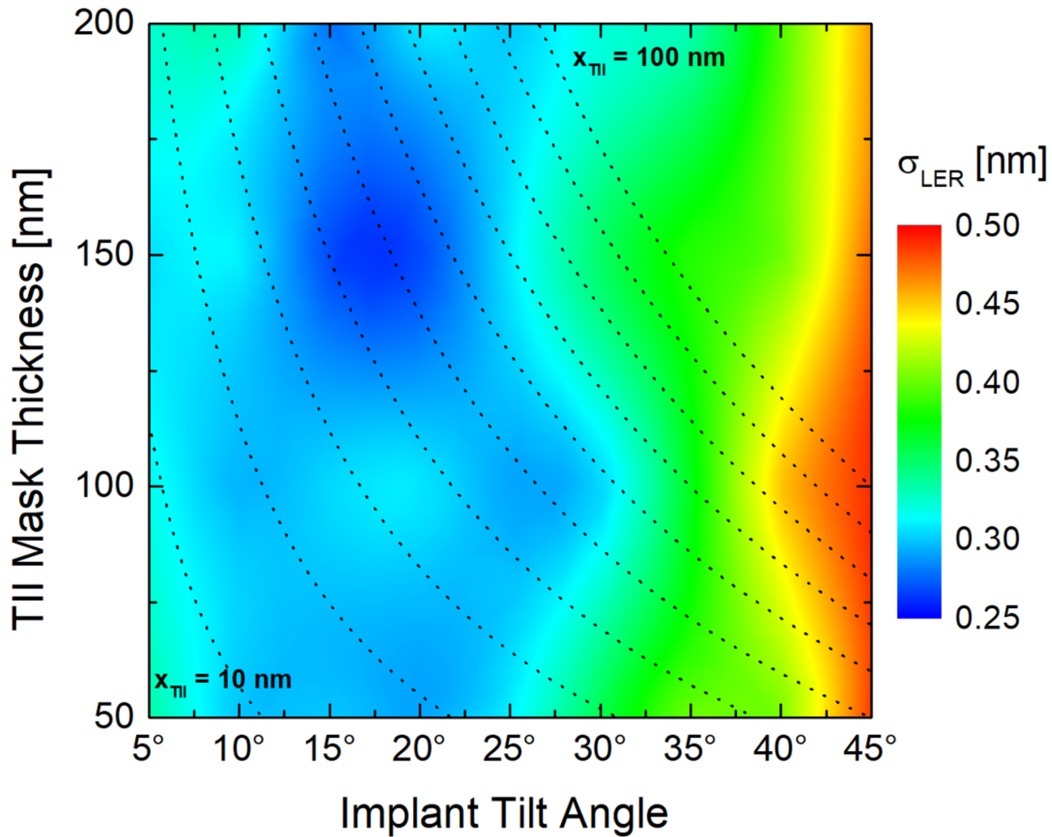


Figure 4.19: Monte Carlo simulations of TII-defined LER as a function of mask thickness and implant tilt angle. Dashed lines represent possible combinations of mask thickness and tilt angle that result in a particular x_{TII} value (from x_{TII} =10 nm to x_{TII} =100 nm in steps of 10 nm).

this via dashed contour lines that indicate all of the combinations of implant tilt angle and masking layer thickness that can be used to achieve a given x_{TII}.

4.6 Conclusion

4.6.1 Summary

This work has extended the application of TII as a sub-lithographic patterning technique, providing experimental proof-of-concept of a negative-tone patterning material as well as Monte Carlo simulations demonstrating the possibility of 2D patterning. In this work we have demonstrated a BEOL-compatible, sub-lithographic patterning technique based on tilted ion implantation (TII). Low-thermal-budget spin-coated SiARC material can be used for the TII layer, as it shows good etch rate contrast for implanted vs. non-implanted regions. The wet etch rate of a spin-coated SiARC film can be reduced by $\sim 9\times$ via Ar^{+} implantation. By using DUV-patterned photoresist over the SiARC layer to mask a tilted implant, sub-lithographic trenches down to $\sim$23 nm shown. Simulations indicate that 2D patterns can be reproducibly formed with high fidelity, down to $\sim$9 nm minimum dimension and that a wide range of PR thickness values and implant angles enables a wide design window for TII-based lithography. TII patterning utilizing SiARC films offers a lower cost, lower thermal budget solution to continued scaling of IC feature sizes and pitches, as compared with double patterning techniques, and hence is promising for extending the era of Moore's Law. Therefore, TII patterning paves a technological pathway for continued transistor miniaturization and density scaling, given the resolution limits of photolithography, to achieve improvements in IC performance and cost per function.

4.6.2 Future Work

In the future, more materials investigation is to be done into pinpointing the mechanism for the decrease in wet etch rate post-implant. While the current hypothesis of implant-induced increase in the number of Si-Si bonds is has been shown to be true via x-ray photoelectron spectroscopy (not included in this report), the increase is too small to be confirmed as the dominant mechanism. Therefore, further materials studies and surface analysis techniques must be performed to better understand the etch resistance mechanism.

Additionally, preliminary results indicates the possibility of using a single SiARC material layer for both positive- and negative-tone patterning, tunable by the implantation dose—one implant dose value causes the wet etch rate of the SiARC to be faster than that of non-implanted SiARC, and another implant dose value causes the wet etch rate to be slower than that of non-implanted SiARC. This has been experimentally verified via both step and trench patterning for positive- and negative-tone patterning, respectively. Development of this material and TII-process would allow for even greater BEOL patterning flexibility and

provide a BEOL-compatible positive-tone TII approach, which has yet to be demonstrated (as previous positive-tone TII results were based on thermally grown SiO_2 as the TII layer).

Simulations have shown the potential for 2D patterning and Boolean patterning; these now need to be experimentally performed to confirm their validity. Also, further optimization of the TII process, etching conditions, and resist use can improve the fidelity of the final TII pattern. While near-20 nm patterns have been shown in this work, previous SiO_2-based TII approaches using hard masks have successfully demonstrated $\sim$9 nm patterns. With continued development of the SiARC TII process, comparable feature sizes should be attainable.

Chapter 5

Conclusion

5.1 Summary

In this dissertation, individual temperature limitations imposed on fabrication processes and device operation in the areas of flexible electronics, IoT gas sensors, and BEOL Si CMOS nanoscale patterning were presented. Solutions to circumvent these limitations without sacrificing device integrity were discussed and demonstrated. For flexible electronics, the temperature limitation was focused on the temperature of the materials deposition processes onto plastic substrates. This was addressed via the application of a novel high rate deposition process to fabricate high quality n-type ZnO thin films. Previous demonstrations of the deposition process, filtered cathodic arc deposition, involved high conductivity transparent oxides for solar cell contacts; adaptation of this process to semiconducting oxide films enabled a novel approach to TFT fabrication, demonstrated via fabrication of all-oxide transparent TFTs on Si, glass, and flexible polyimide substrates as well as an NMOS inverter. For gas sensors, the temperature limitation arose in the use of high temperature heating of sensing elements for CO pollutant gas detection. The solution presented involves utilizing a high sensitivity Si-transistor-based gas sensing architecture combined with noble metal and metal oxide materials for efficient CO detection. Implementation of this device structure and materials platform allowed detection of pollutant level concentrations of CO with minimal device heating. For BEOL nanoscale patterning, the temperature limitation manifests as a maximum processing temperature of 400 °C—the temperature at which minimal effects to underlying device layers can be maintained. This thermal budget restriction was met with a novel alternative lithography approach utilizing spin-on SiARC films and tilted ion implantation. DUV-patterned photoresist features served as masking features for a tilted implantation event, selectively altering the SiARC etch rate in implanted regions, allowing for selective formation of nanoscale patterns on the order of 20 nm.

5.2 Future Work

For future research directions, each presented area will pivot from a temperature-mitigation-focused approach to address more specific outstanding materials- and device-related issues within each area. In the area of flexible electronics, future work will be conducted to look into the use of filtered cathodic arc deposition to form high-quality semiconducting p-type oxides for TFTs. Such a discovery would enable CMOS circuitry for low power flexible and transparent electronics circuitry. As for the Si-based pollutant gas sensors, work will continue both on the CO sensor front as well as addressing gas sensor fabrication for the remaining NAAQS-established pollutant gases. The CO sensor optimization, potentially implemented using approaches such as faceted noble metal nanoparticle deposition and compound oxide materials for enhanced CO oxidation at lower temperatures, will allow for even lower CO gas concentration detection at reduced temperatures, further improving device power consumption. Finally, future nanoscale patterning via spin-on SiARCs and tilted ion implantation should focus on the areas of minimum resolution demonstration, optimization of implant-induced etch rate contrast, and materials characterization. Using thinner and tighter pitch photoresist features, such as via EUV patterning, will allow for SiARC patterning demonstrations into the single-nanometer regime. Enhancing the etch rate contrast, whether for single-tone or dual-tone processes, will enable a larger processing window and provide for higher aspect ratio pattern transfer. Lastly, materials characterization to further clarify the structural and/or chemical change by which the etch rate changes will be necessary to develop future materials and processes utilizing spin-on SiARC materials for TII patterning.

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