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Microstructural Evolution of Nanotwinned Copper in Confined Moderate-Aspect-Ratio Through-Silicon Via Geometries

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Abstract:

Nanotwinned copper exhibits exceptional mechanical and electrical properties, making it a promising interconnect material for advanced electronic packaging. However, its microstructural evolution under microscale geometric confinement remains insufficiently understood. In this work, the thermal annealing–induced grain evolution of nanotwinned copper "pillar" is investigated in moderate-aspect-ratio through-silicon vias. The results reveal that confined nanotwinned copper "pillar" exhibits strongly heterogeneous grain growth, characterized by long-term retention of columnar grains and a high density of coherent twin boundaries in the via interior, while grain coarsening is localized near geometrically constrained regions. In contrast, conventional copper undergoes more uniform and extensive grain growth. Complementary Monte Carlo simulations incorporating twin boundary energetics show that coherent twin boundaries reduce boundary mobility, delay microstructural stabilization, and produce nonclassical grain growth behavior under confinement. These findings provide mechanistic insight into the role of twin boundaries in stabilizing microstructures and offer guidance for designing thermally robust semiconductors interconnects.

Keywords: Nanotwinned copper; Grain growth; Twin boundaries; Through-silicon vias; Thermal annealing.

As transistor scaling in advanced microelectronics continues to slow, conventional technology-node scaling is increasingly constrained by fundamental physical and economic limits [1,2]. Advanced packaging and heterogeneous integration have therefore emerged as a key strategy to extend system-level performance by integrating logic, memory, sensors, and analog components into compact 2.5D and 3D architectures. These approaches enable higher bandwidth density and improved energy efficiency, which are essential for data-intensive applications such as artificial intelligence and high-performance computing [3,4]. Central to these architectures are through silicon vias (TSVs), which provide vertical electrical 3D interconnections through silicon dies for high-density signal and power delivery [5,6]. However, continued scaling toward smaller diameters and higher aspect ratios introduces significant challenges in mechanical integrity, electrical reliability, and thermal stability, motivating the development of advanced interconnect materials and microstructural control strategies. Copper (Cu) is widely used as the TSV filling material due to its high electrical conductivity, compatibility with electroplating processes, and cost effectiveness relative to alternative interconnect metals [7]. Nevertheless, integrating Cu within silicon substrates presents substantial materials reliability challenges. The large coefficient of thermal expansion (CTE) mismatch between Cu and Si generates significant thermo-mechanical stresses during thermal annealing, which promote plastic deformation and Cu protrusion near the wafer surface [8–11]. These deformation mechanisms are strongly coupled to the underlying microstructural evolution of the Cu TSVs. Thermal annealing drives grain growth and recrystallization, reducing grain boundary density and, consequently, decreasing hardness and yield strength in

accordance with the Hall–Petch relationship [10]. As grains coarsen, Cu becomes increasingly susceptible to stress-driven deformation, exacerbating via protrusion and increasing the risk of interfacial delamination, dielectric cracking, and electrical shorting in back-end-of-line (BEOL) structures [11]. The combined effects of microstructural coarsening and thermo-mechanical stress ultimately degrade the mechanical robustness and long-term reliability of Cu TSVs during fabrication and operation.

To address these limitations, nanotwinned copper (NT-Cu) has emerged as a promising alternative interconnect material due to its exceptional combination of high strength, thermal stability, and electrical conductivity [12]. NT-Cu is characterized by nanoscale twin lamellae, typically spaced from a few to several tens of nanometers, resulting in a high density of coherent twin boundaries (CTBs). These CTBs effectively impede dislocation motion, leading to significantly enhanced yield strength compared with coarse-grained Cu [13]. At the same time, the coherent and metallic nature of twin boundaries minimizes electron scattering, enabling electrical conductivities approaching or even exceeding the International Annealed Copper Standard (IACS) [14]. NT-Cu thin films have demonstrated remarkable thermal stability up to approximately 300°C, which has been attributed to the low interfacial energy of CTBs, high triple-junction density, and strong {111} crystallographic texture [15]. These attributes are particularly advantageous in microelectronic environments subjected to repeated thermal cycling, where grain growth and diffusion-driven degradation often limit the performance of conventional Cu. Consequently, NT-Cu has been successfully integrated into a range of advanced microelectronic packaging components, including under-bump metallization (UBM) [16–18], Cu pillars [19–21], redistribution layers (RDLs) [22–24], and TSVs [25–28]. When implemented in TSV structures, NT-Cu has demonstrated notable improvements in thermal stability and mechanical reliability. For example, NT-Cu-filled TSVs exhibit up to a 70.3% reduction in protrusion during thermal annealing at 250°C compared with conventional Cu TSVs, highlighting their enhanced resistance to stress-induced plastic deformation [26]. Despite these advances, most prior studies have focused on TSVs with relatively large diameters with low aspect ratios or thin film [25,26], leaving the microstructural evolution and thermal reliability of fine-pitch, moderate-aspect-ratio NT-Cu TSVs largely unexplored. However, systematic studies examining how annealing temperature governs NT-Cu microstructural evolution under microscale geometric confinement are still lacking in the literature. A clearer, physics-based understanding is therefore required to enable reliable integration of NT-Cu in advanced 3D integrated circuits and to establish models linking microstructural evolution to thermomechanical reliability.

In our previous work, we developed a complete electrochemical disposition process flow for fabricating moderate-aspect-ratio (~4:1) NT-Cu TSVs with a small diameter of 20 μm and systematically investigated the effects of current density and TSV additives on NT-Cu growth behavior [29]. The fabrication process flow for NT-Cu TSVs is highlighted in Supplementary Fig. S1. The NT-Cu electrolyte used in this study is a commercial formulation. While the exact proprietary additive composition is not disclosed by the manufacturer, the electrolyte does not contain conventional TSV additives (accelerator, leveler, suppressor) as used in standard Cu TSV plating. As shown in our prior work [29] and Supplementary Fig. S2, this distinction is critical: the absence of standard TSV additives preserves the overpotential modulation mechanism responsible for sustained twin boundary formation. Building on this foundation, the present study introduces a same-via correlative characterization approach (Supplementary Fig. S3), enabling direct examination of identical TSVs before and after annealing to correlate microstructural evolution with thermal history. Systematic annealing experiments were

conducted at 200°C, 300°C, and 400°C for 1 hour to understand temperature-dependent microstructural evolution in NT-Cu TSVs. For direct comparison, conventional electroplated Cu TSVs with identical geometries and processing conditions were characterized in parallel. This approach enables a controlled investigation of the role of twin boundaries in governing grain growth behavior under moderate-aspect-ratio via geometry confinement. To confirm that the observed post-annealing microstructures are not affected by pre-annealing sectioning or by partial TSV exposure during annealing, additional nearby TSVs are cross-sectioned and analyzed after annealing for comparison. This work seeks to understand how thermal annealing drives microstructural evolution in NT-Cu TSVs with moderate aspect ratios, with particular focus on the role of coherent twin boundaries in producing region-dependent grain growth behavior distinct from that observed in conventional Cu. More broadly, this work will improve the fundamental understanding of grain growth in nanotwinned metals under microscale geometric confinement and support the development of thermally stable copper interconnect materials for future three-dimensional integration technologies.

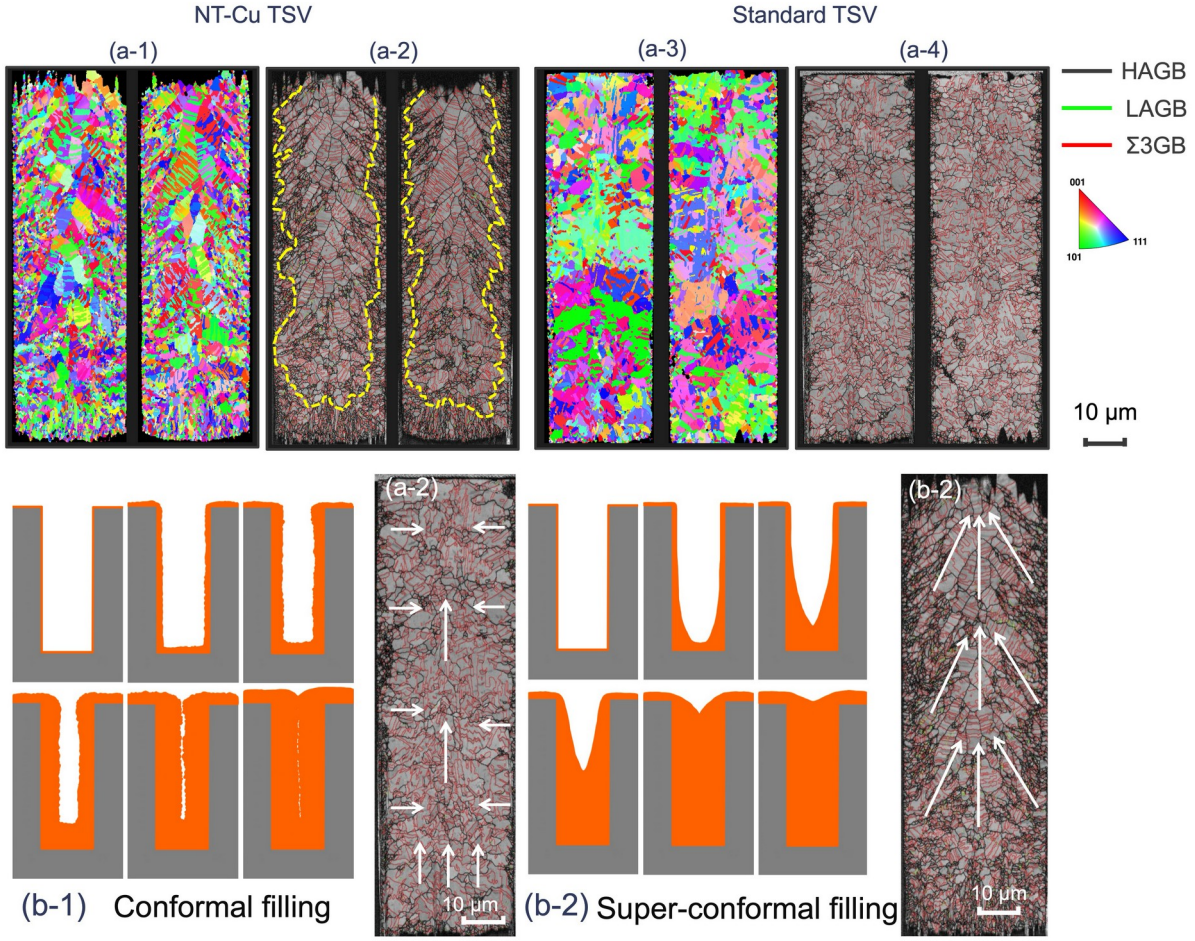

Fig. 1: (a) EBSD orientation maps and corresponding grain boundary distributions of as-plated (a-1) (a-2) NT-Cu TSVs (the dashed line indicates the interface between the NT-Cu region and the transition layer) and (a-3) (a-4) conventional Cu TSVs. High-angle grain boundaries (HAGBs), low-angle grain boundaries (LAGBs), and Σ3 twin boundaries are indicated by black, green, and red lines, respectively. (b) Schematic illustration of (b-1) conformal and (b) super-conformal filling modes during Cu electroplating in TSVs, and Grain boundary distribution map of as-plated NT-Cu TSV showing the inclined upward growth of columnar grains along the via centerline.

As shown in Fig. 1 (a-1), the as-plated NT-Cu TSVs exhibit pronounced spatial heterogeneity in grain structure along both radial and axial directions. The via interior particularly the middle and upper regions is dominated by elongated columnar grains containing a high density of coherent Σ3 twin boundaries. In contrast, a distinct transition layer composed of finer, less-aligned grains is observed near the sidewalls and bottom corners of the via. This microstructural heterogeneity reflects the nonuniform growth conditions inherent to moderate-aspect-ratio TSV electroplating, where geometric confinement and proximity to the sidewalls modify local current density and mass transport. These effects destabilize grain growth near the via periphery, which limits the lateral and axial extension of grains in these regions. The grain boundary maps in Fig. 1 (a-2) further corroborate this interpretation, showing that Σ3 twin boundaries are concentrated predominantly within the columnar grain region, while the transition layer contains a higher fraction of random grain boundaries. This indicates that sustained nanotwinned growth is preferentially achieved in the via interior, whereas near-sidewall regions experience conditions less favorable for twin-dominated growth. As illustrated by comparison with Fig. 1 (a-3), the transition layer in NT-Cu TSVs is noticeably thicker than that in conventional Cu TSVs. This observation suggests that stable nanotwin formation requires a sufficiently high and continuous deposition rate. When this condition is not met, such as near the sidewalls, twin-assisted growth cannot be maintained, resulting in a gradual transition from fine, randomly oriented grains to fully developed nanotwinned columnar structures. Consistent with this interpretation, the grain boundary distribution in Fig. 1 (a-4) confirms that Σ3 twin boundaries are primarily associated with the columnar grain regions.

The mechanism of this heterogeneous microstructure can be understood within the framework of super-conformal electroplating. Previous studies by Wang *et al.* identified two primary Cu filling modes in moderate aspect ratio via geometry-TSVs: conformal filling and super-conformal filling [30]. In conformal filling, Cu deposits uniformly along the via sidewalls, often leading to void or seam formation (Fig. 1 (b-1)). In contrast, super-conformal filling promotes a higher deposition rate at the via bottom than near the top, enabling void-free filling (Fig. 1 (b-3)). During super-conformal growth, spatial variations in current density and mass transport favor faster and more continuous deposition within the via interior, promoting the formation of columnar grains with a high twin density, as observed in Fig. 1 (a-1) (a-2). The inclined upward growth of these columnar grains along the via centerline (Fig. 1 (b-4)) is consistent with a bottom-up growth mechanism. The high concentration of Σ3 twin boundaries in the columnar region (Fig. 1 (a-1) (a-2)) further confirms that the nanotwinned structure is preserved during upward growth, directly linking the observed microstructure to the super-conformal filling process. A dense lamellar twin structure is clearly observed in as-plated NT-Cu TSVs shown in Supplementary Fig. S4, with twin lamellae extending parallel to the columnar grain growth direction. The twin lamella thickness ranges from approximately 10 to 100 nm, with the majority falling between 50 and 70 nm. The EBSD orientation map in Fig. 1 (b-4) reveals inclined, band-like columnar grains in the as-plated NT-Cu TSVs that extend continuously along the via depth. These grains exhibit clear crystallographic orientation continuity along the growth direction. These twin boundaries possess low interfacial energy and high crystallographic coherency, which stabilize the advancing grain front and promote sustained columnar growth while preserving internal crystallographic order. The combined presence of columnar grain morphology, orientation continuity within individual grains, and a high fraction of coherent twin boundaries indicates that the as-plated NT-Cu TSVs exhibit a highly organized growth structure. Such a microstructure is expected to respond fundamentally

differently to subsequent thermal annealing compared with randomly oriented, equiaxed grain structures.

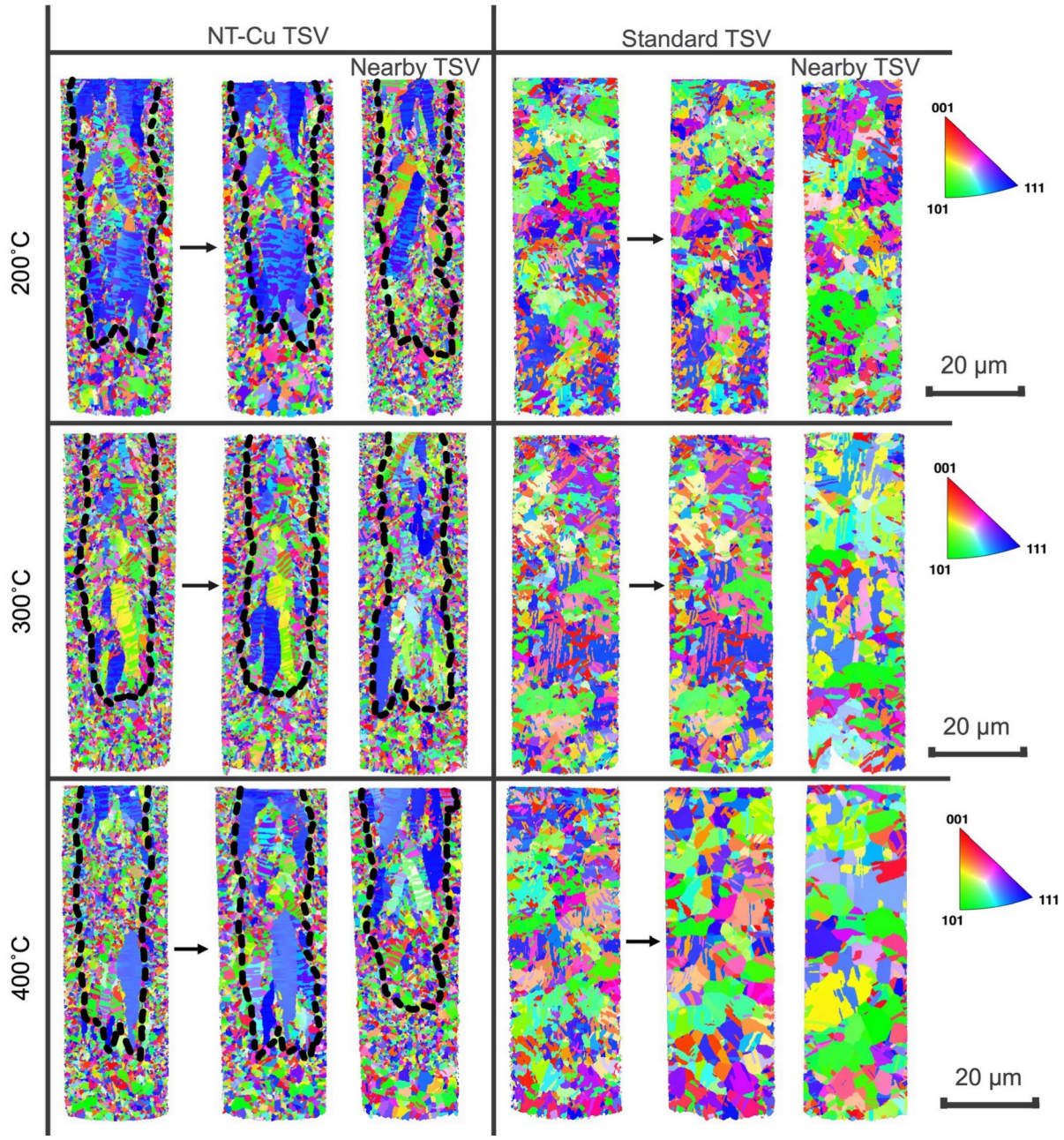

Fig. 2: Same-via cross-sectional EBSD images of NT-Cu TSV and standard TSV before and after thermal annealing under 200˚C, 300˚C, and 400˚C for an hour. The dashed line indicates the interface between the NT-Cu region and the transition layer.

Figure 2 presents same-via cross-sectional EBSD orientation maps of NT-Cu and standard Cu TSVs before and after annealing at 200°C, 300°C, and 400°C for 1 hour. The combined same-via and nearby-via analyses confirm that the observed microstructural changes arise from thermal annealing rather than from pre-annealing polishing or sectioning artifacts. At 200°C, both NT-Cu and standard TSVs exhibit minimal microstructural evolution. Grain size, morphology, and orientation distributions remain largely unchanged relative to the as-plated condition, indicating that annealing at this temperature primarily relaxes residual stresses without activating significant grain growth or recrystallization. At 300°C, distinct differences in

microstructural response emerge between NT-Cu and standard TSVs. In NT-Cu TSVs, the columnar grain structure in the via interior is largely preserved, with grain growth confined mainly to the transition layer near the sidewalls, where finer grains undergo limited coarsening. In contrast, standard Cu TSVs exhibit pronounced grain growth across the entire via cross section, accompanied by the development of larger and more irregular grain morphologies. These differences become more pronounced at 400°C. In NT-Cu TSVs, columnar grains in the via interior remain continuous and well aligned, while the transition layer experiences more noticeable grain growth. Conversely, standard TSVs undergo extensive grain growth and recrystallization throughout the via, resulting in very large grains and a highly nonuniform microstructure. These results demonstrate that while annealing temperature strongly influences grain evolution, the response is governed by the initial microstructural state. NT-Cu TSVs exhibit constrained, region-specific grain evolution, whereas standard TSVs display a more uniform and temperature-sensitive grain growth behavior across the entire via.

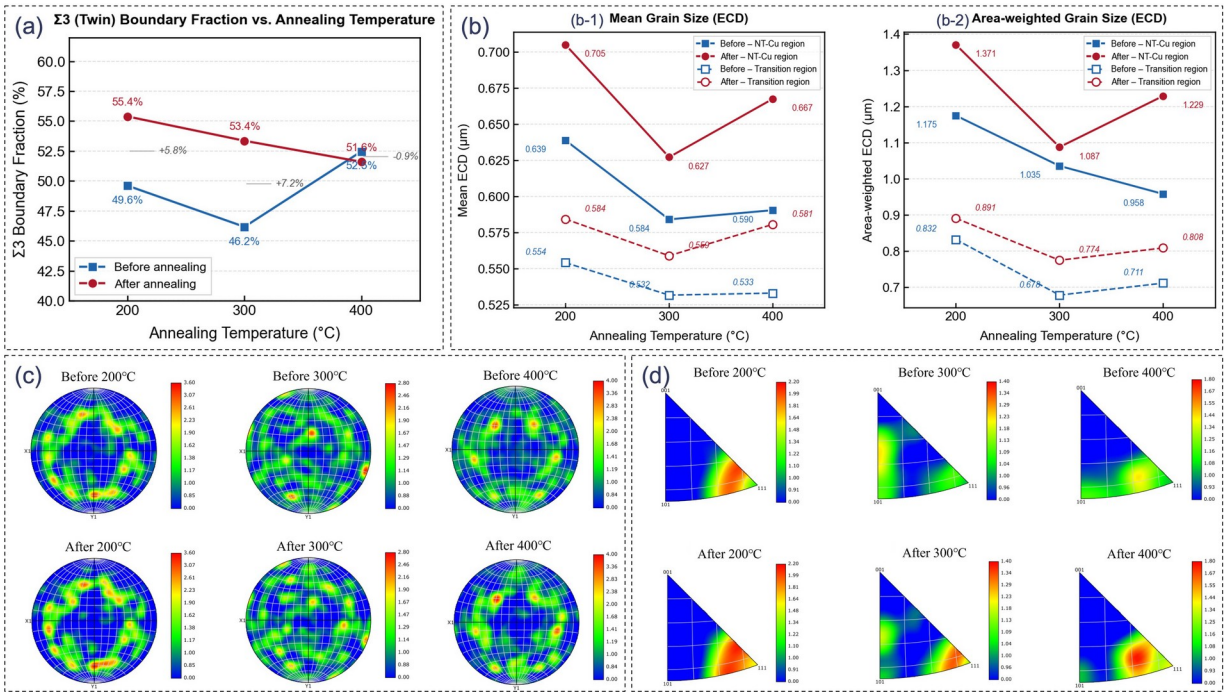

Fig. 3. (a) Evolution of Σ3 boundary fraction before and after annealing. (b) Quantitative comparison of grain size evolution in the nanotwinned region and transition layer before and after annealing: (b.1) mean grain size and (b.2) area-weighted grain size. (c) Pole figure analysis showing the evolution of crystallographic texture before and after annealing at different temperatures. (d) Inverse pole figure (IPF) maps showing the evolution of crystallographic texture before and after annealing at different temperatures.

In Fig. 3 (a), the evolution of Σ3 boundary fraction provides quantitative support for the non-classical grain growth behavior in NT-Cu TSVs. After annealing at 200°C and 300°C, the Σ3 fraction increases by approximately 5–7%. This reflects the selective coarsening of high-angle grain boundaries in the transition layer. As these boundaries migrate and merge during annealing, the stable coherent twin boundaries in the columnar interior account for a larger share of the total boundary population. At 400°C, the Σ3 fraction before and after annealing converges to similar values, that twin boundaries begin to evolve at this temperature but remain relatively stable overall. This trend serves as quantitative evidence that coherent twin boundaries fundamentally alter grain growth kinetics under confinement.

In Fig. 3 (b), grain size statistics extracted from the EBSD maps provide quantitative support for the region-specific grain growth behavior observed in NT-Cu TSVs. In the NT-Cu region, mean ECD increases by 10.3%, 7.4%, and 13.1% after annealing at 200°C, 300°C, and 400°C, respectively. The corresponding area-weighted ECD increases are 16.7%, 5.0%, and 28.3%. In the transition region, mean ECD increases by 5.4%, 9.8%, and 9.0% after annealing at 200°C, 300°C, and 400°C, respectively, with area-weighted ECD increases of 7.1%, 14.2%, and 13.6%. The relatively modest changes at 200°C and 300°C in NT-Cu region confirm that the columnar interior remains largely stable at moderate temperatures. At 400°C, the increase in area-weighted ECD and mean ECD suggests that a small number of larger grains begin to coarsen, while the overall grain size distribution remains relatively unchanged.

Fig. 3 (c) and (d) are the pole figure and inverse pole figure maps, separately, showing the evolution of crystallographic texture before and after annealing at different temperatures. The results indicate that the overall texture remains relatively structured without complete randomization, suggesting that the crystallographic framework of the electroplated Cu is largely preserved during annealing. In additional, the dominant {111} orientation is largely preserved during annealing as is showed in Fig. 3 (d).

Fig. 4: FIB and EBSD images of top view of NT-Cu (NT) and standard TSVs before and after annealing under different temperatures.

In addition to cross-sectional analysis, the top-view surface morphology of NT-Cu and standard Cu TSVs before and after annealing at different temperatures is shown in Fig. 4. At 200°C, both NT-Cu and standard TSVs exhibit relatively smooth surfaces, with only a few small voids observed near the sidewalls. At this temperature, no appreciable surface deformation is detected for either TSV type, indicating limited thermally activated plasticity or grain growth. At higher annealing temperatures, distinct differences in surface morphology emerge. After annealing at 300°C, NT-Cu TSVs develop localized surface protrusions near the via periphery, while the central region remains comparatively smooth. Upon further annealing at 400°C, surface protrusions become more pronounced near the outer region of the via, forming spike-like features, whereas the central nanotwinned region continues to exhibit minimal surface deformation. These observations indicate that thermally induced surface deformation in NT-Cu TSVs is highly localized and predominantly confined to the outer radial region of the via. In contrast, standard Cu TSVs exhibit a markedly different annealing response. Following annealing at 300°C and 400°C, the surface becomes increasingly rough, with widespread, grain-dependent protrusion. Individual grains undergo nonuniform expansion, leading to pronounced surface roughness, the formation of small gaps, and microcracks along grain boundaries. This behavior reflects a more spatially distributed and less controlled structural response during high temperature annealing in the absence of stabilizing twin boundaries. Cross-sectional observations in Supplementary Fig. S4. provide further insight into the origin of the surface features observed in NT-Cu TSVs. After annealing at 300°C and 400°C, distinct protrusions are observed in the upper region of the via at the interface between the central nanotwinned region and the surrounding transition layer. These protrusions are more pronounced at 400°C, consistent with the trend observed in the top-view images. EBSD maps reveal that, even after high-temperature annealing, the grain size within the transition layer remains significantly smaller than that in the central nanotwinned region, while the columnar grains in the via interior, particularly in the middle and upper regions, remain continuous and well aligned. This contrast highlights the different microstructural responses of the central NT region and the transition layer during annealing.

Taken together, the top-view and cross-sectional results demonstrate that the annealing response of NT-Cu TSVs is strongly region dependent. Surface protrusion and microstructural evolution originate primarily from localized changes within the transition layer rather than from uniform deformation of the entire via. The central nanotwinned region exhibits substantially greater thermal stability, with minimal grain coarsening and surface deformation, whereas most annealing-induced changes are confined to the geometrically constrained transition layer. Supplementary Fig. S6 illustrates the evolution of grain boundary networks during Monte Carlo grain growth simulations for conventional Cu TSVs and nanotwinned Cu TSVs using the twin-aware normal grain growth model. For both TSV types, the eventual emergence of bamboo-like grain morphologies arises from the combined effects of nearly isotropic grain growth kinetics and strong geometric confinement imposed by the moderate-aspect-ratio via geometry. However, the presence of stable twin boundaries introduces pronounced deviations from classical grain growth behavior. Coherent twin boundaries act as effective pinning features that impede grain boundary migration, modify local growth kinetics, and delay microstructural stabilization.

In summary, this work demonstrates that the microstructural evolution of nanotwinned copper under thermal annealing is fundamentally governed by the interplay between geometric confinement and twin boundary stability. Through combined same-via experimental characterization and twin-aware grain growth modeling, we show that moderate-aspect-ratio

nanotwinned Cu TSVs retain stable columnar grains and high densities of coherent twin boundaries, while grain coarsening is largely confined to transition regions near geometric constraints. In contrast, conventional Cu TSVs exhibit more uniform and rapid grain growth throughout the via. The results reveal that coherent twin boundaries not only suppress grain boundary mobility but also fundamentally alter grain growth kinetics under confinement, leading to non-classical evolution behavior. These findings provide new mechanistic insight into how microstructural stability can be engineered through twin boundary control and geometric design, offering a foundation for developing thermally robust interconnects for next-generation three-dimensional integration technologies.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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