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***Abstract*—This work introduces the symmetric dual inductor hybrid (SDIH) dc-dc converter topology, which is suitable for large conversion ratios where regulation is required, such as direct 48 V to point-of-load (PoL) applications. A dickson-type switched capacitor network is used to effectively produce two interleaved PWM outputs with a greatly reduced voltage amplitude relative to the input voltage, allowing the subsequent magnetic volume to be reduced while retaining modest switching frequencies. Distinct from related variations, part count is significantly reduced while both even and odd order switched capacitor networks can be used with straightforward split-phase control; allowing either network type to achieve complete soft-charging of all flying capacitors. Additionally, charge flow is uniformly distributed through all elements, with equal capacitor and inductor values being preferred. Subsequently this topology is expected to simplify component selection, improve electrical and thermal performance, and reduce cost. Furthermore, analysis is presented that calculates precise phase durations without making small ripple assumptions, revealing up to a 75% timing error in cases where either inductor or capacitor ripple is ignored. Finally, a discrete prototype validates this analysis and demonstrates very high measured power densities of 1,029 W/in^3, 754 W/in^3, and 663 W/in^3 for 48 V input and regulated output voltages of 3 V, 2 V, and 1 V, respectively, while switching at a frequency of 750 kHz.**

***Index Terms*—dc-dc power conversion, hybrid switched capacitor circuits, split-phase switching, point of load, VRM.**

I. Introduction

As power consumption continues to increase in both data center and telecommunication systems the prevalence of higher bus voltages, such as 48 V, have become common place in an attempt to reduce ohmic loss during power distribution. However, this shift towards high voltage local power distribution necessitates highly compact power converters with very large conversion ratios as well as regulation capability, which can be situated proximal to the intended low voltage load. As such, significant effort has been put into improved power delivery techniques, with power density and efficiency being key metrics used in surveying eligible converter architectures. One common solution is to use a two-stage approach whereby a 48 V bus is first converted to an intermediary voltage (e.g. 12 V) before being stepped down to ∼1 V using voltage regulation modules (VRMs) [2]–[6].

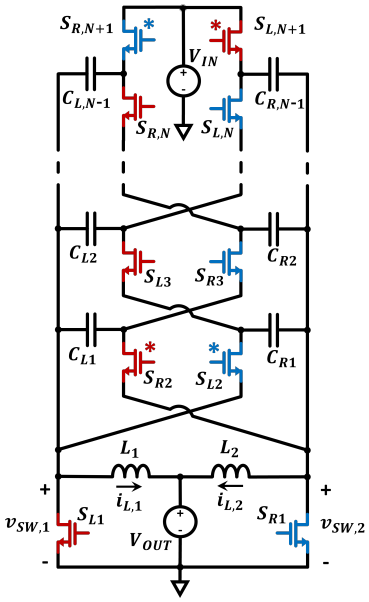

Figure 1. Proposed Symmetric Dual-Inductor Hybrid (SDIH) PoL converter. Switches requiring mirrored split-phase switching [7] are marked with an asterisk (*), assuming all flying capacitors are equal in size.

Alternatively, direct 48 V to point-of-load (PoL) architectures have been proposed with reduced cost and further improved power conversion efficiency and/or density expected. Of these direct approaches, transformer-based solutions have received much interest [8], [9]. In addition, stacked composite structures (e.g. [10]) can further leverage soft-switching and partial power processing [11] by using a fixed ratio DCX stage — such as a resonant LLC — to perform the majority of voltage conversion, while simultaneously enhancing the output regulation range.

Separately, soft-charged [12] or "hybrid" switched-capacitor (HSC) networks, including that depicted in Fig. 1, also demonstrate very high performance [13]–[16]. This approach circumvents the slow switching limit (SSL [17]) and associated transient pulse inrush currents that typically inhibit purely capacitor-based converters from availing of capacitor's high energy densities [18]. To do so, inductors are strategically placed into a capacitor network, preventing the occurrence

Manuscript received XXXXXXX; accepted XXXXXXXX. An earlier version of this paper [1] was presented in part at the 2022 Applied Power Electronics Conference (APEC) [DOI: 10.1109/APEC43599.2022.9773452]. This manuscript further contextualizes this work and includes new analysis and associated experimental verification that assists with design and allows control signals to be calculated without making small ripple assumptions. All figures have also been updated and measured converter performance has been improved. *(Corresponding author: Robert Carl Nikolai Pilawa-Podgurski.)*

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of SSL transient pulses without inhibiting voltage conversion. As a result, flying capacitors can experience large voltage ripple for greatly improved energy utilization [19] and reduced converter volume while preserving high efficiency. Moreover, the inductive elements are typically subjected to greatly reduced volt-seconds when compared with purely inductor-based conversion (e.g. buck/boost) and so can also be reduced substantially in size [20].

At fixed conversion ratios, several HSC designs are resonant and can achieve zero-current or zero-voltage switching (ZCS/ZVS) conditions similar to the popular LLC converter [21]–[23]. However, conduction and core losses typically dominate at heavy load, and so HSC's can alternatively be configured to operate with unipolar currents, including in continuous conduction mode (CCM), by placement of their inductors at the lowside terminal as opposed to within an internal tank structure [24], [25]. As a result, rms currents can be reduced and magnetic core polarity need not be periodically reversed. In addition, this approach provides improved immunity to component mismatch without increasing circulating currents when switching at frequencies above resonance. Furthermore, the ability to interleave phase-shifted PWM outputs and use coupled inductors in regulating designs has positive implications for transient response and maximum achievable slew rate in PoL converters [26], [27].

The drawback of the HSC approach is typically viewed as the high complexity and component count, with added concerns about reliability and cost. However, as noted in [20], dickson-type topologies can achieve best in class volt-amp switch utilization, signifying that while they may have an increased number of switches relative to more traditional architectures (e.g. buck, LLC, DAB), their net die area (in the case of a fully integrated solution) can be greatly improved. In addition, the proliferation of co-packaged gate drive and power semiconductor modules has reduced design complexity [28], with fully integrated solutions improving reliability through use of a monolithic process [29]–[32]. Moreover, the improved performance of these designs may lead to improved reliability as a result of reduced thermal management requirements and lower overall operating temperatures [33], [34].

As such, direct 48 V-to-1 V conversion is a highly active area of research without a clear consensus on best topological approach. In this work we expand on [1] by further introducing an additional converter topology for consideration; the symmetric-dual-inductor-hybrid (SDIH) converter, as depicted in Fig. 1. As will be discussed, it bears similarity to both the recently introduced dual-inductor-hybrid (DIH) converter [13] and the series-capacitor-buck (SCB) converter [35], with all three converters expressing the same volt-amp switch rating [17]. However, as a result of its symmetry the proposed design achieves balanced charge flow through both of its inductors and all of its switches at both even and odd conversion ratios, simplifying design effort and improving component utilization. In addition, it has an interleaved high-side input: when compared with two interleaved instances of either the DIH or the SCB converters—in order to yield identical line filtering requirements—the proposed SDIH topology requires significantly fewer parts.

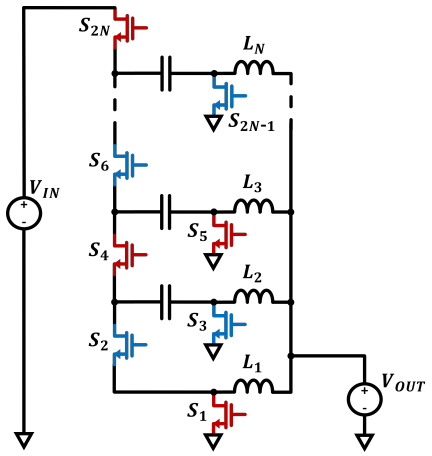

Figure 2. The series-capacitor-buck (SCB) topology, previously demonstrated in [35]–[38]. Switches active during the primary two switching phases are color-coded red and blue.

The rest of this article is organized as follows. Section II contextualizes the evolution of the SDIH by first assessing both the advantages and limitations of the SCB and DIH topologies. Section III formally describes the proposed SDIH topology, highlighting its differentiating features and characteristics. Section IV presents—for the first time—the steady-state large signal (i.e. incorporating the effect of ripple) analysis required to calculate precise timing durations for "split-phase" clocking [7] in a regulating HSC converter; a clocking scheme that is necessary to ensure complete soft-charging of the flying capacitors in several of the most competitive HSC topologies, including both the DIH and SDIH proposed here. Dissimilar to prior work, this analysis does not make any small ripple assumptions and allows the full large signal operating points to be calculated accurately. We demonstrate that previous analysis using small ripple assumptions may result in up to a 75% error in phase timings.

Section V introduces the first SDIH hardware prototype, with subsequent measurements validating the preceding analysis. A subsequent revision is then used to showcase extremely high power densities. The second version is then compared against recent state of the art 48 V-to-PoL converter solutions. Section VI concludes this work.

II. Prior Work

The SCB topology [35]–[38], depicted in Fig. 2, is a HSC structure that has been commercialized in recent years [31] due to its excellent performance in high conversion ratio regulated applications. As a ladder or dickson-type structure, it achieves among the best volt-amp switch stress and benefits from greatly reduced inductor volt-seconds as per fundamental HSC theory [20], [39]. In addition, recent topological variations have also been proposed that trade off switch performance for improved passive component utilization [40], [41]. Switch stress is minimized if the SCB is designed for regulation near its maximum switch duty cycle of 50%, resulting in largely two-phase operation, as color-coded in Fig. 2. Conversely, its conversion ratio may be increased by inserting additional tertiary phases within a switching period, during which odd

numbered (as labelled in Fig. 2) switches only are activated. During these intervals, the flying capacitors remain static and conduct zero charge while the left side of all inductors are temporarily shorted to ground. By regulating the duration of these tertiary phases with respect to the two primary phases depicted, pulse-width-modulated (PWM) regulation can be achieved. Additionally, as a result of charge conservation in the flying capacitors, current is balanced equally among all output inductors [42], provided that each inductor experiences the same PWM duty cycle. Furthermore, there are no sizing requirements imposed on the flying capacitors to avoid SSL losses, allowing the use of high density Class II multi-layer ceramic chip (MLCC) capacitors that offer high energy densities but poor component tolerance [43]. Moreover, at the cost of a further decreased duty cycle, the primary two phases of the capacitor network can be split into phase shifted sub-intervals, allowing each output inductor to operate with an interleaved fractional phase shift less than 180° [35], [44], [45]. While this approach may facilitate the effective use of interleaved coupled inductors for improved magnetic performance, the SCB is often operated with two predominant phases to increase the achievable duty cycle and subsequent switch performance, while simplifying control and resulting in the current ripple of every other inductor being in-phase, as in [36], [38].

Recognizing this phase alignment, the DIH topology improves upon the SCB by lumping together both in-phase inductors and ground referenced switches, greatly reducing the overall component count. The resulting DIH topology — of which there are two interleaved instances depicted in Fig. 3 — is largely equivalent to the SCB, retaining a highly competitive volt-amp switch stress rating and featuring a modestly improved magnetic utilization as a result of consolidated core material [46]. To clarify this transformation, switches S_1 and S_5 in Fig. 2 are combined together to produce switch S_{L1} in Fig. 3, while switches S_3 and S_{2N-1} in Fig. 2 effect switch $S_{L,N+2}$ in Fig. 3. Then, since inductors L_1 and L_3 operate in-phase in Fig. 2, they are combined to form inductor L_1 in Fig. 3. Similarly L_2 and L_N in Fig. 2 combine to form L_2 in Fig. 3. As a result of this consolidation, the DIH requires $N+2$ switches, versus the $2N$ required by the SCB for an Nth order HSC network.

However, dissimilar to the SCB — and as a result of the reduced inductor count — the DIH is subjected to finite flying capacitor sizing constraints in order to avoid SSL losses. Should capacitor values deviate from those prescribed, SSL losses will be reintroduced, but at a gradual rate commensurate with the degree of mismatch. An appropriate flying capacitor sizing scheme that allowed two primary phases to be retained was demonstrated in [47] for odd order capacitor networks only, however this solution leads to diverging capacitor values and excessive passive volume for flying capacitor networks of order $N > 6$, as derived in [48]. As initially noted in [13], a more effective solution is to set all flying capacitors equal in value and to instead employ the use of "split-phase" switching to avoid SSL losses [7], with [16] more recently demonstrating a preferred alternative split-phase control sequence for step-down applications. The split-phase technique involves the careful removal of specific flying capacitors from the conduction path part way through a primary conduction phase. That is, some flying capacitors only conduct charge for a sub-interval of a primary phase, effectively splitting it into two distinct parts. As a result, full SSL mitigation is retained with minimal added clocking complexity or impact on switch stress.

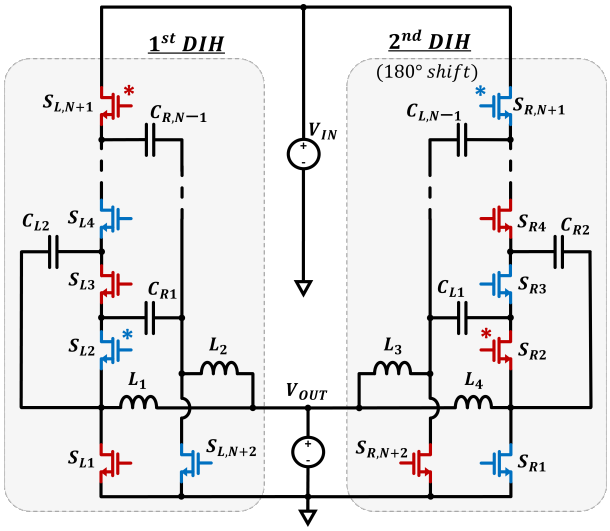

Figure 3. Two interleaved even-order DIH converters operating 180° out of phase for reduced input filtering requirements. Switches active during the two primary phases are color-coded red and blue. Switches marked with an asterisk (*) must undergo split-phase switching to preserve complete SSL mitigation, assuming all flying capacitors have equal value. This arrangement can be consolidated into the proposed SDIH topology depicted in Fig. 1 by combining specific switches and inductors.

Despite these advancements, odd ordered DIH converters still suffer from asymmetric current stress which leads to complications with component selection and thermal management. Furthermore, analysis calculating the timing durations of split-phase intervals has been presented, but has historically made zero ripple assumptions about either inductor current ripple, as in [7], or flying capacitor voltage ripple, as in [13]. As will be demonstrated here, these assumptions can lead to significant timing errors when a converter is operated under large ripple conditions, as is desired for effective passive utilization. Subsequently, Section IV presents analysis that yields accurate split-phase control of a regulating HSC converter without making any small ripple assumptions.

III. Proposed SDIH Converter

To arrive at the proposed topology depicted in Fig. 1, first consider two instances of the even-order DIH topology arranged in an interleaved manner with a 180° phase shift, as depicted in Fig. 3. Here, all flying capacitors are assumed to be equal in value and switches $S_{X,2}$ and $S_{X,N+1}$ are marked with an asterisk, denoting their requirement for split-phase switching. Since both primary phase durations — including the split-phase intervals therein — are identical in an even-order DIH, switch pairs $\{S_{L2}, S_{R,N+1}\}$ and $\{S_{R2}, S_{L,N+1}\}$ can leverage the same split-phase control signal. Moreover, the timing of only one split-phase event need be calculated in practice, with this interval copied through both primary phases. As a result,

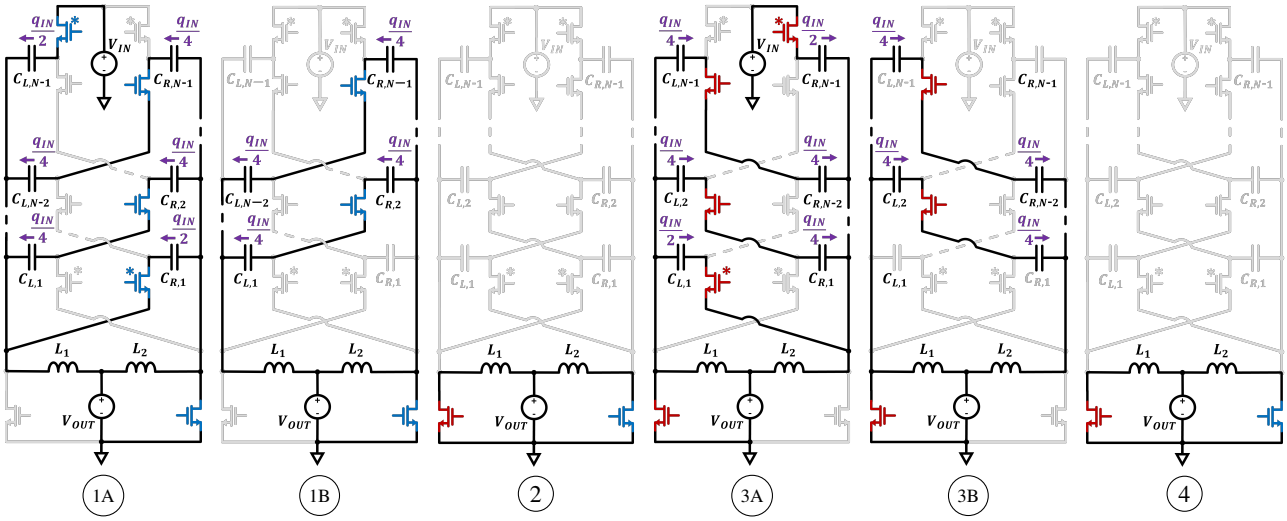

Figure 4. Periodic phase progression of the proposed SDIH converter (left to right) when optimized for step-down split-phase operation. Phases 1 and 3 are split into sub-intervals, A and B, to facilitate split-phase switching. The four switches requiring split-phase operation are marked with an asterisk (*) and reside only at the extreme ends of the switched-capacitor network, for all $N \geq 3$, when all fly capacitors are set equal to C_0. Charge flow through each flying capacitor is annotated and expressed relative to the total periodic input charge quantity q_{IN} that is admitted during phases 1A and 3A.

Table I
COMPONENT COUNT COMPARISON

	Single	Dual-Interleaved	
Topology	SDIH	DIH	SCB
# Switches	2N+2	2N+4	4N
# Inductors	2	4	2N

this arrangement does not add any control complexity relative to a single even-order DIH, while facilitating an interleaved high-side port for reduced input filtering requirements at V_{IN}.

To reduce this configuration into the proposed SDIH topology depicted in Fig. 1, the circuit node at the drain of S_{L1} is merged with that at the drain of $S_{R,N+2}$, with both switches combining into a single device, labelled S_{L1} in Fig. 1. A similar reduction is made for S_{R1} and $S_{L,N+2}$. As a result, the overall switch count is reduced by two. In addition, since inductor pairs $\{L_1, L_3\}$ and $\{L_2, L_4\}$ are now in parallel, they can be combined and the inductor count is halved, further benefiting from the scaling argument posed in [46]. To contextualize this reduction in component count, Table I lists the number of switches and inductors required by the proposed SDIH in comparison with two interleaved instances of both the DIH and SCB, where the latter two are interleaved to ensure identical input and output filtering requirements for fair comparison. Here, the proposed SDIH topology requires significantly fewer parts, with its reduced switch count additionally alleviating gate-drive and level-shift requirements.

While even-order DIH networks are depicted in Fig.3, odd-order DIH networks experience asymmetric phase control with split-phase switching only required during one of the two primary phases. In this case, the second interleaved DIH would require an independent set of 180° shifted control signals, adding to the control complexity. In addition, as noted in [47], switches S_{X1} and $S_{X,N+2}$ would conduct unequal charge, leading to a current imbalance between the DIH's two inductors. Fortunately, these complexities do not extend to the merged SDIH structure, where complete symmetry is imposed for both odd and even order capacitor networks. As a result, control effort is minimal for any capacitor network order N, and component selection is simplified with all mirrored components carrying identical rms currents.

Figure 4 depicts the intended phase progression for the SDIH topology, including two additional regulation phases, 2 and 4, in which both inductors are grounded. Primary phase 1 is split into sub-intervals 1A and 1B to facilitate split-phase constraints, while phases 3A, 3B, and 4 are mirrored copies of phases 1A, 1B, and 2, respectively. As such, only three time intervals need be calculated to define a given operating point (versus the two required by a basic buck converter operating in continuous conduction mode).

As a regulating converter operating in continuous conduction mode, hard-switching losses are expected. However, similar to a conventional buck converter, low-side switches S_{L1} and S_{R1} may achieve ZVS turn-on upon commencement of phases 2 and 4, respectively, provided that sufficiently long preceding dead-time intervals are implemented. During these dead-time intervals, current in L_1 and L_2 serves to discharge $v_{SW,1}$ and $v_{SW,2}$, respectively, to 0 V. Simultaneously, associated high-side switches are also partially discharged, leading to improved high-side related switching losses. Switching losses are otherwise addressed using conventional means and are not elaborated on further in this work.

IV. STEADY-STATE ANALYSIS

This section details the steady-state analysis required to derive the appropriate duration of each phase interval, subject to a given operating point. Similar analysis was conducted in [7], which assumed zero inductor current ripple, and [13], which assumed zero flying capacitor voltage ripple. The analysis presented here does not make any small ripple assumptions

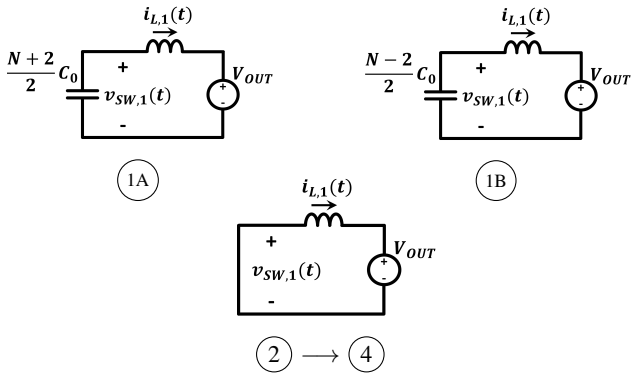

Figure 5. Equivalent circuit states from the perspective of inductor L_1.

and its improved accuracy is validated in hardware in Section V. Similar to previous efforts, lossless conversion is assumed, with the impact of ohmic voltage droop in a high efficiency design deemed to have a negligible impact on relative split-phase timing relationships, although the conversion ratio may need some compensation in practice. Continuous forward conduction in both inductors is also assumed, although the boundaries of both discontinuous conduction mode (DCM) and maximum capacitor ripple will be highlighted. In addition, only one half of the SDIH's operation need be considered as a result of its complete symmetry. That is, only waveforms $i_{L,1}(t)$ and $v_{SW,1}(t)$ are assessed, with the understanding that $i_{L,2}(t)$ and $v_{SW,2}(t)$ are identical bar a 180° phase shift. All flying capacitors and inductors are set equal to C_0 and L, respectively, for simplified part selection, minimal split-phase complexity, and uniform loss distribution.

In order to account for both large signal flying capacitor voltage ripple and inductor current ripple simultaneously, second order LC networks must be considered. Figure 5 depicts the lumped equivalent capacitance, as a function of N, presented to inductor L_1 during phases 1A and 1B. For the remaining phases L_1 is connected across V_{OUT} and sees a linear decrease in current. Figure 6 depicts the associated generalized waveforms for both inductor current i_{L1} and switch node voltage $v_{SW,1}$. Also annotated in Fig. 6 is the natural frequency response during 1A and 1B:

$$\omega_{1A} = \frac{1}{\sqrt{LC_0\frac{N+2}{2}}} \tag{1}$$

$$\omega_{1B} = \frac{1}{\sqrt{LC_0\frac{N-2}{2}}} \tag{2}$$

Additionally, we note the general expressions for an arbitrary LC tank that account for initial inductor current and capacitor voltage:

$$i_L(t) = i_L(0)\cos(\omega t) + v_C(0)\sqrt{\frac{C}{L}}\sin(\omega t) \tag{3}$$

$$v_C(t) = v_C(0)\cos(\omega t) - i_L(0)\sqrt{\frac{L}{C}}\sin(\omega t) \tag{4}$$

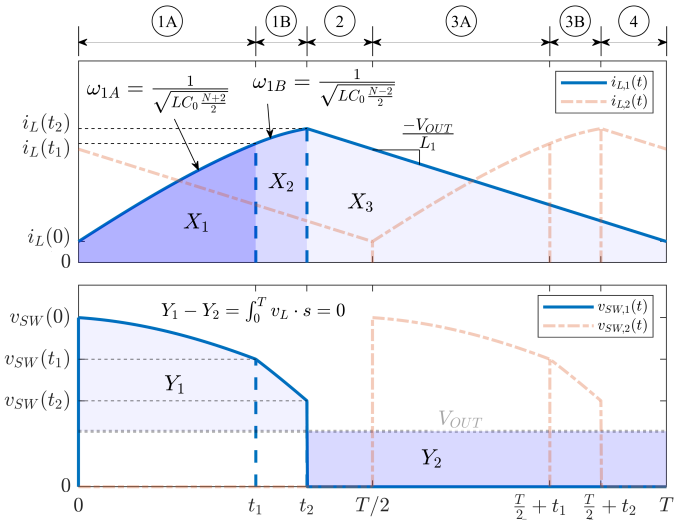

Figure 6. Generalized steady-state i_L and v_{SW} waveforms through one full switching period of duration T.

Using (3) and (4), general expressions for $i_{L1}(t)$ and $v_{SW,1}(t)$ accounting for initial current and voltage can be expressed as

$$i_{L,1}(t) = i_{L,1}(0)\cos(\omega_{1A}t) + (v_{SW,1}(0) - V_{OUT})\sqrt{\frac{C_0}{L}\frac{N+2}{2}}\sin(\omega_{1A}t), \tag{5}$$

$$v_{SW,1}(t) = V_{OUT} + (v_{SW,1}(0) - V_{OUT})\cos(\omega_{1A}t) - i_{L,1}(0)\sqrt{\frac{L}{C_0}\frac{2}{N+2}}\sin(\omega_{1A}t) \tag{6}$$

during interval $\{0, t_1\}$, and

$$i_{L,1}(t) = i_{L,1}(t_1)\cos(\omega_{1B}(t-t_1)) + (v_{SW,1}(t_1) - V_{OUT})\sqrt{\frac{C_0}{L}\frac{N-2}{2}}\sin(\omega_{1B}(t-t_1)), \tag{7}$$

$$v_{SW,1}(t) = V_{OUT} + (v_{SW,1}(t_1) - V_{OUT})\cos(\omega_{1B}(t-t_1)) - i_{L,1}(t_1)\sqrt{\frac{L}{C_0}\frac{2}{N-2}}\sin(\omega_{1B}(t-t_1)) \tag{8}$$

during interval $\{t_1, t_2\}$.

Furthermore, during interval $\{t_2, T\}$;

$$i_{L,1}(t) = i_{L,1}(t_2) - \frac{V_{OUT}}{L_1}(t-t_2), \tag{9}$$

$$v_{SW,1}(t) = 0\,\text{V} \tag{10}$$

Next, we obtain expressions for the instantaneous value of v_{SW} at each phase transition ($v_{SW}(0)$, $v_{SW}(t_1)$, and $v_{SW}(t_2)$), temporarily ignoring the in-phase transitional dynamics described by (5)-(10). To do so, first charge flow analysis similar to that presented in [48] is applied to the flying capacitor network depicted in Fig. 4 to deduce the relative charge flow through all flying capacitors, using the input

charge q_{IN} provided by V_{IN} each period as a normalizing charge quantity. That is;

$$q_{IN} = \frac{I_{IN}}{f_{SW}} = q_{OUT}\frac{V_{OUT}}{V_{IN}} \tag{11}$$

where f_{SW} is the converter's switching frequency. Note that since all flying capacitors have been set equal to C_0, any branch containing two capacitors connected in series expresses twice the net impedance — and conducts half as much charge per unit time — as a branch containing a single capacitor. In addition, since each flying capacitor conducts the same net quantity of charge per period, the split-phase transition between 1A and 1B occurs once half of the total charge required by each series connected branch has been conducted. Using this result, the areas X_1, X_2, and X_3, depicted in Fig. 6 can be generally expressed as

$$X_1 = \frac{N+2}{4}q_{IN} \tag{12}$$

$$X_2 = \frac{N-2}{4}q_{IN} \tag{13}$$

$$X_3 = \frac{V_{IN}}{V_{OUT}}\frac{q_{IN}}{2} - N\frac{q_{IN}}{4} \tag{14}$$

where X_3 is obtained by subtracting X_1 and X_2 from the total charge conducted by L_1 each period.

In addition, an expression for the mid-range dc voltage stored on each flying capacitor is obtained using the large signal KVL analysis presented in Section VI of [48]:

$$V_{C_{L,i}} = V_{C_{R,i}} = i\frac{V_{IN}}{N} + \Delta V\frac{N-2i}{N} \tag{15}$$

where i denotes capacitor numbering as depicted in Figures 1 and 4, and ΔV is half the total peak-to-peak voltage ripple expressed on each flying capacitor

$$\Delta V = \frac{q_{IN}}{4C_0} \tag{16}$$

i.e. each flying capacitor is exercised over the voltage range $V_{C_{X,i}} \pm \Delta V$.

Subsequently, expressions for the instantaneous value of v_{SW} at each phase transition can be obtained via KVL, where (15) and (16) ensure that large signal voltage ripple on the flying capacitors is accounted for.

$$v_{SW}(0) = V_{C_{R,1}} + \Delta V \tag{17}$$

$$v_{SW}(t_1) = V_{C_{R,1}} - \Delta V \tag{18}$$

$$v_{SW}(t_2) = V_{C_{R,2}} - V_{C_{L,1}} - 2\Delta V \tag{19}$$

Having obtained expressions (1)-(19), the converter's steady-state operating point and phase timings, t_1 and t_2, can be accurately solved for as a function of input parameters V_{IN}, V_{OUT}, N, f_{SW}, I_{OUT} (or I_{IN}), C_0, and L. However, as a result of non-linear trigonometric functions, a closed-form solution is non-trivial. Instead, this system of equations is solved numerically with relative ease.

One straight-forward numerical approach is to set an initial guess for $i_{L,1}(0)$ and use this value to progress through (5)-(10), using equations (17)-(19) to determine when a transition to a subsequent phase interval can occur. This results in a value for $i_{L,1}(T)$ at the end of a switching period. This process can then be repeated, adjusting the initial $i_{L,1}(0)$ value, until $i_{L,1}(T) = i_{L,1}(0)$, signifying the arrival at a periodic steady-state solution. Conveniently, the full $i_{L,1}(t)$ waveform is obtained, assisting with any subsequent loss estimation.

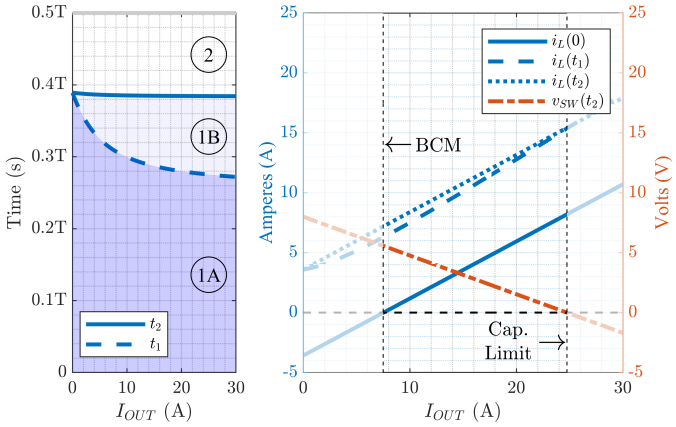

Figure 7. Calculated full-ripple phase durations (left) and operating points (right) both plotted versus load current I_{OUT}. Below 7.5 A the inductor experiences reverse conduction. For $I_{OUT} > 24.75$ A, capacitor ripple increases to the extent that v_{SW} swings below 0 V inducing unintended reverse conduction in switches. $V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, $N = 6$, $f_{SW} = 250$ kHz, $C_0 = 496$ nF, $L = 1.125\,\mu$H.

Figure 7 (left) depicts calculated phase durations plotted versus output load, I_{OUT}, where the time axis is represented as a fraction of total period T. Parameter t_1 is observed to have a strong dependence on load. Figure 7 (right) plots the value of i_L at each instantaneous phase transition giving insight into the inductor's current ripple and dc bias. For $V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, $N = 6$, $f_{SW} = 250$ kHz, $C_0 = 496$ nF, and $L = 1.125\,\mu$H, we see that the lower bound for continuous forward conduction, or boundary conduction mode (BCM), should occur at 7.5 A, below which the inductor current experiences negative current flow unless the clocking scheme is altered to facilitate DCM. Also plotted is $v_{SW}(t_2)$ which is the lowest driving voltage applied to L_1 throughout phases 1A and 1B. As flying capacitor voltage ripple increases with load, $v_{SW}(t_2)$ tends towards 0 V. Should $v_{SW}(t_2)$ reach 0 V, reverse conduction in switch S_{L1} is likely, representing an equivalent capacitor induced DCM.

To compare this approach with prior analysis using small ripple approximations, Fig. 8 plots the calculated steady-state waveforms of $v_{SW,1}$ and $i_{L,1}$ under three sets of assumptions: First, assuming zero inductor current ripple (green), as in [7]. Here $i_{L,1}$ is constant and $v_{SW,1}$ changes with a constant slope. Second, assuming zero capacitor voltage ripple (red) [13], where $v_{SW,1}$ is flat and equal to V_{IN}/N during phases 1A and 1B, and $i_{L,1}$ changes linearly due to a constant voltage being applied to L_1 during each phase. Third, assuming full ripple on both capacitors and inductor (This Work). Here both $i_{L,1}$ and $v_{SW,1}$ follow sinusoidal segments during phases 1A and 1B. An operating point is chosen at which both large flying capacitor voltage ripple and inductor current ripple are expected; this both emphasizes the differences between each case and maximizes given passive component utilization. The

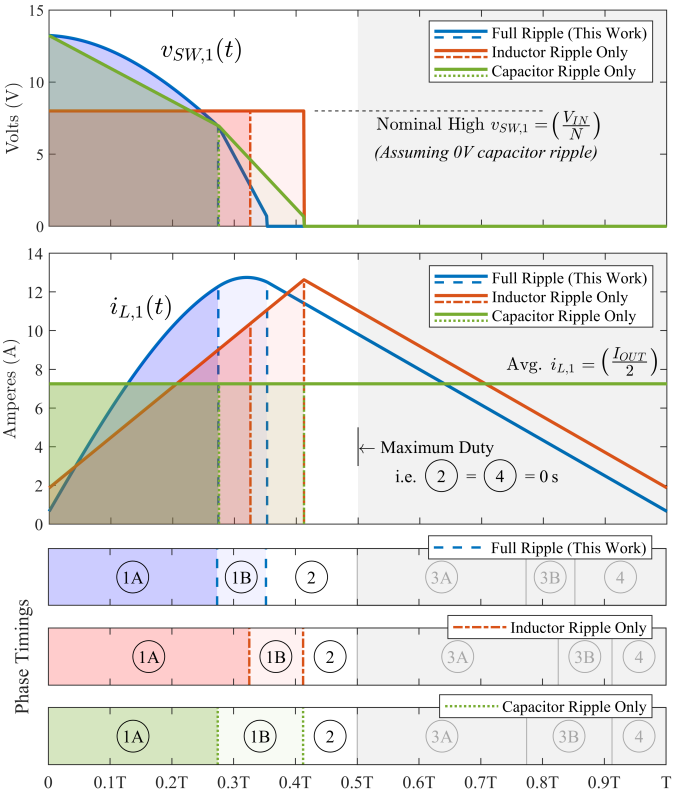

Figure 8. Theoretical switch node voltage $v_{SW}(t)$ (top), inductor current waveform $i_L(t)$ (middle), and phase durations (bottom) for three scenarios: Assuming flying capacitor ripple only (green), inductor ripple only (red), and both capacitor and inductor ripple (blue), the latter being the analysis presented in this work. Phase 1A sees up to 19% timing error when capacitor ripple is neglected, while Phase 1B can have up to 75% timing error when inductor ripple is assumed negligible. $V_{IN} = 48\,\text{V}$, $V_{OUT} = 3.3\,\text{V}$, $I_{OUT} = 14.5\,\text{A}$, $N = 6$, $f_{SW} = 160\,\text{kHz}$, $C_0 = 496\,\text{nF}$, $L = 1.125\,\mu\text{H}$.

area under the curve of $i_{L,1}$ during phases 1A and 1B (X_1 and X_2 in Fig. 6) is identical between the three cases, ensuring (12)-(14) are always satisfied. However, the calculated phase timings required in order to meet these constraints varies depending on which set of assumptions are used.

For example, when using this work's full ripple assumptions, phase 1B is expected to finish much sooner than predicted by either of the other two cases (shorter t_2). Furthermore, while the time ratio of phase 1B to phase 1A is approximated well when only inductor ripple is accounted for, as in [13], the absolute duration of both phases is 19% longer than that predicted by the full ripple case. As a result, the converter's output voltage is expected to be be higher than intended. Moreover, the absolute duration of phase 1B deviates by up to 75% when comparing the full ripple case with that ignoring inductor current ripple.

V. Experimental Results

A hardware prototype of an $N = 6$ SDIH converter, photographed in Fig. 9, was constructed on a 4-layer 0.6 mm thick PCB to validate both the functionality of the proposed topology and the improved accuracy of the preceding full ripple analysis. Power was delivered to the gate-drivers of all fourteen switches using cascaded bootstrapping [49], as

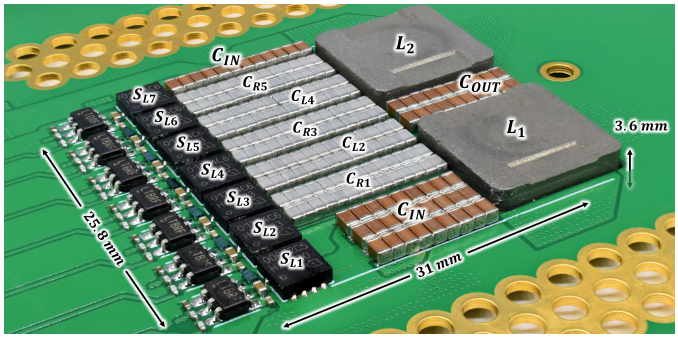

Figure 9. Photograph of the constructed SDIH prototype with a capacitor network order of $N = 6$. Due to the proposed topologies symmetry, the reverse side is largely identical with inverse component naming on flying capacitors and switches. A best-fit cuboid encompassing all components measures 25.8 mm x 31 mm x 3.6 mm, where the converter's overall height is limited by through-plane inductors L_1 and L_2.

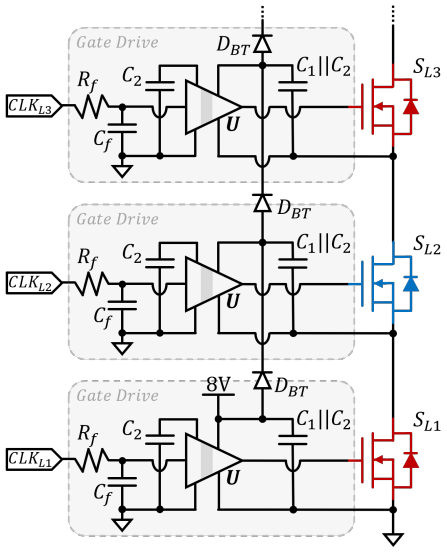

Figure 10. Schematic of the level-shifted gate driving circuitry and cascaded bootstrap power delivery using an 8 V supply, depicted for switches $S_{L1} - S_{L3}$. This same scheme is used for all primary switches $S_{L1} - S_{L7}$ and $S_{R1} - S_{R7}$.

illustrated in Fig. 10. Here charge is handed from the gate driving circuitry of switch $S_{X,i}$ to that of switch $S_{X,i+1}$, via bootstrapping diode D_{BT} during the on-time of switch $S_{X,i}$. This approach tolerates an accumulation of successive diodes drops and may be improved through the introduction of synchronous bootstrapping [50] at the cost of added complexity. Table II lists all of the components used. A HFS9003 clock generator was used to provide clock signals to the input of each level-shifted gate driver. Despite their reduced energy density relative to Class II dielectrics, Class I (C0G) fly capacitors were used here for both their fine matching tolerance, stability, and low loss when subject to large voltage ripple [43], [51].

Two different pairs of inductors were implemented: larger stable ferrites (1 μH) were implemented when validating the preceding timing analysis since this choice minimizes the effects of parasitics and probing and omits the added complexity of inductance derating with load (applicable to Figures 12-14). Conversely, small 150 nH composite core inductors were used

Table II
COMPONENT DETAILS FOR DISCRETE HARDWARE PROTOTYPE

Component	Details	Part Number
L_1, L_2	150 nH 55 A 0.75 mΩ 1 μH$^{(a)}$ 37 A 1.3 mΩ	IHLW-4040CF-11 SER1412-102MED
C_{IN}, C_{OUT}	98× 2.2 μF X5R 0603	GRT188R61H225KE13D
$C_{\text{L,1-5}}$, $C_{\text{R,1-5}}$	28× 18 nF$^{(b)}$ C0G 0603	C1608C0G1V183J080AC
S_{L1}, S_{R1}	0.65 mΩ 25 V 298 A	IQE006NE2LM5CGATMA1
$S_{\text{L,2-7}}$, $S_{\text{R,2-7}}$	1.35 mΩ 40 V 205 A	IQE013N04LM6CGATMA1
U	High-side Gate Driver	LTC4440
D_{BT}	30 V 0.5 A Schottky	VSKY05301006
C_1	2.2 μF 0402	C1005X5R1V225K050BC
C_2	0.1 μF 0201	C0603X5R1E104K030BB
C_{f}	20 pF 0201	GRM0335C1H200JA01D
R_{f}	100 Ω 0201	RMCF0201FT100R

$^{(a),(b)}$Measured values of 1.125 μH and 496 nF were used in practice.

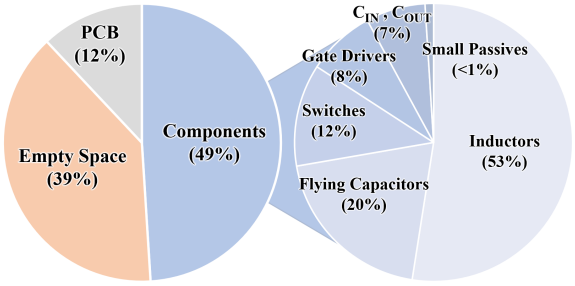

Figure 11. Volume breakdown of the hardware prototype. Overall converter volume breakdown (left) and component volume breakdown (right).

to demonstrate this topology's capability for very high power densities and improved transient response at an increased switching frequency of 750 kHz. Figure 11 depicts the high density revision's volume breakdown where total converter volume is defined as a best-fit cuboid encompassing the entire design, including input and output capacitors.

To begin, Fig. 12 generally illustrates the necessity for split-phase switching in applicable topologies when flying capacitors are operated with large ripple for improved utilization. Here, the voltage on each left-sided flying capacitor is plotted across a full switching period in steady-state. While not plotted for clarity, all right-sided flying capacitors express identical waveforms, albeit with a 180° phase shift. Smooth voltage transitions on the flying capacitors implies complete soft-charging and full mitigation of SSL losses. In contrast, when split-phase operation is disabled — and phases 1B and 3B are effectively removed — abrupt step changes in flying capacitor voltages are observed, signifying the re-introduction of pulsed inrush currents and SSL loss. As a result, measured converter efficiency is severely degraded from 87.1% to 82.7%.

Next, the same operating point as that depicted in Fig. 7 was recreated in hardware. Figure 13 illustrates operation both at the minimum boundary inductor current before DCM and at the point of maximum flying capacitor voltage ripple while

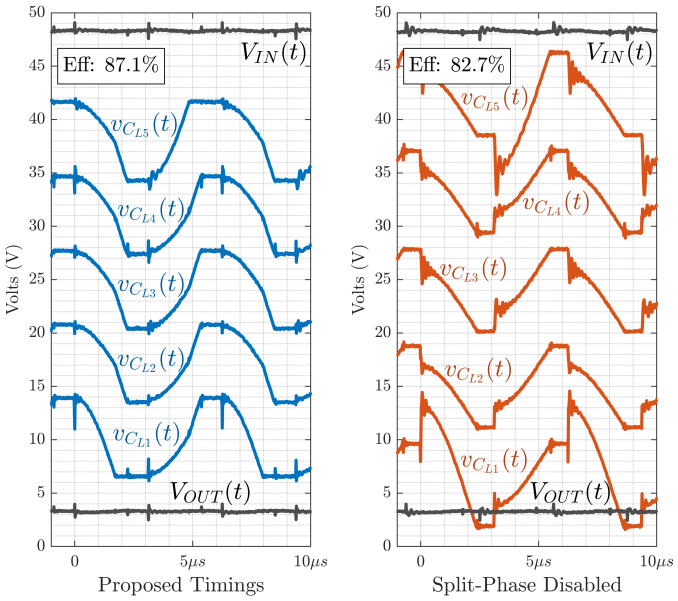

Figure 12. Measured flying capacitor waveforms with this work's control scheme (left) and with split-phase switching disabled (right). Large voltage ripple implies effective capacitor utilization. Smooth voltage transitions imply soft-charging, whereas abrupt voltage transitions indicate pulsed inrush currents and slow-switching-limit losses. $V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, $N = 6$, $f_{SW} = 160$ kHz, $C_0 = 496$ nF, $L = 1.125$ μH, $I_{load} = 14.5$ A.

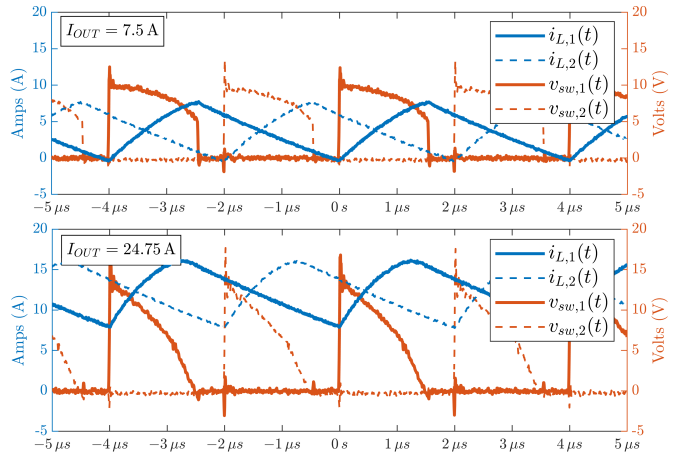

Figure 13. Measured i_L and v_{SW} waveforms that validate the calculated large ripple operating points depicted in Fig. 7. A minimum load of $I_{OUT} = 7.5$ A demonstrates BCM (top), and a maximum load of $I_{OUT} = 24.75$ A results in v_{SW} reaching 0 V (bottom). $V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, $N = 6$, $f_{SW} = 250$ kHz, $C_0 = 496$ nF, $L = 1.125$ μH.

using phase durations calculated without making small ripple assumptions. Here, both $i_{L,1}(t)$ and $i_{L,2}(t)$ current waveforms reach 0 A when $I_{OUT} = 7.5$ A, while both $v_{SW,1}(t)$ and $v_{SW,2}(t)$ waveforms swing to 0 V for $I_{OUT} = 24.75$ A. These operating points align precisely with that predicted by Fig. 7.

To further motivate the presented full ripple analysis in contrast to simplified approaches, the operating point described in Fig. 8 was also recreated. Figure 14 plots measured $v_{SW,1}(t)$ waveforms for the converter operating with both 1) full ripple timings, and 2) timings assuming flying capacitor ripple only. When inductor current ripple is neglected, the required duration of phase 1B is greatly overestimated. Subsequently,

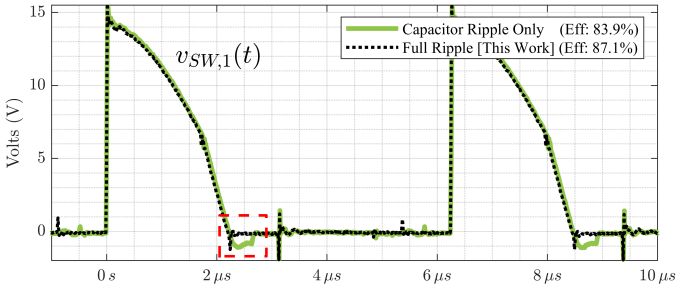

Figure 14. Measured $v_{SW,1}(t)$ waveforms validating the presented large ripple analysis and illustrating a prolonged reverse conduction interval (highlighted) when inductor current ripple is neglected. For both waveforms; $V_{IN} = 48\,\text{V}$, $V_{OUT} = 3.3\,\text{V}$, $N = 6$, $f_{SW} = 160\,\text{kHz}$, $C_0 = 496\,\text{nF}$, $L = 1.125\,\mu\text{H}$, $I_{load} = 14.5\,\text{A}$.

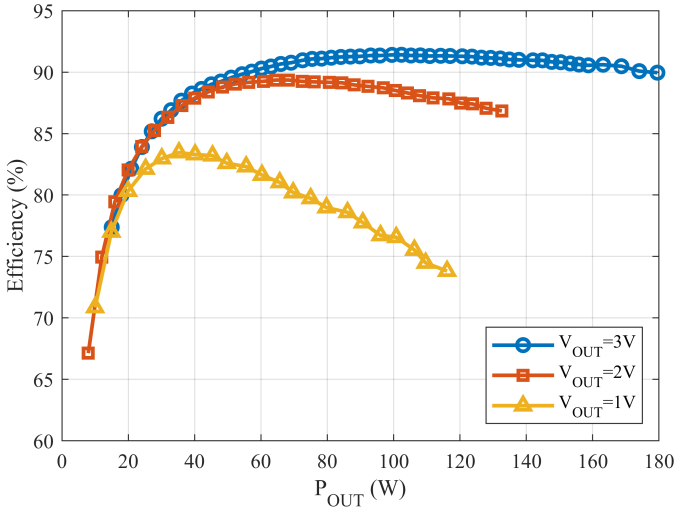

Figure 15. Measured efficiency curves for a discrete hardware prototype demonstrating the proposed SDIH converter topology and operating using the derived full ripple split-phase control scheme. $V_{IN} = 48\,\text{V}$, $N = 6$, $f_{SW} = 750\,\text{kHz}$, $C_0 = 496\,\text{nF}$, $L = 150\,\text{nH}$.

unintended reverse body diode conduction is observed for a significant portion of the total switching period. Conversely, the full ripple analysis provides more accurate control and removes the unintended freewheeling interval and associated reverse conduction loss. Subsequently, measured converter efficiency is increased from 83.9% to 87.1%.

When phase timings accounting for inductor ripple only are used instead, the relative timing of phase 1A to 1B is approximately accurate, as noted in Section IV, and correct soft-charging operation is preserved. However, as a result of the error in absolute duration of phases 1A and 1B, the output voltage increases above its intended operating point of 3.3 V (not depicted).

Finally, L_1 and L_2 were replaced with the smaller 150 nH inductors and the converter's switching frequency was increased to 750 kHz to extend its maximum achievable output power. Figure 15 plots measured efficiency versus output power at output voltages of 3 V, 2 V and 1 V, and omits a gate drive power loss of $1.62\,\mu\text{J}$ per switching period to facilitate a fair comparison with data reported in prior art. In addition, Fig. 16 and Fig. 17 depict transient output voltage steps from

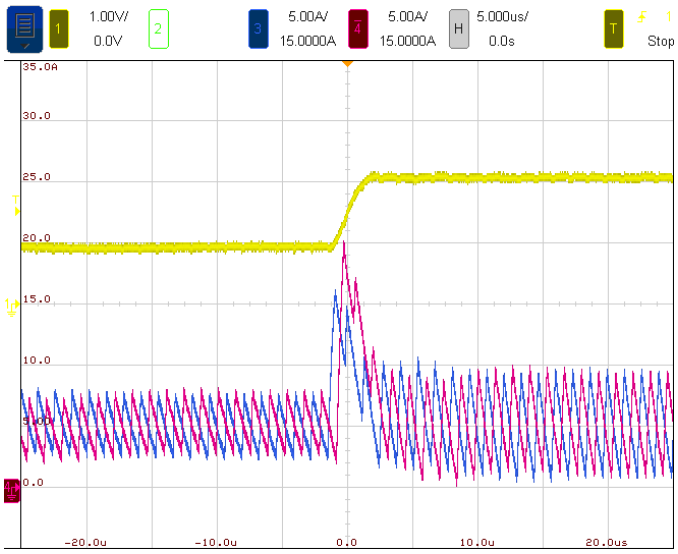

Figure 16. Measured current waveforms, $i_{L,1}(t)$ (blue), $i_{L,2}(t)$ (red), and output voltage, $V_{OUT}(t)$ (yellow), under a controlled voltage step from 1 V to 2 V. $V_{IN} = 48\,\text{V}$, $I_{OUT} = 10\,\text{A}$, $N = 6$, $f_{SW} = 750\,\text{kHz}$, $C_0 = 496\,\text{nF}$, $L_1 = L_2 = 150\,\text{nH}$.

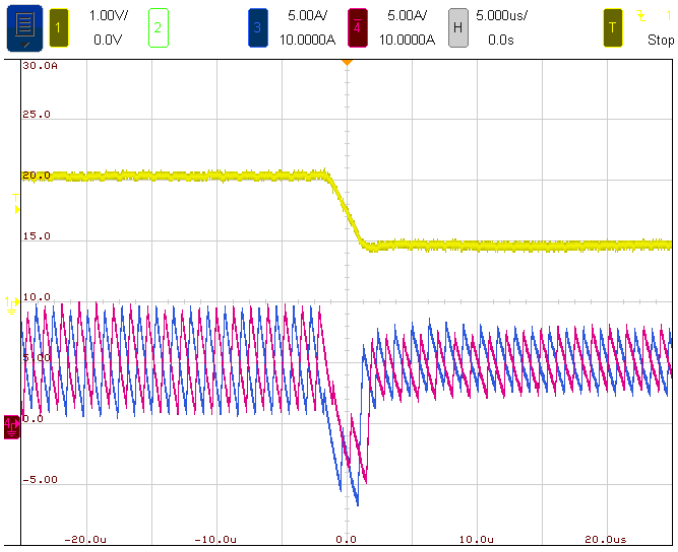

Figure 17. Measured current waveforms, $i_{L,1}(t)$ (blue), $i_{L,2}(t)$ (red), and output voltage, $V_{OUT}(t)$ (yellow), under a controlled voltage step from 2 V to 1 V. $V_{IN} = 48\,\text{V}$, $I_{OUT} = 10\,\text{A}$, $N = 6$, $f_{SW} = 750\,\text{kHz}$, $C_0 = 496\,\text{nF}$, $L_1 = L_2 = 150\,\text{nH}$.

1V-to-2V and 2V-to-1V, respectively, for a constant load current of $I_{OUT} = 10\,\text{A}$. Both transitions reach their target values within $1.6\,\mu\text{s}$, as defined by 10 %–90 % thresholds. For a 48 V input and $N = 6$, each inductor is subjected to a nominal driving voltage of either $8\,\text{V} - V_{OUT}$ or $-V_{OUT}$. Subsequently, using $v/L = di/dt$, an upward and downward slew rate of $\geq 60\,\text{A}/\mu\text{s}$ and $\geq 13\,\text{A}/\mu\text{s}$, respectively, are expected. In practice, the results illustrated in Fig. 16 and Fig. 17 depict a modest upwards and downwards slew of $\geq 52.6\,\text{A}/\mu\text{s}$ and $\geq 8.4\,\text{A}/\mu\text{s}$, respectively, due in part to both voltage ripple on v_{SW}, inductor non-linearity, and added inductance with the introduction of large measurement loops to facilitate current probes. Figure 18 depicts measured waveforms resulting from

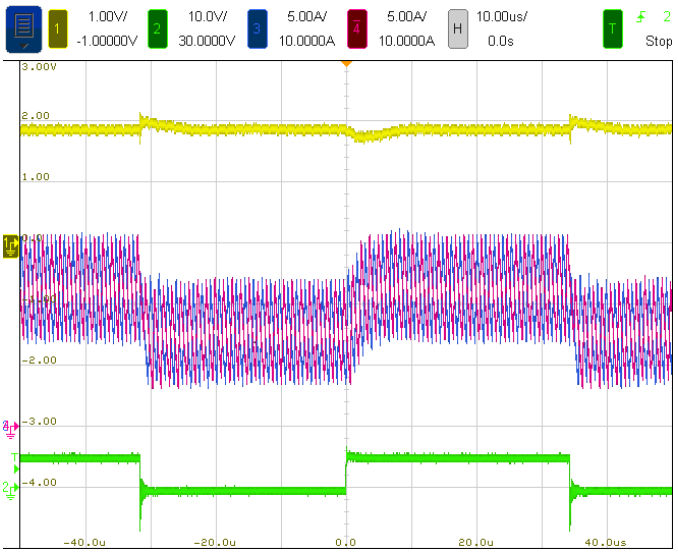

Figure 18. Measured current waveforms, $i_{L,1}(t)$ (blue), $i_{L,2}(t)$ (red), and output voltage, $V_{OUT}(t)$ (yellow), in response to a 15 A $\leftrightarrow$ 22 A load step in I_{OUT}, control signal (green), while maintaining $V_{OUT} = 1.8$ V. $V_{IN} = 48$ V, $N = 6$, $f_{SW} = 750$ kHz, $C_0 = 496$ nF, $L_1 = L_2 = 150$ nH.

a periodic load step in I_{OUT} between 15 A and 22 A. A pre-programmed control response to known disturbances was calibrated and used in Figures 16 - 18 to demonstrate the stability and controllability of the constructed prototype. Such an approach may be implemented using look-up tables, with similar methods finding use in systems employing dynamic-voltage-scaling (DVS) (e.g. [52]). Alternatively, non-linear feedback control building on the large-signal analysis presented in Section IV may be implemented, but is beyond the scope of this work. We note that classical control using small-signal approximations and local linearization does not capture the large-signal effects modelled in Section IV, and subsequently may not ensure complete soft-charging of the flying capacitors under large ripple conditions. Further improvement to transient response in a future prototype may be achieved through the use of coupled magnetics [53], as indicated by the inherent 180° phase shift between inductor current waveforms.

Table III compares this prototype with recent state of the art, demonstrating extremely high measured power densities with this design. This is despite the use of low density Class I dielectrics, which are being effectively operated with large ripple for very high energy density utilization. We note that for this first prototype, switches S_{L2-7} and S_{R2-7} were chosen for ease of implementation given their identical footprint to S_{L1} and S_{R1}, but are significantly oversized. As such, a future iteration may expect a reduction in associated switching losses and provide more competitive efficiencies. Furthermore, while the presented full ripple analysis served to accurately assist with the determination of allowable operating range and clocking requirements, closed-loop adjustments to split-phase timings in response to changes in load was not performed. Moreover, the 150 nH composite core inductors used in this high density revision exhibit soft-saturation with increasing load. As of yet, closed-loop split-phase control that can compensate for both changes in load and passive derating has not yet been demonstrated, but is a subject of active research.

VI. Conclusion

This paper demonstrates a new symmetric dual inductor hybrid (SDIH) dickson-type topology that is well suited for large regulated conversion ratios, such as 48V-to-PoL applications. Due to the symmetry of the proposed topology, the high-side input sees interleaved current draw for reduced filtering requirements and charge flow is equally distributed through all mirrored components for simplified component selection and thermal management. In addition, all flying capacitors are fully soft-charged, circumventing the slow-switching-limit and allowing for increased voltage ripple and subsequent improved energy density utilization. Furthermore, this article presents analysis that yields accurate phase timing control by accounting for large-signal ripple on both flying capacitors and inductors simultaneously. While split-phase control is required, its complexity is minimal and a fixed cost that does not scale with capacitor network order (odd and even inclusive), provided that all flying capacitors are sized equally.

Finally, a 48 V-to-PoL discrete hardware prototype confirms expected operation of the proposed SDIH topology and validates the presented analysis. This prototype demonstrates very high power densities of 1,029 W/in^3, 754 W/in^3, and 663 W/in^3 for regulated output voltages of 3 V, 2 V, and 1 V respectively, despite using calculated split-phase timings without active feedback.

References

[1] N. M. Ellis and R. C. Pilawa-Podgurski, "A Symmetric Dual-Inductor Hybrid Dickson Converter for Direct 48V-to-PoL Conversion," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1267–1271, IEEE, 2022.

[2] R. Miftakhutdinov, "Improving system efficiency with a new intermediate-bus architecture," in *Texas Instruments Inc. Seminar*, vol. 2, Citeseer, 2009.

[3] S. Oliver and V. C. P. Line, "From 48 v direct to intel vr12. 0: Saving 'big data' $500,000 per data center, per year," *Vicor White Paper (Online)*, 2012.

[4] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48-v voltage regulator module with pcb winding matrix transformer for future data centers," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9302–9310, 2017.

[5] Z. Ye, Y. Lei, and R. C. Pilawa-Podgurski, "The Cascaded Resonant Converter: A Hybrid Switched-Capacitor Topology with High Power Density and Efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946–4958, 2019.

[6] T. Ge, Z. Ye, and R. C. Pilawa-Podgurski, "A 48-to-12 v cascaded multi-resonant switched capacitor converter with 4700 w/in 3 power density and 98.9% efficiency," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1959–1965, IEEE, 2021.

[7] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770–782, 2015.

[8] T. Instruments, "Lmg5200: 48 to 1 v or 40 a single-stage converter reference design," *PMP4497 Reference Design*, 2016.

[9] X. Lou and Q. Li, "300a single-stage 48v voltage regulator with multiphase current doubler rectifier and integrated transformer," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1004–1010, IEEE, 2022.

[10] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-stage high-efficiency 48/1 v sigma converter with integrated magnetics," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 192–202, 2019.

Table III
COMPARISON WITH PRIOR WORK

	APEC 2017 [54]	TIA 2019 [13]	COMPEL 2019 [14]	COMPEL 2020 [15]	ECCE 2021 [16]	**This work**
Conversion Ratio:	48V to 1V	48V to 1V-2V	54V to 1.5V	48V to 1V-2.5V	48V to 1V-3V	**48V to 1V-3V**
Topology:	Sigma (DCX + Buck)	DIH	LEGO-PoL	MLB-PoL	DIH	**SDIH**
Switch Type:	GaN FET	GaN FET & Diode	MOSFET	MOSFET	MOSFET	**MOSFET**
f_{SW} :	600 kHz	300 kHz	500 kHz	250 kHz	750 kHz	**750 kHz**
Inductor:	36 μH & 190 nH	2 × 1.5 μH	12 × 1 μH	2 × 600 nH	2 × 1 μH	**2 × 150 nH**
Peak Efficiency: (excl. Gating Loss)	93.5% @1V	95.02% @2V 93% @1V	93.1% @1.5V	95.6% @2.5V 95.1% @2V 93.1% @1V	93.8% @3V 92.2% @2V 87.5% @1V	**91.4% @3V** **89.4% @2V** **83.5% @1V**
$P_{OUT\text{-}MAX}$:	80 A @1V	10 A @2V 10 A @1V	300 A @1.5V	65 A @2.5V 65 A @2V 65 A @1V	50 A @3V 60 A @2V 70 A @1V	**60 A @3V** **66 A @2V** **116 A @1V**
Efficiency @ $P_{OUT\text{-}MAX}$: (excl. Gating Loss)	92% @1V	94.5% @2V 92.3% @1V	78% @1.5V	92.1% @2.5V 91.3% @2V 86.8% @1V	91.1% @3V 88.1% @2V 80% @1V	**90.0% @3V** **86.8% @2V** **73.8% @1V**
Component volume[(a)]:	-	1.436 cm^3	5.859 cm^3	1.842 cm^3	2.756 cm^3	**1.197 cm^3**
Power Density[(a)]: (W/$inch^3$)	-	228 @2V 114 @1V	1,259 @1.5V	1,445 @2.5V 1,156 @2V 578 @1V	892 @3V 715 @2V 422 @1V	**2,464 @3V** **1,807 @2V** **1,588 @1V**
Power Density[(b)]: (W/$inch^3$)	420 @1V	-	152 @1.5V	494 @2.5V 395 @2V 198 @1V	524 @3V 419 @2V 246 @1V	**1,029 @3V** **754 @2V** **663 @1V**

[(a)]Considering power stage components only (flying capacitors, inductors, switches, and diodes).
[(b)]Best-fit cuboid encompassing entire converter solution.

[11] C. Li, Y. E. Bouvier, A. Berrios, P. Alou, J. A. Oliver, and J. A. Cobos, "Revisiting "partial power architectures" from the "differential power" perspective," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–8, IEEE, 2019.

[12] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer," in *2008 IEEE Power Electronics Specialists Conference*, pp. 4008–4015, IEEE, 2008.

[13] G.-S. Seo, R. Das, and H.-P. Le, "Dual Inductor Hybrid Converter for Point-of-Load Voltage Regulator Modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 367–377, 2019.

[14] J. Baek, P. Wang, S. Jiang, and M. Chen, "LEGO-POL: A 93.1% 54V-1.5V 300A Merged-Two-Stage Hybrid Converter with a Linear Extendable Group Operated Point-of-Load (LEGO-POL) Architecture," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–8, IEEE, 2019.

[15] Z. Ye, R. A. Abramson, Y.-L. Syu, and R. C. Pilawa-Podgurski, "MLB-PoL: A High Performance Hybrid Converter for Direct 48 V to Point-of-Load Applications," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–8, IEEE, 2020.

[16] N. M. Ellis and R. C. Pilawa-Podgurski, "Modified Split-Phase Switching with Improved FlyCapacitor Utilization in a 48V-to-POL Dual InductorHybrid-Dickson Converter," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, p. *in press*, IEEE, 2021.

[17] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[18] J. Zou, N. Brooks, S. Coday, N. M. Ellis, and R. C. N. Pilawa-Podguski, "On the Size and Weight of Passive Components: Scaling Trends for High-Density Power Converter Designs," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–7, IEEE, 2022.

[19] N. M. Ellis and R. Amirtharajah, "A Resonant Dual Extended LC-tank Dickson Converter with 50% Two-Phase Operation at Odd Conversion Ratios," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1282–1287, IEEE, 2021.

[20] Z. Ye, S. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and Comparison of Passive Component Volume of Hybrid Resonant Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, 2022.

[21] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched Tank Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5048–5062, 2018.

[22] Z. Ye, Y. Lei, and R. C. Pilawa-Podgurski, "A 48-to-12 V Cascaded Resonant Switched-Capacitor Converter for Data Centers with 99% Peak Efficiency and 2500 W/in 3 Power Density," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 13–18, IEEE, 2019.

[23] T. Urkin, G. Sovik, E. E. Masandilov, and M. M. Peretz, "Digital zero-current switching lock-in controller ic for optimized operation of resonant scc," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5985–5996, 2020.

[24] K. Kesarwani and J. T. Stauth, "The Direct-Conversion Resonant Switched Capacitor Architecture with Merged Multiphase Interleaving: Cost and Performance Comparison," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 952–959, IEEE, 2015.

[25] Z. Ye, Y. Lei, and R. C. Pilawa-Podgurski, "A Resonant Switched Capacitor Based 4-to-1 Bus Converter achieving 2180 W/in^3 Power Density and 98.9 % Peak Efficiency," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 121–126, IEEE, 2018.

[26] P.-L. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving vrms with coupling inductors," *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 499–507, 2001.

[27] J. Li, C. R. Sullivan, and A. Schultz, "Coupled-inductor design optimization for fast-response low-voltage dc-dc converters," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No. 02CH37335)*, vol. 2, pp. 817–823, IEEE, 2002.

[28] Y. Xie and P. Brohlin, "Optimizing gan performance with an integrated driver," *Texas Instruments White Paper*, p. SLYY085, 2016.

[29] X. Yang, H. Cao, C. Xue, L. He, Z. Tan, M. Zhao, Y. Ding, W. Li, and W. Qu, "33.4 an 8a 998a/inch3 90.2% peak efficiency 48v-to-1v dc-dc converter adopting on-chip switch and gan hybrid power conversion," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, pp. 466–468, IEEE, 2021.

[30] X. Yang, L. Zhao, M. Zhao, Z. Tan, L. He, Y. Ding, W. Li, and W. Qu, "A 5v input 98.4% peak efficiency reconfigurable capacitive-sigma converter with greater than 90% peak efficiency for the entire 0.4˜ 1.2 v output range," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, pp. 108–110, IEEE, 2022.

[31] Texas Instruments, *Small, 10-MHz, 8-V to 14-V, 10-A synchronous SWIFT™ series capacitor buck converter*, (accessed September 5th, 2022). https://www.ti.com/product/TPS54A20?dcmp=dsproject&hqs=pf.

[32] Analog Devices, *Fixed Ratio High Power Inductorless (Charge Pump) DC/DC Controller*, (accessed September 5th, 2022). https://www.analog.com/en/products/ltc7820.html.

[33] J. A. Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 50–61, 2019.

[34] J. A. Anderson, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, and J. W. Kolar, "Three levels are not enough: Scaling laws for multilevel converters in ac/dc applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3967–3986, 2020.

[35] K. Abe, K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "A novel three-phase buck converter with bootstrap driver circuit," in *2007 IEEE Power Electronics Specialists Conference*, pp. 1864–1871, IEEE, 2007.

[36] K. Matsumoto, K. Nishijima, T. Sato, and T. Nabeshima, "A Two-Phase High Step Down Coupled-Inductor Converter for Next Generation Low Voltage CPU," in *8th International Conference on Power Electronics-ECCE Asia*, pp. 2813–2818, IEEE, 2011.

[37] P. S. Shenoy, M. Amaro, J. Morroni, and D. Freeman, "Comparison of a Buck Converter and a Series Capacitor Buck Converter for High-Frequency, High-Conversion-Ratio Voltage Regulators," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7006–7015, 2015.

[38] R. Das and H.-P. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1997–2001, IEEE, 2019.

[39] Y. Lei and R. C. N. Pilawa-Podgurski, "A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, 2014.

[40] O. Kirshenboim and M. M. Peretz, "High-efficiency nonisolated converter with very high step-down conversion ratio," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3683–3690, 2016.

[41] M. Halamicek, T. McRae, and A. Prodić, "Cross-coupled series-capacitor quadruple step-down buck converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1–6, IEEE, 2020.

[42] P. S. Shenoy, O. Lazaro, M. Amaro, R. Ramani, W. Wiktor, B. Lynch, and J. Khayat, "Automatic current sharing mechanism in the series capacitor buck converter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2003–2009, IEEE, 2015.

[43] J. Xu, L. Gu, and J. Rivas-Davila, "Effect of Class 2 Ceramic Capacitor Variations on Switched Capacitor and Resonant Switched Capacitor Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[44] Y. Chen, P. Wang, H. Cheng, G. Szczeszynski, S. Allen, D. M. Giuliano, and M. Chen, "Virtual intermediate bus cpu voltage regulator," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6883–6898, 2021.

[45] Y. Zhu, T. Ge, Z. Ye, and R. C. Pilawa-Podgurski, "A dickson-squared hybrid switched-capacitor converter for direct 48 v to point-of-load conversion," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1272–1278, IEEE, 2022.

[46] C. R. Sullivan, B. A. Reese, A. L. Stein, and P. A. Kyaw, "On Size and Magnetics: Why Small Efficient Power Inductors Are Rare," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, pp. 1–23, IEEE, 2016.

[47] R. Das, G.-S. Seo, and H.-P. Le, "A 120 V - to - 1.8 V 91.5 %-Efficient 36-W Dual-Inductor Hybrid Converter with Natural Soft-charging Operations for Direct Extreme Conversion Ratios," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1266–1271, IEEE, 2018.

[48] N. M. Ellis and R. Amirtharajah, "Large signal analysis on variations of the hybridized dickson switched-capacitor converter," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 15005–15019, 2022.

[49] Z. Ye, Y. Lei, W.-C. Liu, P. S. Shenoy, and R. C. Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2019.

[50] N. M. Ellis, R. Iyer, and R. C. Pilawa-Podgurski, "A synchronous bootstrapping technique with increased on-time and improved efficiency for high-side gate-drive power delivery," in *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, pp. 462–466, IEEE, 2021.

[51] S. Coday and R. C. N. Pilawa-Podgurski, "High accuracy calorimetric measurements and modeling of ceramic capacitor losses under large ripple operation," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 188–194, IEEE, 2020.

[52] M. Barai, S. Sengupta, and J. Biswas, "Digital controller for dvs-enabled dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 557–573, 2009.

[53] C. R. Sullivan and M. Chen, "Coupled inductors for fast-response high-density power delivery: Discrete and integrated," in *2021 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–8, IEEE, 2021.

[54] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 48/1v sigma converter voltage regulator module," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2207–2212, IEEE, 2017.

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