UNIVERSITY OF CALIFORNIA SAN DIEGO

High-Power and Low-Noise Circuit Techniques for Wideband RF, Millimeter-Waves and Optical Wireline Systems in Advanced RFSOI Technologies

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Committee in charge:

Professor Gabriel Rebeiz, Chair
Professor Peter Asbeck
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Professor Drew Hall
Professor William Hodgkiss

2020

The dissertation of Omar El-Aassar is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

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DEDICATION

To my family

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Chapter 2, in full, is a reprint of the material as it appears in: O. El-Aassar and G. M.

Rebeiz, "A Compact pMOS Stacked-SOI Distributed Power Amplifier With Over 100-GHz Bandwidth and Up to 22-dBm Saturated Output Power," *IEEE Solid-State Circuits Letters*, vol. 2, no. 2, pp. 9–12, Feb 2019.

Chapter 3, in full, has been submitted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "A 120 GHz Bandwidth CMOS SOI Distributed Power Amplifier with Multi-Drive Intra-Stack Coupling," *IEEE Microwave and Wireless Components Letters*, submitted.

Chapter 4 is mostly a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "A DC-to-108-GHz CMOS SOI Distributed Power Amplifier and Modulator Driver Leveraging Multi-Drive Complementary Stacked Cells," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3437-3451, Dec 2019.

Chapter 4 is also, in part, a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "4.7 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P1dB, and Over 100Gb/s in 64-QAM and PAM-4 Modulation," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb 2019, pp. 86-88.

Chapter 5, in full, has been accepted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "Cascaded Multi-Drive Stacked-SOI Distributed Power Amplifier with 23.5 dBm Peak Output Power and over 4.5 THz GBW," *IEEE Transactions on Microwave Theory and Techniques*, accepted.

Chapter 6, in full, has been submitted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "Design of Low-Power Sub-2.4 dB Mean NF 5G LNAs Using Forward Body Bias in 22nm FDSOI," *IEEE Transactions on Microwave Theory and Techniques*, under revision.

Chapter 7, in full, is a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "A 350mV Complementary 4-5 GHz VCO based on a 4-Port Transformer Resonator

with 195.8dBc/Hz Peak FOM in 22nm FDSOI," *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, USA, 2019, pp. 159-162.

Chapter 8, in full, is a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "26.5 A 0.1-to-0.2V Transformer-Based Switched-Mode Folded DCO in 22nm FDSOI With Active Step-Down Impedance Achieving 197dBc/Hz Peak FoM and 40MHz/V Frequency Pushing," *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2019, pp. 416-418.

Chapter 9, in full, has been submitted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "A 5 GHz 0.5 V Hybrid Class-B/F_{-1} CMOS Oscillator with -147 dBc/Hz Phase Noise at 10 MHz Offset Using Body-Biased 22nm FDSOI," *IEEE Microwave and Wireless Components Letters*, submitted.

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The dissertation author was the primary investigator and author of the work in these chapters, and the co-author (Prof. Gabriel M. Rebeiz) has approved the use of the material for this dissertation.

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PUBLICATIONS

O. El-Aassar and G. M. Rebeiz, "A 16 Path All-Passive Harmonic Rejection Mixer with Watt-Level In-Band IIP3 in 45 nm CMOS SOI," *IEEE Microwave and Wireless Components Letters*, submitted.

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O. El-Aassar and G. M. Rebeiz, "A 350mV Complementary 4-5 GHz VCO based on a 4-Port Transformer Resonator with 195.8dBc/Hz Peak FOM in 22nm FDSOI," *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, USA, 2019, pp. 159-162.

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O. El-Aassar and G. M. Rebeiz, "4.7 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P1dB, and Over 100Gb/s in 64-QAM and PAM-4 Modulation," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb 2019, pp. 86-88.

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ABSTRACT OF THE DISSERTATION

High-Power and Low-Noise Circuit Techniques for Wideband RF, Millimeter-Waves and Optical Wireline Systems in Advanced RFSOI Technologies

by

Omar El-Aassar

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2020

Professor Gabriel Rebeiz, Chair

The inevitable migration to deeply-scaled technology nodes forces special considerations on high-power, low-noise, and high spectral purity integrated circuits. The dissertation addresses these considerations for a wide spectrum of RF, mm-waves, and optical-wireline circuits in advanced CMOS SOI technologies. The major contributions are in distributed power amplifiers (DPAs), optical drivers, RF and mm-wave voltage controlled oscillators (VCOs), mm-waves low-noise amplifiers (LNAs), and high linearity mixers.

The work in power amplifiers culminated in the design and measurement of several novel ultra-wide-band DPAs/drivers with 100+GHz of bandwidth (BW) in GlobalFoundries

45nm RFSOI technology. Several design techniques are introduced to break the gain-bandwidth (GBW), and power-BW trade-offs in conventional distributed designs. The first PMOS-only DPA with 100+GHz BW is demonstrated exploiting the decreasing gap between NMOS and PMOS performance in deeply-scaled technology nodes. Transistors stacking is exploited for high power while introducing two new stack compensation techniques, the multi-drive intra-stack and inter-stack coupling. Improved stability coupling networks and magnetic field confining transmission lines are also devised to allow high gain stable operation. Over 4.5 THz GBW is recorded from a cascaded DPA and over 100 Gb/s is measured in both 64-QAM and PAM-4 modulations for a CMOS modulator driver.

The mm-wave 5G LNAs contributions focus on K/Ka bands designs for next generation phased-array systems and exploits the body-bias of fully depleted SOI devices to control the linearity and gain of LNAs in 22nm FDSOI technology.

The efforts in RF and mm-waves LC VCOs focus on implementations in deeply scaled 22nm FDSOI technology node. New circuit techniques are proposed to allow ultra-low-voltage operation (sub 0.1 V), low flicker noise variability across the tuning range without a dedicated tuning for the common-mode, ultra-low phase noise while using thin-oxide only devices, and over 70% of tuning range spanning the X and Ku-bands.

The work in high linearity mixers exploits the enhancement of the figure of merit of CMOS switches in new technology nodes, to implement all-passive 16-path harmonic-reject mixers with watt-level IIP_3 and over 35 dBc harmonic rejection ratio for all harmonics up-to 3 GHz.

Chapter 1

Introduction

1.1 Technology Scaling Challenges and Opportunities

The continuous scaling of the channel length (L_g) in CMOS technology nodes has lead to considerable improvement in the intrinsic devices performance. The technology scaling allows for higher field-effect transistor (FET) speed and lower operational voltage by increasing the cut-off frequencies (f_T and f_{max}), while reducing the threshold voltage (V_T), which effectively reduces the power consumption. Advancements in CMOS processes solved a lot of problems associated with short channel effects in bulk CMOS, thereby, allowing deep scaling sub-28nm nodes. Also, high-K metal gates (HKMG) reduced gate leakage. Strain engineering improved channel mobility for both NMOS and PMOS. SiGe channels allowed further mobility improvement for PMOS devices towards a more balanced complementary operation. Silicon over insulator (SOI) reduced the depletion capacitance, improved f_T, reduced the drain induced barrier lowering (DIBL) and the risks of bulk punch through associated with short channel bulk CMOS. While FinFETs increased the intrinsic gain of the devices.

While the technology scaling offers substantial speed improvement, power and area reduction for the back-end, a lot of concerns should be addressed when accompanied with high

performance front-end systems. The low supply of operation coincides with a low breakdown voltage for the devices which limit their linearity and reliable output power levels. The reduction of the allowed voltage swing also limits the minimum achieved phase noise by the local oscillator (LO) circuitry, while the shrinking of the device channel increases the flicker noise corner frequency. On the other hand, the quality factor of the on-chip passives degrades in deeply-scaled technology nodes due to the thinner back-end-of-line metalization (BEOL) layers, the reduced height of the ground plane, and the mandatory high density metal filling for mechanical stability. The reduced quality factor for passive components directly affects the system performance, and in particular, the transmitter efficiency, receiver noise (sensitivity) and oscillator phase noise.

Moreover, the technology scaling trends are accompanied with a continuous demand for higher data rates for both wireless and wireline communication systems. This growing demand pushes more communication standards to adopt spectrally efficient high-order modulation schemes with high peak-to-average-power-ratio (PAPR). The high PAPR tightens the error vector magnitude (EVM) requirements and therefore puts its additional burden on the linearity specs for power amplifiers and phase noise specs for the LO chain.

This thesis tries to address the high-linearity, high-power, low-noise, and high spectral purity signal generation challenges in deeply-scaled silicon over insulator (SOI) technology nodes. In order to address these challenges, several circuit techniques are proposed for distributed power amplifiers [1–5], low noise amplifiers [6], oscillators [7–11] and mixers [12], and applied using thin-oxide devices with rated supply voltages of 1.2 V (45 nm RFSOI) and 0.8 V (22 nm FDSOI).

1.2 Thesis Overview

This thesis presents fully integrated high-power and low-noise circuit techniques for wideband communication systems in advanced RFSOI technologies.

Chapter 2 presents an all-PMOS stacked-SOI distributed power amplifier (DPA) as an

alternative to conventional NMOS for higher reliable operating voltages. PMOS devices are proposed for the stacked DPA design for their higher reliability and comparable RF performance to NMOS in deeply-scaled technology nodes. The PMOS-DPA uses 8-shaped input and output transmission lines (TLs) for magnetic field confinement and compact chip area. The amplifier operates from 1.5 GHz to greater than 100 GHz using an on-chip 2-section DC-feed, diminishing the need for a bulky external bias-tee. A prototype 8-stage, 16-dB gain, 101 GHz small-signal 3dB-bandwidth all-PMOS DPA is implemented in 45nm CMOS SOI with a core area of 0.33 mm^2. The PMOS design demonstrates an output P_{1dB} and P_{SAT} higher than 17 and 19 dBm, respectively, and a state-of-the-art PAE higher than 10%, up to 60 GHz, with a 60 GHz P_{SAT} 3dB-bandwidth. At 28 GHz, the DPA achieves 30 Gb/s 64-QAM and 8 Gb/s 256-QAM with average P_{out} of 14.5 dBm, and 10.2 dBm, respectively. To the authors' knowledge, this is the first implementation of a silicon DA with over 100 GHz bandwidth made exclusively with PMOS. The PA reports the highest 256-QAM data rate (8 Gb/s) for a 10 dBm output power. The PMOS amplifier also has the smallest reported chip area including the DC-feed for DPAs achieving 500+ GHz GBW.

Chapter 3 presents a DPA topology that improves both the power combining efficiency and the operation bandwidth. Multi-drive intra-stack coupling is introduced in the design of the gain cells to break the trade-off between high output power (P_{OUT}) requirement and the achieved bandwidth. The proposed technique also compensates for the input TL loss to accommodate more stages and achieve flat gain and higher P_{OUT}. A prototype 8-stage, 16-dB gain, 120 GHz bandwidth DPA is fabricated in 45nm CMOS SOI using elevated coplanar waveguide (CPW) TLs with a core area of 0.51 mm^2. The amplifier maintains an output P_{1dB} and P_{SAT} higher than 18 and 20 dBm, respectively, up-to-60 GHz and achieves a peak PAE of 19.7% at 15 GHz. A 64-QAM modulated signal with data rate 30 Gb/s (5 GBaud/s) is demonstrated at 55 GHz with a 13.5 dBm average P_{OUT} and 6.9% PAE while the error vector magnitude (EVM) is kept below 5%. To the authors' knowledge, the achieved 757 gain-bandwidth product (GBW) is the highest

among reported non-cascaded DAs.

Chapter 4 proposes a complementary distributed power amplifier using stacked gain cells with multiple input driving signals. The stack multi-drive compensates for the increasing input TL and stack losses as frequency increases and results in bandwidth (BW) extension with flat gain response. The technique simultaneously increases the GBW and the output power at high frequencies while maintaining a smaller chip area compared to the conventional DPA design and the intra-stack coupling technique presented in chapter 3. A broadband active splitter is introduced before the output stage to create two complementary distributed paths which are exploited for AM-AM and AM-PM non-linearity compensation. The CMOS DPA is implemented in 45nm RFSOI with a core area of 0.31 mm^2. The amplifier has a 23 dB gain and 108 GHz 3-dB BW from true DC frequency with no need for external bias-tees. The DPA maintains a P_{1dB} and P_{SAT} over 16.9 dBm and 18.4 dBm, respectively, from DC-to-70 GHz, with a 70 GHz P_{SAT} 3-dB BW. When operated with modulated signals, the DPA provides over 100 Gb/s in both 64-QAM and PAM-4 modulations. To the authors knowledge, the CMOS DPA reports the highest published GBW to date (1.525 THz), the highest data-rate in 64-QAM for carriers up-to 59 GHz, and the highest single-ended output swing in PAM-4 modulation.

Chapter 5 presents a cascaded distributed power amplifier topology with greater than 4.5 THz GBW. The DPA uses stacking with multi-drive inter-stack coupling to compensate for the stacked gain cells and input TL losses. The techniques improve the gain and output power without compromising the BW. The addition of resistive degeneration is proposed, for the multi-drive coupling transformer secondary windings, in order to improve the stability and attain $>$ 30 dB gain. The cascaded DPA employs 8-shaped TLs to allow inter-stack coupling in a compact area and for field confinement. A 33 dB gain, 101.5 GHz bandwidth DPA is realized in the 45nm RFSOI GlobalFoundries process. The amplifier maintains a P_{1dB} and $P_{SAT} > 18.7$ and 21 dBm, respectively, up-to-60 GHz, while demonstrating $>$ 14 dBm of average P_{OUT} for a 30 Gb/s 64-QAM modulated signal, with an EVM $< 5\%$. The DPA is also able to provide a

72 Gb/s 64-QAM signal with 13.6 dBm average P_{OUT} from a 13 GHz carrier. To the authors knowledge, the cascaded multi-drive DPA achieves the highest reported GBW, continuous-wave P_{SAT}, and average P_{OUT} for 64-QAM 30 Gb/s modulated signal, in a compact core area compared to published silicon-based DPAs with comparable power levels.

Chapter 6 presents K/Ka-band low-noise-amplifiers (LNAs) for 5G front-ends. The use of forward body bias (FBB) in fully-depleted silicon-on-insulator (FDSOI) devices is studied and utilized to improve the LNA performance under reduced supply voltage and dc power (P_{DC}). Design procedures targeting high linearity, low noise, and high gain are provided. The 2-stage CS-LNA achieves sub-2.1 dB mean-NF, 20.1 dB peak-Gain, 9 GHz 3dB-bandwidth (BW) from 19.5-to-28.5 GHz, and an in-band IIP_3 of 0 dBm with 9.6 mW P_{DC}. The single-stage CAS-LNA achieves over 10 dB gain, 11 GHz 3dB-BW, and an IIP_3 of 7.5 dBm for a 2.2 dB mean-NF. The 2-stage CAS-LNA has 28.5 dB peak-gain, 4 GHz BW and 2.25 dB mean-NF for 20 mW P_{DC}. In the low power mode, the CS-LNA operates at 0.4 V with P_{DC} of 3.2 mW, 16.9 dB gain and less than 2.2 dB mean-NF, while the 2-stage CAS-LNA achieves 2.4 dB NF and 23 dB gain for 5.5 mW. Also, ultra-low-power operation and sub-3 dB NF is possible with the CS-LNA at 0.2 V/1 mW with 12 dB gain, and for the CAS-LNA at 0.4 V/2.4 mW with 17.7 dB gain. To the authors knowledge, the single stage CAS-LNA shows the highest IIP_3 at 28 GHz compared to published CMOS work. The 2-stage FBB CS and CAS designs have the lowest voltage supply, P_{DC}, and best FoM for mm-waves 5G LNAs in the low power mode.

Chapter 7 presents an ultra-low voltage and power complementary VCO topology based on a 4-port transformer resonator. The design benefits from the high current efficiency of a CMOS topology and the low phase noise (PN) and supply voltage of the NMOS/PMOS-only structure without sacrificing reliability. A 4-port transformer resonator is used to provide two differential-mode (DM) and two common-mode (CM) harmonic impedances for lower phase noise, voltage supply, and sensitivity to CM tuning. The CMOS VCO is implemented in 22nm FDSOI with a core area of 0.19 mm^2. The VCO dissipates < 0.45mW from 350mV supply while

achieving a peak figure-of-merit (FOM) of 192-195.8 dBc/Hz across the 20% continuous tuning range of 4.06-to-4.96 GHz. To the authors knowledge, the 4-port resonator-based CMOS VCO has the highest reported FOM for oscillators with sub-0.5 mW power consumption and the lowest supply voltage (350 mV) for complementary designs.

Chapter 8 proposes an LC DCO based on a folded, transformer-based, circuit topology to improve phase noise performance at low supply voltages. This topology divides the main-tank impedance between two stacked devices for lower phase noise for a given supply voltage without sacrificing loop gain, thus being important in ultra-low-voltage applications. Implemented in 22nm FDSOI, the circuit oscillates from 4.2 to 5 GHz with a record peak FOM of 197 dBc/Hz, -142.1 dBc/Hz PN at 10 MHz offset, 40 MHz/V pushing from a 0.15 V supply. The oscillator can operate down to 0.1 V supply.

Chapter 9 presents a self-biased 5 GHz hybrid class-B/F_{-1} oscillator for low phase noise and robust start-up. The design exploits the concurrent conduction of nMOS and pMOS, when placed on differential sides, to form a differential-mode (DM) high quality factor second harmonic resonator for low phase noise. Moreover, the same DM second harmonic resonator is shared between both cores to allow phase noise reduction for the main core (class-F_{-1}), and the start-up core (class-B). The hybrid oscillator is fabricated in 22nm FDSOI technology with a core area of 0.22 mm^2. The CMOS design uses thin-oxide only devices, operated from 0.5 V supply, and achieves a phase noise $<$ -147 dBc/Hz at 10 MHz offset across an 11% tuning range. The peak figure-of-merit (FoM) is 190 dBc/Hz, the supply frequency pushing ranges from 20-44 MHz/V, while the power consumption is from 15-to-18 mW. To the authors knowledge, the hybrid class-B/F_{-1} oscillator delivers the lowest phase noise by a 0.5 V oscillator at 5 GHz.

Chapter 10 proposes a 5 GHz stacked-complementary oscillator (SCO) that uses high quality factor Q single-turn nested differential inductors to achieve very low tank fundamental impedance R_{Tank} and even-harmonic shaping. The complementary nature of nMOS and pMOS is exploited to achieve 2^{nd} and 4^{th} harmonic common-mode resonances using differential-only

inductors with higher Q compared to the conventional single-ended tail filter. The complementary-stacked topology ensures the voltage between any two device terminals remains within reliable limits, while the body-bias is used to set the oscillator class with much lower noise sensitivity compared to the standard gate biasing. The SCO achieves $<$ -150 dBc/Hz phase noise (PN) at 10 MHz offset across the tuning range from 4.75-to-5.4 GHz and a supply frequency pushing better than 20 MHz/V, while using thin-oxide devices operated from 0.6 V in a 22 nm technology node. To the authors knowledge, the SCO reports the lowest phase noise achieved by a thin-oxide RF oscillator while keeping a figure-of-merit (FoM) of 191-193 dBc/Hz at 10 MHz offset.

Chapter 11 presents a low phase noise wide tuning range dual-core transformer-based VCO using a switch-less tertiary magnetic coupling loop. The design employs the benefits of transformer-switching without incurring switch loss and quality factor degradation, and also the benefits of mode-switching without the parasitics from the mode-selection network. The VCO uses dual-mode operation with a constant quality factor capacitors bank and a positive feedback DC-coupled inductive-degenerated output buffer to maximize the tuning range. The VCO, implemented in 22nm FDSOI, achieves a 72% tuning at 8-17 GHz and a figure-of-merit-tuning (FoM_T) of 208.8 dBc/Hz at 11 GHz. The chip operates from an 0.45 V supply with a power consumption of 17-33 mW and a core area of 0.39 mm^2. To the authors knowledge, the VCO achieves the highest FoM_T and lowest supply for designs over 10 GHz.

Chapter 12 presents an all-passive harmonic rejection mixer (HRM) with watt-level in-band IIP$_3$. The HRM operates in the voltage mode by using resistors to scale the voltages of the different paths across the frequency cycle and therefore attains very high linearity. The passive HRM employs a non-overlapping clock generation chain combined with duty cycle control circuit to trim the rise and fall times of individual paths and maintain the harmonic rejection ratio (HRR) over the RF frequency band. A prototype 0.13-3 GHz 16-path HRM is fabricated in 45 nm CMOS SOI technology using thick-oxide devices with 80 MHz IF bandwidth and a core area 0.06 mm^2. The HRM achieves a HRR $>$ 35 dBc for all harmonics up-to 3 GHz with a conversion loss of

8-10 dB, while the in-band IIP_3 is 24-31 dBm and IP_{1dB} is 11-13 dBm for an RF of 0.5-3 GHz. To the authors knowledge, the all-passive HRM achieves the highest reported in-band IIP_3 and IP_{1dB}.

The thesis concludes with chapter 13 which discusses future work opportunities based on the proposed techniques through out the thesis. Some prototypes for the future opportunities already passed the design and implementation phases and the fabricated new chips are presented and briefly discussed.

Chapter 2

A Compact PMOS Stacked-SOI Distributed Power Amplifier with over 100 GHz Bandwidth and up to 22 dBm Saturated Output Power

2.1 Introduction

The ever-increasing need for higher data rates in wired/wireless applications created a new interest in distributed power amplifiers (DPAs). While a number of DAs with over 100 GHz bandwidth were reported in SiGe HBT technologies [13–16], this is not common in CMOS which is favored for monolithic integration and lower manufacturing cost. The speed improvement from scaling of CMOS technologies favors ultra-wideband amplification. However, the lower breakdown and relatively high knee voltages render the design of efficient CMOS DPAs a challenging task.

The design of DAs involves a compromise between higher required output power and

gain on one side, and achieved bandwidth and chip area on the other side. Most of the reported silicon-based DAs fall into one of two categories: (a) a bandwidth over 100 GHz at the expense of power performance [13–15], or (b) an output power $>$ 15 dBm with smaller bandwidth [16, 17].

In this letter, we propose an all-PMOS stacked-DPA as an alternative to NMOS for higher reliable voltage of operation [18]. The amplifier is realized in 45nm SOI and uses multiple design approaches to break the power-bandwidth trade-off in a compact chip area (0.33 mm^2). The DPA achieves over 100 GHz bandwidth without needing an external bias-tee and demonstrates state-of-the-art continuous-wave (CW) and modulated signals performance.

2.2 PMOS PA Cells

PMOS is chosen for its higher reported breakdown voltage compared to NMOS in deeply scaled technologies. This is attributed to the lower rate of impact ionization for holes compared to electrons and the less abrupt junctions [19]. In addition, the analog and RF performance of the strain-engineered PMOS is becoming comparable to NMOS. This is also partly due to the fact that FET speeds are becoming dominated by the extrinsic routing parasitics rather than the intrinsic device performance at millimeter-waves.

A comparison is done between the simulated performance of a stacked PMOS and NMOS PA in 45nm SOI, in order to choose the DPA unit-cell (Fig. 2.1). Each test-cell comprises a 4-stack PA with 40 μm device widths and 20 pH series intra-stack peaking inductors for high frequency compensation. The PA cells are simulated with $|5|$ V supply divided equally between the 4 devices. For a fair comparison, the layout, decoupling and ground network is kept exactly the same for both designs, in order to have nearly equal TLs cut-off frequencies when used in a DPA structure, with the PMOS PA operated with a negative supply and bias voltages. The 4-stack PMOS PA has nearly the same simulated maximum-available-gain (MAG) as the NMOS PA with a reduction in the effective transconductance (Gm) of $< 15\%$ and an increase in the intrinsic

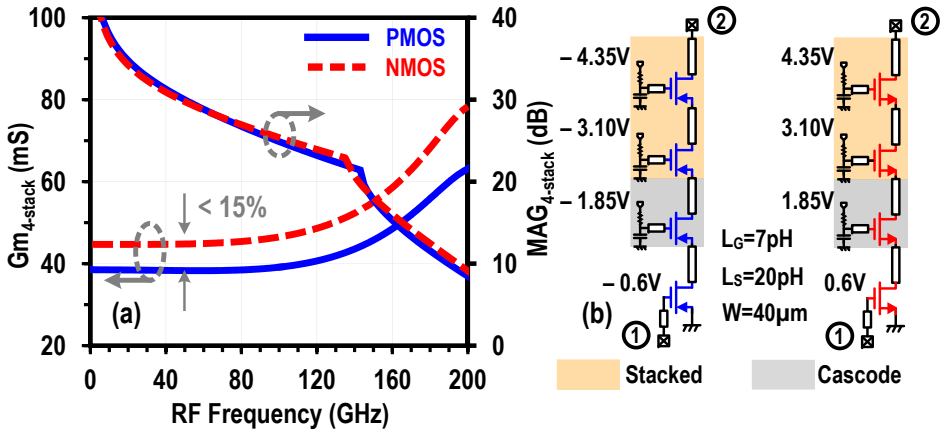

Figure 2.1: Simulated performance of a 4-stack PMOS versus NMOS PA cells in 45nm CMOS SOI: (a) simulated Gm and maximum available gain (MAG) for 4-stack unit cells; (b) schematic of the 4-stack unit cells.

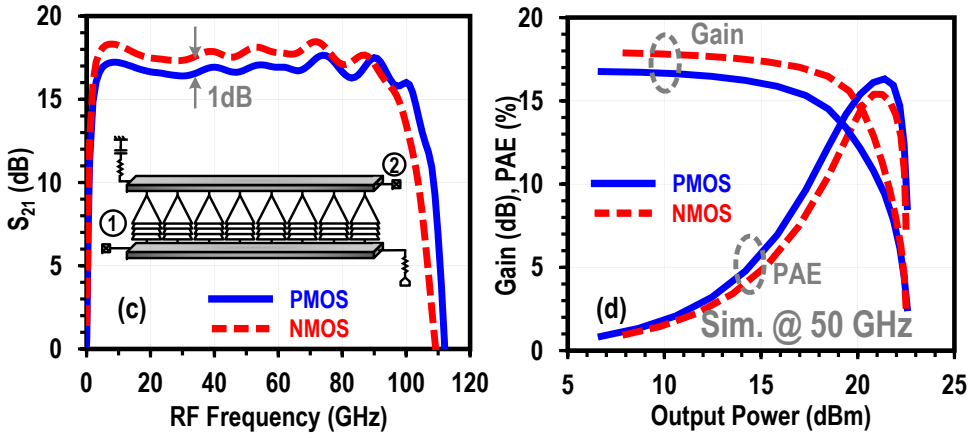

Figure 2.2: (a) Small signal gain of 8-stage DPAs using the presented 4-stack unit cells. (b) Power gain and PAE for the 8-stage DPAs versus output power at 50 GHz.

output impedance. Both PAs are then used as the unit cells of the 8-stage DPA, described in section III . The simulated performance in Fig. 2.2 shows that the PMOS DPA achieves slightly higher bandwidth with only 1-dB less power gain compared to the NMOS DPA. In addition, the PMOS design can deliver the same saturated output power and PAE as the NMOS design at 50 GHz. These results suggest PMOS devices are suitable for millimeter-waves PA design in deeply scaled technologies, particularly for stacked topologies where devices voltage stress consideration is essential.

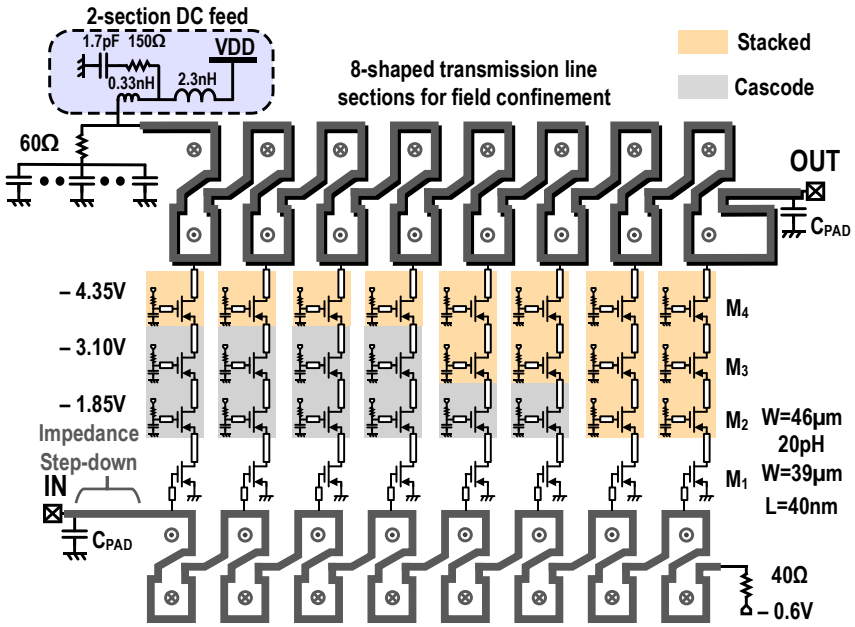

Figure 2.3: Schematic of the distributed PMOS SOI power amplifier with 8-shaped transmission line sections and 2-section DC-feed.

2.3 PMOS Distributed PA Design

The proposed 8-stage PMOS DPA is shown in Fig. 2.3. Each stage incorporates a 4-stack PMOS gain cell. The 4-stack topology allows P_{OUT} to increase by $4\times$ by quadrupling both the optimum output load line impedance and voltage swing (in ideal operation). The bandwidth, dictated by the cut-off frequency of the TLs, is preserved since only one fourth of the parasitic capacitance of the power amplifying devices needs to be absorbed by the input and output TLs. Note that the voltage swing is larger for the higher devices within the stack, while for a DPA, the signal swing builds up towards the output stages of the output TL. Consequently, only the upper devices / output stages need to allow a gate swing for the stacked devices, while the input stages can incorporate AC-grounded gates in a cascode configuration to improve the gain performance. In all stages, the gate scaling capacitors are designed to prohibit a maximum instantaneous voltage swing between any two device terminals $> |2.8|$V at P_{SAT}.

In addition to the 20 pH inductors (L_S) for intra-stack series peaking, a small routing

inductance ($L_G \approx 7$ pH) is placed on the gates of the stacked devices to peak Gm at high frequencies and compensate for the increasing TL loss so as to obtain a flat gain versus frequency. Furthermore, L_G of M_2 creates a negative impedance component at the drain node of M_1 which is translated through its gate-to-drain capacitance to provide a complementary compensation for the input TL loss at high frequencies when the TL loss is significant. Stability is ensured by limiting the L_G value such that the real impedance of the input TL remains always positive. The Gm peaking enables efficient staking of 4 FETs while the input TL loss compensation using L_G allows the number of stages to increase up to 8 for higher gain and P_{OUT}.

Both input and output TLs are shaped as 8-shaped inductor sections. This is particularly useful for magnetic field confinement and to increase the inductance per unit length while saving chip area [20]. The GSG pad parasitics (≈ 13 fF) are exploited to form small step-down impedance networks (between 40 and 50 Ω) at both ports for optimum matching and power delivery. A 2-section DC-feed is integrated on-chip to enable the operation from 1 to greater than 100 GHz without requiring bulky external bias-tees for additional area saving. An optional third DC-feed section can be placed off-chip to extend the lower frequency end for wireline applications.

2.4 Implementation

The PMOS-DPA is fabricated in GlobalFoundries 45nm SOI process with a core area of 0.48×0.68 mm^2 including the 2-section DC-feed (Fig. 2.4). Floating body partially-depleted PMOS with an effective channel length of 40nm are used for all the SOI devices. The stacked devices are slightly larger than the common source ones to help compensate for the delay difference between the loaded input and output TLs. The gates of the stacked devices are routed to the scaling capacitors via a 5 to 7 pH parasitic inductance (L_G). R-C low pass filters are placed between the biasing nodes of the stacked devices for consecutive stages to ensure stability. The output 8-shaped TL is implemented by tying the top two 1.2 μm thick copper metals together for

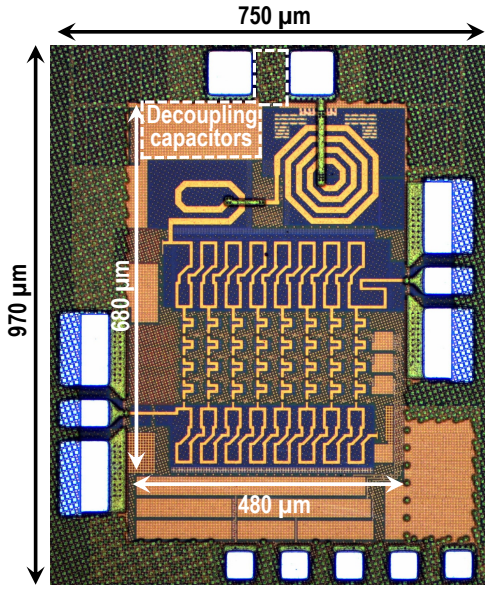

Figure 2.4: Die micrograph of the fabricated PMOS distributed power amplifier chip in 45nm CMOS SOI process.

higher current handling and to obtain a lower unloaded Z_0 compared to the input TL, implemented only on the top copper layer. This is important to achieve equal delay per stage for maximum power combining efficiency at high frequencies. Both TLs are fabricated over a trap-rich high resistivity substrate ($\rho \approx 2.5$ kΩ.cm) without using a ground-plane underneath for minimum loss and maximum unloaded Z_0. A properly damped multi-section DC-feed is mandatory to preserve gain flatness in the DA. The overall inductance of the DC-feed need to be large enough for low GHz operation while the effective second resonance need to be pushed far enough out of the amplifierâĂŹs operation band (>120 GHz). This is achieved by a 2-section DC-feed using a shunt 1.7 pF capacitor with a series 150 Ω resistor between a small 0.33 nH and a larger 2.3 nH inductors. The 0.33 nH inductor is designed as a 1.5-turn with large spacing between windings to maximize its parallel resonance and ensure a series resonance ≈180 GHz. The output termination is co-designed with the 2-section DC-feed to provide $\approx 40\ \Omega$ termination impedance from 1 to greater than 100 GHz.

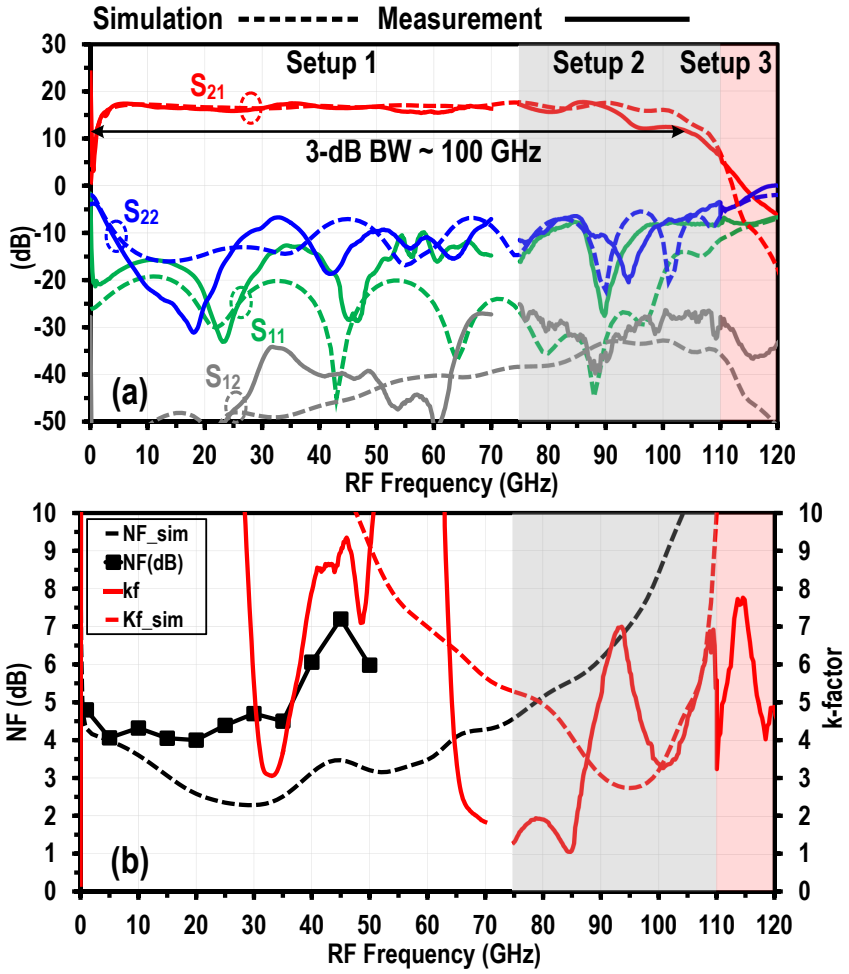

Figure 2.5: Small-signal performance versus frequency: (a) simulated and measured S-parameters; (b) noise figure and stability factor (k-factor).

2.5 Measurements

The PMOS-DPA is wafer-probed for small-signal performance from DC to 120 GHz using three setups. Frequencies less than 70 GHz are measured using a vector network analyzer (Keysight N5247A PNA-X) with 1.85 mm coaxial connectors. WR-10 probes are then used with frequency extenders modules and a millimeter-head controller to cover the range from 75 to 110 GHz, and WR-6 probes are used with another set of modules for frequencies higher than 110 GHz. The simulated and measured S-parameters of the PMOS-DPA are shown in Fig. 2.5(a).

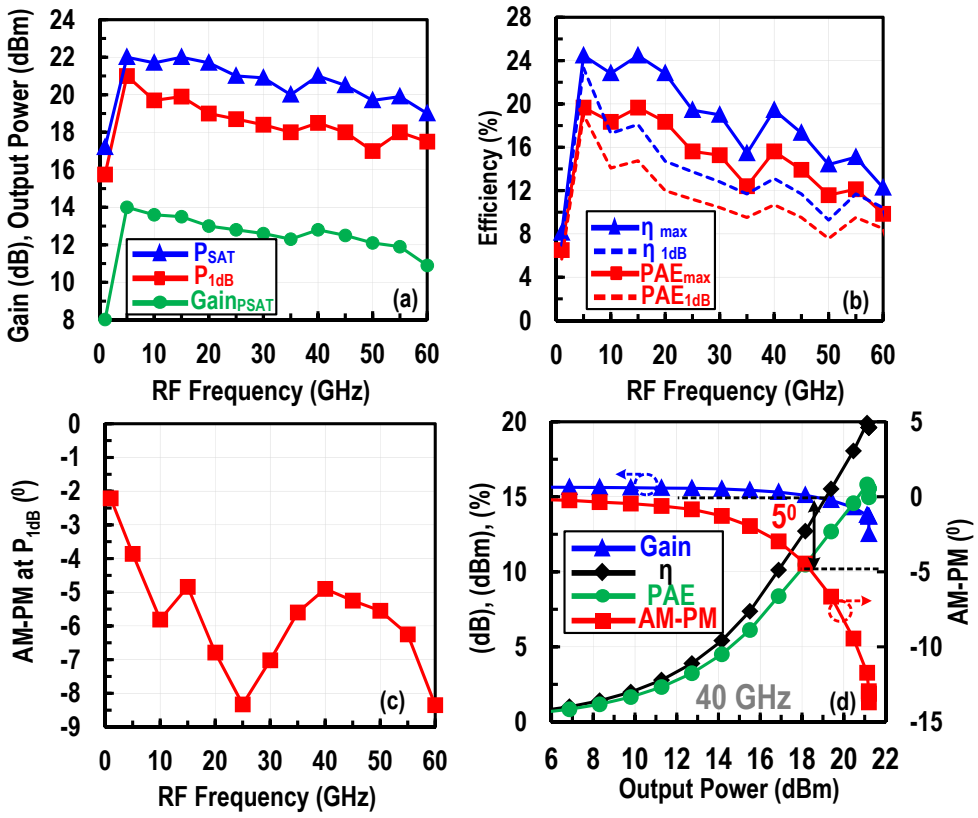

Figure 2.6: CW large-signal performance versus frequency: measured P_{1dB}, P_{SAT}, and the DA gain at saturation $Gain_{PSAT}$ (a). Measured PAE_{P1dB}, PAE_{max}, and drain-efficiencies η_{1dB}, η_{max} (b). Measured AM-PM conversion at P_{1dB} (c). Measured gain, η, PAE, and AM-PM versus output power at 40 GHz (d).

The amplifier achieves a 16-dB gain with an in-band-ripple $< \pm 1$ dB and over 100 GHz 3-dB bandwidth. The 640 GHz gain-bandwidth product (GBW) is among the highest reported for non-cascaded DAs. The return loss at both ports is better than -7 dB across the 100 GHz operation bandwidth. The stability factor (k-factor) is higher than unity up to 120 GHz, while the noise figure (NF) is less than 7.2 dB up to 50 GHz with an minimum value of 4.1 dB at 20 GHz (Fig. 2.5(b)).

The CW large-signal performance of the PA is measured across frequency up to 60 GHz. In all measurements, the pads loss were included since they represent a part of the matching networks at both ports. The DPA achieves a P_{SAT} and P_{1dB} higher than 19 and 17 dBm, respectively, up to 60 GHz (Fig. 2.6(a)). The peak P_{SAT} is 22 dBm resulting in a P_{SAT} bandwidth

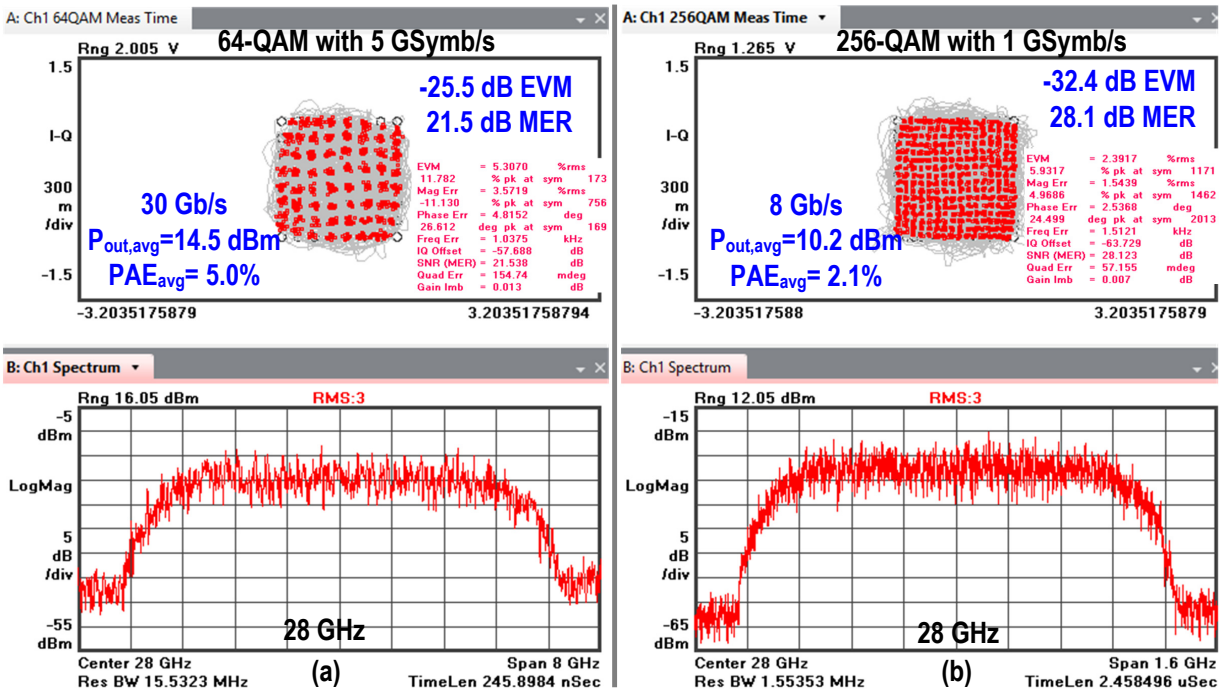

Figure 2.7: Measured constellations and spectrum for a 28 GHz carrier: (a) 64-QAM at 30 Gb/s and P_{out}=14.5 dBm, and (b) 256-QAM at 8 Gb/s and P_{out}=10.2 dBm.

of $\approx$ 60 GHz. Figure 2.6(b) presents the maximum and 1-dB values of the drain efficiency, η, and PAE across frequency. The PAE_{max} / PAE_{1dB} remain better than 10% / 8% at 60 GHz with state-of-the-art values of 19.5% / 14.8% around 15 GHz, compared to published DPAs, while the AM-PM non-linearity at the 1-dB compression point is $< 9.5^0$ from 1 up to 60 GHz. At 40 GHz, the PMOS-DPA delivers 21 dBm P_{SAT} with a 15.7% PAE from a -5 V supply. At the 1-dB compression point, the output power is 18.5 dBm with a PAE $>$ 10% while the AM-PM conversion is $< 5^0$ (Fig. 2.6(d)).

The PMOS-DPA is tested using 64/256-QAM signals to assess linear power and EVM performance under high PAPR, ultra-wide band mm-waves modulation at 28 GHz (Fig. 2.7). An Arbitrary waveform generator (Keysight AWG M8195A) is used to generate the complex-modulated signals at 7 GHz. The signals are then up-converted to 28 GHz using an external mixer and amplified before the probed DUT. A 63 GHz real-time scope (Keysight DSOZ632A) with the VSA software captures the signal and extracts the constellations and EVM, while a power sensor

is used to calculate the average P_{out}. All measurements are performed with linear equalization without digital pre-distortion. The real-time bandwidth dictating the maximum baud-rate is limited by the setup up-converting mixer, pre-amplifier and attenuator before the probed DUT. The PA achieves 30 Gb/s in 64-QAM with 14.5 dBm average P_{out}. For the 256-QAM, the DPA demonstrates 8 Gb/s with 10.2 dBm P_{out} while the EVM is kept below -32 dB.

Table 2.1: Comparison with state-of-the-art distributed power amplifiers

Design	**This work**		**[16] JSSC'16**	**[13] JSSC'15**	**[17] TMTT'19**	**[1] ISSCC'19**
Technology process	45nm PMOS SOI		130nm SiGe	130nm SiGe	45nm SOI	45nm SOI
Frequency (GHz)	1.5-103		14-105	DC-170	10-82	DC-108
Supply (V)	5		4, 3.6, 3.2, 2.7	3.6	1.5-2.4	5, 6.6
Gain (dB)	16		12	10	13	23
GBW (GHz)	**640**		362	537	322	1525
&P_{1dB} (dBm)	**19.0 @ 20GHz** **18.5 @ 40GHz** **17.5 @ 60GHz**		14.9 @ 50GHz	7.5* @ 50 GHz	13 @ 50GHz	20.8 @ 50GHz
&P_{SAT} (dBm)	**21.7 @ 20GHz** **21.0 @ 40GHz** **19.0 @ 60GHz**		17 @ 50GHz	9.4* @ 50 GHz	17.2 @ 50GHz	21.5 @ 50GHz
PAE_{max}(%) / **PAE_{P1dB}(%)**	**18.4**/12.0 @ 20GHz **15.7**/10.7 @ 40GHz **10.0**/8.4 @ 60GHz		12.6/8.5* @ 50GHz	N.R.	17.1/10* @ 50GHz	13.4/12.5 @ 50GHz
AM-PM **@P_{1dB} (^{0})**	-5 @ 40GHz		N.R.	N.R.	7.5* @ 50GHz	-3 @ 50GHz
Frequency (GHz)	28		N.R.	N.R.	42.5	59
Modulation	64-QAM	256-QAM			16-QAM	64-QAM
Bit-rate (Gb/s)	**30**	**8**			20	30
^EVM (dB)	-25.5	-32.4			-25.3	> -25
Pout (dBm)	**14.5**	**10.2**			11.7	13.2
PAE (%)	5.0	2.1			5.2*	4.7
External bias-tee	**No**		No	Yes	No	No
Core Area (mm^2)	**0.33**		1.51	0.38#	0.8	0.31

N.R. = Not Reported ^ Normalized to the constellation peak * Estimated from plots
& Best-setting at each frequency # Excluding required external bias-tee

Table 2.1 compares the stacked-PMOS design with recent published DPAs. This work demonstrates the highest GBW for non-cascaded DAs and provides state-of-the-art P_{1dB} and P_{SAT} up to 60 GHz. The PMOS PA achieves the highest reported PAE for mm-waves DPAs operating

from a single supply. Furthermore, the DPA achieves the highest data rate in 64/256-QAM. The PA has also the smallest footprint (including on-chip DC-feed) owing to the compact 8-shaped TLs and is able to operate from 1.5 GHz without bulky external bias-tees.

2.6 Conclusion

This work presented an all-PMOS stacked-SOI DPA using 8-shaped TLs and multi-section DC-feed. PMOS devices are proposed for the stacked DPA design for their higher reliability and comparable RF performance to NMOS in deeply-scaled technology nodes. The amplifier is fabricated in 45nm CMOS SOI and is able to operate from less than 1.5 GHz up to more than 100 GHz in an area comparable to non-distributed PAs (0.33 mm^2 excluding pads). The PMOS design achieves a 640 GHz GBW (from a non-cascaded structure) and delivers state-of-the-art performance in both CW and modulated signals measurements. Such performance suggests the inclusion of PMOS along with NMOS in mm-waves design for new technology nodes. Application areas include high resolution imaging systems, radars, millimeter-waves multi-Gb/s communications systems, and instrumentation.

2.7 Acknowledgment

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Chapter 2 is, in full, a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "A Compact pMOS Stacked-SOI Distributed Power Amplifier With Over 100-GHz Bandwidth and Up to 22-dBm Saturated Output Power," *IEEE Solid-State Circuits Letters*, vol. 2, no. 2, pp. 9–12, Feb 2019. The dissertation author was the primary investigator and primary author of this paper.

Chapter 3

A 120 GHz Bandwidth CMOS SOI Distributed Power Amplifier with Multi-Drive Intra-Stack Coupling

3.1 Introduction

The increasing demand for high data rates along with the emergence of millimeter-waves technologies, create a new interest in broadband circuit techniques. The ability of distributed amplifiers (DAs) to process ultra-narrow pulses and multi-Gb/s signals renders them attractive circuit blocks for wireline optical links, high-resolution imaging and radar applications. The DAs face a clear trade-off between the gain and output power (P_{OUT}) from one side , and the bandwidth and chip area from the other. While a number of DAs with a bandwidth over 90 GHz were successfully demonstrated in silicon-based technologies [13, 15, 16] their P_{OUT} and efficiency are relatively low, limiting their spectrum of applications.

In this work, a 16-dB gain, 120 GHz bandwidth DPA is realized in 45nm stacked CMOS-SOI. The PA adopts several techniques to compensate for the power and gain loss associated with

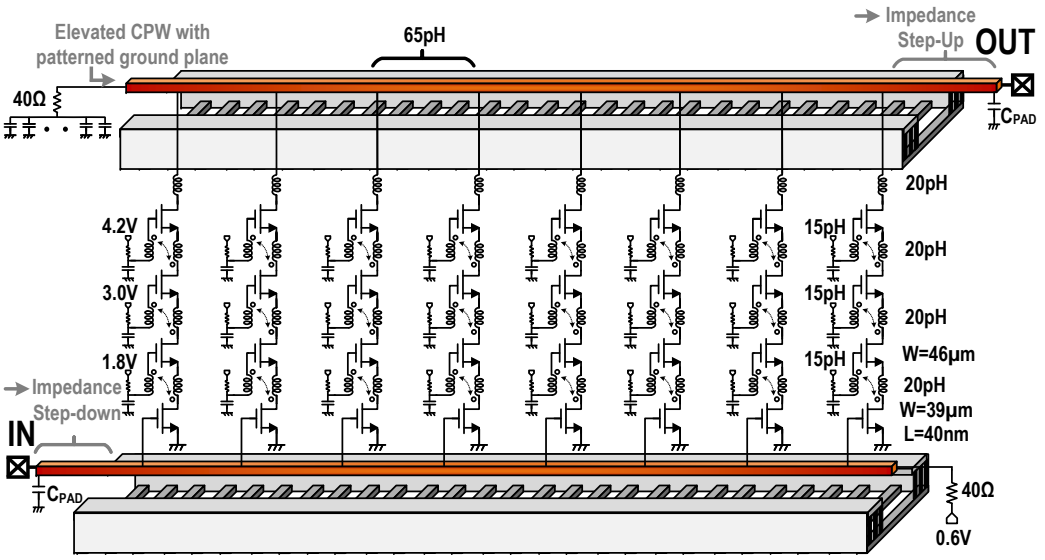

Figure 3.1: Schematic of the distributed power amplifier with multi-drive intra-stack coupling.

transmission lines (TLs) and gain cells at tens of gigahertz and maintains a saturated $P_{OUT} > 20$ dBm up-to-60 GHz. A 30 Gb/s, 64-QAM modulated signal is successfully demonstrated at 55 GHz with 13.5 dBm average P_{OUT} while the error vector magnitude (EVM) is kept below 5%.

3.2 PA Design

To generate high P_{OUT} under a limited supply voltage, large device sizes are needed for the PA design. This is achieved in a DPA structure by increasing the number of stages such that the parasitic capacitance of the devices is distributed over the input and output TLs to preserve the bandwidth, dictated by the cut-off frequencies of the loaded TLs. In practical implementations, the number of stages is limited by the input TL loss which increases with the square of the operating frequency [13]. Higher line loss causes less signal power to reach the last stages decreasing, thus, their gain and P_{OUT} contribution at high frequencies.

Several techniques are adopted in the proposed DPA to increase P_{OUT} without compromising the bandwidth (Fig. 3.1). The DPA consists of 8 stages. Each stage comprises a 4-stack gain cell with TL and stack loss compensation mechanisms, analyzed in section III . Staking is applied

to break the trade-off between the large power requirement and the limited cut-off frequency of the TLs due to the loading of large-sized devices. The amplifier, for each cell, is divided to 4 series combined PAs sharing the same current and with $4\times$ the supply. Consequently, only one fourth of input/output capacitance of the power amplifying devices need to be absorbed by the input/output TL. By controlling the swing at the gate nodes of the stacked devices, the PA output voltage swing and impedance can be evenly divided between the devices in the stack, diminishing the need for band-limiting and lossy output transformation network for maximum P_{OUT} delivery.

In order to minimize reflections and improve the matching and in-band gain flatness, the loaded input and output TLs impedances need to be designed near 50 Ω. Therefore, the unloaded input and output TLs characteristic impedances (Z_0) should be designed as high as possible such that they are able to absorb high device capacitance. This can be achieved by reducing the width of the TLs at the expense of more resistive loss and, consequently, a limited number of stages. In the proposed design, both TLs are implemented as elevated coplanar waveguides (CPW) where the signal track is higher than the accompanying ground strips. This leads to an increase in Z_0 of the line without the need to decrease the signal track width. A patterned ground plane is added as a substrate shield to improve signal confinement at the expense of some Z_0 reduction. The loaded impedance of both lines is designed to be ≈ 40 Ω, and this value is chosen in order to maximize P_{OUT} of the 4-stack DPA structure based on load-pull simulation. The input and output pads routing and parasitic capacitance are then exploited to form small step-down impedance transformation networks for better matching and power performance.

3.3 Intra-Stack Coupling Gain Cells

The design of the gain cells need to accommodate high P_{OUT} while ensuring a bandwidth over 100 GHz. A 4-stack topology reduces the capacitive loading on the input and output TLs and increases P_{OUT} by scaling the supply. For a reliable operation, the drain-to-source (V_{DS}) and

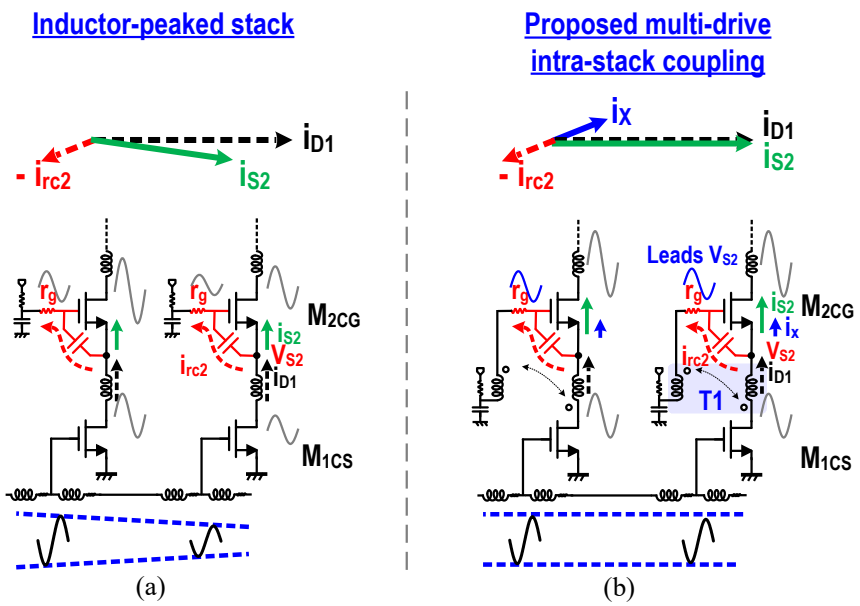

Figure 3.2: Schematic and current phasor diagram of (a) the inductor-peaked unit cells compared to (b) the proposed multi-drive intra-stack coupling.

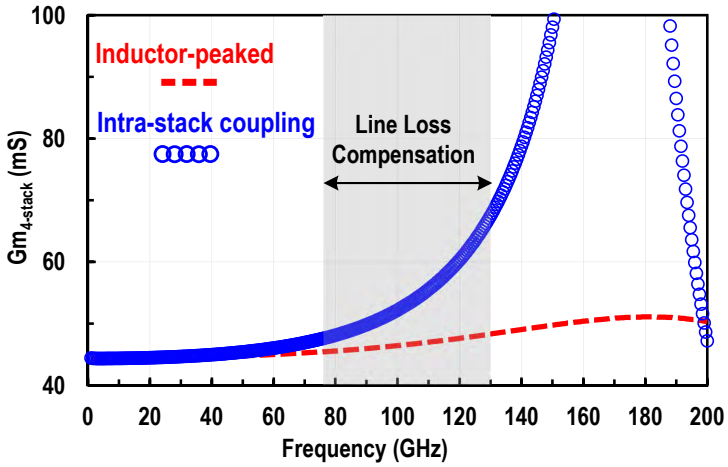

Figure 3.3: Simulated transconductance (Gm) for a 4-stack unit cell using series inductor peaking versus intra-stack coupling across frequency .

drain-to-gate (V_{DG}) voltages of all devices need to be kept under the break-down value. This is traditionally achieved by controlling the gate swing of the stacked devices using a capacitive divider between the gate-to-source capacitance (C_{gs}), and a discrete capacitor placed between the gate and the ground node. The current generated by the input common-source (CS) MOS is buffered to a higher impedance at the output of the stacked MOS and the power is added in a

series fashion. However, at tens of gigahertz, a portion of the RF current is lost in the intra-stack parasitic capacitance and the combining efficiency is reduced limiting the benefit of stacking and requiring peaking inductors to restore the performance. For a DPA structure, the peaking inductors should be placed in series to provide wide-band and DC operation at the expense of series resistive loss (Fig. 3.2(a)). The peaking inductors resonate with the intermediate nodes parasitic capacitance to align the current within the stack and improve the combining efficiency.

However, at 40 GHz and above, a part, i_{rc2}, of the current generated by the CS device (M_{1CS}), i_{D1}, is dissipated in the gate resistance (r_g) of the stacked common-gate (CG) device (M_{2CG}). The current loss increases with frequency and less current, i_{S2}, end up entering M_{2CG}, even if aligned with i_{D1}. As a result, the current at the top of the stack, and thus P_{OUT} and the efficiency, are reduced with frequency. To improve the performance, a multi-drive stacked-FET topology was proposed in [21], where the gate swing of the stacked device is controlled by a dedicated pre-driver to generate an extra current component, i_X, with the same magnitude and phase of i_{rc2}, to align and equate i_{D1} and i_{S2}. However, the benefit of the stack multi-driving is diminished by the need of power consuming pre-drivers particularly at lower frequencies where less stack driving is needed. The need to adjust the relative phases for the different driving signals also increases the layout complexity.

For a distributed structure, the stack multi-drive can be efficiently applied by tapping a part of the voltage swing at the drain of the device M_n to the gate of the stacked device M_{n+1} within the same stack (Fig. 3.2(b)). The voltage at the gate of M_{2CG} now slightly leads its source voltage V_{S2} which forces M_{2CG} to inject i_X in phase with i_{rc2} to compensate for the current lost (in the ideal case). The leading gate voltage also helps in compensating the loss in the intra-stack parasitic capacitance. Therefore, the series inductors size can be reduced for lower loss and smaller footprint. The realization of the multi-drive intra-stack coupling with a small transformer (T1), ensures the technique is only applied at high frequencies, when the gate resistance loss is relevant.

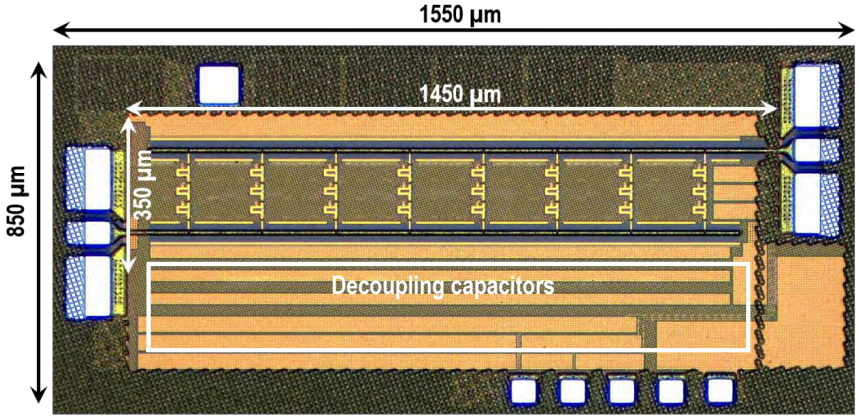

Figure 3.4: Die micrograph of the fabricated distributed power amplifier chip in 45nm CMOS SOI process.

The operation bandwidth of the multi-drive technique is controlled by the coupling between both inductors of T1, and adjusted by their separation. The intra-stack coupling increases the effective transconductance of the stack (Gm) at high frequency to compensate for the input TL loss for a flat gain (Fig. 3.3). In addition, the presence of a small gate inductance for M_{2CG} reduces the loss of the loaded input TL. The gate inductance of M_{2CG} generates a negative real component at the source node which is translated to the input TL through the gate-to-drain capacitance of M_{1CS}. The technique is only applicable if the gate inductance is small enough to ensure the real part of the impedance of the TL remains positive over the entire frequency range. The compensation of both the input TL and the stacks enables more stages and larger devices to be used and, thus higher P_{OUT}, without compromising the bandwidth.

3.4 Implementation

The proposed multi-drive intra-stack coupled DPA is implemented in 45nm CMOS SOI process with a core area of 0.35×1.45 mm^2 (Fig. 3.4). Floating-body, thin-oxide, partially depleted NMOS are used for all the devices within the 8 stacks. The NMOS peak f_t and f_{max} are 250 and 290 GHz, respectively, when referenced to the top metal. The stacked devices are slightly larger than the input CS ones to help compensate for the group delay between the input

and output TLs per stage. The difference needed in size is less than 20% owing to the extra input line compensation from the intra-stack coupling. The elevated CPW signal lines are implemented on the top 2 μm-thick aluminum layer, while the ground lines are on a lower 1.2 μm-thick copper layer with shorted vias to the patterned ground plane, placed orthogonally to the signal path. The intra-stack coupling transformers are implemented on the upper two copper layers (both 1.2 μm-thick) with a custom ground plane underneath to localize the coupling within each stack. The gate biasing for the stacked devices is provided while placing R-C sections between the bias nodes of the different stages for common mode stability. The distance between stages is 150 μm, providing $\approx$ 65 pH per section and adequate devices separation for thermal management at high power levels. Each RF pad provides an extra 13 fF parasitic capacitance which is used as a part of the matching network at both ports.

3.5 Measurements

The small signal performance of the intra-stack coupled DPA is measured from DC-to-140 GHz using three setups. For frequencies less than 70 GHz, the chip is wafer probed while using a vector network analyzer (Keysight N5247A PNA-X) combined with 1.85 mm coaxial connectors. The PNA-X also provides a bias-tee for the output port. A millimeter-head controller and two sets of frequency extenders modules are then added with WR-10 probes to cover the range from 75-to-110 GHz, and with WR-6 probes for the range above 110 GHz. The measurement results of all three setups are concatenated and plotted in Fig. 3.5. The PA achieves a 16-dB in-band gain with a 3-dB bandwidth of 120 GHz (Fig. 3.5(a)), and a record GBW of 757 GHz for non-cascaded DAs. The amplifier maintains an excellent matching at both ports keeping S_{11} and S_{22} both below -10 dB up to 110 GHz. Owing to the good matching, the measured stability factor (k-factor) is better than 2.8 for the whole frequency range. The noise figure (NF) is also measured from DC-to-50 GHz with minimum of 4.2 dB at 35 GHz while the maximum value is less than 6.2 dB

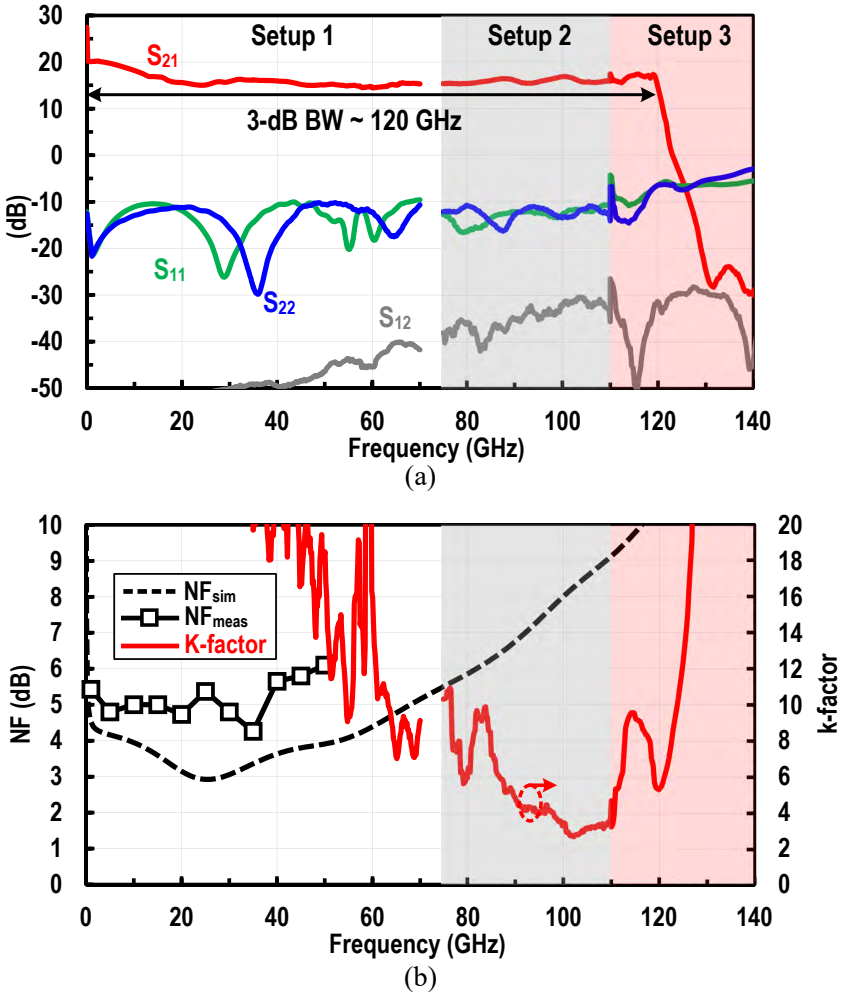

Figure 3.5: Small-signal performance versus frequency: (a) measured S-parameters; (b) Noise figure and stability factor (k-factor).

at 50 GHz (Fig. 3.5(b)).

The continuous-wave (CW) large-signal performance vs both power and frequency is shown in Fig. 3.6. The DPA is measured from DC-to-70 GHz without de-embedding the pads loss, since they are parts of the matching networks at both ports. The DPA achieves a $P_{SAT} > 20$ dBm, while P_{1dB} is $>$ 18 dBm up-to-60 GHz (Fig. 3.6(a)). The DPA demonstrates a peak P_{SAT} and P_{1dB} of 23 and 21.3 dBm, respectively, around 20 GHz. The maximum and 1dB values of the drain efficiency, η, and PAE are plotted in Fig. 3.6(b). The amplifier shows a maximum PAE $>$ 10% up to 60 GHz with a state-of-the-art maximum of 19.7% at 15 GHz compared to published

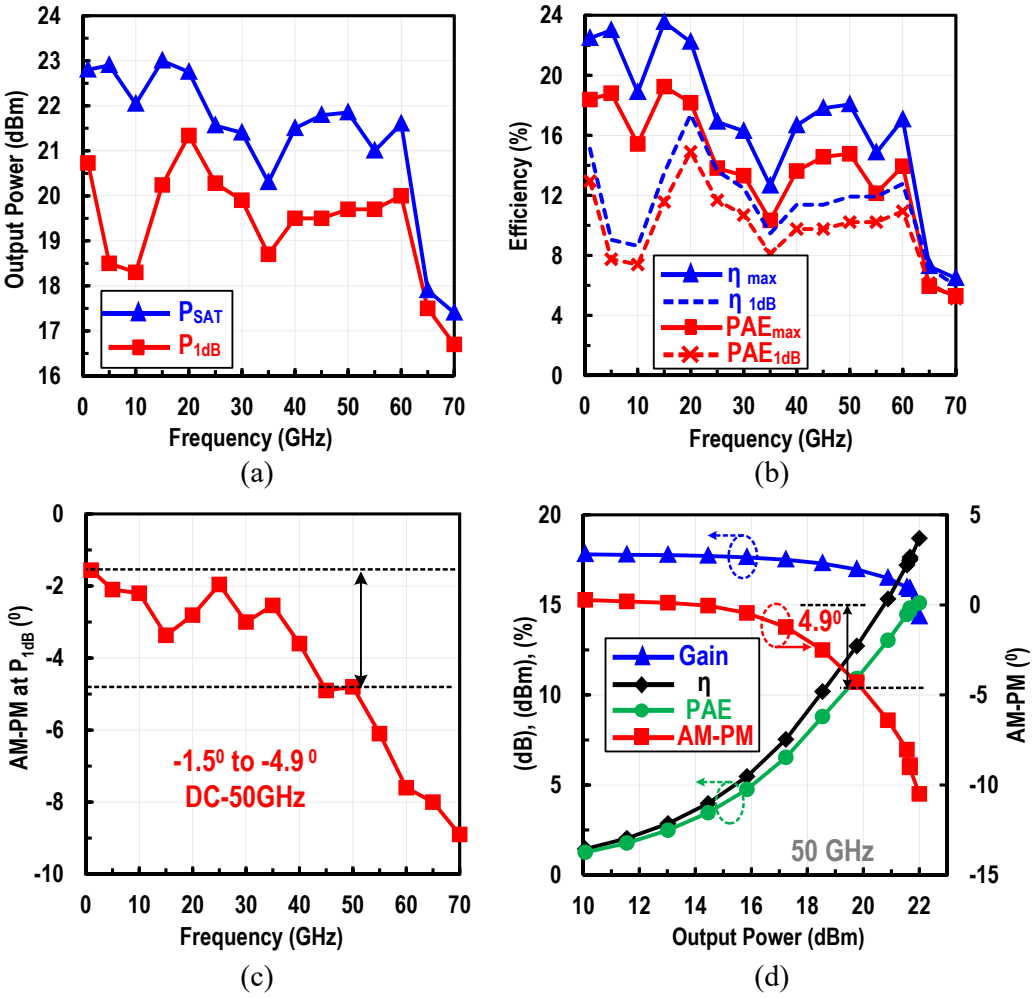

Figure 3.6: CW large-signal performance: measured P_{1dB}, P_{SAT} and AM-PM across frequency (a & c). Measured PAE_{P1dB}, PAE_{max}, and drain-efficiencies η_{1dB}, η_{max} versus frequency (b). Measured gain, η, PAE, and AM-PM versus output power at 50 GHz (d).

DAs. The AM-PM non-linearity at P_{1dB} remains less than 5^0 from DC-to-50 GHz while it is less than 10^0 at P_{SAT} (Fig. 3.6(c, d)).

Modulated data measurements are conducted with 64-QAM signals at 55 GHz. The EVM is measured using an arbitrary waveform generator as a source followed by an up-converting mixer, attenuator and amplifier before the probed DUT. A real-time-scope (Keysight DSOZ632A) with the VSA software is used to capture the signal and extract the constellations and EVM. The power is measured using a coupler before the scope, connected to a power sensor. Baud rates up to 5 GBaud/s (30 Gb/s) are tested while the EVM is kept below -25 dB. The measured 64-QAM

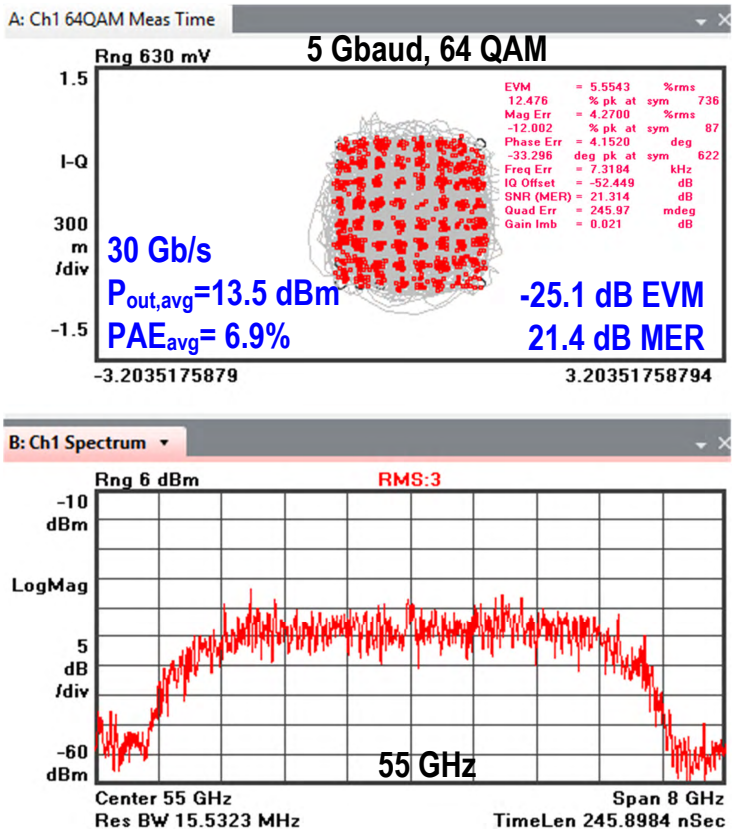

Figure 3.7: Measured 64-QAM constellation and spectrum with 13.5 dBm average output power for a 30 Gb/s data rate at 55 GHz.

constellation and the respective frequency spectrum are shown in Fig. 3.7 for a 55 GHz carrier. The DPA achieves an average P_{out} of 13.5 dBm with a PAE of 6.9%. To the authors' knowledge, this is the highest data rate, average P_{OUT}, and modulated PAE for reported DAs at frequencies higher than 50 GHz.

Table 3.1 compares the intra-stack coupled DPA with other published wide-band and distributed PAs. This work achieves the highest GBW for non-cascaded DAs while providing state-of-the-art P_{1dB} and P_{SAT} performance up to 70 GHz. The DPA also demonstrates the highest 64-QAM modulation bit rate (30 Gb/s) with the highest average P_{OUT} for a 55 GHz carrier. The DPA has the highest CW and modulated PAE compared to other published DAs while the area is comparable to silicon-based non-distributed PAs achieving the same power level.

Table 3.1: Comparison with wideband millimeter-wave

Design	This work	[2] JSSC'19	[3] SSCL'19	[17] TMTT'19	[16] JSSC'16
Technology process	45nm RFSOI	45nm RFSOI	45nm RFSOI	45nm RFSOI	130nm SiGe
Frequency (GHz)	DC-120	DC-108	1.5-103	10-82	14-105
Supply (V)	4.8	5/6.6	5	1.5/2.4	4, 3.6, 3.2, 2.7
Gain (dB)	16	23	16	13	12
GBW (GHz)	757	1525	640	322	362
$^{\&}P_{1dB}$ (dBm)	21.3 @ 20 GHz 19.5 @ 40 GHz 20.0 @ 60 GHz	19.5 @ 25 GHz 20.8 @ 50 GHz 17.5 @ 70 GHz	19.0 @ 20 GHz 18.5 @ 40 GHz 17.5 @ 60 GHz	13 @ 50 GHz	14.9 @ 50 GHz
$^{\&}P_{sat}$ (dBm)	22.6 @ 20 GHz 21.4 @ 40 GHz 21.6 @ 60 GHz	20.5 @ 25 GHz 21.5 @ 50 GHz 18.4 @ 70 GHz	21.7 @ 20 GHz 21.0 @ 40 GHz 19.0 @ 60 GHz	17.2 @ 50 GHz	17 @ 50 GHz
PAE_{max}(%) / PAE_{P1dB}(%)	18/13.8 @ 20 GHz 15/10 @ 40 GHz 14/10.2 @ 60 GHz	10.8/9.1 @ 25 GHz 13.4/12.5 @ 50 GHz 6.8/5.9 @ 70 GHz	18.4/12 @ 20 GHz 15.7/10.7 @ 40 GHz 10/8.4 @ 60 GHz	17.1/10 @ 50 GHz	12.6/8.5* @ 50 GHz
$^{\&}$AM-PM @ P_{1dB} (^{o})	-1.5 to -5 from DC to 50 GHz	+2.1 to -3.6 from DC to 70 GHz	-5 @ 40 GHz	7.5* @ 50 GHz.	N.R.
Frequency (GHz) Modulation Bit-rate (Gb/s) $^{\#}$EVM (dB) Pout (dBm) PAE (%)	55 64-QAM 30 -25 +13.5 6.9	59 64-QAM 30 -25 +13.3 4.7	28 64-QAM 30 -25 +14.5 5	47.5 16-QAM 20 -25 11.8* 7.5*	N.R.
Core Area (mm^2)	0.51	0.31	0.33	0.8	1.51

* Estimated from plots
& Best-setting at each frequency
N.R. = Not Reported
# Normalized to peak of the constellation

3.6 Conclusion

This work presented a 16-dB gain, 120 GHz bandwidth DPA with elevated CPW TLs and multi-drive intra-stack coupled gain elements to achieve high power levels without compromising the bandwidth. The amplifier achieves a record GBW of 757 GHz for non-cascaded DAs and maintains output P_{1dB} and P_{SAT} higher than 18 and 20 dBm, respectively, up-to-60 GHz. At 55 GHz, the DPA is able to provide a 30 Gb/s 64-QAM signal with 13.5 dBm average P_{OUT} and an EVM less than 5%. The amplifier can be used as an optical modulator driver, in imaging applications, millimeter-waves instrumentation, and for multi-Gb/s communications systems.

3.7 Acknowledgment

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Chapter 4

A DC-to-108 GHz CMOS SOI Distributed Power Amplifier and Modulator Driver Leveraging Multi-Drive Complementary Stacked Cells

4.1 Introduction

Broadband power amplification is essential in high resolution imaging systems, millimeter-waves instrumentation, and multi-gigabit wireless and wireline communication links. In the past 5 years, both data center and mobile data traffic increased by several folds [22]. This increasing demand for higher data rates projects a continuous need for improvements in broadband power amplification techniques.

Distributed amplifiers (DAs) are suitable candidates for all these systems due to their superior operational bandwidth over other broadband topologies, low sensitivity to components mismatch and modeling inaccuracies, and broadband power matching. Since their invention

by Percival in 1936 a substantial effort was made to improve the DAs gain [23–27], bandwidth (BW) [28–32], efficiency [16], power [15, 17, 33–36], and noise performance [37, 38]. However, the usage of DAs in power generation poses a clear trade-off between the BW and the achieved power level where large power devices limit the cut-off frequency of the distributed power amplifier (DPA) transmission lines (TLs). Producing over 100 mW of power in the gigahertz range from a DPA with over 100 GHz of BW is still a challenging task for silicon-based designs.

DAs are equally important for optical wireline systems where a BW $>$ 50 GHz is usually required for over 100 Gb/s links. Multi-level pulse amplitude modulation (PAM) and quadrature amplitude modulation (QAM) are suggested for future photonic systems to satisfy the prolific data rates for next generation 400 Gb/s standards [39, 40]. The half-wave voltage (V_π) for the system MachZehnder modulator (MZM) is typically $>$ 3 V for InP and often surpasses 4 V for silicon photonics [41–44]. The design of high voltage-swing broadband linear drivers for the MZM is mostly confined to SiGe [45–48] and group III-V semiconductors [49, 50]. Although FETs stacking [51] in CMOS SOI can achieve reliable high voltage swings with power levels reaching 25 dBm from a single ended 4-stack at 28 GHz [52], most of the published stacked optical drivers are limited to non return to zero (NRZ) modulation [43] and a 100 Gb/s for a linear PAM-4 modulation with over 4 V swing is yet to be demonstrated in CMOS. A CMOS implementation in an advanced high density node is highly desirable for monolithic integration with the back-end.

In this chapter, a complementary stacked SOI DPA and linear driver is proposed with over 100 Gb/s 64-QAM and PAM-4 modulations. This work is an expanded version of [1], and provides additional design details on the architecture and circuit levels. This work also provides new measurements for small-signal, continuous-wave (CW) large-signal, and time domain performance for both complex modulated data and serial data, to further highlight the linearity and flexibility of the design. More comprehensive comparison tables are included to benchmark the proposed DPA when operated as a broadband amplifier (in both CW-mode and

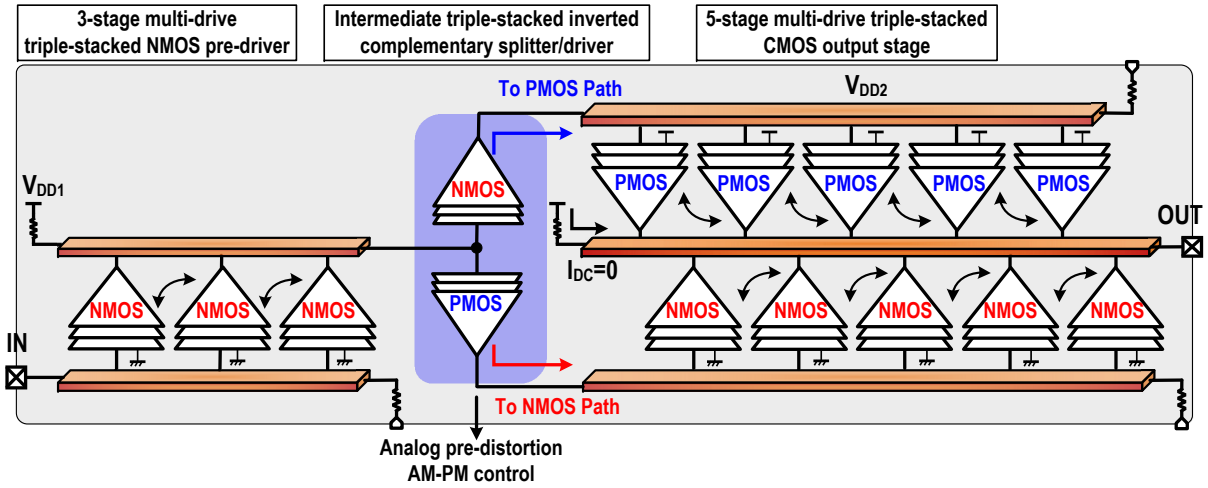


Figure 4.1: Architecture of the CMOS distributed amplifier with multi-drive inter-stack coupling.

complex modulated data mode) and as a linear modulator driver.

4.2 Multi-Drive Cascaded Distributed Power Amplifier Architecture

The CMOS DPA architecture is shown in Fig. 4.1. The DPA consists of three cascaded amplifiers: an input 3-stage NMOS DA with supply-fed termination drives an intermediate inverted complementary driver. The latter splits the signal in two paths, NMOS and PMOS, to feed a dual-input 5-stage triple-stacked output CMOS DPA. The DPA uses several techniques to break the trade offs between gain, BW, power, and area in a conventional DA design. These trade-offs and the proposed techniques are explained on the architecture level in this section, and on the circuit level in section III .

4.2.1 Gain-Bandwidth Enhancement

The GBW has been the conventional way to benchmark DAs where larger devices typically have higher power gains but larger capacitance which limits the input TL cut-off frequency, f_c,

and thus the BW given by:

$$f_c = \frac{1}{\pi\sqrt{L_u \times C_u}}, \tag{4.1}$$

where L_u and C_u are the input and output TLs inductance and loaded capacitance per stage, including the parasitics of the active element. The input capacitance of the gain stage typically dominates C_u and limits f_c.

Cascading several stages, however, alleviates this trade-off by increasing the gain for a fixed BW at the expense of efficiency. Cascading also reduces the overall chip area for a targeted GBW. In this case, we consider synchronized signal propagation and similar loaded impedance $Z_\circ$ for both input and output TLs, for N identical cascaded stages, each comprising M_1 unit gain cells with an effective transconductance gm_u. When the loss per stage is dominated by the input TL, the power gain by [53] can be simplified as:

$$G_{N,M_1} = \left((gm_u \frac{Z_\circ}{2}) \times \frac{(e^{-M_1\alpha(\omega)} - 1)}{\alpha(\omega)} \right)^{2N} \tag{4.2}$$

$$\approx \left((M_1 gm_u \frac{Z_\circ}{2}) \times (1 - M_1 \frac{\alpha(\omega)}{2}) \right)^{2N}, \tag{4.3}$$

where $\alpha(\omega)$ is the attenuation per stage for the propagated wave across the lossy input TL, dominated by the gate resistance, which increases quadratically with frequency [13, 53]. The overall GBW increases exponentially with N while the chip footprint scales in a linear fashion.

The number of cascaded stages is usually limited in DAs by the stability due to the high gain and limited reverse isolation. While the overall efficiency also degrades, in case of a DPA, since pre-drivers are usually less efficient compared to the output stage. The 3-stages, including the pre-driver, active splitter and active combiner, are used to achieve a gain $>$ 20 dB with a BW $>$ 100 GHz. A compact area is targeted by providing an overlap for an intentional magnetic coupling between consecutive gain cells and TL sectors described in sections III & IV .

4.2.2 Power Enhancement

In addition to the GBW trade-off, a clear trade-off exits between BW and the achieved P_{SAT} for silicon-based DPAs. This is because achieving higher P_{SAT} under a limited supply voltage typically requires larger devices to handle the desired current, which compromises the BW. The output power is increased for DPAs by increasing the number of gain cells without sacrificing the BW. The number of gain cells is usually limited by the input TL insertion loss which increases with frequency [54–56]. As a result, less input signal swing reaches the final cells for a DA limiting their contribution in the overall gain and P_{out}. The number of DPA gain cells in published work is limited to 8 [15–17], a point after which the power and gain improvements are limited while efficiency degradation is considerable.

The proposed design uses triple-stacked FETs in all gain cells. Stacking N-FETs [52, 57, 58] relaxes the power-BW trade-off since only 1/N of the overall devices capacitance need to be absorbed by the input/output TLs for a targeted P_{out}. However, in the DPA design, efficient operation of the stacked gain cells up to 100 GHz is mandatory in order not to limit the performance prior to the TLs f_c. The DPA design uses triple-stacked gain cells to achieve an optimum load impedance near 50 Ω for the output stage and avoids band limiting matching networks. In addition, the multi-drive inter-stack coupling technique [1], described in section III, is applied to increase the GBW, improve P_{out} delivery and compensate for the input TL loss at high frequencies.

The output stage is split to two parallel DPAs to achieve the required P_{out} with a higher GBW compared to a single DPA. When the input and output TL impedance are not equal, (4.3) becomes:

$$G_{1,M_2} = \left((M_2 g m_u \frac{\sqrt{Z_g Z_d}}{2}) \times (1 - M_2 \frac{\alpha(\omega)}{2}) \right)^2, \tag{4.4}$$

where $Z_g = \sqrt{L_g/C_g}$ and $Z_d = \sqrt{L_d/C_d}$ are the gate an drain TL $Z_\circ$, respectively, while $L_g C_g = L_d C_d$, for an equal propagation constant β for both lines. For maximum P_{out}, Z_d should be

designed equal to R_{opt} given by:

$$R_{opt} = \frac{v_{max,M1}}{i_{max,M1}}, \tag{4.5}$$

where $v_{max,M1}$ and $i_{max,M1}$ are the maximum voltage and current fundamental swing of the last unit cell. Typically, Z_d is designed near 50 Ω to avoid BW limitations, while it is desired to increase Z_g to improve G. However, the input unit-cell capacitance is usually higher than the output one in silicon technologies leading to a lower impedance $Z_g = k \times R_{opt}$ where $k = C_d/C_g < 1$. Therefore, G is reduced by a factor k compared to (4.3). The gain can be restored by increasing the stacked devices size with respect to the input devices at the expense of higher intra-stack parasitic capacitance and an f_c reduction. Alternatively, when the DPA is split to two parallel stages with two input TLs, the impedance for each input TL becomes $Z_g = 2k \times R_{opt}$, keeping equal β for all 3 TLs. In the proposed design, the two output DPAs are complementary leading to a larger PMOS DPA size ζ times, compared to the NMOS one, for an equal power split. $\zeta = \mu_n/\mu_p > 1$ represents the ratio of mobility (μ) of the NMOS to PMOS. The impedances of both input TLs become:

$$Z_{g,N} = k(1+\zeta^1) \times R_{opt} \tag{4.6}$$

$$Z_{g,P} = k(1+\zeta^{-1}) \times R_{opt}, \tag{4.7}$$

while,

$$r_G = \frac{G_{CMOS}}{G_{NMOS}} = \frac{(1+\zeta^1) \times (1+\zeta^{-1})}{2} > 2. \tag{4.8}$$

G_{CMOS} represents the gain for the complementary output stage, while G_{NMOS} is the gain of an NMOS output stage with a single input TL generating similar P_{out}. Additionally, f_c for the CMOS topology is reduced due to the higher C_d from the PMOS side where:

$$r_{f_c} = \frac{f_{c,CMOS}}{f_{c,NMOS}} = \frac{2}{(1+\zeta^1)}, \tag{4.9}$$

leading to:

$$r_{GBW} = \frac{GBW_{CMOS}}{GBW_{NMOS}} = (1 + \zeta^{-1}) > 1, \tag{4.10}$$

which shows a higher GBW for the CMOS design under the same R_{opt} and P_{out}. In standard CMOS technologies, ζ is ≈ 2, while it reduces to 1.2 in the used 45RFSOI technology, as discussed in section III .C, leading to further GBW enhancement.

4.2.3 True DC-Operation and Efficiency Enhancement

It is desired to operate the DPA from the MHz frequency range to be used as a linear driver for optical and wireline applications. This is traditionally achieved by having a supply fed resistive termination either in distributed or lumped designs [14, 45–47, 59] which limits the efficiency and the achieved output swing. Some designs report the usage of an on-chip bias-tee which sets a lower limit on the tested baud-rates and distorts the group delay [59], or bulky external bias-tees [13] for an area penalty. The proposed design does not use any capacitive coupling between cascaded stages or any bias-tee. The supply resistive biasing is only used in the first and intermediate stages and is essential to provide matching and flat gain from true DC. The output stage provides 15 dB gain out of 23 dB overall in order to compensate for the inefficient pre-driver due to resistive DC power loss. The intermediate pre-driver/power splitter is designed to provide a real low input impedance across the power levels and frequency spectrum from DC. The CMOS current-reuse topology in the output stage enables operation from DC with large voltage swing while no current flows in the output termination resistor under equal NMOS-PMOS drive. Without DC power dissipation in the termination resistor, the DPA efficiency can be optimized.

4.2.4 Linearity Enhancement

The presence of complementary paths (NMOS and PMOS), in both intermediate and output stages, is exploited to compensate for both AM-AM and AM-PM non-linearity [60, 61]. This is satisfied by independent NMOS-PMOS biasing which sets the classes of both output complementary DPAs. An extra degree of freedom is achieved by controlling the input signals amplitudes or the power division ratio between both paths.

4.3 Multi-drive DPA circuits design

In this section circuit techniques allowing the performance enhancements of the DPA over conventional designs are explained. In addition, a comparison is conducted between the performance of stacked NMOS versus PMOS DAs in 45nm RFSOI to validate the inclusion of PMOS leading to the implemented CMOS Stacked-SOI DPA.

4.3.1 Multi-Drive for Stacked Gain-Cells

To arrive at the DPA unit-cell, a 3-stack inductor-peaked cell is first studied (Fig. 4.2(a)). The peaking inductors should be placed in series to operate from DC at the expense of series resistive loss. The inductors resonate with the intermediate-node parasitic capacitances and increase the effective Gm at high frequencies to help compensate for the input TL loss [13].

There remains, however, a part, i_{rc2}, of the current generated by the common-source device (M_{1CS}), i_{D1}, which is lost in the gate resistance (r_g) of the stacked common-gate device (M_{2CG}) through its gate-to-source capacitance Cgs. As frequency increases, the current at the top of the stack becomes lower than that generated by M_{1CS} (even if aligned), reducing the benefit of stacking. A multi-drive stacked cell [21] can alleviate this problem by forcing the common-gate device to inject an extra current compensating the current lost in r_g. However,

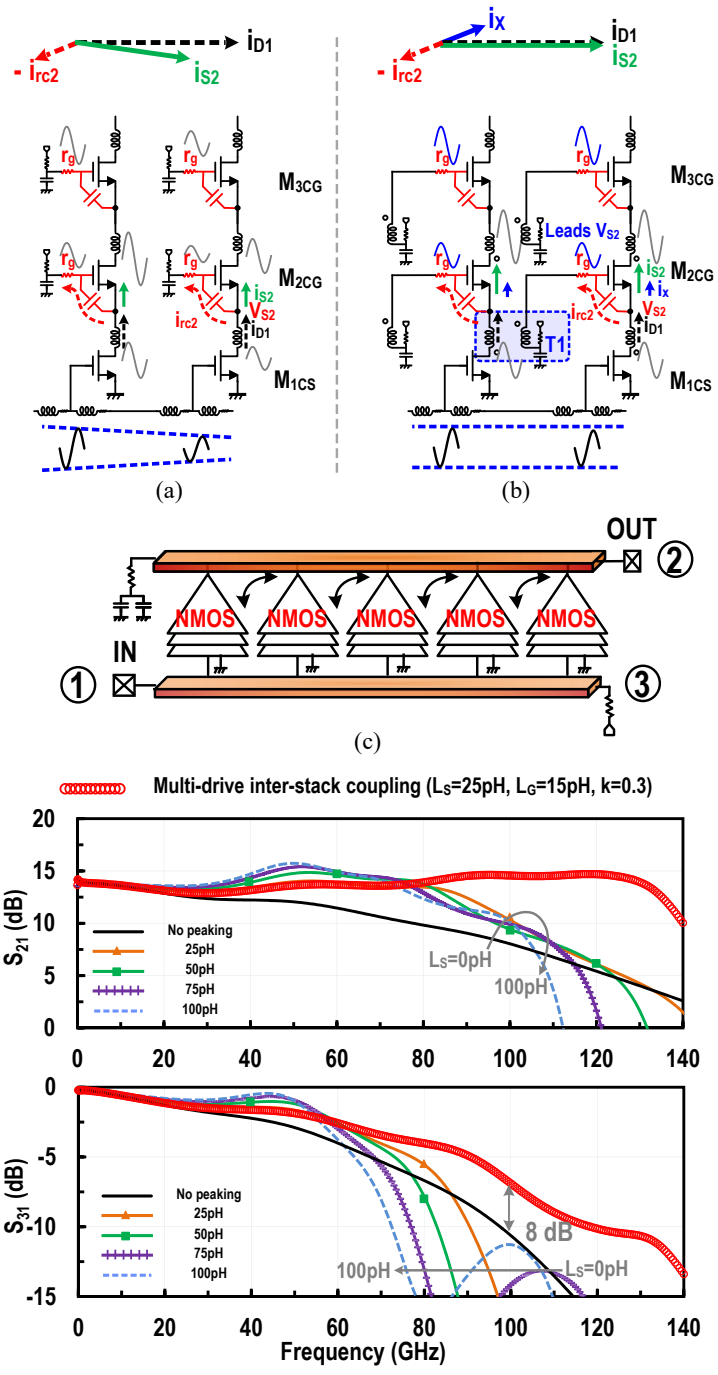


Figure 4.2: (a) Schematic and current phasor diagram for (a) inductor-peaked versus (b) multi-drive inter-stack coupling unit-cells. (c) Schematic of a 5-stage triple-stacked DPA. (d) Simulated gain and input TL insertion loss of the 5-stage DPA for inductor-peaked versus multi-drive inter-stack coupled cells.

the dissipated power of the common-gate drivers renders this technique non-efficient at lower frequencies, where less stack driving is needed. For a distributed structure, a stack multi-drive can be efficiently implemented by tapping a part of the voltage swing from the output of device M_n to drive the gate of the device M_{n+1} of the following stage (Fig. 4.2(a)). The gate swing of M_{2CG} now slightly leads its original source voltage (V_{S2}), creating an extra current component (i_X) equal in amplitude and phase to i_{rc2} (in ideal operation) to align and equate i_{D1} and i_{S2}. Tapping from a previous stage also results in a leading voltage to compensate for the currents in the parasitic capacitance at V_{S2}, and thus the series inductor can be reduced for lower loss.

The use of a small transformer (T1) for the feed-forward tapping ensures the technique is only applied at high frequencies when the multi-drive is needed while the behavior follows the traditional inductor peaked stacked FETs at lower frequencies. The coupling between the primary and secondary of T1 is adjusted by their separation to control the BW where the tapping is applied.

T1 offers another advantage by having a small inductor at the gate of M_{2CG}. This inductor can create a negative real impedance component at V_{S2}, which is translated through the gate-to-drain capacitance (Cgd) of M_{1CS} to compensate for the input TL loss at high frequencies. The effect is illustrated by simulating the gain and insertion loss of the loaded input TL of a 5-stages NMOS DPA employing the multi-drive inter-stack coupling and comparing it to the case employing inductor peaked gain-cells (Fig. 4.2(c & d)). The simulated BW extension is $\approx$ 40% compared to the series inductor peaking while the insertion loss is 8 dB lower when using the multi-drive inter-stack coupling at 100 GHz. A lower insertion loss allows increasing the number of stages for higher gain and P_{out} for the required BW. Similar to the emitter capacitive degeneration used in most SiGe DAs, the inductor value should be kept small to ensure the real part of the TL input impedance remains positive over the entire frequency range.

4.3.2 Inverted Complementary Dual Path Driver

In order to allow DC operation in the cascaded structure, an intermediate network is needed to DC couple the signal out of the pre-driver DA to both output complementary DPAs. The intermediate stage should act as a power splitter, level shifter and a load for the pre-driver DA. An active inverted complementary topology is proposed for this role (Fig. 4.3(a)). The 3-stack NMOS and PMOS set suitable DC bias points for the following DPAs through the DC current flowing in their respective drain resistive loads. The power split ratio and the two path gains are set by the ratios and absolute values of Gm for both paths. These are achieved by independent control for the two biasing knobs $V_{GN,CG}$ and $V_{GP,CG}$. A similar voltage variation for both knobs controls the power (current) split ratio, while an opposite variation controls the path gains. An important aspect in the design is to limit the input impedance (Z_{in}) variation, for the driver, across the input signal swing for a broadband frequency spectrum. A large variation in Z_{in} can sacrifice the stability and the output matching of the pre-driver, and thus the overall gain flatness. The complementary splitter structure with equivalent Gm from both sides reduces Z_{in} variation which follows the lower impedance for both paths across the swing (Fig. 4.3(c)). Furthermore, the input capacitance variation is partially compensated by the opposite variation of NMOS and PMOS gate-to-source capacitance (Cgs) versus the voltage swing (Fig. 4.3(b)). The real part of Z_{in} is adjusted close to 35 Ω which is equal to $Z_{\circ}$ of the output TL for the input pre-driver (Fig. 4.3(c)). The input capacitance degrades the matching however the degradation is not severe since it is partially resonated by the input TL. The intra-stack series peaking inductors (25 pH) are used to reduce the effect of the wiring and parasitic capacitance within the stack. The output impedance of the 3-stack is $\approx$ 90 Ω yielding to a worst case S_{22} = -7 dB in the MHz range (Fig. 4.3(d)). The active splitter provides a power gain of 3-to-0 dB from DC-to-100 GHz while the simulated k-factor is $>$ 1.15 (Fig. 4.3(e)).

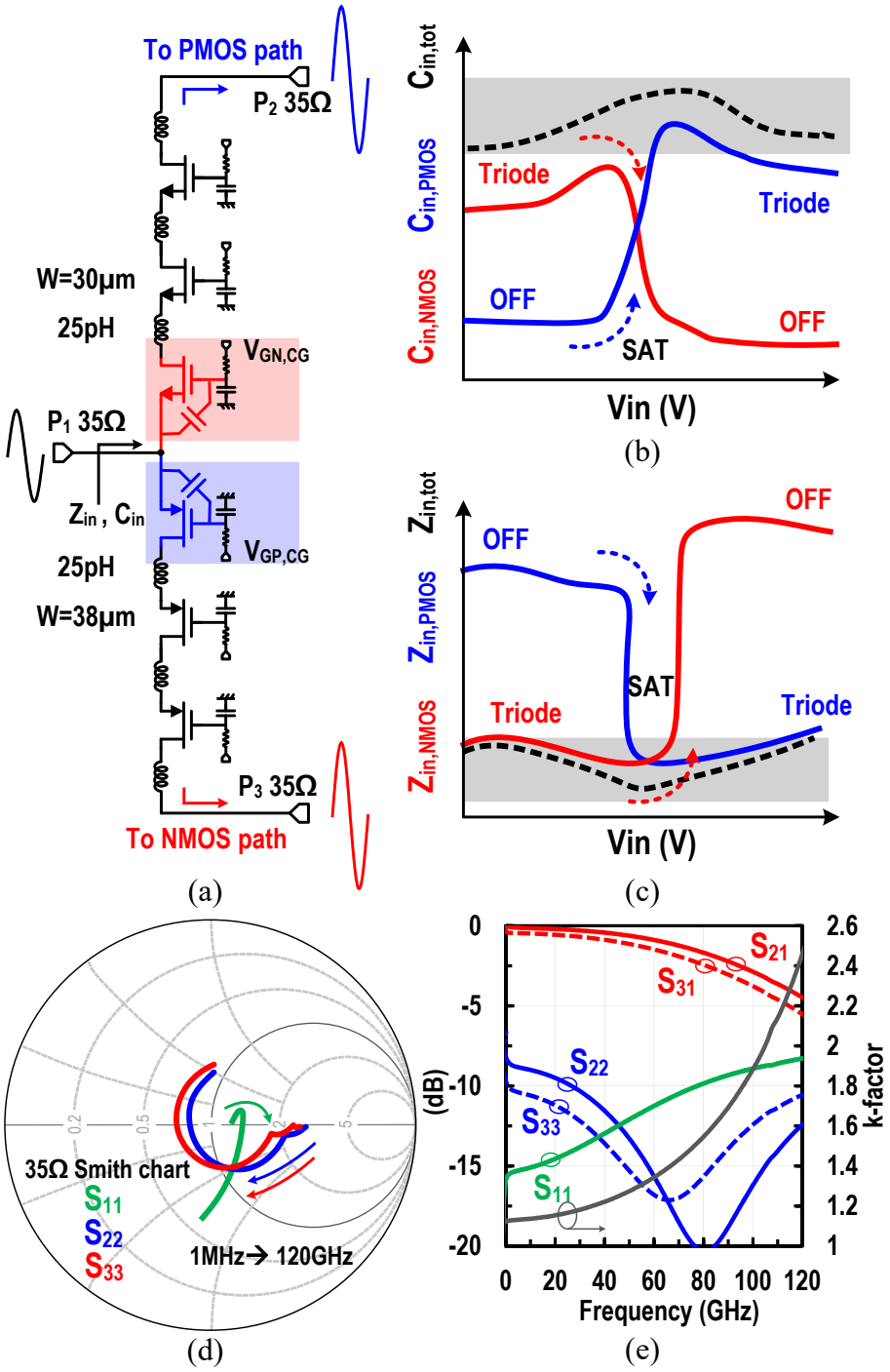


Figure 4.3: (a) Intermediate stage inverted-complementary driver/splitter. (b & c) Input capacitance and impedance variation across the input voltage swing. (d) Input and output impedance variation from 1 MHz to 120 GHz based on 35 Ω ports. (e) Simulated S-parameters and stability factor for the active splitter.

4.3.3 Output Complementary DPA

A push-pull output PA topology offers several benefits in terms of non-linearity compensation, current-reuse for efficiency, and operation as a linear driver from DC frequency without external bulky bias network. However, a concern can arise from using PMOS gain-cells targeting a 100 GHz operation due to the inferior holes mobility and f_T compared to NMOS. This is investigated for the 45nm RFSOI technology node to ensure that no limitation exists from the PMOS path on the GBW or broadband power generation.

4.3.3.1 NMOS versus PMOS PA Cells

The gap in RF and analog performance between the NMOS and PMOS is shrinking in deeply scaled CMOS nodes [62]. The strain engineering enables substantial mobility enhancement while the FET speeds, f_T, and f_{max} are becoming limited by the extrinsic device routing rather than the intrinsic parasitics. Furthermore, PMOS is favored in high-power design due to the reported higher breakdown voltage compared to NMOS in advanced technology nodes [19]. This is due to the less abrupt junctions and the lower rates of holes impact ionization compared to electrons. As a result, several stacked PMOS and complementary PAs have been successfully reported at millimeter waves frequencies with state-of-the-art performance [18, 63, 64].

A PMOS-only DPA is recently reported in [3] with 640 GHz GBW and a $P_{SAT} > 19$ dBm up-to 60 GHz using the same technology process. A comparison between NMOS and PMOS stacked gain cells revealed similar P_{SAT} values for equally sized devices with ≈ 1 dB less gain for the PMOS stack. In the proposed design, all transistors have double contacted gates with a 1 μm finger width (W_f) to minimize the gate resistance. A low gate resistance is important to minimize the loss of the input TL and for efficient inter-stack coupling. Further reduction of W_f increases the gate vertical resistance component and does not improve f_{max}. The peak f_T and f_{max} of a 38×1 μm NMOS (PMOS) device when referred to the lowest metal are 290 (240) GHz

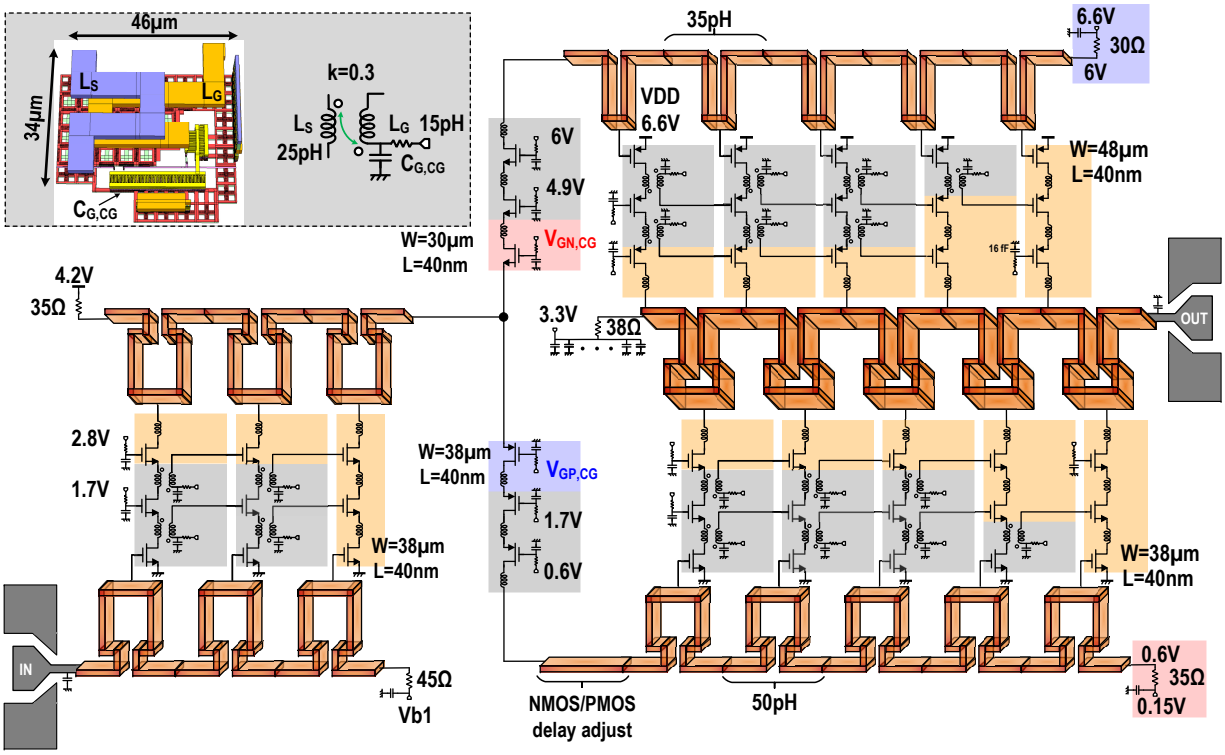


Figure 4.4: Schematic of the CMOS DPA.

and 250 (255) GHz, respectively. These numbers drop to 240 (198) GHz for f_T, and 200 (207) GHz for f_{max} after layout extraction to the top copper metal. Interestingly, f_T of the PMOS is $\approx$ 83% that of the NMOS predicting a 1.6 dB drop in G, while both devices have comparable f_{max}.

4.3.3.2 CMOS DPA Schematic

The output stage has 3-stack PMOS and NMOS DAs sharing the same supply (Fig. 4.4). In order to guarantee no DC power loss in the output termination in the nominal operation, the width of the lower common source (CS) NMOS and PMOS devices are 38 μm and 48 μm, respectively. The nominal operation is chosen to be a class-A mode for both output PAs in order to maximize f_{max}. The group delay of both input paths and output path are then designed to be comparable by sizing their respective TLs for broadband operation. Matching of group delays per section implies matching the LC product and results in lower loaded $Z_\circ$ for the PMOS path, as

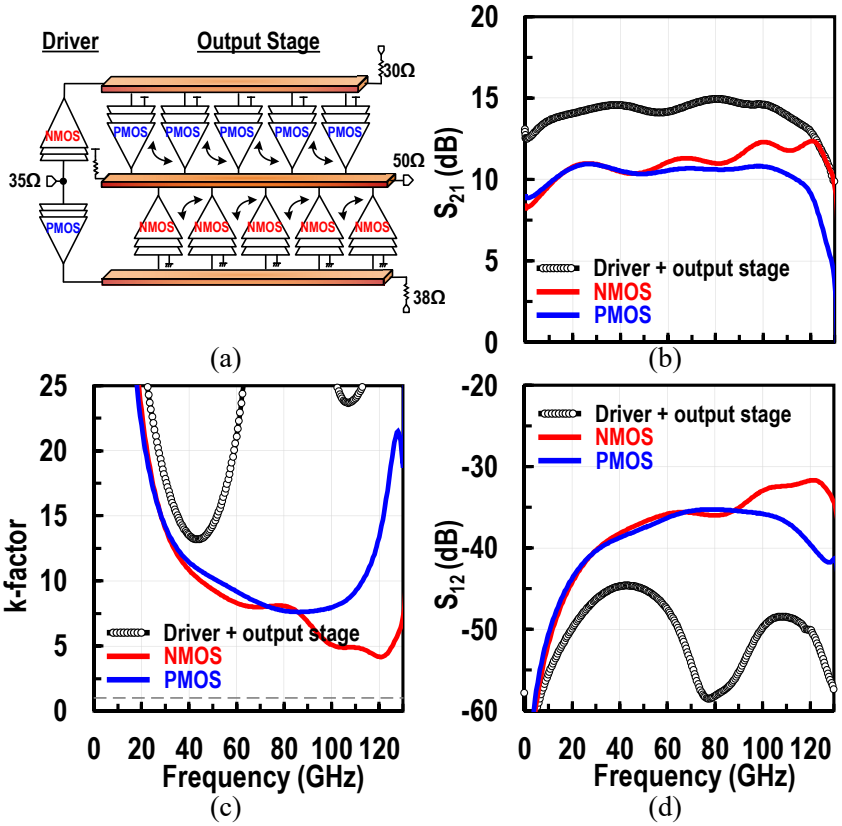


Figure 4.5: (a) Schematic of the driver and the output stage. (b) Simulated gain, (c) stability factor k, and (d) reverse isolation, for the three cases: output NMOS path, output PMOS path, and the overall driver and output stage.

predicted by (4.7), which reduces its input TL voltage swing and the path gain. The driver for the PMOS path can be biased to compensate for this effect by having a ≈15% higher Gm than the NMOS path pre-driver.

The output voltage swing builds up in a DPA structure towards the output stages and the upper devices in the stacks. Therefore, gate capacitors allowing for gate voltage swing are needed for the upper stacked devices while the rest of the devices (lower/input stages) can incorporate AC-grounded gates for higher gain. The scaling capacitors in all stages are designed to prohibit a peak-to-peak voltage swing > 2.5V between any two device terminals at P_{SAT}.

Unconditional stability of the DPA cannot be guaranteed by only checking k-factor for the whole design. This is because the internal nodes impedance values are subject to changes

with process and temperature. Therefore, unconditional stability for every stage in the DPA is mandatory for proper operation. The simulated gain, k-factor, and reverse isolation for each of the two output paths and the overall output stage are plotted in Fig. 4.5. The output stage combined with the driver achieve a 15 dB gain with nearly equal gain for both complementary paths (Fig. 4.5(b)). The simulated k-factor for both paths are > 1 with a minimum of 4.5 for the NMOS path (Fig. 4.5(c)). Splitting the output stage into two parallel DPAs, and having two separate drivers enhances the overall stability compared to individual paths due to the improved reverse isolation from the 3-stack driver (Fig. 4.5(d)).

It is desired to achieve over 20 dBm of P_{SAT} from the output stage given by:

$$P_{SAT} = \frac{(V_{DD}/2 - 3V_k)^2}{2R_{opt}}, \tag{4.11}$$

where V_{DD} is the supply voltage and V_k is the MOS knee voltage ≈ 0.1 V. For maximum P_{SAT}, R_{opt} is designed to be $\approx 40\ \Omega$ keeping the transformation ratio Q to $50\ \Omega \leq 1/2$. A 3-stack complementary topology is, thus, the minimum for a V_{DD} = 6.6 V. The overall width (W_{tot}) of the output devices is then determined to provide enough current to achieve the required output swing. The power is split equally between the NMOS and PMOS for $W_{tot} = M \times W_{N,u} \times (1+\zeta)$ with $W_{N,u}$ being the width of an NMOS unit-cell and M is the number of stages. The distance between the consecutive stages is determined to be $< 50\ \mu$m for proximity in order to apply the inter-stack coupling. For this distance the maximum input TL inductance per section (L_g) based on a single turn inductor is ≈ 50 pH. The capacitance per-stage is determined based on L_g value and according to (4.6). Knowing that k/ζ are 0.4/1.2 in the used process, the capacitance per section is determined to be 40 fF leading to 5 gain-stages with 3-stack topology.

4.4 Implementation

The full schematic of the multi-drive DPA is shown in Fig. 4.4. The input and output TLs are shaped as single-turn inductor sections to improve the inductance per unit length and ensure stages proximity which is mandatory for multi-drive inter-stack coupling. Since the PMOS stacks are connected half an inductor earlier than the NMOS ones, a delay adjust TL is placed before the output NMOS DA to guarantee in phase summation for both output complementary DPAs. The output TL is designed to have a loaded $Z_\circ \approx 38\ \Omega$ to maximize P_{out}, while the output RF pad capacitance ($\approx$ 13 fF) is exploited to form a small step-up impedance network to 50 Ω.

The multi-drive CMOS DPA is implemented in 45nm RFSOI technology node with a core area of 0.312 mm^2 (Fig. 4.6). Thin-oxide floating-body partially depleted FETs are used for all NMOS and PMOS with 40 nm in channel length. All TLs are implemented on the upper two copper layers (1.2 μm each) with no ground-plane underneath and using a trap-rich high resistivity substrate (ρ=2.5 kΩ.cm) in order to maximize their unloaded $Z_\circ$ and minimize the resistive losses. The upper two copper layers are tied together for the output TL to improve the current handling and further reduce the resistive loss at the expense of some reduction in $Z_\circ$. The inter-stack coupling transformers are designed as broadside coupled single turn windings with a patterned ground plane underneath. The ground plane eases the prediction of the current return path by the EM-solver, and thus the value of the coupling coefficient (k=0.35 at 50 GHz). All EM-structures are simulated using Integrand EMX electromagnetic wave solver. RC lowpass filters are placed between the bias nodes to impede any common-mode instability due to routing. The lower two metals are used to form a ground mesh that extends in the whole chip to minimize ground inductance. The supply and biasing nodes are decoupled using a combination of stacked MOS and degenerated vertical natural capacitors. The chip consumes 890 mW with 660 mW for the output complementary stage when biased in Class-A (20 mA per transistor) and 230 mW for the input pre-driver and active power splitter. The input pre-driver is biased in a Class-AB mode

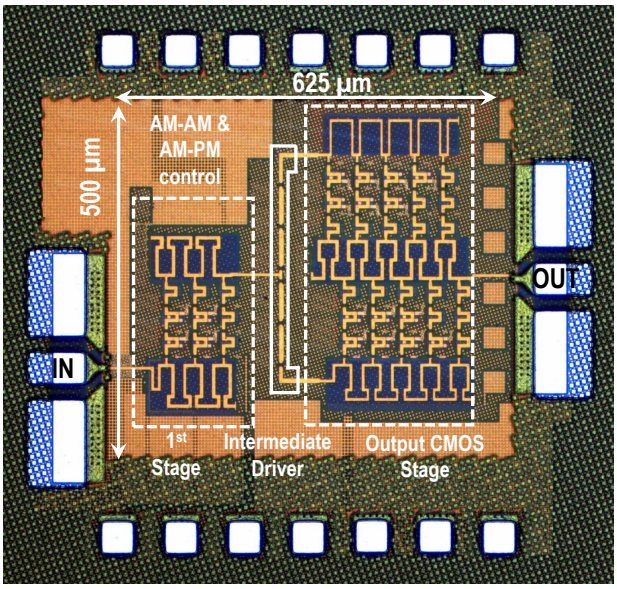


Figure 4.6: Die micrograph of the fabricated CMOS distributed amplifier chip in 45nm RFSOI.

with 11 mA per transistor, while the NMOS and PMOS stacks for the power splitter consume 20 mA and 13 mA, respectively, in the default state.

4.5 Continuous-wave Measurements

Continuous-wave (CW) measurements are conducted using three separate setups to cover the frequency range from DC-to-120 GHz. In all measurements, the DPA is RF probed and the pads loss are not de-embedded since they constitute a part of the matching networks at both ports. A vector network analyzer (Keysight N5247A PNA-X) is used for frequencies < 70 GHz. A millimeter-wave head controller (Keysight N5260A) and two sets of VDI frequency extension modules and waveguide-based WR-10 probes are used to cover the range from 75-to-110 GHz. Frequencies > 110 GHz are measured using another set of OML frequency extenders combined with WR-6 probes.

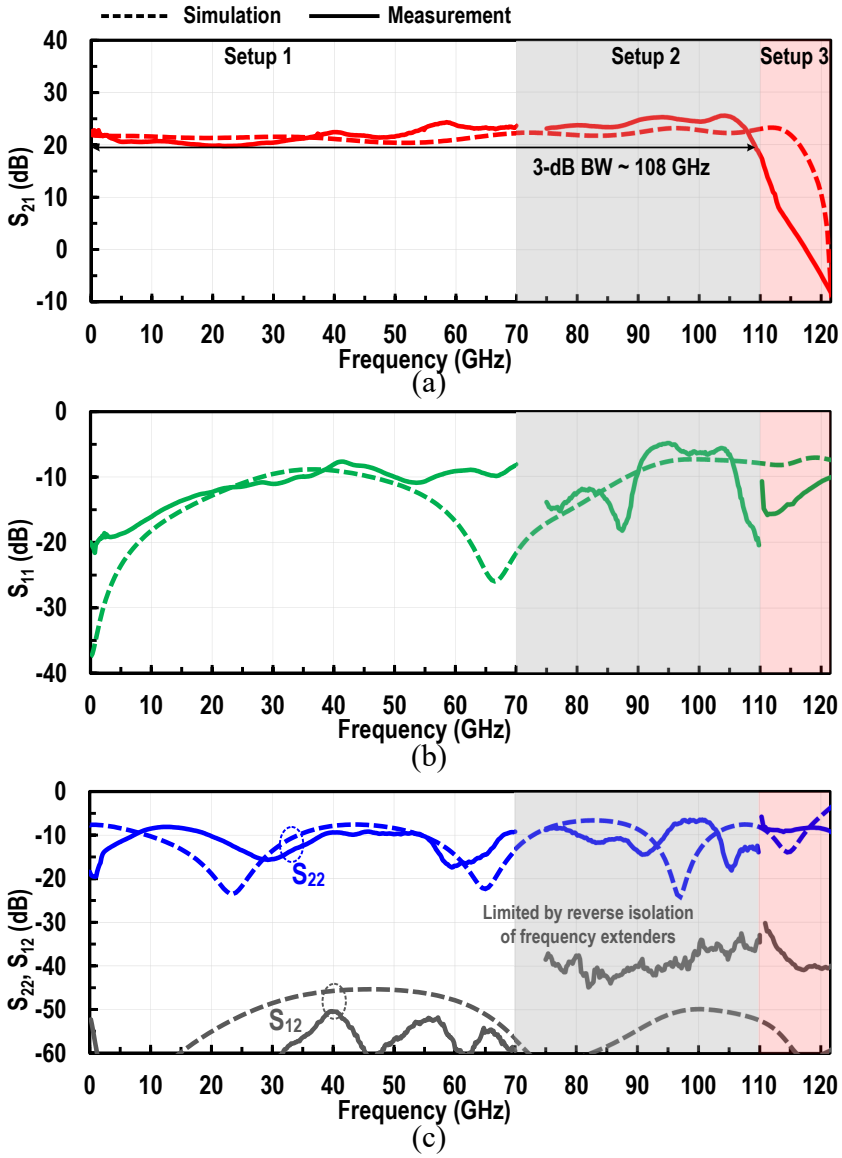


Figure 4.7: Measured and simulated S-parameters versus frequency.

4.5.1 Small-Signal Performance

The simulated and measured CMOS DPA S-parameters are plotted in Fig. 4.7. The DPA achieves 23 dB gain and 108 GHz 3-dB BW, and the measured GBW (1525 GHz) is the highest among reported silicon-based DAs (Fig. 4.7(a)). The in-band ripple is $< \pm$ 3 dB and has a good agreement with simulation. The achieved BW is a little lower than the simulated value

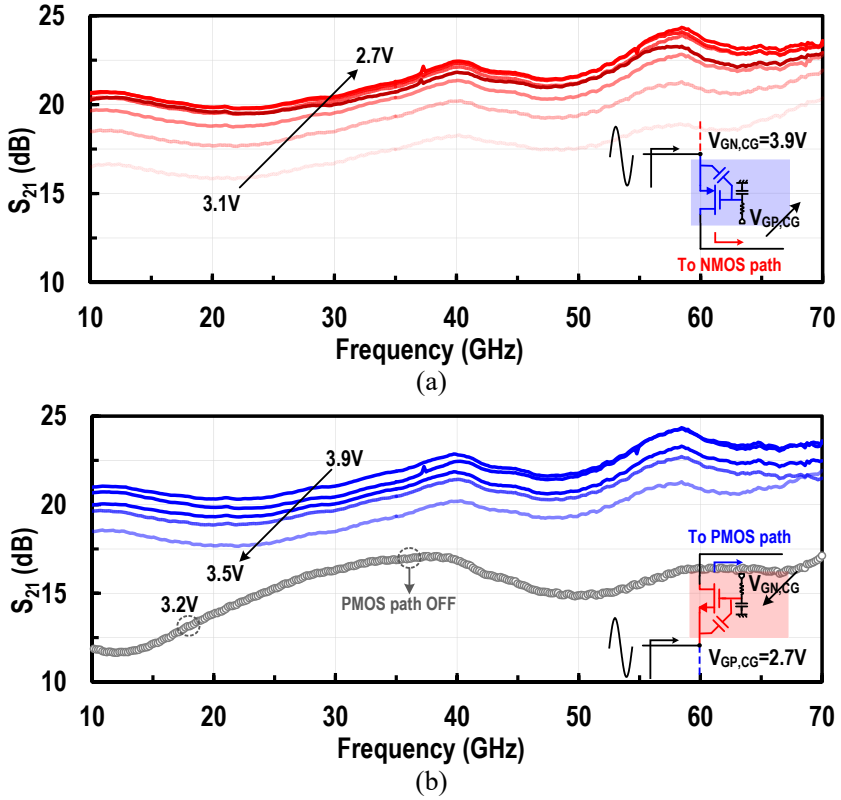


Figure 4.8: Measured S_{21} when varying the driver biasing: (a) $V_{GP,CG}$ for NMOS path, and (b) $V_{GN,CG}$ for PMOS path.

of 116 GHz. This is attributed to slightly underestimated multi-drive transformers values and k. Larger multi-drive transformers and/or k result in a higher compensation of the input TL and intra-stack losses occurring at a lower frequency. This can be observed from the S_{21} response slightly peaking towards the higher frequency end compared to simulation then sharply falling around 108 GHz. An underestimated capacitance cannot cause this S_{21} peaking while reducing the BW. The amplifier maintains input and output matching across the frequency spectrum with values $<$ -9 dB up-to-90 GHz, while sub-GHz matching can be observed at both ports (S_{11} and S_{22} $<$ -20 dB) which is essential for wireline applications (Fig. 4.7(b & c)). Th reverse isolation (S_{12}) is $<$ -40 dB up to 70 GHz, while the isolation over 70 GHz is limited by the frequency extenders.

The effect of the driver biasing on the measured gain is separately studied in Fig. 4.8.

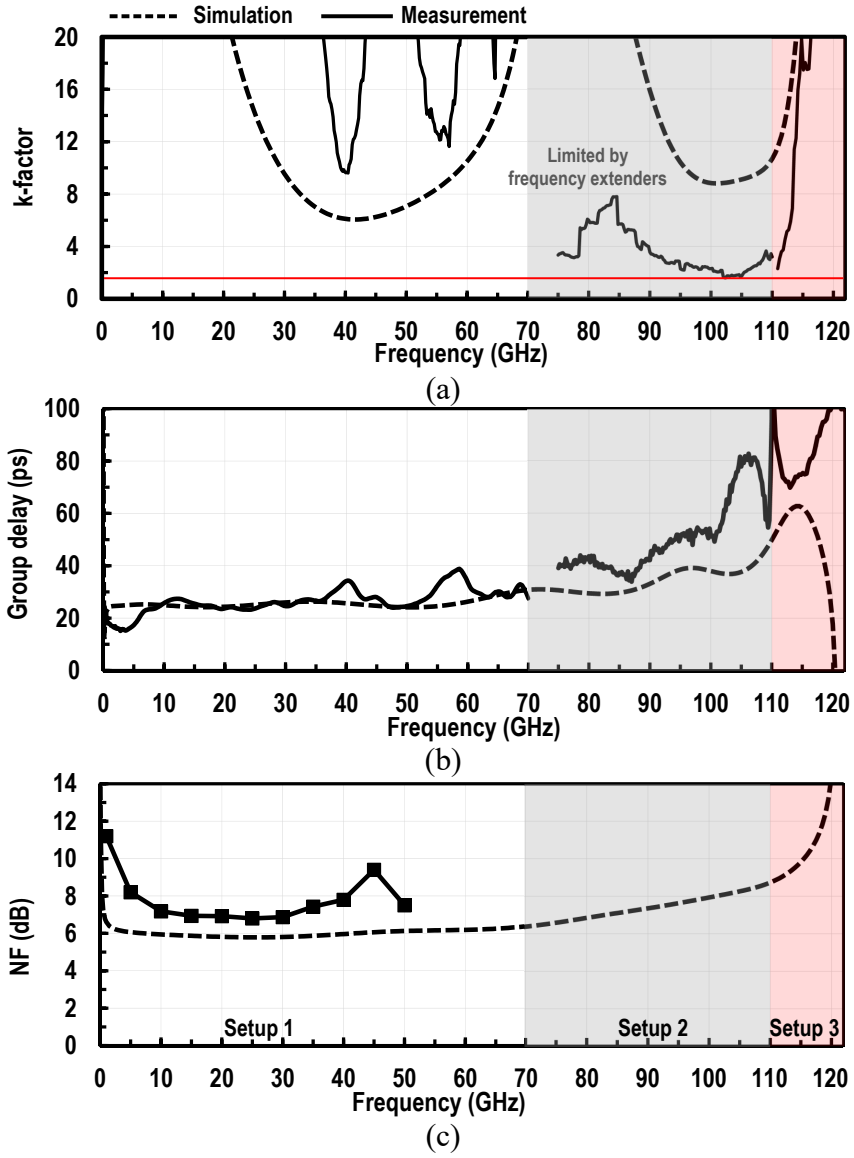


Figure 4.9: Measured and simulated (a) stability factor, (b) group delay, and (c) noise-figure, versus frequency.

Both $V_{GN,CG}$ and $V_{GP,CG}$ can be tweaked to change the biasing class of the output PA stage for their respective paths, and therefore control the gain. In the extreme case where $V_{GN,CG}$ ($V_{GP,CG}$) is too high (low), one of the output stage PAs turns-off. As a result, a large DC current flows in the output termination, thus limiting the headroom for the ON output PA, which reduces the gain and degrades the output matching.

The measured and simulated k-factor, group-delay, and noise figure (NF), are shown in

Fig. 4.9. The amplifier is unconditionally stable, and the dip in the k-factor for frequencies > 75 GHz is due to limited isolation when using frequency extenders, which was previously observed in the measured S_{12}. The k-factor remains better than 1.7 including the VNA extenders non-ideality. The group delay is within $\pm$ 15 ps up 90 GHz (limited by the VNA calibration errors). The group delay variation quickly increases for frequencies > 90 GHz, when the multi-drive inter-stack coupling is effective. This is because the phase of the main signal through the input TL is linear with frequency while the phase of the coupled signal is not linear. The group delay variation can degrade broadband data transmission in this frequency range and proper equalization is needed. The NF is measured up-to 50 GHz using the PNA-X with a minimum of 6.9 dB at 30 GHz. The relatively high NF is predicted by design since the input stage and power splitter only contribute 6-7 dB of gain to allow for a higher overall efficiency as discussed in section II , which compromises the NF a bit. While the main focus of the design is power amplification rather than noise, it is important to note that the NF of the multi-drive inter-stack coupling topology is similar to the series peaked stack up-to 60 GHz and follows the analysis provided by [38]. For higher frequencies, the forward gain BW is extended for the multi-drive coupling case leading a lower NF compared to the series peaking design.

4.5.2 CW Large-Signal Performance

The DPA large-signal performance is measured from DC-up-to 70 GHz. The same PNA-X is used for large signal measurements. A power meter (KS N1912A) connected to a power sensor (KS N8488A) are used to calibrate the absolute power levels. A power sweep is first conducted at 40 GHz to assess the effect of the driver biasing which can act as analog pre-distortion knobs (Fig. 4.10). It is noted that the driver biasing can modulate the AM-PM non-linearity when going into compression while the P_{SAT} remarkably remains within 1 dB in all biasing conditions (Fig. 4.10(a)). The biasing steps are 100 mV showing moderate sensitivity to the bias voltage. Therefore, a DAC can easily be implemented to control the biasing knobs. Similarly, the bias

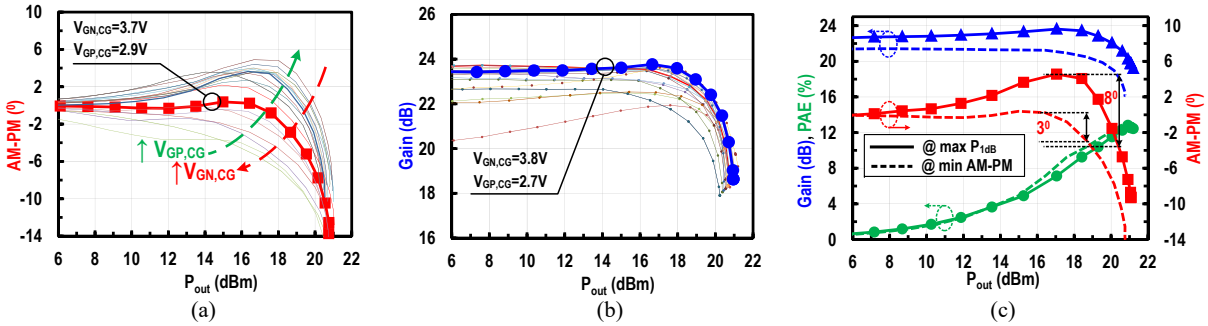


Figure 4.10: Measured CW large-signal performance versus power at 40 GHz: (a) AM-PM non linearity, and (b) AM-AM non linearity. (c) Gain, AM-PM and PAE for two different settings: maximum P_{1dB} and minimum AM-PM.

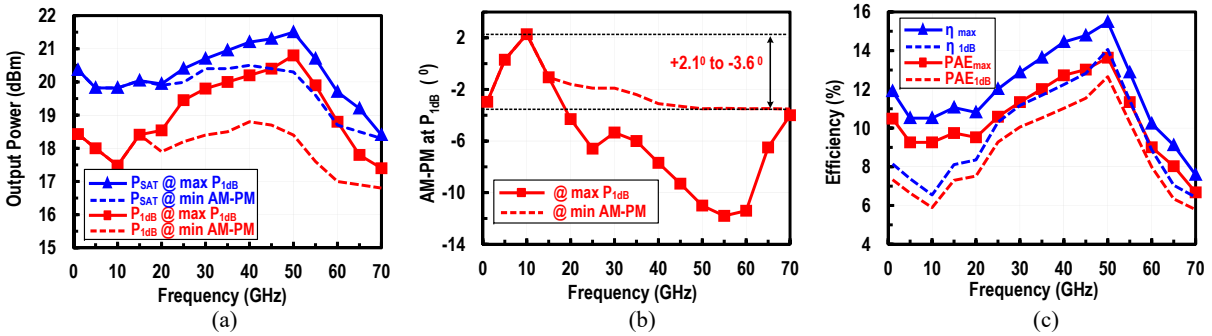


Figure 4.11: Measured CW large-signal performance versus frequency for two different settings: maximum P_{1dB} and minimum AM-PM. (a) P_{SAT} and P_{1dB} (b) AM-PM non linearity at P_{1dB}. (c) Drain efficiencies η_{1dB}, η_{max}, PAE_{1dB}, and PAE_{max}.

point can be optimized to minimize the AM-AM non-linearity, and thus class of operation of the two output complementary DPAs (Fig. 4.10(b)). Consequently, two modes of operation are achieved: (a) minimum AM-PM non-linearity, and (b) maximum P_{1dB}, with fine control in between. Fig. 4.10(c) summarizes the measured performance of both modes versus power at 40 GHz. The maximum P_{1dB} mode extends the linear range by 1.4 dB (from 18.8 to 20.2 dBm). The minimum AM-PM mode limits the AM-PM value at P_{1dB} to $< 3°$ instead of $8°$ in the other mode.

The performance of both modes measured across the frequency spectrum is shown in Fig. 4.11. In both modes, the P_{SAT} and P_{1dB} remain better than 18.4 dBm and 16.9 dBm, respectively, up-to-70 GHz (Fig. 4.11(a)). For the max P_{1dB} mode, the P_{SAT} and P_{1dB} are within

Table 4.1: Continous-wave performance comparison with wideband millimeter-wave and distributed power amplifiers

Design	This work	[66] Vigilante JSSC'18	[67] Chappidi JSSC'18	[3] El-Aassar SSCL'19	[13] Testa JSSC'15	[16] Fang JSSC'16	[27] Jahanian TMTT'12	[17] Fang TMTT'19	[15] Chen TMTT'11
Technology process	45nm RFSOI	28nm CMOS	130nm SiGe	45nm RFSOI	130nm SiGe	90nm SiGe	65nm CMOS	45nm RFSOI	130nm SiGe
f_T/f_{max} (GHz)	290/250 (NMOS) 240/255 (PMOS)	300	220/280	240/255 (PMOS)	300/500	300	160/200	290/250	200
Topology	Dist.	Lumped	Lumped	Dist.	Dist.	Dist.	Dist.	Dist.	Dist.
Frequency (GHz)	DC-108	29-57	30-55	1.5-103	DC-170	14-105	DC-65	10-82	DC-110
Supply (V)	5 (Pre-driver) / 6.6 (PA)	0.9	4, 1.6	5	3.6	4, 3.6, 3.2, 2.7	1.3	1.5-2.4	3
Gain (dB)	23	20.8	23.4	16	10	12	22	13	10
GBW (GHz)	**1525**	307	370	640	537	362	818	322	348
&P_{1dB} (dBm)	**19.5 @ 25 GHz** **20.8 @ 50 GHz** **17.5 @ 70 GHz**	13.4 @ 30 GHz 11.1 @ 40 GHz 10.9 @ 50 GHz	N.R.	19.0 @ 20 GHz 18.5 @ 40 GHz 17.5 @ 60 GHz	7.5⋆ @ 50 GHz	14.9 @ 5 GHz	10 @ 2 GHz	13 @ 50 GHz	16.7 @ 40 GHz
&P_{SAT} (dBm)	**20.5 @ 25 GHz** **21.5 @ 50 GHz** **18.4 @ 70 GHz**	16.6 @ 30 GHz 15.9 @ 40 GHz 15.1 @ 50 GHz	23.7 @ 40 GHz	21.7 @ 20 GHz 21.0 @ 40 GHz 19.0 @ 60 GHz	9.4⋆ @ 50 GHz	17 @ 50 GHz	12⋆ @ 2 GHz	17.2 @ 50 GHz	17.5 @ 40 GHz
PAE_{max} (%)	10.8 @ 25 GHz 13.4 @ 50 GHz 6.8 @ 70 GHz	24.2 @ 30 GHz 18.4 @ 40 GHz 14.9 @ 50 GHz	24.7⋆ @ 30 GHz 28.5 @ 40 GHz 23.4⋆ @ 50 GHz	18.4 @ 20 GHz 15.7 @ 40 GHz 10.0 @ 60 GHz	N.R.	12.6 @ 50 GHz	N.R.	17.1 @ 50 GHz	13.2 @ 60 GHz
PAE_{P1dB} (%)	9.1 @ 25 GHz 12.5 @ 50 GHz 5.9 @ 70 GHz	12.6 @ 30 GHz 7.5 @ 40 GHz 7.0 @ 50 GHz	N.R.	12.0 @ 20 GHz 10.7 @ 40 GHz 8.4 @ 60 GHz	N.R.	8.5⋆ @ 50 GHz	N.R.	10⋆ @ 50 GHz	11.5 @ 60 GHz
&AM-PM @P_{1dB} (°)	+2.1 to -3.6 from DC to 70 GHz	0.45 @ 50 GHz	N.R.	-5 @ 40 GHz	N.R.	N.R.	N.R.	7.5⋆ @ 50 GHz	N.R.
Core Area (mm^2)	**0.31**	0.14	0.96	0.33	0.38	1.51	0.93	0.8	2.18^

N.R. = Not Reported ^ Including pads
⋆ Estimated from plots & Best setting at each frequency

1.2 dB from 25 to 70 GHz. The P_{SAT} 3-dB BW is $\approx$ 70 GHz for this mode while it is $>$ 70 GHz for the minimum AM-PM mode. The AM-PM conversion at P_{1dB} is improved to +2.1Âř/-3.6Âř at DC to 70GHz, compared to +2.1Âř/-11.9Âř for the maximum P_{1dB} setting (Fig. 4.11(b)). The power gain is reduced by $\approx$ 1.9 dB while the PAE remains unchanged (Fig. 4.11(c)). Peak performance is obtained around 50 GHz with P_{SAT}, P_{1dB}, and peak PAE of 21.5 dBm, 20.8 dBm, and 13.4%, respectively, for the maximum P_{1dB} mode (Fig. 4.11(a & c)).

4.5.3 CW Performance Comparison

The CW performance of the multi-drive CMOS DPA is compared with state-of-the-art published silicon-based distributed amplifiers [3, 13, 15–17, 27, 65] and wideband millimeter-

waves PAs [66, 67] in Table 4.1. The DPA reports the highest GBW for published silicon-based DAs (1.525 THz) and one of the highest P_{1dB} and P_{SAT} up-to-70 GHz. The PAE at P_{1dB} is also the highest among DAs at 50 GHz, in a chip area comparable in size to lumped PAs. The reason behind the improvement compared to published DPAs is the multi-drive inter-stack coupling which provides a simultaneous optimization of BW, output power and area. These parameters are typically trading-off in conventional designs.

4.6 Time Domain measurements

Since the proposed design can operate from true-DC frequency with a BW over 100 GHz, the DPA can be used as a wideband millimeter-wave PA or a linear driver in optical wireline systems. In this section, time domain measurements are conducted for both complex modulated data and serial data followed by a comparison with the state-of-the-art.

4.6.1 Complex Modulated Data Measurements

Fig. 4.12 presents the measurement setup for real-time complex modulated data. An arbitrary waveform generator (Keysight M8185A AWG), is used as the source of QAM signals followed by an attenuator and up-converting passive mixer. The up-converted signal is fed to an amplifier and variable attenuator to control the power level at the input of the probed DUT. The DPA output is attached to a DC-to-63 GHz real-time scope (Keysight DSO-Z632A) loaded with the Keysight 89601 Vector Signal Analyzer (VSA) software. The scope captures the output signal, extracts the data spectrum and constellations, and measures the EVM. The output power is measured through a 20 dB coupler connected to a power sensor followed by a power meter with a dedicated calibration for each carrier frequency. The input signal power to the DUT is only controlled by the preceding variable attenuator and not the AWG. This is essential to fix signal-to-noise-ratio (SNR) out of the AWG. In all measurements, a linear equalization is

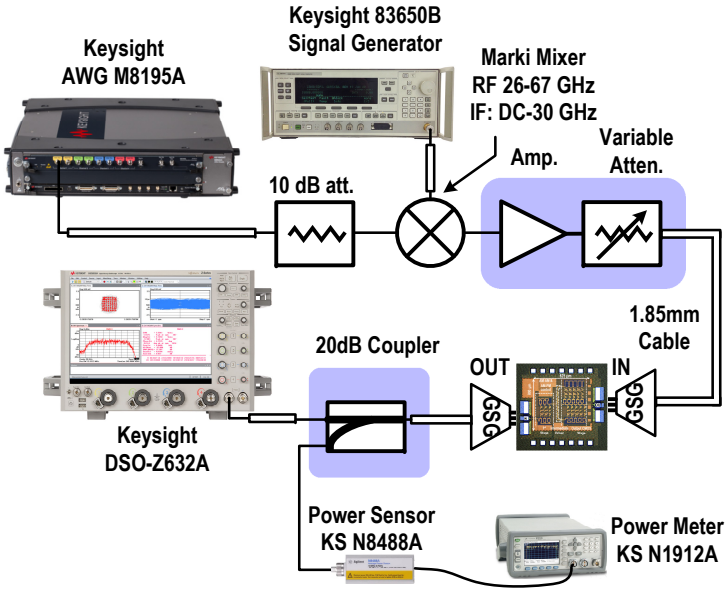
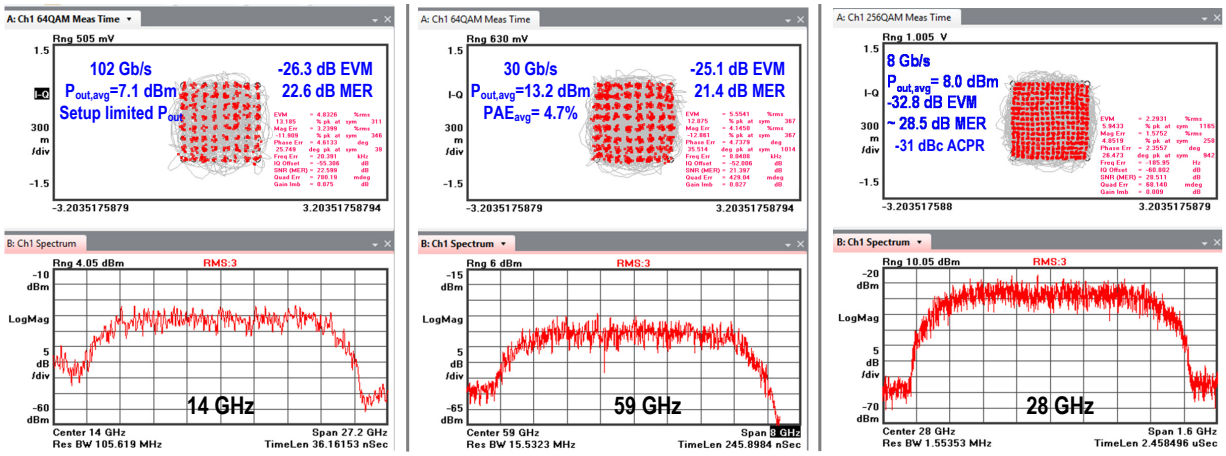


Figure 4.12: Measurement setup for the EVM measurements.

performed by the real-time scope but no pre-distortion is applied. The equalization is essential in order to correct for the setup linear frequency response to be able to detect large baud-rates. However it cannot remove non-linear errors such as harmonic distortion and spectral-regrowth. In order to cover carrier frequencies up-to-59 GHz, the frequency spectrum is divided into 5 setups and for each setup, the amplifier, variable attenuator and output coupler are changed while the rest of the setup remains fixed. The biasing values $V_{GN,CG}$ and $V_{GP,CG}$ are obtained from the CW-large signal measurements to maximize P_{1dB}. The values are set based on the carrier frequency and no further changes in the bias points are done in all EVM measurements when changing the power level, baud-rate, or modulation type.

The DPA is first tested with 64-QAM signals and data rates up-to 102 Gb/s (17 GBaud/s) are achieved at 14 GHz with an EVM_{rms} $<$ -26 dB with an average output power $P_{out,avg}$=7.1 dBm limited by the test setup (Fig. 4.13(a)). Next, bit rates up-to 30 Gb/s (5 GBaud/s) are applied and the carrier frequency is swept up-to-59 GHz. The maximum baud-rate is limited by the BW of the different setups. For all frequencies, $P_{out,avg}$ is recorded for an EVM_{rms} $<$ -25 dB. The CMOS DPA achieves a state-of-the-art 13.2 dBm $P_{out,avg}$ with 30 Gb/s 64-QAM signals at 59



(a) (b) (c)

Figure 4.13: (a) Measured EVM, data spectrum and average P_{OUT} for: (a) 64-QAM constellation with 102 Gb/s for a 14 GHz carrier frequency. (b) 64-QAM constellation with 30 Gb/s for a 59 GHz carrier frequency. (c) 256-QAM constellation with 8 Gb/s for a 28 GHz carrier frequency.

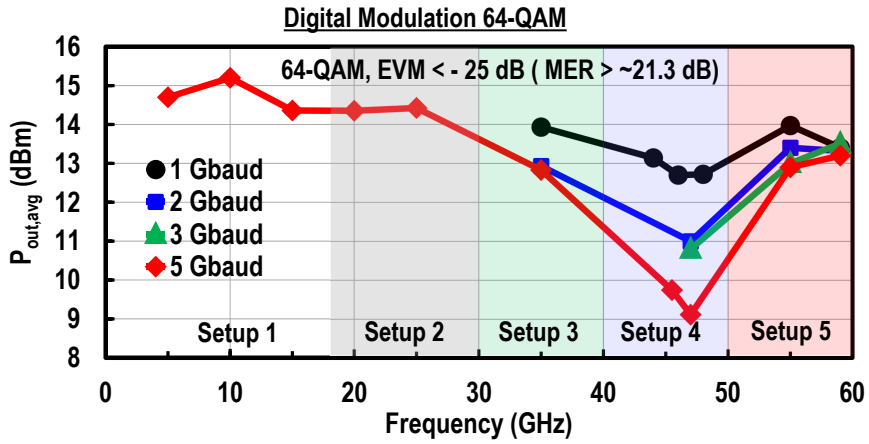


Figure 4.14: Measured average P_{OUT} for 64-QAM constellations and an EVM_{rms} < -25 dB with different carrier frequencies up-to-59 GHz.

GHz (Fig. 4.13(b)). The DPA maintains a $P_{out,avg} > 13$ dBm for 30 Gb/s across frequency except a dip in setup 4, between 40 and 50 GHz (Fig. 4.14). This dip is mostly limited by the setup BW since it improves as the baud-rate is reduced.

In order to further show the linearity of the CMOS DPA, 256-QAM signals are applied for a higher peak to average power ratio (Fig. 4.13(c)). A data rate of 8 Gb/s is recorded at 28 GHz for $P_{out,avg}$=8 dBm while the EVM_{rms} is < -32 dB. The DPA is also tested with 16-QAM

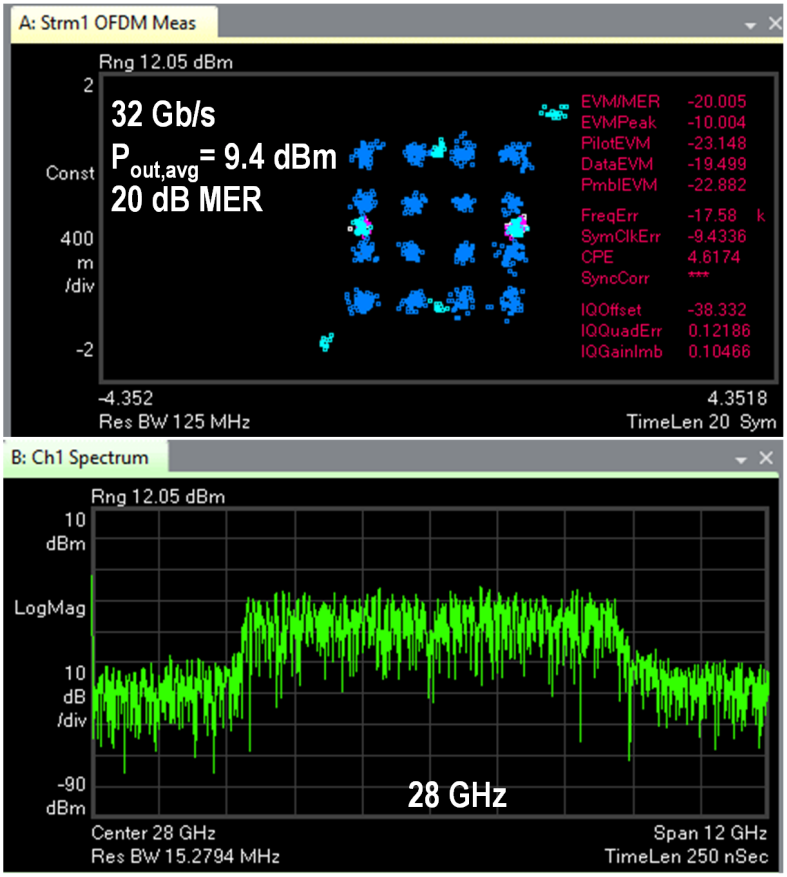


Figure 4.15: Measured EVM, spectrum and average P_{OUT} for a 32Gb/s 16-QAM OFDM constellation using a 28 GHz center frequency for sub-carriers.

OFDM signals at 28 GHz with 16 sub-carriers. The PA achieves 9.4 dBm $P_{out,avg}$ with 20 dB modulation error ratio (MER) for data rates up-to-32 Gb/s (Fig. 4.15).

Table 4.2 compares the complex modulated data performance with existing wide-band PAs [17, 66–71]. The CMOS DPA records the highest data rates in all types of QAM modulations up-to-59 GHz. The measured $P_{out,avg}$ are the highest compared to reported DAs and among the highest overall.

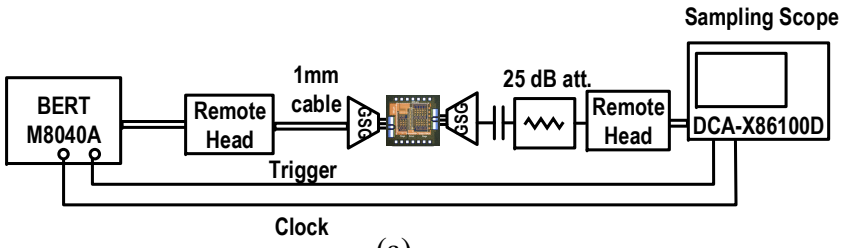
4.6.2 Serial Data Measurements

The eye diagram measurements setup is shown in Fig. 4.16. A bit-error-rate-tester (Keysight BERT M8040A) is used as the source of PRBS9 NRZ and PAM-4 signals, which are

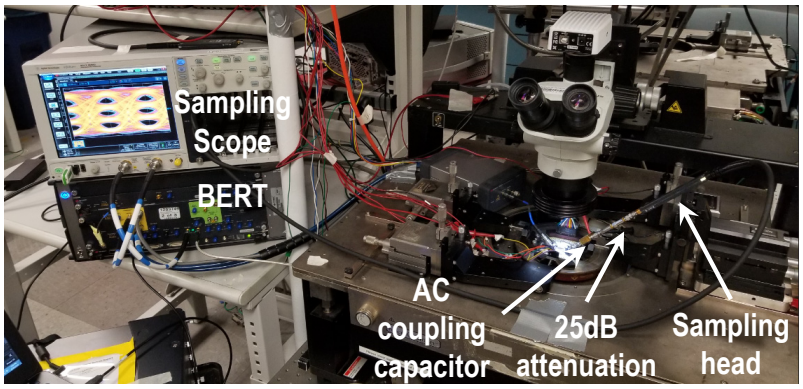
Table 4.2: Complex modulated data performance comparison with wideband millimeter-wave and distributed power amplifiers

Design	This work					[66] Vigilante JSSC'18	[68] Hu ISSCC'17	[67] Chappidi JSSC'18	[69] TW. Li ISSCC'18	[17] Fang TMTT'19	[70] Nguyen ISSCC'19	[71] Wang ISSCC'19
Technology process	45nm RFSOI					28nm CMOS	130nm SiGe	130nm SiGe	130nm SiGe	45nm RFSOI	45nm RFSOI	45nm RFSOI
Frequency (GHz)	14	25	59	28		34	39	50	28.5	47.5	60	28
Modulation	64-QAM			256-QAM	16-QAM OFDM	64-QAM	64-QAM	16-QAM	64-QAM	16-QAM	64-QAM	64-QAM
Bit-rate (Gb/s)	**102**	**30**	**30**	**8**	**32**	6	3	4	18	20	12	15
#EVM (dB)	<-25			<-32	<-20	-28.7	-28.7	-21.75	-25	<-25	-27.1	-24
Pout (dBm)	+7.1	+14.3	+13.3	+8	+9.4	+5.9	+9.3	+16.9	+9.8	11.8*	20.9	15
PAE (%)	2.6	5	4.7	1.7	2.0	2.3	17.2 (CE)	12.6*	18.4	7.5*	3.4	26.4

* Estimated from plots # Normalized to the peak of the constellation



(a)



(b)

Figure 4.16: (a) Measurement setup for the serial-data measurements. (b) Setup photograph.

fed to the probed DUT through the input sampling head and a 1mm cable. The chip output is AC coupled and attenuated by 25 dB to avoid damaging of the sampling head at the output, before going into a sampling scope (DCA-X, infiniium 86100D) to measure the eye diagrams. The bias point for the pre-driver is chosen to maximize the P_{1dB}. Data rates up to 56 GBaud/s in both NRZ and PAM-4 are tested and the de-embedded single-ended peak-to-peak voltage, $V_{ptp,se}$ is

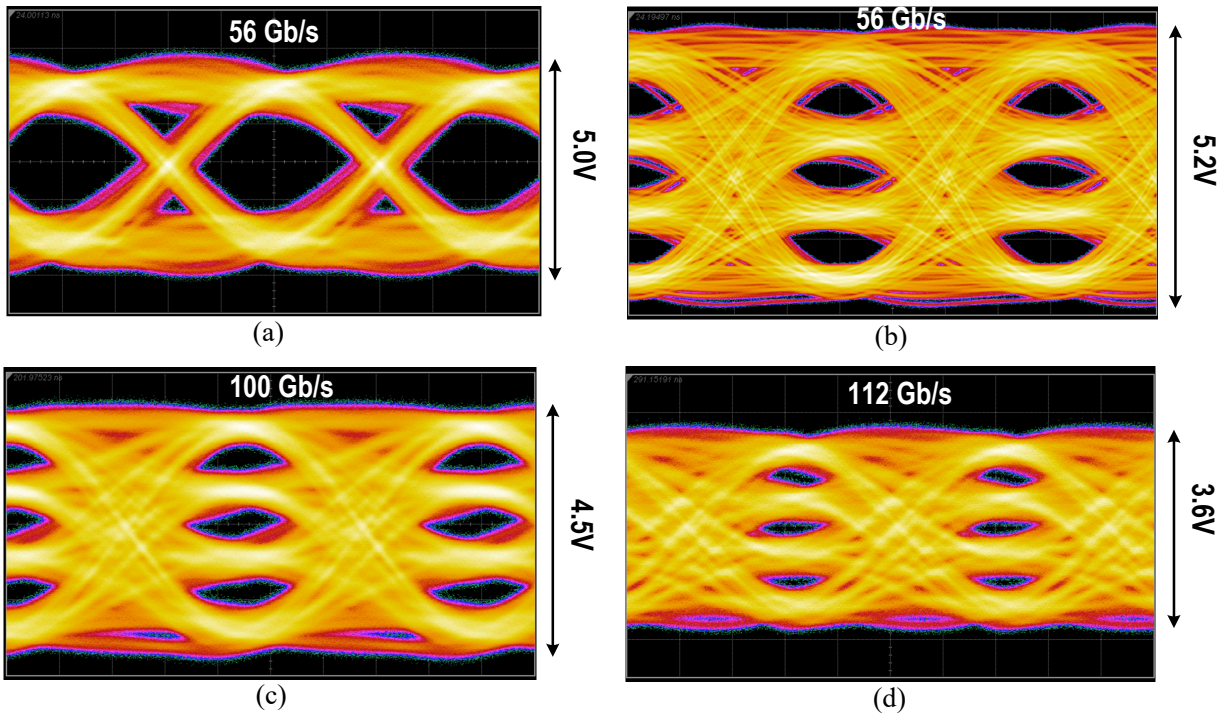


Figure 4.17: Measured PRBS9 (a) NRZ and (b,c & d) PAM-4 eye diagrams and output amplitudes for 56 Gb/s up-to-112 Gb/s data rates.

recorded. The maximum baud-rate is limited by the ENOB of the BERT. The CMOS driver achieves a state-of-the-art 5 $V_{ptp,se}$ for 56 Gb/s NRZ. For PAM-4 signals, the achieved $V_{ptp,se}$ values are 5.2V, 4.5V and 3.6V, for 56 Gb/s, 100 Gb/s, and 112 Gb/s, respectively. The reduction of the output amplitude from 4.5V to 3.6V for the 100 Gb/s to 112 Gb/s case is mostly due to the limited input power provided by the BERT and not the DPA.

The performance of the CMOS DPA as a linear driver is compared with state-of-the-art designs [45, 46, 48, 72–74] in Table 4.3. The multi-drive DPA achieves the highest reported single-ended V_{ptp} for all data rates up to 112 Gb/s. Since the output voltage/power requirements for linear drivers is different based on the standard and applications, it is beneficial to benchmark designs based on a *FoM* defined as the efficiency per bit rate per output voltage swing. The output CMOS DA has a state-of-the art *FoM* of 1.47 to 1.62 pJ/bit/V for 100 and 112 Gb/s PAM-4. The *FoM* is only outperformed by [45] which has a lumped design with nearly half the CMOS DPA

Table 4.3: Comparison with wideband and distributed linear drivers

Design	**This work**			**[45] Zandieh TMTT'17**	**[46] Baker RFIC'17**	**[72] Rito IMS'17**	**[48] Rito TMTT'16**	**[73] Menolfi ISSCC'18**	**[74] Kim ISSCC'18**
Technology process	45nm RFSOI			55nm SiGe BiCMOS	55nm SiGe BiCMOS	130nm SiGe:C	0.25µm SiGe:C	14nm FinFET	10nm FinFET
Topology	Distributed **Single-ended**			Lumped Differential	Distributed Differential	Distributed Differential	Lumped Differential	Lumped Differential	Lumped Differential
Bandwidth (GHz)	108			57.5	>70	90	52	N.R.	40
P_{DC} (mW)	890/660*			820/600*	1100	550	1500	229	193
Modulation type	PAM-4			PAM-8	PAM-8	PAM-4	PAM-4	PAM-4	PAM-4
Data Rate (Gb/s)	56	100	112	168	168	60	50	112	112
Output swing (Vptp)	**5.2**	**4.5**	**3.6**	3.8	3	3	4	0.5	0.75
Efficiency (pJ/bit)	15.6 / 11.8*	8.86 / 6.6*	7.9 / 5.83*	4.88 / 3.57*	6.54	9.17	30	2.04	1.72
FoM (pJ/bit/V)	3 / 2.26*	1.97 / 1.47*	2.2 / 1.62*	1.28 / 0.94*	2.18	3.06	7.5	4.08	2.29

* Not including pre-driver

BW (57.5 GHz) and uses PAM-8 signals.

4.7 Conclusion

This chapter presented a CMOS-SOI DPA based on stacked-FETs gain cells. A multi-drive inter-stack coupling technique is proposed and applied between consecutive gain cells to break the trade-off between gain, BW, P_{out}, and chip area in conventional DA designs. An intermediate inverted complementary active splitter is also proposed to synthesize an active real impedance across power levels and frequency spectrum from DC. Complementary intermediate and output stages are designed and exploited to compensate for both AM-AM and AM-PM non-linearities. State-of-the-art performance is achieved for Si-based DPAs in both CW and modulated data measurements. The CMOS DPA has the highest reported GBW and the smallest chip area for DPAs with comparable power levels while allowing a true-DC operation without needing bulky external bias-tees. The DPA also records the highest 64-QAM data rates up to 59 GHz and the highest reported PAM-4 single-ended voltage swing, when operated as a linear driver.

4.8 Acknowledgment

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Chapter 4 is mostly a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "A DC-to-108-GHz CMOS SOI Distributed Power Amplifier and Modulator Driver Leveraging Multi-Drive Complementary Stacked Cells," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3437-3451, Dec 2019. The dissertation author was the primary investigator and primary author of this paper.

Chapter 4 is also, in part, a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "4.7 A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P1dB, and Over 100Gb/s in 64-QAM and PAM-4 Modulation," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb 2019, pp. 86-88. The dissertation author was the primary investigator and primary author of this paper.

Chapter 5

Cascaded Multi-Drive Stacked-SOI Distributed Power Amplifier with 23.5 dBm Peak Output Power and over 4.5 THz GBW

5.1 Introduction

With the emergence of millimeter-waves technologies, the ability of distributed power amplifiers (DPAs) to achieve high output power (P_{OUT}), large gain and wide bandwidth (BW), in commercial CMOS technologies will open the door to new broadband applications. There is, however, a design trade-off, where most of reported silicon-based distributed amplifiers (DAs) either have a BW $>$ 100 GHz in exchange with lower-power performance [13, 47, 54, 65], or an output power $>$ 15 dBm with a smaller BW [16, 17, 33–36, 75]. The reason is that high-power generation under a limited voltage supply requires large device sizes for high current generation (low impedance designs). However, in distributed amplifiers, a high P_{OUT} is achieved

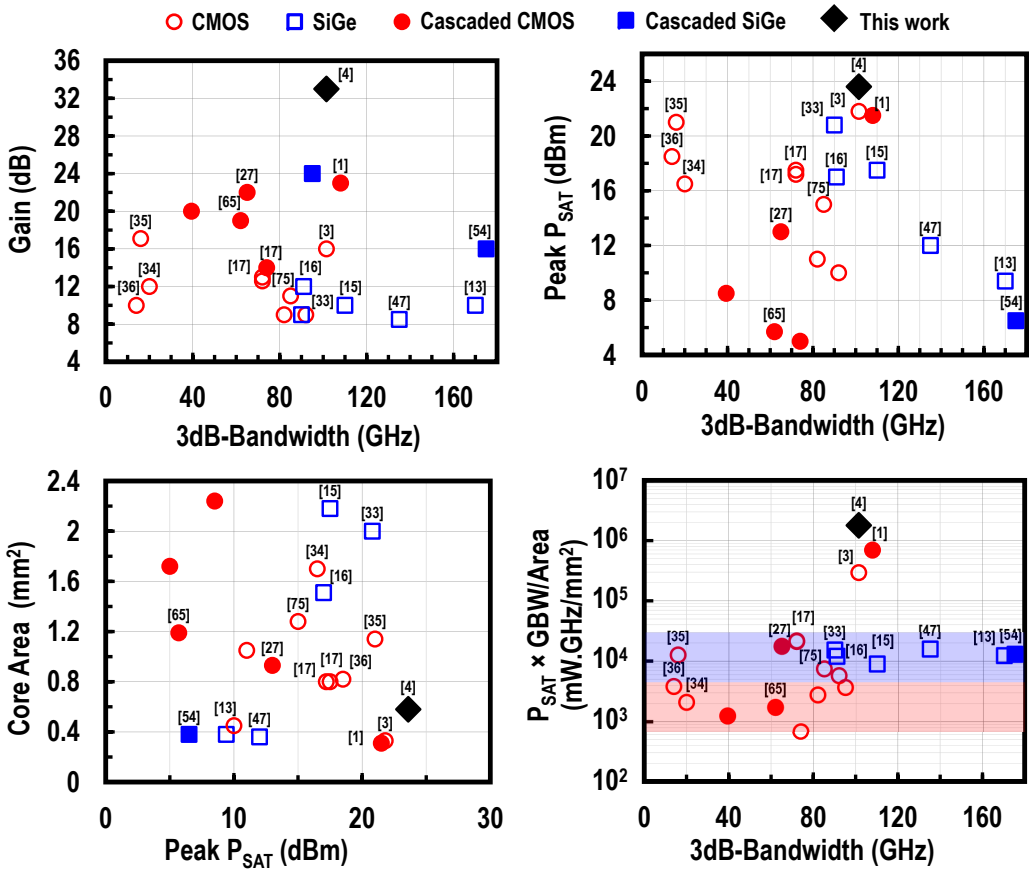


Figure 5.1: Distributed power amplifiers trends showing gain-bandwidth, P_{SAT} and core area trade-offs.

by increasing the number of stages while keeping a small device per stage to preserve the BW. The number of stages is limited by the input TL loss which increases with frequency, as higher TL loss impedes the input signal flow to the last stages, limiting their P_{OUT} and gain contribution. The gain-bandwidth-product (GBW) can still be improved for a limited P_{OUT} by cascading DAs to increase the gain at the expense of chip-area and efficiency.

Fig. 5.1 captures the gain-BW, P_{SAT}-BW, and P_{SAT}-area trade-offs for published cascaded and non-cascaded DPAs in both SiGe and CMOS technologies. Note that few publications achieve $>$ 100 GHz BW and $>$ 15 dBm peak P_{SAT} and this is done by stacking [3], pseudo-differential topology [15], or multi-drive inter-stack coupling [1, 2]. A multi-drive DC-to-108 GHz DPA/ modulator driver is recently reported with state-of-the-art 1.525 THz GBW and 21.5 dBm peak

P_{SAT} in a core area of 0.31 mm^2 [1, 2].

In this work, we propose a 4.53 THz GBW DPA realized in 45nm SOI. In order to achieve $>$ 30 dB gain, the CMOS PA exploits a modified multi-drive inter-stack coupling through the addition of resistive damping in the coupling network. The damping improves the stability without sacrificing the BW, input TL compensation, or DC power consumption as explained in section III. The DPA relies on two cascaded stages and the use of magnetic-field confinement in 8-shaped TLs [3] to deliver record performance with nearly 3$\times$ the GBW and 2 dB higher peak P_{SAT} when compared to the state-of-the-art. In addition to continuous-wave (CW) performance, the proposed design provides the highest average P_{OUT} for different modulation schemes and data rates compared to published silicon-based DPAs.

5.2 Design

In a DPA architecture, the parasitic capacitance of the unit gain cells is absorbed by the input and output TLs. Several factors affect the operational BW including Bragg cut-off frequency, f_c, of the loaded input/output TLs and the topology of the gain cells. The loaded input TL f_c and insertion loss are the dominant factors due to the higher input capacitance and attenuation per stage, $\alpha(\omega)$, compared to the output TL. When the drain and intrinsic TL losses are small compared to the gate loss, $\alpha(\omega)$ is given by the effective gate resistance r_g and input capacitance C_{in} per stage as [53, 76]:

$$\alpha(\omega) \approx \frac{1}{2} r_g C_{in}^2 Z_\circ \omega^2, \tag{5.1}$$

which increases quadratically with frequency, and sets a limit on the number of unit gain cells M [13]. For equal propagation delay and loaded impedance for the input and output TLs, the power gain G is approximated as [2]:

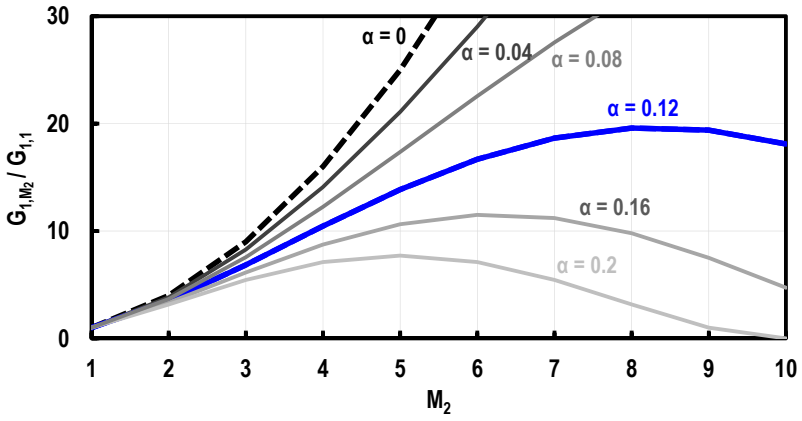


Figure 5.2: Normalized power gain for an M_2 unit cells amplifier for different loss per stage, $\alpha(\omega)$.

$$G_{N,M_1} \approx \left((M_1 g m_u \frac{Z_\circ}{2}) \times (1 - M_1 \frac{\alpha(\omega)}{2}) \right)^{2N} \tag{5.2}$$

where N is the number of cascaded stages, M_1 is the number of unit gain cells per stage, each with an effective transconductance gm_u, and $Z_\circ$ is the loaded impedance of the TLs. The overall area scales linearly with N where $A_{N,M_1} = N \times M_1 A_u$, and A_u being the area of a unit cell.

For a non-cascaded topology having M_2 gain cells, (5.2) reduces to:

$$G_{1,M_2} = \left((M_2 g m_u \frac{Z_\circ}{2}) \times (1 - M_2 \frac{\alpha(\omega)}{2}) \right)^{2} \tag{5.3}$$

with the area $A_{1,M_2} = M_2 A_u$. Fig. 5.2 presents G_{1,M_2} normalized to the unit-cell power gain $G_{1,1}$ for different values of $\alpha(\omega)$. For the maximum gain, an optimum number of gain cells is calculated by differentiating (5.3) with respect to M_2 resulting in $M_{2,opt} = 1/\alpha(\omega)$.

Equating (5.2) and (5.3) for equal gain for both cascaded and non-cascaded topologies, the chip area ratio is:

$$r = \left(\frac{A_{1,M2}}{A_{N,M1}} \right)_{G_{fixed}} = \frac{(M_1 g m_u \frac{Z_\circ}{2})^{N-1}}{N} \times \frac{(1 - M_1 \frac{\alpha(\omega)}{2})^N}{(1 - M_2 \frac{\alpha(\omega)}{2})}, \tag{5.4}$$

where $A_{1,M2} > A_{N,M1}$ for all $N > 1$ and the cascaded stage gain $M_1 g m_u Z_\circ / 2 \geq 2$. Similarly, the

gain ratio for equal chip areas, obtained by setting $M_2 = N.M_1$ then dividing (5.2) by (5.3), is also given by r where:

$$r = \left(\frac{G_{N,M1}}{G_{1,M2}}\right)_{A_{fixed}} = \left(\frac{A_{1,M2}}{A_{N,M1}}\right)_{G_{fixed}} > 1. \tag{5.5}$$

The cascaded topology can therefore provide an area or GBW enhancement over the non-cascaded design. In practice, the BW is $< f_c$ due to the gain-cell limited speed and the signal loss along the input TL. Therefore, r is even higher than (5.4) for all $M_1 < M_2$, increasing the cascaded topology advantage. On the other hand, the number of cascaded stages is usually limited in DAs by amplifier stability due to the high gain and limited reverse isolation caused by the inevitable substrate coupling in a small chip area. Note that the overall efficiency also degrades for cascaded topologies since pre-drivers are less efficient compared to the output stage. Therefore, in order to achieve a target gain and P_{OUT}, the output stage should be designed with the maximum number of unit-cells for an allowable BW as given in Fig. 5.2 so as not to limit the BW. The input stage(s) are then designed to increase the gain with enough linearity to drive the output stage.

The proposed DPA structure consists of two cascaded stages, each containing 8-stage multi-driven stacked gain-cells analyzed in section III (Fig. 5.3). Although the stages are not identical, the area and GBW enhancements hold as long as the gain per stage is ≥ 6 dB. The output PA employs a 4-stack topology to achieve high P_{OUT} with only one fourth of the power-amplifying device capacitance needed to be absorbed by the input and output TLs, thus maintaining a large BW. The input driver is designed using 2-stack gain cells with less than half of the voltage supply to provide the required gain and reverse isolation while preserving high efficiency. Reliable operation is achieved by equally dividing the output voltage swing and drain impedance between the devices within the stack and allowing a gate voltage swing for the stacked devices in exchange for some gain reduction [3, 51, 52, 57].

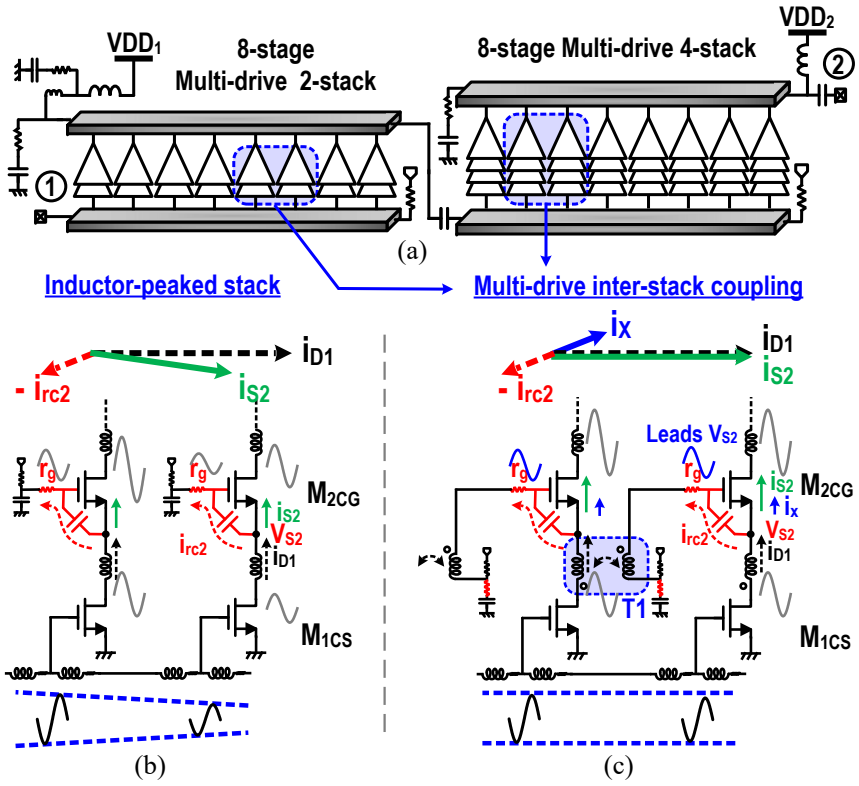


Figure 5.3: (a) Structure of the cascaded distributed power amplifier. Schematic and phasor diagram of (b) inductor-peaked unit cells compared to (c) multi-drive inter-stack coupling.

5.3 Multi-Drive Inter-Stack Coupled-Gain Cells

The stacked gain elements, for both driver and output stage, are first optimized for gain and P_{OUT} up-to-100 GHz. As frequency increases, a part of the current, i_{D1}, generated by the lower common-source devices (CS) is lost in the intermediate nodes parasitic capacitance (Fig. 5.3(b, c)). As a result, the current entering the stacked device, i_{S2}, is not aligned with i_{D1}, reducing the power combining efficiency. This is usually solved by using intra-stack peaking inductors which are placed in series in a DA structure to allow for DC operation at the expense of some series resistive loss (Fig. 5.3(b)) [3, 13]. The peaking inductors resonate with the parasitic capacitance to improve current alignment within the stack. They also increase the effective transconductance (*Gm*) of the stack at high frequencies to help compensate for the increased loss of the input TL

versus frequency and results in better gain flatness across frequency.

Series peaking compensation is a viable solution until the stack-loss is dominated by r_g of the stacked devices. Previously, a stack multi-drive technique [21] has been proposed to compensate for the current lost in r_g so as to improve the efficiency and P_{OUT} over conventional series peaking in the mm-waves regime. This was achieved using a dedicated driver for the stacked device of the output stage. The concept was extended in [1, 2] to compensate for the loss in a DPA structure with the use of inter-stack passive coupling. The inter-stack coupling only peaks at high frequencies through a transformer T1 (Fig. 5.3(c)) while the performance follows a standard series-peaked stack design in the lower frequency range. This coupling efficiently realizes synchronized multi-drive signals for the stacked elements of the different gain cells, and removes the power and area overhead of dedicated stack drivers. In this work, a similar technique is exploited to improve the GBW with a focus on stability in order to achieve $>$ 30 dB gain.

Referring to Fig. 5.3(c), T1 transforms a part of the current i_{D1} generated from the CS device to a voltage swing at the gate of the stacked device of the following stage. This leading voltage signal at the gate of the stacked device compared to its source node replenishes the current, i_{rc2}, lost in its r_g by generating an extra current component i_X equal in magnitude and opposite in phase with i_{rc2}.

Fig. 5.4 presents the trans-impedance (Tran-Z) gain of T1 under proper loading conditions. It is seen that the trans-Z gain only peaks at frequencies $>$ 60 GHz. The magnetic coupling, k_m, controls the trans-Z peaking frequency, and thus the compensation BW. In this design, the BW extension is applicable from 60 to 115 GHz, for k_m=0.35, where the phase of V_{out} is positive signaling a leading voltage. Above 115 GHz, when V_{out} starts lagging the input current i_{in}, the coupled signal does not compensate for the delay across the stack and the performance drops.

The small gate inductance (L_G) of T1 creates a negative real impedance at the drain of the CS devices, and this is translated through the gate-to-drain capacitance to compensate for the input TL loss. Since a small value of L_G is essential to guarantee stability across PVT (process-voltage-

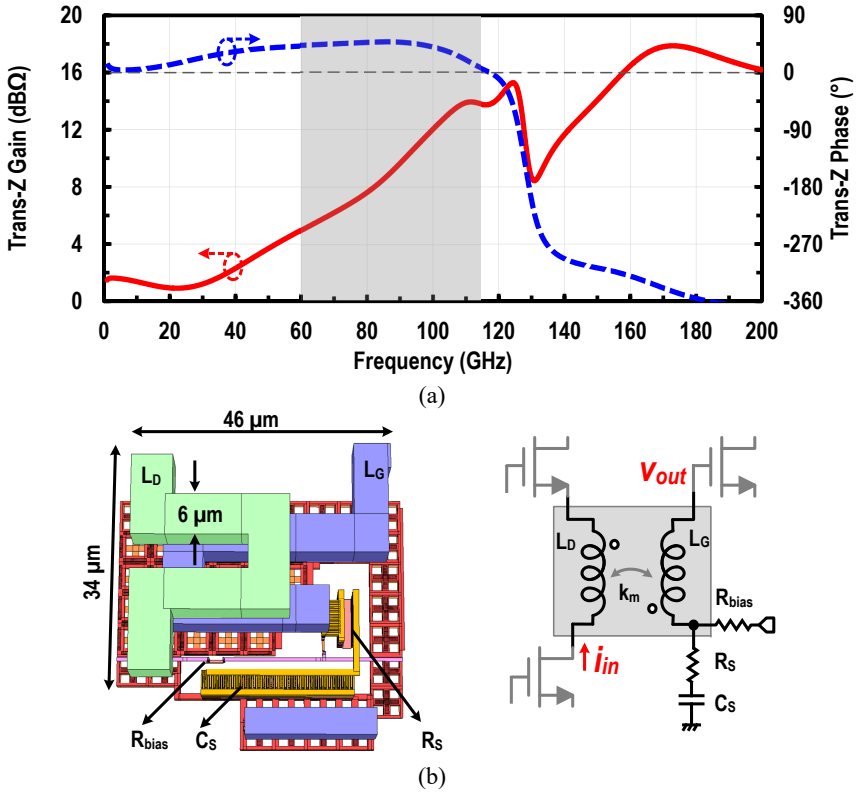
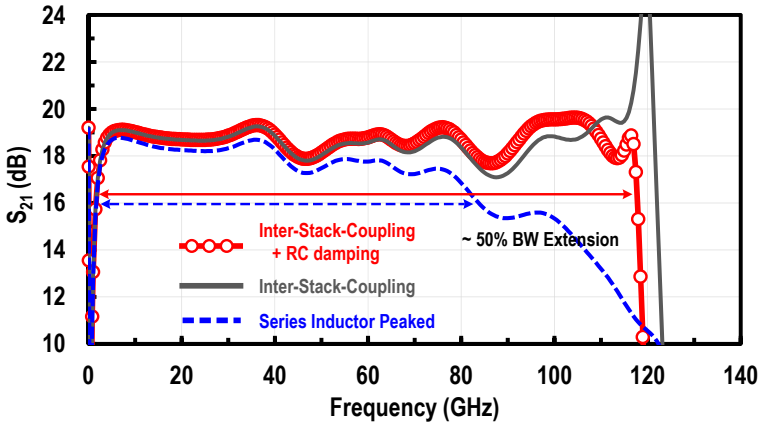
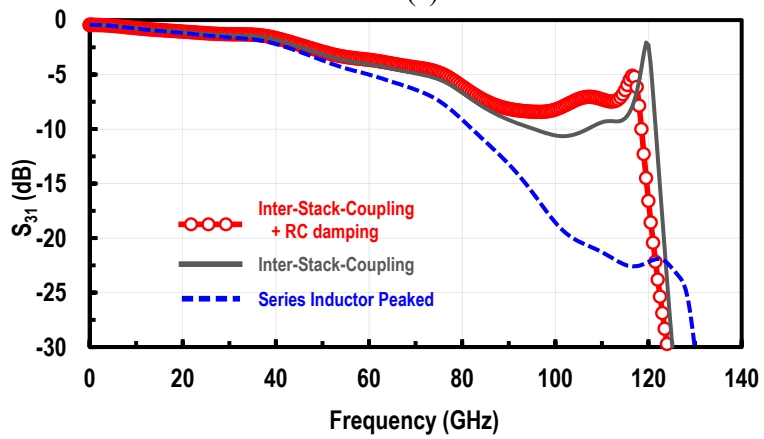


Figure 5.4: (a) Simulated trans-impedance gain and phase for the inter-stack coupling transformer. (b) Transformer 3-D layout and connection.

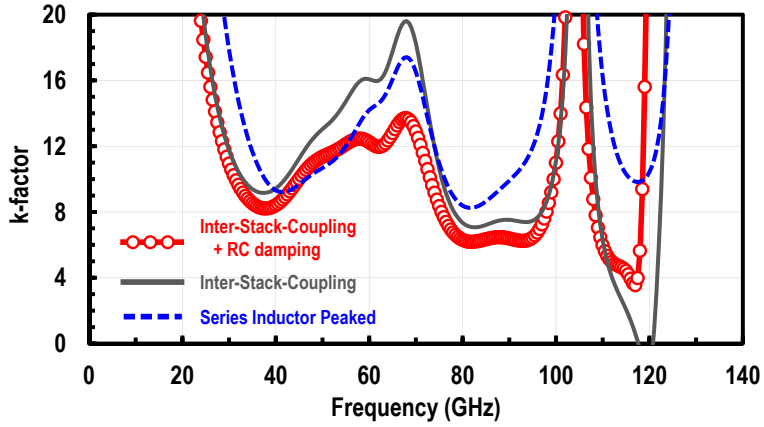
temperature), a damping resistor (R_S=7 Ω) is placed in series with the gate-scaling capacitors (C_S) (Fig. 5.4(b)). The damping resistor limits the quality factor of the parallel resonance of T1 secondary winding to improve the inter-stack stability. The damping resistor should be large enough to render the design unconditionally stable (k-factor $>$ 1), while not being overly large in order not to limit T1 Trans-Z gain, and thus compensation, near the resonance. Fig. 5.5 compares the simulated gain (S_{21}), input TL insertion loss (S_{31}) and stability factor for the output stage having 8 gain elements each with a 4-stack cell topology. The multi-drive inter-stack coupling results in $\approx$ 50% BW extension compared to series inductor peaking. This is due to input TL line compensation in addition to *Gm* peaking to yield a flat gain. A lower input TL insertion loss allows increasing the number of stages to increase the gain and power without sacrificing the BW. Since the transformers are used off-resonance to provide the leading voltage, the damping



(a)



(b)



(c)

Figure 5.5: Effect of the inter-stack coupling on the output stage: (a) small-signal gain (S_{21}),(b) input TL insertion loss (S_{31}), and (c) stability-factor (k-factor).

resistors have little effect on the BW extension and input TL compensation but do improve the stability near the cut-off frequency. In addition, the placement of the damping resistors on the

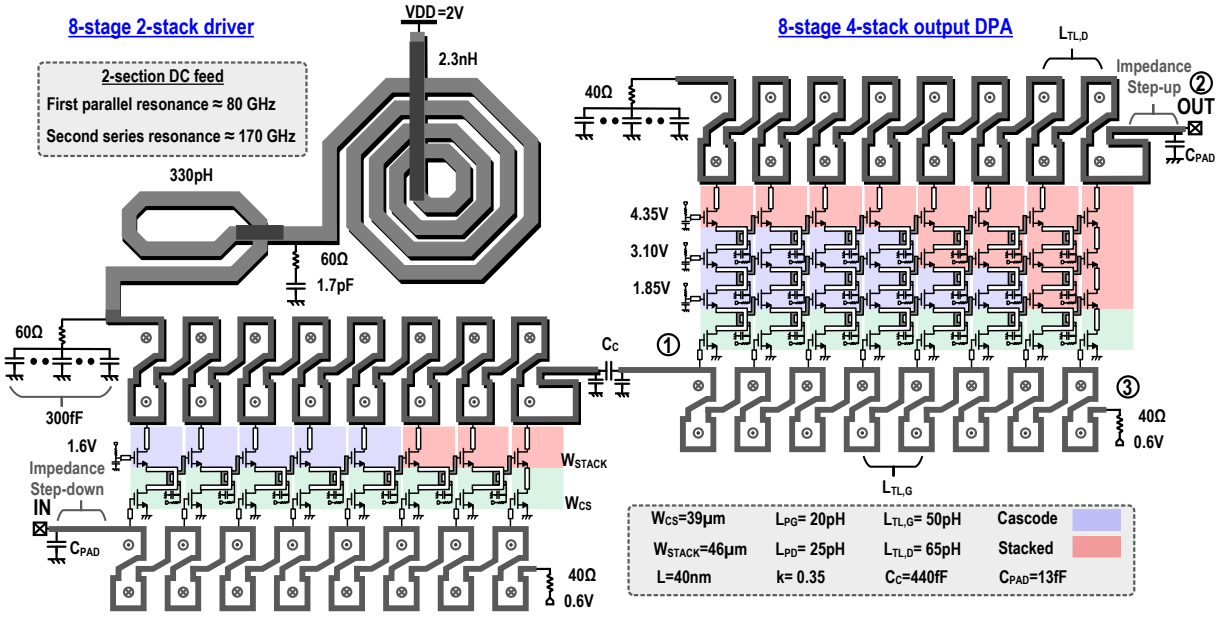


Figure 5.6: Schematic of the cascaded distributed power amplifier with multi-drive inter-stack coupling. Note the TL overlap (transformer T1) between the different stacks resulting in multi-drive inter-stack coupling.

gate nodes avoids DC power consumption and efficiency degradation. The line compensation allows the number of stages to increase to 8 for both the driver and output PA and results in higher gain and P_{OUT} without compromising the bandwidth.

5.4 Implementation

In a DA structure, the voltage swing builds-up on the output TL towards the output stages. Therefore, only the output stages need to adopt a stacked topology for linearity and reliability, while the input stages can be designed in a cascode fashion (AC grounded common gates) for high gain (Fig. 5.6). The loaded output TL $Z_\circ$ is designed around 40 Ω to maximize P_{OUT}, based on load-pull simulations.

The multi-drive inter-stack coupled gain cells are combined with 8-shaped input and output TLs. The 8-shaped lines increase the inductance per unit length in a compact footprint, keep neighboring stages in physical proximity for the inter-stack coupling and are particularly

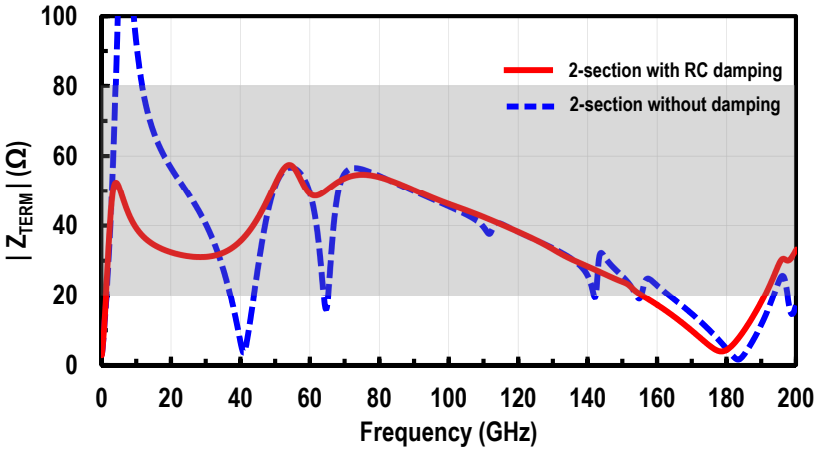


Figure 5.7: Simulated output TL termination impedance Z_{TERM}.

useful in magnetic field confinement [20]. The driver output TL and termination are combined with a 2-section DC feed which provides ≈ 40 Ω impedance at 2 GHz to greater than 100 GHz without requiring an external bias-tee for the driver. Fig. 5.7 presents the simulated output TL termination impedance Z_{TERM} with and without the DC feed damping. The RC damping ensures the termination impedance remains between 80-20 Ω (-10 dB matching) within the 3 dB-BW by limiting the parallel resonance of the larger inductor (2.3 nH) and degenerating its series resonance. The smaller inductor (330 pH) is designed with 80 GHz self (parallel) resonance while its second (series) resonance is at 170 GHz, far enough from the operating frequency range.

The cascaded multi-drive inter-stack coupled DPA is realized in the 45nm RFSOI Global-Foundries process with a core area of 0.58 mm^2 (Fig. 5.8). The NMOS devices, having a peak f_t/f_{max} of 290/250 GHz when referenced to the top metal layer, are 20% larger for the stacked devices (46 μm) compared to the CS ones (39 μm) to equate both input and output TL delays per stage. All transistors have a 40 nm channel length, a 1 μm width per finger, and double contacted gates to reduce r_g. In addition, the 8-shaped output TL uses the upper two 1.2 µm thick copper layers tied together for current handling and lower unloaded $Z_\circ$ compared to the input TL. Both TLs are implemented on a high-resitivity substrate (ρ ≈ 2.5 kΩ) for lower loss and higher unloaded $Z_\circ$ (78 Ω and 70 Ω for the input and output TLs, respectively). The inter-stack coupling

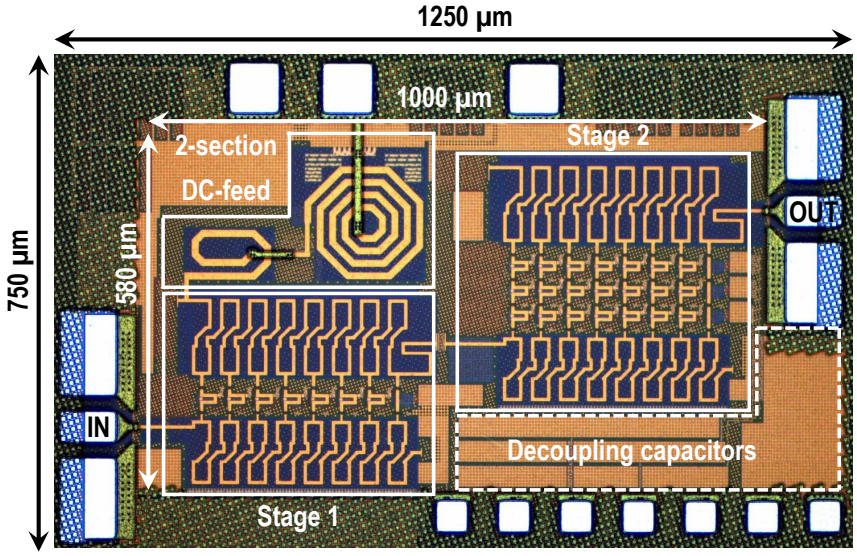


Figure 5.8: Die micrograph of the fabricated distributed amplifier chip in 45nm CMOS SOI process.

transformers are implemented using the top two copper metals with a patterned ground plane for field confinement. The pads parasitics (≈13 fF) are included in the matching networks at both ports for a small impedance step-down (between 40 and 50 Ω) for optimum power delivery.

5.5 Measurements

5.5.1 Continuous-Wave Performance

Three setups are used to measure the small-signal performance of the cascaded multi-drive DPA. A vector network analyzer (Keysight N5247A PNA-X) is used for frequencies < 70 GHz, which also provides a bias-tee for the output port. Millimeter-head controller and two sets of frequency extenders modules are used to cover the ranges from 75-to-110 GHz with WR-10 probes, and above 110 GHz with WR-6 probes. The DPA achieves an in-band gain of 33 dB with > 100 GHz bandwidth reaching a record 4.533 THz GBW (Fig. 5.9(a)). The simulated gain for the loaded driver and output stage are 14 dB and 19 dB respectively. The measured gain is within 1 dB from simulations up-to-50 GHz. The in-band ripple is $< \pm 3$ dB up-to 104

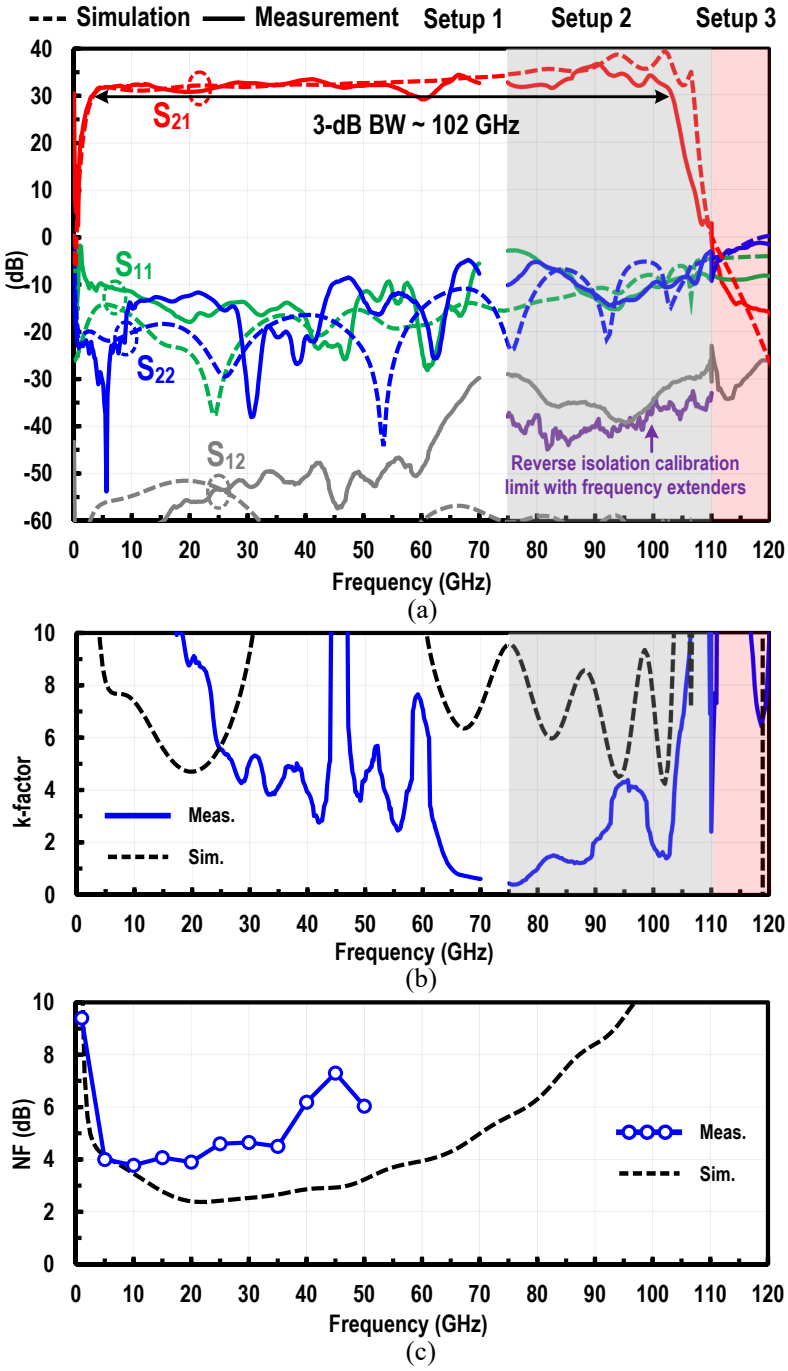


Figure 5.9: Small-signal performance versus frequency: (a) simulated and measured S-parameters; (b) k-factor, and (c) noise figure. .

GHz. The measured 3-dB cut-off frequency is 104 GHz compared to 107 GHz in simulations. Except a ripple at 60 GHz, the deviation of the measured gain for frequencies higher than 50

GHz can be attributed to an over-estimation of the self resonance of the gate capacitors in the driver cascode stages. EM-simulations of 640 and 385 fF AC ground capacitors reveal 62 and 85 GHz self-resonance frequencies, respectively, when including the routing networks. An over-estimation of the self resonance of the gate capacitors can explain the BW reduction. In addition, the reverse isolation, and thus stability-factor (k), at W-band and above is limited by the inherent isolation of the frequency extenders, where a value of $S_{21} + S_{12} > 0$ dB yields a k-factor < 1 (Fig. 5.9(b)). The measured noise figure (NF) at DC-to-50 GHz is shown in Fig. 5.9(c) with a minimum of 3.8 dB at 10 GHz and < 7.5 dB at 45 GHz.

The measured large-signal continuous-wave (CW) performance is presented in Fig. 5.10. The output stage is biased in class-AB with an 0.45 V overdrive voltage (V_{od}) and 13 mA per transistor, in order to maximize the linearity, while the driver is biased in class-A (V_{od} = 0.6 V and 20 mA per transistor) for high gain. The chip consumes 820 mW at power back-off with 320 mW for the driver and 500 mW for the output stage. The DPA achieves P_{SAT}, P_{1dB} and peak PAE > 21 dBm, 18.7 dBm , and 9.9%, respectively, up-to-60 GHz. The large-signal 3 dB-BW for both P_{SAT} and P_{1dB} is > 60 GHz. At 60 GHz, the DPA demonstrates record P_{SAT}/ P_{1dB} values of 22.5/21.3 dBm, respectively, compared to published silicon-based DAs with a peak PAE of 14% (Fig. 5.10(a, b)), while the measured |AM-PM| distortion at P_{1dB} is $< 7^\circ$ at DC-to-50 GHz (Fig. 5.10(c, d)).

Table 5.1 compares the CW performance for the cascaded multi-drive DPA with silicon-based DAs. This work demonstrates the highest reported GBW by any technology while achieving the highest peak P_{SAT} for silicon-based DPAs. Compared to [2], using the same technology and multi-drive inter-stack coupling technique, the GBW is improved by $3\times$ while peak P_{SAT} is 1-2 dB higher owing to the 8-stack 4-stack output PA. Other work with lower GBW have lower P_{OUT} [13, 27] or larger area when the power is comparable [15–17].

Table 5.1: Continous-wave performance comparison with distributed power amplifiers

Design	This work	[2] El-Aassar JSSC'19	[3] El-Aassar SSCL'19	[65] Arbabian RFIC'12	[13] Testa JSSC'15	[16] Fang JSSC'16	[27] Jahanian TMTT'12	[17] Fang TMTT'19	[15] Chen TMTT'11
Technology process	45nm RFSOI	45nm RFSOI	45nm RFSOI	130nm SiGe	130nm SiGe	90nm SiGe	65nm CMOS	45nm RFSOI	130nm SiGe
f_T/f_{max} (GHz)	290/250	290/250 (NMOS) 240/255 (PMOS)	240/255 (PMOS)	200	300/500	300	160/200	290/250	200
Frequency (GHz)	2.5-104	DC-108	1.5-103	15-110	DC-170	14-105	DC-65	10-82	DC-110
Supply (V)	4.8, 2.4	5 (Pre-driver) / 6.6 (PA)	5	3.3	3.6	4, 3.6, 3.2, 2.7	1.3	1.5-2.4	3
Gain (dB)	33	23	16	24	10	12	22	13	10
GBW (GHz)	4533	1525	640	1500	537	362	818	322	348
$^{\&}P_{1dB}$ (dBm)	20.9 @ 20GHz 19.5 @ 40GHz 21.3 @ 60GHz	19.5 @ 25 GHz 20.8 @ 50 GHz 17.5 @ 70 GHz	19.0 @ 20 GHz 18.5 @ 40 GHz 17.5 @ 60 GHz	N.R.	7.5* @ 50 GHz	14.9 @ 5 GHz	10 @ 2 GHz	13 @ 50 GHz	16.7 @ 40 GHz
$^{\&}P_{SAT}$ (dBm)	23.6 @ 20GHz 22.0 @ 40GHz 22.5 @ 60GHz	20.5 @ 25 GHz 21.5 @ 50 GHz 18.4 @ 70 GHz	21.7 @ 20 GHz 21.0 @ 40 GHz 19.0 @ 60 GHz	N.R.	9.4* @ 50 GHz	17 @ 50 GHz	12* @ 2 GHz	17.2 @ 50 GHz	17.5 @ 40 GHz
PAE_{max} (%)	17.8 @ 20GHz 12.4 @ 40GHz 14.0 @ 60GHz	10.8 @ 25 GHz 13.4 @ 50 GHz 6.8 @ 70 GHz	18.4 @ 20 GHz 15.7 @ 40 GHz 10.0 @ 60 GHz	N.R.	N.R.	12.6 @ 50 GHz	N.R.	17.1 @ 50 GHz	13.2 @ 60 GHz
PAE_{P1dB} (%)	10.4 @ 20GHz 7.7 @ 40GHz 11.6 @ 60GHz	9.1 @ 25 GHz 12.5 @ 50 GHz 5.9 @ 70 GHz	12.0 @ 20 GHz 10.7 @ 40 GHz 8.4 @ 60 GHz	N.R.	N.R.	8.5* @ 50 GHz	N.R.	10* @ 50 GHz	11.5 @ 60 GHz
$^{\&}$AM-PM @P1dB (°)	-1.7 to -6.8 from DC to 50GHz	+2.1 to -3.6 from DC to 70 GHz	-5 @ 40 GHz	N.R.	N.R.	N.R.	N.R.	7.5* @ 50 GHz	N.R.
Core Area (mm^2)	0.58	0.31	0.33	0.41	0.38	1.51	0.93	0.8	2.18^

N.R. = Not Reported ^ Including pads
* Estimated from plots & Best setting at each frequency

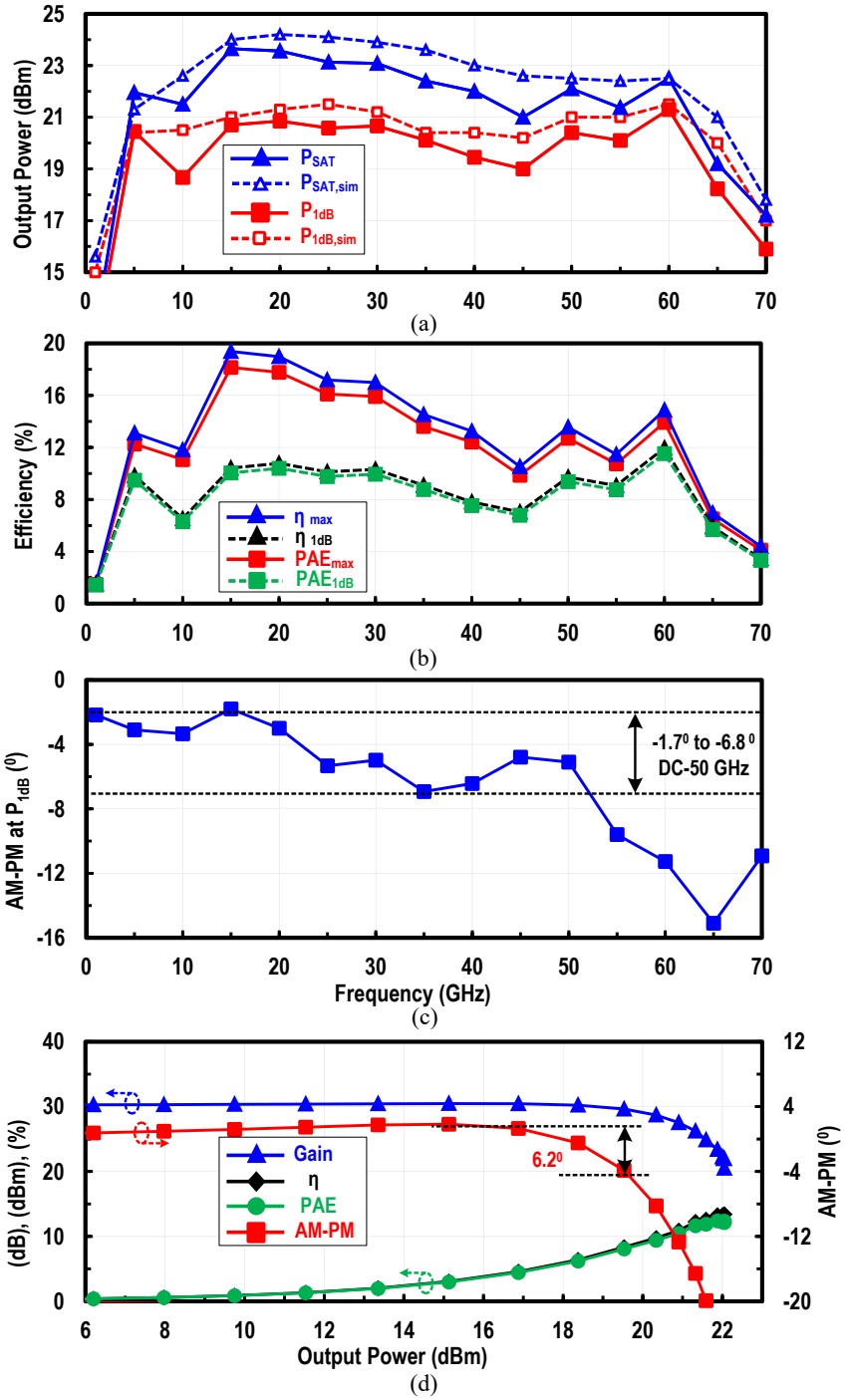


Figure 5.10: CW large-signal performance: (a) Measured and simulated P_{1dB} and P_{SAT} across frequency. (b) Measured PAE_{P1dB}, PAE_{max}, and drain-efficiencies η_{1dB}, η_{max} versus frequency. (c) Measured AM-PM. (d) Measured gain, η, PAE, and AM-PM versus output power at 40 GHz.

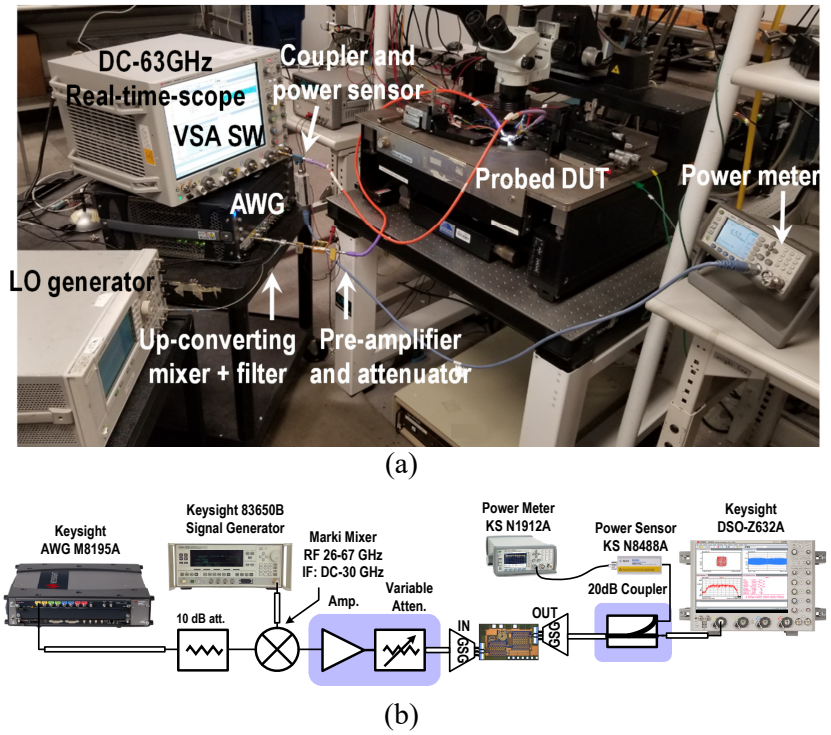


Figure 5.11: EVM measurements: (a) photograph, and (b) setup.

5.5.2 Modulated-Data Measurements

The DPA is tested with 16/64/256-QAM modulated signals for several data-rates and carrier frequencies (up-to-56 GHz) to assess the performance under complex modulation schemes. Fig. 5.11 presents the error vector magnitude (EVM) measurement setup: an arbitrary waveform generator (Keysight AWG M8195A) provides the 64-QAM signals followed by an optional up-converting mixer, depending on the desired carrier frequency, an attenuator and a drive amplifier. A 63 GHz real-time-scope (Keysight DSOZ632A) is used to capture the signal from the DUT and extract the constellations and EVM values using the Keysight 89601 Vector Signal Analyzer (VSA) software. The calculated EVM is normalized to the peak of the constellation, while the modulation-error-ratio (MER) is also reported to normalize the error to the average power of the signal. A linear 21 symbol feed-forward equalizer is used in the scope to remove linear errors such as group-delay distortion and frequency response ripples. The equalizer cannot remove

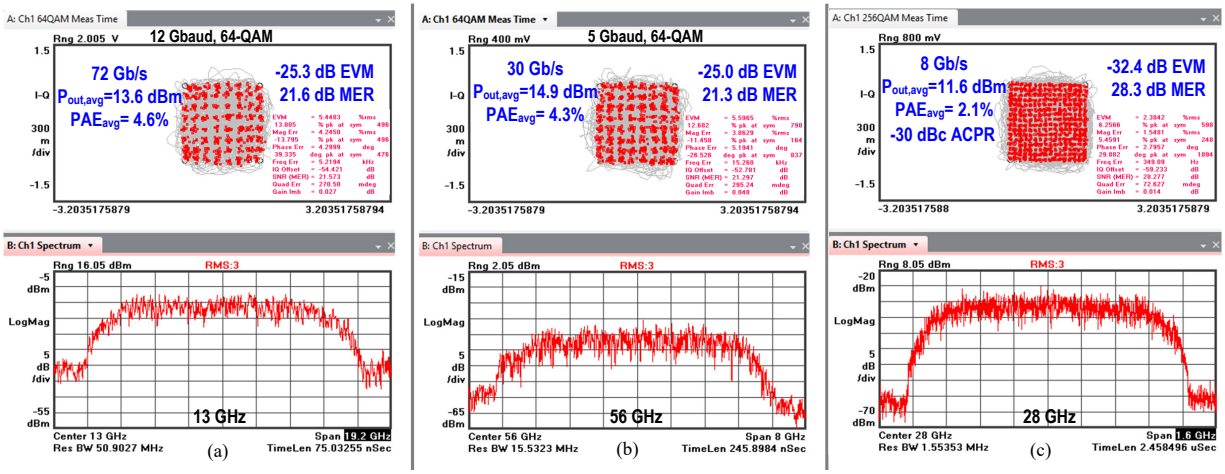


Figure 5.12: (a) Measured EVM, data spectrum and average P_{OUT} for: (a) 64-QAM constellation with 72 Gb/s and a 13 GHz carrier frequency. (b) 64-QAM constellation with 30 Gb/s and a 56 GHz carrier frequency. (c) 256-QAM constellation with 8 Gb/s and a 28 GHz carrier frequency.

non-linear errors such as harmonic distortion and spectral-regrowth. Same type of equalizer and number of symbols are used for all measurements but different equalizer coefficients are present for each setup, and no pre-distortion is applied. The average P_{OUT} is measured with a power sensor connected at the DUT output using a coupler with dedicated power calibrations at each carrier frequency.

The DPA is first measured with 64-QAM signals and a 13 GHz carrier for data rates from 30-up-to-90 Gb/s (5 to 15 GBaud). Next, the carrier frequency is swept from 5-to-56 GHz and the average P_{OUT} is captured for 30 Gb/s signals (5 GBaud). For all 64-QAM measurements, the EVM is kept at -25 dB (Fig. 5.12). The 64-QAM modulated signals performance is summarized in Fig. 5.13. For the 30 Gb/s measurements, the cascaded DA achieves an average $P_{out} > 14$ dBm across frequency with a 14.9 dBm level for a 56 GHz carrier. To the authors knowledge, this is the highest data-rate and average P_{OUT} for reported DAs over 50 GHz. The DPA also demonstrates up-to 3$\times$ higher data rates (90 Gb/s, 64-QAM waveforms) with an average $P_{OUT} > 10$ dBm at 13 GHz, limited by the setup noise.

The adjacent channel power ratio (*ACPR*) is measured for the DPA for a 64-QAM 6 Gb/s signal and a 28 GHz carrier frequency (Fig. 5.14). An *ACPR* $<$ -27 dBc is achieved for an average

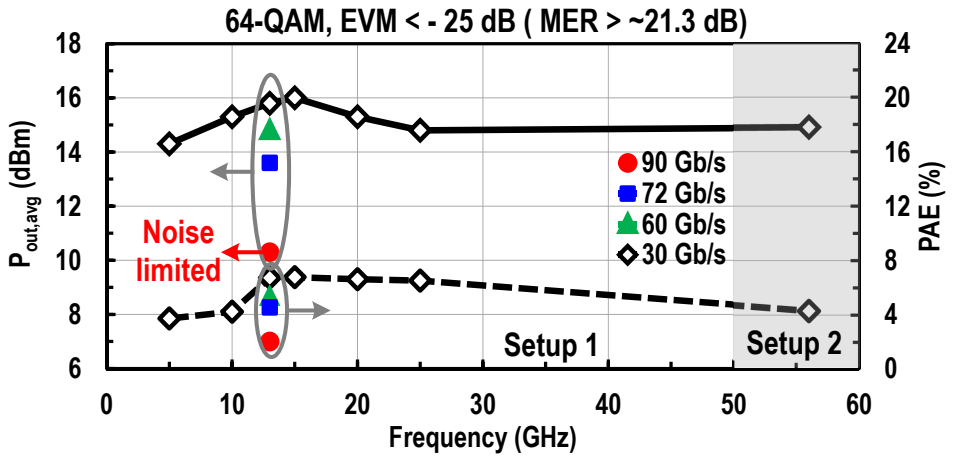


Figure 5.13: Measured average P_{OUT} for 64-QAM constellations and an EVM < -25 dB with different carrier frequencies up-to-56 GHz. Data is taken at 5 GHz BW (30 Gb/s) except at 13 GHz where different bandwidths are used.

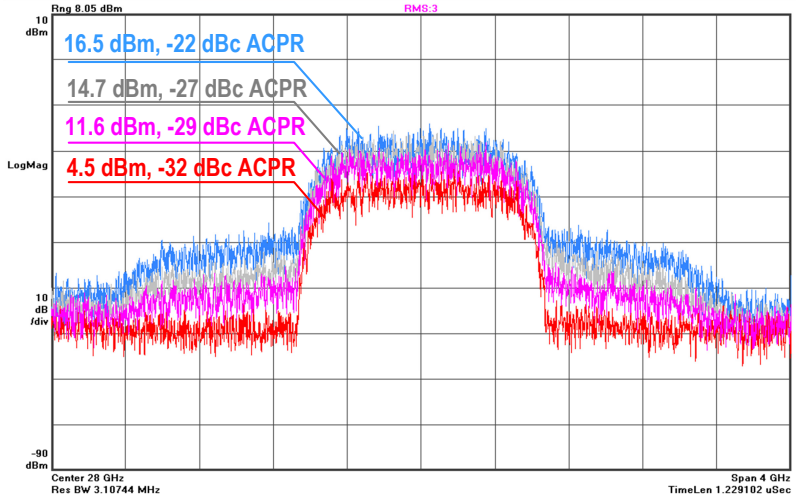


Figure 5.14: Measured spectrum and *ACPR* for 6 Gb/s 64-QAM constellations at 28 GHz for different average P_{OUT}.

P_{OUT} up-to 14.7 dBm with the minimum *ACPR* being noise limited by the setup to -32 dBc. For all power values, the upper and lower side *ACPR*s are within 1.7 dB showing little impact of memory effects.

The DPA is also tested with a 256-QAM 8 Gb/s signal around 28 GHz (Fig. 5.12(c)). An average P_{OUT} = 11.6 dBm is recorded for an EVM/ *ACPR* < -32 dB/ -30 dBc respectively. A 12 dBm 32 Gb/s 16-QAM OFDM signal is also measured using a 28 GHz center frequency for

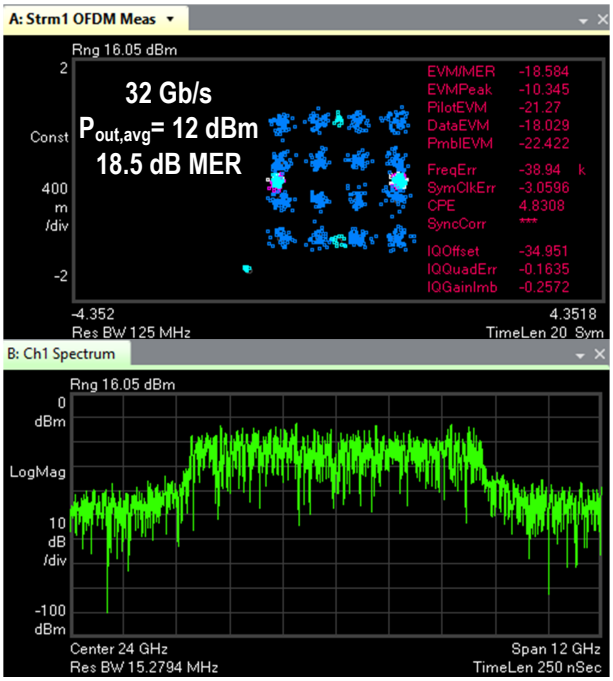


Figure 5.15: Measured EVM, spectrum and average P_{OUT} for a 32 Gb/s 16-QAM OFDM waveform with 28 GHz center frequency for sub-carriers.

sub-carriers with a modulation error ratio (MER) $<$ 18.5 dB (Fig. 5.15).

Table 5.2 benchmarks the DPA modulated-data performance with silicon-based wideband and distributed PAs [2, 17, 67, 69–71]. The DPA achieves the highest average P_{OUT} for $>$ 30 Gb/s bit-rates. For lower data-rates, the reported average P_{OUT} levels are the highest compared to DPAs and among the highest compared to non-distributed PAs.

5.6 Conclusion

This work presented a cascaded DPA with a record 4.53 THz GBW. Cascading, stacking, and multi-drive inter-stack coupling techniques are all analyzed and exploited to achieve simultaneously high P_{OUT} and gain in a BW $>$ 100 GHz. The addition of resistive degeneration is proposed, for the multi-drive coupling transformer secondary windings, in order to improve the stability and attain $>$ 30 dB gain. The 8-shaped TLs enable magnetic field confinement and

Table 5.2: Complex modulated data performance comparison with wideband millimeter-wave and distributed power amplifiers

Design	This work					[2] El-Aassar JSSC'19					[67] Chappidi JSSC'18	[69] TW. Li ISSCC'18	[17] Fang TMTT'19	[70] Nguyen ISSCC'19	[71] Wang ISSCC'19
Technology process	45nm RFSOI					45nm RFSOI					130nm SiGe	130nm SiGe	45nm RFSOI	45nm RFSOI	45nm RFSOI
Frequency (GHz)	13	25	56	28	24	14	25	59	28		50	28.5	47.5	60	28
Modulation	64-QAM			256-QAM	16-QAM OFDM	64-QAM			256-QAM	16-QAM OFDM	16-QAM	64-QAM	16-QAM	64-QAM	64-QAM
Bit-rate (Gb/s)	72	30	30	8	32	102	30	30	8	32	4	18	20	12	15
#EVM (dB)	<-25			<-32	<-18.5	<-25			<-32	<-20	-21.75	-25	<-25	-27.1	-24
Pout (dBm)	+13.6	+14.9	+14.9	+11.6	+12.0	+7.1	+14.3	+13.3	+8	+9.4	+16.9	+9.8	11.8*	20.9	15
PAE (%)	4.6	6.5	4.3	2.1	2.3	2.6	5	4.7	1.7	2.0	12.6*	18.4	7.5*	3.4	26.4

* Estimated from plots # Normalized to the peak of the constellation

inter-stack coupling in a compact area. The DPA maintains a P_{1dB} and $P_{SAT} > 18.7$ and 21 dBm, respectively, up-to-60 GHz and demonstrates over 14 dBm average P_{OUT} in 64-QAM with an EVM $< 5\%$ for 30 Gb/s data rate for carriers up-to-56 GHz. The state-of-the-art performance in both CW and modulated signals permits the DPA to be used in most radar and imaging applications, and multi-Gb/s communications systems.

5.7 Acknowledgment

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Chapter 5, in full, has been accepted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "Cascaded Multi-Drive Stacked-SOI Distributed Power Amplifier with 23.5 dBm Peak Output Power and over 4.5 THz GBW," *IEEE Transactions on Microwave Theory and Techniques*, accepted. The dissertation author was the primary investigator and primary author of this paper.

Chapter 6

Design of Low-Power Sub-2.4 dB Mean NF 5G LNAs Using Forward Body Bias in 22nm FDSOI

6.1 Introduction

Improvements in noise and power performance of deeply-scaled CMOS nodes at mm-waves promises their inclusion in the next generation 5G front-ends. The LNA is a critical block in the front-end since it dominates the *NF* of the receive channel. The *NF* values for silicon-based K/Ka-band LNAs are 2-5 dB with DC power ranging from 13-80 mW [77–84]. The lowest reported *NF* values are 1.4-1.5 dB for 28 GHz CMOS-SOI LNAs with 13 dB gain [85, 86]. Also, the LNA gain is important for phased-arrays since the *NF* of 28 GHz phase-shifters is 10-16 dB [87, 88]. Therefore, for an overall channel *NF* of sub-3 dB prior to the TRX switch, the LNA gain should be 15-20 dB. A high LNA gain, however, typically poses stability and linearity concerns.

This work presents a detailed guideline for LNAs design in the mm-wave range in deeply

scaled technology nodes. The main focus is to provide optimization procedures for the devices, passives and topologies that yield to state-of-the-art designs while showing the technology-scaling, noise, power and linearity trade-offs.

We present three different K/Ka-band LNAs targeting high linearity, low noise, and high gain. The forward body bias (FBB) in FDSOI is exploited to improve the LNA performance under low supply conditions. Design considerations are first presented for each LNA to achieve the target specifications and a design recipe is provided considering noise, power, matching and stability trade-offs. The effect of FBB is then investigated in detail for the common-source (CS) and cascode (CAS) designs, and optimal bias is used for low power designs. Measurements across power levels and FBB bias are performed to provide an insight on the NF, gain, and bandwidth (BW) trends, and FoM scaling with reduced P_{DC}.

6.2 Technology and Device Selection

For LNA design, it is important to carefully optimize the device size and layout, particularly in the millimeter-waves frequency range where the active device noise contribution is dominant. The minimum noise figure (NF_{min}) for a MOS device can be expressed as [89, 90]:

$$NF_{min} = 1 + K\sqrt{gm(R_G + R_S)} \times \frac{f_T}{f}, \tag{6.1}$$

where gm is the device trans-conductance, R_G & R_S are the gate and source resistance, respectively, f is the operating frequency and f_T is the unity current gain frequency. CMOS technology scaling allows higher f_T and lower threshold voltage (V_T) resulting in lower noise and power consumption for the LNAs. This is difficult in bulk CMOS at sub-28nm nodes due to the short channel effects which can lead to bulk and surface punch-through across the source and drain depletion regions [91]. Moreover, intrinsic device gain deteriorates rapidly due to the drain induced barrier lowering (DIBL) [19].

Partially and fully-depleted SOI MOS devices and FinFETs are currently used for further scaling. Typically, FinFETS have better gate control over the channel leading to higher intrinsic gains compared to bulk and SOI CMOS. However FinFETs exhibit higher vertical gate resistance which limit the scaling benefit particularly for LNA designs. SOI devices, being planar, share a lot of fabrication masks with bulk CMOS while offering the advantages of reduced parasitic capacitance, lower leakage and higher *gm*. In fully depleted SOI, the bulk can be biased to control V_T and improve the device RF performance or save power. This is also applicable to bulk CMOS, to an extent, if a triple-well device is used. Nevertheless, the voltage values for body biasing, and thus V_T control range, is limited by the forward biasing of source and drain parasitic diodes. The lack of parasitic diodes in the 22nm FDSOI technology allows a V_T control range of $\approx$ 150 mV when the body bias is swept from 0 to 2 V and results in low-enough sensitivity for body bias control (75 mV/V) needed for robust trimming. The effect of the body bias on the LNA performance is one of main goals of this work.

6.3 Low Power/ Low Noise Design

6.3.1 Common Source Design

Simultaneous noise and power power matching for an inductively degenerated LNA, is typically achieved by increasing the device size, and biasing the transistor at the optimum current density for minimum noise ($J_{D,NF}$), in order to bring Z_{opt} to the 50 Ω circle (Fig. 6.1(a)) [92–94]. Z_{opt} is defined as the optimum source impedance yielding a minimum NF for the device. A source inductor (L_S) is then used to reduce the real part of the input impedance (Z_{in}) and bring it close to 50 Ω. A gate inductor (L_G) is finally added to resonate the capacitance of Z_{in} and match the input to 50 Ω. This technique, however, penalizes power consumption in deeply scaled nodes

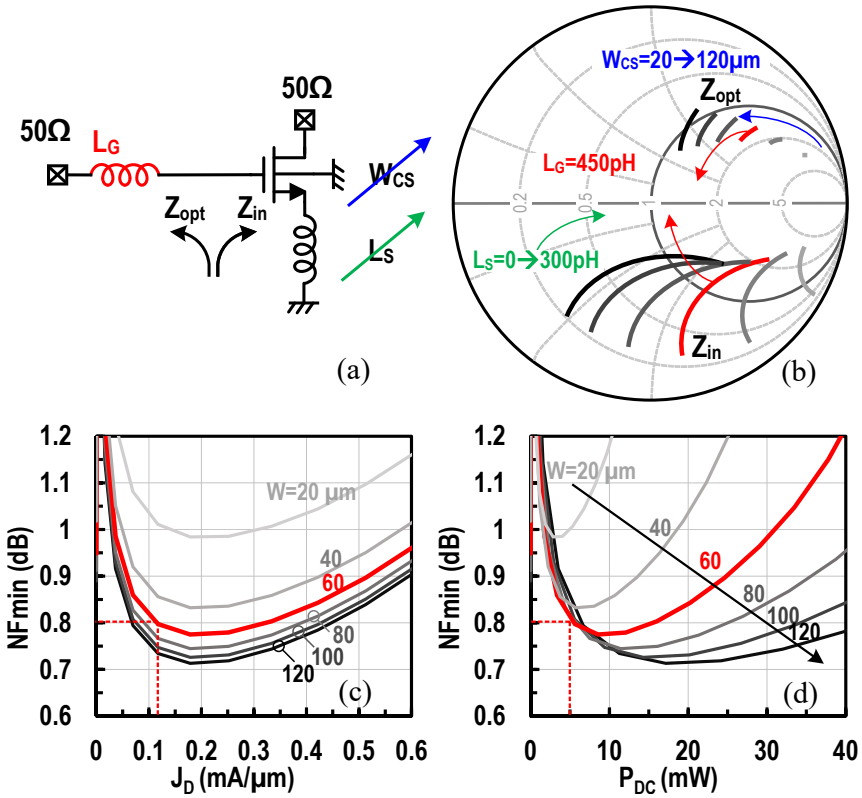

Figure 6.1: (a) Schematic of a CS inductive degenerated LNA. (b) Z_{in} and Z_{opt} variation with the device size. Simulated device noise performance at 28 GHz for several device widths: (c) NF_{min} versus the current density J_D, and (d) versus the power consumption P_{DC} for V_{DD} = 0.8 V.

as the real component of Z_{opt} is [77]:

$$Re[Z_{opt}] \approx \sqrt{\frac{R_G}{2gm}} \times \frac{f_T}{f}. \tag{6.2}$$

When biasing the device at $J_{D,NF}$, $Re[Z_{opt}]$ can be expressed in terms of the power consumption (P_{DC}) as:

$$Re[Z_{opt}] \approx \sqrt{\frac{R_G V_{od} V_{DD}}{4P_{DC}}} \times \frac{f_T}{f}, \tag{6.3}$$

where V_{od} is the overdrive voltage to achieve $J_{D,NF}$ irrespective of the device size. Therefore, a higher P_{DC} is needed to bring $Re[Z_{opt}]$ close to 50 Ω for high f_T technologies. An increase in the channel length or the addition of an extrinsic gate-to-source capacitance (C_{GS}) can satisfy

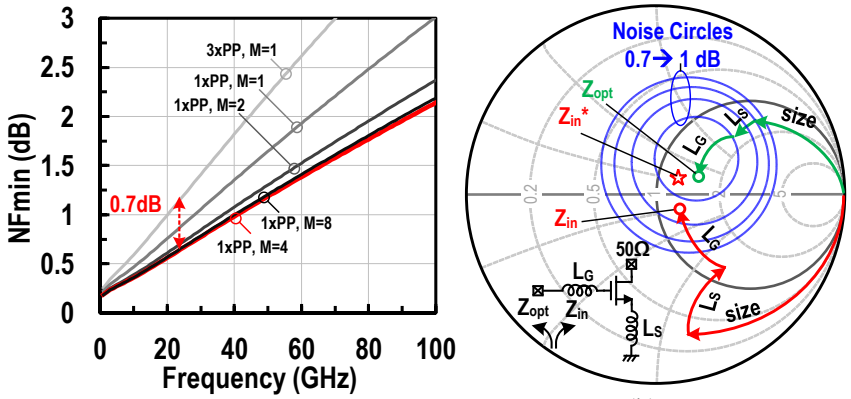

Figure 6.2: (a) Simulated NF_{min} versus frequency for a 60 μm nMOS with different gate poly-to-poly pitch (PP) and multiplier cells (M). (b) Z_{in} and Z_{opt} trajectories on Smith chart for the chosen 60 μm nMOS at 28 GHz.

the noise matching at a lower P_{DC} at the expense of f_T reduction and thus NF degradation (6.1). Fig. 6.1(b) plots Z_{opt} and Z_{in} when scaling the device size for different L_S values. A $Re[Z_{opt}]$ = 50 Ω is achieved for a 120 μm device at 28 GHz, and simultaneous noise and power matching can be satisfied when consuming 20 mW from a 0.8 V V_{DD} Figs. 6.1(c, d). A power-conservative approach can also be achieved by selecting a device size of 60 μm to reduce the power by half while ensuring $50 < Re[Z_{opt}] < 100$ Ω for an input matching better than -10 dB.

After selecting the transistor size based on noise/power trade-off, the device layout optimization is studied to minimize R_G. The finger width (W_{fing}) should be designed small enough to minimize the horizontal poly gate resistance, but large enough to minimize the vertical component according to the used technology. Simulations show that a 0.5 μm W_{fing} achieves a minimum NF_{min} of 0.52 dB, at 28 GHz, prior to upper metals routing. The NF_{min} varies by $<$ 0.02 dB when W_{fing} is increased to 1 μm. A 1 μm finger is, thus, chosen to minimize routing parasitics.

The 22nm FDSOI technology offers different values for the gate poly-to-poly pitch. The relaxed pitch (3xPP = 312 nm) reduces the fringing capacitance and the drain and source routing resistances, and is usually favored in power amplifiers designs. The narrow pitch (1xPP = 104

nm) reduces gate metal routing resistance and is selected for the LNA. The simulated NF_{min} of the 60 μm nMOS is plotted versus frequency for relaxed and narrow poly-pitches and different numbers of multipliers cells (M) ((Fig. 6.2(a)). An optimum number of multipliers M = 4 reduces metal routing resistance and results in $NF_{min} \approx 0.66$ dB after parasitic extraction to the top metal layer, compared to $NF_{min} = 1.36$ dB for the single multiplier/ relaxed pitch design.

Once the device size and layout are determined, the noise circles are plotted for the extracted design, and L_G and L_S are then chosen to bring Z_{in}^* to Z_{opt} within the desired noise circle (Fig. 6.2(b)).

6.3.2 Cascode Design

In order to increase gain without area penalty from cascading stages, a CAS topology is usally favored over the CS design. The CAS LNA benefits from the trans-impedance gain of the added common gate (CG) amplifier to increase the output impedance and overall power gain. A high output impedance provides the flexibility of using several CAS stages with high impedance inter-stage matching for higher gain but at the expense of BW [77, 95]. The CAS also reduces the impact of the gate-to-drain feedback capacitance (C_{GD}) of the CS device, and thus improves the reverse isolation by alleviating the miller effect.

Several concerns are addressed for mm-wave 5G CAS-LNAs, namely the BW limitation for a single stage, the LNA stability, and the noise contribution of the cascode device. Fig. 6.3(b) highlights the BW limitation by plotting the output impedance (Z_{out}), Z_{in}, and Z_{opt}, from 20-to-30 GHz, for equally sized CS and CAS LNAs. The CAS topology reduces the effective input capacitance while having little impact on Z_{opt}. More important is the Z_{out} increase, requiring a BW-limiting higher-Q matching network to bring it to 50 Ω. Two techniques are considered to improve the BW: series peaked cascode, and stacked configurations (Fig. 6.3(a)).

The inductance of a series-peaked cascode (L_{SP}) resonates the intra-stack capacitance and peaks *gm* for higher gain and results in a reduced cascode noise contribution, while the

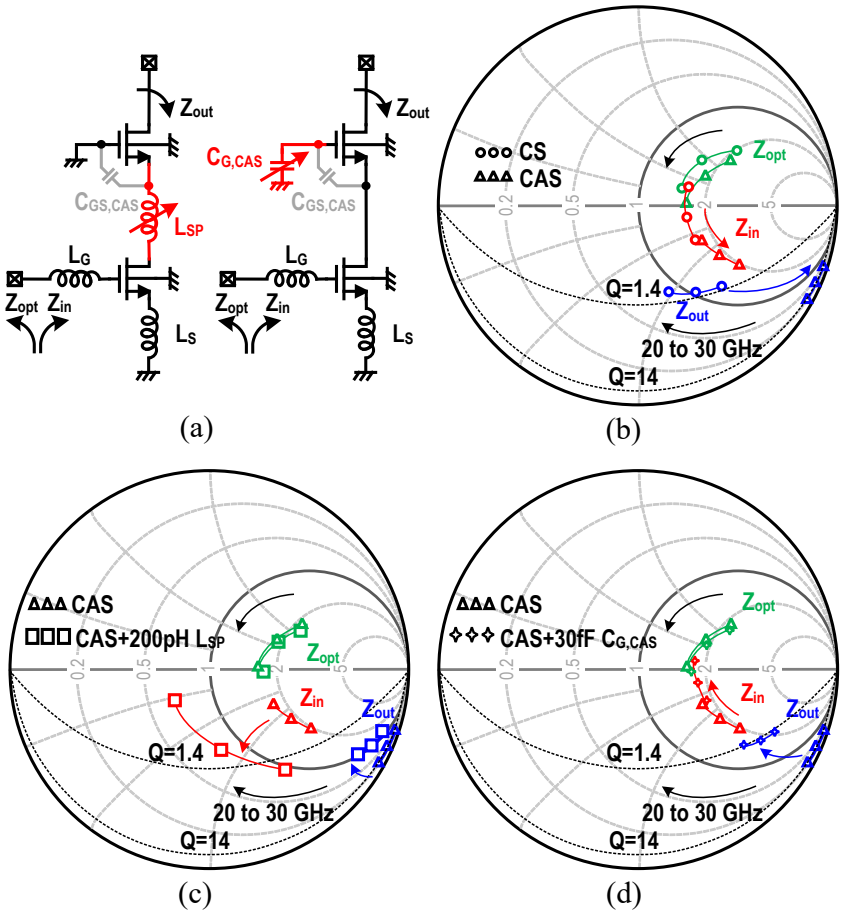

Figure 6.3: (a) Schematics of inductive degenerated LNAs using series peaked CAS and stacked configurations. Smith chart impedance trajectories from 20-to-30 GHz for Z_{in}, Z_{opt} and Z_{out}: (b) CS versus CAS configurations, (c) CAS versus series peaked CAS configurations, and (d) CAS versus stacked configurations.

zero introduced by the series peaking allows for BW extension (Fig. 6.3(c)). However, L_{SP} also translates through the CS C_{GD} and creates a negative real component reducing thus $Re[Z_{in}]$ while Z_{opt} remains the same. An increase in L_S is therefore mandatory to recover the noise matching condition. A larger L_S is usually accompanied by gain and NF degradation considering its finite Q as in (6.1).

The stacked configuration also allows for a voltage swing at the gate of the CAS device by proper scaling of $C_{G,CAS}$ leading to a reduced gm and Z_{out} (Fig. 6.3(d)). Similar reduction in gm and Z_{out} can be achieved by choosing a smaller CAS device. However, the stacking technique

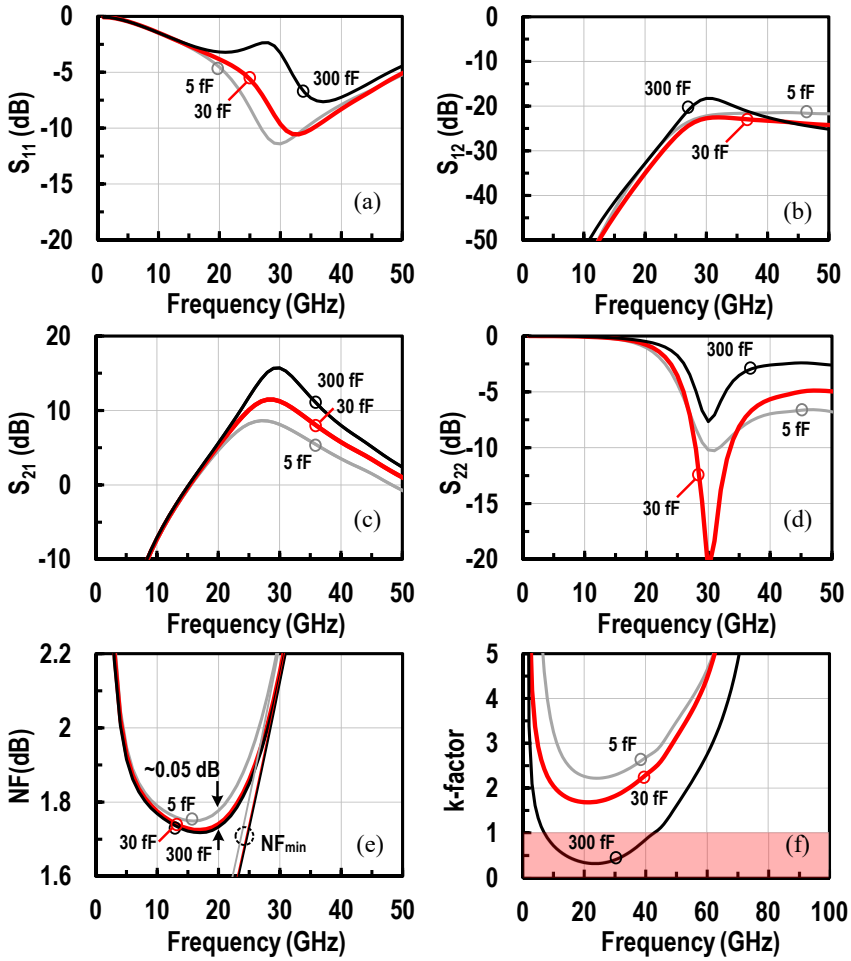

Figure 6.4: Simulated small-signal operation across frequency for a stacked LNA for different $C_{G,CAS}$ values: (a, b, c, d) S-parameters, (e) NF, and (f) stability factor k-factor.

enables an equally sized CAS, compared to the CS, also biased at $J_{D,NF}$ to minimize its noise contribution.

Fig. 6.4 compares the stacked and cascode topologies in terms of gain, matching, noise and stability. A stacked topology with $C_{G,CAS}$ = 30 fF improves the matching, isolation, 3dB-BW and renders the LNA unconditionally stable for the 60 μm device size (Fig. 6.4(a, b, d, f). The gain penalty is 4.5 dB compared to the cascode LNA (Fig. 6.4(c)), while the NF is within 0.05 dB (Fig. 6.4(e)).

The noise contribution of the common gate is exacerbated at mm-waves when the intermediate node parasitic capacitance provides a low impedance path for its current noise to flow to the

load. This noise component is usually removed using an additional intra-stack series peaking [80], parallel peaking [79, 96], or a transformer [97, 98] at the expense of area and resistive loss. The 22nm FDSOI technology achieves a post layout f_T of 180 GHz for the 60 μm nMOS biased at $J_{D,NF}$. This value is 6-to-9 times higher than the operation frequency range yielding to a small noise contribution from the common gate. Compared to a CS LNA, the CAS design has $\approx$ 0.3 dB higher NF at 28 GHz.

6.4 Forward Body Bias for Low power LNAs Design

The FBB is previously used in sub-6 GHz bulk CMOS designs with a $\approx$ 0.5 V tuning range limited by the forward-bias of the bulk-source junction. The FBB is used in nMOS [99], cascode [100], CMOS [101], and folded topologies [102] to reduce the power consumption and improve the gain and output conductance for reduced supply of operation. The FBB is also used at 60 GHz in bulk CMOS as a linearizer device in parallel with the gm-cell to improve the IIP_3 at the expense of NF [103]. Recently the FBB is exploited in fully-depleted SOI up-to 2 V for a 5G 22-32 GHz LNA to provide a less sensitive DC power control knob in addition to the gate bias voltage [80]. In this work, we aim to study the effect of FBB on Gain, NF, and IIP_3 for CS and CAS topologies across frequency and power level in the 22nm FDSOI technology.

Consider the 60 μm nMOS CS with FBB where the device is split into 4 multipliers to reduce R_G (Fig. 6.5(f)). The FBB can be used in 22nm FDSOI to reduce V_T from 320 mV to $<$ 50 mV when sweeping the FBB from 0-4 V with a simulated sensitivity of $\sim$ -76 mV/V. The gm, maximum available gain (MAG), and NF_{min} are plotted at 28 GHz versus J_D for the nominal (0.8 V) and reduced V_{DD} (0.3 V) in Fig. 6.5. A minimum NF_{min} is achieved at $J_{D,NF} \approx$ 0.1-0.15 mA/μm for all voltages. At this bias point, the simulated gm and MAG at 28 GHz are nearly the same for both the nominal and reduced V_{DD} conditions with a slight Nf_{min} degradation. This shows that one can design low-power mm-wave LNAs without trading gain and NF.

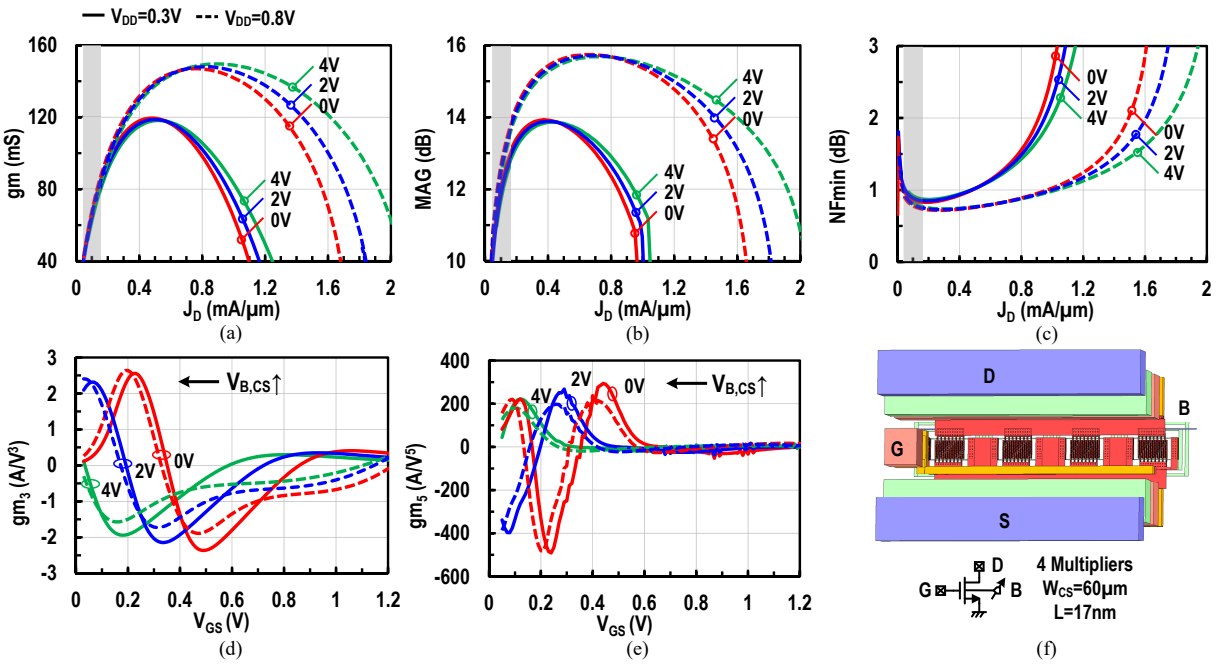

Figure 6.5: Simulated small-signal operation of a body-biased common-source nMOS for nominal (0.8 V) and reduced (0.3 V) V_{DD} at 28 GHz: *gm*, *MAG* and NF_{min} versus the current density (a, b, c); gm_3 and gm_5 variation versus the gate bias (d, e). Layout of the body-biased nMOS transistor (f).

The FBB also improves the band flatness of *gm* and *MAG* at high J_D values, and this can be exploited in power amplifiers to improve their linearity. Figs. 6.5(d, e) present the 2nd and 4th derivatives of *gm* (gm_3 and gm_5) for the nominal and reduced V_{DD} conditions. The optimal biasing primarily depends on J_D, and thus, is nearly constant for different device size and V_{DD} values. The FBB can manipulate gm_3 and gm_5 to bias around the sweet-spot for improved IIP_3 (Figs. 6.5(d, e)). This can also be achieved by changing the gate-to-source voltage (V_{GS}), however with a much higher sensitivity compared to FBB control which has $\sim$ 10 times less *gm* compared to the gate node. The FBB can, thus, be used to trim for better IIP_3 in the output stages of an LNA.

Fig. 6.6 presents results for an nMOS CAS with 60 μm width for the CG and CS devices. The body of the lower CS is grounded since it does not affect performance at $J_{D,NF}$, while the body of the CG device is left as a tuning knob. The simulated *gm*, *MAG*, and NF_{min} at 28 GHz are plotted versus J_D for a reduced V_{DD} of 0.5 V and compared to the single CS in Fig. 6.5(f) for

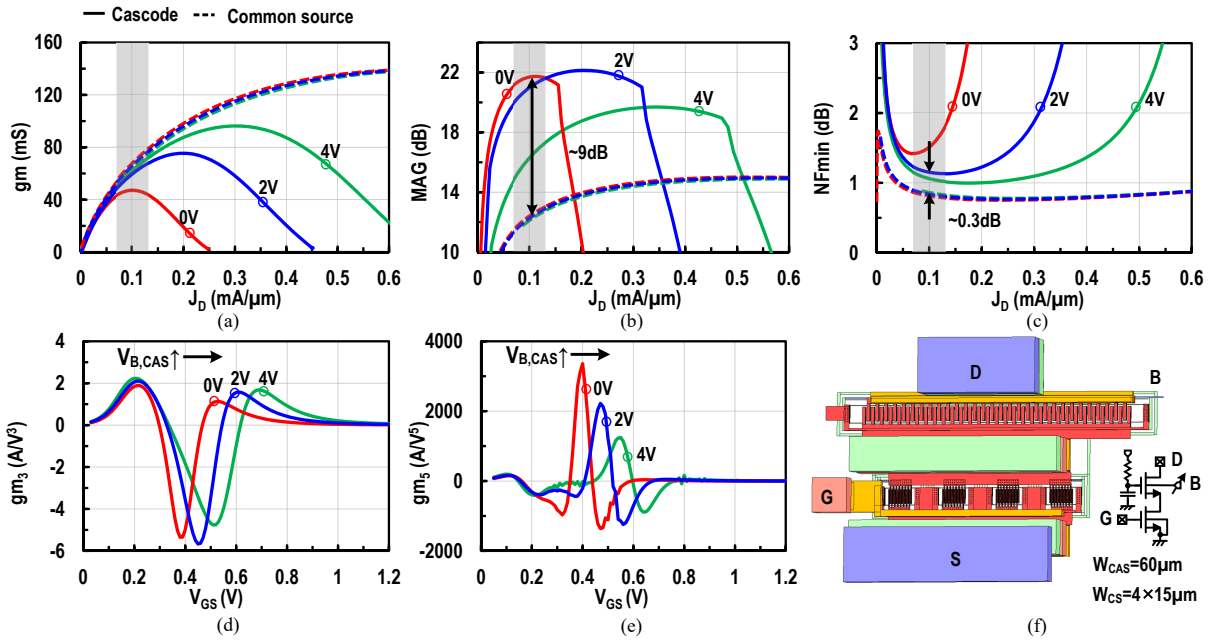

Figure 6.6: Simulated small-signal operation of a body-biased CAS compared to a CS with equal P_{DC} for V_{DD} = 0.5 V at 28 GHz: *gm*, *MAG* and NF_{min} versus the current density (a, b, c); gm_3 and gm_5 variation versus the CS gate bias (d, e). Layout of the CAS with a body-biased common-gate transistor (f).

the same P_{DC} (Fig. 6.6(a, b, c)). At $J_{D,NF}$, the reduced CS headroom in the CAS design limits *gm* and degrades NF_{min} (0.7 dB higher than the CS design), while *MAG* is increased due to the high cascode impedance. Applying FBB reduces V_{GS} of the CG device leading to a higher headroom and *gm*, and less *NF* for the CS device. When the FBB is increased to 4 V, the CG enters into the triode region under limited supply, thus reducing its trans-impedance gain and lowering *MAG* but the *gm* of the CS keeps improving due to the higher headroom and this improves NF_{min}. At the optimum FBB, the CAS can provide $\sim$ 9 dB *MAG* improvement over the CS in exchange with 0.3 dB NF_{min} degradation for the same P_{DC} and nearly the same chip area. The FBB of the CG device can also manipulate the effective gm_3 and gm_5 of the structure at low V_{DD} operation with little change in J_D and a lower sensitivity than its gate bias (Figs. 6.6(d, f)).

For high-gain designs, the LNA linearity can be limited by the output channel conductance (g_{ds}) rather than g_m. This output linearity limitation is usually dominant for low V_{DD} designs with reduced headroom for the RF swing. Fig. 6.7(a) presents the derivative g_{ds3} for the cascode across

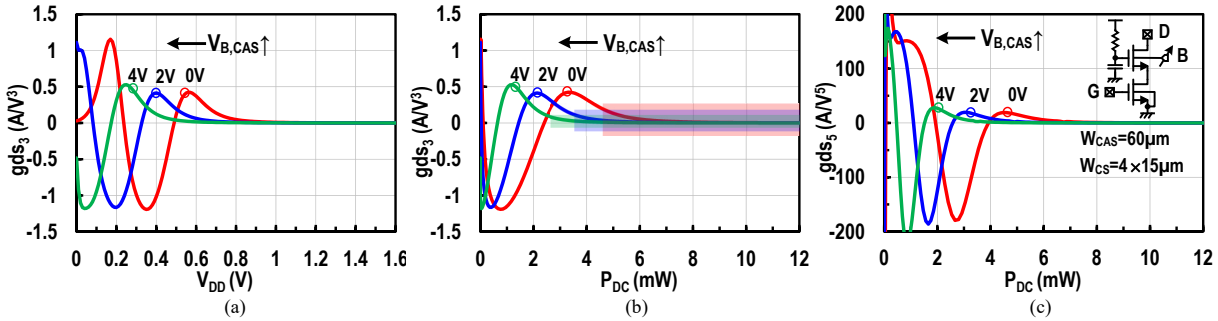

Figure 6.7: Simulated small-signal output channel performance for a body-biased CAS at 28 GHz: (a) channel conductance second derivative gds_3 versus V_{DD}; (b, c) gds_3 & gds_5 versus P_{DC} for different CAS body bias voltages revealing output linearity improvement for a given P_{DC} when using the FBB.

V_{DD} for three values of the FBB. A higher FBB value reduces g_{ds3} for a given supply. Notably, the FBB improves the cascode output linearity for a fixed P_{DC} (Figs. 6.7(b & c)). This is because the current, primarily controlled by the CS device, is weakly dependent on V_{DD}. While a lower V_T for the CAS device increases the output headroom of the CS for a fixed V_{DD}. Therefore, the FBB can be exploited to improve the IIP_3 for output-limited LNAs without incurring a power penalty.

6.5 Implementation

Three different mm-wave LNAs (1-stage CS, 2-stage CS and 2-stage CAS) were fabricated in GlobalFoundries 22nm FDSOI with a core area of 0.12mm^2 and 0.19 mm^2, respectively, for the single and 2-stage designs (Fig. 6.8). The 1-stage CAS design targets high linearity and broadband operation with $>$ 10 dB gain and $>$ 10 GHz 3dB-BW (Fig. 6.8(a)). Note that C_1 is reduced to 30 fF and this allows some RF swing on the stacked device gate and improves the output linearity at the expense of gain. The 2-stage CS is designed for minimum NF while achieving $>$ 20 dB gain and sub 10 mW operation (Fig. 6.8(b)). The size of M_{2CS} is 25% lower than M_{1CS} to increase its input impedance for gain and save power. The 2-stage CAS LNA aims for $>$ 25 dB gain with unconditional stability and low NF (Fig. 6.8(c)). The 2-stage design allows sufficiently high reverse isolation such that C_1 is increased to 95 fF for improved gain. Thin-oxide

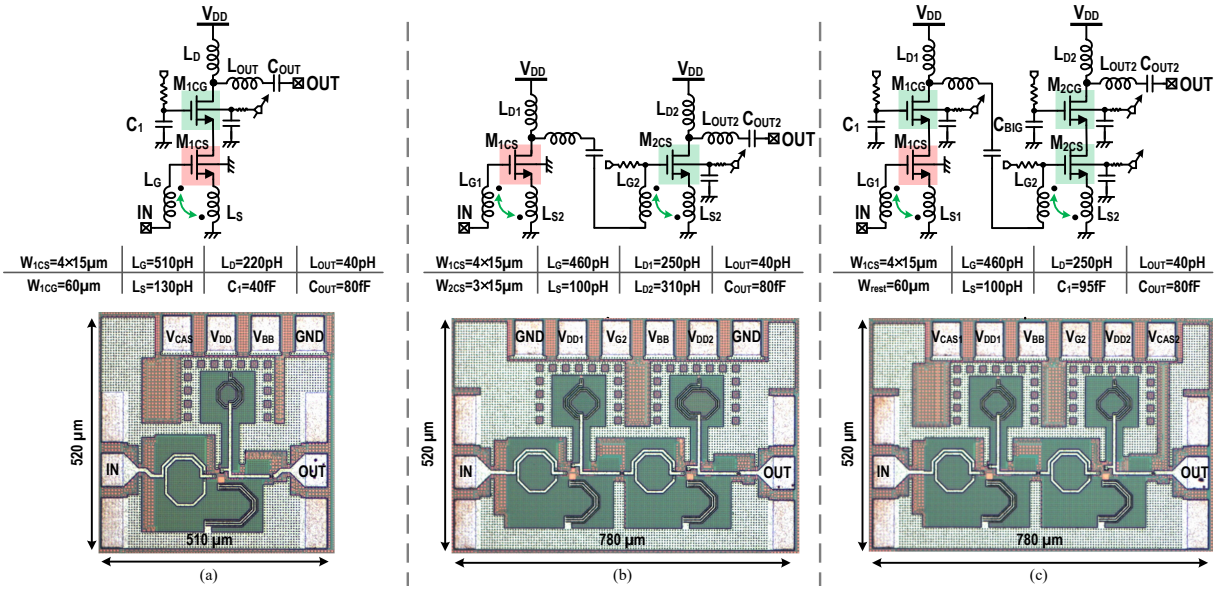

Figure 6.8: Schematics and die micrographs of the fabricated 5G LNAs with FBB in 22nm FDSOI: (a) Single-stage cascode, (b) 2-stage common-source, and (c) 2-stage cascode.

nMOS with minimum channel-length (L_{eff}=17 nm) are used for minimum NF and maximum gain. The body of the input device (M_{1CS}) is grounded since it does not affect the gain and NF at J_D= 0.1 mA/μm. The FBB is provided to the rest of the devices via a low-pass filter.

In the implemented designs, the gate layout routing is exploited to form a small extra C_{gs} MOM capacitor while minimizing routing overlap with the drain side (as mentioned in Section III, this improves the input impedance match). M_{1CS} is designed as four multipliers cells with tight finger-pitch (104 nm) for lower R_G in exchange for extra capacitance employed in the input matching. Cascode devices (M_{CG}) are designed with relaxed finger-pitch (312 nm) for less drain and source routing resistance and less overlap capacitance. In addition, a small negative coupling between the gate and source of M_{1CS} ($k_{gs} \approx$ -0.07) increases the effective $Re[Z_{in}]$ while reducing the imaginary of Z_{opt} which is also lowered by increasing C_{gs} and L_S. The size of L_S can thus be reduced for higher gain and lower NF (for a finite quality factor (Q_{LS}) case). This technique consumes the same P_{DC} of the extrinsic capacitor method and yields better gain and NF.

The passive structures are EM-simulated using Integrand EMX. Both L_D and L_S are

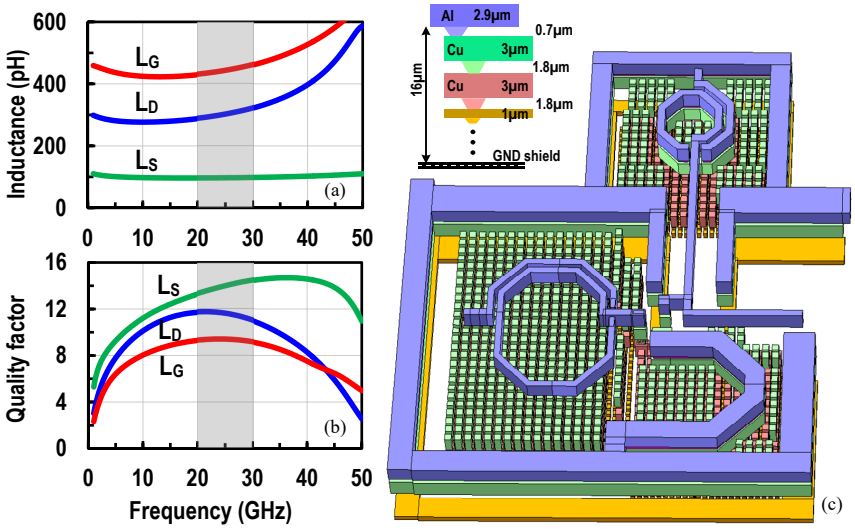

Figure 6.9: (a, b) Post metal-fill EM-Simulated inductances and the corresponding quality-factors (Q) for a single-stage cascode LNA. (c) Back-end metal stack cross-section and 3D layout view of the single stage LNA revealing the metal filling placement.

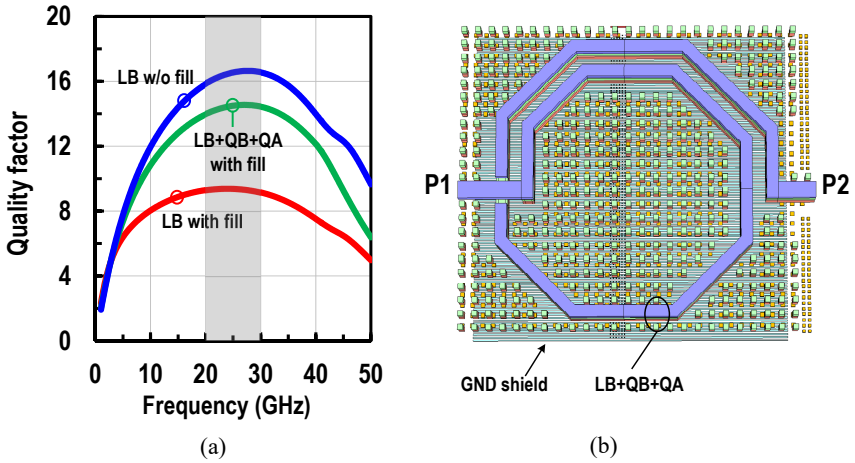

Figure 6.10: (a) EM-Simulated Q for the gate inductance before and after metal-fill. (b) 3D layout view.

implemented in the top 2 metal layers (2.9 μm aluminum and 3 μm copper), while L_G was designed on the top layer alone to maximize its self resonance. A patterned ground plane is placed on the lower two metals to shield the inductors from the low-resistivity substrate loss ($\rho \approx 7$ Ω-cm). The EM-simulated Q values for L_G, L_D, and L_S are 9.1, 11.9, and 14, respectively at 25 GHz (Fig. 6.9). It is important to mention that the initial Q values before the mandatory metal-fill is $\sim 30\%$ higher. Reducing the metal fill for the upper thick metals directly below the

winding is the most effective in lessening the Q degradation. In future designs, the inductor Q can also be enhanced by tying the top thick-metals together for the inductor winding at the expense of a reduced self resonance frequency. In this case, the peak Q for L_G can be increased from 9.1 to 14.5 in the 20-to-30 GHz band (Fig. 6.10).

6.6 Measurements

The three LNAs are RF probed and tested using a vector network analyzer (Keysight N5247A PNA-X) up-to 40 GHz (Fig. 6.11). The measured peak gain for the 1-stage CAS design is 10.2 dB with a 3dB-BW of 21.6-to-32.8 GHz. The power dissipated is 15 mW from a 1.6 V supply (Fig. 6.11(a)). The input and output matching are $<$ -10 dB from 26-to-34 GHz, and 26-to-31 GHz, respectively. The 2-stage CS achieves 20.1 dB peak gain with a 9 GHz BW from 19.5-to-28.5 GHz with P_{DC}=9.6 mW for the nominal 0.8 V supply. The gain is $>$ 15 dB from 18.5-to-32 GHz and the input matching (S_{11}) is $<$ -10 dB in the range from 22.3-32.2 GHz (Fig. 6.11(b)). The 2-stage CAS achieves 28.5 dB peak gain and 4 GHz BW from 23-to-27 GHz for the nominal operating conditions (P_{DC}=20 mW & V_{DD}=1.6 V) (Fig. 6.11(c)). Compared to simulations, the matching and peak gain frequencies are shifted down by $\sim$ 10% likely due to under-estimated inductors values and their parasitic capacitances. A ground mesh distributed across the chips reduces the ground inductance and yields a measured stability-factor $>$ 1 for the single-ended designs with gain up-to 28.5 dB (Fig. 6.11(d, e, f)).

The measured and simulated NF for the three LNAs is shown in Fig. 6.11(g, h, & i)) for the nominal operation. The measured mean-NF of the 1-stage CAS is 2.2 dB with a worst $NF <$ 2.5 dB up-to-30 GHz. The 2-stage CS demonstrates a 2.1 dB mean-NF within the 3dB-BW and with a minimum of 2 dB, while the 2-stage CAS design has a 2.25 dB mean-NF with a minimum of 2.2 dB ($\sim$ 0.2 dB higher than the CS LNA). The measured NF for the three LNAs is 0.3-0.5 dB higher than simulated values. The detrimental effect on the inductors Q from the high-density

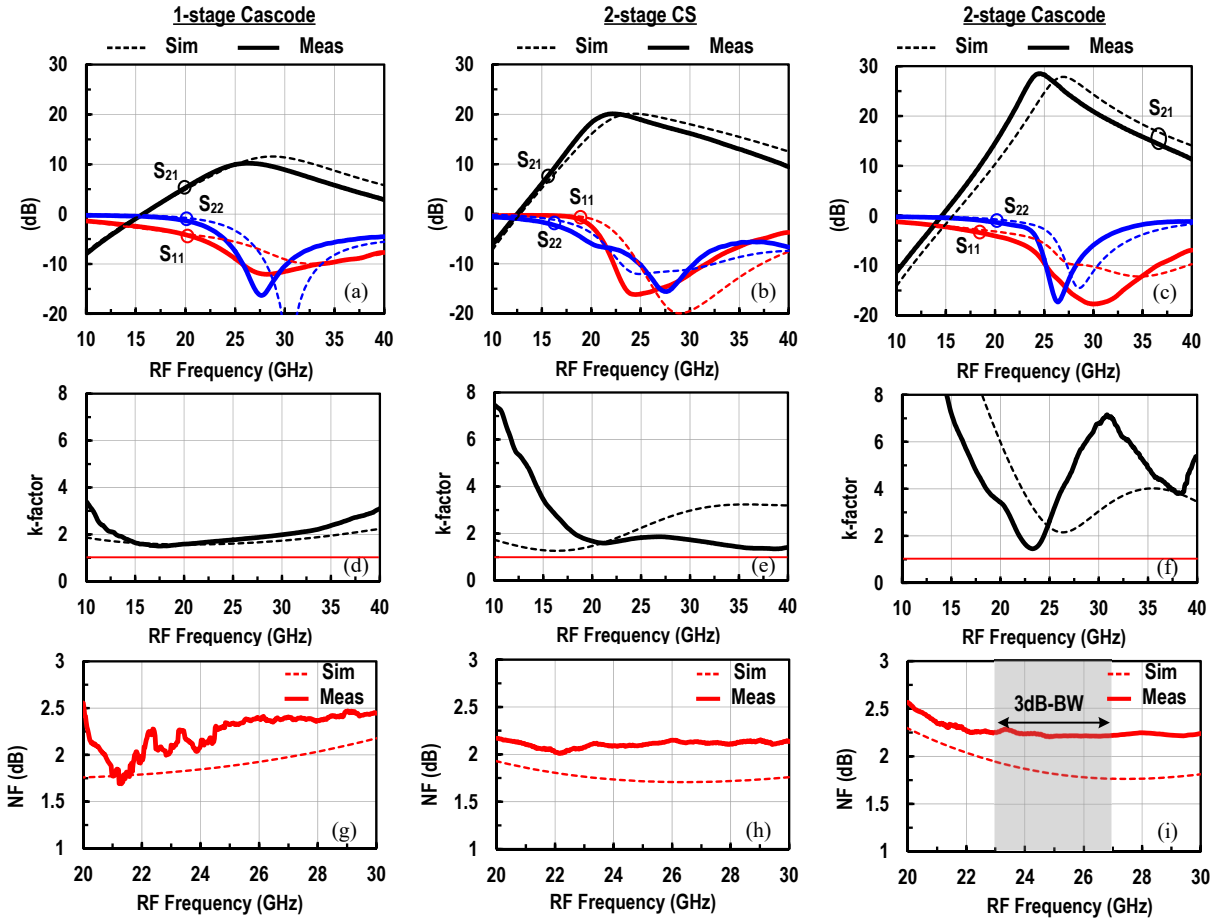

Figure 6.11: Measured and simulated small-signal performance versus frequency for the three fabricated 5G LNAs: (a, b, c) S-parameters for the nominal operation: $V_{DD,CS}$ = 0.8 V with 9.6 mW and $V_{DD,CAS}$ = 1.6 V with 15 mW for the singe-stage, and 20 mW for the 2-stage design. (d, e, f) k-factors. (g, h, i) NF.

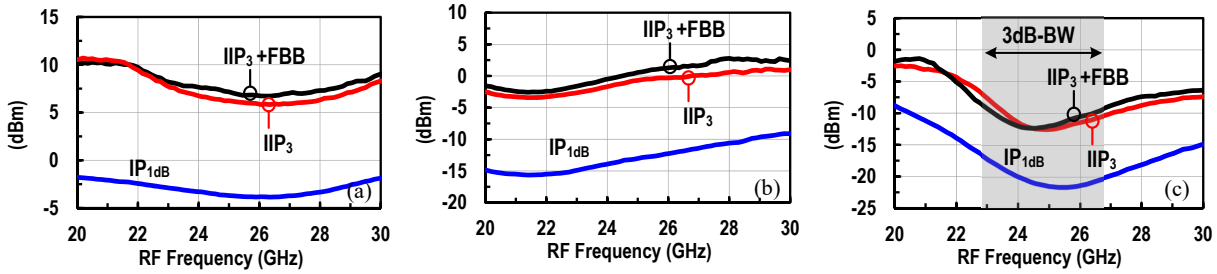

Figure 6.12: Measured linearity across frequency for the three fabricated LNAs: IP_{1dB} and IIP_3 with and without FBB while fixing P_{DC}. (a) 1-stage CAS with 9.6 mW, (b) 2-stage CS with 15 mW, and (c) 2-stage CAS with 20 mW.

metal fill is a possible reason for this discrepancy.

The measured IP_{1dB} and in-band IIP_3 are presented in Fig. 6.12. The 1-stage CAS

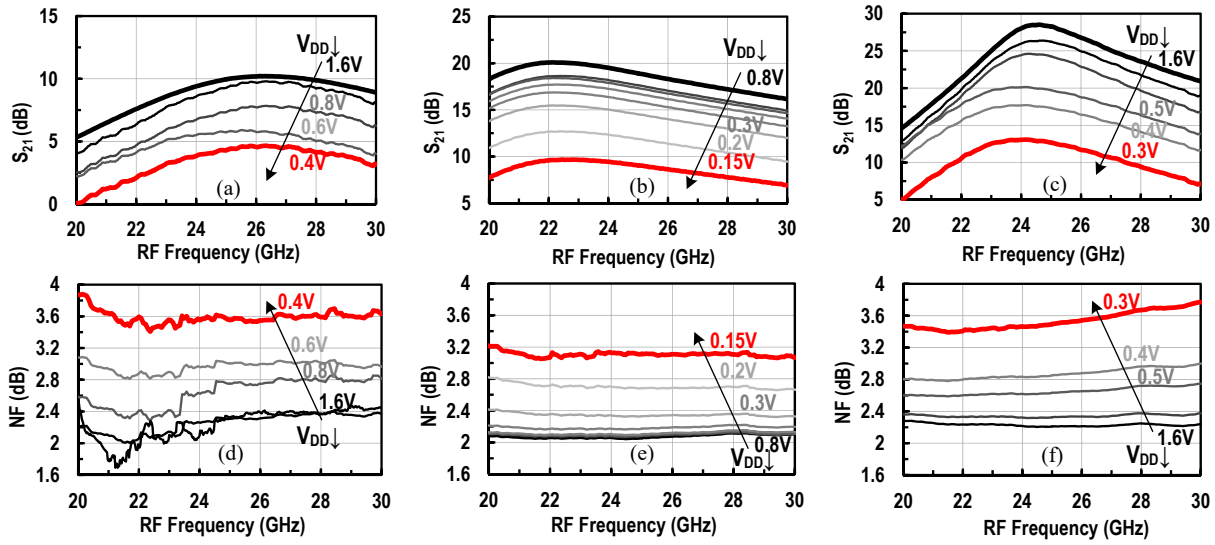

Figure 6.13: Measured gain & *NF* across frequency for different V_{DD} values: (a, d) 1-stage CAS, (b, e) 2-stage CS, and (c, f) 2-stage CAS.

achieves an IP_{1dB}/ IIP_3 > -3.5/ +7 dBm across the 3dB-BW. For the 2-stage designs, an IIP_3 of +2.6 and -10.4 dBm, is measured, respectively, for the CS and CAS designs when FBB is applied. The FBB enhances the IIP_3 of the 1-stage CAS and 2-stage CS designs by $\sim$ 2.5 dB for the same power consumption due to the linearity improvement of the output conductance. This improvement is not visible for the 2-stage CAS when the gain of the input stage exceeds 10 dB. In that case, the IIP_3 linearity is dominated by the swing at the input of the second stage rather than its output (Fig. 6.12(c)).

The operation at low power is studied by stepping down V_{DD} and re-measuring the gain and *NF* (Fig. 6.13). The FBB is used when V_{DD} is $\leq$ 0.5 and $\leq$ 1 V for the CS and CAS designs, respectively. All LNAs maintain the same gain shape for a reduced V_{DD} with the 2-stage CS-LNA achieving 12 dB gain at 0.2 V, and the 2-stage CAS-LNA achieves 17.7 dB at 0.4 V when FBB is used (Fig. 6.13(b, c)). For the 2-stage designs, the measured NF across the 3dB-BW is below 2.8 and 3 dB, respectively, for the CS and CAS LNAs using 0.2 V and 0.4 V supplies (Fig. 6.13(e, f)). This value increases to 3.6 dB for the 1-stage LNA due to the gain degradation to 4.8 dB (Fig. 6.13(a & d)).

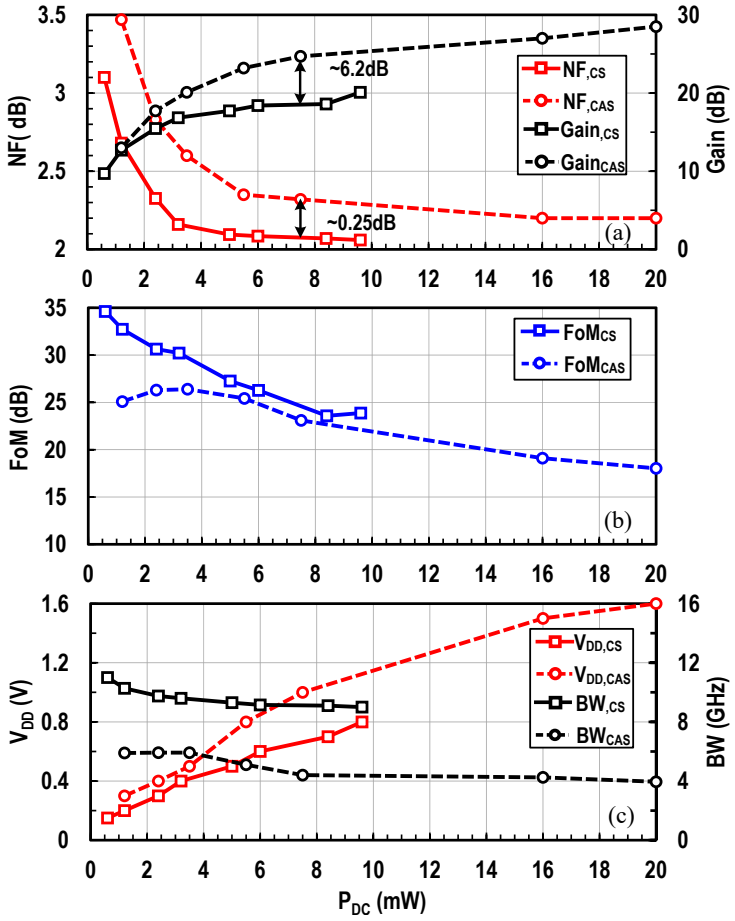

Figure 6.14: (a) Measured performance across P_{DC} for the 2-stage LNAs: (a) *NF* & gain, (b) *FoM*, and (c) 3dB-BW and V_{DD}. FBB (0-2V) is used for $V_{DD} < 0.5$, and < 1 V, for the CS and CAS-LNAs, respectively, to improve *NF* and *FoM*.

In order to analyze the low power operation, the measured peak gain, *NF*, 3dB-BW, and the calculated Figure-of-Merit (*FoM*) for the two 2-stage 5G LNAs are presented versus DC power consumption (Fig. 6.14). The CS design achieves 12 dB gain and sub-3 dB *NF* when P_{DC} is only 1 mW (V_{DD}= 0.2 V). Sub-3 dB *NF* operation is achieved for the CAS-LNA at 0.4 V/2.4 mW with 17.7 dB of gain. For the same 7.5 mW, the CAS-LNA achieves 25 dB gain, which is 6.2 dB higher than the CS-LNA, while the *NF* is 2.32 dB (and is only 0.23 dB higher than the CS-LNA), as predicted from Fig. 6.6(c). The CAS design, however, has nearly half the BW of the CS one. It is thus useful to compare their *FoM*s across DC power levels which considers the BW in addition to the gain and *NF* (Fig. 6.14(b)).

Both 2-stage LNAs achieve excellent *FoM*s >20 dB across most of their operation range. The *FoM* increases as P_{DC} is reduced since the gain and *NF* improvement saturate for higher power levels. The two LNAs have comparable *FoM*s of 24-28 dB at 5-10 mW with the CAS-LNA favoring the gain while the CS-LNA favoring the ULV operation, BW, and slight *NF* improvement.

Table 6.1 summarizes the performance of the three FBB-LNAs and presents a comparison with published silicon-based K/Ka-band LNAs. To the authors knowledge, the single-stage CAS LNA demonstrates the highest in-band IIP_3 for a 10 dB gain 5G LNA. The 2-stage CS-LNA reports the highest *FoM*, the lowest V_{DD} and P_{DC} in the K/Ka-band with more than 9 GHz of BW and state-of-the-art sub-2.2 dB mean-*NF*. The 2-stage CAS-LNA has the same 28.5 dB peak-gain as in [77] but with 4 $\times$ less P_{DC} and 1.15 dB less mean-*NF*. In the low-power mode, the 2-stage CAS-LNA has the highest reported gain of 23.2 dB for a 5 mW design with a $NF < 2.4$ dB.

6.7 Conclusion

This work detailed the design and measurement of mm-wave 5G K/Ka band FBB LNAs in 22nm FDSOI. Three LNAs targeting high linearity, low noise, and high gain, respectively, and exploiting the FBB feature were presented. The FBB effect is studied and applied to improve the performance under scaled V_{DD} and P_{DC} for CS and CAS-LNAs. The single-stage CAS-design reports the highest IIP_3 for a CMOS LNA operating at 28 GHz, while the 2-stage LNAs deliver state-of-the-art sub-2.4 dB mean NF in low power mode (3.2 mW for CS-LNA and 5.5 mW for CAS-LNA) with an *FoM* over 25 dB. Such performance can improve current 5G K/Ka-band phased-array front-ends.

Table 6.1: Comparison with K/Ka band mm-waves LNAs

Design	This Work			[77] Chen RFIC'18	[78] Kanar TMTT'14	[79] El-Nozahi JSSC'10	[86] Zhang RFIC'19	[81] Lo TMTT'11	[95] Ma TMTT'15	[83] Kodak TMTT'19	[80] Cui RFIC'19	[85] Li IMS'18
Technology	22nm FDSOI			0.25µm SiGe	0.18µm SiGe	0.18µm SiGe	22nm FDSOI	0.18µm CMOS	0.25µm SiGe	45nm RFSOI	22nm FDSOI	45nm RFSOI
Topology	1-stage CAS	2-stage CS	2-stage CAS	Diff. 2-stage CAS	2-stage CS-CAS	2-stage CAS-CS	1-stage CAS	3-stage CG-2CS	3-stage 2CAS-CS	1-stage CAS	2-stage CS-CAS	1-stage CAS
Frequency (GHz)	21.6-32.8	19.5-29	23-27	29-37	16-24	23-32	19-34	14.3-29.3	25-34	23-34	19-36	14-31
V_{DD} (V)	0.8/1.6	0.4/0.8	0.8/1.6	2	1.8	1.5	1.3	0.8-1.2	2.5-1.2	1.5	1.05	1.6
DC Power (mW)	6/15	3.2/9.6	5.5/20	80	22.5	13	9.8	13.9	133	12	17.3	15
Peak Gain (dB)	7.8/10.2	16.9/20.1	23.2/28.5	28.5	19.0	12	12	9.9	26.4	8.5	21.5	12.8
3dB-BW (GHz)	11.6/11.2	9.6/9	5.1/3.95	8	8	9	15	15	9	11	17	17
NF[#] (dB)	2.65/2.2	2.18/2.08	2.38/2.25	3.4	2.2	5	1.55[&]	5	2.5	2.7	2[&]	1.4
FoM (dB)	15/11.2	30.1/23.7	25.2/18	7.0	13.6	2.1	23	3.9	1.8	9	26	22.3
IIP_3[*] (dBm)	+7.5 @ 28GHz	+2.6 @ 28GHz	-10.4 @ 26GHz	-12.5 @ 32GHz	-15.5 @ 20GHz	-6.2 @ 28GHz	+3 @ 28GHz	-2 @ 24GHz	-5 @ 30GHz	N.R.	-13.4 @ 22GHz	+5 @ 28 GHz
IP_{1dB}[*] (dBm)	-3 @ 28GHz	-10.2 @ 28GHz	-21 @ 26GHz	N.R.	-4 @ 20GHz	N.R.	-7.6 @ 28GHz	-12 @ 24GHz	-14.9 @ 30GHz	-3 @ 28GHz	N.R.	-5 @ 28GHz
OIP_3/ DC Power	3.7	10.66	1.95	0.5	1.4	0.29	3.23	0.3	1	N.R.	0.37	3.2
Core Area (mm^2)	0.12	0.19	0.19	0.21	0.25	0.25	0.12	0.54[^]	0.165	0.15	0.05	0.3[^]

N.R.= Not Reported

[*] High power mode

[^] Including pads

[1] $FoM = 20log_{10}\left(\frac{Gain[lin.]\times BW[GHz]}{P_{DC}[mW]\times(NF[lin.]-1)}\right)$

[#] Mean value within the 3dB-BW

[&] Estimated from plots

6.8 Acknowledgment

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Chapter 7

A 350 mV Complementary 4-5 GHz VCO based on a 4-Port Transformer Resonator with 195.8 dBc/Hz Peak FOM in 22nm FDSOI

7.1 Introduction

The advancements in ultra low voltage and power (ULV/P) circuit techniques enable near battery-free energy harvesting and IoE applications. In these systems, the phase noise (PN) requirements are generally relaxed, and efficient ULV/P operation sets the target for LC oscillators. The figure-of-merit (FOM) is, thus, the parameter to be optimized rather than the PN. The peak FOM can be expressed as [104]:

$$\mathrm{FOM_{MAX}} \propto 20\log(\mathrm{Q}) + 10\log(\eta) + 10\log(1 + \alpha/\mathrm{Av}), \tag{7.1}$$

where Q is the effective tank quality factor and is primarily dependent on the technology, η is the DC-to-RF efficiency (P_{RF}/P_{DC}) which can be optimized by waveform engineering for minimum I/V overlap in switching FETs, α is the effective transconductor current noise shaped by the impulse sensitivity-fuction (Γ), and Av is the voltage gain across the transconductor which can suppress device noise contribution for high Av values. High Av values are usually achieved using a step-up transformer between the drain and gate of the transconductor in high-performance low-PN NMOS topologies [105]. The gate voltage swing, however, greatly surpasses $2V_{DD}$ posing reliability concerns and forcing the usage of thick-oxide core devices which limit the loop gain, η, and the tuning range. Reducing V_{DD} to reliable levels results in a reduced loop gain and penalizes the PN and FOM [106].

In this work, we propose a reliable and ULV/P complementary VCO suitable for energy harvesting IoE applications when V_{DD} is < 400mV and P_{DC} is < 0.5mW while maintaining an excellent FOM of 192-195.8dBc/Hz across the achieved 20% continuous tuning range.

7.2 Complementary VCO design

We first consider the CMOS VCO with implicit common-mode (CM) resonance where an NMOS and a PMOS VCOs with identical tanks are tied from their center-tap to form a CMOS structure [104] (Fig. 7.1(a)). A complementary VCO topology is favored over NMOS or PMOS-only in ULP applications since it results in $\sim 4\times$ less P_{DC} for the same tank (and 6-dB higher PN) under the same FOM. The CMOS topology maintains the CM resonance around the second harmonic ($2F_{LO}$) of individual tanks resulting in a smaller effective impulse-sensitivity-function (Γ_{eff}) and PN, while improving the current efficiency at the expense of the achieved voltage swing. The structure achieves an FOM up-to-196dBc/Hz with 0.5mW P_{DC}, however a V_{DD} of 0.7V is needed to accommodate the complementary operation and reliable start-up, which is not feasible in harvesting systems.

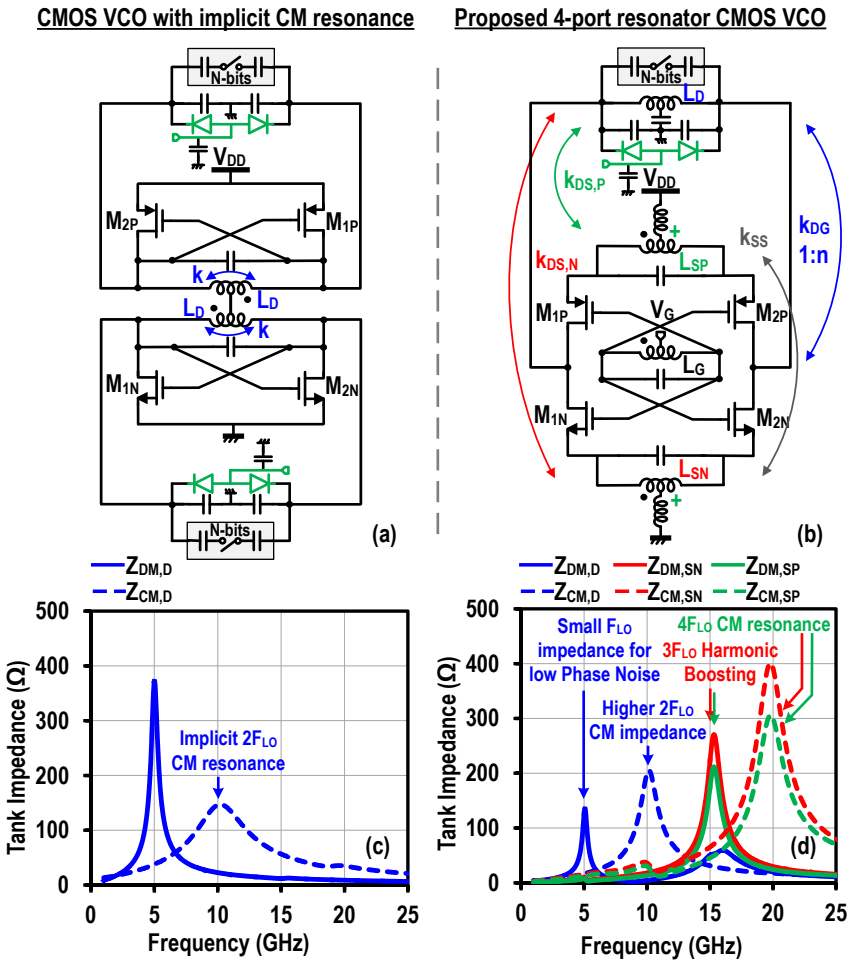

Figure 7.1: A CMOS VCO with implicit CM resonance and its composite tank impedance (a & c); Proposed CMOS VCO based on a 4-port resonator and its composite tank impedance (b & d).

By modifying the two similar tanks to form a single step-up class-F_{23} transformer [105], between the drains and gates of the CMOS transconductors ($gm_{N/P}$), the resonator becomes a 2-port network and FOM_{MAX} can be improved by up-to 2.2dB [104] (Fig. 7.1(b)). The drain swing is half that of an NMOS only topology so thin-oxide devices can be used for better start-up and η. The source feedback paths between $L_D/L_{SN/P}$ and L_{SN}/L_{SP} are used for gain boosting and $3F_{LO}$ harmonic shaping for higher η and lower PN. The $L_{SN/P}$ inductors allow voltage swings lower than ground and above V_{DD} for higher gm, and thus, the swing on the main tank is maximized.

The class-F_{23} tank generates a higher CM impedance at $2F_{LO}$ for less PN compared to the implicit CM resonance, and generally requires dedicated CM tuning in addition to DM

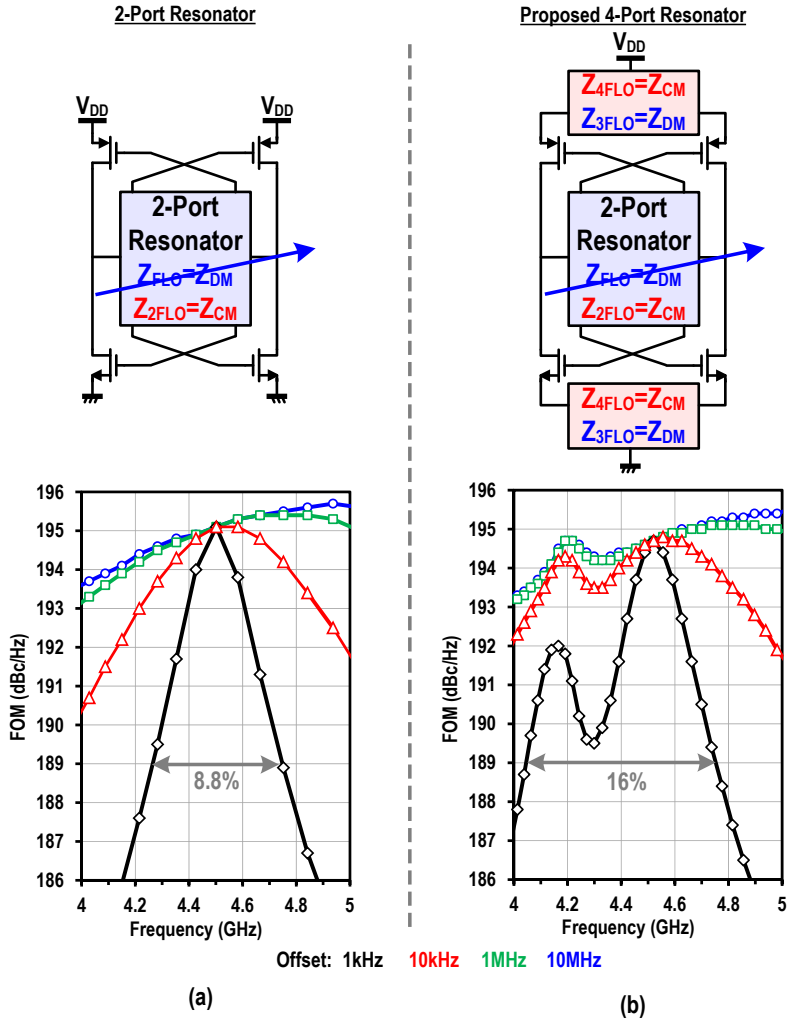

Figure 7.2: Simulated FOM at different frequency offsets across the fundamental tuning range for (a) a 2-port resonator design, compared to (b) the proposed 4-port resonator design.

(differential mode) tuning by controlling the ratio of differential to single-ended capacitors at the L_D side. In this design, however, the source feedback transformer is adjusted to provide a CM resonance around $4F_{LO}$ for both NMOS and PMOS. The CM resonance at $4F_{LO}$ is generally broad since it is limited by the finite Q of the capacitors and does not alter the CM $2F_{LO}$ resonance at the L_D side. The $4F_{LO}$ resonance slightly improves the PN, supply pushing, and renders the VCO less sensitive to CM tuning across the operating frequency range.

Fig. 7.2 compares the FOM at different offsets for a CMOS oscillator with a 2-port resonator versus the proposed 4-port resonator. For both designs, only the main tank differential

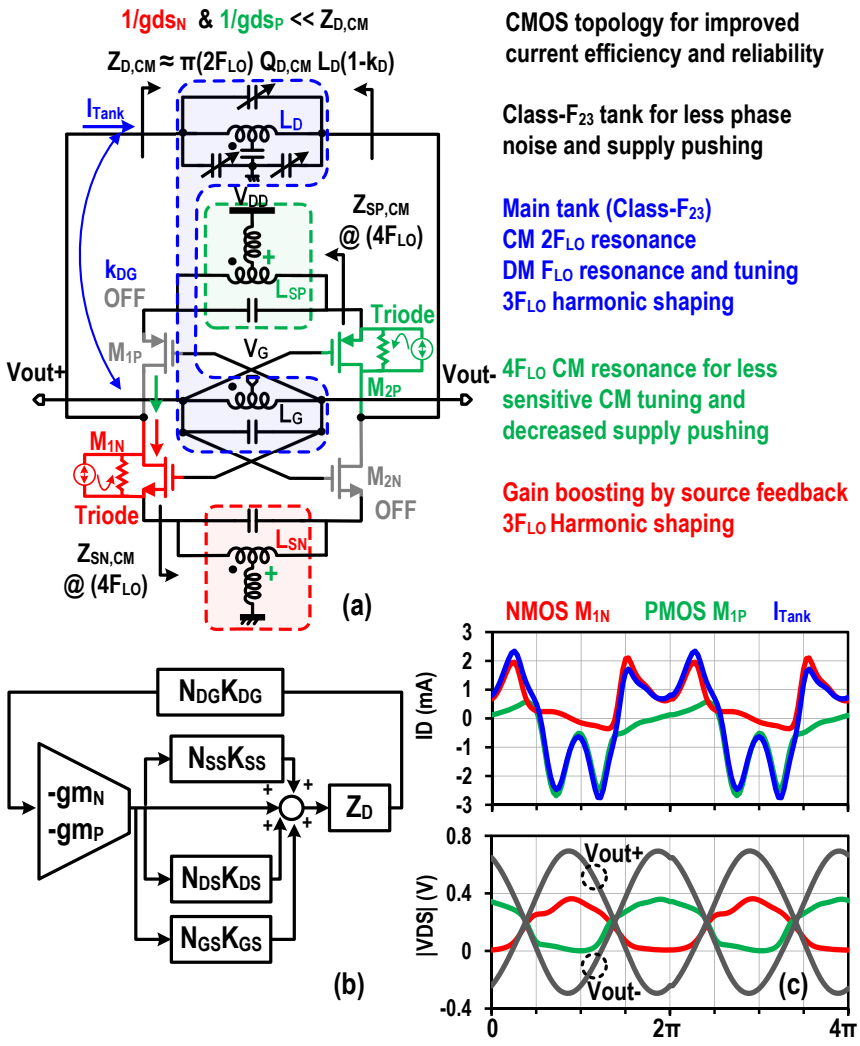

Figure 7.3: (a) VCO switching mechanism. (b) Block diagram for the DM of operation. (c) Simulated time domain waveforms at 0.35V supply: drain tank current, drain-to-source current and voltage for both NMOS and PMOS, and output gate voltage.

capacitors bank is used to change the frequency without changing the common mode impedance resonance. In case of a 2-port resonator, Z_{CM} does not track the fundamental tuning and the FOM quickly degrades across the tuning range (Fig. 7.2(a)). Alternatively, the $4F_{LO}$ resonance for the 4-port resonator allows *FOMengineering* across the tuning range with no dedicated tuning for the CM.

Several feedback mechanisms (Fig. 7.3(b)) improve the DM loop gain and allow the VCO to operate from a V_{DD}=0.35V (half of the CMOS design with implicit CM resonance in [104]

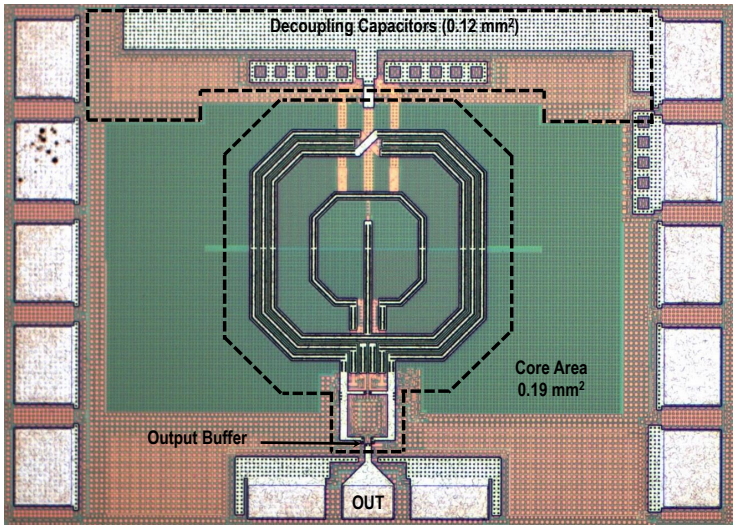

Figure 7.4: Die micrograph of the fabricated CMOS VCO chip in 22nm FDSOI.

with nearly same PN and FOM). Under large signal swing, the CM resonance at the L_D side forces the noise of the triode NMOS/PMOS to circulate inside their channel resistance instead of reaching the main tank (Fig. 7.3(a)). The push-pull structure ensures voltage reliability, and improves the tank current efficiency (where current is either pushed-in or pulled-from the main tank each half cycle). Also, the gate swing is $\sim$ 1V peak-to-peak to provide rail-to-rail drive for the on-chip buffer to reduce its power consumption (Fig. 7.3(c)).

7.3 Implementation

The CMOS VCO is fabricated in GlobalFoundries 22nm FDSOI with a core area of 0.19 mm^2 (Fig. 7.4). Thin-oxide low-VT devices are used in the VCO core to provide large loop gain, reliable start-up and better PN performance in the thermal region. The 4-winding transformer, shown in Fig. 7.5(a), is implemented on the top 3 metal layers (a 2.9μm aluminum and two 3μm copper layers). The coupled windings L_G and L_D are implemented in a planar fashion while tying the two upper metals together. In addition to lowering the series resistance, this is particularly useful in reducing the mandatory metal fill imposed by the technology in the upper metal layers

which can reduce Q. The source windings L_{SN} and L_{SP} form a single turn broadside transformer with k≈0.75 at 5 GHz. The center taps, for the supply and ground nodes, are realized from the same side for minimum current return path and easy decoupling. A patterned ground plane is added on the lowest metals to act as a shield from the low resistivity substrate ($\rho \approx 7\Omega$-cm). EM-structures are modeled using IntegrandâĂŹs EMX simulation software. The EM-simulated Q of L_G, L_D, L_{SN}, and L_{SP}, are 11.1, 11.6, 15, and 12.7, respectively, at 5 GHz.

The VCO is combined with a 3-bit differential switched capacitors bank and thick-oxide N-varactors placed in parallel with the drain tank for discrete and continuous tuning. The drain side (L_D) CM resonance minimizes AM-PM noise conversion from the varactor, while the lower swing (compared to L_G side) allows the usage of thin-oxide NMOS switches in the capacitors bank for their lower $R_{ON}C_{OFF}$. The switched capacitors are controlled by two digital supply levels to minimize R_{ON}, in the ON-state, and avoid accidental switch turn-on, in the OFF-state, while ensuring reliable voltage swing across the the thin switches (Fig. 7.5(b)).

7.4 Measurement Results

A signal source analyzer (Keysight E5052B) is used for frequency, PN, and power measurements. The analyzer output DC power port is used as the VCO supply to accurately measure the supply current and the supply voltage frequency pushing. The pseudo-differential output buffer has one output terminated on-chip and the other one is RF probed through a GSG pad. The rest of the biasing and controls are provided from a dedicated LDOs board. The CMOS VCO achieves a continuous tuning range of 20% from 4.06-to-4.96 GHz with $>$ 40% bands overlap and a VCO gain (K_{VCO}) from 120-to-340 MHz/V (Fig. 7.5(c)).

The PN and FOM are plotted in Fig. 7.6 versus the offset frequency for the highest (F_{MAX}=4.91 GHz), and lowest (F_{MIN}=4.15 GHz) bands when using a 350mV supply. At F_{MAX}, the VCO achieves a PN of -137.7, -116.6, and -91.6 dBc/Hz at 10MHz, 1MHz, and 100kHz

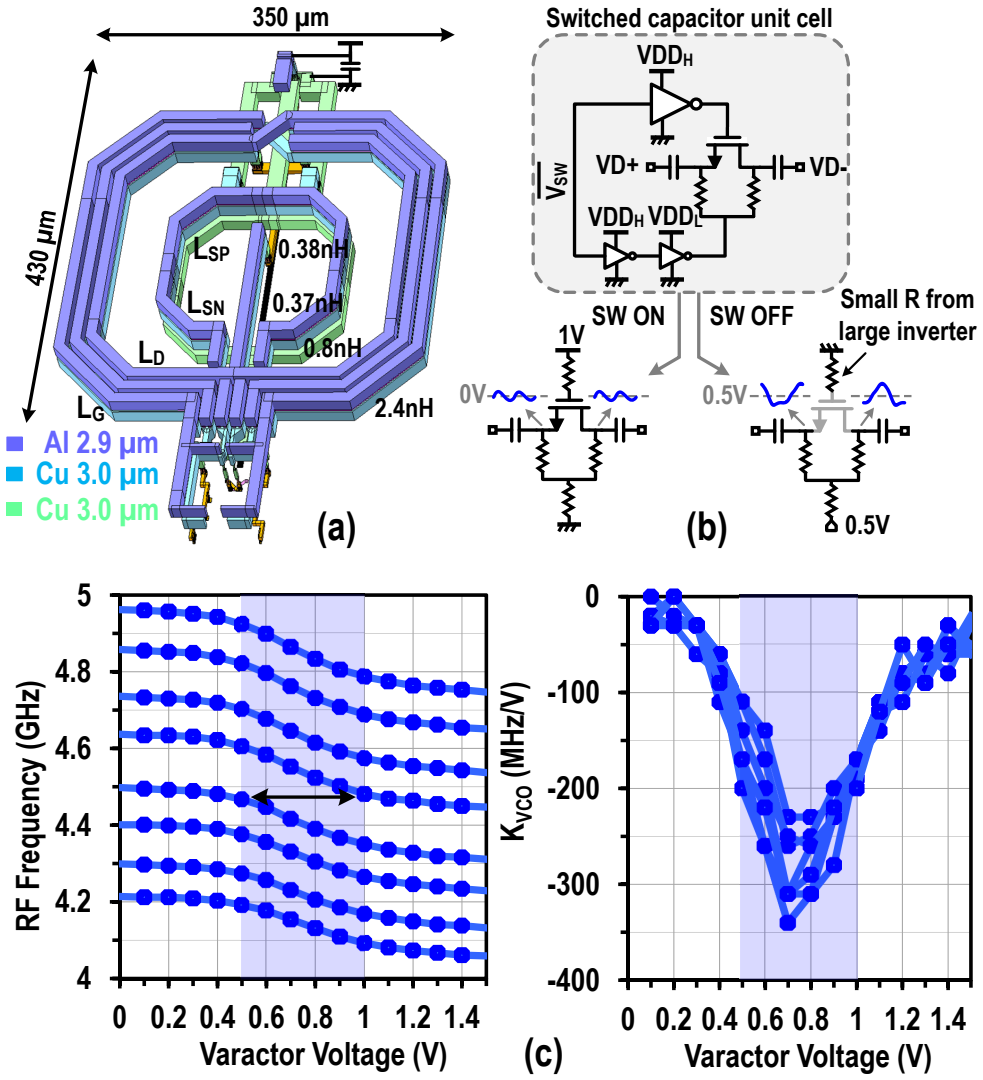

Figure 7.5: (a) 4-port transformer based resonator layout. (b) Switched capacitor unit cell and its biasing scheme in ON and OFF states. (c) Measured tuning curves and VCO gain (K_{VCO}).

frequency offsets, respectively, while dissipating $<$ 0.42 mW. The peak FOM is 195.8 dBc/Hz in the thermal region and better than 195, 194, and 190.5 dBc/Hz at 10MHz, 1MHz, and 100kHz offsets, respectively. The flicker corner frequency, where the FOM is 3-dB lower than the peak value, is 250 kHz. The simulated flicker corner for low-VT thin-SOI FETs is between 5 and 10MHz, showing, thus, the effect of the CM resonance on close-in VCO PN and FOM improvement in deeply-scaled technology nodes. At F_{MIN}, with a 0.44 mW P_{DC}, the flicker-corner is 100kHz, while the peak FOM is reduced due to the decreased tank impedance (loop gain) and

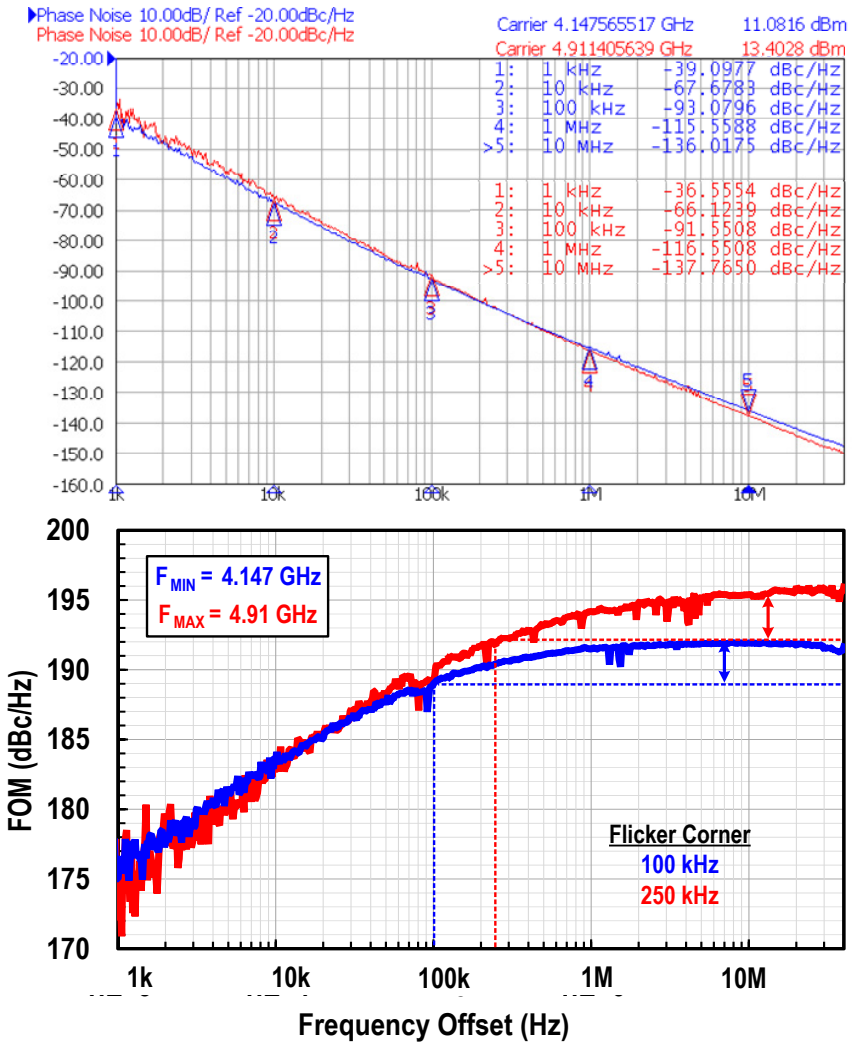

Figure 7.6: Measured phase noise and FOM versus offset frequency for the high band (red) and the low band (blue) at 0.35V supply.

the loading of the capacitors bank switches, but remains better than 192 dBc/Hz with a PN of -136 dBc/Hz at 10 MHz offset.

The PN and FOM (P_{DC}) are measured across the tuning range while keeping the varactor bias at 0V for the smallest K_{VCO} (Fig. 7.7(a & c)). The results are consistent with F_{MAX} and F_{MIN} measurements, where the PN and FOM are most improved near the high band, when the loop gain is high, while the flicker corner is most reduced near the lower band. The flicker corner is always better than 250kHz without employing a dedicated CM tuning capacitors bank, which

needs to be single ended and thus more lossy. This is attributed to the extra $4F_{LO}$ CM resonance at the source nodes which is inherently low Q. In addition, the gate bias, separated from the supply node, provides an extra degree of freedom to minimize both FETs flicker up-conversion by reducing the DC component of Γ_{eff}. This is done by modifying the noise-modulation-function of both FETs to ensure symmetry and is simply obtained by changing the V_G bias.

The varactor effect on the PN and FOM is separately studied at F_{MAX} and F_{MIN} while fixing V_G in Fig. 7.7(b & d). As expected, the FOM is most sensitive at large K_{VCO} values but remains better than 190 dBc/Hz at 1MHz offset across the frequency range. Adding extra bits in the capacitors bank can yield less varactor impact.

A drawback in the typical CMOS cross-coupled VCO is the high frequency pushing (supply sensitivity). The 4-port transformer in this design decouples the voltage-dependent gate-to-source capacitance (C_{gs}) of the NMOS from the supply variation and results in less pushing. Also, the supply inductor, L_{SP}, with a CM resonance at 4LO provides complementary frequency pushing reduction. The measured pushing is < 60 MHz/V for the high band when sweeping V_{DD} from 300-to-400mV (Fig. 7.8). For the low band, the minimum V_{DD} is increased to 325mV to cope with gain reduction and the measured pushing is < 80 MHz/V when sweeping to 425mV.

Table 7.1 compares the 4-port resonator-based CMOS VCO with state-of-the art low-power oscillators. The VCO achieves the lowest PN and highest FOM for sub-0.5mW oscillators. The VCO has also the lowest V_{DD} (350mV) for published complementary designs. The proposed design delivers nearly the same PN and FOM performance as the CMOS VCO with implicit CM resonance in [104] with half the supply voltage and 45% more tuning range while abiding by the metal filling and reliable voltage limits of the technology rules. The inverse Class-F design [107] shows slightly higher FOM but a $3\times$ higher P_{DC} and with two separate capacitor banks to simultaneously tune DM and CM resonances, with one capacitors bank placed between the high swing gate nodes. The folded design in [7] operates from only 100mV supply but has a slightly lower FOM for 0.5mW P_{DC} and a larger chip area.

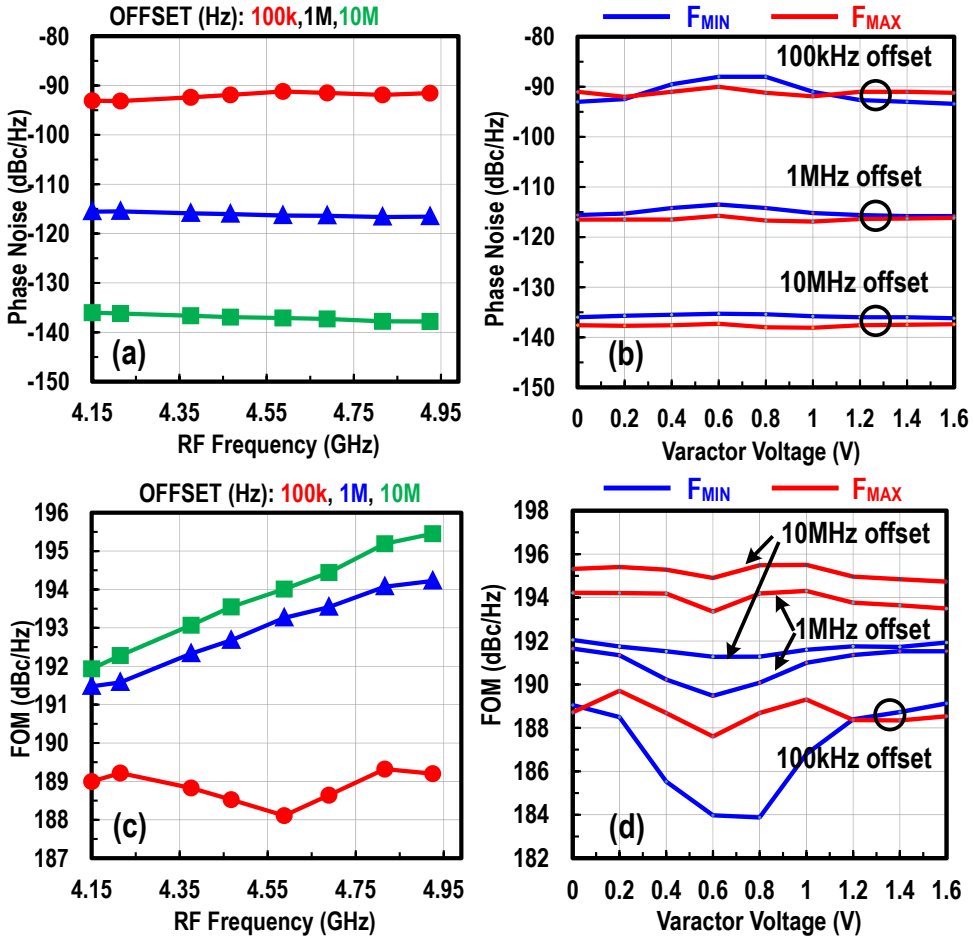

Figure 7.7: Measured phase noise and FOM versus oscillation frequency (a & c); and versus the varactor tuning voltage for the upper and lower bands (b & d) at 100k, 1M, and 10MHz offsets for a 0.35V supply.

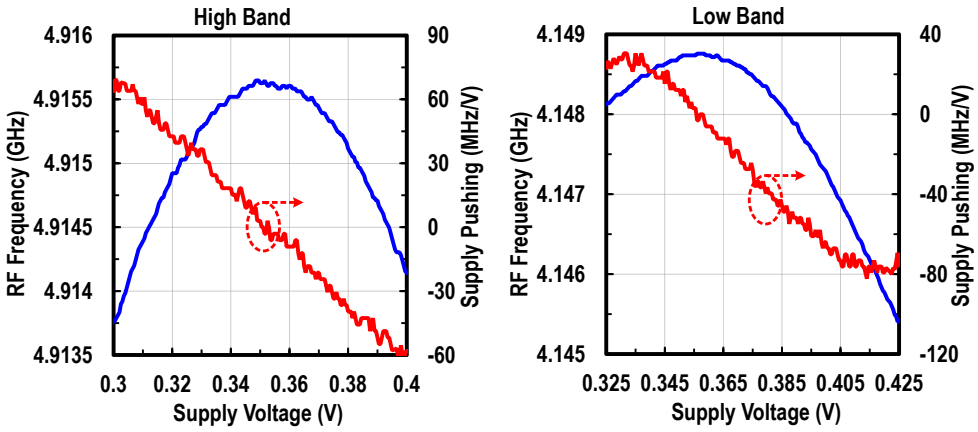

Figure 7.8: (a) Measured frequency pushing for the highest and lowest bands.

Table 7.1: Comparison with state-of-the-art low-power oscillators

Design			**This Work**	**[104] JSSC'17**	**[107] ISSCC'18**	**[7] ISSCC'19**	
Topology			CMOS 4-port resonator	CMOS CM resonance	CMOS Inverse Class-F	CMOS Folded	
Technology process			22nm FDSOI	28nm	65nm	22nm FDSOI	
Frequency (GHz)			4.06-4.96	4.7-5.4	3.49-4.51	4.15-4.97	
Tuning Range (%)			20%	13.8%	25.5%	18%	
VDD (V)			0.35	0.7	0.6	0.2	0.1
Power (mW) @ f_{min} / f_{max}			**0.44/0.415**	0.5	1.2/1.14	2.28/ 1.77	0.54/ 0.46
Phase noise (dBc/Hz)	**@ 100 kHz**	f_{min}	-93.1/ -91.6	-91.5#/ -92#	-102.4/ -98.5	-100/ -96.1	-91.3/ -92.3
		f_{max}					
	@ 10 MHz	f_{min}	-136/ -137.8	-139#/ -137#	-145.6/ -143.7	-142.2/ -144.3	-133/ -136.5
		f_{max}					
FOM (dBc/Hz)	**@ 100 kHz**	f_{min}	189/ 189.2	188*/ 187.5*	192.5/ 191	188.9/ 187.6	186.4/ 189.6
		f_{max}					
	@ 10 MHz	f_{min}	**192/ 195.5**	195.6*/ 194*	195.6/ 196.2	191/ 195.8	188/ 193.7
		f_{max}					
1/f^3 Corner (kHz)			100-250	160-400*	100-300	70-700	50-180
Frequency pushing (MHz/V)			< 80	N.R.	4.5-15	< 40	
Core Area (mm^2)			0.19	0.18	0.14	0.272	

N.R. = Not Reported
* Estimated from plots
[1] FOM = -PN + 20log$_{10}$(f_o/Δf) -10log(P_{DC}/1mW)
Calculated based on the provided P_{DC}

7.5 Conclusion

This work presented a complementary VCO based on a 4-port transformer resonator. The proposed design combines the advantages of high current efficiency of the CMOS cross-coupled topology and the low supply voltage and PN of the NMOS design while not sacrificing the reliability. The VCO employs CM resonance and DM harmonic shaping for low flicker and improved switching efficiency. A broad $4F_{LO}$ resonance helps maintaining the close-in PN performance across the tuning range with no dedicated tuning for the CM. The prototype, 22nm FDSOI VCO achieves a 195.8 dBc/Hz peak FOM, 20% tuning range from 4.06-to-4.96 GHz,

with < 0.45 mW P_{DC} while operating from a 350mV supply.

7.6 Acknowledgment

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Chapter 7, in full, is a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "A 350mV Complementary 4-5 GHz VCO based on a 4-Port Transformer Resonator with 195.8dBc/Hz Peak FOM in 22nm FDSOI," *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, USA, 2019, pp. 159-162. The dissertation author was the primary investigator and primary author of this paper.

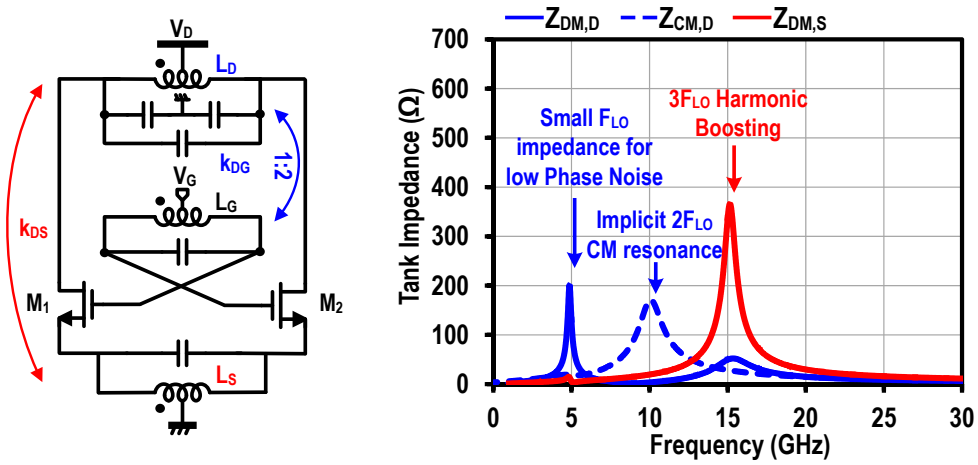
Chapter 8

A 0.1-to-0.2 V Transformer-Based Switched-Mode Folded DCO in 22nm FDSOI with Active Step-Down Impedance Achieving 197 dBc/Hz Peak FoM and 40 MHz/V Frequency Pushing

8.1 Introduction

The continuous improvement in ultra-low-power/voltage (ULP/V) circuits paves the way for new near-battery-free IoE applications. In this work, we propose an LC oscillator that can significantly improve phase noise performance (PN) and figure-of-merit (FOM) at ULV supply levels. The structure is applied to a 4.15-4.97 GHz switched-mode DCO that operates from a supply less than 100 mV and achieves a peak FOM of 197 dBc/Hz at 150 mV supply.

A trifilar-coil oscillator [106] can operate from an ULV supply. The structure benefits



(a) (b)

Figure 8.1: (a) A Class-F_{23} oscillator with source feedback, and (b) its composite tank impedance.

from reduced drain impedance and passive voltage gain, provided by the source feedback and the class-F transformer, to achieve low PN and reliable start-up at 0.4 V. However, at 0.2 V, the PN is penalized from the limited loop gain and voltage swing, and an FOM of 188 dBc/Hz was achieved. For the same headroom, and using N-coupled oscillators, it is possible to decrease the PN by 10log(N) with the same loop gain and FOM at the expense of chip area. Another approach is to reduce the impedance seen by the transistor to achieve a higher power while also increasing the loop gain for reliable start-up.

8.2 Folded Oscillator Design

We first consider a modified version of the trifilar-coil design by modifying the class-F transformer to a class-F_{23} [108], which provides a common mode (CM) resonance around the second harmonic ($2F_{LO}$) [109, 110] at the drain nodes (Fig. 8.1). This is particularly useful in reducing flicker up-conversion while decreasing the impulse sensitivity function (ISF), and results in a lower overall PN.

By adding a common-gate PMOS in a folded-cascode topology (Fig. 8.2), the main tank

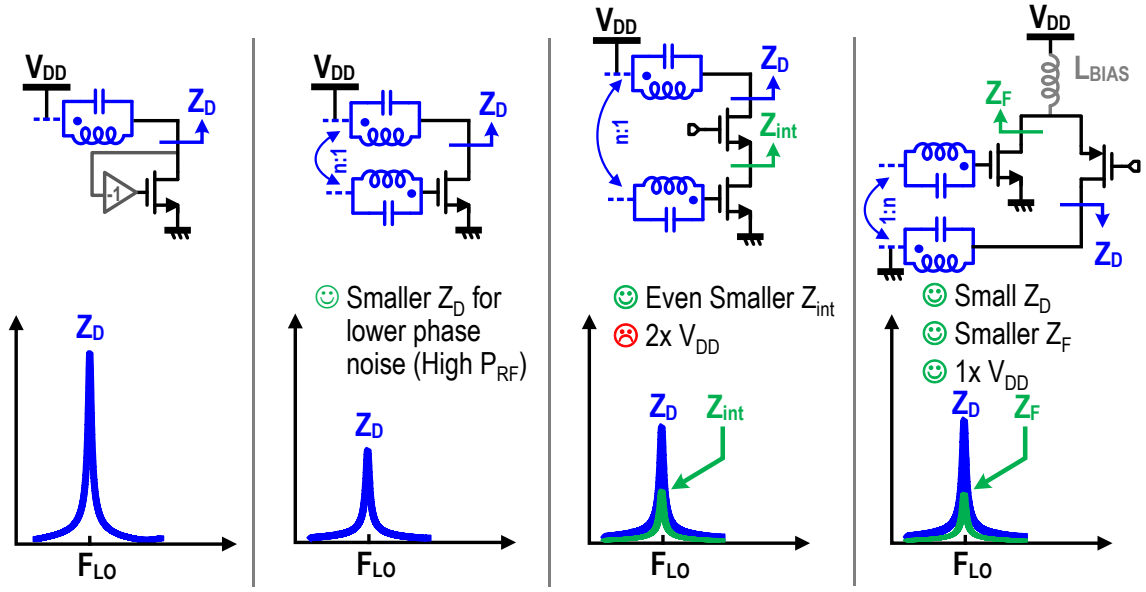


Figure 8.2: DM drain tank impedance for different oscillators topologies.

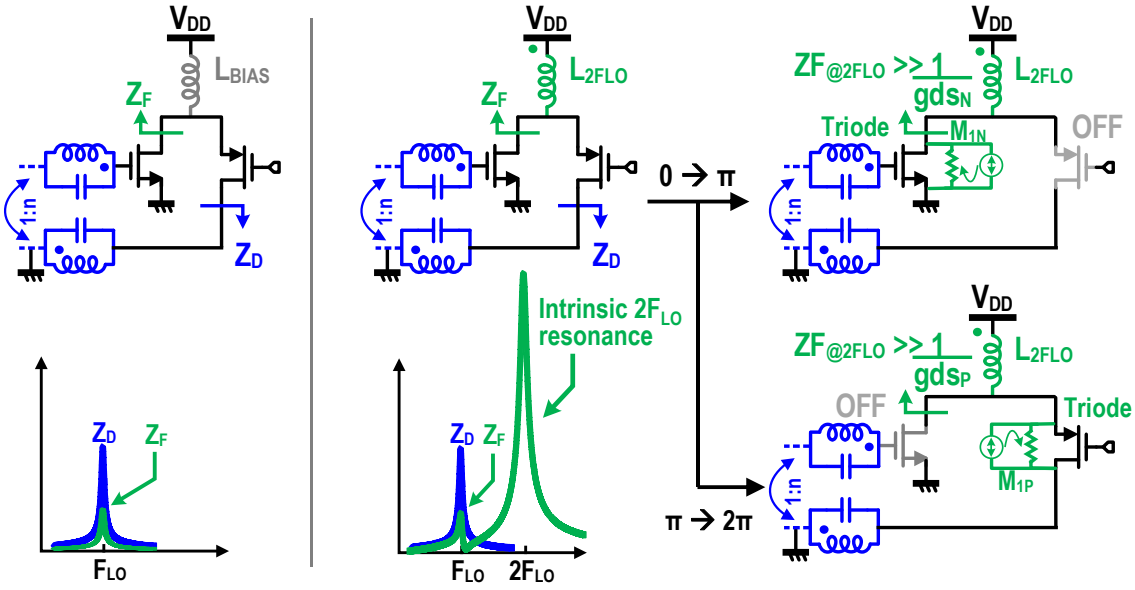


Figure 8.3: Effect of an intrinsic $2F_{LO}$ resonator at the folding node, weakly coupled to the main tank, on impedance and switching mechanism.

impedance (L_D side) can be effectively divided between both NMOS and PMOS devices under the same supply without sacrificing loop gain.

The resonator at the supply/folding node (L_F) is designed to have a high quality factor (Q) intrinsic resonance around $2F_{LO}$ for PN and frequency pushing improvements. A weak positive

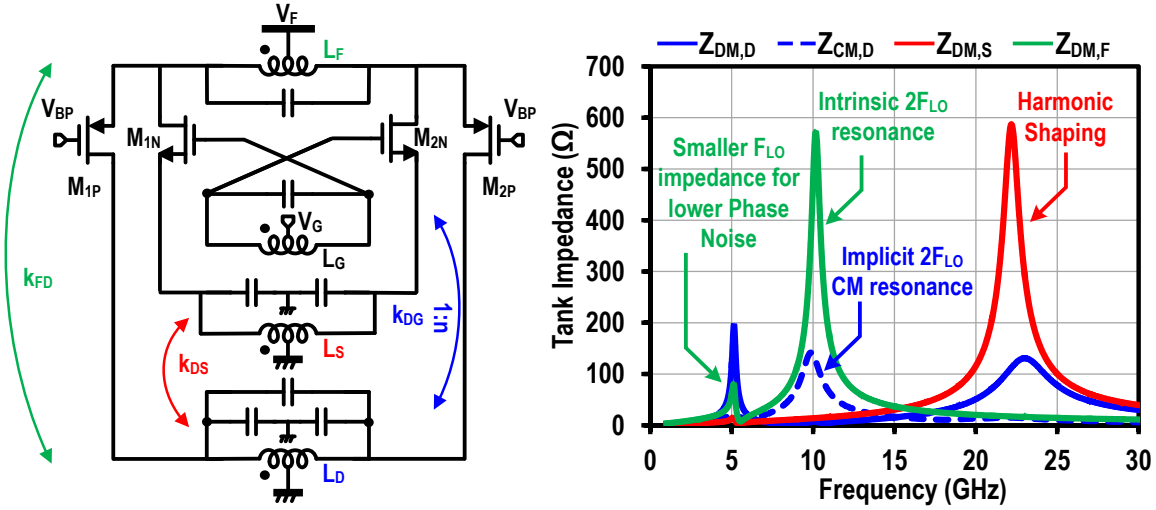


Figure 8.4: (a) Proposed folded oscillator using an intrinsic $2F_{LO}$ resonator at the folding node, and (b) its composite tank impedance.

coupling, k_{FD} (between L_F and L_D), is engineered along with the PMOS transconductance (Gm) to control the swing at the folding node, and thus the impedance division between the NMOS and PMOS devices. Therefore, the single side Gm-cell resembles a *folded-stacked* topology more than a folded-cascode (Fig. 8.3).

The CM resonance at the PMOS drain is preserved by controlling the ratio of the differential to single-ended capacitance at this node. A source feedback resonator L_S is used for gain boosting and harmonic shaping. Instead of aligning the source resonator with $3F_{LO}$, a process similar to the source/load pull in power amplifiers is adopted to maximize the oscillator efficiency. Non-purely real, but adequately high, impedance values at the 4^{th} and 5^{th} harmonics were found to maximize the efficiency for the implemented design (Fig. 8.4).

The maximum FOM theoretical value (FOM_{max}) is dictated by the Q of the passives for a given process. The FOM peaks when the CM resonance is adjusted around 2FLO (Fig. 8.5). There remains, however, an FOM gap, for practical implementations, due to the limited CM resonance Q and the oscillator switching power loss. These two factors are addressed in the switching mechanism of the proposed folded oscillator (Figs. 8.6 and 8.3).

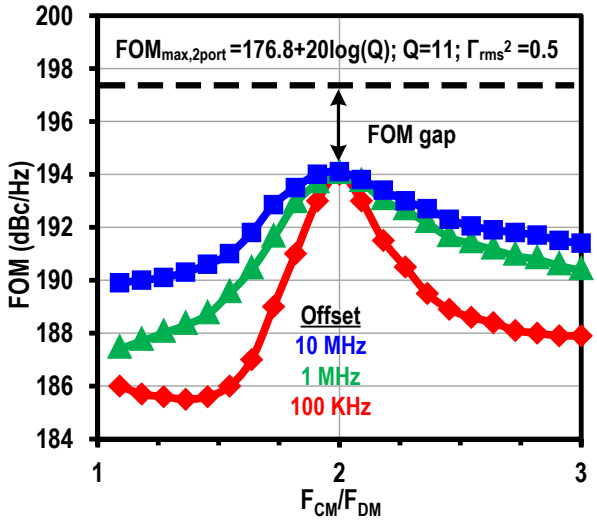


Figure 8.5: Dependence of the FOM on the accuracy of the CM resonance and existence of a FOM gap from sub-optimal operation.

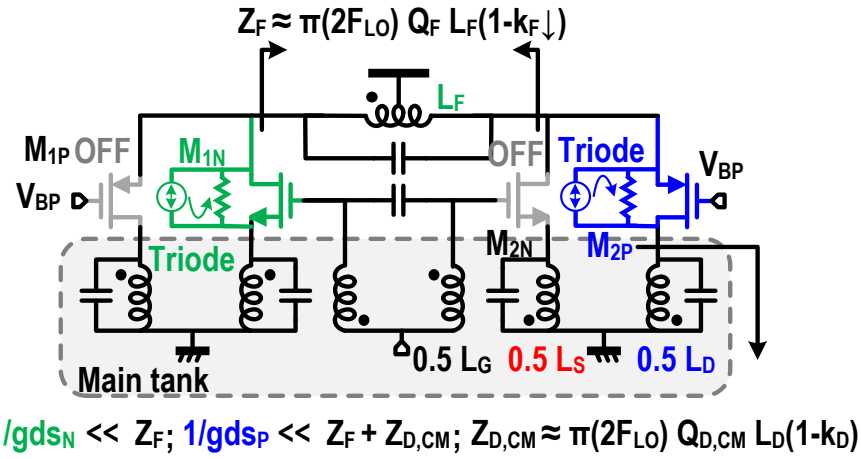


Figure 8.6: Folded oscillator switching mechanism to bridge the FOM gap.

Under large signal swing, both NMOS and PMOS on one side (M_{1N} and M_{1P}) are ON at different halves of the oscillator cycle. When the NMOS is in triode region, an OFF state PMOS prevents the NMOS from de-Qing the main tank (L_D-L_G), while a high-Q resonance at the folding node at $2F_{LO}$ forces the NMOS current noise to circulate in its channel resistance ($1/gds_N$). Similarly, when the PMOS is in triode, the intrinsic $2F_{LO}$ resonance at L_F, in addition to the CM resonance at L_D, minimize the current noise injection in the tank. When both NMOS and PMOS are in saturation, the channel length modulation loading, which is critical for short-channel

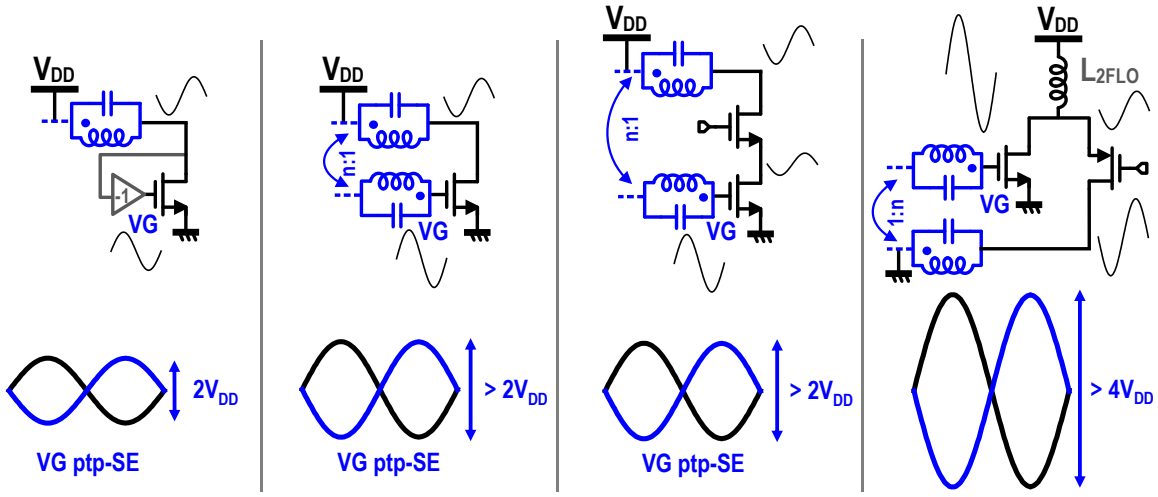


Figure 8.7: Gate voltage swing for different oscillators topologies.

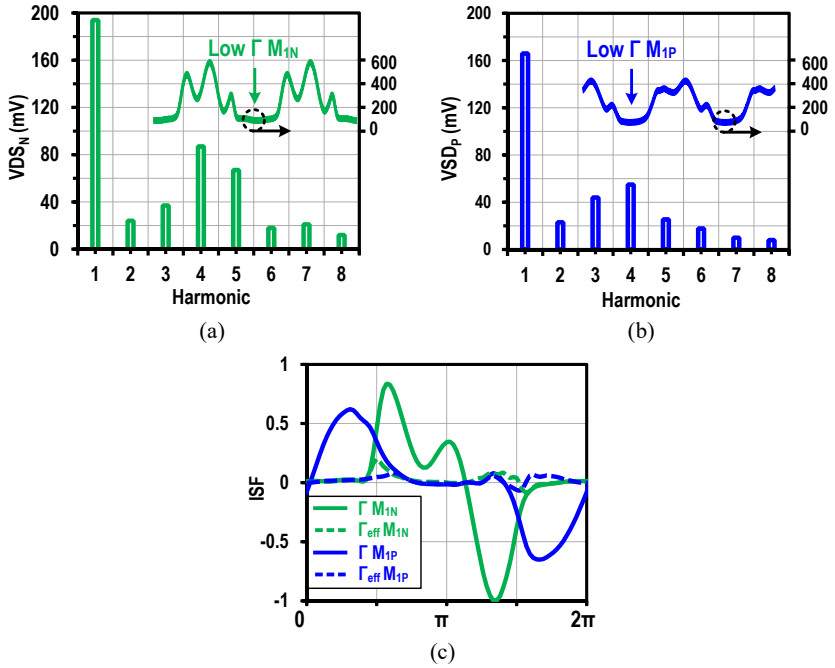


Figure 8.8: Simulated drain to source voltage harmonics for both (a) NMOS and (c) PMOS and (c) their respective ISF.

devices, is reduced due to the cascode structure while the transimpedance loop gain is boosted, thus allowing the gate voltage to swing $2\times$ higher for a given supply at $V_t extF$ compared to a class-F_{23} with source feedback 8.7.

At 0.2 V supply, the single-ended peak-to-peak voltage swing at the gate node is 1.3 V,

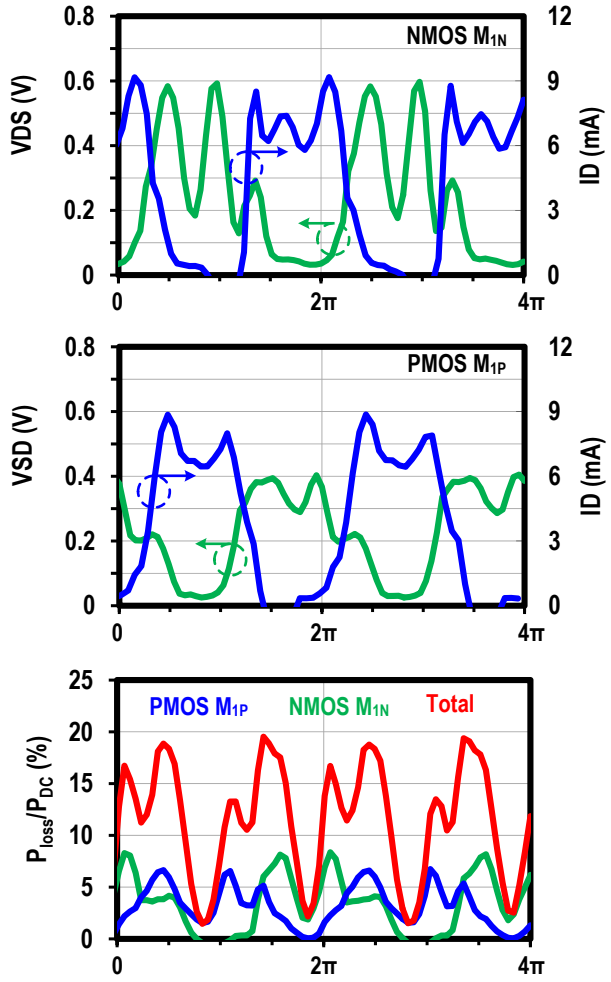


Figure 8.9: Simulated drain to source voltage, current, and the normalized power loss with respect to the DC power for the switching FETs per cycle showing an efficiency higher than 85%.

providing rail-to-rail operation for the following on-chip buffer. The harmonic-rich drain-to-source (V_{DS}) voltage for both NMOS and PMOS shapes the time domain ISF (Γ), (Fig. 8.8), while the small I/V overlap shifts the noise modulation function (NMF) from the ISF, thus yielding a negligible device effective ISF (Γ_{eff}) with a simulated switching efficiency higher than 85% at 5GHz (Fig. 8.9).

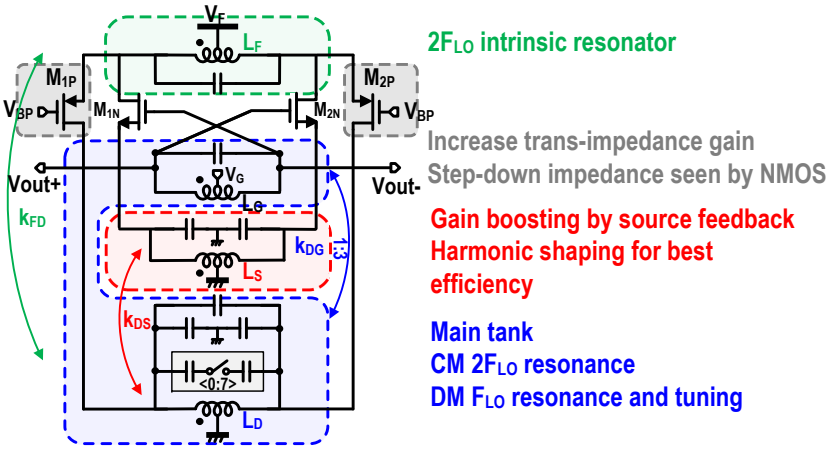


Figure 8.10: Schematic of the folded DCO.

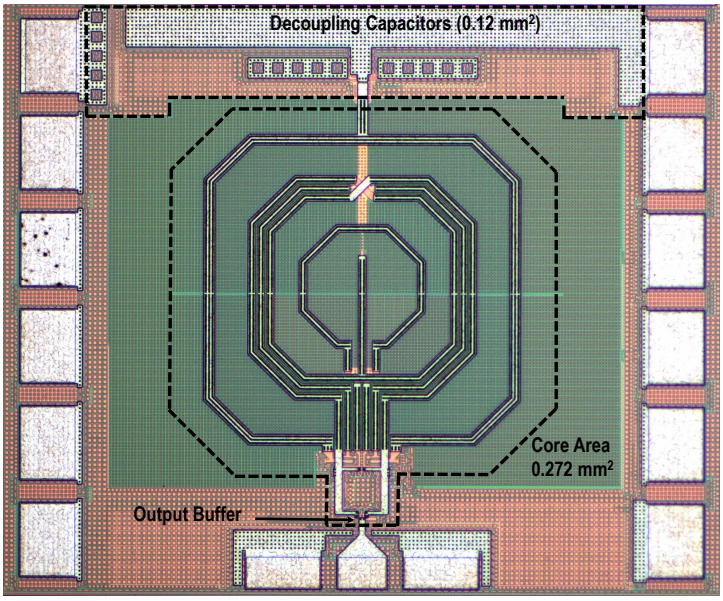


Figure 8.11: Micrograph of the fabricated folded DCO chip in 22nm FDSOI.

8.3 Implementation

A prototype of the folded DCO was fabricated in 22nm FDSOI (Fig. 8.11). Low-V_T (250 mV for NMOS and 300 mV for PMOS) thin-oxide devices are used to provide a larger loop gain and better PN performance (particularly in the thermal region). Reliable start-up is ensured, at low supply levels, by optimizing the gate bias for the NMOS/PMOS pairs.

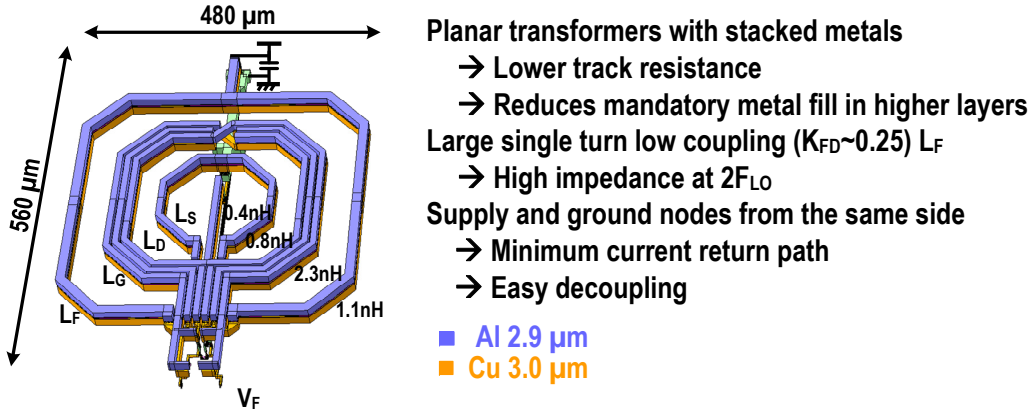


Figure 8.12: Transformer layout.

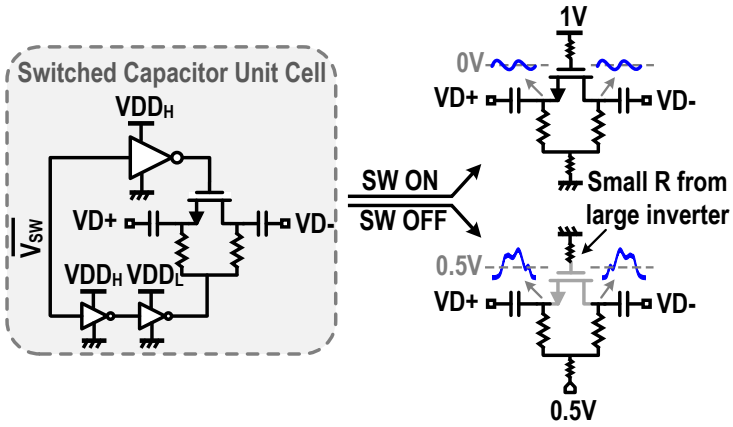


Figure 8.13: Switched capacitor unit-cell and its biasing scheme in ON and OFF states.

The 4-windings transformer (Fig. 8.12) is designed in a planar fashion while stacking the upper two thick metals (copper and aluminum) for each winding. This is necessary to reduce the mandatory metal fill in the upper layers which reduce Q. The simulated Q values for L_G, L_D, L_F and L_S are 11, 11.2, 16 and 17, respectively, at 5 GHz.

A 3-bit differential switched-capacitor bank is placed in parallel with the lower swing inductor LD for frequency tuning (Fig. 8.13). Therefore, thin-oxide low-VT NMOS switches can be used with their smaller Ron-Coff. Two digital supply levels are employed to bias the switches in ON and OFF states. This avoids accidental switch turn on from the large voltage swings while ensuring that the swing across the OFF switch remains within reliable limits.

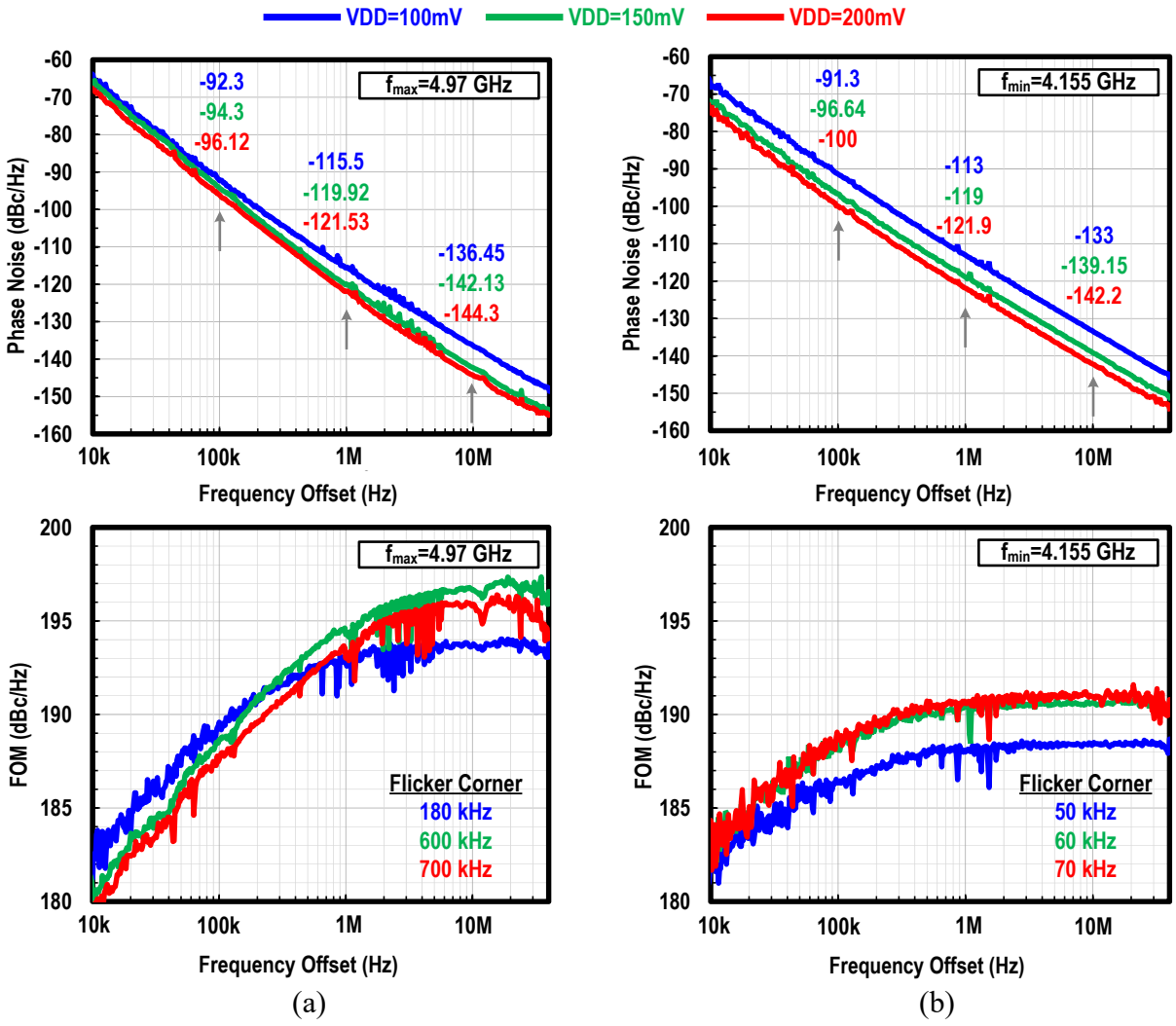


Figure 8.14: Measured phase noise and FOM for the 0.1 V, 0.15 V and 0.2 V supplies versus offset frequency for (a) the high band and (b) the low band.

8.4 Measurements

Fig. 8.14 presents the measured PN and FOM at the maximum (f_{max} = 4.97 GHz) and minimum (f_{min} = 4.15 GHz) tuning range for three different supplies (0.2, 0.15, 0.1 V). At the upper band (f_{max}), a 10 MHz offset PN of -144.3, -142.1 and -136.5 dBc/Hz, is measured for 0.2, 0.15, and 0.1 V, respectively. The achieved FOMs are higher than 193.7 dBc/Hz for all supply levels in the thermal region, and reach a record of 197 dBc/Hz at 0.15 V. The flicker corner

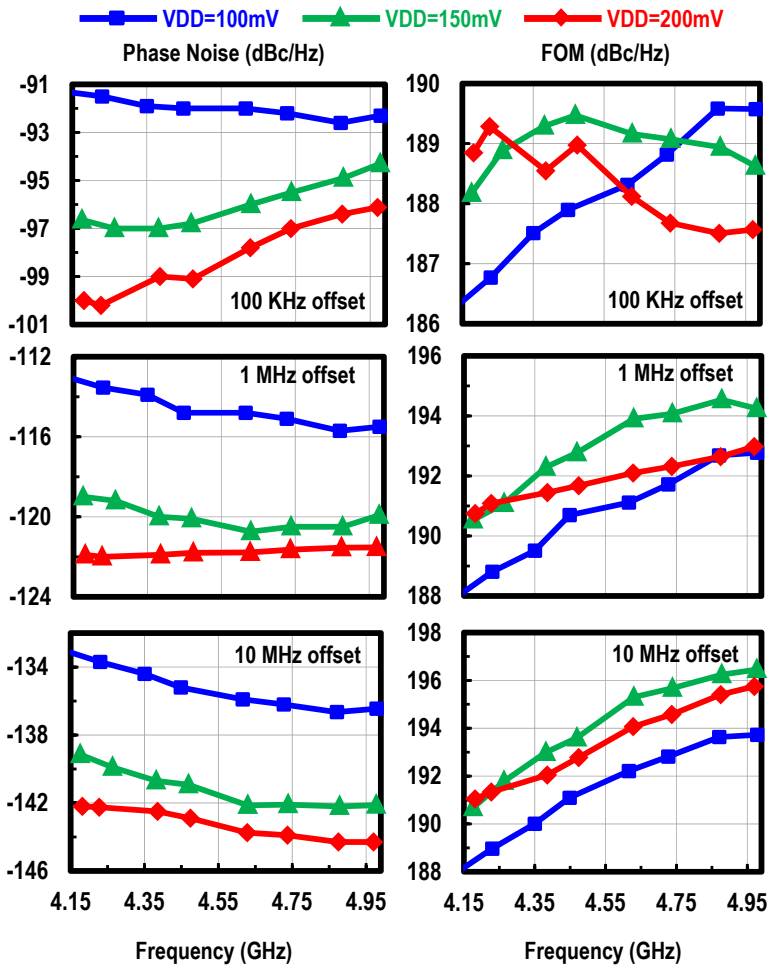


Figure 8.15: Measured phase noise and FOM versus oscillation frequency for 0.1 V, 0.15 V and 0.2 V supplies.

frequency, where the FOM is 3 dB lower than its peak value, is between 180 and 700 kHz at f_{max} (the simulated flicker corner for low-V_T thin SOI devices is 5-10 MHz). Also, at f_{min}, the flicker corner is greatly reduced to 50-70 kHz for all three supplies. This validates the effectiveness of flicker reduction by the resonator L_F, but also shows the importance of tuning the tank at the folding node. The L_F tank is more tolerant to de-Qing from capacitive tuning since it is isolated from the main L_G-L_D tank. The FOM is reduced, at f_{min}, due-to the loading of the capacitor bank and the reduced gain, but remains better than 190 dBc/Hz at both 0.2 and 0.15 V.

The PN and FOM results across the frequency range (Fig. 8.15) reach best values at the

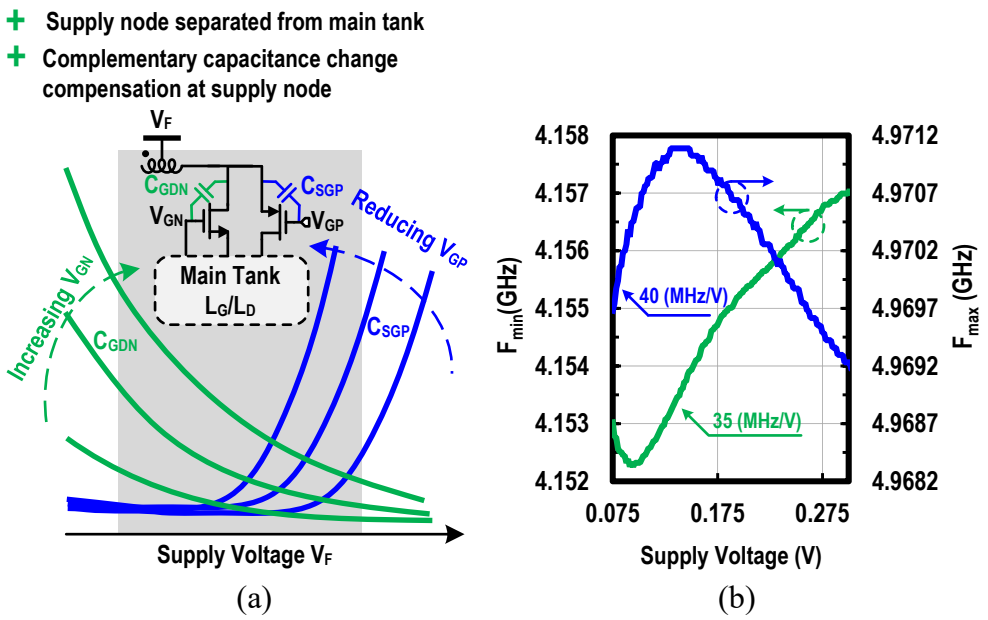


Figure 8.16: (a) Frequency pushing reduction mechanisms. (b) Measured frequency pushing for the highest and lowest band demonstrating lower than 40 MHz/V for sub-threshold supply levels.

thermal region near f_{max}, when the capacitor bank is OFF, while the flicker is most reduced near f_{min}.

The folded structure also decouples the supply from the main tank, thus allowing reduced frequency pushing. In addition, the dominant non-linear capacitors, C_{GDN} and C_{SGP} (Fig. 8.16), change in opposite ways with increasing supply, and provide complementary capacitance-change compensation at the supply node. The implemented topology allows the DCO to operate from 75 mV (2.25× less than any reported CMOS/FinFET oscillator) to 300 mV, and with a frequency pushing no larger than 40 MHz/V across the whole frequency range.

Compared with state-of-the-art, low supply, LC oscillators employing common-mode resonance in table 8.1, our folded DCO operates from the lowest supply and achieves the highest FOM at 10 MHz offset, and one of the highest FOMs at 100 kHz offset. The PN achieved at 200 mV supply is nearly 10 dB better than the 16 nm FinFET design in [106]] operating from the same supply, while it is comparable to the CMOS 65nm inverse class-F design [108] operating from 3× the supply.

Table 8.1: Comparison with state-of-the-art oscillators employing common-mode resonance showing the best FOM, and lowest supply of operation.

Design			**[108] Shahmohammadi ISSCC'15**	**[110] Murphy ISSCC'15**	**[107] Lim ISSCC'18**	**[106] Li ISSCC'17**		**This Work**		
Topology			Class-F_{23}	NMOS implicit CM resonance	CMOS Inverse Class-F	Trifilar-Coil		Folded, 4-winding transformer		
Technology process			40nm	28nm	65nm	16nm FinFET		22nm FDSOI		
Frequency (GHz)			5.4-7	2.85-3.75	3.49-4.51	3.2-4		4.15-4.97		
Tuning Range (%)			25%	27.2%	25.5%	22%		18%		
VDD (V)			1	0.9	0.6	0.4	0.2	**0.2**	**0.15**	**0.1**
Power (mW) @ f_{min} / f_{max}			12/10	7.2/6.35	1.2/1.14	3.8	0.6	**2.28/ 1.77**	**1.22/ 0.91**	**0.54/ 0.46**
Phase noise (dBc/Hz)	**@ 100 kHz**	f_{min}	-105.3/ -102.05	-107/ -102	-102.4/ -98.5	-99*/ -95*	-88*/ -90*	-100/ -96.1	-96.7/ -94.3	-91.3/ -92.3
		f_{max}								
	@ 10 MHz	f_{min}	-146.7/ -144.5	-152†/ -148†	-145.6/ -143.7	-145/ -143	-133/ -135	**-142.2/ -144.3**	**-139.2/ -142.1**	**-133/ -136.5**
		f_{max}								
FOM (dBc/Hz)	**@ 100 kHz**	f_{min}	189.1/ 188.9	186.5/ 186.5	192.5/ 191	183.3#/ 181.3#	180.4#/ 184.2#	188.9/ 187.6	188.2/ 188.7	186.3/ 189.6
		f_{max}								
	@ 10 MHz	f_{min}	190.5/ 191.4	192.2&	195.6/ 196.2	190	188	**191/ 195.8**	**190.7/ 196.5**	**188/ 193.7**
		f_{max}								
1/f^3 Corner (kHz)			60-130	200	100-300	120	40	70-700	60-600	50-180
Frequency pushing (MHz/V)			12-23	N.R.	4.5-15	3.6-27.3	12.6-38.2	**< 40 (from 75mV to 300mV)**		
Core Area (mm^2)			0.13	0.19	0.14	0.11		0.272		

N.R. = Not Reported
[1] FOM = -PN + $20\log_{10}(f_o/\Delta f)$ - $10\log(P_{DC}/1mW)$
† Normalized from 5 MHz offset
* Estimated from plots
& Best-case across the reported range
# Calculated based on the provided P_{DC}

8.5 Conclusion

This work proposes an LC DCO based on a folded, transformer-based, circuit topology to improve phase noise performance at low supply voltages. This topology divides the main-tank impedance between two stacked devices for lower phase noise for a given supply voltage without sacrificing loop gain, thus being important in ultra-low-voltage applications. Implemented in 22nm FDSOI, the circuit oscillates from 4.2 to 5 GHz with a peak FOM of 197 dBc/Hz, -142.1 dBc/Hz PN at 10 MHz offset, 40 MHz/V pushing from a 0.15 V supply. The oscillator can operate down to 0.1 V supply.

8.6 Acknowledgment

The authors would like to thank Analog Devices for their financial support, Integrand for EMX electromagnetic simulator and GlobalFoundries for chip fabrication.

Chapter 8, in full, is a reprint of the material as it appears in: O. El-Aassar and G. M. Rebeiz, "26.5 A 0.1-to-0.2V Transformer-Based Switched-Mode Folded DCO in 22nm FDSOI With Active Step-Down Impedance Achieving 197dBc/Hz Peak FoM and 40MHz/V Frequency Pushing," *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2019, pp. 416-418. The dissertation author was the primary investigator and primary author of this paper.

Chapter 9

A 5 GHz 0.5 V Hybrid Class-B/F$_{-1}$ CMOS Oscillator with -147 dBc/Hz Phase Noise at 10 MHz Offset Using Body-Biased 22nm FDSOI

9.1 Introduction

The stringent phase noise requirements for cellular standards pose challenges on the design of LC oscillators in new low-voltage technology nodes. This is typically addressed by using more voltage-tolerant thick-oxide devices at the expense of efficiency and tuning range, or multi-core designs in compromise with the chip area. High performance oscillators are usually designed with a small tank fundamental impedance (R_{Tank}) and a second harmonic ($2f_{LO}$) common mode (CM) resonance to reduce the phase noise for given allowable swing. The $2f_{LO}$ resonance can be implemented as a separate CM single-ended tank as a tail filter or on the supply node [111, 112]. Alternatively, the implicit CM resonance of a multi-turn low magnetic-coupling (k) inductor [110]

or transformer [8, 105, 113] can be adjusted at $2f_{LO}$ with a limited quality factor (Q) at $2f_{LO}$ compared to the explicit designs. Two recent works exploited the concurrent conduction of nMOS and pMOS when placed on differential sides to implement high-Q differential-mode (DM) $2f_{LO}$ resonance and reach very high figure-of-merits (FoMs) [7, 107]. Nevertheless, the minimum R_{Tank}, and thus phase noise, were limited by the multi-turn transformers used in both designs.

This work presents a 5 GHz hybrid thin-oxide only oscillator with two cores driving consecutively a very low R_{Tank} to achieve low phase noise and a reliable start-up. A DM $2f_{LO}$ resonator is shared between both cores, thereby allowing wide swing low noise triode operation with $<$ -147 dBc/Hz at 10 MHz offset from 0.5 V supply in 22nm FDSOI technology.

9.2 Hybrid Class-B/F$_{-1}$ Oscillator design

Fig. 9.1 depicts three complementary oscillator topologies employing a transformer resonator where both nMOS and pMOS are conducting in the same half of the frequency cycle resulting in high current-efficiency. In order to minimize the phase noise for a given allowable voltage swing, a class-C biasing scheme is favored over class-B. An ideal class-C biasing allows $\approx$ 36% DC-to-RF efficiency improvement over class-B while the reduced current conduction angle provides lower noise sensitivity near the voltage zero crossings [114].

The design in Fig. 9.1(a) provides self-biasing at $V_{DD}/2$ for equal transconductance (gm) for nMOS and pMOS. Therefore, the class-C biasing is only achieved for limited and low V_{DD} range, which limits the maximum output swing and penalizes the phase noise. A higher V_{DD} forces the transistors in triode region where their effective ON resistance ($1/gds_{N/P}$) loads the drain tank and deteriorates the phase noise. The problem is alleviated by exploiting the transformer resonator to form a second harmonic ($2f_{LO}$) resonance at the drain side (Z_D) [105]. The $2f_{LO}$ resonance impedes the phase noise degradation when the devices are in triode region an allows switched class-F$_{-1}$ operation. Nevertheless, the output swing is limited to V_{DD} and the gate biasing (tied to

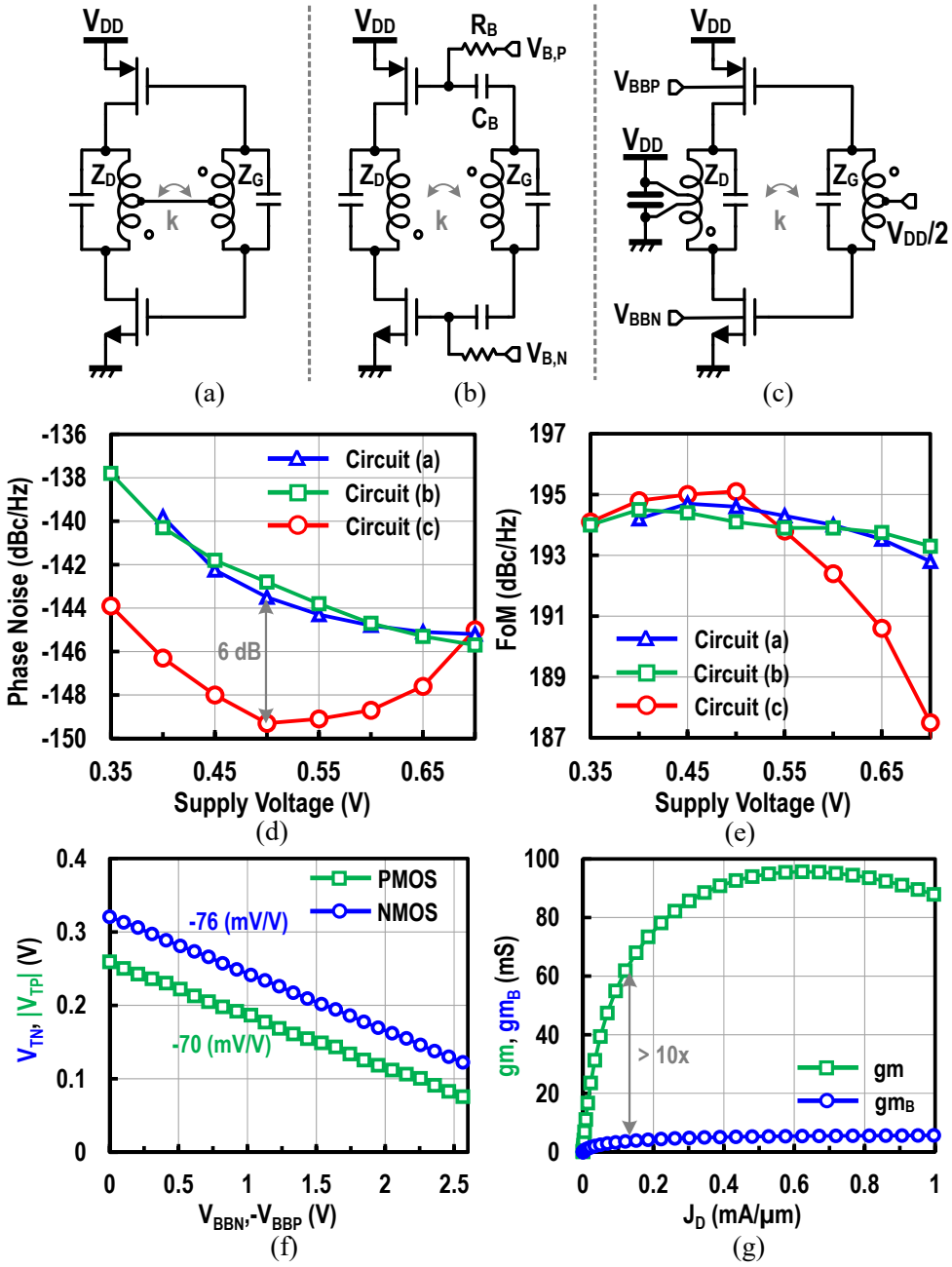


Figure 9.1: CMOS oscillators with DM 2^{nd} harmonic resonance at drain node: (a) self-biased, (b) RC bias, and (c) proposed wide-swing body-biased. (d) Simulated phase noise, and (e) FoM, at 10 MHz offset for 5 GHz operation ($Q = 15$). (f) Body-bias V_T control and (g) corresponding gm_B compared to gm.

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the self-bias conditions) cannot be separately optimized to improve the switching efficiency.

The class-C operation range can be satisfied for a higher V_{DD} irrespective of the transistors

threshold voltages ($V_{T,N/P}$) by independent biasing for both nMOS and pMOS through RC bias networks (Fig. 9.1(b)). Moreover, similar transformer with $2f_{LO}$ resonance can be used to allow low noise triode operation. However, the design of a low cut-off bias network poses its own challenges. A large bias resistor (R_B) generates thermal noise prone to AM-PM conversion, while a small AC-coupling capacitor (C_B) reduces the gate swing and increases the devices noise contribution. Alternatively, a small R_B directly loads the tank and limits its quality factor (Q), while a large C_B reduces the tuning range by the bottom plate parasitic capacitance. The RC bias network typically degrades the phase noise (and FoM) by < 1 dB validating its inclusion in efficient class-C designs [114]. However, the independent optimum gate biasing comes at the expense of a robust oscillation start-up across process, voltage, and temperature (PVT), and a low noise bias circuit design. The robust start-up is achieved through a common-mode feedback bias loop with a large output filter to guarantee stability and low-noise, or a hybrid topology with a less noise-efficient class-B oscillator [114].

The proposed design uses a complementary core while allowing up-to $2\times$ the swing of circuits (a) and (b) for the same V_{DD} (Fig. 9.1(c)) and therefore, a 6-dB reduction in phase noise with comparable FoM (Figs. 9.1(d & e)). The center-tap of the drain resonator is split in two branches connected to the chip V_{DD} and ground, respectively, and heavily decoupled by a large capacitor. This transformer behaves exactly like the one in circuits (a) and (b) in the differential-mode (DM) of operation with a $2f_{LO}$ resonance on the drain side for low phase noise. Since the drain swing is around V_{DD} and ground, for nMOS and pMOS, respectively, the output swing is limited to $2V_{DD}$ similar to an nMOS/pMOS-only topology. A fundamental difference, however, is the concurrent operation of both nMOS and pMOS which inject current to the tank, Z_D, in the same half of the oscillation cycle while preserving a differential output at their drain nodes. This concurrent operation allows a high-Q DM $2f_{LO}$ resonance, instead of a common-mode (CM) low-Q $2f_{LO}$ resonance in case of an nMOS/pMOS-only topology. The gate bias is provided by another core, also exploiting the same high-Q $2f_{LO}$ resonator, thus guaranteeing robust start-up

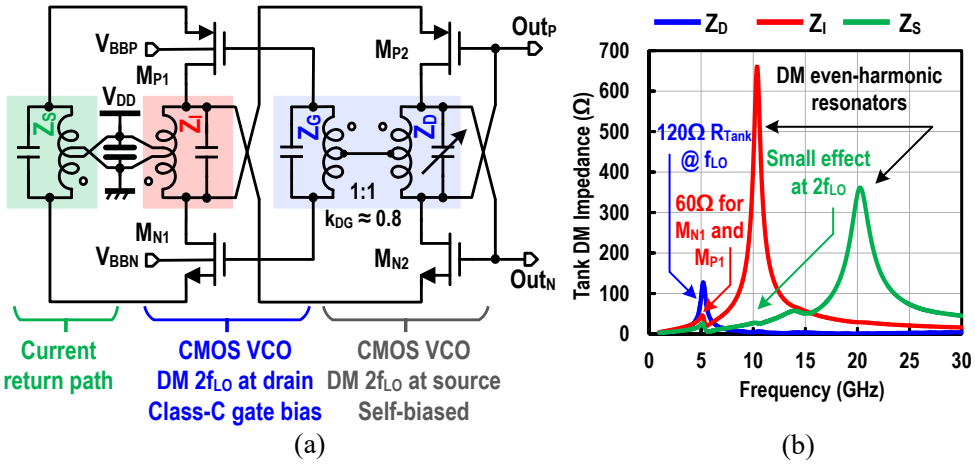


Figure 9.2: (a) Proposed hybrid class B/F$_{-1}$ oscillator. (b) Corresponding DM tank impedance for each node.

and low phase-noise. In order to optimize the gate bias for nMOS and pMOS independently, the forward-body-bias (FBB) in fully-depleted SOI technology is exploited to change their threshold voltages. The FBB can effectively change $|V_{T,N(P)}|$ from 0.32 V (0.26 V) to 0.11 V (0.09 V) with 10$\times$ less sensitivity to bias noise compared to gate biasing as depicted by the gate and bulk transconductances (Fig. 9.1(f) & (g)).

Fig. 9.2 shows the schematic of the proposed oscillator. A class-B single-side CMOS core uses a single-turn drain tank (Z_D) tightly coupled to the main VCO gate tank (Z_G). A 1:1 high-k transformer is therefore realized to provide a Q boost over individual windings Q. The center taps are tied to provide the gate bias for the main class-F$_{-1}$ core. Moreover, the concurrent operation of the nMOS and pMOS (M_{N2} and M_{P2}) of the class-B oscillator, allows exploiting the same DM $2f_{LO}$ resonator (Z_I) on their source nodes for low phase noise contribution. At one half of the oscillation cycle a high $2f_{LO}$ impedance forces the noise of M_{N1} and M_{P1} to circulate in their respective channel conductance for the main class-F$_{-1}$ core (Fig. 9.3(a)). Similarly, on the other half of the cycle, the $2f_{LO}$ high DM impedance at the source of M_{N2} and M_{P2} prevents de-Queing Z_D tank (Fig. 9.3(b)).

In order to reach very-low phase noise, only single turn windings with small inductance

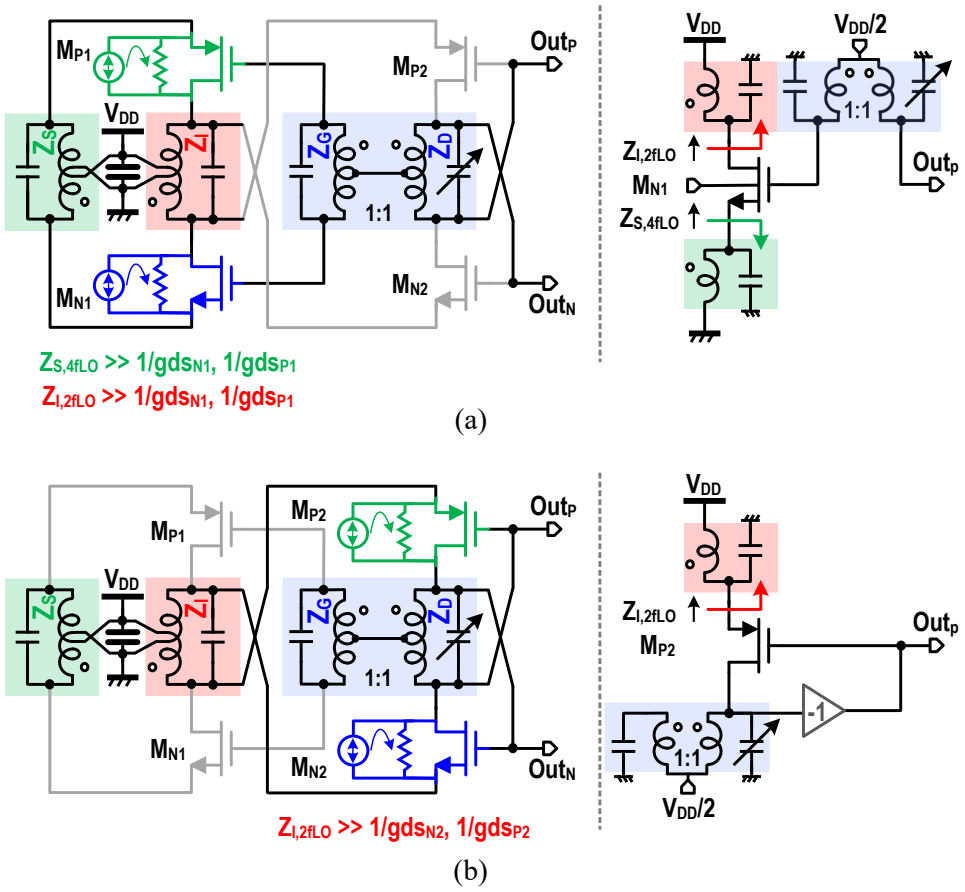


Figure 9.3: Proposed CMOS oscillator switching mechanism and the single-ended equivalent circuit for: (a) first half, and (b) second half of the frequency cycle exploiting the same DM Z_I tank to reduce transistors noise.

and tank fundamental impedance (R_{Tank}) are used to increase the f_{LO} RF power for a given voltage swing. In addition, single-turn inductors naturally provide higher peak Q and self-resonance due to the non-existent inter-winding capacitance. A major challenge, however, is the current return path which becomes hard to model in case V_{DD} and ground are not from the same side. An extra DM source resonator (Z_S) is therefore designed to guide the RF-current of the main VCO, provide a $4f_{LO}$ resonance and has minimal effect on the $2f_{LO}$ operation of Z_I Fig. 9.2(b).

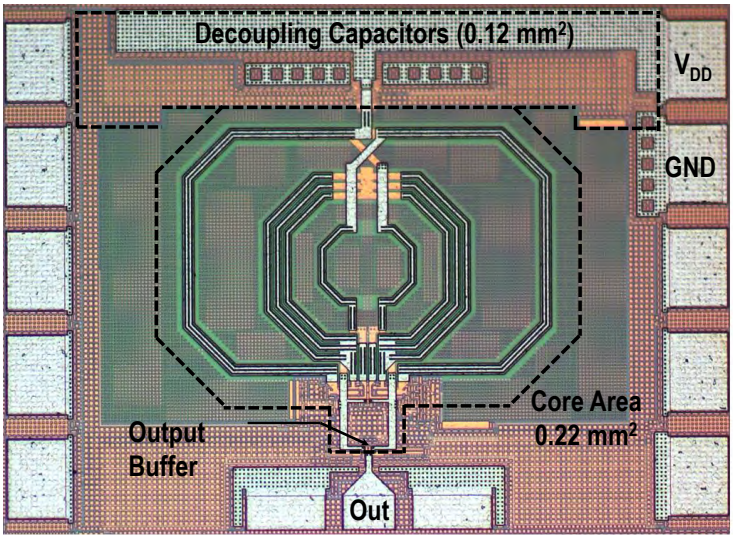


Figure 9.4: Die micro-graph of the fabricated oscillator chip in 22 nm FDSOI.

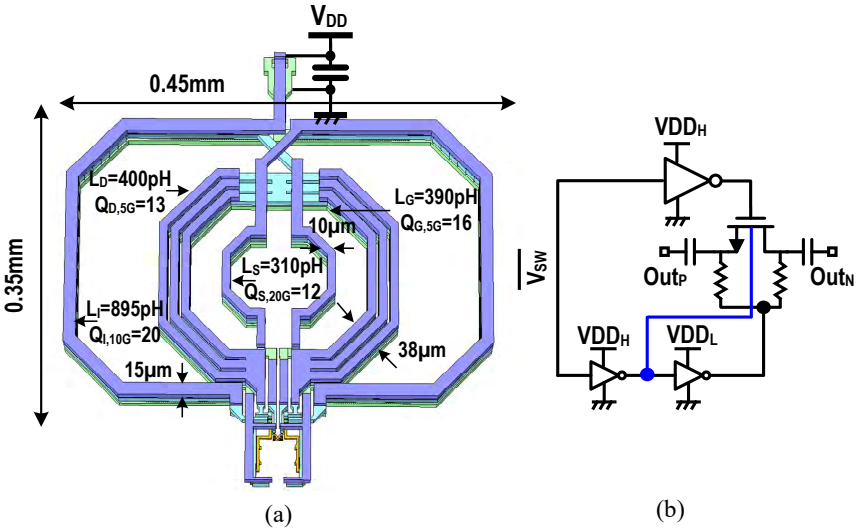


Figure 9.5: (a) Transformer layout. (b) Corresponding FBB switched capacitor bank bit-slice.

9.3 Implementation and Measurement Results

The proposed oscillator is fabricated in 22 nm FDSOI using low-V_T thin-oxide devices with a core area of 0.22 mm^2 (Fig. 9.4). The upper 2 copper metals (3 μm each) and an aluminum capping (2.9 μm) are used to provide the single turn windings of the proposed tank. The drain-gate tank (Z_D-Z_G) reaches an 0.81 coupling factor (k) at 5 GHz to get a maximum Q of 21. While the

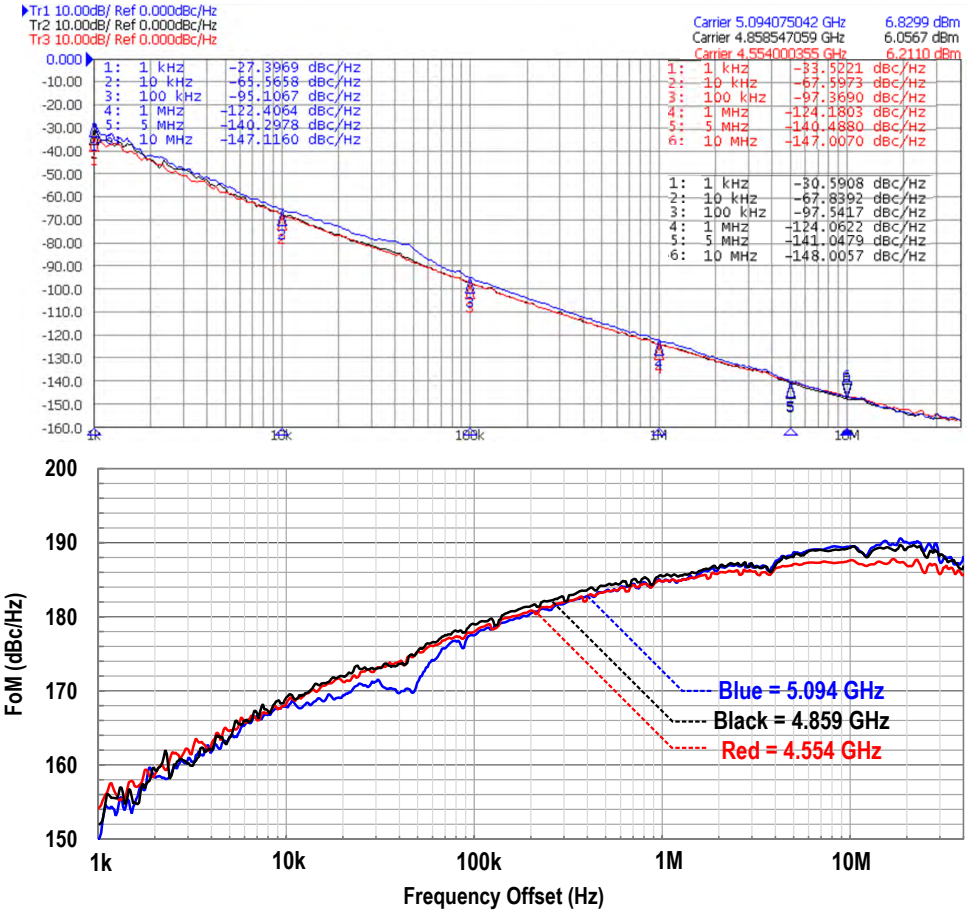


Figure 9.6: Measured phase noise and FoM for the high, mid, and low bands versus offset frequency demonstrating down to -148 dBc/Hz phase noise at 10 MHz offset with a 190 dBc/Hz peak FoM.

intrinsic Q of L_G is 16 at 5 GHz, which degrades to 13 at the drain side (L_D), inevitably due to the routing to the capacitor bank. The Z_I tank provides a 60 Ω fundamental impedance divided between M_{N1} and M_{P1} while the $2f_{LO}$ impedance reaches 650 Ω for device noise suppression. A 3-bit capacitor bank is placed on Z_D side with FBB switches to reduce their ON resistance and OFF capacitance Fig. 9.5(b).

A signal source analyzer (Keysight E5052B) is used for phase noise and frequency measurements. The measured phase noise and FoM from 4.55-to-5.1 GHz are plotted in Fig. 9.6 across frequency offset for the low, mid, and high-bands. The oscillator achieves a best phase noise of -148 dBc/Hz at 10 MHz offset from a 4.86 GHz carrier with a peak FoM of 190 dBc/Hz

Table 9.1: Comparison with state-of-the-art low phase noise oscillators

Design	This Work	[112] JSSC'15	[110] ISSCC'15	[111] JSSC'13	[7] ISSCC'19	[107] ISSCC'18
Topology	CMOS Hybrid Class-B/F_{-1}	Class-B with tail filter	NMOS implicit CM resonance	Class-D with tail filter	Folded	Inverse Class-F
Technology process	22nm FDSOI Thin	55nm Thick	28nm Thick	65nm Thin	22nm FDSOI Thin	65nm Thin
Frequency (GHz)	4.55-5.10	7.4-8.4	2.85-3.75	3-4.8	4.15-4.97	3.49-4.51
V_{DD} (V)	0.5	1.5	0.9	0.4	0.2	0.6
Power (mW) @ f_{min} / f_{max}	18/15	18.4*	7.2/6.35	6.8/3.6	2.28/1.17	1.2/1.14
PN (dBc/Hz) @ 10 MHz f_{min}	-147.0	-146.8	-152†	-150	-142.2	-145.6
PN (dBc/Hz) @ 10 MHz f_{max}	-147.1		-148†	-144.5	-144.3	-143.7
FoM (dBc/Hz) @ 10 MHz f_{min}	187.6	190.5	192.2	191	191	195.6
FoM (dBc/Hz) @ 10 MHz f_{max}	189.5	192.3		192	195.8	196.2
PN @ 10 MHz (dBc/Hz) normalized to 915 MHz	-162.5	-165.7	-161.9	-160#	-159	-155.32
Frequency pushing (MHz/V)	20-44	20*	N.R.	60-500*	40	4.5-15
Core Area (mm^2)	0.22	0.17	0.19	0.152	0.272	0.14

N.R. = Not Reported
† Normalized from 5 MHz offset
[1] FoM = -PN + $20\log_{10}(f_o/\Delta f)$ - $10\log(P_{DC}/1mW)$
* Estimated from plots

in the thermal range while dissipating 17 mW. Across the 11% tuning range, the phase noise at 10 MHz offset is $<$ -147 dBc/Hz, while the FoM varies between 187 and 190 dBc/Hz with a 15-to-18 mW DC power.

Table! 9.1 summarizes the performance and compares it with state-of-the-art low-noise oscillators. The hybrid class-B/F_{-1} design delivers the best phase noise for thin-oxide only designs with only 0.5 V supply. While the performance is competitive with thick-oxide designs using over $2\times$ the supply.

9.4 Conclusion

This work presented a hybrid class-B/F_{-1} 5 GHz oscillator for robust start-up and very low phase noise. The design shares the same DM $2f_{LO}$ resonator between both cores commutating in opposite halves of the oscillation cycle. Moreover, the concurrent operation of the differential complementary transistors is leveraged to achieve wide swing over a differential-only $2f_{LO}$

resonator to maximize the fundamental power and reduce the phase noise for a low V_{DD}. Self biasing and FBB are exploited to optimize the switching efficiency with low noise sensitivity from the bias network. The CMOS oscillator delivers the lowest phase noise reported by a 0.5 V supply oscillator while using thin-oxide only devices.

9.5 Acknowledgment

The authors would like to thank Analog Devices for their financial support, Integrand for EMX electromagnetic simulator and GlobalFoundries for chip fabrication.

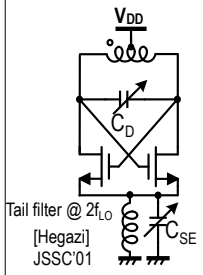
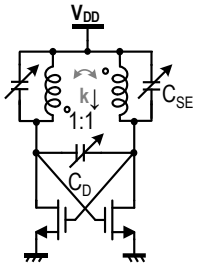
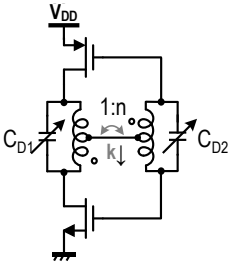
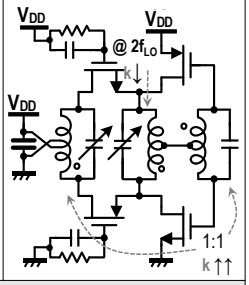
Chapter 9, in full, has been submitted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "A 5 GHz 0.5 V Hybrid Class-B/F$_{-1}$ CMOS Oscillator with -147 dBc/Hz Phase Noise at 10 MHz Offset Using Body-Biased 22nm FDSOI," *IEEE Microwave and Wireless Components Letters*, submitted. The dissertation author was the primary investigator and primary author of this paper.

Chapter 10

A Stacked-Complementary 5 GHz Oscillator with Even-Only Differential Harmonic Shaping Achieving -150 dBc/Hz Phase Noise at 10 MHz Offset Using Body-Biased Thin-Oxide 22nm FDSOI

10.1 Introduction

The quest for high spectral-purity LC oscillators stems from the migration to low-voltage low-power technology nodes which limit the phase noise (*PN*) by a single-core. To satisfy the strict requirements for cellular standards, the second harmonic ($2f_{LO}$) resonance is extensively used to reduce the *PN* for a given allowable swing. The $2f_{LO}$ resonance can be implemented by a separate tank [112] or implicitly using a low magnetic coupling (k) multi-turn inductor [110] or transformer (xfrmr) [107] (Fig. 10.1). The first technique [112] has larger area but is viable

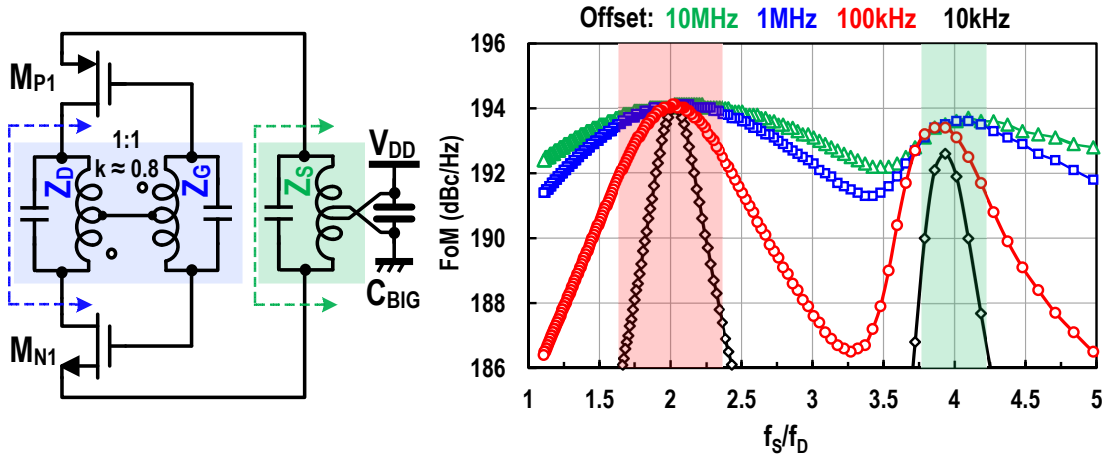
[1] JSSC'17	[2] ISSCC'15	[3] ISSCC'18	This Work
			
Tank			
High-Q single-turn inductor Low R_{Tank} @ f_{LO}	Multi-turn inductor to realize low-k Higher R_{Tank} @ f_{LO}	Multi-turn 1:n xfrmr to realize low-k Moderate R_{Tank} @ f_{LO}	High-Q high-k single-turn 1:1 xfrmr lower R_{Tank} @ f_{LO}
Moderate-Q single-ended CM inductor @ $2f_{LO}$	Low-Q single-ended CM inductor @ $2f_{LO}$	2 turn differential inductor @ $2f_{LO}$	High-Q single-turn differential inductor @ $2f_{LO}$
Differential cap. bank for DM Single-ended cap. bank for CM	Differential cap. bank for DM Single-ended cap. bank for CM & DM	Differential-only cap. bank	Differential-only cap. bank
Voltage swing limits and fundamental power P_{Tank}			
$V_{ptp\text{-}Drain} \approx 2\,V_{DD}$ $V_{ptp\text{-}Gate} \approx 2\,V_{DD}$	$V_{ptp\text{-}Drain} \approx 2\,V_{DD}$ $V_{ptp\text{-}Gate} \approx 2\,V_{DD}$	$V_{ptp\text{-}Drain} \approx V_{DD}$ $V_{ptp\text{-}Gate} > 2\,V_{DD}$	$V_{ptp\text{-}Drain} \approx 2\,V_{DD}$ $V_{ptp\text{-}Gate} \approx 2\,V_{DD}$
$V_{DD,max} = \frac{1}{2} \times V_{Gate\text{-}Drain,max}$	$V_{DD,max} = \frac{1}{2} \times V_{Gate\text{-}Drain,max}$	$V_{DD,max} < \frac{2}{3} \times V_{Gate\text{-}Drain,max}$	$V_{DD,max} = \frac{2}{3} \times V_{Gate\text{-}Drain,max}$
P_{Tank} @ f_{LO} high	P_{Tank} @ f_{LO} moderate	P_{Tank} @ f_{LO} moderate	P_{Tank} @ f_{LO} highest
Area			
Separate inductors	Single inductor	Nested inductors	Nested inductors

DM: Differential-Mode CM: Common-Mode

Figure 10.1: Oscillators' topologies employing 2^{nd} harmonic resonance and key design features.

with a single-turn small drain inductor to achieve high quality factor (Q), low f_{LO} impedance (R_{Tank}), and low phase noise, limited by the reliable swing for the core devices. The implicit $2f_{LO}$ resonance method [110] uses one multi-turn inductor footprint to realize low-k between the windings and entails the presence of a single-ended capacitorsâĂŹ bank, which limits the lowest implementable R_{Tank} and achieved transformer Q at f_{LO} ($2f_{LO}$). The Q at $2f_{LO}$ is boosted using a low-k 1:n transformer [107] at the expense of a lower Q at f_{LO} compared to a high-k 1:1 transformer.

This work proposes a 5 GHz stacked-complementary oscillator (SCO) that uses high-Q single-turn nested differential inductors to achieve very low R_{Tank} and even-harmonic shaping.



(a) (b)

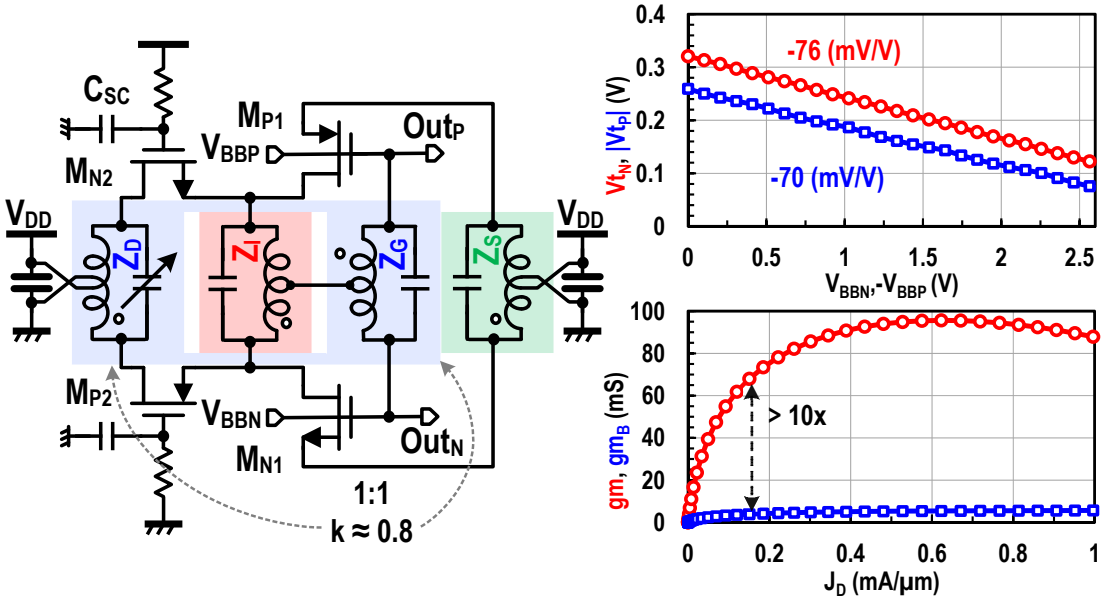
Figure 10.2: (a) A complementary oscillator with DM source resonator. (b) Dependence of the FoM on the accuracy of the source resonance around the even harmonics.

Such small R_{Tank} allows the oscillator to achieve a phase noise $<$ -150 dBc/Hz at 10 MHz offset using thin-oxide devices operated from 0.6 V (V_{DD}) in a 22 nm technology node.

10.2 Stacked-Complementary Oscillator design

We first consider a complementary oscillator with both nMOS and pMOS conducting in the same half of the frequency cycle (Fig. 10.2(a)). In contrast with [107], the main tank (L_D/L_G) is designed as a single-turn high-k 1:1 transformer to obtain the highest effective Q_{Tank} at f_{LO} [115]. The inductor turn can be arbitrary small to obtain low R_{Tank} and phase noise as long as the devices are able to provide the current for high swing and Q_{Tank} is not dominated by routing parasitics. The structure, however, lacks harmonic shaping at the drain nodes or a passive voltage gain (A_v) for MOS noise suppression which is typically achieved by a 1:n transformer.

Since the complementary devices are switching ON and OFF concurrently, the resonator Z_S between the sources of M_{N1} and M_{P1} can be made differential for a higher Q for even and odd harmonics. A differential inductor has a higher self-resonance and lower substrate loss, and thus achieves higher peak Q compared to an equally sized single-ended inductor. Notably, only even



(a) (b)

Figure 10.3: (a) Proposed stacked-complementary oscillator with dual DM even-harmonic resonances and a 1:1 high-k single-turn fundamental transformer. (b) Threshold voltage control to set the class of the oscillator through forward body-biasing and the corresponding gm_B compared to gm.

harmonics produce a duty-cycle distortion for non-real loads and thus yield a non-zero DC value for the impulse sensitivity function (ISF) causing flicker up-conversion. Therefore, a resonator around $2f_{LO}$ or $4f_{LO}$ improves the figure-of-merit (FoM) at all offsets (Fig. 10.2(b)) with a $2f_{LO}$ resonance favored for the higher $2f_{LO}$ current compared to $4f_{LO}$.

The proposed design (Fig. 10.3(a)) uses another pair of stacked-complementary devices M_{N2} and M_{P2} to realize a higher swing on Z_D for a given V_{DD} as in [7]. A core difference, however, is the concurrent operation of the stacked-devices M_{N2} and M_{P2}, which conduct in the other half cycle compared to M_{N1} and M_{P1}. The intermediate nodes are leveraged to form a single-turn high Q differential resonator (Z_I) at $2f_{LO}$ that is weakly coupled ($k = 0.31$) to the main tank, such that the f_{LO} impedance for L_I is $2\times$ lower than that provided on the gate side of M_{N1} and M_{P1}. Therefore, a passive A_v is achieved by drain-to-gate coupling for M_{N1} and M_{P1} to reduce their noise contribution. Also, Z_I provides a high-impedance path for the $2f_{LO}$ current for the stacked-devices (source nodes) and the common-source (CS) devices (drain nodes) in their

respective half cycles to minimize their current noise injection to Z_D (main tank).

The $2f_{LO}$ resonator is sufficient to provide a low *ISF* without an extra resonator Z_S. However, since a single-turn inductor is desired for the main tank, the current return path would be hard to model without Z_S to guide the RF current to well-decoupled V_{DD} and ground nodes. Z_S is therefore designed around $4f_{LO}$ to provide a controlled current routing path and improve the supply frequency pushing without disturbing Z_I operation. Z_S cannot be designed around $2f_{LO}$ to avoid altering the $2f_{LO}$ resonance of Z_I, being part of the same transformer. Alternatively, a resonance around $3f_{LO}$ can still provide considerable impedance at $2f_{LO}$.

The SCO provides self-biasing which avoids noise up-conversion from a bias network and ensures reliable start-up for the nominal V_{DD}. However, the class of operation for the devices, only controlled by V_{DD}, can lead to sub-optimal operation. The body-bias of the fully depleted SOI devices is therefore used to control the threshold voltage Vt, and class of operation for both nMOS and pMOS (Fig. 10.3(b)). The bulk trans-conductance (gm_B) is more than $10\times$ lower than the gate one (gm) to ensure very low sensitivity to bias noise.

10.3 Implementation

The proposed SCO is fabricated in 22 nm FDSOI using low-Vt thin-oxide devices. The core area is 0.2 mm^2 and the die size is 0.57 mm^2 including pads (Fig. 10.4). This technology provides 2 thick copper metals (3 μm each) and an aluminum capping (2.9 μm) which are used to implement the 4 windings of the proposed transformer (Fig. 10.5(a)). The main tank (L_D, L_G) is laid out as a broadside single-turn transformer while connecting 3 parallel 10 μm metal strips to increase the effective surface area and maximize k (k = 0.81 at 5 GHz). The intrinsic Q of L_G is 16 at 5 GHz, which degrades to 13 at the drain side, inevitably due to the routing to the capacitorsâĂŹ bank. Therefore, $(L_GC_G)/(L_DC_D)$ is designed to be 0.85 (rather than 1) at the middle of the band to get a maximum Q of 21. The rest of the windings tie the top 2 metals

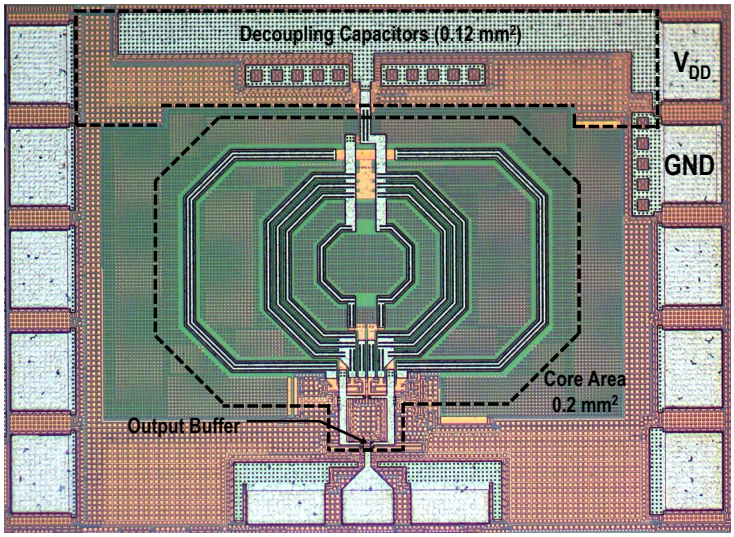


Figure 10.4: Die micro-graph of the fabricated oscillator chip in 22 nm FDSOI.

to avoid metal fill underneath. A 120 Ω drain impedance (R_{Tank}) is driven by the differential stacked core, and divided evenly between the 4 devices through proper design of C_{SC} and biasing conditions (Fig. 10.3(a)). An intrinsic Q of 20 is achieved for Z_I at 10 GHz, while A_v at $2f_{LO}$ between the drain and gate for the *CS* pair is kept below 0 dB by selecting $L_G C_G > L_I C_I$ to avoid mode ambiguity. Z_S provides 360 Ω at $4f_{LO}$ with a minimum effect around $2f_{LO}$ (Fig. 10.5(b)).

The maximum gate-to-drain voltage reaches 1.1 V for M_{N1} and M_{P1} under the nominal 0.6 V supply. The value is higher than the $1.5\times$ V_{DD} predicted by Fig. 10.1 due to the addition of Z_S for current return path, allowing the voltage to go over V_{DD} and under zero at the source nodes followed by the intermediate nodes (Fig. 10.5(c)). Nevertheless, the value remains lower than $2V_{DD}$ for reliability.

10.4 Measurements

The chip is mounted on a DC board with low-noise low-drop-out voltage supplies (LDOs) for biasing and digital controls. The SCO output is buffered on-chip and the phase noise is measured using a signal source analyzer (Keysight E5052B). The signal source analyzer provides

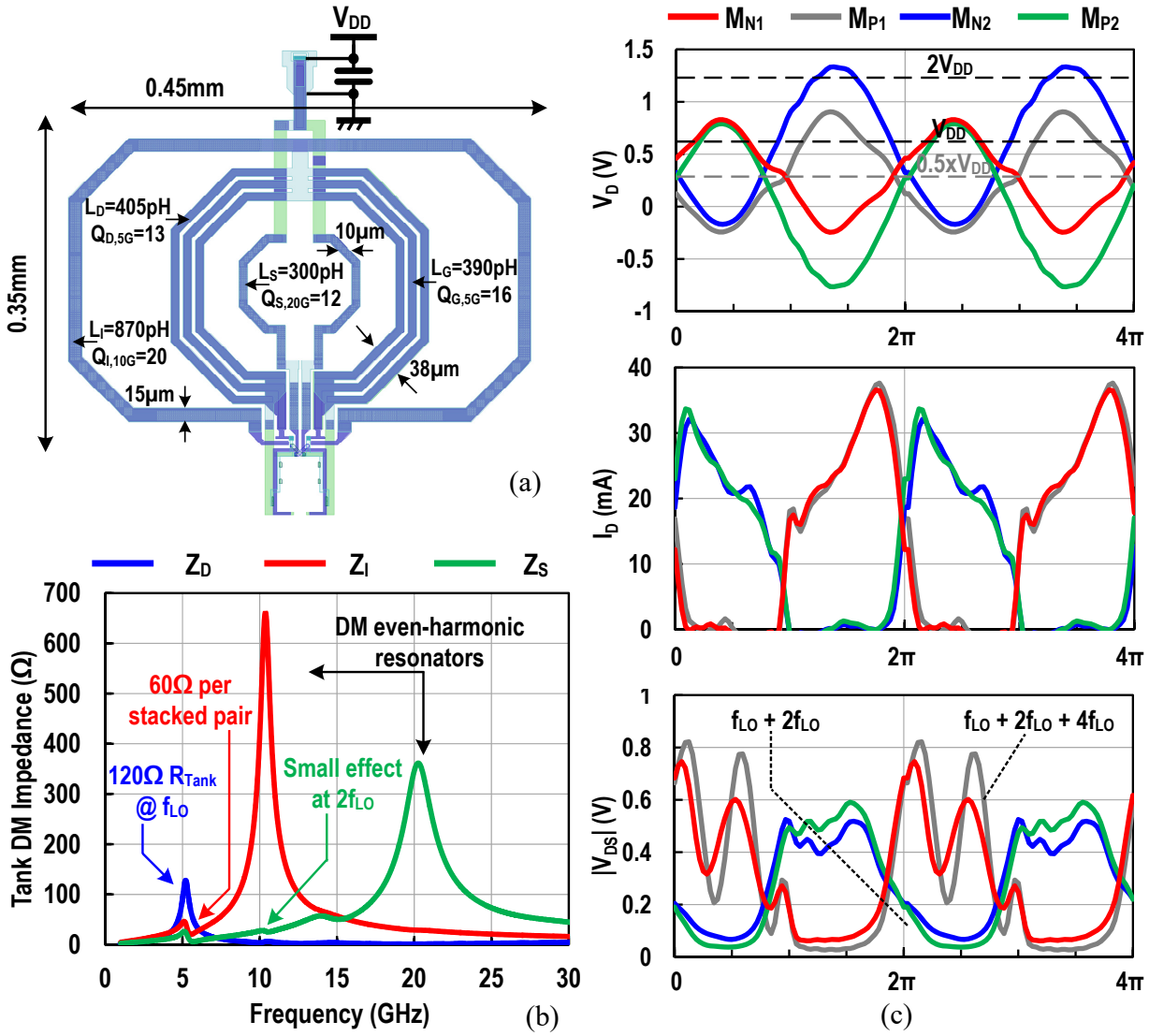


Figure 10.5: (a) Proposed stacked-complementary oscillator transformer layout. (b) Corresponding DM tank impedance for each node. (c) Simulated drain voltages, currents, and drain to source voltages for the proposed oscillator showing stack operation and harmonic shaping.

an internal voltage supply used as V_{DD} for the chip in frequency pushing measurements. The measured phase noise and FoM from 5.4-to-4.75 GHz are plotted in Fig. 10.6. The SCO achieves a phase noise $<$ -127 and -150 dBc/Hz respectively at 1 MHz and 10 MHz offsets across the tuning range. The phase noise reaches best values of -128.7 and -151 dBc/Hz at 5 GHz. The achieved FoMs in the thermal range at 10 MHz offset are between 191-193 dBc/Hz across the tuning range. These values slightly decrease at higher offsets limited by the noise floor of the

on-chip output buffer. The measured flicker-corner varies between 800 kHz and 1 MHz and is 2-3$\times$ worse than simulations. This can be partially attributed to modeling inaccuracies in the passives causing off-resonance harmonic operation, in addition to the thin-SOI devices flicker corner modeling under large signal conditions ($\approx$ 5-7 MHz in simulations for the intrinsic pMOS and nMOS devices).

The measured phase noise and FoM across the tuning range are within $\pm$ 1 dB in the thermal range and increase to $\pm$ 2 dB in the flicker-dominated range (Fig. 10.7). The power consumption is 18.2 mW at the low band and reduces to 15.2 mW at the high band with less capacitive loading and higher R_{Tank}.

The measured supply frequency pushing is shown in Fig. 10.8. The pushing value varies between -6 to -20 MHz/V for high and low bands. These values are $\approx 2\times$ better in simulations indicating a slightly off-resonance $4f_{LO}$ resonator in the measured prototype. A negative value indicates the tank current harmonics, which increase by increasing V_{DD}, flow in a capacitive path and reduce the oscillation frequency by the Groszkowski effect [116]. Nevertheless, the values remain better than most reported oscillators achieving comparable phase noise.

Compared with oscillators employing $2f_{LO}$ resonance in Table 10.1, the SCO achieves one of the lowest reported phase noise in the thermal range using thin-oxide devices, only surpassed by [113] which drives two separate transformers and uses thick-oxide devices with over $2\times$ the supply. To our knowledge, this SCO is the first single-core design to report a phase noise better than -160 dBc/Hz at 10 MHz offset normalized to a 915 MHz carrier using thin-oxide devices in a sub-65 nm technology (exceeding it by 6 dB) [111]. Both FoM and the supply pushing are among the best reported for switched-mode designs.

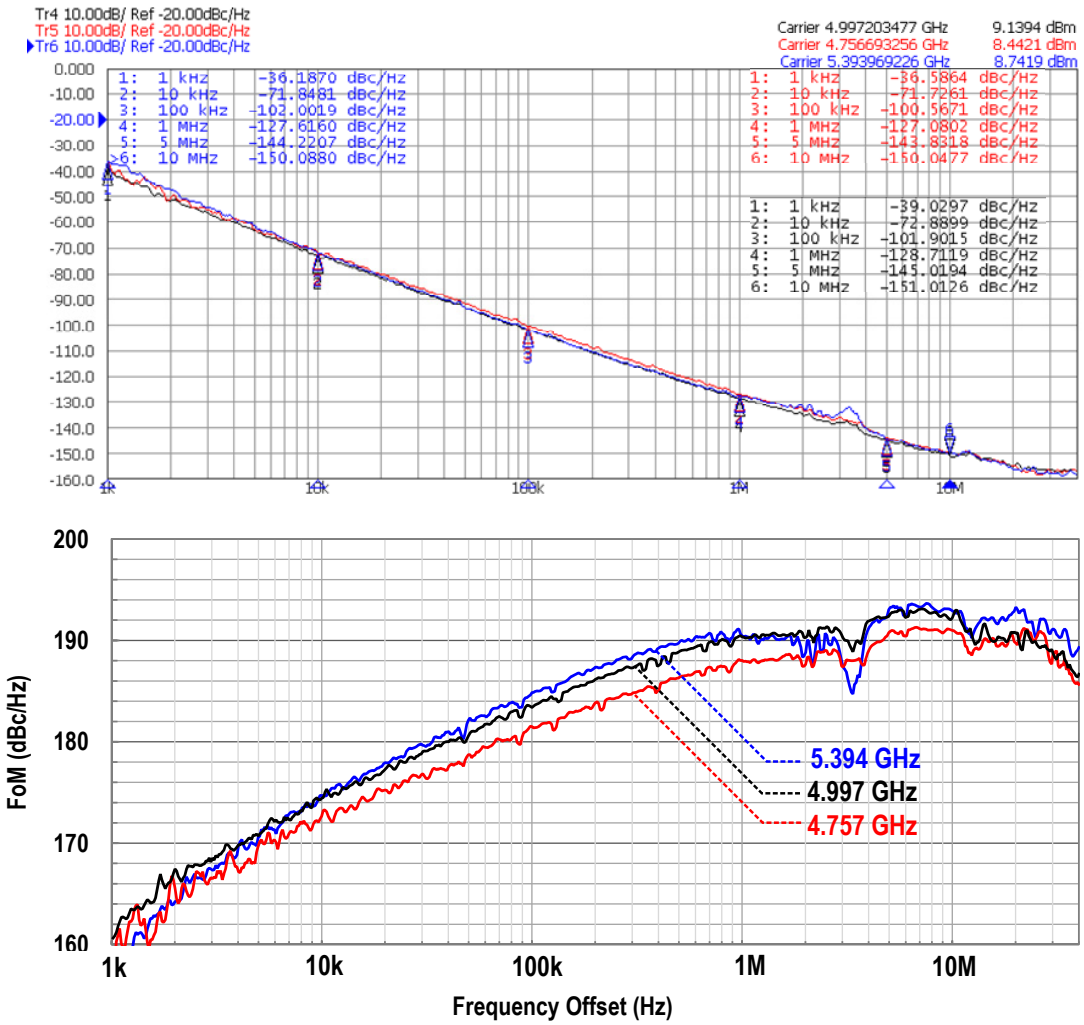


Figure 10.6: Measured phase noise and FoM for the high, mid, and low bands versus offset frequency demonstrating lower than -150 dBc/Hz phase noise at 10 MHz offset with a FoM higher than 190 dBc/Hz across the tuning range.

10.5 Conclusion

This work presented a stacked complementary 5 GHz oscillator with very low phase noise using thin-oxide only devices. The design uses a single-turn high-k 1:1 differential transformer for the main tank at f_{LO} to achieve the highest Q with a low R_{Tank} for phase noise improvement under limited V_{DD}. The stacked topology properly divides the voltage swing between the core devices while ensuring the maximum voltage between any two device terminals does not reach $2V_{DD}$ for

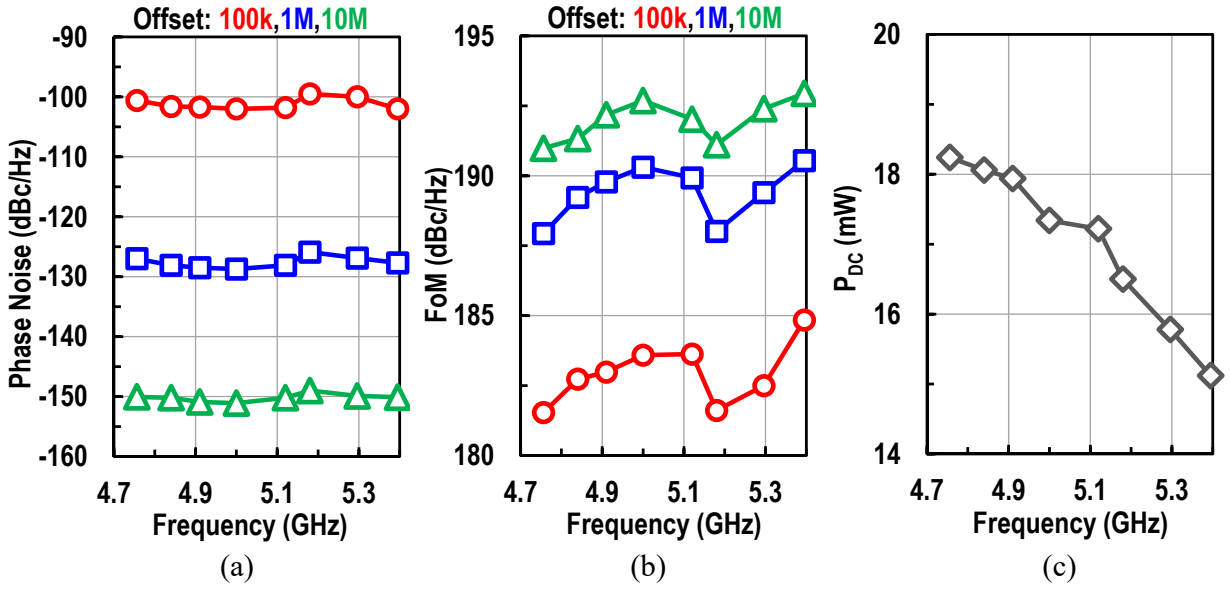


Figure 10.7: (a) Measured phase noise, (b) FoM and (c) power consumption versus the oscillation frequency.

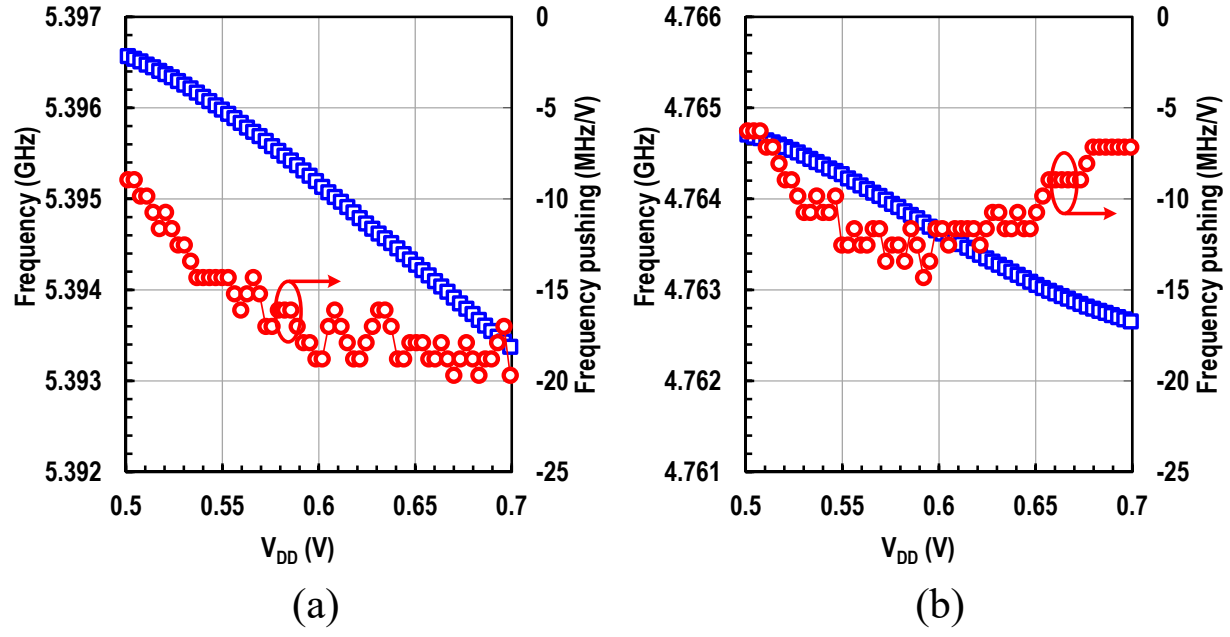


Figure 10.8: Measured supply frequency pushing for (a) the highest and (b) the lowest bands showing lower than 20 MHz/V sensitivity for a nominal 0.6 V supply.

reliability. The body-bias is exploited to set the oscillator class with 10× less noise sensitivity compared to conventional gate biasing. The complementary nature of nMOS and pMOS is

Table 10.1: Comparison with state-of-the-art low phase noise oscillators

Design			**This Work**	**[112] JSSC'15**	**[110] ISSCC'15**	**[113] JSSC'15**	**[111] JSSC'13**	**[7] ISSCC'19**
Topology			**Stacked Complementary**	Class-B with tail filter	NMOS implicit CM resonance	Class-F_2 with 2 xfrmrs	Class-D with tail filter	Folded
Technology process			**22nm FDSOI Thin**	55nm Thick	28nm Thick	65nm Thick	65nm Thin	22nm FDSOI Thin
Frequency (GHz)			**4.75-5.4**	7.4-8.4	2.85-3.75	7.2-8.7	3-4.8	4.15-4.97
V_{DD} (V)			**0.6**	1.5	0.9	1.3	0.4	0.2
Power (mW) @ f_{min} / f_{max}			**18.2/15.2**	18.4*	7.2/6.35	41.6	6.8/3.6	2.28/1.17
PN (dBc/Hz)	**@ 10 MHz**	**f_{min}**	**-150.1**	-146.8&	-152†	-149.25	-150	-142.2
		f_{max}	**-151.0**		-148†		-144.5	-144.3
FoM (dBc/Hz)	**@ 10 MHz**	**f_{min}**	**191**	190.5	192.2&	191.8&	191	191
		f_{max}	**193**	192.3			192	195.8
PN @ 10 MHz (dBc/Hz) normalized to 915 MHz			**-166.42**	-165.7	-161.9	-168.75	-160#	-159
Frequency pushing (MHz/V)			**6-20**	20*	N.R.	22-42	60-500*	40
Core Area (mm^2)			**0.2**	0.17	0.19	0.2	0.152	0.272

N.R. = Not Reported
[1] FoM = -PN + $20\log_{10}(f_o/\Delta f)$ - $10\log(P_{DC}/1mW)$
† Normalized from 5 MHz offset
& Best-case across the reported range
* Estimated from plots
# Calculated based on the provided P_{DC}

leveraged to achieve harmonic shaping for even modes ($2f_{LO}$ and $4f_{LO}$) using differential-only transformers for higher Qs compared to a traditional single-ended $2f_{LO}$ tail filter. The prototype, implemented in 22 nm FDSOI, achieves the lowest phase noise in the thermal range when compared to thin-oxide designs while using 0.6 V supply. The FoM and supply frequency pushing are state-of-the-art owing to the high switching efficiency of thin-oxide devices and the even-mode harmonic shaping.

10.6 Acknowledgment

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Chapter 10, in full, has been submitted for publication of the material as it may appear in:

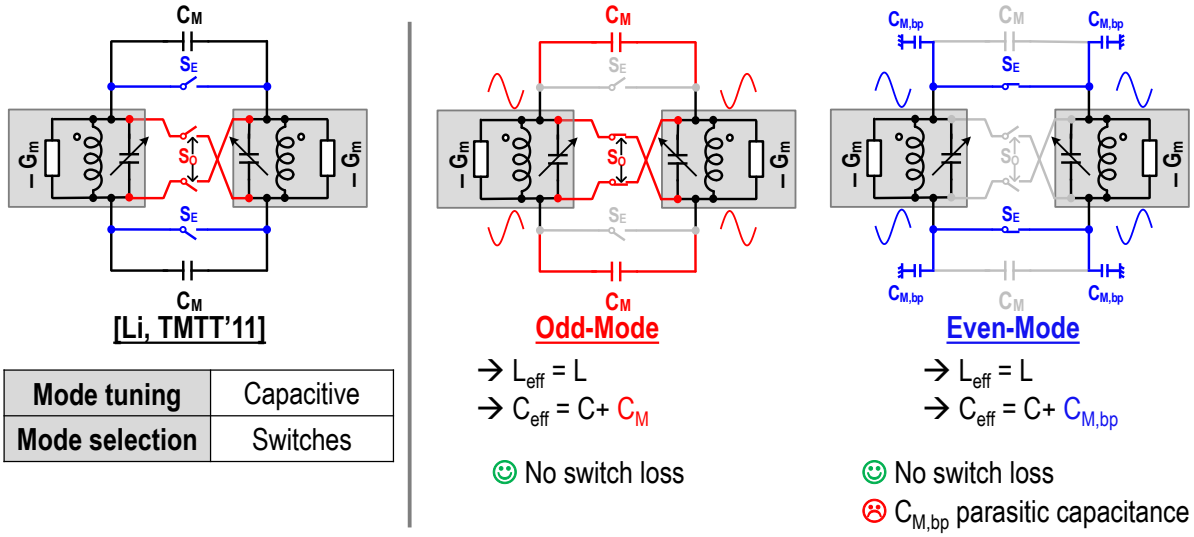
O. El-Aassar and G. M. Rebeiz, "A Stacked-Complementary 5 GHz Oscillator with Even-Only Differential Harmonic Shaping Achieving -150 dBc/Hz Phase Noise at 10 MHz Offset Using Body-Biased Thin-Oxide 22nm FDSOI," *IEEE Solid-State Circuits Letters*, submitted. The dissertation author was the primary investigator and primary author of this paper.

Chapter 11

A Dual-Core 8-17 GHz LC VCO with Enhanced Tuning Switch-less Tertiary Winding and 208.8 dBc/Hz Peak FoM_T in 22nm FDSOI

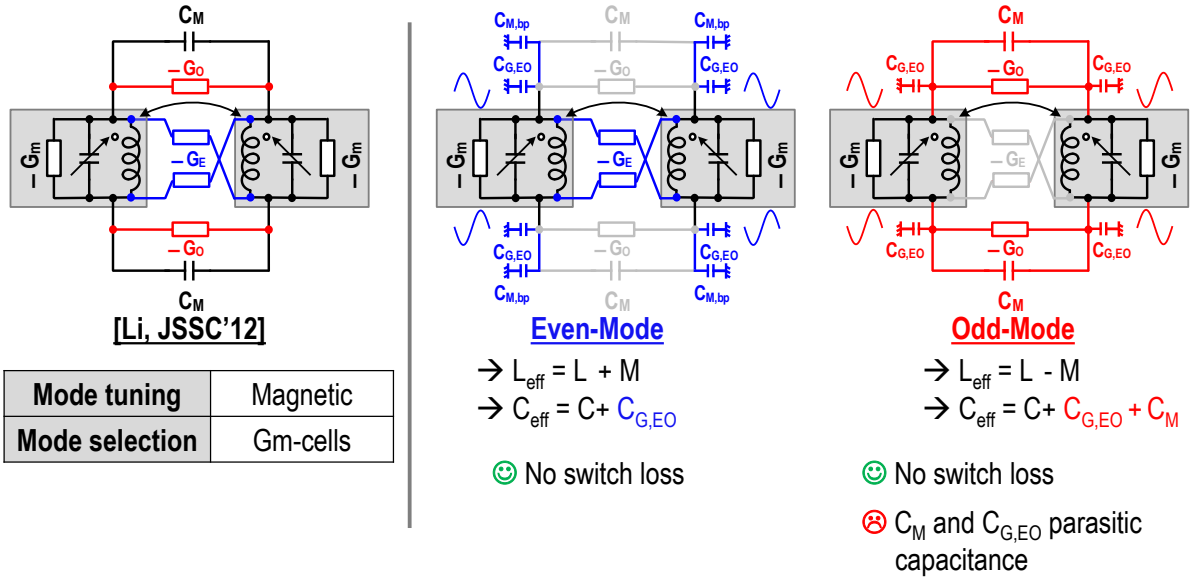
11.1 Introduction

With the proliferation of new 5G bands for both sub-6 GHz and mm-wave frequencies, multi-standard wide frequency-tuning-range (FTR) oscillators are increasingly required. The design of wide tuning VCOs is challenging in the mm-wave regime due to the limited quality factor (Q) of the tuning capacitors and switched inductors, and routing parasitics. A VCO with transformer-enhanced tuning was recently demonstrated with 30% FTR at 20-28 GHz by placing the tuning capacitors on a secondary winding away from the core [117]. Mode-switching transformer-based VCOs [118] were also developed to improve the tuning range without sacrificing the phase noise (PN). This concept was extended in [119] to the mm-wave



Mode tuning	Capacitive
Mode selection	Switches

Figure 11.1: Capacitive mode-switching.

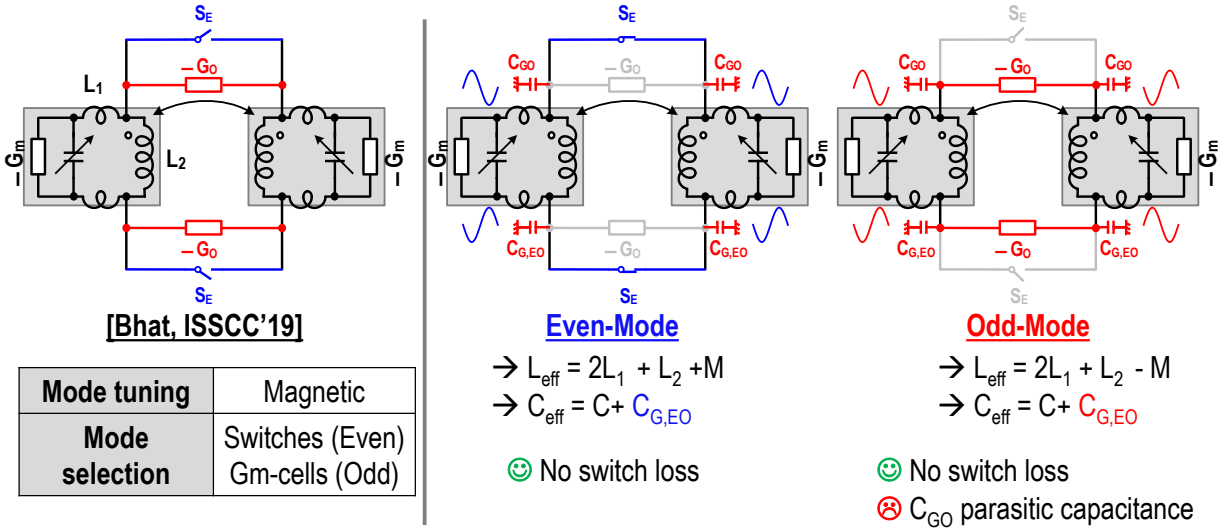


Mode tuning	Magnetic
Mode selection	Gm-cells

Figure 11.2: Resonant mode-switching.

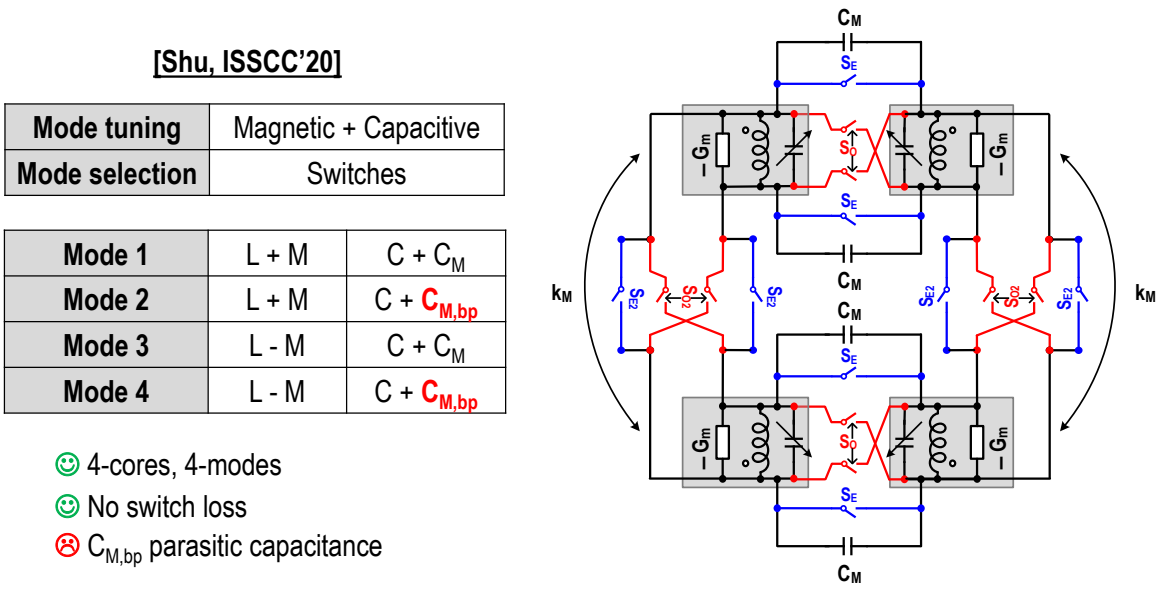
region for a dual-core 42% FTR VCO with a peak figure-of-merit-tuning (FoM_T) of 197.2 dBc/Hz at 25 GHz, and was limited by the parasitics of the mode-selection switches and capacitors.

Figs. 11.1, 11.2, and 11.3 summarize the different types of mode-switching which do not involve a switch loss [118, 120, 121]. In these topologies, switches or trans-conductors (Gm-cells) force two resonators to operate in phase (even mode), or out of phase (odd mode). The frequency



Mode tuning	Magnetic
Mode selection	Switches (Even) Gm-cells (Odd)

Figure 11.3: Inductive mode-switching.



Mode tuning	Magnetic + Capacitive
Mode selection	Switches

Mode 1	L + M	C + C_M
Mode 2	L + M	C + $C_{M,bp}$
Mode 3	L - M	C + C_M
Mode 4	L - M	C + $C_{M,bp}$

Figure 11.4: Mixed-coupling mode-switching.

tuning is achieved through inter-resonators capacitors, which are only seen in the odd-mode (capacitive switching), or an effective inductance change due to the positive and negative magnetic coupling, between both resonators, in the even and odd modes, respectively (inductive switching). A combination of both techniques can be used for a 4-resonators network to extend the number of modes to 4 (Fig.11.4) [122]. While small switches with zero current are used in these techniques,

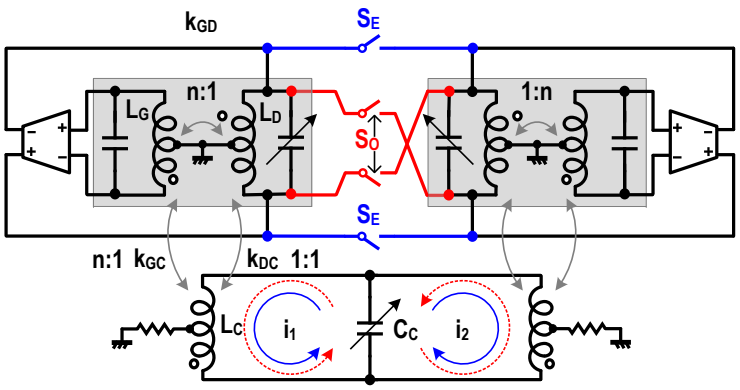


Figure 11.5: Proposed dual-core VCO with mode-switching and tertiary coupling winding.

the parasitic capacitance of the mode selection Gm-cells as well as the bottom plate capacitance of the inter-resonators capacitance usually limit the maximum achievable frequency in the high frequency mode.

This work demonstrates a dual-core dual-mode transformer-based VCO using a switch-less tertiary winding to increase the FTR without sacrificing the phase noise. The tertiary winding reduces the parasitic capacitance in the high frequency mode thereby increasing the FTR. Also, several techniques are used in the design and scaling of the capacitors bank and output buffer to reduce their loading and improve the tuning range. The fabricated VCO in 22nm FDSOI achieves a 72% FTR and a peak FoM_T of 208.8 dBc/Hz.

11.2 Dual-core VCO design

The VCO design is shown in Fig. 11.5. Two transformer-based VCOs are coupled through a network of mode switches S_E and S_O. Half of the capacitors bank is placed on the drain side L_D, while the other half (MSB) is placed on a tertiary winding L_C tightly coupled to L_D with a grounded center-tap resistance to eliminate potential common-mode resonance. In the even-mode (Fig. 11.6(a)), S_E is ON and both cores operate in phase. The current induced in L_C for both cores is also in phase, and therefore the middle node is a virtual open circuit. L_C has little effect when

C_C is small (MSB is OFF) and extends the low-band FTR when C_C is large (MSB is ON). In the odd-mode (Fig. 11.6(b)), the currents induced in L_C are opposite for both cores. This RF current circulates in the switch-less L_C loop with minimum loss and results in reduced inductance for the main tank (L_D, L_G) through magnetic coupling without sacrificing its quality factor. In this mode, the parasitics of the switched-capacitor C_C have no effect since the middle node is a virtual ground for the tertiary winding. Therefore, only half the capacitors bank and varactor on the L_D side should be sufficient for continuous tuning with some overlap with the even-mode.

No current flows in S_E and S_O for both even and odd modes (i_R = 0 mA in Fig. 11.6(a & b)). Switch sizes can thus be reduced for low parasitics. The switch R_{ON} only degrades the phase noise in case of mismatch between the two cores. A moderate size of 15/0.02 μm is therefore used with R_{ON} = 10 Ω. The simulated drain tank parallel resistance R_D varies between 95 Ω and 250 Ω at 8.4-17.4 GHz Fig. 11.6(c).

Fig. 11.7 presents the VCO circuit details. The VCO uses a folded-core topology to simulatenously achieve a low phase noise and a low V_{DD} [7]. The nMOS transistors $M_{N1,2}$ act as a common-source trans-conductance Gm-cell, followed by a folded-cascode pMOS pair $M_{P1,2}$. The outputs of the cascode pair are fed back to the nMOS gates using a voltage step-up transformer (L_D, L_G) to provide a passive voltage gain and to suppress the nMOS devices noise. The cascode devices increase the output swing on L_D for a given V_{DD} by dividing its drain impedance between the nMOS and pMOS pairs which results in low PN. The impedance division is controlled by the pMOS pair biasing, gate capacitors C_1, and the weakly coupled resonator on the folding node (k_{FD} = 0.28). A source resonator (L_S) provides an explicit current return path to the ground pad.

The loading of the VCO buffer is an important factor limiting the tuning range for mm-wave designs 11.8. A DC-coupled buffer ensures rail-to-rail operation and high driving ability at the expense of large loading capacitance on the VCO core. On the other hand, an AC-coupled buffer with a small coupling capacitor reduces the buffer capacitive loading at the expense of low buffer input swing and therefore low driving capability. Moreover, the bias resistor of an

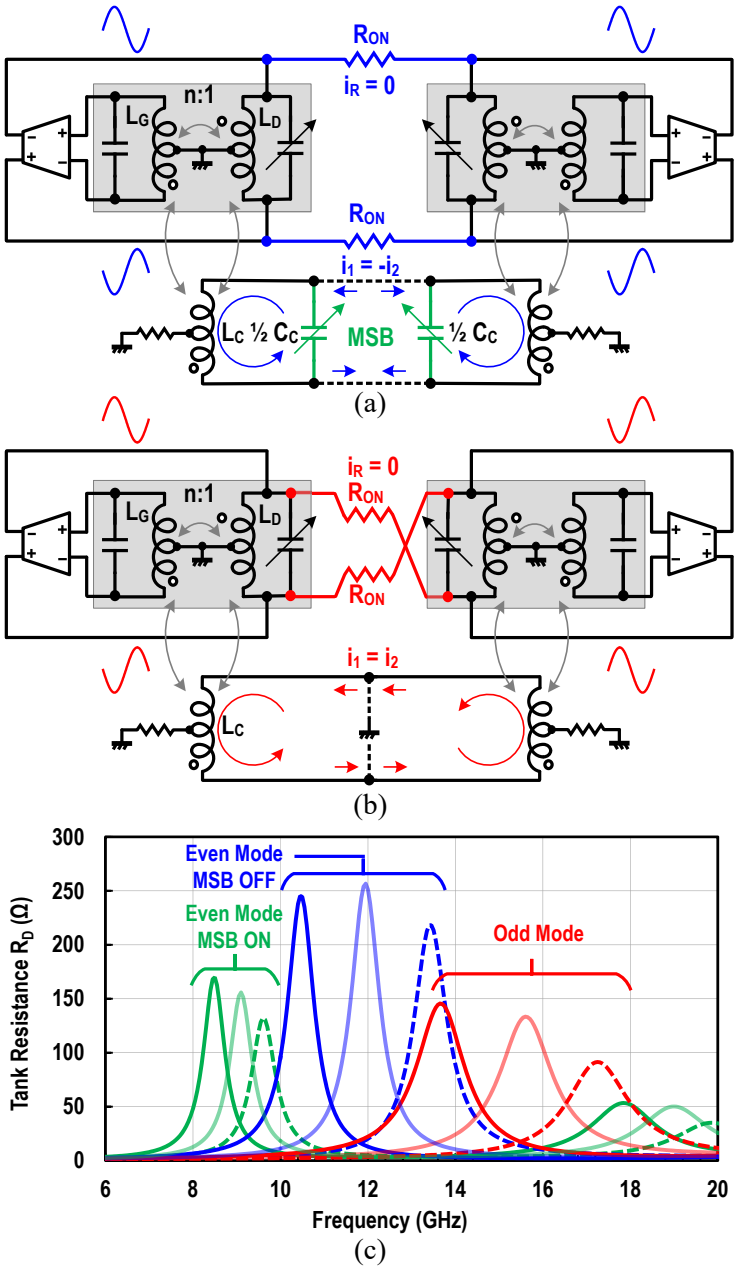


Figure 11.6: (a) Equivalent oscillator circuit in even-mode, and (b) odd-mode. (c) Simulated drain tank effective resistance R_D across the coarse tuning range.

AC-coupled buffer poses its own challenges. A large resistor results in high thermal noise on the tank nodes that can be converted to phase noise in the non-linear capacitors, but a small bias resistor loads the tank and adds to the substrate losses. In the proposed design, a DC-coupled inductive-degenerated buffer is used. A transformer positive feedback is also used between the

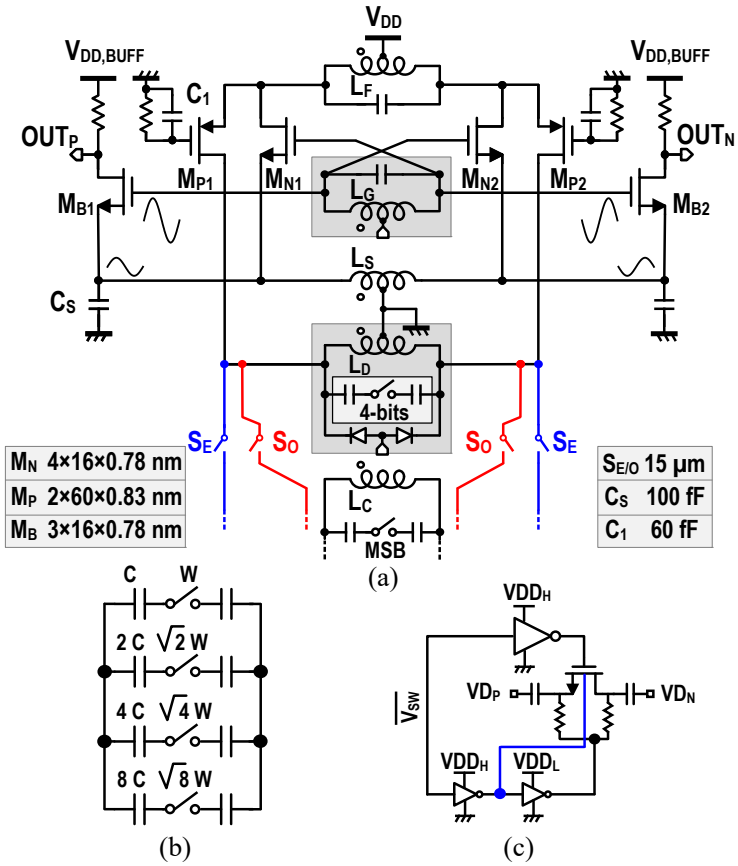


Figure 11.7: (a) Circuit schematic of the proposed VCO core and interfacing buffer (only one core is shown). (b) Drain-side capacitors bank configuration showing switches and capacitors scaling to fix Q_C across the tuning range. (c) Bit-slice of the drain capacitors bank exploiting the FBB to reduce $R_{ON}C_{OFF}$.

gate (L_G) and source (L_S) inductors for the buffer. This feedback reduces the buffer capacitive loading and results in a negative resistance contribution at the buffer input to enhance the main tank swing.

The continous tuning is achieved by an nMOS thick-oxide varactor placed on L_D side while the coarse tuning is achieved by a differential capacitors bank on L_D side with the MSB placed on L_C side. The conventional binary-weighted capacitors bank scales both the capacitors and switches simultaneously to keep a fixed $R_{ON}C$ and C_{max}/C_{min} across the tuning bits, and therefore results in a Q_C degradation as frequency increases. The capacitors bank in this work employs a more aggressive scaling where $R_{ON}\sqrt{C}$ is fixed. This results in a constant Q_C across frequency and also increases C_{max}/C_{min} and the tuning range due to the significantly lower switch

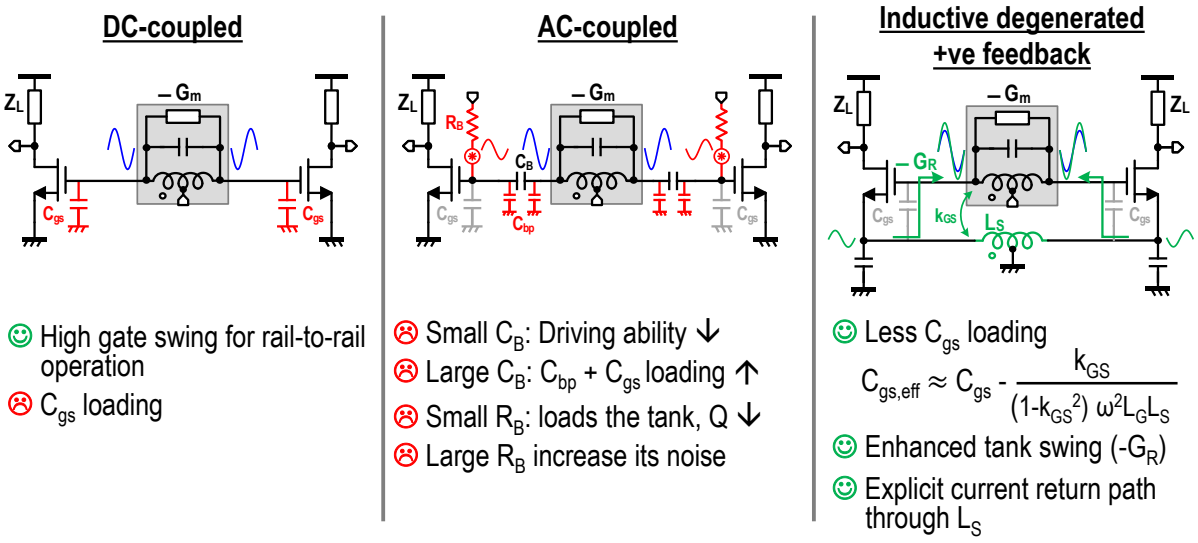


Figure 11.8: VCO interfacing buffer configurations

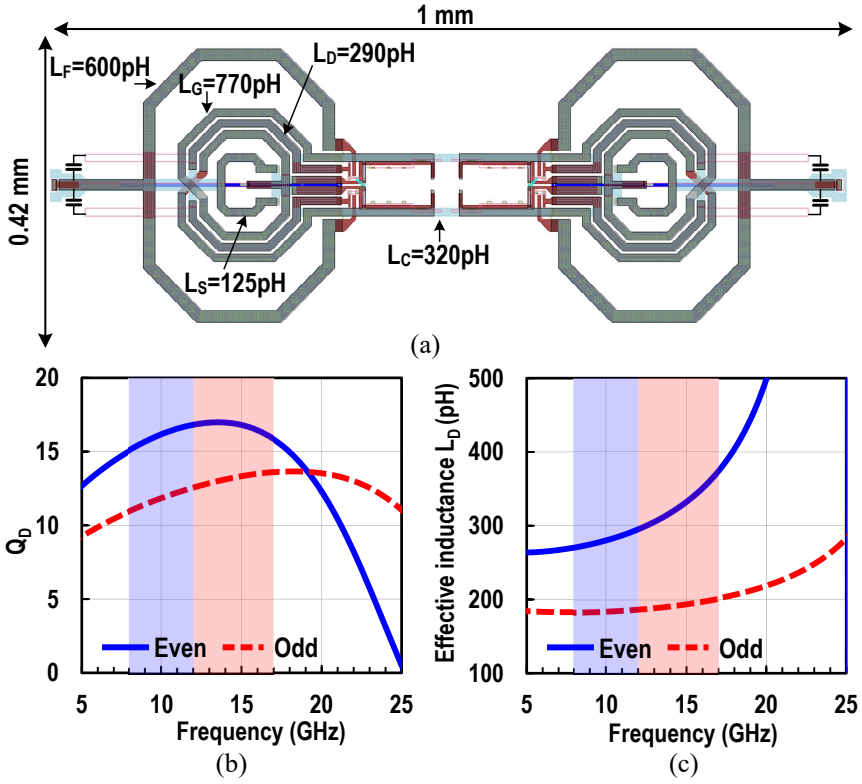


Figure 11.9: (a) Dual-core tank layout. (b) EM-simulated drain tank quality factor Q_D, and (c) effective inductance L_D, for even and odd modes.

sizes and parasitics for the MSBs when compared to binary-weighted switches (Fig. 11.7(b)). The forward-body-bias (FBB) for the nMOS switches is used to further reduce $R_{ON}C_{OFF}$ by reducing the threshold voltage, and therefore R_{ON} in the ON state (Fig. 11.7(c)).

11.3 Implementation

The dual-core VCO is implemented in the GlobalFoundries 22nm FDSOI technology process. The back-end-of-line provides 11 metal layers including two 3 μm copper metals. The main gate-drain transformer is implemented as a 2:1 turns with an inductance ratio of 2.65:1 and a k_{GD} of 0.68 at 10 GHz (Fig. 11.9(a)). The tertiary coupling winding L_C is placed directly under L_D to form a broadside 1:1 transformer with k_{CD} = 0.77 at 15 GHz. The EM-simulated drain-side transformer quality factor (Q_D) and inductance (L_D) are plotted in Fig. 11.9(b & c). In the even-mode, Q_D and L_D are $\approx$ 16.5 and 290 pH, receptively, at 10 GHz. These values reduce to 13.5 and 195 pH when operating in the odd-mode at 15 GHz with current flowing in L_C. It is important to note that a FoM degradation $<$ 1 dB using a transformer-switched design in the high-band requires a shorting switch with $R_{ON} < 1\ \Omega$. This can only be achieved using a 280 μm wide nMOS switch which will greatly limit the tuning range in the low-band.

11.4 Measurements

The die micro-graph is shown in Fig. 11.10 with a core area of 0.39 mm^2 and chip area of 1.33 mm^2 including pads. The VCO chip is assembled on a printed-circuit board with low-drop-out voltage supplies (LDOs) to provide low-noise control and bias voltages, and the chip output is probed using the GSSG pads. The tuning range is first measured with a Keysight E4448A spectrum analyzer (Fig. 11.11). The VCO operates at 8-17 GHz with a 72% continuous FTR. The VCO has a minimum frequency overlap of 440 MHz between the even and odd modes

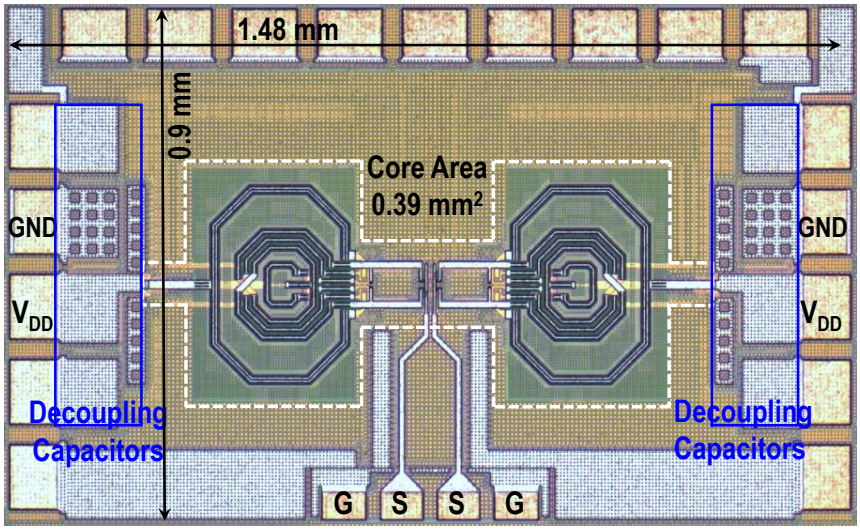


Figure 11.10: Micro-photograph of the dual-core VCO chip in 22 nm FDSOI.

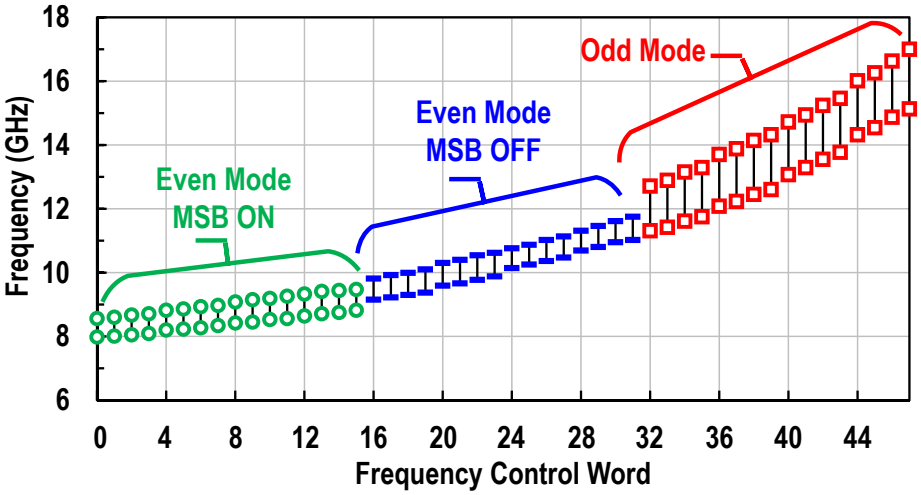


Figure 11.11: Measured frequency tuning range.

at 11 GHz, while the continuous varactor bands overlap is $> 40\%$ across the FTR.

The phase noise is measured using a Keysight E5052B signal source analyzer. The VCO output is first down-converted using a mixer and a low phase noise Keysight E8257D signal generator for the mixer LO. The E5052B also provides the low-noise DC-bias for the tuning varactors. Fig. 11.12 presents the measured phase noise at the low, mid, and high bands. When the MSB is ON, the VCO achieves a phase noise of -139 dBc/Hz at 10 MHz offset from a 7.855 GHz carrier. The phase noise and *FoM* are improved at the mid-band (MSB is OFF) reaching

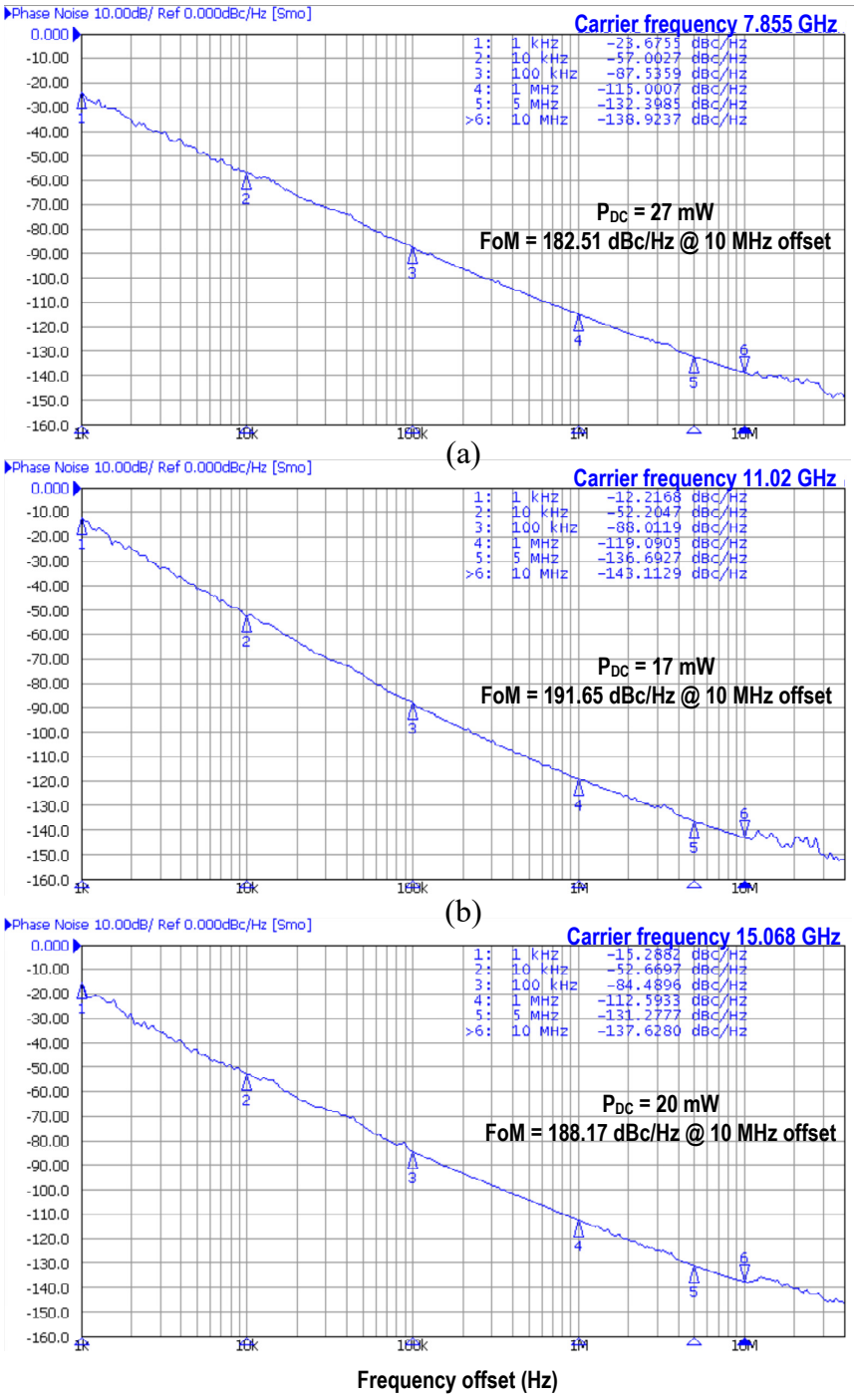


Figure 11.12: Measured phase noise for the high, mid, and low bands versus offset frequency showing a peak *FoM* of 191.65 dBc/Hz in the mid band at 11 GHz.

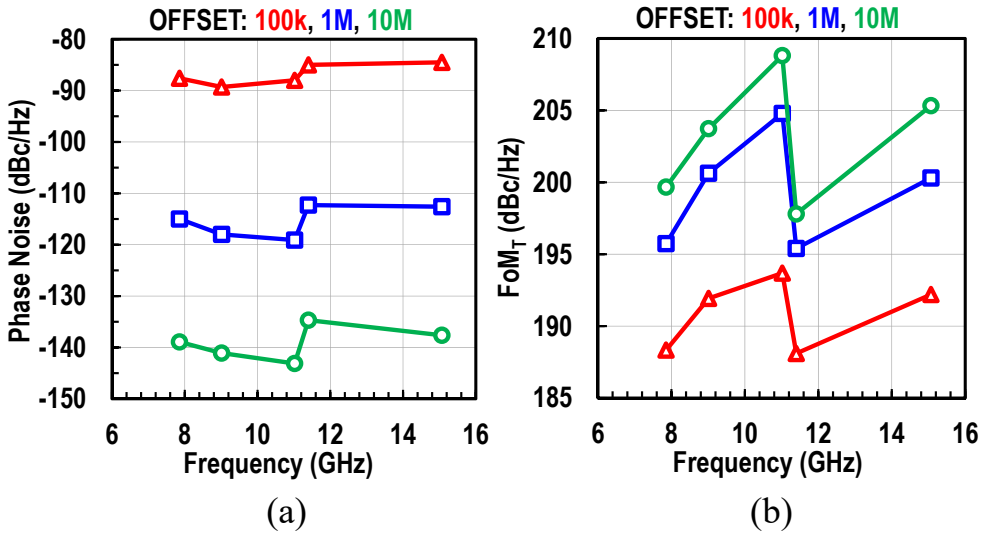


Figure 11.13: (a) Measured phase noise, and (b) FoM_T across the coarse frequency tuning range.

-143.1 and 191.65 dBc/Hz, respectively, at 11 GHz. In the high-band at 15.07 GHz, the VCO operates in the odd-mode and achieves -137.6 dBc/Hz at 10 MHz offset while consuming 20 mW with a peak FoM of 188 dBc/Hz.

The phase noise and FoM_T are measured across the tuning range for different offset frequencies in Fig. 11.13. The VCO achieves best values at mid-band with a state-of-the-art FoM_T of 208.8 dBc/Hz at 10 MHz offset with 17 mW DC power. The FoM_T is lower when the capacitors bank is fully ON for both even-mode (7.85 GHz, P_{DC} = 27 mW) and odd-mode (11.4 GHz, P_{DC} = 33 mW), but remains $>$ 198 dBc/Hz at 10 MHz offset (at all frequencies).

The effect of the varactor tuning on the phase noise and FoM is studied for the mid-band in Fig. 11.14. For all frequency offsets, the PN/FoM variation is $< \pm$ 2 dB across the varactor voltage. The measured VCO gain K_{VCO} is between 150 and 285 MHz/V when considering bands overlap.

Table 11.1 compares the proposed VCO performance with previously published works. The VCO achieves the highest FoM_T for oscillators operating over 10 GHz with the lowest V_{DD}. The VCO in [123] exhibits a lower phase noise through coupling 4 cores, while using $> 6\times$ V_{DD}, at the expense of larger area, limited tuning range and lower FoM/FoM_T. Other VCOs with

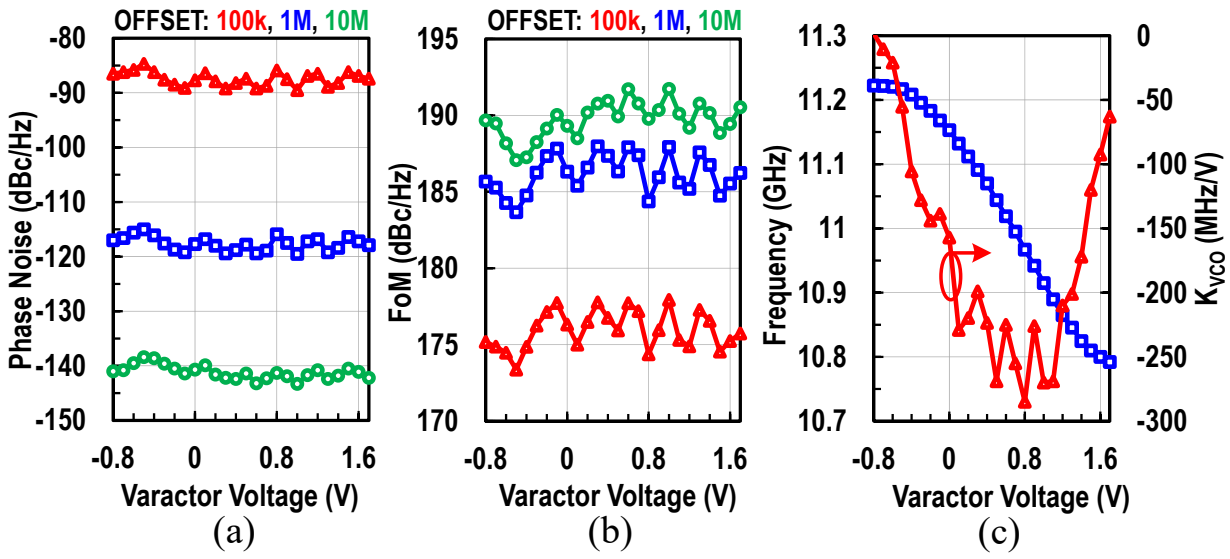


Figure 11.14: (a) Measured phase noise, (b) *FoM*, and (c) K_{VCO} across varactor voltage for the mid-band.

Table 11.1: Comparison with state-of-the-art wide-tuning oscillators

Design		**This Work**	**[124] RFIC'13**	**[118] JSSC'12**	**[123] ISSCC'18**	**[125] RFIC'15**	**[119] RFIC'18**
Topology		**Dual-Core Tri-band**	Tri-Band	Dual-Band	Quad-Core Class-C	Dual-Band	Dual-Core Dual-Band
Technology		**22nm FDSOI**	180nm	65nm	130nm SiGe	65nm	28nm
Frequency (GHz)		**8-17**	5.12-12.95	2.48-5.62	11.8-15.6	6.39-14	20.7-31.8
Tuning Range (%)		**72**	86.7	77.5	16	74.6	42.3
V_{DD} (V)		**0.45**	1	0.6	3	0.45-0.6	0.9
Power (mW)		**17-33**	5-10	9.8-14.2	72	2.2-10.3	5.5
PN (dBc/Hz)	**1 MHz**	**-119.1/-112.3**	-122.9/-112	-128.6/-121.3	-124	-110/-117*	-103.6
	10 MHz	**-143.1/-134.7**	N.R.	-151.9/-145.8	-144*	-130.3/137.7	-125
FoM @ 10 MHz (dBc/Hz)		**191.65 180.65**	189.7 185	193.7 188.8	189	188 186	184.7&
FoM_T @ 10 MHz (dBc/Hz)		**208.8/197.8**	208.5/203.8	211.5/206.6	193	205/203	197.2&
Core Area (mm^2)		**0.39**	0.33	0.294	1	0.126	0.07

[1] FoM = -PN + $20\log_{10}(f_o/\Delta f)$ - $10\log(P_{DC}/1mW)$
[2] FoM_T = FoM + $20\log_{10}$(Tuning Range/10%)
* Estimated from plots
& Best-case across the reported range

higher tuning range operate at lower frequencies [118] and achieve lower FoM/FoM_T [124, 125].

11.5 Conclusion

In this chapter, a dual-core transformer-based LC VCO with wide tuning range is proposed. A switch-less tertiary winding is introduced to couple both cores and provide half the coarse capacitive tuning for the low-band operation. This significantly reduces the parasitics on the main tank and enhances the FTR. Also, constant Q switched capacitors scaling and FBB for switches are used to increase the FTR. The VCO is combined with a mode-switching network not passing current in both even and odd modes and therefore small switches are used for low parasitics. A folded-core design is used to achieve high swing and low phase noise from a V_{DD} of 0.45 V. The dual-core VCO is DC-coupled to an inductive-degenerated positive feedback buffer leveraging the source and gate inductors of the core to reduce its parasitic capacitance loading and provide additional negative resistance to the main tank. The fabricated VCO in 22nm FDSOI process achieves state-of-the-art performance with 72% FTR from 8-to-17 GHz, the highest FoM_T and the lowest V_{DD} for carrier frequencies over 10 GHz. Such performance can be used for both sub-6 GHz and mm-waves 5G communications.

11.6 Acknowledgment

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Chapter 11, in full, has been accepted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "A Dual-Core 8-17 GHz LC VCO with Enhanced Tuning Switch-less Tertiary Winding and 208.8 dBc/Hz Peak FoM_T in 22nm FDSOI," *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Los-Angeles, accepted. The dissertation author was the primary investigator and primary author of this paper.

Chapter 12

A 16 Path All-Passive Harmonic Rejection Mixer with Watt-Level In-Band IIP3 in 45 nm CMOS SOI

12.1 Introduction

Stringent linearity requirements for wide-band receivers are usually addressed with power hungry heterodyne architectures and bulky channel selection filters. The harmonic reject mixer (HRM) is introduced to relax the RF and IF filter requirements by rejecting blockers around specific local oscillator (LO) harmonics, and therefore, improve the out-of-band IIP_3 [126]. This is achieved by synthesizing an LO signal which does not contain some harmonics by summing multiple out-phased LO paths with sinusoidal amplitude weighting. The amplitude scaling is typically implemented using trans-conductors (Gm-cells) in the RF or IF paths [127–132] which limits the in-band IIP_3 to < 0 dBm. Some systems, however, require wideband high dynamic-range receivers with very high in-band linearity such as instrumentation and base-station applications. A wide-band high linearity HRM improves the dynamic range and reduces the

channel selectivity requirements at the same time.

An 8-path passive HRM was proposed in [133] and achieves excellent in-band watt-level IIP_3 and a harmonic rejection ratio (HRR) $>$ 35 dBc for the 3^{rd} and 5^{th} harmonics for base-station applications with external high-linearity amplifiers. However, for a wide band receiver operating from the MHz range, higher LO harmonics can still fall within the receiver band and limit the overall signal-to-noise ratio. This work extends the harmonic rejection to the 13^{th} harmonic by using a 16-path all-passive HRM with 31 dBm peak IIP_3 at 1.6 GHz. A HRR $>$ 35 dBc is measured from 0.13-3 GHz for all harmonics by optimizing the layout through RF scaling resistors sharing between paths and combing the LO generation network with duty cycle control capability.

12.2 Mixer design

Fig. 12.1 depicts the all-passive HRM. The design employs 8 double balanced Gilbert-cell mixers (quads) driving the same output IF differential ports. The RF signal scaling is done in the voltage domain with resistors rather than in the current domain with Gm-cells. The omission of the Gm-cells renders the design fully passive and enhances the linearity. However, since there is no isolation between different paths in the all-passive topology, the HRM LO must provide non-overlapping clocks for the different paths.

For an N-path differential HRM all RF signals around the LO harmonics are rejected at the IF output ports except signals at $(kN \pm 1)$ LO, where k is an integer. This is satisfied provided that the IF signals at the different mixing outputs paths follow a sinusoidal amplitude pattern given by:

$$A_n = \left| \sin\left(\frac{2n}{N}\pi + \theta\right) \right|, \tag{12.1}$$

where n is the path number $\in 0$ to $N-1$, and θ is an arbitrary phase shift that can be chosen $= 0$

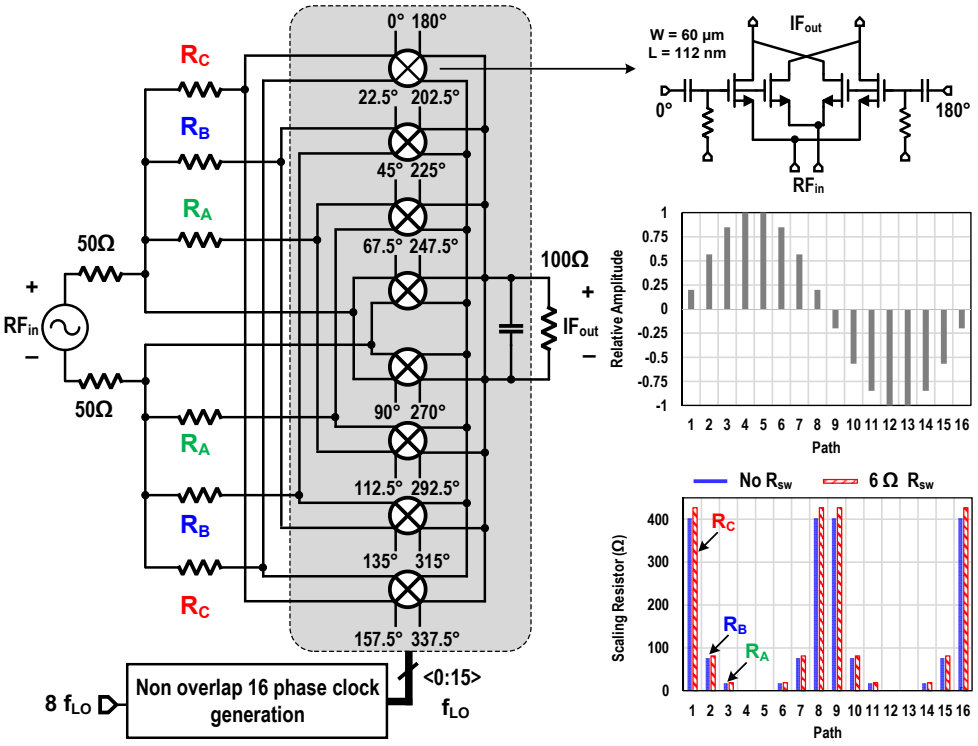

Figure 12.1: High linearity 16-path HRM using resistive scaling.

to null A for two paths and reduce the circuitry by one mixing quad. In the proposed design, $\theta = \pi/N$ which removes the scaling resistors from 4-paths and ensures a symmetric layout where each of the paths is shared between two mixing quads. Since the operation of the different paths is not concurrent, a resistive divider between the source and load impedances (Z_S and Z_L) is achieved by introducing a series resistor R_n. Therefore, the voltage of the different paths are summed on Z_L across the LO frequency cycle. Assuming an N-phase ideal non-overlapping LO clocks, the fundamental conversion gain for an all-passive N-path HRM ($G_{C,N}$) can be calculated as:

$$G_{C,N} = \text{sinc}\left(\frac{1}{N}\right) \times \frac{Z_L + Z_S}{Z_L + Z_S + R_{sw}} \times \frac{2}{N}\left|\sum_{n=0}^{N/2-1} \sin\left((2n+1)\frac{\pi}{N}\right) e^{j(2n+1)\frac{\pi}{N}}\right|. \tag{12.2}$$

The first term in (12.2) represents the conversion loss for an N-path mixer driven by a $1/N$ duty cycle square waves which is given by the fundamental component of the synthesized LO signal with N non-overlapping phases. The second term is the resistive loss due to a single mixer switch ON resistance (R_{sw}), while the third term describes the scaling loss for the different paths given by (12.1) and the vector summation of the voltage waveforms from the N paths.

The scaling resistors for the different paths can be calculated by scaling the path loss according to (12.1) and normalizing to the amplitude of the zero resistance path, where:

$$\frac{Z_S+Z_L}{Z_S+Z_L+R_{sw}+R_n} = \frac{Z_S+Z_L}{Z_S+Z_L+R_{sw}} \times \frac{\left|\sin\left((2n+1)\frac{\pi}{N}\right)\right|}{\sin(\frac{\pi}{2}\pm\frac{\pi}{N})}, \tag{12.3}$$

which results in R_n value given by:

$$R_n = (Z_S+Z_L+R_{sw}) \times \left(\frac{\sin(\frac{\pi}{2}\pm\frac{\pi}{N})}{\left|\sin\left((2n+1)\frac{\pi}{N}\right)\right|} - 1\right). \tag{12.4}$$

For a 16-path HRM, the conversion loss due to the 16-phase LO is 0.059 dB, while the implemented R_{sw} of 6 Ω contributes 0.51 dB loss. The scaling resistors reduce the gain by 2.15 dB while the voltage summation at the IF has 3.87 dB loss resulting in an overall $G_{C,16}$= −6.58 dB. Therefore, the passive resistive scaling only adds 2.15 dB to the mixer loss but results in a much higher linearity compared to Gm-cells.

In practice, $G_{C,N}$ reduces with the LO frequency due to the finite rise and fall times and layout mismatches between the different paths. The problem is exacerbated for large N where the LO duty cycle is easily affected by mismatches, which also limits the HRR. Moreover, a mismatch between rise and fall times produces a duty cycle distortion and limits the rejection of even harmonics. The proposed LO chain uses a duty cycle control circuit to trim the rise or fall time of individual paths (Fig. 12.2). A single-ended 8 × LO is buffered on chip and transformed

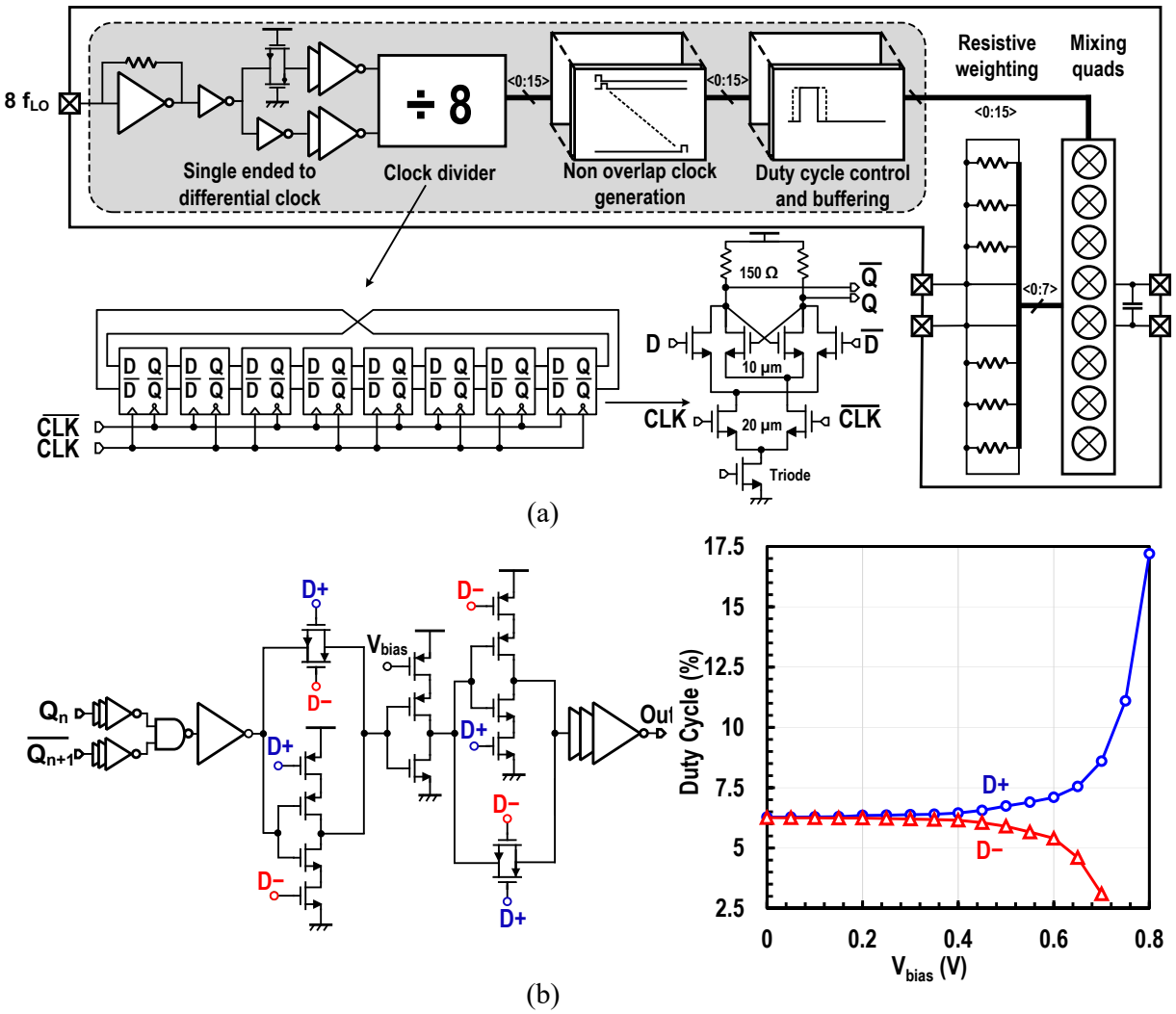

Figure 12.2: (a) Block diagram of the 16-path HRM and clock divider circuitry. (b) Non-overlap clock generation and duty cycle control.

to differential through two chains of inverters and an always-on transmission gate to equalize the delay for both paths. A current mode logic (CML) divide-by-8 produces 16-phases at LO frequency with 50% duty cycle. To extend the divider operation to 24 GHz (for an RF up to 3 GHz), the drivers are designed to provide rail-to-rail swing at its input. A transistor in triode is used instead of a current source to allow nearly rail-to-rail operation for the latch while providing some common mode rejection for differentiality. The non-overlapping clocks are obtained using NAND gates using signals from two consecutive latches with rail-to-rail input swing through a

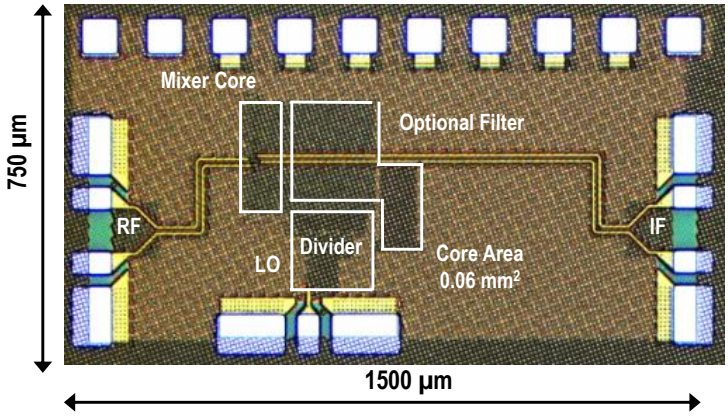

Figure 12.3: Die micro-graph of the fabricated HRM in 45nm SOI.

buffer chain to allow high frequency operation. The duty cycle control uses a current starved inverter to trim the rise time and equal delay polarity-flip logic for fall time trimming. The starved inverter can change the duty cycle from 2.5-to-9% when changing the bias voltage from 0 to 0.7 V for a 1 V nominal supply. The outputs are buffered by additional thick-oxide inverters with 1.6 V supply to increase the the LO swing for the mixing quads. An additional 30 pF capacitor is placed at the IF ports to limit the IF bandwidth to 80 MHz and improves the HRR.

12.3 Implementation and Measurement Results

Two all-passive HRM chips are fabricated in 45 nm RFSOI using thin and thick oxide devices respectively (Fig. 12.3). The thick-oxide mixing quads uses 60 μm/112 nm transistors with a simulated R_{sw} = 6 Ω and C_{off} = 30 fF. While a thin oxide variant for linearity comparison uses 30 μm/40 nm transistors with a simulated R_{sw} = 7.5 Ω and C_{off} = 16 fF. The thick oxide chip consumes 110-to-280 mW from 0.13-to-3 GHz dominated by the LO buffers. Measurements are conducted using a 4-port vector network analyzer (keysight N5247A PNA-X). The measured conversion loss for the fundamental and harmonics is shown in Fig. 12.4(a) with a 20 MHz IF signals. The gain is between 6.3-8.4 dB up-to 3 GHz while the HRR is $>$ 35 dBc for all harmonics except the 3^{rd} which degrades with frequency. This is improved by using the duty cycle control

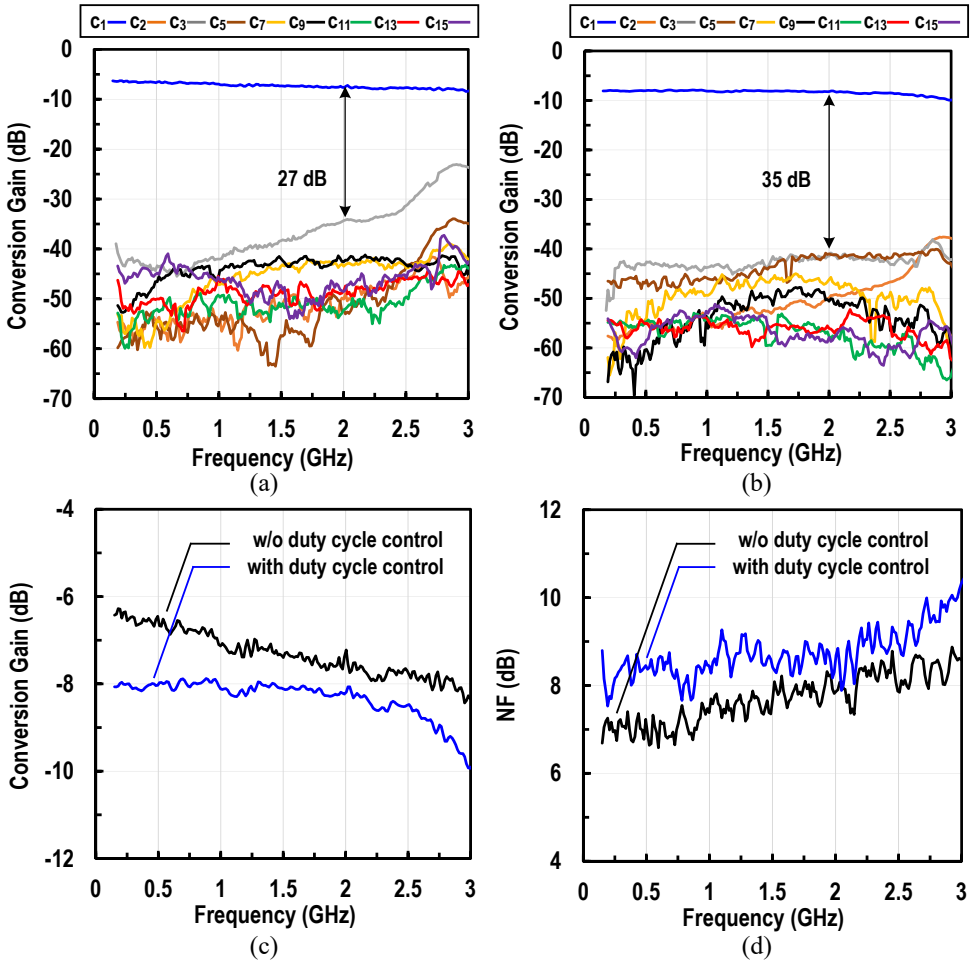

Figure 12.4: (a) Measured conversion gain at the fundamental and harmonics without duty cycle control and (b) with duty cycle control. (c) Measured conversion gain for the fundamental and 3^{rd} harmonic and (d) noise figure with and without duty cycle control.

to achieve a HRR $>$ 35 dBc for all harmonics at the expense of some gain reduction (Fig. 12.4(b, c)). The 16-path HRM should not reject the 15^{th} harmonic by more than 23.5 dB, however the passive mixer up-converts the base-band impedance to RF creating a filter with the same base-band bandwidth defined by the capacitor at the output ports which further improves the HRR. The measured noise-figure (NF) varies between 8.2-10 dB when using the duty cycle control and is very similar to the conversion gain due to the negligible NF contribution from harmonics (Fig. 12.4(d)). The conversion loss for the fundamental and 3^{rd} harmonics are measured for and RF of 2.6 GHz across the duty cycle control where up-to 20 dB improvement in the HRR can be

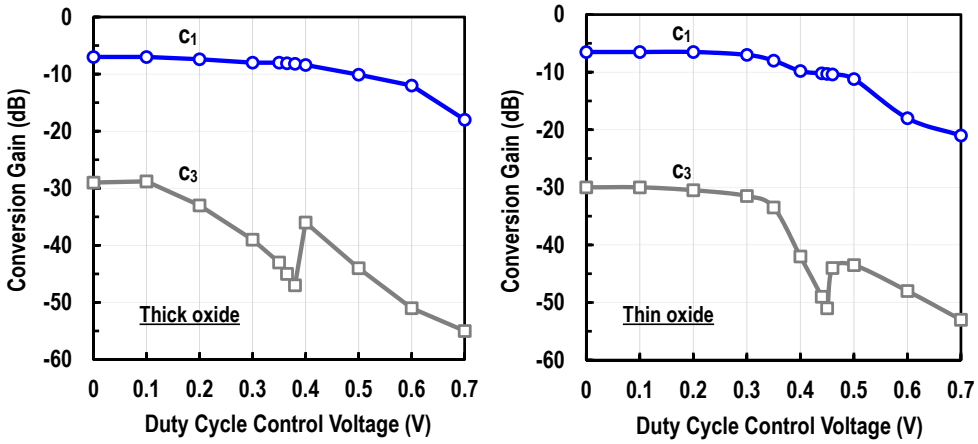

Figure 12.5: (a) Measured conversion gain at the fundamental and 3^{rd} harmonic across the duty cycle control for (a) thick-oxide mixer and (b) thin-oxide mixer.

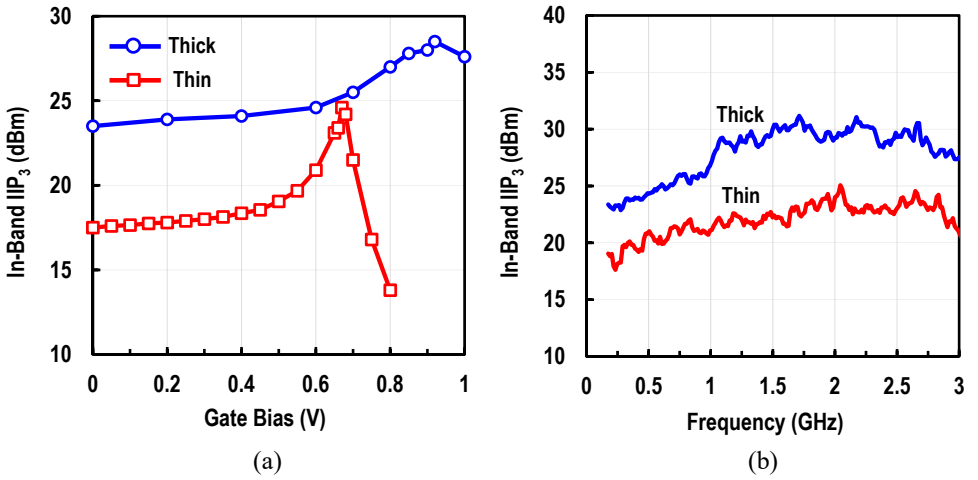

Figure 12.6: Measured in-band IIP_3 for both thick and thin oxide HRMs (a) across the gate bias voltage, and (b) across frequency.

achieved at the expense of 1-2 dB fundamental loss (Fig. 12.5).

The in-band IIP_3 is measured using 2 tones with 10 MHz separation at LO+30 MHz and LO+40 MHz to generate IM_3 tones at 20 and 50 MHz at the IF ports. The IIP_3 is first measured for a 2 GHz RF across the gate bias for the mixing quads (Fig. 12.6(a)), then by sweeping the RF frequency for this bias voltage (Fig. 12.6(b)). The thick (thin) oxide design achieves and $IIP_3 >$ 24 (20) dBm from 0.5-to-3 GHz and 31 (24.5) dBm peak IIP_3.

Table 12.1 compares the performance to harmonic reject receivers. The thick-oxide

all-passive HRM achieves the highest in-band IIP_3 and input P_{1dB} making it suitable for high linearity applications such as base-stations and instrumentation.

Table 12.1: Comparison with harmonic reject receivers

Design	[129] TMTT'10	[130] JSSC'09	[131] JSSC'10	[133] RFIC'17	This Work
Technology process	180nm	65nm	65nm	32nm SOI	45nm SOI
Frequency (GHz)	0.05-0.86	0.4-0.9	0.1-2.4	0.05-4	0.13-3
Gain	40	34	40-70	-6.4/-9.2	-8/-10
Number of phases	8	8	8	8	**16**
Number of odd harmonics rejected	2	2	2	2	**6**
HRR (dBc)	>70	60	35	>35	35
In-Band IIP_3 (dBm)	N.R.	3.5	-67	31-22	**31-24**
Input P_{1dB} (dBm)	N.R.	-22	-	11-6	**13-11**
NF (dB)	5.5	4 ± 0.5	4 ± 1	$6.4\text{-}9.5 \pm 1.2$	8.2-10.2
Supply (V)	1.8	1.2	1.2/2.5	1.1/1.5/2.1	1/1.6
Power (mW)	140	60	37-70	98-298	110-280

12.4 Conclusion

This work presented a 16-path all-passive HRM using resistive scaling. The voltage mode operation is analyzed to calculate the conversion loss and values for scaling resistors. The LO circuitry is combined with a duty cycle control to trim the rise/fall time of individual paths and maintain the HRR across frequency. The HRM achieves a state-of-the-art watt level in band IIP_3 and $>$ 35 dBc HRR for all harmonics.

12.5 Acknowledgment

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Chapter 12, in full, has been submitted for publication of the material as it may appear in: O. El-Aassar and G. M. Rebeiz, "A 16 Path All-Passive Harmonic Rejection Mixer with Watt-Level In-Band IIP3 in 45 nm CMOS SOI," *IEEE Microwave and Wireless Components Letters*, submitted. The dissertation author was the primary investigator and primary author of this paper.

Chapter 13

Future Work

13.1 Broadband and MM-Waves Amplifiers

The performance improvement for the PMOS devices to catch-up with the NMOS ones is predicted to continue with further technology scaling. This opens a spectrum of opportunities and circuit topologies not typically used in the mm-waves regime. First, the reported improved high voltage tolerance compared to NMOS need to be assessed through reliability measurements for the PMOS-only DPA proposed in chapter 2. A better PMOS reliability can favor a "folded-stack" power amplifier topology where the output device sustaining most of the voltage stress is a PMOS while the RF current generation device is an NMOS for high gain. This can be accompanied with innovative harmonic shaping and bias network at the folding node. An exemplary network is proposed for the VCO in chapter 8 for phase noise suppression. Similar concept can be extended to power amplifiers for power and efficiency improvement. In addition, the complementary push-pull power amplifiers design (such as class-D) can be extended to the 5G bands.

The multi-drive inter-stack coupling and multi-drive intra-stack coupling techniques were exploited in chapters 3, 4, and 5 for broadband DPAs. Similar techniques can be leveraged for other broadband circuits. A broadband 100+ GHz 2-stack low-noise amplifier is implemented in

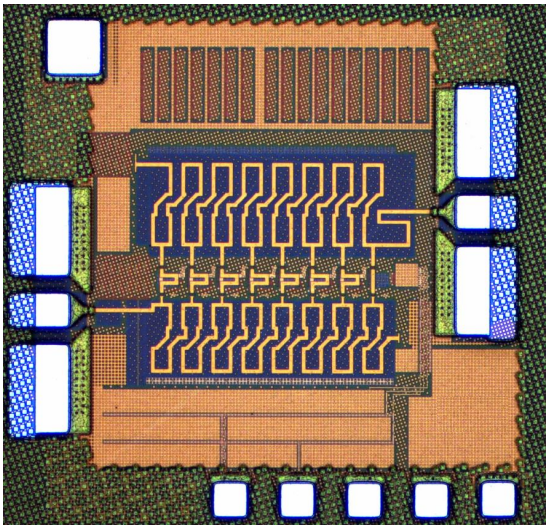

Figure 13.1: Chip micro-graph of the fabricated distributed 2-stack LNA in 45 nm CMOS SOI.

45 nm CMOS SOI using the same technique for low noise performance rather than high power (Fig.13.1). The noise benefit over conventional and series peaked low-noise distributed amplifiers happens at high frequencies when the inter-stack coupling is effective. This is expected since the forward gain extends to a higher frequency leading to reduced noise contribution from the input termination. Additionally, the source impedance of the stacked devices remain high to a higher frequency, degenerating their noise and minimizing their contribution in the noise figure.

The multi-drive inter-stack coupling can be implemented for distributed wireline circuits. One example is a distributed muli-level PAM modulator fabricated in 45 nm CMOS SOI (Fig. 13.2). This modulator can synthesize a M-PAM signal (8-PAM in the fabricated chip), while using high efficient switched-mode stages, thereby improving the energy per bit for tens of Gb/s data rates. At the same time, feed-forward-equalization (FFE) taps are available when operating in the PAM-2 (NRZ) or PAM-4 modes of operation.

The work is extended to differential-signaling by implementing a complete differential serializer employing the same techniques in the driver stage in 45 nm CMOS SOI. The serializer is expected to achieve 100+ Gb/s for NRZ and PAM-4 signals with record differential peak-to-peak output swing (Fig. 13.3).

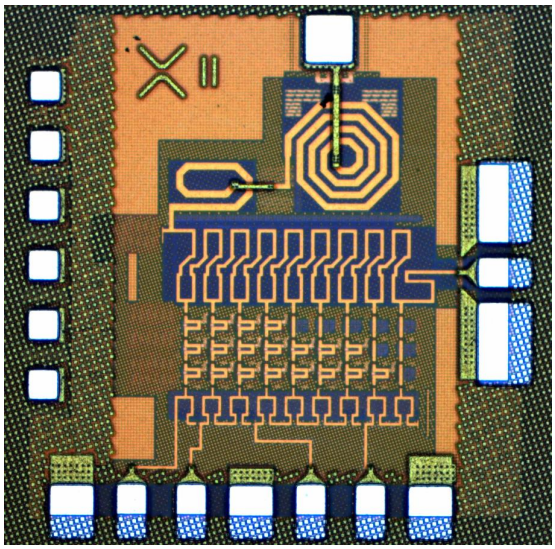

Figure 13.2: Chip micro-graph of the fabricated distributed PAM modulator in 45 nm CMOS SOI.

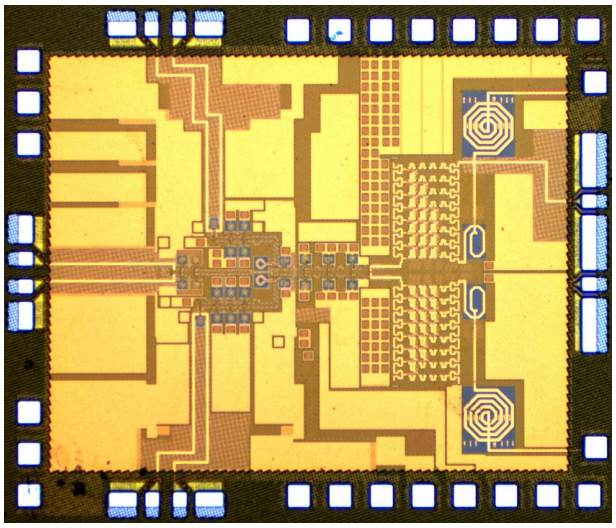

Figure 13.3: Chip micro-graph of the fabricated serializer in 45 nm CMOS SOI.

Finally, the multi-drive coupling techniques can also be realized in non-distributed topologies where only a single stage is needed for the multi-drive intra-stack coupling or two-stages for the multi-drive inter-stack coupling. These techniques compensate for the stack loss and can prove beneficial in high frequency operation such as for D-band applications, as well as for amplifiers with back-off efficiency enhancement such as Doherty and outphasing.

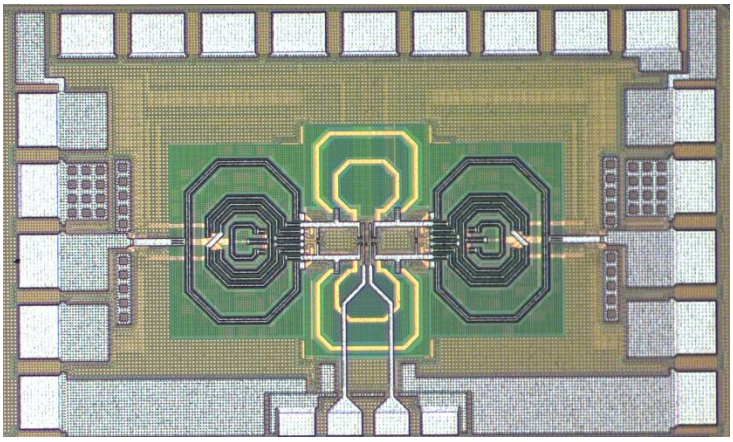

Figure 13.4: Chip micro-graph of a fabricated VCO with over 100% tuning range in 22 nm FDSOI.

13.2 Low-Noise Amplifiers

The better PMOS devices can be exploited to design CMOS LNAs in the 5G bands. These can offer several benefits compared to NMOS-only designs in particular for low even order distortion. Most importantly the superior IIP_2 which can be challenging in single-ended stages (typically the first stage of the LNA). In such a design, the body-bias in FDSOI technologies can be exploited as a trimming node for both NMOS and PMOS with a much lower sensitivity compared to the conventional gate bias.

13.3 Oscillators

The frequency tuning techniques presented in chapter 11 enabled 3 modes of operation for a dual-core VCO without incurring switch loss. These can be extended by increasing the number of cores and/or tuning mechanisms to achieve over 100% tuning range and allow multi-band frequency generation using a single synthesizer (Fig. 13.4).

13.4 Mixers

The body-bias was used in the capacitors bank of the VCO proposed in chapter 11. A similar biasing scheme can be extended to passive mixers as well as RF switches when implemented in FDSOI to minimize the ON resistance and prevents un-intentional turn ON during the OFF state. Thereby, the conversion loss is reduced while the linearity is improved. Finally, the concept of an all-passive HRM can be generalized to include image rejection in addition to harmonic rejection by incorporating two all-passive HRMs driven by quadrature LO signals and using the same LO generation and duty cycle control circuitry proposed in chapter 12. This can allow watt level IIP_3 with image rejection for high linearity instrumentation.

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