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Stability of the Baseline Holder in Readout Circuits For Radiation Detectors

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Abstract

Baseline holder (BLH) circuits are used widely to stabilize the analog output of application-specific integrated circuits (ASICs) for high-count-rate applications. The careful design of BLH circuits is vital to the overall stability of the analog-signal-processing chain in ASICs. Recently, we observed self-triggered fluctuations in an ASIC in which the shaping circuits have a BLH circuit in the feedback loop. In fact, further investigations showed that methods of enhancing small-signal stabilities cause an even worse situation. To resolve this problem, we used large-signal analyses to study the circuit's stability. We found that a relatively small gain for the error amplifier and a small current in the non-linear stage of the BLH are required to enhance stability in large-signal analysis, which will compromise the properties of the BLH. These findings were verified by SPICE simulations. In this paper, we present our detailed analysis of the BLH circuits, and propose an improved version of them that have only minimal self-triggered fluctuations. We summarize the design considerations both for the stability and the properties of the BLH circuits.

Index Terms

ASIC; Baseline holder; Large-signal analyses; Stability; Transient-noise analyses

I. Introduction

Room-temperature semiconductor radiation detectors, such as those made of cadmium zinc telluride (CdZnTe or CZT) are attractive for applications in x-ray and gamma-ray spectroscopy and medical-imaging because of their high energy resolution, compactness, and ability to operate at room temperature [1]–[3]. The signals generated by these detectors are relatively weak; thus, readout circuits with a high gain are needed to achieve a good signal-to-noise ratio (SNR). When the readout channel is DC-coupled to the detectors, and by using a unipolar shaping-network, the output of the readout channel will shift towards the power, or to ground, due to the leakage current of the detectors and the increased event rate.

Previously, a baseline holder (BLH) circuit was developed to stabilize the output baseline by establishing a low-frequency feedback loop to the shaping circuits without introducing extra noise or instabilities [4]. Compared to AC coupling, the non-linear response of the BLH can minimize baseline shifting at high event-rates. Such a BLH was successfully implemented in several different application-specific integrated circuits (ASICs) [5]–[11].

Recently, we observed self-trigged triangular-shape fluctuations on the baseline of an ASIC using a BLH circuit (Fig. 1). We found no issue of stability in the shaper-BLH closed loop, either by small-signal analysis, or by SPICE simulation. However, the observed slow recovery time, similar to the response of the BLH to an injected signal opposite to the expected polarity, led us to analyze the large-signal response of the circuit to the noise and other perturbations. In Section II, we discuss the stability of the BLH circuit both in small-signal and large-signal analyses; it suggests that there is a trade-off between the stability and performance of the BLH circuit that ensures the stability of the circuit in a large-signal response. In section III, we discuss some improved circuit structures. In section IV, we detail our use of the SPICE simulation to validate our analyses, and to obtain the time-domain response of BLH to the noise on the baseline using transient-noise analysis. Some factors revealed by this simulation, significantly degrade the large-signals' stability, as is discussed in Section V. The circuits are implemented in a 0.25-μm CMOS technology with a 2.5-V power supply.

II. Analysis of BLH stability

Generally, the baseline holder is inserted into a feedback loop including the entire shaping stage, as shown in Fig. 2. We assumed that the input current signal, $I_i(t)$, viz. the output of the charge-sensitive amplifier (CSA), is unipolar, and that the leakage current has the same direction as the signal, as is common in CZT-based detector systems. The baseline holder has two functions: 1) Minimizing the variations of the output baseline caused by the leakage (DC) current, which is occasioned by the low-pass stage; and, 2) limiting the negative shift of the baseline caused by signals at high rates, which is fulfilled by the non-linear stage. This closed loop must be stable to prevent oscillations, as discussed in Ref. [4].

A. Properties and small-signal stability of BLH

We implemented a BLH circuit similar to the one described in [4], which is shown in Fig. 3. Both the non-linear stage and the low-pass stage were built using source followers due to their simple structure and low power consumption, as is needed in applications with a high channel-density. The source followers are biased at a tiny current (around 10 nA for the NL stage, and 10 pA for the LP stage [4]) to drive large capacitors so hence, the slew rates are limited, and a non-linear I-V response to larger input signals is implemented. The BLH is designed for unipolar signals, while $V_{out}(t)$ is positive, as shown in Fig. 2.

To simplify the analysis, the shaper in Fig. 2 is assumed to be a single-pole low-pass filter with a transfer function $H(s) = H(0)/(1 + s\,\tau_{SH})$, where τ_{SH} is the time constant, and $H(0)$ is the DC trans-impedance gain. Given the voltage gain, A_{AMP}, of the error amplifier, and the trans-conductance, g_0, of the V-to-I output stage, the frequency response of the BLH can be modeled as a low-pass filter with two poles, as depicted in (1), where $\omega_{NL} = I_{NL}/(nV_TC_1)$ and $\omega_{LP} = I_{LP}/(nV_TC_2)$ respectively are the pole frequencies of the non-linear stage and the low-pass stage, I_{NL} and I_{LP} are the bias currents of both stages, and C_1 and C_2 are the load capacitors.

$$\frac{i_F(s)}{V_{\text{out}}(s)} = \frac{A_{AMP}g_0}{\left(1+\frac{s}{\omega_{NL}}\right)\left(1+\frac{s}{\omega_{LP}}\right)} \quad (1)$$

$V_T = kT/q$ is the thermal potential with a value of 25.8 mV at 300 K, and n is the sub-threshold slope factor of MOSFETs. Next, we rewrite some important conclusions from [4] to assist our further discussions here.

1. *Small-signal stability:* When ω_{LP} is set much lower than ω_{NL} and $1/\tau_{SH}$, the following requirements should be met for assuring enough phase-margin in the Shaper-BLH system. Generally, the left should be at least one to two orders-of-magnitude smaller than the right.

$$\begin{cases} A_{\text{loop}}\omega_{LP} << \omega_{NL} \\ A_{\text{loop}}\omega_{LP} << 1/\tau_{SH} \end{cases} \Rightarrow \begin{cases} H(0)A_{AMP}g_0(I_{LP}/C_2) << I_{NL}/C_1 \\ I_{LP}/C_2 << nV_T/H(0)A_{AMP}g_0\tau_{SH} \end{cases} \quad (2)$$

   $A_{loop} = H(0)\,A_{AMP}\,g_0$ is the DC gain of the loop.

2. *Close-loop DC gain:* Under (2), the close-loop response and its DC gain, A_{cl}, can be approximated by (3) and (4) [4].

$$\frac{V_{\text{out}}(s)}{I_i(s)} \approx H(s) \times \frac{\left(1+\frac{s}{\omega_{LP}}\right)}{A_{\text{loop}}\left(1+\frac{s}{A_{\text{loop}}\omega_{LP}}\right)} \quad (3)$$

$$A_{cl} = \frac{H(0)}{A_{\text{loop}}} = \frac{1}{A_{AMP}g_0} \quad (4)$$

A_{cl} indicates the baseline gain to the input leakage current that should be minimized.

3. *High-rate performance:* In ref. [4], when the event rate R_t of the input current pulses is high, the baseline shift was described by (5), where V_{dd} is the supply power voltage, and τ_P is the peaking time of the output signal.

$$\Delta V_{\text{out}} \approx -2V_{dd}\tau_P R_t \frac{K_a}{A_{AMP}} \quad (5)$$

The coefficient K_a is a constant at $\omega_{NL} < 1/(6\tau_P)$, and increases as ω_{NL} thereafter.

Equations (4) and (5) suggest the need for a larger A_{AMP} and g_o to assure the better performance of the BLH. Equation (2) reveals that, for good small-signal stability, the slew rate of the low-pass stage (I_{LP}/C_2) should be low, while that of the non-linear stage (I_{NL}/C_1) should be relatively large. Considering the compromise between (2) and $\omega_{NL} < 1/6\tau_P$, ω_{NL} should have the same magnitude as $1/\tau_{SH}$. It is noteworthy that as long as the second pole of the open-loop $\omega_{NL} < 1/\tau_P$, increasing I_{NL}/C_1 will enhance the circuit's stability.

The parameters of BLH in the tested ASIC are listed in Table I; the AC sweep simulation by the Silvaco® SmartSpice simulator showed that a small-signal phase-margin of more than 90 degrees was achieved. Nevertheless, the closed loop still exhibited instability, and the self-trigged negative pulses on the baseline without signal inputs, as shown in Fig. 1, and increasing I_{NL}/C_1 actually worsened the oscillation, that is, in contrast to the small-signal analysis. Hence, we decided further to investigate the stability of the BLH by analyzing the circuit's large-signal response.

B. Transient response of the low-pass stage, and the large-signal stability of the BLH

Since the pole of low-pass stage should be set at an extremely low frequency, and implementing large capacitors on the chip is impractical, the low-pass source follower must be biased at a very small value, typically no more than 100 pA. Thus, the MOSFET of the source follower works in the sub-threshold region; its I_d-V_{gs} relationship is exponential rather than square [12], leading to a big variation in the trans-conductance, $g_m = I_d/nV_T$, even when the operation point changes only slightly. In this case, the large-signal response of MOSFET should be used to calculate the transient current, I_d, when V_{gs} is changed.

Fig. 4 is a detailed circuit of the low-pass stage. In the static state, (6) is used to describe the relationship between I_{LP} and the static voltages V_{NL0} and V_{LP0} of $V_{NL}(t)$ and $V_{LP}(t)$ [12],

$$I_{LP} = \left(\frac{W}{L}\right)_{M1} I_0 e^{\frac{V_{LP0}-V_{NL0}}{nV_T}} \quad (6)$$

where I_0 is a process-dominant parameter, and W and L, respectively, are the width and length of M1. In our design, W/L is 0.48 μm/4.08 μm for *M1*, and 0.48 μm/19.08 μm for *M2*. Both ratios are small enough to ensure a very low static current in the low-pass stage.

When there is no signal, the noise generated by the detector's leakage current and the front-end circuits may cause a small increase in the baseline voltage injected into the error amplifier of the BLH. If the output at the error amplifier $V_{amp}(t)$ is large enough, the output voltage of the non-linear stage $V_{NL}(t)$ decreases linearly with a slope K equal to the slew rate of non-linear source follower, I_{NL}/C_1 (7).

$$V_{NL}(t)=V_{NL0}-Kt, K=I_{NL}/C_1 \quad (7)$$

The transient current $I_d(t)$ of the source follower then will discharge the capacitor, C_2, causing a decline in the output of the low-pass stage $V_{LP}(t)$. The following equations can be used to describe this process.

$$I_d(t)=\left(\frac{W}{L}\right)_{M1} I_0 e^{\frac{V_{LP}(t)-V_{NL}(t)}{nV_T}} \quad (8)$$

$$I_C(t)=C_2\frac{dV_{LP}(t)}{dt}=I_d(t)-I_{LP} \quad (9)$$

Equations (6)–(9) can be transformed into a Riccati equation of $I_c(t)$ with $I_C(0^+)\approx 0$ and can be solved as follows:

$$I_C(t)=\frac{e^{Kt/nV_T}-e^{(I_{LP}/nV_TC_2)t}}{e^{(I_{LP}/nV_TC_2)t}-\frac{I_{LP}}{C_2K}e^{Kt/nV_T}}I_{LP} \quad (10)$$

Considering the assumption in Section A, $I_{LP}/C_2 << K$, (10) can be approximated to (11) during the discharging process.

$$I_C(t)\approx\left(e^{Kt/nV_T}-1\right)I_{LP}, 0<t\le t_{\text{dis}} \quad (11)$$

$$I_{C\,\max}=I_C(t_{\text{dis}})=\left(e^{Kt_{\text{dis}}/nV_T}-1\right)I_{LP}$$

Here, t_{dis} refers to the total time of such discharging process to C_2 when $V_{NL}(t)$ decreases at a constant rate, K.

Equations (10) and (11) indicate that the decrease on $V_{LP}(t)$ is smaller than the decrease on $V_{NL}(t)$, and $I_d(t)$ (as well as $I_C(t)$) will increase exponentially with time, with a time constant of nV_T/K. This transient change of $I_C(t)$ is much bigger than small-signal analysis, wherein $I_C(t)$ is close to $(g_mK)t\approx(I_{LP}K/nV_T)t$. As is the case in our ASIC, within a duration t_{dis} of $6\tau_{SH}$=1 μs (twice the peaking time of a 3rd CR-RC shaper [13]) it will generate $I_{Cmax}\approx 130I_{LP}$, viz., much larger than the designed bias current.

The discharging current $I_C(t)$ will cause an increase of the feedback current $I_f(t)$ shown in Fig. 2 with a peak value of I_{fp} (12). As $I_f(t)$ also increases exponentially with a time

constant, nV_T/K, comparable to τ_{SH}, the baseline according could even drop below the original value, leading to increase of $V_{NL}(t)$ and a cessation of the discharging process at the time t_{dis}.

$$I_f(t) \approx -g_0 V_{LP}(t) = -\frac{g_0}{C_2}\int_{0^+}^{t} I_C(t)dt = g_0\left(\frac{I_{LP} nV_T}{C_2 K}\left(e^{\frac{K}{nV_T}} - 1\right) - \frac{I_{LP}}{C_2}t\right) + I_f\left(0^+\right), \quad (12)$$

$$0 < t \le t_{\mathrm{dis}}$$

$$I_{fp} = I_f(t_{\mathrm{dis}}) \approx \frac{g_0 I_{LP}/C_2}{K/nV_T} e^{\frac{K}{nV_T}t_{\mathrm{dis}}} = \frac{g_0}{C_2 K/nV_T} I_{c\ \max}$$

After that, as shown in Fig. 5, $I_d(t)$ will decrease exponentially to almost 0. The falling time t_f of $I_d(t)$ (as well as $I_C(t)$) is smaller than t_{dis} because both the drop of $V_{LP}(t)$ and the increase of $V_{NL}(t)$ will force $M1$ in LP stage to cut off quickly. However, it is determined by the time-domain response of the shaping circuit, the error amplifier and the NL stage altogether. A SPICE simulation can be used to derive the accurate value of t_f, which is explained in Section IV.A. Since $I_f(t)$ is the integration of $I_C(t)$, the peak value I_{fp} can be multiplied by a simple factor λ, which is related to the ratio of $(t_{dis}+t_f)/t_{dis}$. After that, the charging current to C_2 is almost constant and equal to I_{LP}, and $I_f(t)$ is:

$$I_f(t) = -g_0 V_{LP}(t) \approx -g_0 \frac{I_{LP}}{C_2}(t - t_{\mathrm{dis}}) + I_{fp}, t > t_{\mathrm{dis}} \quad (13)$$

Thus, in a case when signals with polarity opposite to the normal detector signals are injected, the baseline voltage will recover in a very slow rate proportional to I_{LP}/C_2. During this recovery period, M1 is cut-off so there is no discharging on C_2 until the baseline returns to the normal value.

Therefore, a negative triangular-shaped voltage pulse will occur at the baseline, similar to the measurement in Fig. 1. The entire process is depicted in Fig. 6, which agrees with SPICE simulation discussed later in this paper. During the charging process, the variation rate $g_0 I_{LP}/C_2$ of the $I_f(t)$ baseline is slow compared with $1/\tau_{SH}$, and thus, the $I_f(t)$ can be approximated by a step function, while the DC trans-impedance $H(0)$ of the shaper can be used to calculated the peak amplitude of the negative pulse:

$$V_{fp} \approx H(0) I_{fp} = \frac{H(0) g_0}{C_2 K/nV_T} I_{C\ \max} \quad (14)$$

Such a pulse, triggered by the noise, cannot be derived using only small-signal analysis and can occur randomly over time with and without signal inputs, so resulting in random fluctuation on the baseline. Thus, we suggest that large-signal stability should be considered, wherein the height of the negative pulse in (14) should be smaller than the noise level, V_P itself, at the baseline.

$$V_{fp}<V_P \quad (15)$$

To calculate the discharging time t_{dis}, we assumed that the noise pulses at the baseline bear a similar normalized waveform $h(t)$ as do the signals with amplitude of V_P, and that they are separated from the following negative triangular pulses caused by the feedback. During the discharging process, the output of the error amplifier $V_{amp}(t)$ can be estimated as $A_{AMP}V_p h(t)$. Then, t_{dis} is the time when $V_{amp}(t)$ goes across $V_{NL}(t)$ at the lagging edge (i.e., after the peaking time, t_p), before which the slope of $V_{NL}(t)$ is limited to the slew rate K, as explained in Fig. 6.

$$\begin{cases} A_{AMP}V_p h(t_{\rm dis})=Kt_{\rm dis} \\ t_{\rm dis}>t_p \end{cases} \quad (16)$$

Equation (16) can be solved numerically. For the 3rd CR-RC shaper in the test ASIC, and using the parameters in Table I, we found that the result of $e^{Kt_{dis}}$ will increase when either $A_{AMP}V_P$ or K increases, as shown in Fig. 7. Particularly, an increase in K will cause an almost exponential increase of e^{Kt_{dis}/nV_T} (i.e., I_{Cmax} and V_{fp}), which entails a heavier instability on the baseline. Also, it should be considered that when more than two noise-pulses occur simultaneously, their overlap can generate t_{dis} much larger than the solution to (16), leading to an exponential increase of V_{fp}. Thus the assumption of t_{dis} should be larger, as discussed later in Section V.

Apparently, the key to stopping the whole process and enhancing the large-signal stability of BLH is to limit the discharging current I_{Cmax} described in (14), which is exponential to the product of Kt_{dis}. Decreasing K and A_{AMP} will help, but a reduced K could introduce instabilities in the small signals, and smaller A_{AMP} should be a compromise with the high-rate performance of BLH, already shown in (5). Thus, we introduced the new circuit structures to improve the large-signal stability of the shaper-BLH loop in next section.

III. Improved design of the BLH for large-signal stability

To limit the discharging current, another current source M0 is connected to the drain node of the LP source follower (Fig. 8), as discussed in [4]. The bias current of M0 is designed as twice that of the bias current of $M2$, so the current, $I_d(t)$, should be limited up to $2I_{LP}$. $V_E(t)$ is about 20 mV in the static condition. When $V_{NL}(t)$ decreases, $V_E(t)$ will go up to $V_{LP}(t)$, bringing the source-drain voltage of $M1$ almost down to 0, and reducing the $M1$ current $I_d(t)$ to $2I_{LP}$. However, since there are the parasitic drain-bulk capacitors, C_{d0} and C_{d1}, the transient discharging current, $I_{d0}(t)+I_{d1}(t)$, still can be much larger than $2I_{LP}$, so generating a large-value I_{Cmax} to discharge C_2.

Assuming $V_{LP}(t)$ constantly is equal to V_{LP0}, using (11) we can derive an approximate I_{cmax1} and its time t_{max} using (17) and (18) ($C_E = C_{d0} + C_{d1}$).

$$V_E(t_{\max})=\frac{1}{C_E}\int_0^{t_{\max}} I_C(\tau)d\tau+V_{E0}=V_{LP0} \quad (17)$$

$$I_{c\ \max\ 1}=I_C(t_{\max}) \approx C_E(V_{LP0}-V_{E0})(K/nV_T) \quad (18)$$

When $t_{max} < t_{dis}$, the maximum discharging current $I_c(t)$ can be limited to (18), and the amplitude of the negative voltage pulse in (14) can be replaced by the following:

$$V_{fp} \approx \frac{H(0)g_0}{C_2K/nV_T}I_{c\ \max\ 1}=H(0)g_0\frac{C_E}{C_2}(V_{LP0}-V_{E0}) \quad (19)$$

Equation (19) provides an upper limit to the amplitude of the negative pulses, which is independent of the NL-stage current and discharging time, t_{dis}, but is sensitive to the parasitic parameters. In our design, we selected the channel width W of both *M1* and *M0* as the minimum value (0.48 μm) in our CMOS process, leading to a minimum C_E = 2.7 fF, which is limited by the fabrication process. Meanwhile V_{LP0} should be sufficiently high to allow all MOSFETs to work at their proper static condition. For a V_{LP0} of around 0.8 V, I_{cmax1} is about 5 nA, still much larger than the DC bias current of the LP stage. A source-bulk-connected PMOS *M1* can be used to decrease the discharging current (Fig. 9(a)); in this case, the current, $I_{d1}(t)$, will flow only in the opposite direction to $I_d(t)$, so reducing the equivalent capacitor at node E to $C_E \sim C_{d0}$. However, such a source-bulk connection will affect the threshold voltage *M1*, so requiring the redesign of the static voltage at each node. Extra area is also needed to implement a separate N-well in the layout; thus, we did not adopt this method in our current ASIC.

To minimize the voltage change in (19), we introduced a float voltage to the source node of *M0* to elevate the static value of V_{E0}, so enhancing the large-signal stability of the BLH (Fig. 9(b)). V_{float} was implemented by a MOSFET voltage-divider in our design, and V_{E0} was optimized ensuring that *M1* operates in the saturation region. For a small-signal input, the source of *M0* is connected equivalently to the ground via a small resistor, so maintaining all the conditions in (3)–(5). The proposed *W/L* ratios are (0.48 μm/2.04 μm) for both M_{b0} and M_{b1}, and (0.48 μm/19.8 μm) for *M0*.

IV. Circuit Simulation with SPICE

We used the Silvaco® SmartSpice simulator to analyze the transient response of our BLH. First, we simulated the negative pulses triggered by a single noise-pulse at the baseline, and then compared them with our theoretical analyses in Sections II and III. The influence of varying I_{NL} and A_{AMP} are shown. Then, we invoked transient noise simulation to study the transient response to noise sources in both the detectors and the electronics.

A. Transient response of BLH to single noise-pulses at the baseline

At the input of the shaper, we injected a 5-fC current pulse to generate a noise pulse of ~20 mV amplitude at the baseline, i.e., twice the measured root-mean-square (rms) value on the

baseline, and equal to an ENC of 300 e^{-}. Figure 10 shows the simulated waveforms of baseline voltage $V_{out}(t)$, the NL stage output voltage $V_{NL}(t)$, the LP capacitor's discharging current $I_C(t)$, and the BLH feedback current, $I_f(t)$. We found that the input signal triggered an exponentially increasing, and slowly decreasing feedback current, $I_f(t)$, so generating a triangular-shaped negative pulse on the baseline, immediately after the output pulse. This finding agrees with the analysis depicted in Fig. 6. By measuring the ratio between t_{dis} and t_f, we derived a simple multiplication factor λ of 1.6 as the correction to the V_{fp} in (14). In general, to assure safety in a new design, we could estimate the falling time of $I_C(t)$ as being the same as its rising time, thus an estimate of λ = 2 was chosen for consideration in our design.

To analyze the pulse height influenced by A_{AMP} and K, we employed A_{AMP} values from 10 to 100, and I_{NL} from 10 nA to 100 nA. We noted that the range we chose for I_{NL} guarantees that ω_{NL} is within 10 $A_{loop}\,\omega_{LP} \sim 1/\tau_{SH}$, so maintaining the properties summarized in Section II.A. Fig.11 compares the calculations and the SPICE simulations, both of which indicate an exponential increase with I_{NL}. Their variation, according to A_{AMP}, is almost linear, a conclusion that also can be derived by the approximate linear relationship shown in Fig. 7 (left).

We also simulated the situation where the current-control structures shown in Figs. 8 and 9 were used; the results are shown in Fig. 12. When no source-shifting structure was used, the parasitic capacitor C_E was ~2.7 fF, and V_{LP0}- V_{E0} is 0.8 V. The source-shifting structure we used lowered V_{LP0}- V_{E0} to 0.3 V. The limit of the height of the feedback pulse, V_{fp}, was found both by calculation and simulation, indicating our validation of this approach to enhancing the stability in the large-signal response.

B. Transient Noise Simulations

To analyze the response of the time-domain of the circuit to the noise, we analyzed the transient noise using the SmartSpice simulator. The software uses Monte-Carlo techniques to generate random numbers with a Gaussian distribution based on intensity of the noise each device should produce [14]. Thus, noise can be taken into account in simulating a transient response. Fig. 13 shows the waveforms of such transient-noise simulations. When no negative pulses occur, the noise level at $Vout(t)$ is 10 mV (rms), similar to the test results.

Since the discharging current in the LP stage is the key to the whole process described in section III, its standard deviation value in the simulation results can indicate the large-signal stability. We simulated the transient response of shaper and the BLH over 5 minutes in one run (Fig. 13), and employed 10 samples with difference initial seed for the Monte Carlo approach. Table II summarizes the results. Both the decrease in A_{AMP} and I_{NL} can reduce the discharging process, as detailed before. It also was found that the current mirror and source voltage shift structure can contribute to the large-signal stability by limiting the peaking value of the discharging current (Fig. 14). It is found that by adopting both the current mirror- and source-voltage-shift-structures, A_{AMP} can be left as 100 while maintaining a comparable stability performance as A_{AMP} = 40, which can reduce the variation of the baseline caused both by the leakage current and counting rate by a factor of 2.5, as revealed in (4) and (5). This is validated in our newly designed ASIC. Since such

instability from the large-signal process cannot just be derived from simulations of an AC noise analysis or small-signal stability, the simulation of transient noise, combined with Monte Carlo calculations will be useful when designing a BLH to evaluate the outcome on the baseline of such randomly occurring negative pulses

V. Discussion

A. Effects from noise overlap

As detailed in Section IV.A, we found that the maximum V_{fp} caused by twice the noise level, V_P, is quite small compared with to the V_P itself; thus, for most cases we simulated, a large-signal stability of (15) should be obtained. However, in the simulating the transient noise, bigger variations than calculated still occurred occasionally in the baseline. We found that the overlap of noise pulses will cause t_{dis} to be larger than (16). Looking back at (11) and (14), we found that a variation of t_{dis} influences V_{fp} significantly since they have an exponential relationship.

As discussed, the entire process can be triggered only by a positive pulse on the baseline. There could be three timing relations between two noise-pulses; the results of their SPICE transient simulations results are shown in Fig. 15. When two pulses occur successively (as shown in Fig. 15(b)), the combination of two linear ones decreasing on $V_{NL}(t)$ will generate a single exponential $I_C(t)$ pulse with a duration of up to $2t_{dis}$, so resulting in a much larger negative pulse. When the two pulses are too close to each other (Fig. 15(a)), the discharge duration is shorter than $2t_{dis}$ and the overlap of pulses approximately generates a single pulse with a height of $2V_p$. According to Fig. 7, e^{Kt_{dis}/nV_T} increases approximately linearly with V_P, so finally only a negative value of $2V_{fp}$ can be found on the baseline. In the case wherein the later pulse occurs within the recovery time of the first pulse (Fig. 15 (c) and (d)), the current flowing through the LP-stage source follower is smaller than I_{LP}; thus, $I_C(t)$ triggered by the latter pulse is smaller, and the final variation of the baseline also is smaller than $2V_{fp}$.

As the noise pulses are distributed randomly over time with their intervals following an exponential distribution [15], we assumed that the possibility is small of more than two positive pulses occurring exactly one after another; thus the maximum discharging time of $2t_{dis}$ can be used to evaluate the stability of the BLH. Fig. 16 shows the ratio of V_{fp}/V_p changing with I_{NL} when A_{AMP}=100, so providing a large big increase in V_{fp} when the discharging duration is from t_{dis} to $2t_{dis}$. A more precise prediction of the random discharging process can be obtained by using more detailed time-domain noise models.

B. Design considerations for both small-signal- and large-signal-stability

The properties and stability requirement of BLH circuits are summarized in (22) where t_{dis} is derived using (16), and twice the value is used for analyzing stability. λ is the multiplication factor we described in Section IV.A, and is estimated as 2 for safety. For a specific shaping system, $H(0)$, τ_{SH} (related to τ_P), and the noise level, V_P, are fixed and there are four parameters to be optimized: I_{NL}/C_1, I_{LP}/C_2, A_{AMP}, g_0. Thus, we generally can obtain the design flow of a BLH.

$$\begin{cases} dV_{\text{out}}/dI_{\text{leak}}=A_{cl}(0)=1/A_{AMP}g_0 \\ \Delta V_{\text{out}}\Big|_{R_t} = -2V_{dd}\tau_P R_t K_a/A_{AMP} \\ H(0)A_{AMP}g_0(I_{LP}/C_2)<<I_{NL}/C_1<\sim nV_T/\tau_{SH} \\ \lambda\frac{H(0)g_0}{I_{NL}/C_1nV_T}\left(e^{2t_{\text{dis}}I_{NL}/C_1nV_T}-1\right)\frac{I_{LP}}{C_2}<V_P \\ \text{or } H(0)g_0\frac{C_E}{C_2}(V_{LP0}-V_{E0})<V_P \end{cases} \quad (20)$$

The first two properties are required by the system, so both A_{AMP} and g_0 have their lower limits. For the third equation on small-signal stability, we can introduce a factor F which should be larger than 10 and maximized:

$$F \cdot H(0)A_{AMP}g_0(I_{LP}/C_2)=I_{NL}/C_1 \quad (21)$$

In a structure without a limitation in current, we can substitute (21) into the fourth equation in (20) and get the following one:

$$e^{2t_{\text{dis}}I_{NL}/C_1nV_T}-1<V_P A_{AMP}FnV_T/\lambda \quad (22)$$

From Fig. 7, the left term in (22) varies approximately linearly with A_{AMP}, and exponentially with I_{NL}/C_1; therefore I_{NL}/C_1 should be minimized, and F should be maximized to ensure that condition (22) is met.

After that, all the optimizations of A_{AMP}, g_0, I_{NL}/C_1, and F will make the I_{LP}/C_2 an extremely small value. The main challenge lies in implementing the large capacitor C_2 on the chip, especially for high-density multichannel readout. Some methods were developed to implement large equivalent capacitors by using active feedback [16]. However, extra circuits and power consumption are costly. In this case, however, the current limiting structure is of much help, which frees the large-signal's stability free from the NL stage and A_{AMP}. However, we noted that both the parasitic capacitor C_E, and bias voltage V_{LP0}- V_{E0} should be minimized, and they all have limitations.

VI. Conclusions

In this paper, we used large-signal analysis to explain the instability in BLH circuits, and then generated the design requirements for enhancing the large-signal stability of the circuit. Besides the fact that an extremely low frequency is required at the low-pass stage to ensure the small-signal stability, our analysis showed that both the gain of the error amplifier, and the slew rate of non-linear stage are critical to the stability of the circuit, and their values should be selected based on the trade-off between the stability and performance of the BLH. We also analyzed the case where extra current control is used in a low-pass stage, and we implemented the source shifting circuit structure in our newly designed ASIC, which is able to suppress the fluctuation, whilst maintaining the good performance of the BLH.

SPICE circuit simulations were carried out in our analysis to verify our conclusions at each step. The transit noise simulation provided by SPICE simulators is especially useful in the

stability and noise analysis of the BLH, and also provides guidance for the designing the circuit even though an improved time-domain noise model is in need to estimate the fluctuation amplitude more accurately, a problem that will be resolved in our future work.

Acknowledgments

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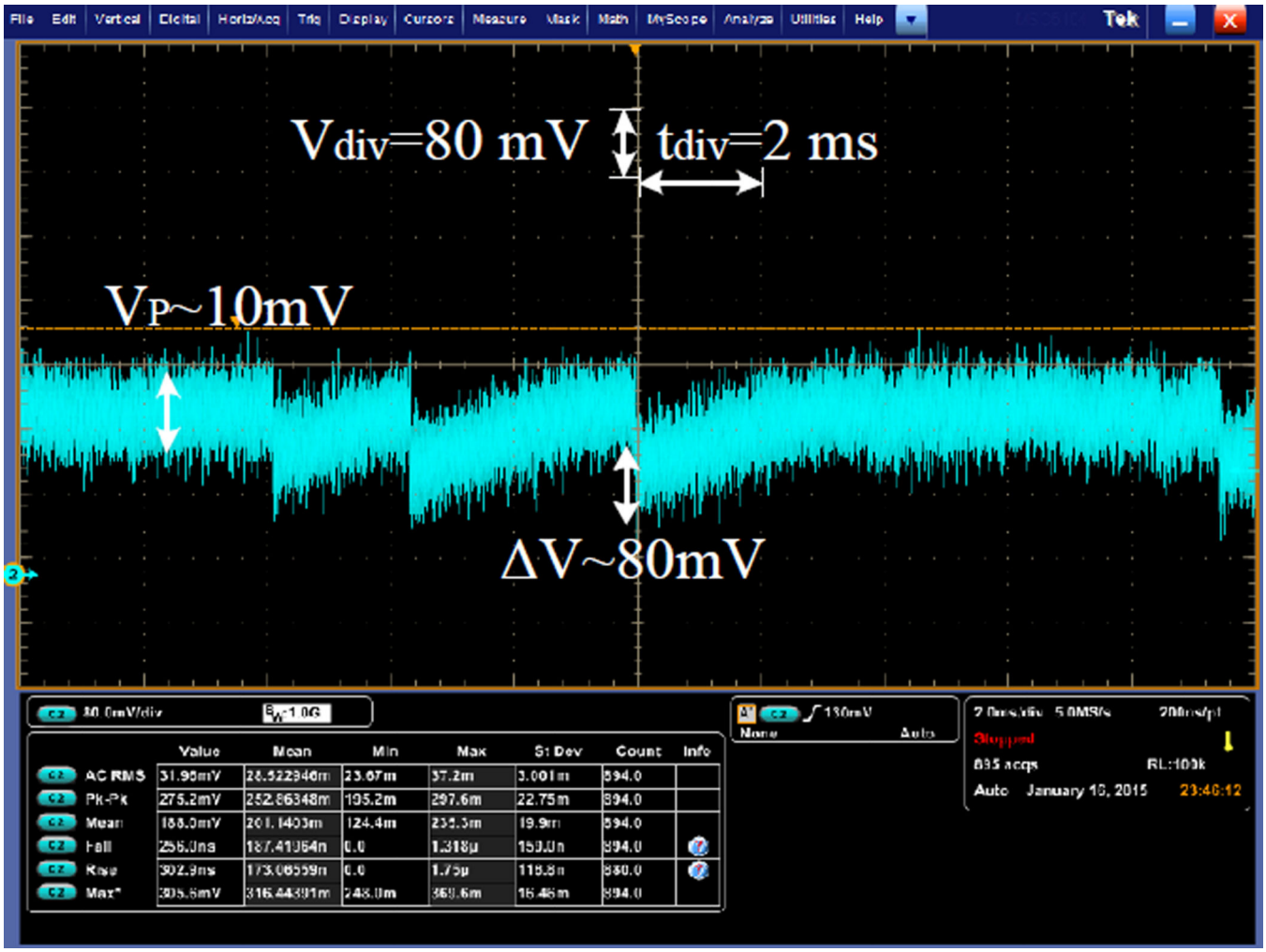

Fig. 1.

Self-triggered pulses on the baseline measured with an oscilloscope. V_P~10 mV is the noise level (root-mean-square (rms) value) at the baseline without the self-triggered pulses.

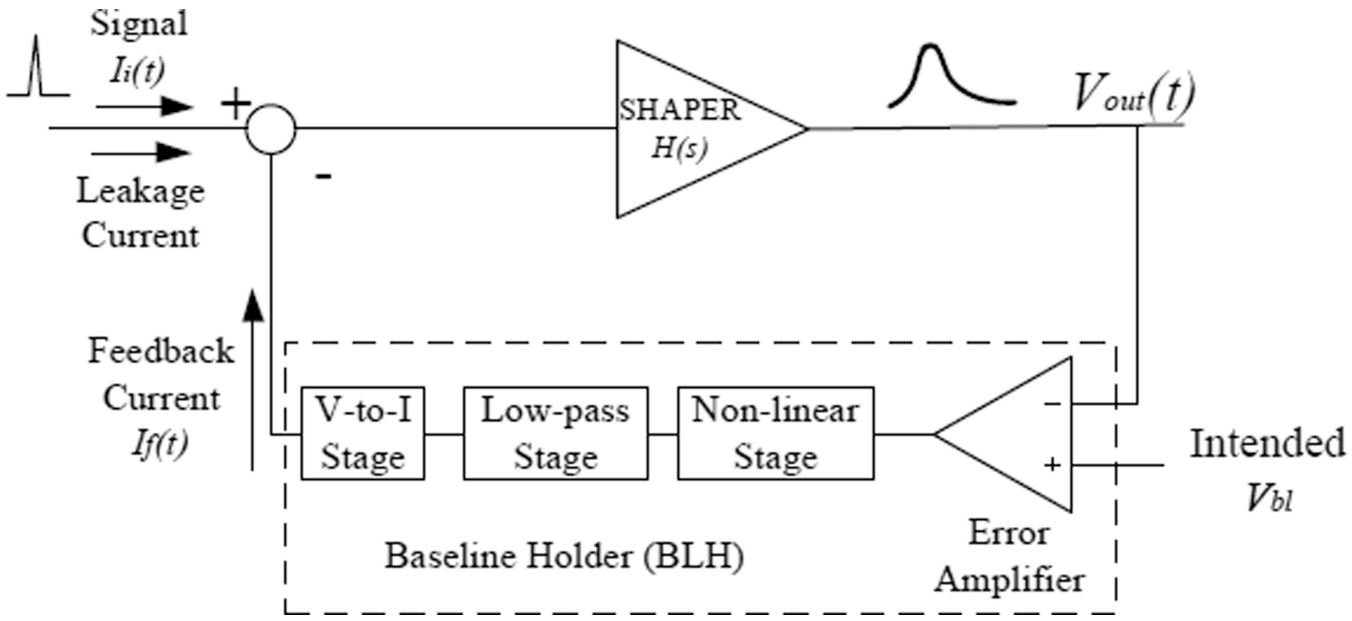

Fig. 2.
Block diagram of the shaping stage with a baseline holder (BLH).

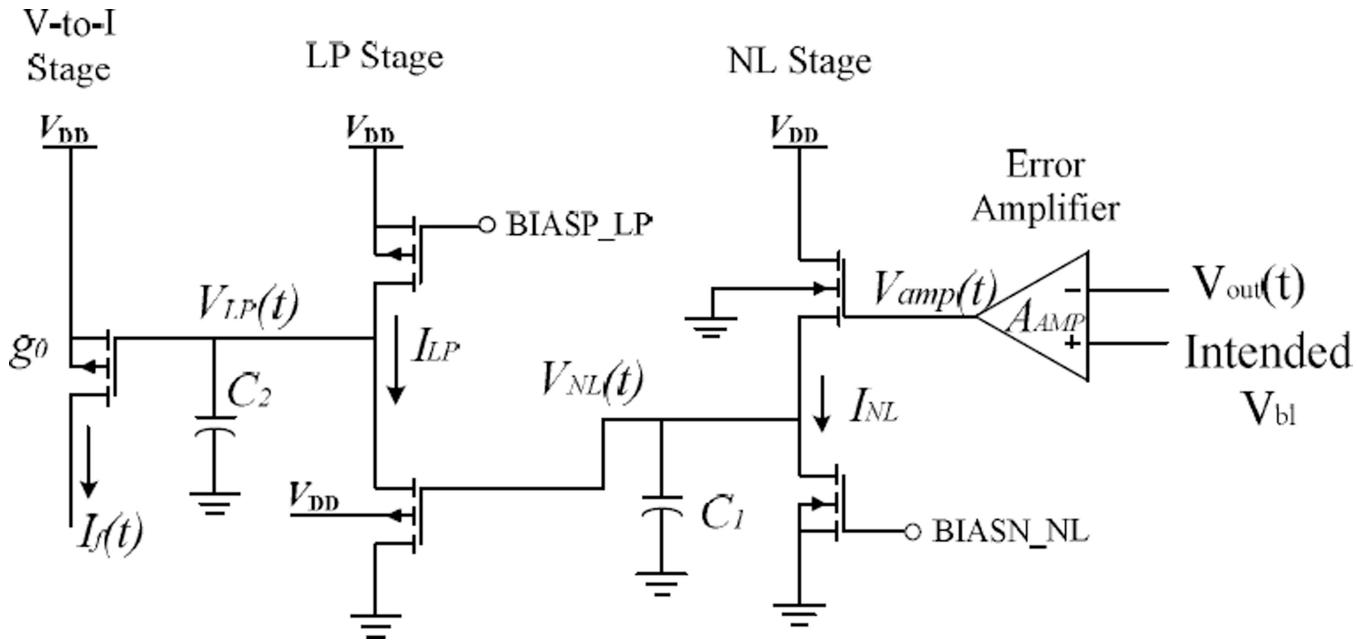

Fig. 3.
Detailed structure of a BLH in [4].

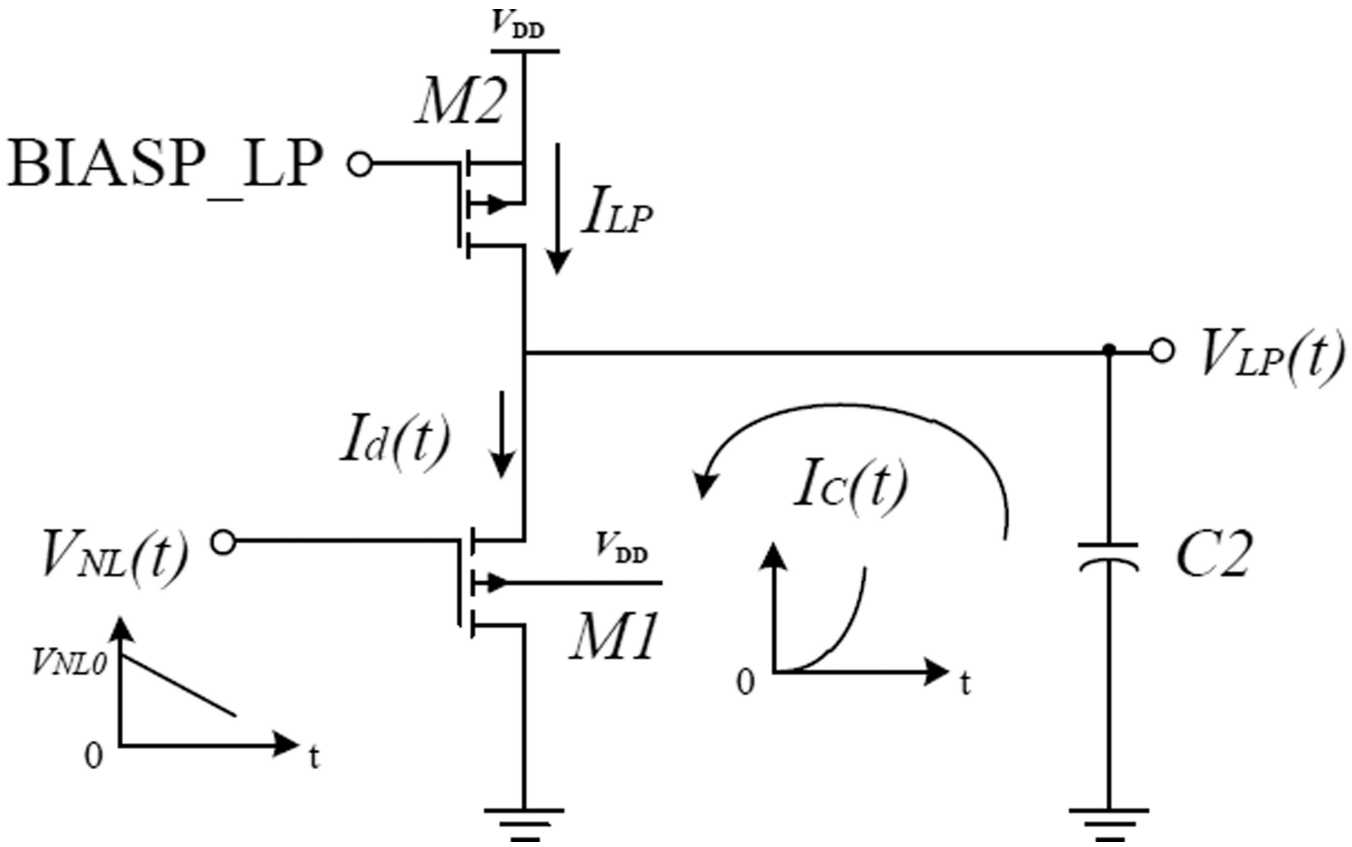

Fig. 4.

Discharging process of the LP stage. Figure should follow its description in the text, so move it below the following paragraph.

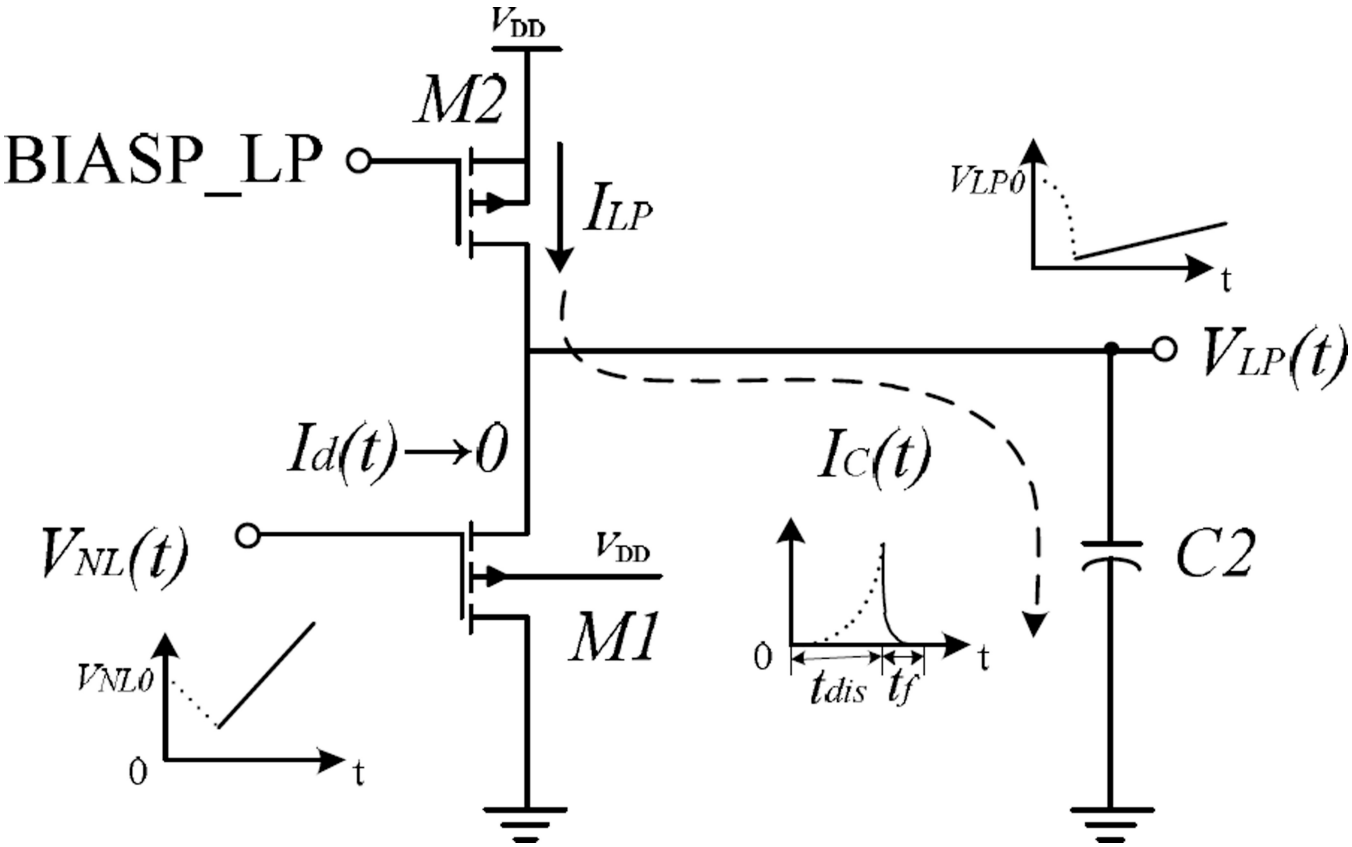

Fig. 5.
Charging process of LP stage.

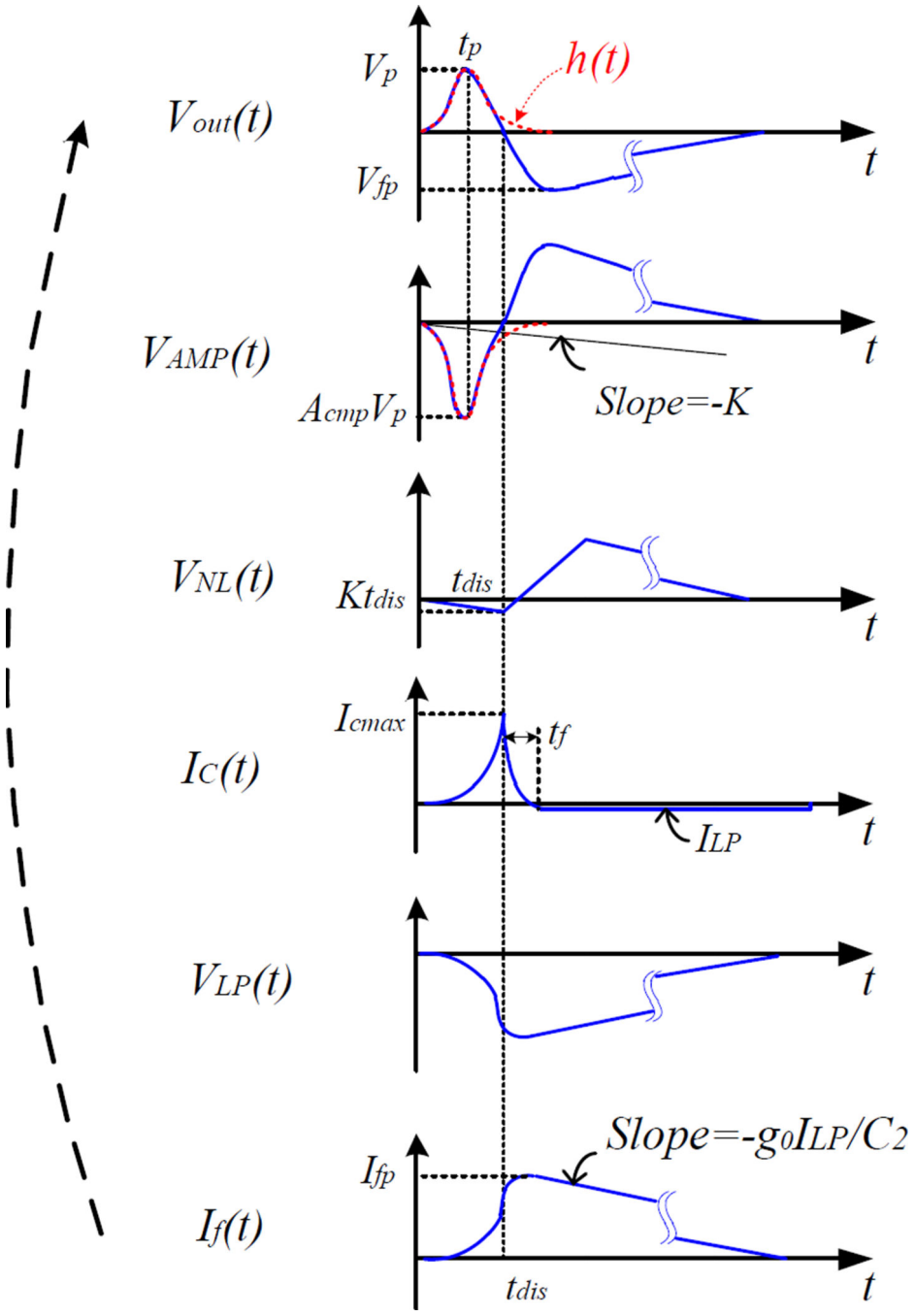

Fig. 6.

Time-domain waveforms of large-signal analysis of the LP stage. Static values are ignored. The red dashed waveform in $V_{out}(t)$ indicates the output pulse $h(t)$ from the shaper without the influence of feedback from the BLH.

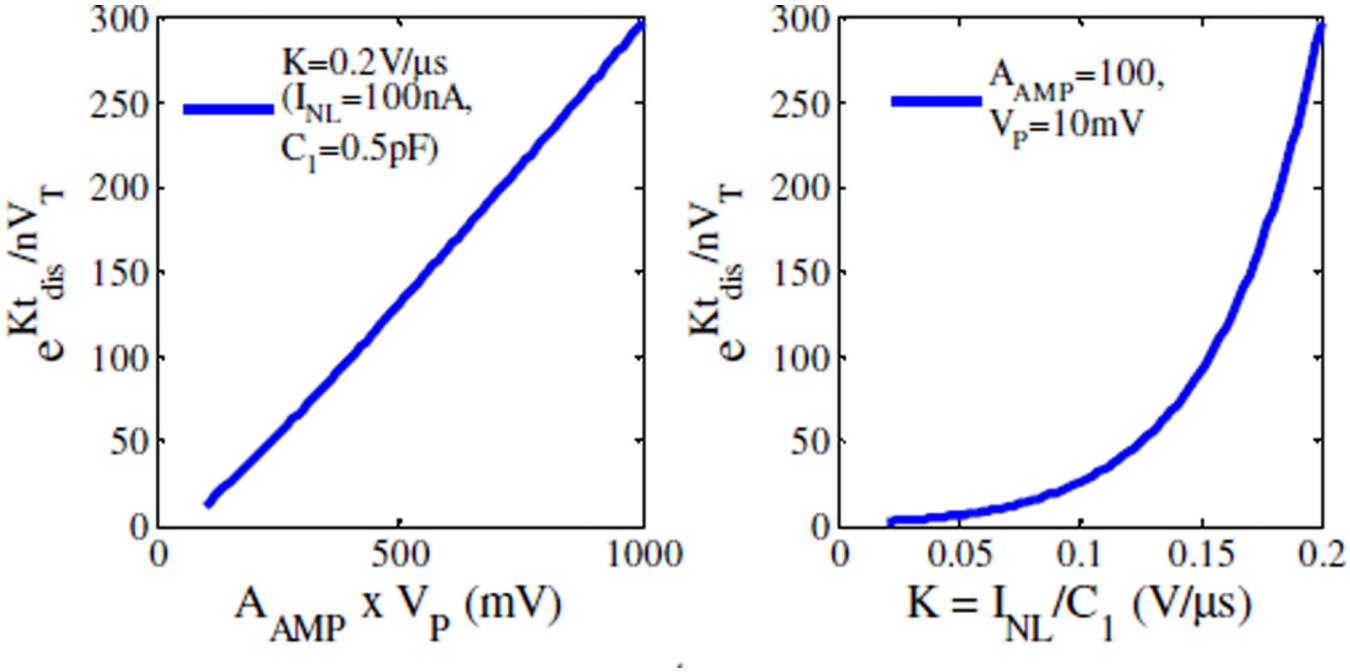

Fig. 7.

Numerical solution of e^{Kt_{dis}/nV_T} from (16). For the whole channel of our tested ASIC, V_p=10 mV as specified in Table I.

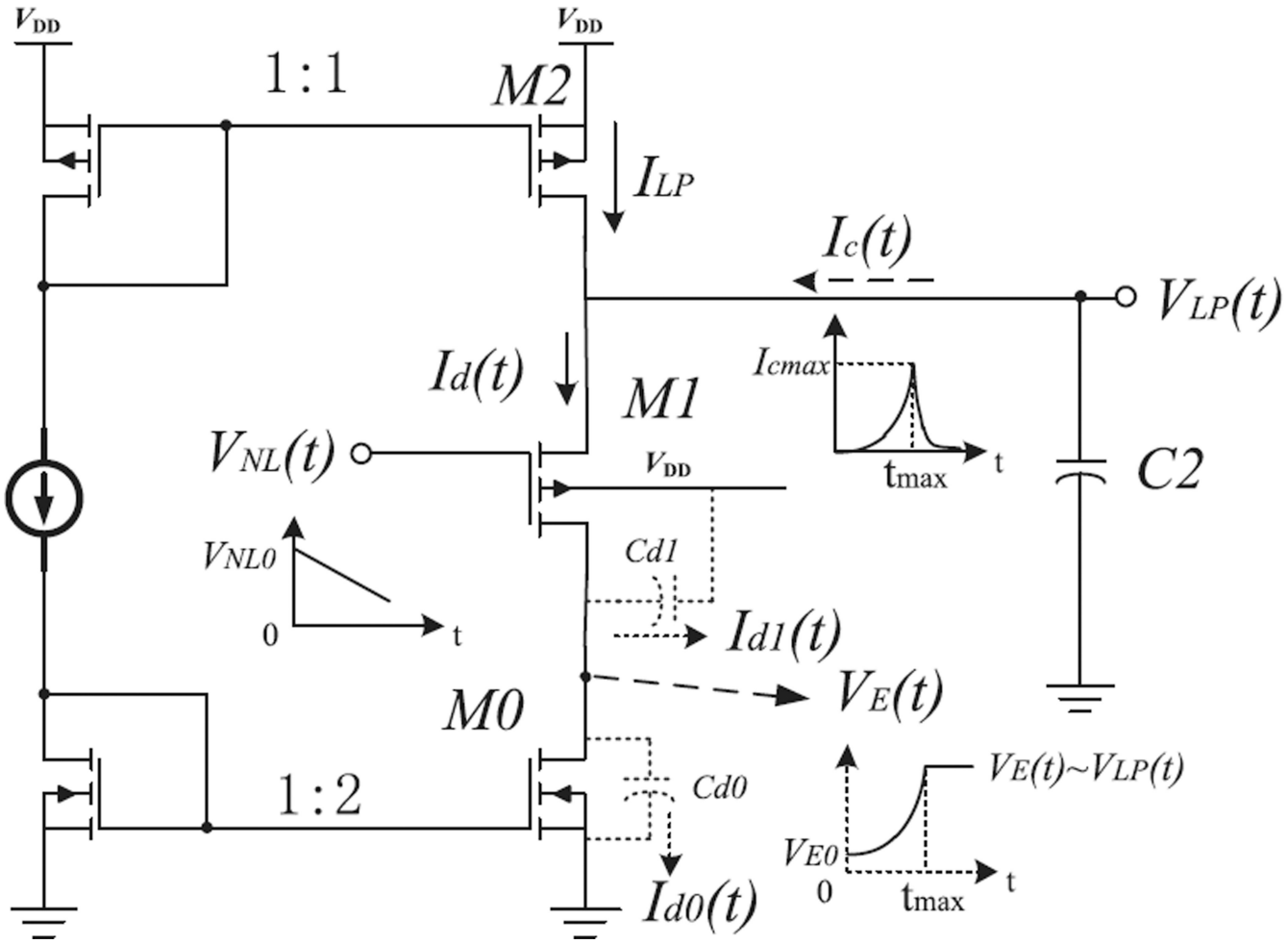

Fig. 8.
The transient process in the LP stage with current limitation used in [4].

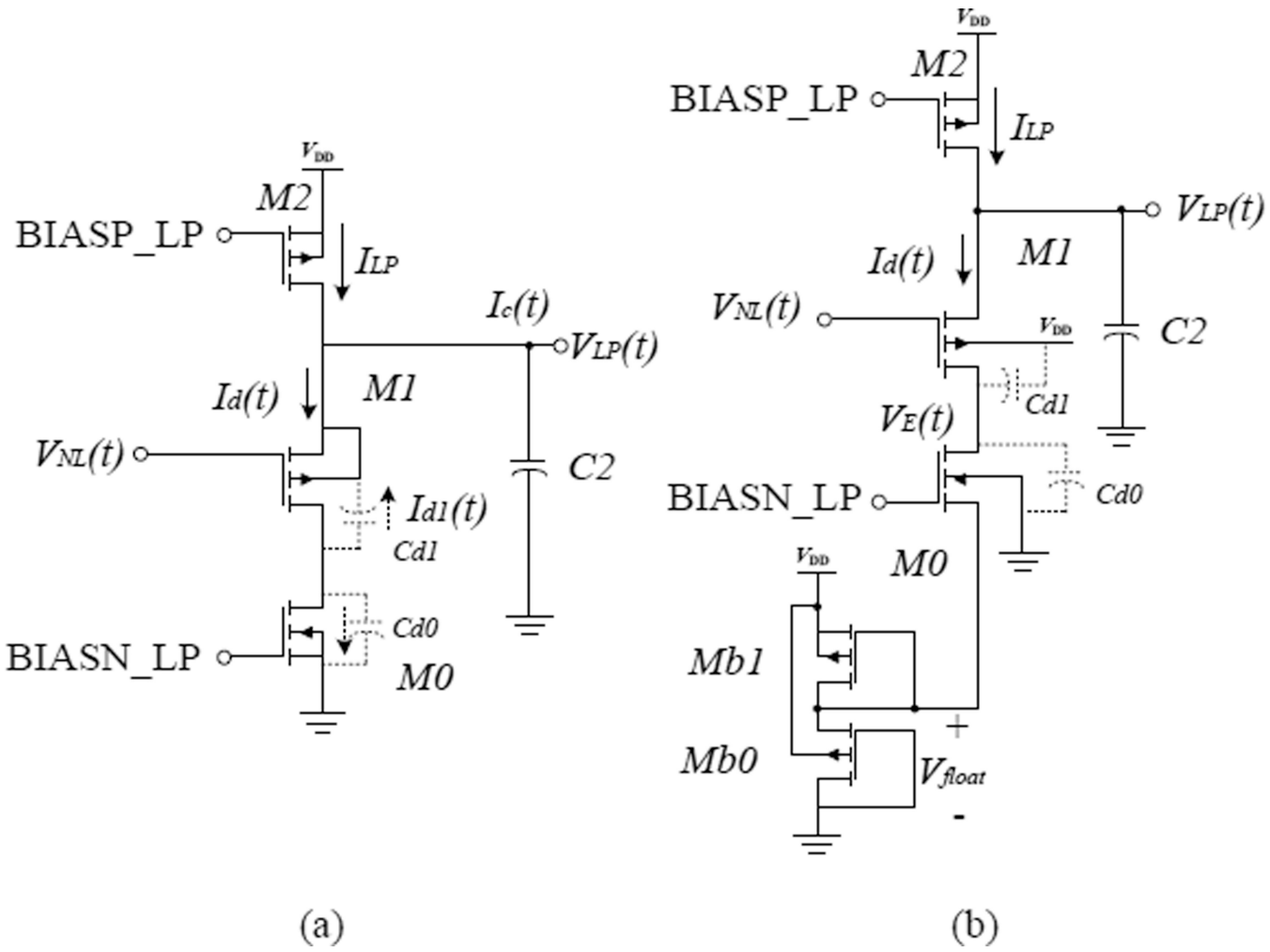

Fig. 9.
Improved structures to limit the current in the LP stage.

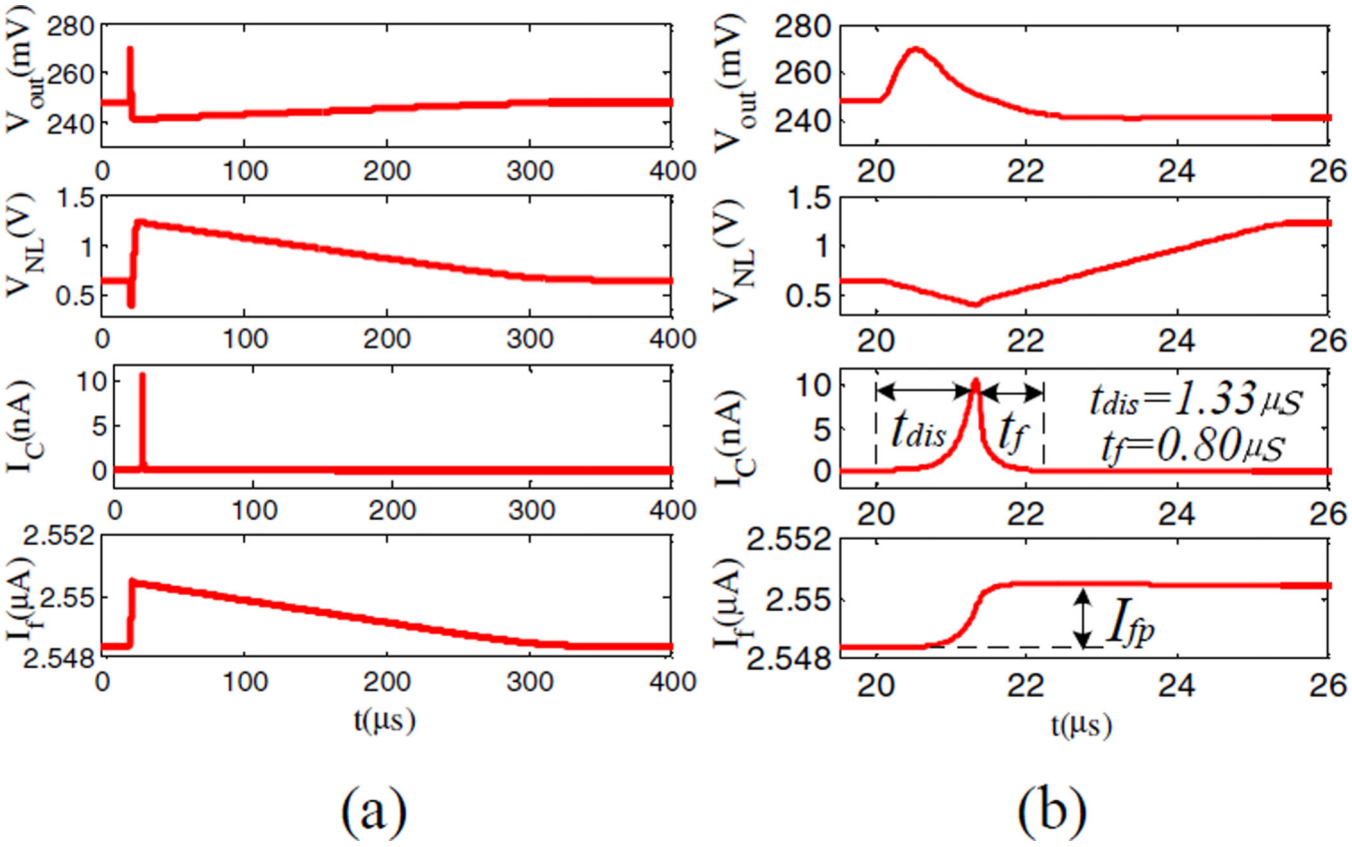

Fig. 10.

Results of a transient simulation when I_{NL}=100 nA and A_{AMP} = 100. A current pulse with a total charge of 5 fC is injected to the input at 20 μs. (a) The total response. (b) A zoom of the waveforms around 20–25 μs. λ can be derived as 1.6 from the ratio of $(t_{dis}+t_f)/t_{dis}$

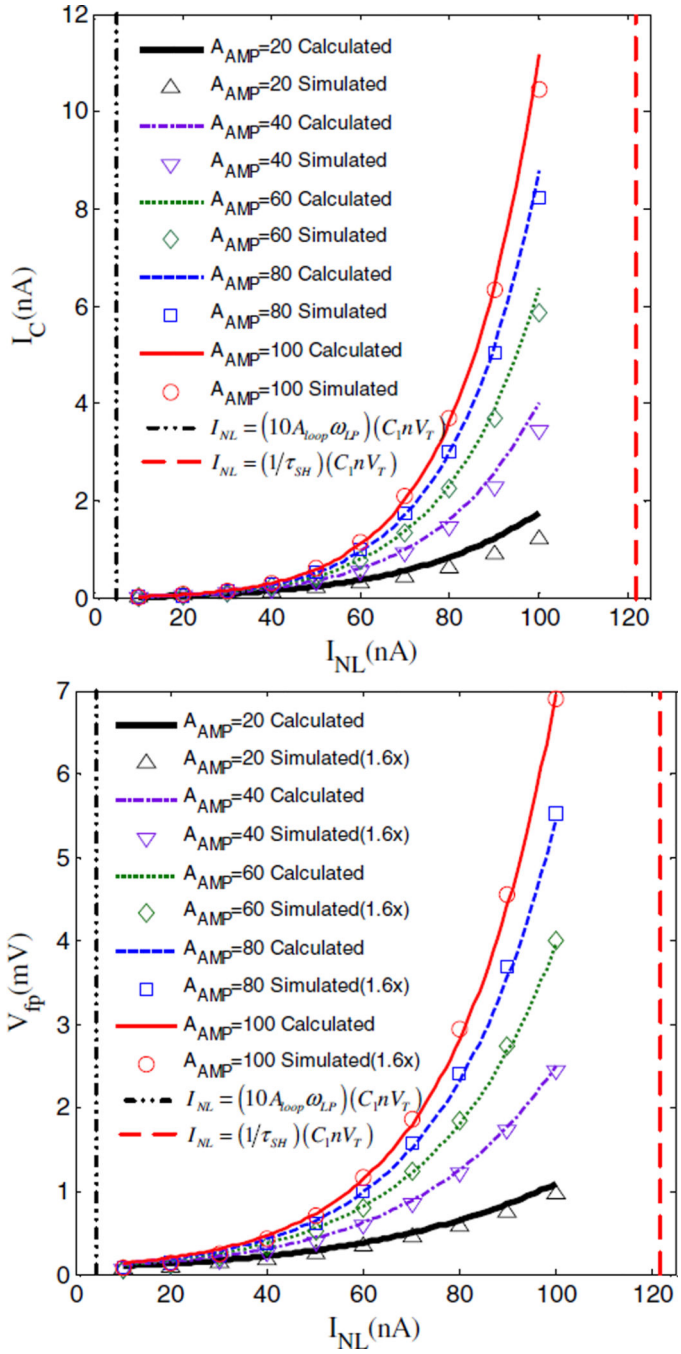

Fig. 11.

Maximum I_C and V_{fp} variations with I_{NL} and A_{AMP}. The original variation at $V_{out}(t)$ caused by the injected current pulses is ~20 mV. The calculated V_{fp} is multiplied by a shape-correction factor λ of 1.6. The vertical dashed lines indicate the required range of I_{NL} for BLH properties from the small-signal analyses, which range from $10A_{loop}\omega_{LP}C_1nV_T$ to C_1nV_T/τ_{SH}.

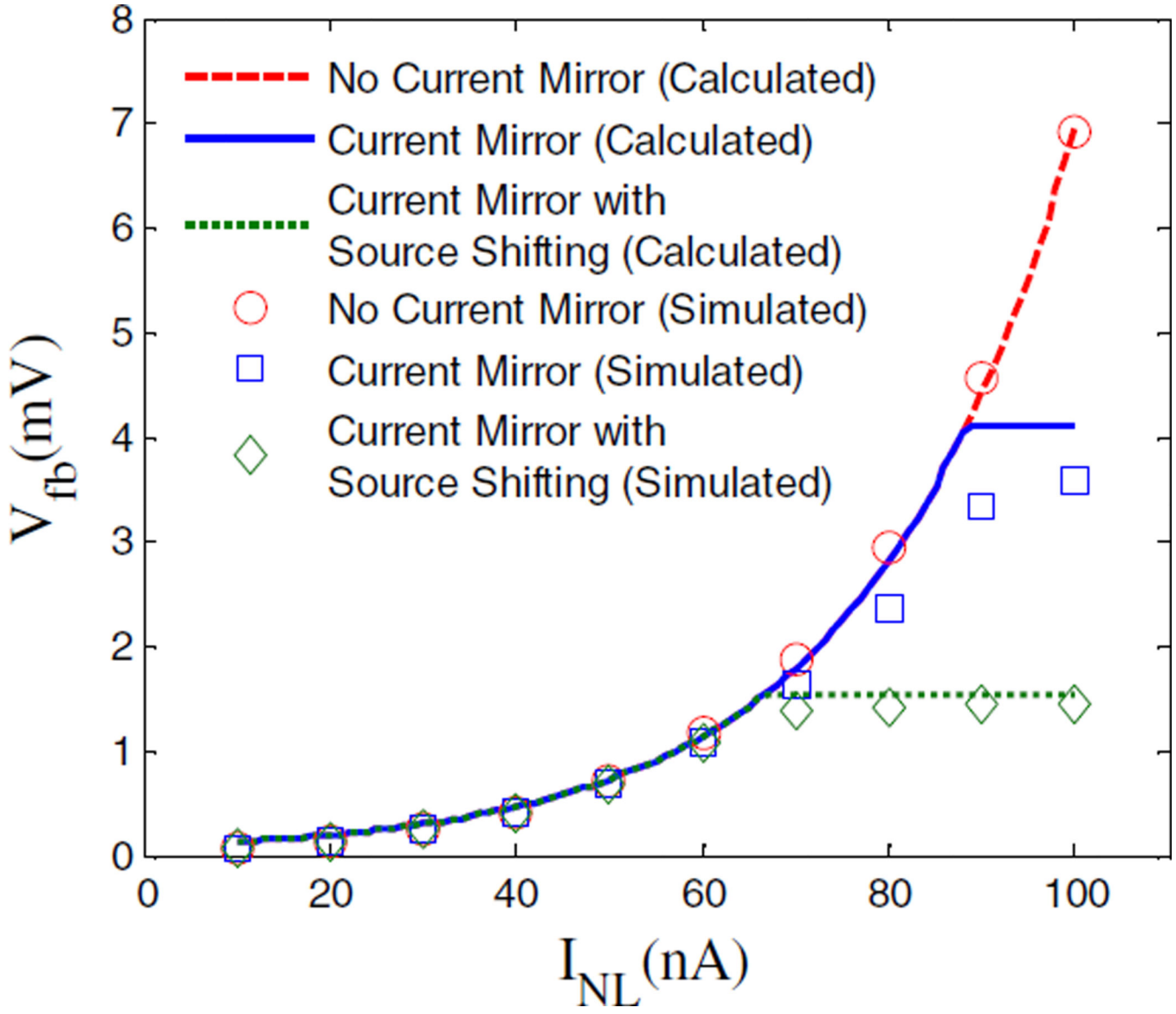

Fig. 12.
Influence of current control structures on V_{fp} when A_{AMP}=100

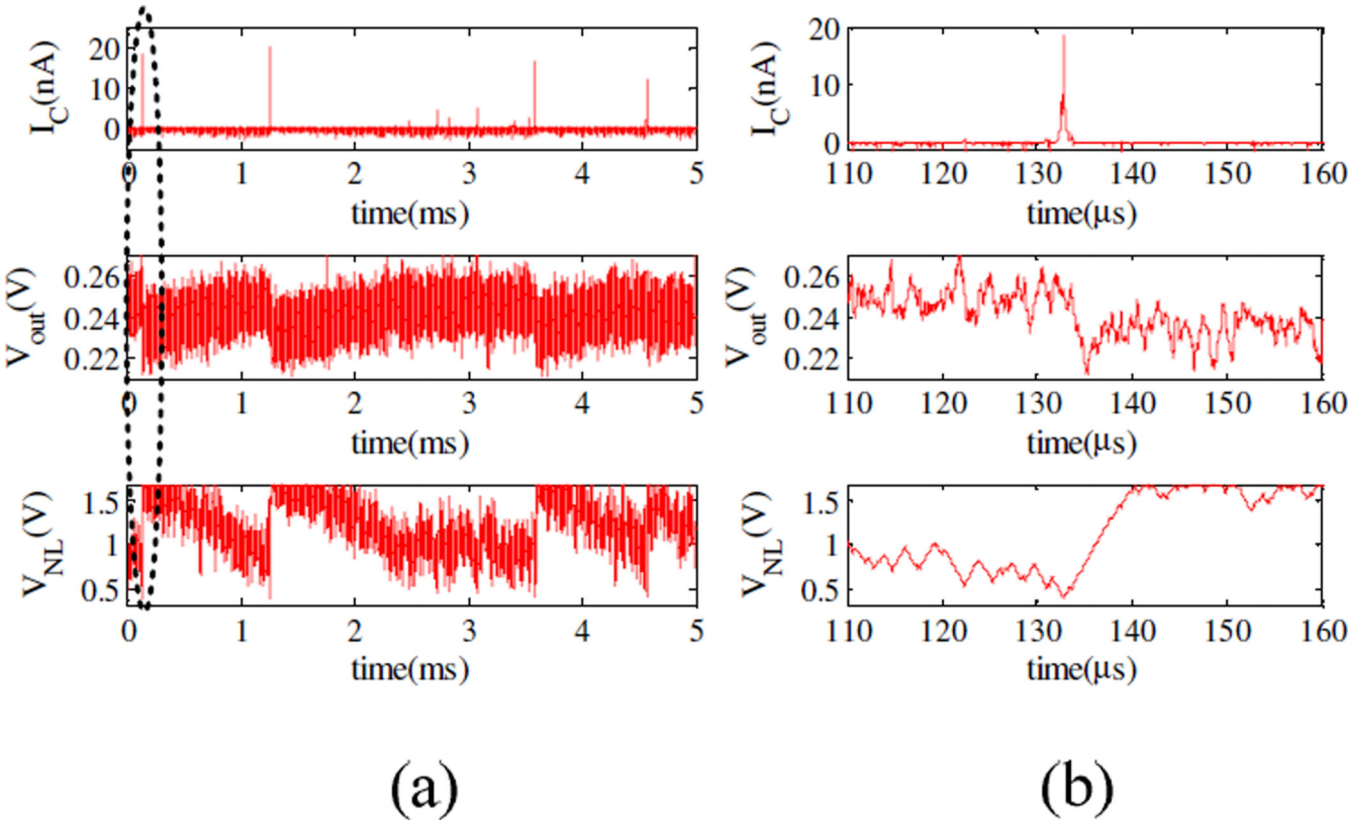

Fig. 13.

(a) Simulation results using transient noise analysis. A_{AMP}=100 and I_{NL}=100 nA. (b) The zoomed-in views of regions marked with the dashed line in (a).

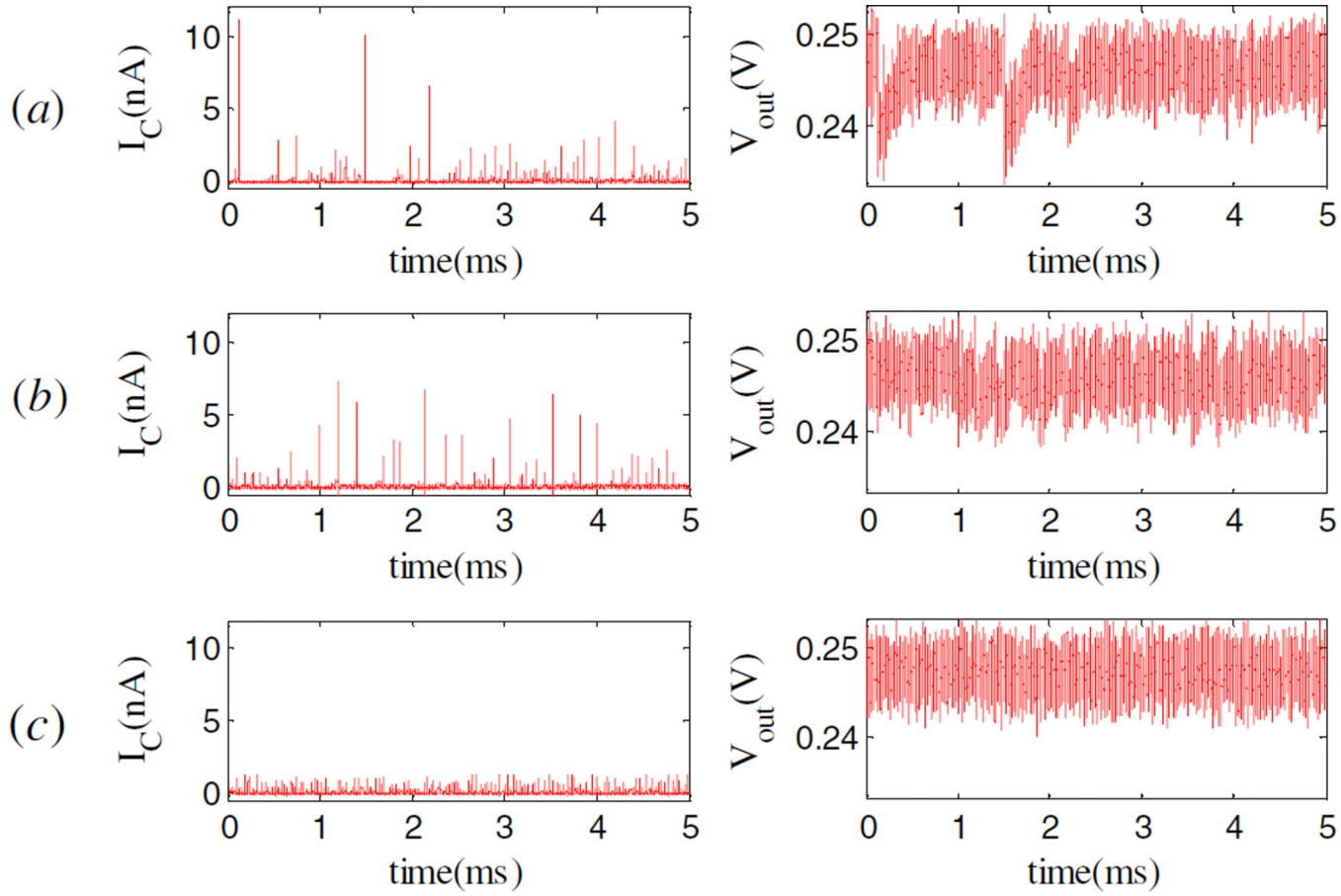

Fig. 14.

Simulation of transient noise shows the stability of improved BLH circuits. A_{AMP}=100 and I_{NL}=100 nA. (a) No current limitations; (b) Current mirror added (Fig. 8); and, (c) Current mirror and voltage shift added (Fig. 9(b)).

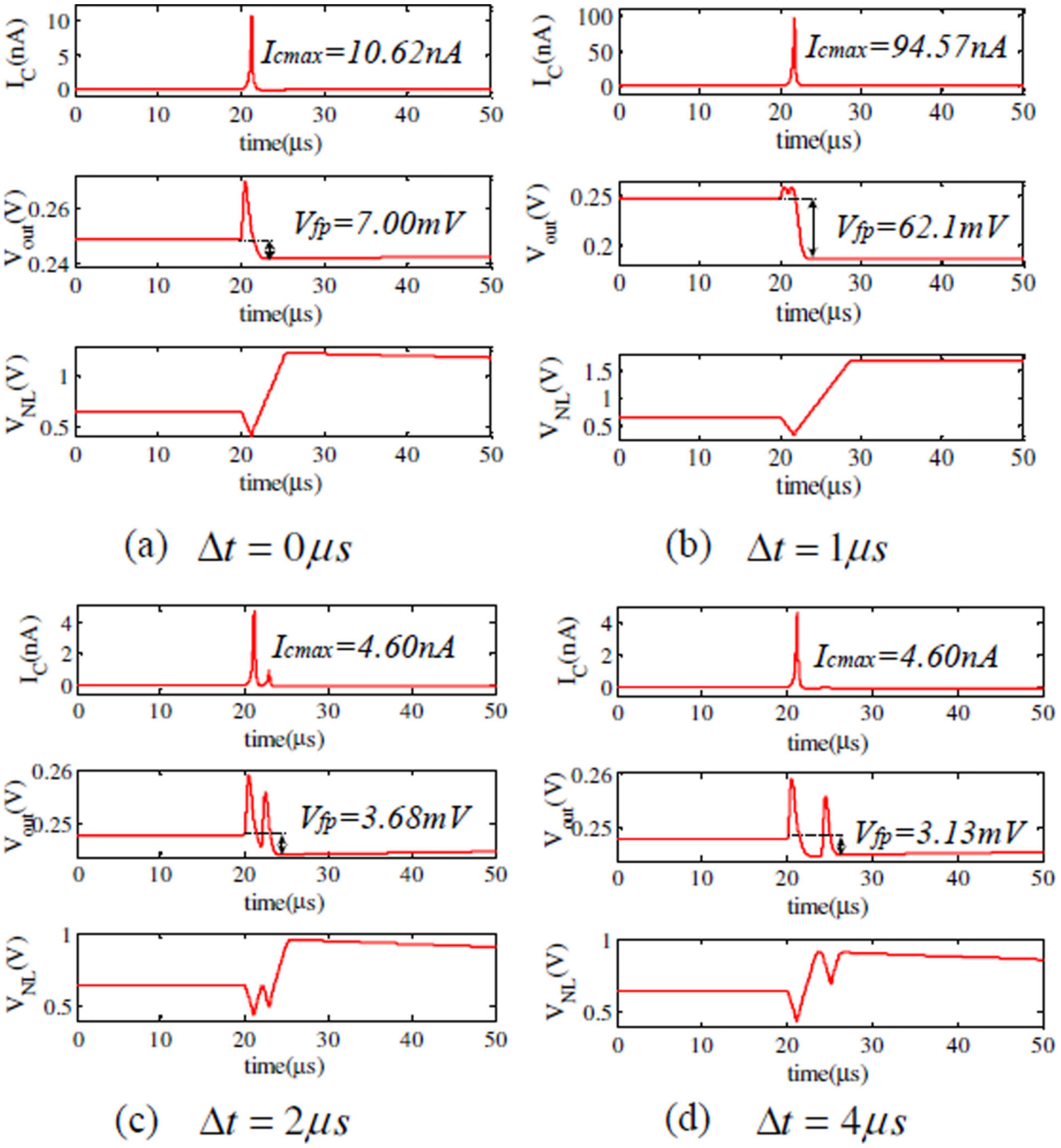

Fig. 15.

Overlap of two noise pulses and their transient responses. I_{NL}=100 nA, and A_{AMP}=100.Two noise pulses with height of 10 mV and interval of Δt are generated at the baseline. (a) Two pulses are too close to each other; (b) Two pulses occur successively; (c) and (d) Two pulses are separated, and the latter occurs during the recovery time of the first pulse.

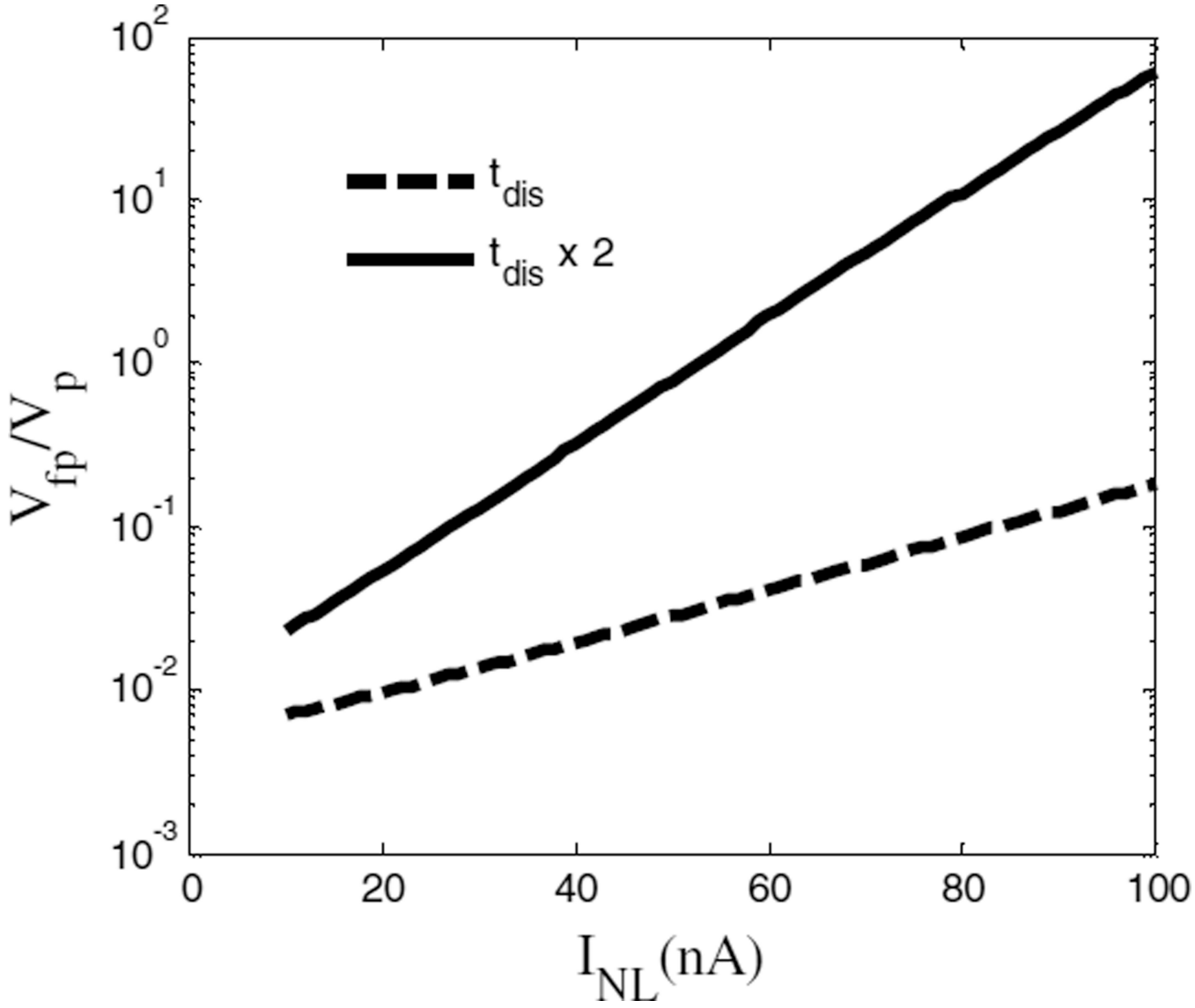

Fig. 16.

Feedback Ratio V_{fp}/V_p vs. I_{NL} with enlarging t_{dis}. Here, V_p=10 mV and A_{AMP}=100.

Table I

Parameters of tested ASIC for BLH analysis

Parameters in BLH	Designed Value
A_{AMP}	100
g_0	4.3 μS
n	1.59 (Derived from I_d- V_{gs} Curve by SPICE simulation)[a]
V_T	25.8 mV
I_{NL}	100 nA
C_1	0.5 pF
I_{LP}	16.62 pA
C_2	7.5 pF
$H(0)$ of Shaper	130 dB
τ_{SH}	167 ns
Gain from detector to Baseline Voltage	400 mV/fC
RMS noise value V_P on the baseline without the instability cause by BLH	10 mV (equivalent to ~150 e- ENC)

[a] I_d is the drain current and V_{gs} is the gate-source voltage of a MOSFET.

Table II

Simulation results using transient noise analysis in the time of 10 × 5 milliseconds. Other circuit parameters are the same as in Table I.

Circuit Conditions	Standard deviation of I_{Cmax} (pA)	Peak value of I_{Cmax} (nA)
I_{NL}=100 nA, A_{AMP}=100	385.38	156.51
I_{NL}=100 nA, A_{AMP}=80	281.18	47.76
I_{NL}=100 nA, A_{AMP}=60	228.65	23.49
I_{NL}=100 nA, A_{AMP}=40	101.8	7.92
I_{NL}=80 nA, A_{AMP}=60	182.68	19.35
I_{NL}=60 nA, A_{AMP}=60	130.79	14.13
I_{NL}=40 nA, A_{AMP}=60	86.51	9.91
I_{NL}=100 nA, A_{AMP}=100, current mirror added	137.95	8.85
I_{NL}=100 nA, A_{AMP}=100, current mirror and source voltage shift added	102.06	2.68