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Low Jitter Techniques for High-Speed Phase-Locked Loops

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Low Jitter Techniques for High-Speed Phase-Locked Loops

A dissertation submitted in partial satisfaction

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Doctor of Philosophy in Electrical and Computer Engineering

by

Yu Zhao

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ABSTRACT OF THE DISSERTATION

Low Jitter Techniques for High-Speed Phase-Locked Loops

by

Yu Zhao
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2022
Professor Behzad Razavi, Chair

The problem of clock generation with low jitter becomes much more challenging as wireline transceivers are designed for higher data rates, e.g., 224 Gb/s. This dissertation addresses the clock generation problem and proposes both integer-N and fractional-N phase-locked loop architectures that achieve low jitter with low power consumption.

This dissertation consists of two parts. We first introduce an integer-N PLL that incorporates two new techniques. A double-sampling architecture samples both the rising and falling edge of the reference clock, which improves the in-band phase noise by 3 dB. Also, a robust retiming technique is presented to reduce the phase noise of the frequency divider. Fabricated in 28 nm CMOS technology, the 19-GHz prototype achieves an rms jitter of 20.3 fs from 10 kHz to 100 MHz with a spur of -66 dBc, all at a power of 12 mW.

Next, we propose a 56-GHz fractional-N PLL targeting 224-Gb/s PAM4 transmitters. The PLL employs a novel current-mode FIR filter to avoid phase and frequency detectors (PFDs) and charge pumps and to suppress the DSM quantization noise with negligible noise folding. To provide a compact solution suited to multi-lane systems, the PLL also incorporates an inductorless divide-by-8 circuit that draws 3.1 mW. Fabricated in 28-nm CMOS technology, the PLL exhibits an rms

jitter of 110 fs, consumes 23 mW, and occupies an active area of 0.1 mm^2.

The dissertation of Yu Zhao is approved.

Chee Wei Wong

Danijela Cabric

Gregory J. Pottie

Behzad Razavi, Committee Chair

University of California, Los Angeles

2022

To my parents

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PUBLICATIONS

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CHAPTER 1

Introduction

1.1 Motivation

The demand for higher data rates in wireline systems have been steadily increasing with the dramatic rise of data transport over the Internet. It has been predicted that the data traffic grows by 25% per year, possibly reaching 20 zetabytes (20×10^{21} bytes) in 2025 [1]. Such a demand poses several challenges to the clock generation with low jitter in the wireline transmitter/receiver design.

On the transmitter part, PAM4 wireline transmitters operating at 224 Gb/s can employ a 56-GHz phase-locked loop (PLL) for multiplexing, as shown in Figure 1.1. Such an environment poses *three* constraints on the design. First, the PLL rms jitter must be no more than a few percent of the symbol period, 8.93 ps, dictating values around 100 fs_{rms}. Second, the PLL should preferably provide fractional-N operation so as to accommodate different crystal frequencies. Third, in a multi-lane system, it is desirable to avoid distributing a 56-GHz clock over long interconnects. Hence the need for a low-power, compact PLL that can be used within each lane.

PAM4 receivers can employ an analog-to-digital converter (ADC) to enable more complex and flexible digital signal processing (DSP) for equalization and symbol detection compared to analog receivers [2]. The ADC-based wireline receiver poses challenging requirements on the PLLs in terms of speed, power consumption, and jitter. Observed in both wireless and wireline systems, this trend arises primarily because of the need for higher data rates. For example, a 112-Gb/s PAM4 wireline receiver employing a 7-bit 56-GHz ADC incurs 3 dB of signal-to-noise ratio penalty at

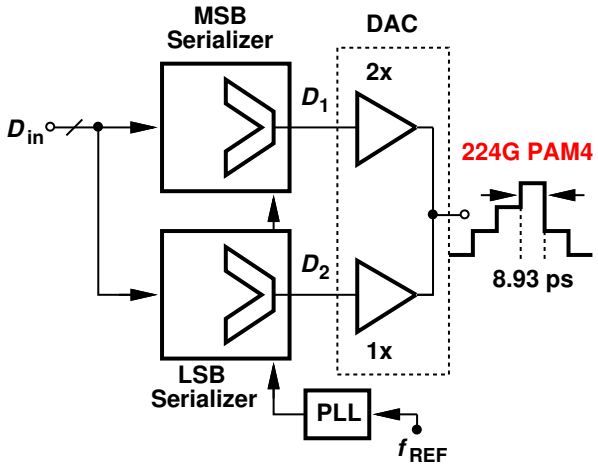


Figure 1.1: A 224G PAM4 wireline transmitter.

the Nyquist rate if the clock jitter exceeds 36 fs_{rms}, as plotted in Figure 1.2. While, in practice, the ADC is realized as a number of time-interleaved channels running at lower clock frequencies, this jitter bound still governs the generation of the clocks. Moreover, 12-bit ADCs designed for direct RF sampling [3] face similar jitter constraints as they approach a rate of 20 GHz.

Recent work has demonstrated jitter values below 100 fs_{rms} at frequencies ranging from 7 GHz to 31 GHz [4–14]. Some of these examples incorporate subsampling; extensive work on subsampling PLLs has been reported [15–19].

1.2 Thesis Organization

This dissertation consists of 5 chapters. Chapter 2 reviews the fundamentals of PLLs including bandwidth, noise transfer function and optimal PLL output jitter.

Chapter 3 presents a double-sampling integer-N PLL that samples both the rising and falling edge of the reference clock, which improves the in-band phase noise by 3 dB. A robust retiming technique is used to reduce the phase noise of the frequency divider.

Chapter 4 proposes a 56-GHz fractional-N PLL targeting 224-Gb/s PAM4 transmitters. The PLL employs a current-mode FIR filter to avoid phase and frequency detectors (PFDs) and charge

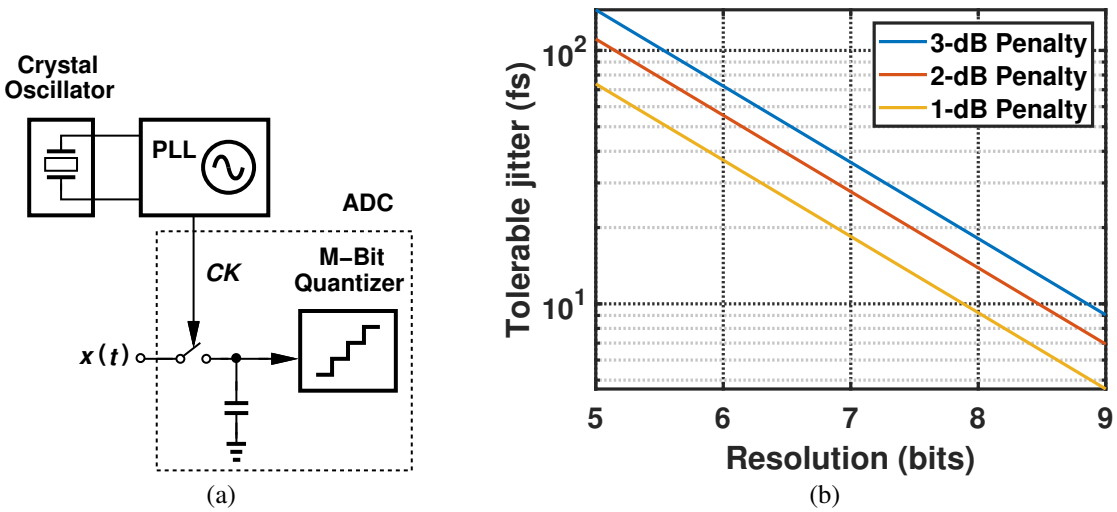


Figure 1.2: (a) An ADC clocked by a PLL and, (b) tolerable jitter for a 56-GHz ADC for SNR penalties of 1, 2, and 3 dB.

pumps and to suppress the DSM quantization noise with negligible noise folding. To provide a compact solution suited to multi-lane systems, the PLL also incorporates an inductorless divide-by-8 circuit that draws 3.1 mW.

Chapter 5 summarizes the dissertation.

CHAPTER 2

Background

This chapter provides the background for the integer-N PLL design and presents the optimization of the loop in terms of the reference and oscillator phase noise.

2.1 Basic Phase-Locked Loops

A phase-locked loop (PLL) is a feedback system that generates an output signal whose phase is regulated with respect to that of a reference signal. As in shown in Figure 2.1(a), a general PLL consists of a phase detector (PD), a loop filter, a voltage-controlled oscillator (VCO) and a feedback divider. The phase detector compares the phase of the divider output to that of the reference clock, f_{REF}, and converts the phase difference to a voltage or current signal. The PD output contains periodic pulses at the reference frequency, which disturbs the VCO control voltage [20]. To resolve this issue, a low-pass filter is placed between the PD and the VCO to suppress the high-frequency component of the PD output. A VCO is an oscillator whose oscillation frequency is controlled by its voltage input. A CMOS VCO can be implemented using a ring topology or an LC resonant circuit. The frequency divider takes the output of the VCO and generates an output signal of a frequency equal to f_{VCO}/N, where f_{VCO} is the VCO oscillation frequency and N is an integer. With the help of the divider, the PLL can generate an output signal whose frequency is N times of the reference frequency. This function is also known as "frequency multiplication".

2.2 PLL Jitter Optimization

As we seek jitter values in the range of a few tens of femtoseconds, the contribution of all noise sources becomes significant. We first quantify these contributions and then decide which ones can be avoided. Given our target jitter of 20 fs_{rms} and the numerous contributors in a typical design, we also explore the possibility of jitter values around a few femtoseconds for some of the functions.

2.2.1 Reference Phase Noise

The phase noise of crystal oscillators has become increasingly more critical as sub-100-fs jitter values have been targeted. We predict that PLL bandwidths must fall well below the $f_{REF}/10$ rule of thumb if both the reference and the voltage-controlled oscillator (VCO) contributions are to be minimized. We neglect the effect of flicker noise for now.

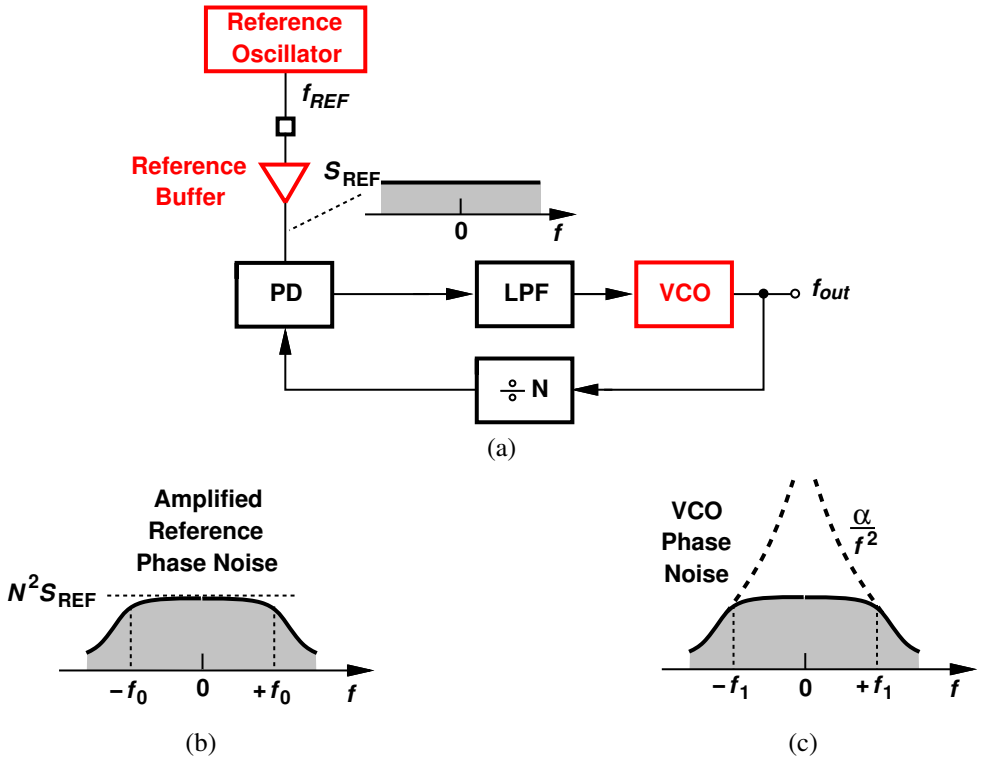


Figure 2.1: (a) Basic PLL architecture, (b) output profile due to reference phase noise, and (c) output profile due to VCO.

Consider the generic type-II PLL shown in Figure 2.1(a), noting that the reference phase noise, S_{REF}, experiences a low-pass response as it travels to the output. The loop bandwidth is likely to be far narrower than f_{REF}/10, and hence the damping factor, ζ, to be greater than 2, allowing us to assume that the zero and the first pole of the transfer function, $H(s)$, coincide. We thus have

$$H(s) \approx \frac{N}{1+\frac{s}{\omega_0}}, \tag{2.1}$$

where $\omega_0 = 2\pi f_0$ denotes the second pole frequency and the loop bandwidth. The reference phase noise emerges at the output as

$$S_{out1} = \frac{N^2 S_{REF}}{1+\frac{\omega^2}{\omega_0^2}}, \tag{2.2}$$

yielding a total area of $A_{REF} = \pi f_0 N^2 S_{REF}$ from $f = -\infty$ to $f = +\infty$.

To appreciate the reference phase noise's significance, let us assume a noiseless PLL and express the output jitter as

$$\begin{aligned}\sigma_j &= \frac{\sqrt{A_{REF}}}{2\pi}\frac{T_{REF}}{N} \\ &= \sqrt{\frac{f_0}{4\pi}\frac{S_{REF}}{f_{REF}^2}},\end{aligned} \tag{2.3}$$

where $T_{REF} = 1/f_{REF}$. If f_0 is near its practical upper bound of $0.1 f_{REF}$, we can plot σ_j as a function of S_{REF} and f_{REF} (Figure 2.2). The resulting envelope indicates that, for $\sigma_j = 20$ fs$_{rms}$, one can select $200\ \text{MHz} \leqslant f_{REF} \leqslant 500\ \text{MHz}$ and $-175\ \text{dBc/Hz} \leqslant S_{REF} \leqslant -170\ \text{dBc/Hz}$. The situation becomes more difficult if the VCO phase noise is included.

The VCO phase noise contribution, S_{out2}, can be approximated as shown in Figure 2.1(c), with a plateau up to $\pm f_1$ and an α/f^2 roll-off beyond this offset. The total area under this profile is equal to $A_{VCO} \approx 4 S_1 f_1$, where $S_1 \approx \alpha/f_1^2$. For $\zeta > 2$, we have $f_1 \approx f_0$. We must now minimize $S_{tot} = A_{REF} + A_{VCO}$ as a function of the loop bandwidth, f_0. The optimum bandwidth is given by

$$f_{0,opt} = \sqrt{\frac{4\alpha}{\pi N^2 S_{REF}}}, \tag{2.4}$$

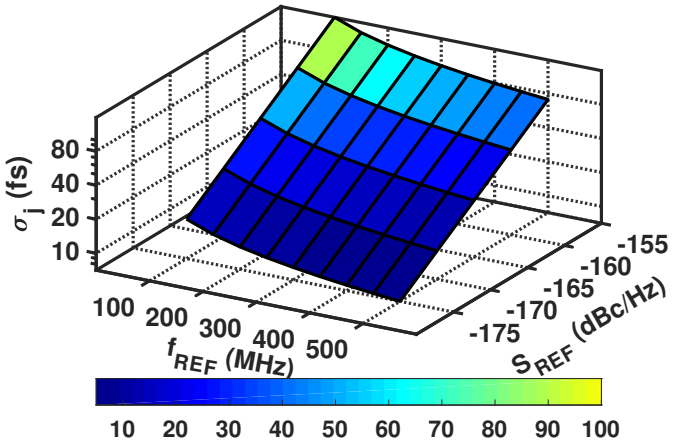


Figure 2.2: Integrated jitter of PLL as a function of reference frequency and reference phase noise.

and the minimum integrated phase noise by

$$S_{tot,min} = 4\sqrt{\alpha\pi N^2 S_{REF}}. \tag{2.5}$$

This optimum leads to two attributes. First, the reference and VCO contributions become approximately equal. Second, the plateaus in the output spectra of Figs. 2.1(b) and (c) roughly coincide. This is seen by recognizing that, for $f \ll f_0$, $S_{out1} = N^2 S_{REF}$ and $S_{out2} \approx \alpha/f_{0,opt}^2 \approx (\pi/4)N^2 S_{REF}$. It can also be shown that the tails of S_{out1} and S_{out2} coincide in a similar manner. In other words, the optimum attempts to shape the reference profile so that it resembles that of the VCO.

To obtain the total jitter, we write

$$\begin{aligned}\sigma_j &= \frac{\sqrt{S_{tot,min}}}{2\pi}\frac{T_{REF}}{N}, \\ &= \sqrt[4]{\frac{\alpha S_{REF}}{\pi^3 N^2}}\frac{1}{f_{REF}}.\end{aligned} \tag{2.6}$$

We repeat the plot of Figure 2.2 for Eq. (2.6), assuming that the VCO is so designed as to provide a phase noise of α/f^2 = -113 dBc/Hz at 1-MHz offset (as is the case in our prototype) (Figure 2.3). To obtain a jitter of 20 fs$_{rms}$, we can still choose $200\ \text{MHz} \leqslant f_{REF} \leqslant 500\ \text{MHz}$ and $-175\ \text{dBc/Hz} \leqslant S_{REF} \leqslant -170\ \text{dBc/Hz}$. With $f_{REF} = 250$ MHz and $S_{REF} = -170$ dBc/Hz,

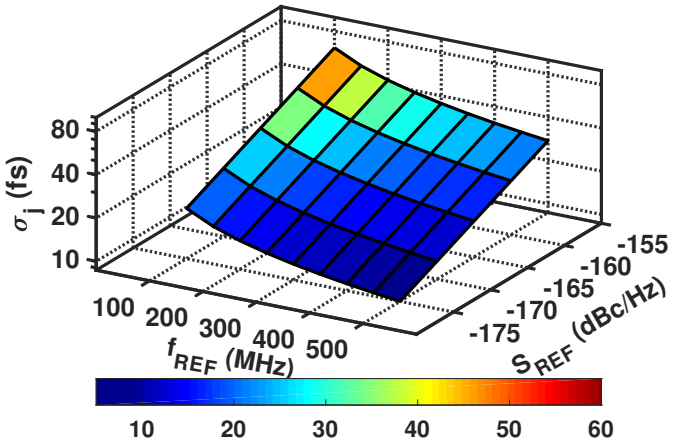


Figure 2.3: Optimum integrated jitter of PLL as a function of reference frequency and reference phase noise for a VCO phase noise of -113 dBc/Hz at 1-MHz offset.

we must have a loop bandwidth of 10 MHz. Note that these results apply to subsampling PLLs as well.

2.2.2 Reference Buffer Phase Noise

Stand-alone low-noise crystal oscillators typically provide a nearly-sinusoidal output. For example, Crystek's CRBSCS-01-250, used in our measurements, exhibits harmonics that are at least 20 dB below the fundamental. The sampling phase detector can directly sample this sinusoidal waveform [21, 22], but the noise contribution from the sampler and the following Gm stage will be large due to the low phase detector gain. This waveform must be sharpened by an on-chip inverter before reaching the PLL, thereby suffering from additional phase noise. The resulting phase noise adds to that of the crystal oscillator and must be included in the bandwidth optimization described above. The principal issues here are that, owing to the slow input transitions, (1) the inverter transistors inject noise over a long time window, and (2) both devices produce noise on each output edge.

For a sinusoidal input, the output slew rate (SR_{out}) strongly depends on the input slew rate (SR_{in}). As an approximation, we can say that the two differ by a factor equal to the inverter's

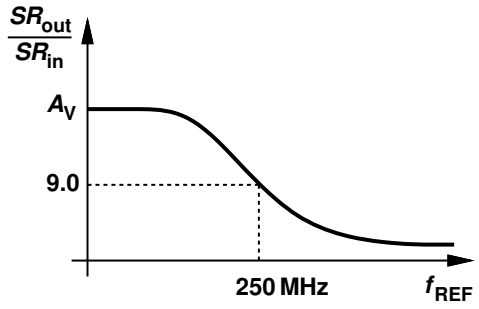


Figure 2.4: SR_{out}/SR_{in} ratio vs reference frequency.

small-signal voltage gain, A_v. At sufficiently high frequencies, however, the output slew rate is also limited by the output current and the load capacitance. We thus expect the general behavior depicted in Figure 2.4. For the reference buffer (RBUF) design in our work, we note that $SR_{out}/SR_{in} \approx 9$ at 250 MHz.

The phase noise of an inverter due to the transistors' white noise is derived in [23] for an input with a period of T_{in} and expressed as

$$S_\phi(f) = \frac{\pi^2}{r_{edge}^2 C_L^2} \frac{\Delta T}{T_{in}} \left[S_{I,N}(f) + S_{I,P}(f) \right], \tag{2.7}$$

where r_{edge} is the output slew rate (also denoted by SR_{out} in this paper), C_L the load capacitance, ΔT the noise window shown in Figure 2.5(a), and $S_{I,N}(f)$ and $S_{I,P}(f)$ the noise current spectra of the NMOS and PMOS devices, respectively.[1] This result is derived for relatively fast input edges, and assumes that only the NMOS device corrupts the falling edge and only the PMOS device, the rising edge.

Equation (2.7) can be extended to the case of a sinusoidal input as follows. We consider the input and output waveforms shown in Figure 2.5(b), noting that the NMOS transistor enters saturation at t_1. We also assume t_1 to be the starting point of the PMOS noise window because the noise injected onto C_L before t_1 is discharged by the triode NMOS device. This point is verified by transient simulations in Cadence's Spectre. Another simplifying assumption is that the noise

[1]These spectra are measured with $|\mathrm{V_{GS}}| = \mathrm{V_{DD}}$ and $|\mathrm{V_{DS}}| = \mathrm{V_{DD}}/2$.

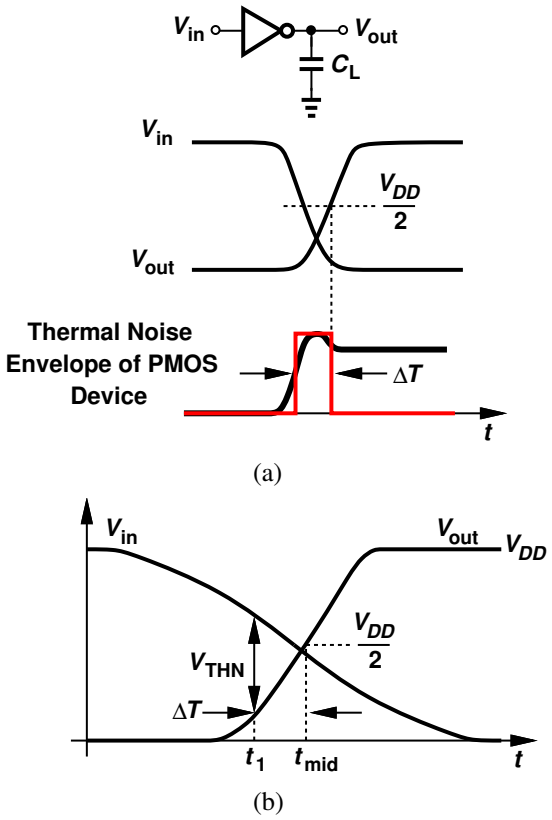


Figure 2.5: (a) CMOS inverter input/output waveforms during sharp transitions, and (b) noise window of NMOS device in RBUF with a sinusoidal input.

injected by the transistors after t_{mid} is unimportant to the output phase noise [23]. We conclude that, for both transistors, the noise window, ΔT, is from t_1 to t_{mid}, which is approximately half of the rise time. The overall output phase noise then emerges as:

$$S_\phi(f) = \frac{2\pi^2}{r_{edge}^2 C_L^2} \frac{\Delta T}{T_{in}} \left[S_{I,N}(f) + S_{I,P}(f) \right], \tag{2.8}$$

where we assume equal output rise and fall times and hence the same ΔT for the two edges. The factor of 2 accounts for the phase corruption on each edge due to both devices.

The dependence of the RBUF phase noise upon the input frequency is of interest but is made more complex by the behavior depicted in Figure 2.4. In this particular design, the buffer's phase noise decreases by about 1.4 dB if f_{REF} rises from 40 MHz to 80 MHz. This is because SR_{out} in Figure 2.4 increases by only a factor of 1.4 and ΔT decreases by a factor of 1.4 in Eq. (2.8).

With T_{in} halved, the right hand side of Eq. (2.8) drops by a factor of $(1.4)^3/2 \equiv 1.4$ dB. Plotted in Figure 2.6 are the simulated phase noise profiles of our buffer for f_{REF} = 40 MHz, 80 MHz, 160 MHz and 250 MHz. The key point here is that the buffer's integrated jitter falls as f_{REF} rises. In Figure 2.6, the corresponding rms jitter values are equal to 79.2 fs, 33.7 fs, 14.3 fs and 8.5 fs.

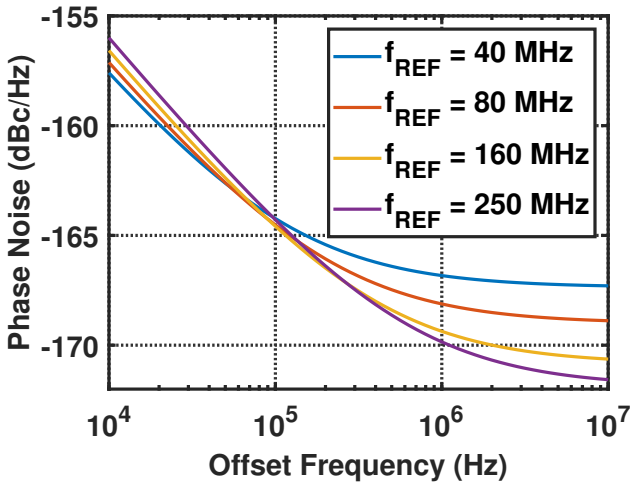


Figure 2.6: Phase noise of reference buffer at different input frequencies.

Besides using higher reference frequencies, the noise-power trade-off of RBUF can also be exploited to reduce its jitter contribution. If the inverter's output capacitance is much greater than the input capacitance of the next stage, every doubling of the transistor widths lowers the phase noise by 3 dB. This can be seen from Eq. (2.8), where $S_{I,N}(f)$, $S_{I,P}(f)$, and C_L are doubled while other quantities remain unchanged. In this work, the NMOS and PMOS aspect ratios are 1120 μm/400 nm and 1600 μm/400 nm, respectively, leading to a power consumption of 1.3 mW at 250 MHz and the phase noise profile shown in Figure 2.6. With such large dimensions, the buffer still contributes significant jitter, underscoring the future challenges that we will face as we seek smaller jitter values.

The last issue related to RBUF is its supply sensitivity, K_{DD}. Typically fed from an on-chip low-dropout (LDO) regulator, RBUF converts the LDO noise to phase noise. For the inverter design described above, K_{DD} = 1.2 rad/V. To maintain the supply-induced phase noise about 10 dB below the profile shown in Figure 2.6, the LDO noise spectrum must be less than 0.5 nV/$\sqrt{\mathrm{Hz}}$,

an extremely stringent constraint. For example, an LDO op amp employing a differential pair with ideal exponential transistors would require a tail current of at least 3.4 mA to achieve this noise level. As explained in Section 3.2, our proposed phase detector relaxes this issue by orders of magnitude.

2.2.3 Phase/Frequency Detector Phase Noise

The phase noise of phase/frequency detectors (PFDs) has been analyzed in [23], with the conclusion that true single-phase clocking (TSPC) implementations are advantageous. Figure 2.7(a) depicts an example optimized according to [23] and Figure 2.7(b) plots the circuit's simulated phase noise at 250 MHz. Consuming 60 μW, the PFD generates an rms jitter of 9.4 fs. For this value to fall below, for example, 5 fs, one would need to multiply the transistor widths by a factor of 3.5.[2] The PFD therefore does not appear to be serious bottleneck.

2.2.4 Charge Pump Noise

The thermal and flicker noise of the up and down current sources in a charge pump (CP) corrupt the current delivered to the loop filter, equivalently generating phase noise. It can be shown that the CP thermal noise referred to the PFD input leads to

$$S_{CP}(f) = 8\pi^2 \frac{T_{CP}}{T_{REF}} \frac{\overline{I_n^2}}{I_P^2}, \tag{2.9}$$

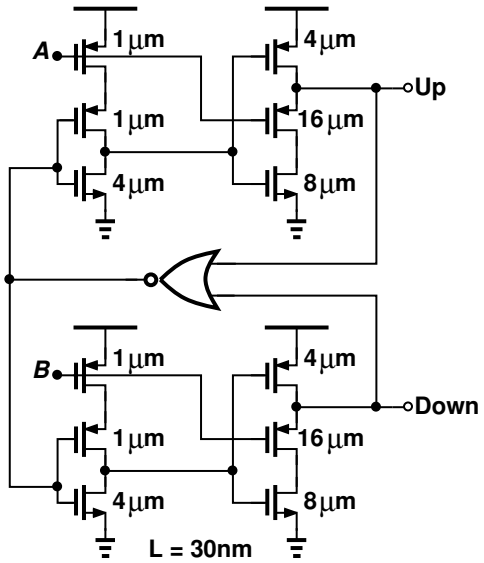
where T_{CP} denotes the minimum PFD output pulse width, $\overline{I_n^2}$ the thermal noise spectrum of each current source, and I_P the nominal CP current. Neglecting the CP flicker noise and considering typical values for the parameters in Eq. (2.9), we can readily appreciate the difficulties. Suppose we wish the CP contribution in a PLL bandwidth of 10 MHz to be less than 5 fs. From Section 2.2.1, we have

$$\frac{\sqrt{\pi f_0 S_{CP}}}{2\pi} T_{REF} < 5 \text{ fs}. \tag{2.10}$$

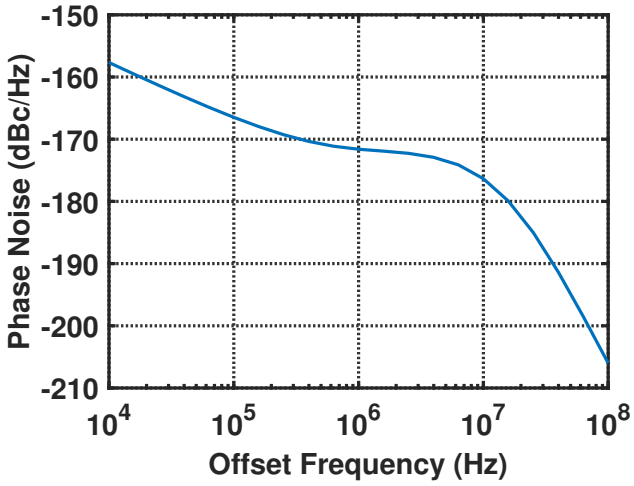
[2]Every doubling of the transistor widths in the PFD reduces the jitter by a factor of $\sqrt{2}$.

It follows that S_{CP} = -177 dBc/Hz if T_{REF} = 4 ns. Returning to Eq. (2.9) and assuming (1) $\overline{I_n^2} = 2kT\gamma g_m = 2kT\gamma(2I_P)/|V_{GS} - V_{TH}|$, (2) $|V_{GS} - V_{TH}|$ = 200 mV, and (3) T_{CP} = 50 ps, we obtain I_P = 110 mA.

The foregoing observations suggest that CPs prove ill-suited to low-jitter PLLs.



(a)



(b)

Figure 2.7: (a) Optimized TSPC PFD, and (b) phase noise of TSPC PFD.

CHAPTER 3

A 19-GHz Integer-N PLL with 20.3-fs Jitter

In this chapter, we proposed a low-jitter PLL architecture and analyze the phase noise of each block.

The proposed PLL architecture is shown in Figure 3.1. It consists of a reference buffer, a double-sampling PD (DSPD), a transconductor, a loop filter, a VCO followed by a $\div 2$ stage, and a multimodulus "self-retimed" divider that controls the PD through a nonoverlap generator. We wish to make negligible the jitter arising from the PD, the Gm stage, and the divider. If successful, such an endeavor allows us to apply the optimization described in Section 2.2.1.

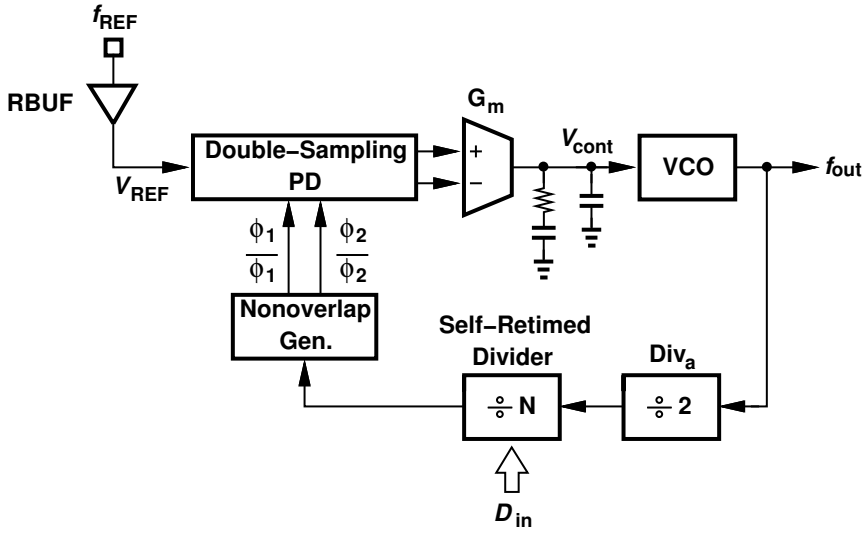


Figure 3.1: Proposed PLL architecture.

3.1 Double-Sampling PD

The PD proposed here plays a central role in the PLL's performance. Before describing this topology, we consider the (single) master-slave sampling PD introduced in [24, 25] and shown in Figure 3.2(a). The circuit adjusts the PLL feedback signal, ϕ_1, such that the sampled value of V_{REF} (V_a) becomes equal to the control voltage necessary for the VCO (Figure 3.2(b)).

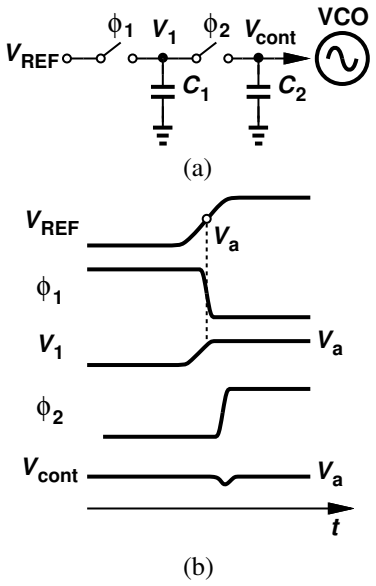


Figure 3.2: (a) Single-sampling PD, and (b) its time-domain waveforms.

Next, ϕ_2 and C_2 resample this level, creating minimal perturbation on V_{cont}. [1]

Owing to the high slew rate of V_{REF}, the master-slave sampling PD exhibits a high gain, thereby minimizing the noise contributed by the switched-capacitors and any other components preceding the VCO. If the slew rate of V_{REF} in Figure 3.2(b) is denoted by SR_{REF}, this PD's gain emerges as

$$K_{PD} = \frac{SR_{REF}}{2\pi \cdot f_{REF}}. \tag{3.1}$$

[1]The PD can directly sample the reference sinusoid (without a buffer) [21, 22], but the much lower PD gain makes the noise of the subsequent stages more significant.

We now turn to the proposed double-sampling PD shown in Figure 3.3(a). Assuming for now that V_{REF} has a 50% duty cycle, we note that C_1 and C_2 sample V_a and V_b, respectively, such that $V_a - V_b$ translates to the necessary control voltage for the VCO. The double-sampling action not only provides higher gain than single sampling but also offers new benefits. We elaborate on these points below.

Double sampling increases the PD gain by a factor of 2. This is seen by noting that, in Figure 3.3(b), a phase displacement of Δt in ϕ_1 shifts both A and B to the right or to the left, changing V_a and V_b in *opposite* directions. Thus,

$$K_{PD} = \frac{SR_{REF}}{\pi \cdot f_{REF}}. \tag{3.2}$$

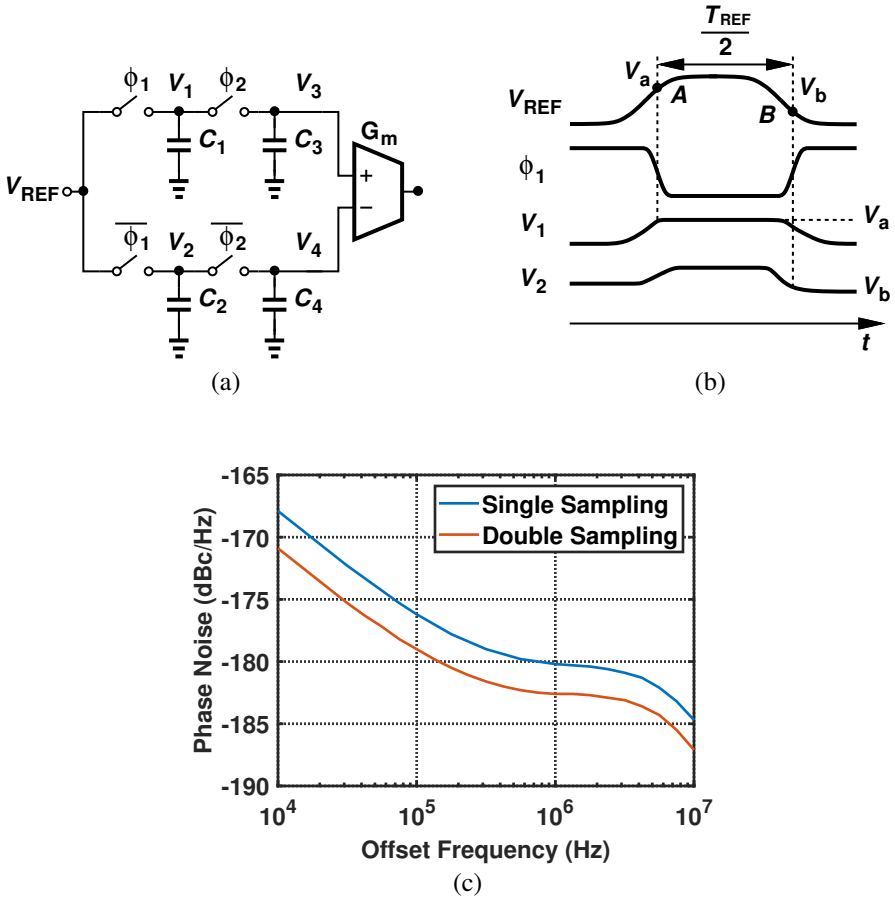


Figure 3.3: (a) Double-sampling PD, (b) its time-domain waveforms, and (c) its simulated phase noise.

As a result, the kT/C noise components associated with the four switches in Figure 3.3(a) are divided by another factor of 4 when referred to the PD input (Section 3.3), providing a 3-dB reduction in PD's phase noise. For $C_1 = C_2 = 100$ fF and $C_3 = C_4 = 40$ fF, simulations yield the phase noise profiles shown in Figure 3.3(c) at 250 MHz. The integrated jitter drops from 2.9 fs to 2.1 fs.

3.2 Reference Phase Noise Reduction

The most remarkable advantage of double sampling arises from its ability to reduce the jitter contributed by the crystal oscillator and the reference buffer. We present this property for three sources of phase noise, namely, thermal noise, supply noise, and flicker noise.

Illustrated in Figure 3.4(a), this PD attribute can be understood by assuming that the rising edge of V_{REF} is displaced by a random amount, Δt_1. Consequently, the sampled voltage inherited by V_3 in Figure 3.3(a) changes by

$$\Delta V_3 = \Delta t_1 \cdot SR_{REF}. \tag{3.3}$$

if charge sharing between C_1 and C_3 is neglected.

Similarly, a displacement of Δt_2 in the falling edge translates to a change of

$$\Delta V_4 = \Delta t_2 \cdot SR_{REF}. \tag{3.4}$$

in V_4. These random changes are combined by the differential-to-single-ended converter shown in Figure 3.3(a). If V_{REF} carries white phase noise and hence Δt_1 and Δt_2 are uncorrelated, the differential output noise of the double-sampling PD is given by

$$\overline{V_{n,out}^2} = SR_{REF}^2 \cdot (\sigma_{\Delta t_1}^2 + \sigma_{\Delta t_2}^2). \tag{3.5}$$

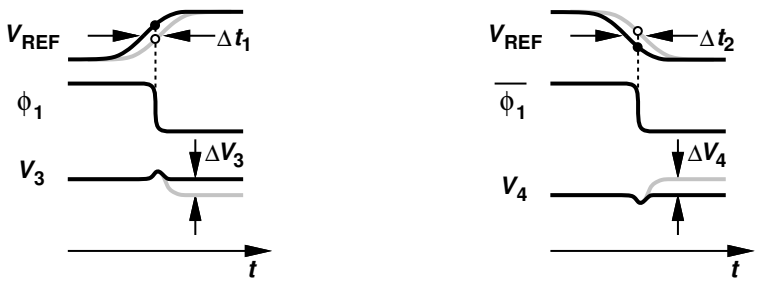
where $\sigma_{\Delta t_1}$ and $\sigma_{\Delta t_2}$ denote the rms jitter of V_{REF} on the rising and falling transitions, respectively. Divided by K_{PD}^2, this noise is referred to the PD input as

$$\phi_{n,in,rms}^2 = \frac{\pi^2}{T_{REF}^2}(\sigma_{\Delta t_1}^2 + \sigma_{\Delta t_2}^2). \tag{3.6}$$

To appreciate the significance of this result, we convert $\phi_{n,in,rms}$ to jitter:

$$\overline{\sigma_j^2} = \frac{\sigma_{\Delta t_1}^2 + \sigma_{\Delta t_2}^2}{4}. \tag{3.7}$$

That is, double sampling in essence averages the jitter of the PD input rising and falling edges, providing a 3-dB reduction. This property applies to the jitter of both the crystal oscillator and the



(a) (b)

Figure 3.4: Double-sampling PD detecting (a) rising edge of V_{REF}, or (b) falling edge of V_{REF}.

reference buffer.

Plotted in Figure 3.5 are the simulated phase noise profiles at the output of a noiseless PLL employing our RBUF design and with single-sampling and double-sampling PDs. The PLL band-

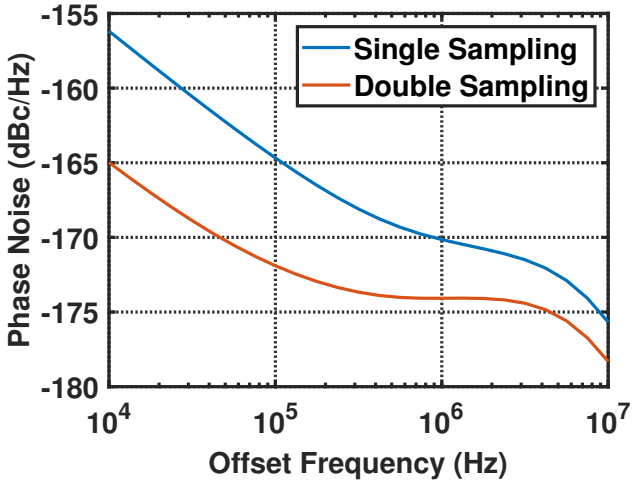


Figure 3.5: Simulated phase noise of RBUF in a noiseless PLL.

width is about 10 MHz and the feedback divide ratio is unity. We note that the phase noise of RBUF is lowered by 3 dB around 1-MHz offset in the latter case.

At low offsets, double sampling reduces the phase noise by even greater factors, e.g., by 7 dB at 100 kHz; we explain this phenomenon below. The integrated jitter falls from 8.6 fs_{rms} to 5.8 fs_{rms}.

The proposed PD also lowers the effect of RBUF supply noise dramatically. Unlike noise

sources within an inverter, the supply noise modulates the output *duty cycle*, and the double-sampling PD converts this effect to a common-mode perturbation. To illustrate this point, we begin with the RBUF output waveform, V_{REF}, shown in Figure 3.6 and recognize that a static supply change of $+\Delta V_{DD}$ raises the slew rates while keeping the transition times fairly constant. As a result, the duty cycle increases. We observe that the values sampled by ϕ_1 on the rising and falling edges shift up together, introducing a common-mode change of $\Delta V_3 = \Delta V_4$ in V_3 and V_4. Most of this perturbation is rejected by the Gm stage. Verified experimentally (Section **??**), this

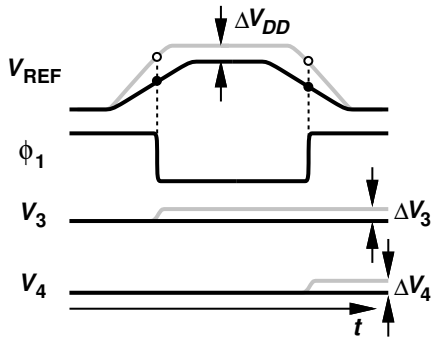


Figure 3.6: Double-sampling PD response to RBUF supply noise.

property greatly eases the LDO output noise requirement.

If the supply noise frequency is high enough to cause substantial change from one V_{REF} edge to the next, then the PD suppresses the result to a lesser extent. But such noise components can be filtered by means of moderately-sized capacitors attached to the LDO output.

The common-mode effect described above also explains the large RBUF phase noise suppression observed at low offsets in Figure 3.5. Recall from Section 2.2.2 that *both* transistors in the buffer inject noise on the output rising and falling edges. For example, the flicker noise current of M_1 in Figure 3.7 injects excess positive charge on the rising transition of $\mathrm{V_{REF}}$, thus shifting it upward. Another packet of positive charge is also deposited on C_L on the falling edge, shifting this transition upward as well. The falling transition is delayed by approximately the same amount because this noise changes negligibly in a time interval of $T_1 \approx T_{REF}/2$. That is, the noise components injected by M_1 on two consecutive edges are strongly correlated. As a result, in a manner

similar to that in Figure 3.6, the flicker noise of M_1 and M_2 translates to a CM error in V_3 and V_4 and is thus suppressed.

3.3 PD Transfer Function and Phase Noise

The single-sampling circuit of Figure 3.2(a) can be approximately modeled by the following transfer function [24]:

$$H_{PD}(j\omega) = \frac{SR_{REF}}{2\pi \cdot f_{REF}} \cdot \frac{1}{1 + \dfrac{C_2}{C_1 f_{REF}} j\omega} \times \\ \times e^{-j\omega T_{REF}/2} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}. \tag{3.8}$$

For the double-sampling counterpart, the gain rises by a factor of 2 but the remaining terms are unchanged. With a gain of $SR_{REF}/(\pi f_{REF})$ = 39.5 V/rad, f_{REF} = 250 MHz, C_1 = 100 fF, and C_2 = 40 fF, the PD magnitude and phase responses are relatively flat across the bandwidth of 10 MHz chosen in this design. That is, the PD behavior negligibly affects the PLL dynamics.

The PD phase noise, $\phi_{n,PD}$, arises primarily from the samplers' kT/C noise. If C_1 = C_2 and C_3 = C_4 in Figure 3.3(a), the noise voltage deposited on C_1 is equal to $\sqrt{kT/C_1}$, corresponding to a charge amount of $\sqrt{kTC_1}$. This charge is next shared with C_3, yielding a voltage of $\sqrt{kTC_1}/(C_1 + C_2)$. The square of this value is added to the kT/C noise associated with the slave sampler, and the final result is multiplied by 2 for the differential output:

$$V^2_{n,out,rms} = 2\left[\frac{kTC_1}{(C_1 + C_2)^2} + \frac{kT}{C_2}\right]. \tag{3.9}$$

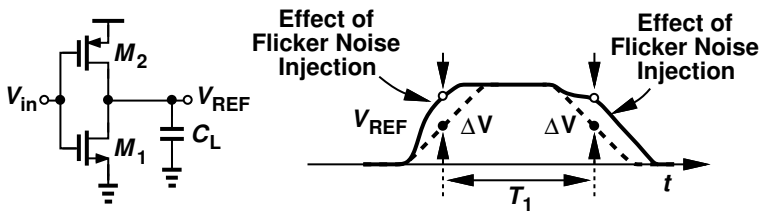


Figure 3.7: Effect of RBUF flicker noise.

We must now divide this quantity by the square of the PD gain to obtain the equivalent phase noise. This gain, $SR_{REF}/(\pi f_{REF})$, can be approximated as follows. When the voltage on C_1 is around $V_{DD}/2$, the current available for charging it is given by $(V_{DD} - V_{DD}/2)/(R_{BUF} + R_{sw})$, where R_{BUF} and R_{sw} denote the buffer output resistance and the switch resistance, respectively. Thus,

$$SR_{REF} \approx \frac{V_{DD}}{2(R_{BUF} + R_{sw})C_1}. \tag{3.10}$$

From Eqs. (3.9), (3.10) and (3.2), we compute the PD's jitter as

$$\begin{aligned}\phi^2_{in,,PD,rms} &= \frac{\phi^2_{n,PD,rms} \cdot T^2_{REF}}{(2\pi)^2 K^2_{PD}} \\ &= \frac{2kT}{V^2_{DD}}(R_{BUF} + R_{sw})^2 C_1^2 \left[\frac{C_1}{(C_1 + C_2)^2} + \frac{1}{C_2}\right]. \end{aligned} \tag{3.11}$$

Note, however, that this jitter "power" resides in a frequency range of $-f_{REF}/2$ to $+f_{REF}/2$.

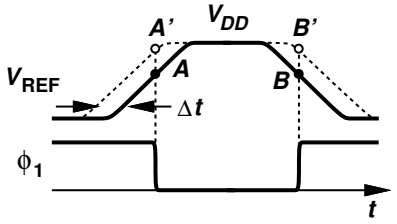


Figure 3.8: V_{REF} duty cycle error.

We must therefore divide $\phi^2_{in,,PD,rms}$ by f_{REF}, subject the spectrum to the PLL transfer function, and integrate the result.

3.4 Effect of Duty Cycle Error

The PD operation described in Section 3.1 tacitly assumes a duty cycle of 50% for the reference. Crystal oscillators, on the other hand, can suffer from some duty cycle error (DCE). We wish to determine how DCE affects the performance.

Consider the reference buffer waveforms shown in Figure 3.8(a), where the solid plot represents a duty cycle of 50% and the dashed plot a greater value. We observe two phenomena. (1) Samples

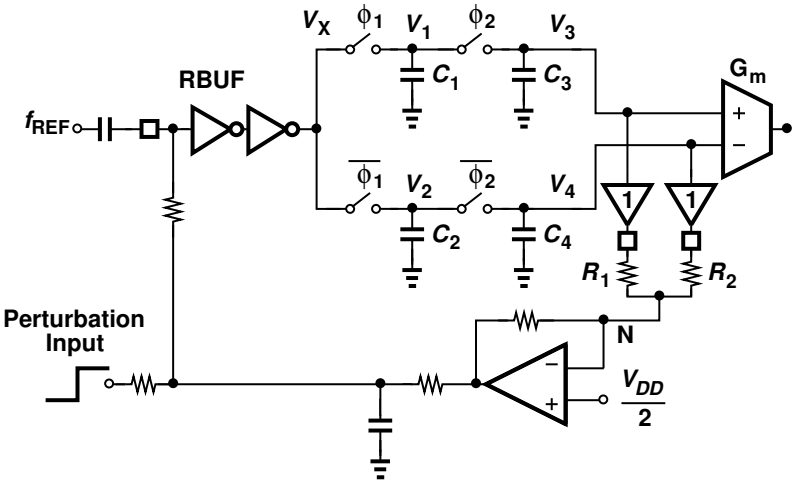


Figure 3.9: V_{REF} duty cycle correction circuit.

A and B assume a higher common-mode level as the duty cycle increases. That is, for a sufficiently large DCE, the CM level approaches V_{DD} or zero, an issue resolved by designing the Gm stage in Figure 3.1 so as to accommodate rail-to-rail inputs. (2) Either A' or B' in Figure 3.8 can land near V_{DD}, carrying little phase information and converting the circuit to a single-sampling PD. To avoid this difficulty, the input duty cycle can be adjusted such that the CM level of V_3 and V_4 in Figure 3.3(a) remains near $V_{DD}/2$.

3.5 Duty Cycle Detection and Correction

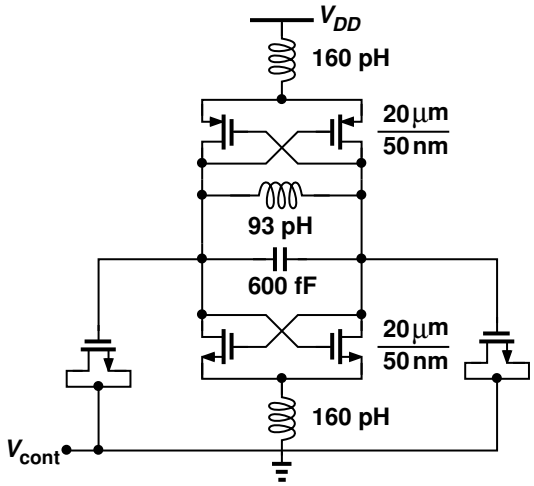
The task of duty cycle correction (DCC) has been widely studied [10, 26], achieving errors less than 0.004% [10]. An important advantage of the proposed double-sampling PD is the simplicity that it affords for duty cycle *detection*. As explained above, the optimum duty cycle ensures that the CM level of V_3 and V_4 in Figure 3.8, i.e., $(V_3+V_4)/2$, is around $V_{DD}/2$. Thus, $(V_3+V_4)/2-V_{DD}/2$ serves as the duty cycle error.

Figure 3.9 shows the duty cycle correction loop. On-chip unity-gain buffers sense V_3 and V_4 and resistors R_1 and R_2 provide their CM level at node N. For test and characterization flexibility, an off-chip op-amp compares the result with $V_{DD}/2$ and adjusts the bias input of the reference

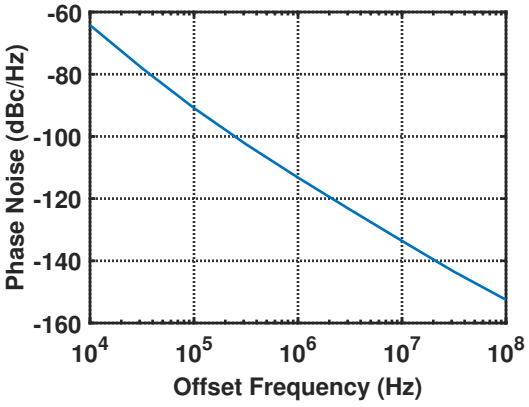
buffer. An external input port allows a perturbation to be applied to the loop so that its response can be studied (Section 3.9).

3.6 VCO and $\div 2$ Stage

Shown in Figure 3.10(a), the VCO employs a complementary LC topology with inductive tail resonance at the second harmonic.[2] Due to the lack of ultra-thick-metal layers, the 93-pH inductor is realized as two metal-8 and metal-9 octagons in parallel. The quality factor of the tank is around



(a)



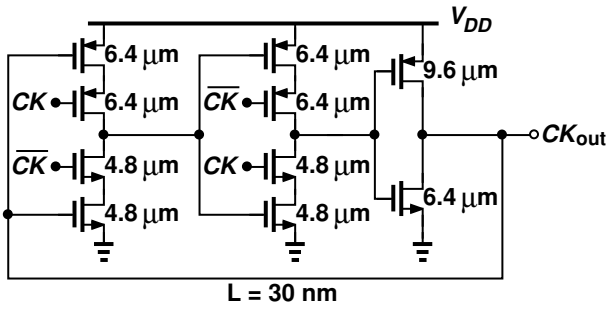
(b)

Figure 3.10: (a) VCO implementations, and (b) its simulated phase noise.

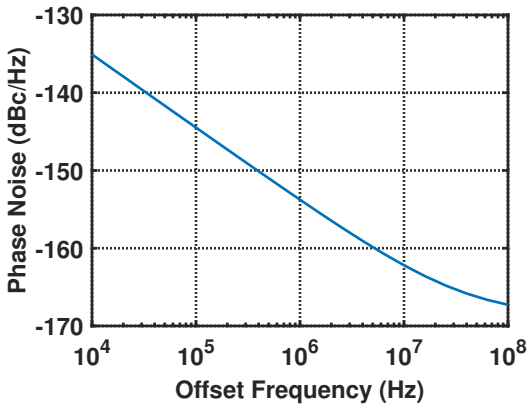
[2]The resonance occurs with the tail parasitics and is not tunable.

14.5, yielding the simulated phase noise profile shown in Figure 3.10(b) for a power consumption of 7.2 mW.

The $\div 2$ stage following the VCO in Figure 3.1 is realized using complementary CMOS (C^2MOS) logic and shown in Figure 3.11(a). Drawing 1.4 mW, the circuit exhibits the simulated output phase



(a)



(b)

Figure 3.11: (a) C^2MOS $\div 2$ circuit, and (b) its simulated phase noise at an input frequency of 20 GHz.

noise plotted in Figure 3.11(b), which translates to a jitter of about 2.6 fs.

3.7 Multimodulus Divider

Multimodulus dividers generally produce a great deal of phase noise because of the large number of asynchronous stages that they incorporate. It is possible to insert at the divider output a retiming flipflop (FF) driven by the VCO so as to remove the divider's phase noise [27]. This

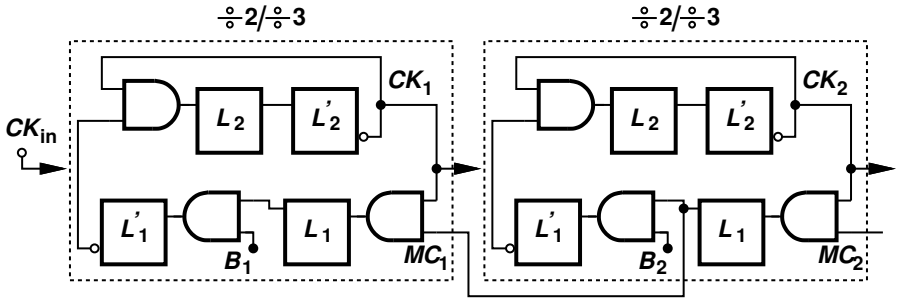
method, however, is prone to failure with process, supply voltage, and temperature (PVT) variations.

To elaborate on this point, we begin with the "modular" divider shown in Figure 3.12(a) [28], where L_j denotes a latch. For ease of illustration, we draw a 4-stage example as shown in Figure 3.12(b), follow it with a $\div 2$ circuit (necessary for our PLL), and retime its output by means of FF_0. We denote the delay of dual-modulus stage j by Δt_j. Constructing the circuit's waveforms as in Figure 3.12(c), we observe that FF_0 avoids metastability if the total delay from CK_{in} to CK_5 does not exceed one period of CK_{in}. More specifically, this path introduces the CK-to-Q delay of four $\div 2/3$ cells and one $\div 2$ stage. To this total, we must add the setup time of FF_0, arriving at the following bound:

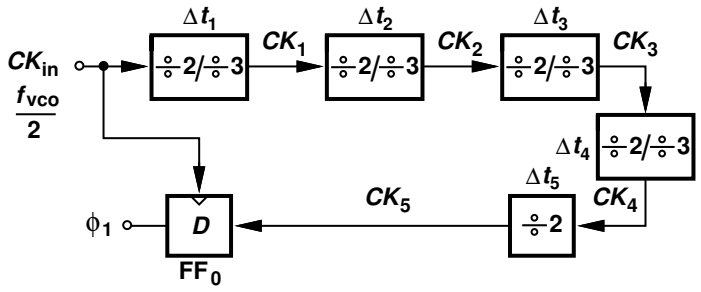
$$\Delta t_1 + \Delta t_2 + \cdots + \Delta t_5 + t_{setup,FF_0} \; < \; 100\,\text{ps}. \tag{3.12}$$

Otherwise, the falling edges of CK_{in} and and CK_5 can coincide and make FF_0 metastable, a condition that prohibits the system from locking.

Unfortunately, the condition expressed by Eq. (3.12) is difficult to meet even in the typical-typical corner of the process. Simulations of the extracted layout suggest a total delay of about 110 ps in this corner.



(a)



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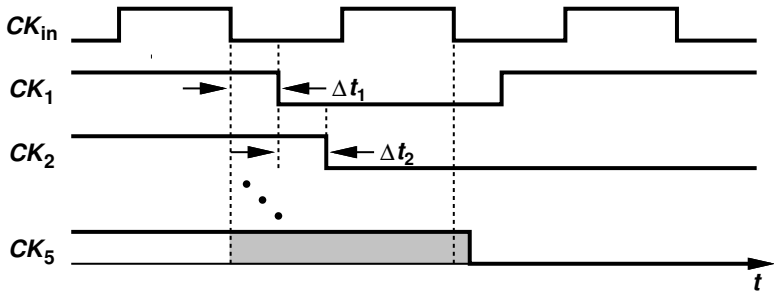
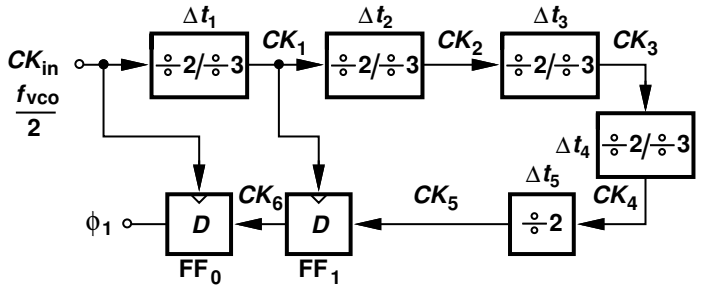


(c)



(d)

Figure 3.12: (a) Modular divider, (b) multimodulus divider with one flipflop as retimer, (c) timing diagram, and (d) multimodulus divider with two flipflops as retimers.

To alleviate this issue, we recognize that CK_1 in Figure 3.12(b) is also available as a retiming command. We then interpose between the $\div 2$ stage and FF_0 another flipflop and drive it by CK_1 [Figure 3.12(d)]. Here, FF_1 avoids metastability if the total delay from CK_1 to CK_5 is less than one period of CK_1:

$$\Delta t_2 + \cdots + \Delta t_5 + t_{setup,FF_1} < 200 \text{ ps}. \tag{3.13}$$

For FF_0, on the other hand, the delay from CK_{in} to CK_1 to CK_6 plus the setup time of FF_0 must remain less than 100 ps:

$$\Delta t_1 + \Delta t_{FF_1} + t_{setup,FF_0} < 100 \text{ ps}. \tag{3.14}$$

Of the two conditions prescribed by Eq. (3.13) and Eq. (3.14), the former proves more stringent as the extracted layout in the slow-slow high-temperature corner yields a value of 120 ps for its left-hand side. To improve the robustness of the circuit, we add one more flipflop as shown in Figure 3.13(a) obtaining

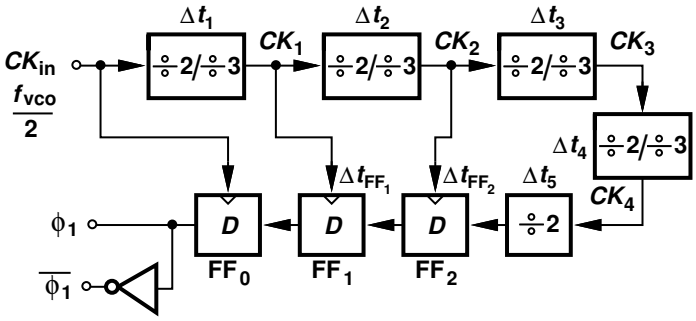
$$\begin{aligned} \Delta t_3 + \Delta t_4 + \Delta t_5 + t_{setup,FF_2} &< 400 \text{ ps} \\ \Delta t_2 + \Delta t_{FF_2} + t_{setup,FF_2} &< 200 \text{ ps} \\ \Delta t_1 + \Delta t_{FF_1} + t_{setup,FF_0} &< 100 \text{ ps}. \end{aligned} \tag{3.15}$$

The proposed divider in Figure 3.13(a) merits two remarks. First, the output, ϕ_1, carries only the phase noise of CK_{in} and FF_0. Second, this method guarantees that the excess delay around the critical loop is no more than the delay of one divider cell and one flipflop.

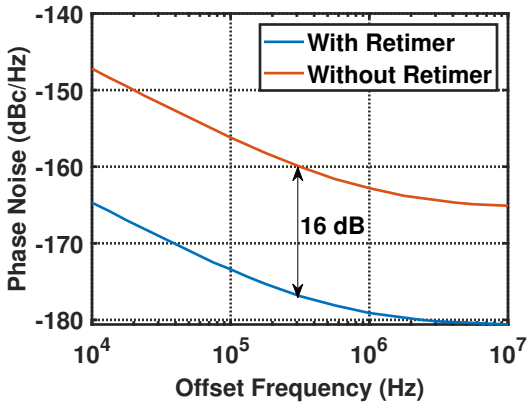
Plotted in Figure 3.13(b) are the divider output phase noise profiles before and after retiming flipflops are added, suggesting a 16-dB reduction. The integrated jitter falls from 19 fs to 3 fs.[3] Drawing 1.8 mW at 10 GHz (mostly in the input clock buffer), the circuit provides a divide ratio from 32 to 62.

The multimodulus divider blocks are realized by TSPC and CMOS circuits. Specifically, the first two $\div 2/3$ stages, FF_0, FF_1 employ the former type and the slower blocks, the latter.

[3]Simulations confirm our intuition that the phase noise is the same as in the case of using a single retiming flipflop.



(a)



(b)

Figure 3.13: (a) Proposed multimodulus divider with 3 flipflops as retimers, and (b) its simulated phase noise spectrum.

3.8 Nonoverlapping Clock Generator

In order to minimize the ripple on the control voltage, the PD of Figure 3.3(a) must avoid transparency between the master and slave samplers, requiring nonoverlapping clock phases. The challenge here is that conventional topologies, such as those based on cross-coupled gates, generate significant jitter. We must therefore avoid passing ϕ_1 through additional stages and yet generate ϕ_2. This is accomplished as shown in Figure 3.14(a), where latches L_1 - L_3 and delay stage ΔT produce a signal ϕ_0 at 500 MHz, with a delay of ΔT with respect to ϕ_1. From the ϕ_2 and $\overline{\phi_2}$ waveforms shown in Figure 3.14(b), we observe a nonoverlap time of ΔT, about 50 ps in this work. We should note that ϕ_0 and ϕ_2 inherit the phase noise of the delay stage, but the master samplers in Figure 3.3(a) rely on only ϕ_1 and $\overline{\phi_1}$. Since ϕ_2 and $\overline{\phi_2}$ only transfer charge to the slave

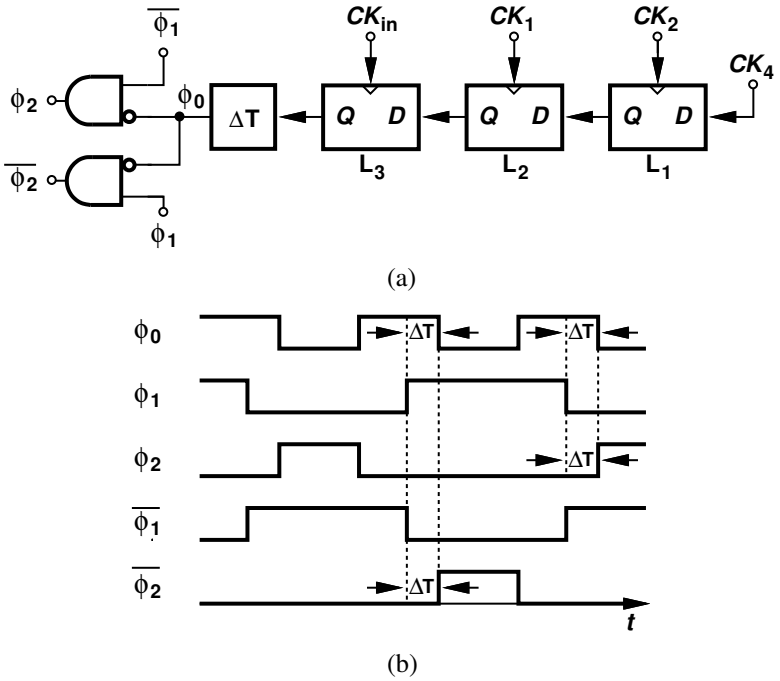


Figure 3.14: (a) Nonoverlapping clock generator, (b) nonoverlapping clock waveform.

capacitors, their phase noise is not critical.

3.9 Experimental Results

The proposed PLL has been fabricated in 28-nm CMOS technology. Figure 3.17 shows a photograph of the die, where the active area measures approximately $320\,\mu\mathrm{m} \times 310\,\mu\mathrm{m}$. The prototype consumes 12 mW: 7.2 mW in the VCO, 1.4 mW in the $\div 2$ stage, 1.8 mW in the multi-modulus divider, and 1.3 mW in the reference buffer.[4] The power supply voltage of reference buffer is 1.2 V and the rest of the PLL is supplied at 1 V. The loop is locked with a divide ratio of 80 and an output frequency of 20 GHz. The VCO has a gain of 120 MHz/V and a total tuning range of 450 MHz, allowing synthesis of only 20 GHz with a 250-MHz reference. This range somewhat relaxes the oscillator power-jitter trade-off and should be borne in mind in the comparison with the prior

[4]The DC current from the RBUF supply is 1.08 mA.

art (see below). The PD can be configured to operate as a single-sampling or a double-sampling circuit.

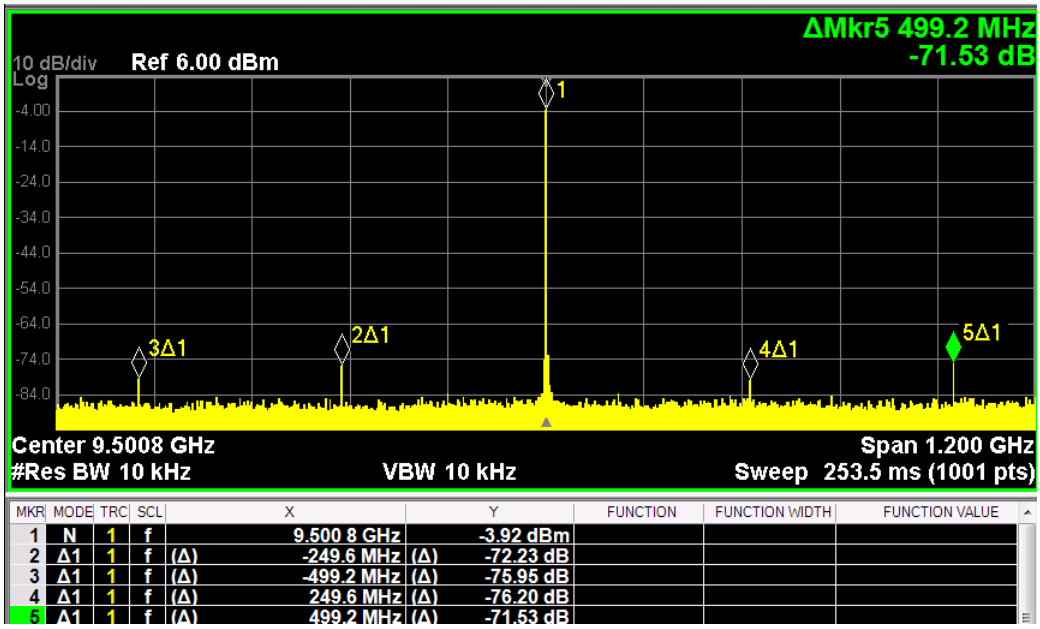


Figure 3.15: Measured PLL output spectrum.

The 250-MHz reference frequency is provided by Crystek's CRBSCS-01-250 crystal oscillator. Its phase noise is plotted in Figure 3.18, exhibiting a value of -171.5 dBc/Hz at 1-MHz offset.

For ease of measurement, the output of the $\div 2$ circuit, Div_a, in Figure 3.1 is used for the characterization. Figure 3.15 shows the measured spectrum, indicating a reference spur level of -72 dBc, which translates to -66 dBc at the VCO output.

Figure 3.16 plots the measured phase noise at the output of the $\div 2$ circuit for single sampling and double sampling. The profile exhibits a plateau of about -133 dBc/Hz up to 10-MHz offset and falls to -156 dBc/Hz at 100-MHz offset; the phase noise at the VCO output is 6 dB higher. We observe that double sampling lowers the profile by 2.5 dB from 10 kHz to 1 MHz and 1.5 dB from 1 MHz to 3 MHz. Since the VCO contribution remains the same,[5] the overall phase noise declines

[5]The value of the Gm following the PD is adjusted for single and double sampling so as to keep the loop bandwidth constant.

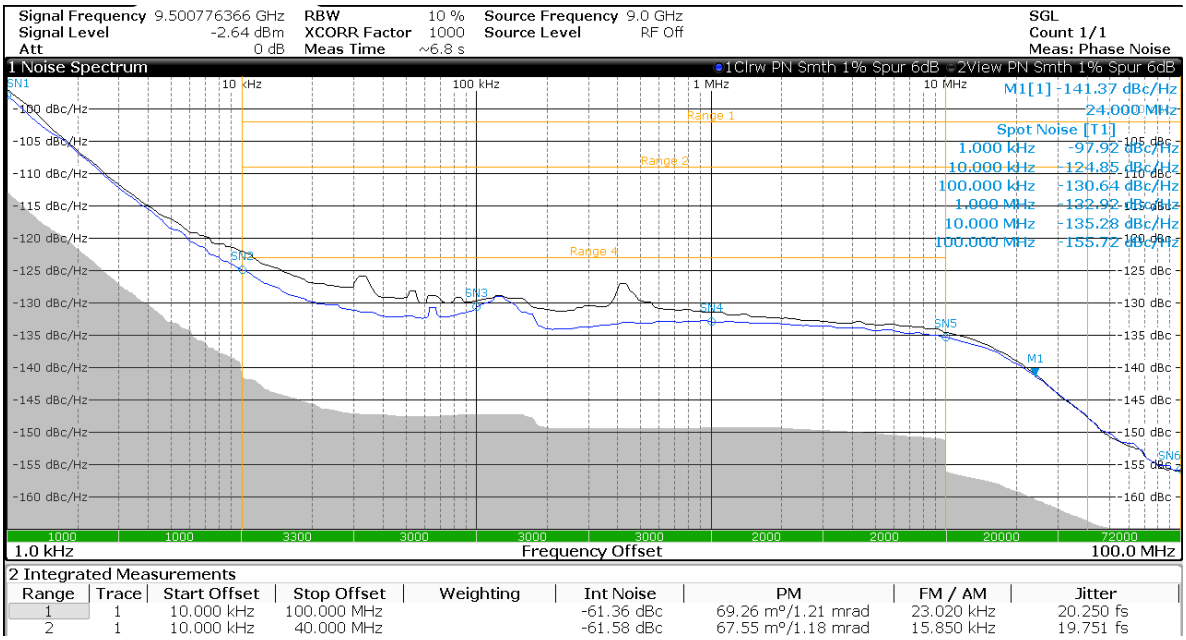


Figure 3.16: Measured PLL phase noise.

by less than 3 dB. The free-running VCO flicker noise corner is around 800 kHz, contributing negligible jitter after the loop is closed.

The jitter integrated from 10 kHz to 100 MHz is equal to 20.25 fs. According to simulations, the crystal oscillator contributes 10 fs, the reference buffer 6.2 fs, and the VCO 15 fs.

As explained in Section 3.1, the reference buffer supply rejection becomes critical unless the LDO feeding it provides an extremely low output noise voltage. With double sampling, on the other hand, this issue is greatly relaxed. This point is verified as follows. The supply voltage of the buffer is modulated by a sinusoid having a peak amplitude of 140 mV and a variable frequency. The corresponding spurs at the PLL output are then studied for single sampling and double sampling. Figure 3.19 plots the measured spur levels as a function of the sinusoid's frequency, revealing an improvement of at least 20 dB.

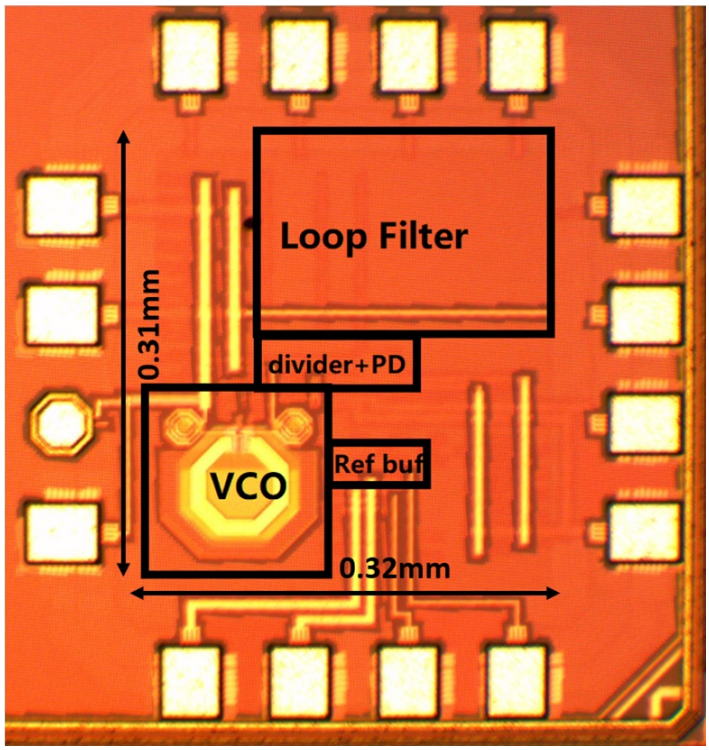


Figure 3.17: Die photograph.

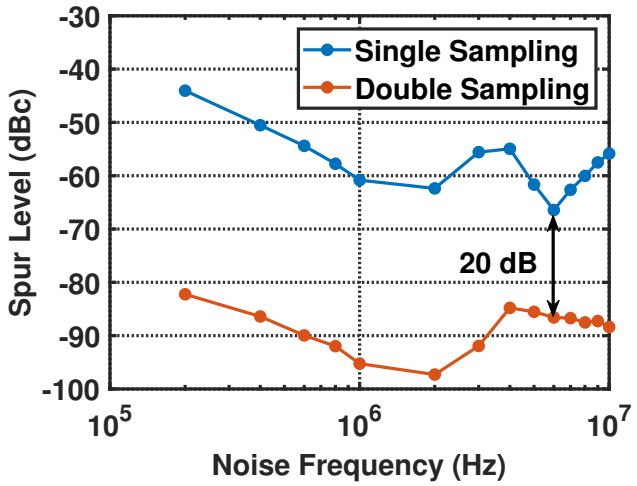


Figure 3.19: Measured spur level due to the RBUF supply disturbance.

The duty cycle and its correction circuit have been characterized by several tests. Since direct, accurate measurement of the duty cycle is difficult, we first disable the loop in Figure 3.9 and

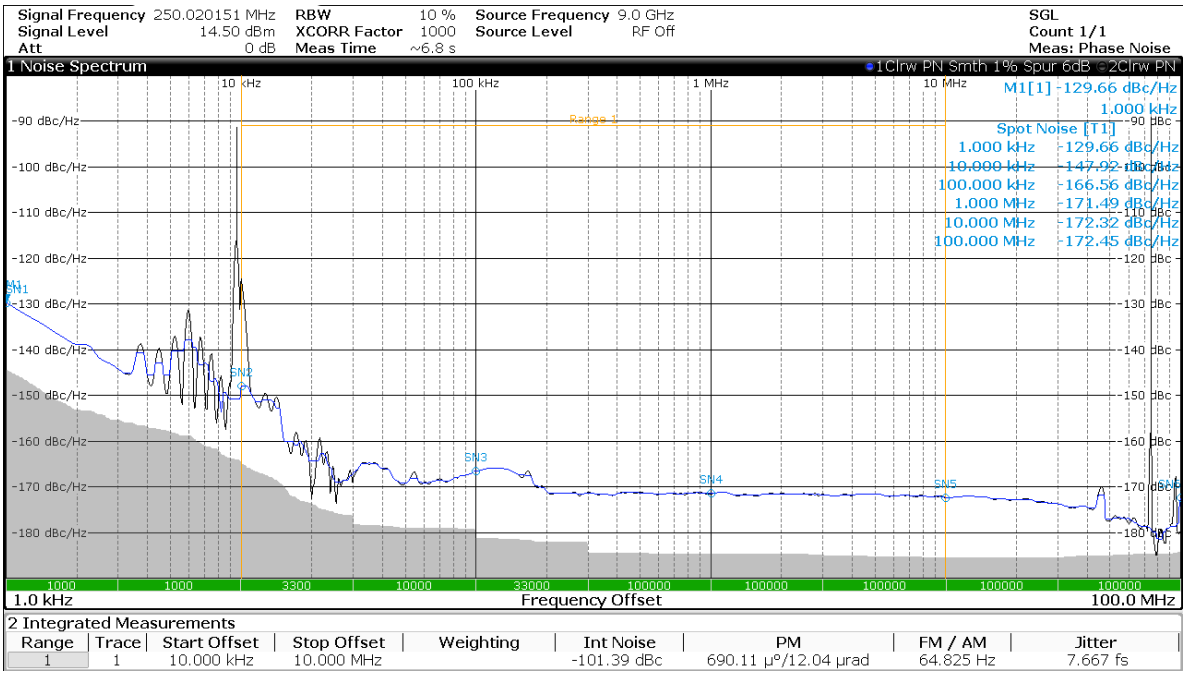


Figure 3.18: Measured phase noise of the 250-MHz crystal oscillator.

measure the PLL output reference spur levels and phase noise for different values of the PD output CM level, $V_{PD,CM}$. This is accomplished by changing the input bias voltage of RBUF. We also find the relationship between between $V_{PD,CM}$ and the duty cycle error (DCE) by simulations. We can then plot the spur levels and the integrated jitter as a function of DCE. The results are depicted in Figure 3.20. We should remark that the minima occur for $V_{PD,CM} \approx V_{DD}/2$. Next, we enable the correction loop and apply an external step as illustrated in Figure 3.9. Shown in Figure 3.21,

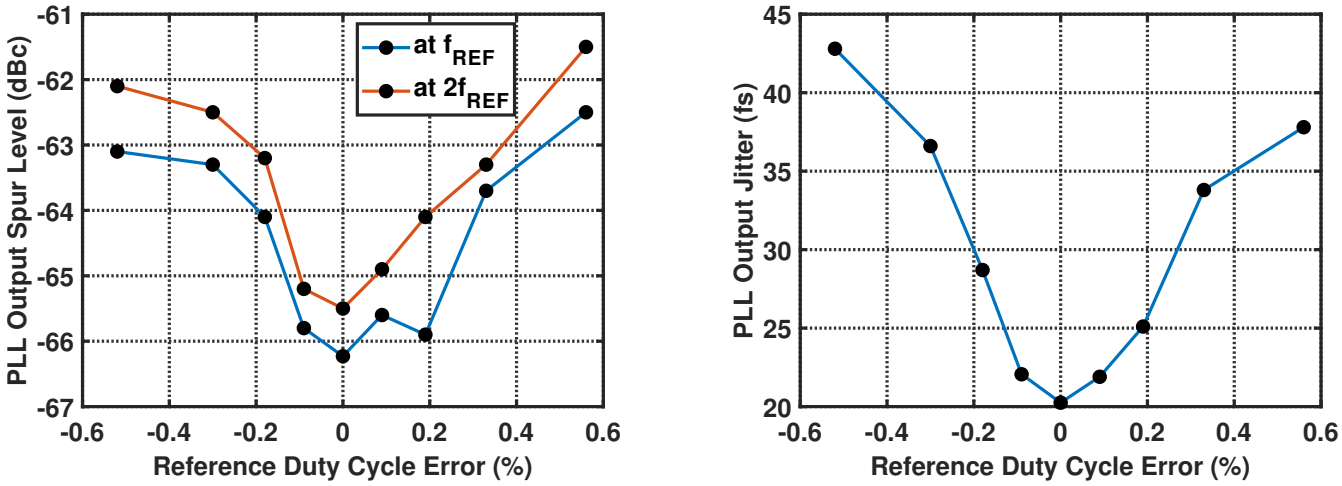


Figure 3.20: (a) Measured spur levels, and (b) PLL output jitter against V_{REF} DCE.

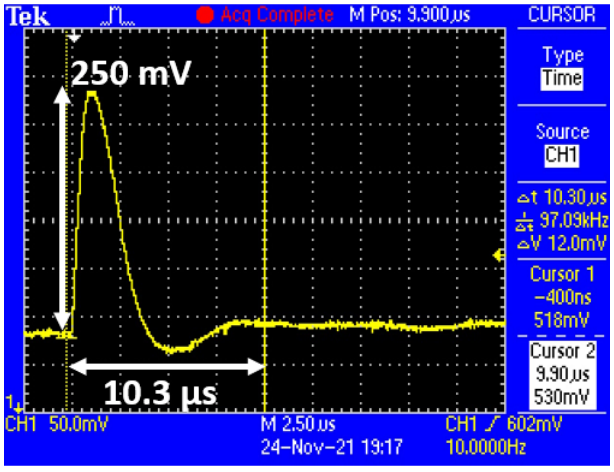


Figure 3.21: Measured transient response of $V_{PD,CM}$.

the transient response of $V_{PD,CM}$ reveals that this voltage jumps by 250 mV but returns to 530 mV($\approx V_{DD}/2$).

In order to study the robustness of the paper, we apply to the VCO supply voltage an external square wave having a peak-to-peak amplitude of 300 mV. The Agilent E5052A signal analyzer

captures the frequency transient.[6] Plotted in Figure 3.22 is the result, indicating that the loop relocks.

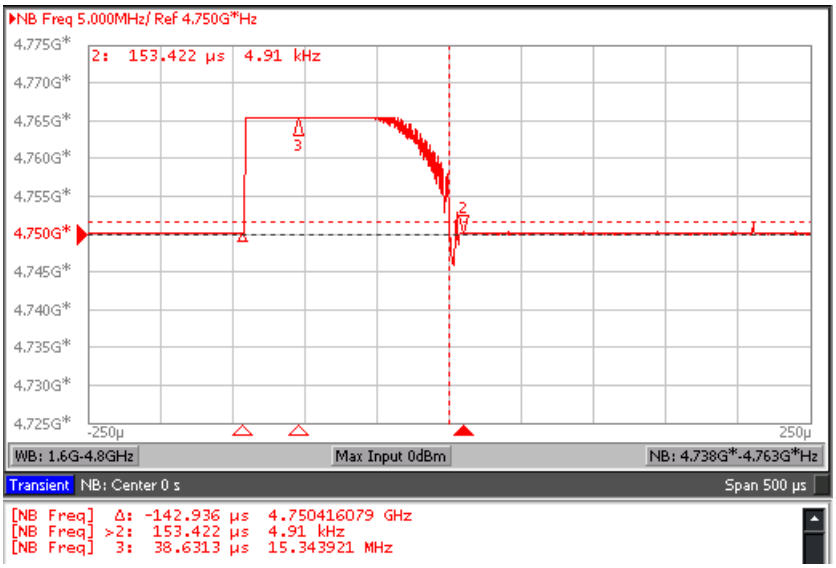


Figure 3.22: Measured PLL frequency transient response.

Table 3.1 presents the measured performance of our prototype and compares it to that of other PLLs (Figure 3.23) that have achieved sub-60-fs jitter values. The jitter is reduced by more than a factor of 2 and the FoM is improved by 4.1 dB.

[6]Due to this equipment's limitations, we precede it with an external ÷ 2 stage.

Table 3.1: Performance summary and comparison to prior art

	Zhang ISSCC 2019	Gong RFIC 2020	Mercandelli ISSCC 2020	Turker ISSCC 2018	This Work
Architecture	Sub–sampling PLL	Charge Sampling PLL	Single–Sampling PLL	Charge–pump based PLL	Double Sampling PLL
Ref. Freq.(MHz)	200	100	500	500	250
Freq. Range (GHz)	12 ~ 16	9.8 ~ 12.2	11.9 ~ 14.1	7.4 ~ 14	19
RMS Jitter (fs) Integ. range (MHz)	56.4 (0.001~100)	50.5 (0.001~100)	51.7 [2] (0.001~100)	53.6 (0.01~10)	20.3 (0.01~100)
Ref. Spur (dBc)	–64.6	–65.7	–73.5	–75.5	–66
Power (mW)	7.2	5	18	45	12
Area (mm^2)	0.234	0.13	0.16	0.45	0.06
Tech. (nm)	40	40	28	16	28
FoM[1] (dB)	–256.4	–258.9	–253.2	–248.9	–263
Crystal Osc. Power (mW)	N/A	150[3]	175[4]	N/A	170

1: $\text{FoM} = 10\log_{10}[(\frac{\text{Jitter}}{1\text{ s}})^2(\frac{\text{Power}}{1\text{ mW}})]$ 2: Integer–N Jitter

3: From datasheet of Taitien VLCU–type series

4: From private communication with author and datasheet of Crystek CCSO–914X–500

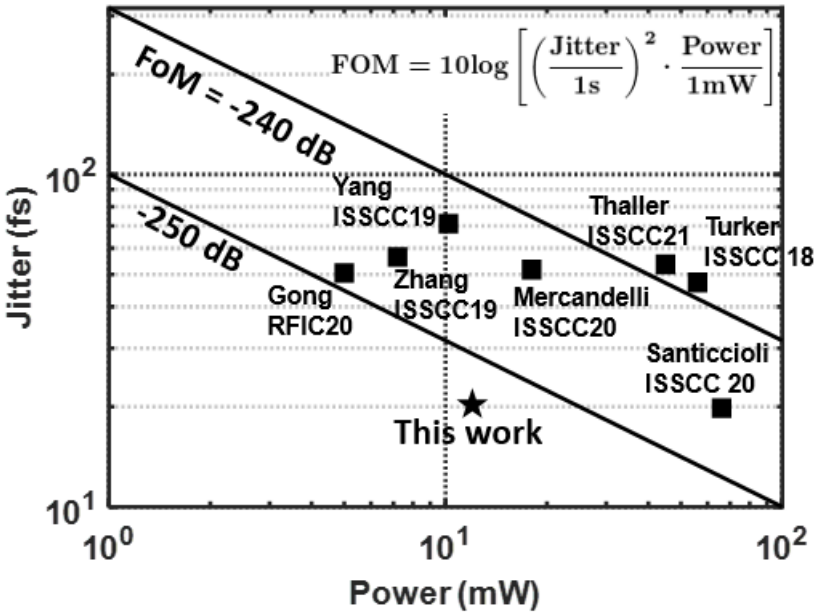


Figure 3.23: Comparison to the state-of-the-art low-jitter PLLs.

As explained in Chapter 2, the reference phase noise and frequency play a significant role in the performance of PLLs. For this reason, the crystal oscillator power consumption also becomes

problematic. According to our measurements, Crystek's CRBSCS-01-250 draws about 170 mW. Shown in Table 3.1 are the crystal oscillator power consumptions.

CHAPTER 4

A 56-GHz 23-mW Fractional-N PLL with 110-fs Jitter

This chapter proposes a 56-GHz fractional-N PLL that achieves an integrated jitter of 110 fs. This is accomplished through the use of a phase-domain FIR filter that filters out the $\Delta\Sigma$ noise. The power consumption of this PLL is 23 mW.

4.1 Design Challenges

Fractional-N synthesis generating a clock at the frequency of 56 GHz (Figure 4.1) faces two main challenges. The first challenge is that the speed of the multimodulus divider (MMD) is limited

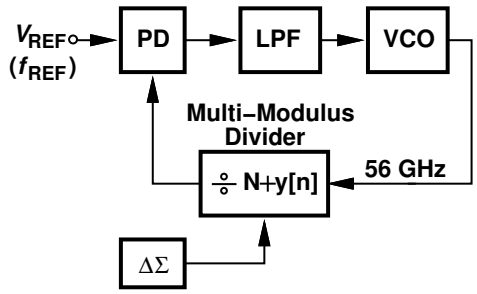


Figure 4.1: A general 56-GHz Fractional-N PLL.

below 20 GHz, which motives us to insert a chain of div-by-2 stages after the voltage-controlled oscillator (VCO). The second challenge is that the optimization of the PLL bandwidth faces a trade-off between the VCO phase noise and the $\Delta\Sigma$ quantization noise. A wideband PLL suppresses the VCO phase noise but the peaking of the $\Delta\Sigma$ noise worked against this premise. Therefore, the bandwidth-noise trade-off motivates us to reduce the $\Delta\Sigma$ noise by additional techniques.

Two general approaches to $\Delta\Sigma$ noise have been reported in the prior art. The first approach incorporates a digital-to-time converter (DTC) to cancel the quantization error of the DSM for fractional-N synthesis [8, 10, 16, 26, 29–32]. This method requires a calibration loop to adjust the gain of the DTC and assumes the DTC are linear enough to negligibly fold down the high-pass shaped $\Delta\Sigma$ noise. Various noise cancellation techniques have been proposed to achieve better performance, but they require stringent matching or complex calibration.

The second approach is to filter the $\Delta\Sigma$ noise before it reaches the VCO. In [33] a simple FIR filter is inserted between the phase detector (PD) and the frequency divider of the PLL to generate the delayed copies of the divider output. The filtering operation happens when a resistor-based network combines the copies to a single feedback signal with much less jitter. The following MSSF samples the output of the resistor network and controls the frequency of the VCO. The FIR-filtering method has two advantages: 1. The mismatch of the resistors (or other type of combination elements) only alters the frequency response of the FIR filter but does not introduce folding of the high-frequency $\Delta\Sigma$ noise, which eases the matching requirement. 2. The flip-flops in the FIR filter is clocked by the VCO output, generating delayed copies of the divider output without affecting the loop stability of the PLL. This FIR-filtering method affords a loop BW of around $f_{REF}/4$.

In this paper, we introduce a 56-GHz fractional-N PLL that incorporates the above-mentioned FIR-filter-based method that suppresses the $\Delta\Sigma$ noise. The FIR filter consists of 22 taps and a switched-current combination circuit with better linearity and less noise-folding than those of the resistor-based network. The FIR-filter provides 12-dB $\Delta\Sigma$ noise rejection at 10-MHz offset and offers a BW of 3 MHz.

4.2 Linearity analysis of the Phase-Domain FIR filter

In this section, we analyze the linearity of the FIR filter in the phase-domain.

4.2.1 Resistor-based FIR filter

In [33], XOR gates convert the phase error to a voltage signal and a resistor network performs the FIR filtering to the PD output. The coefficient of the FIR filter is determined by the value of the resistance. According to our analysis, despite of linear resistors, capacitors and switches, there is a nonlinearity issue in the phase domain with this implementation. We use a simple example to illustrate this point.

Figure 4.2(a) shows a simplified 2-tap resistor-based FIR filter. V_{F} represents the MMD output and $V_{\mathrm{F}\Delta}$ the delayed copy. As shown in Figure 4.2(b), the phase jump Δt_a is delayed by $\mathrm{T_{REF}}$ and

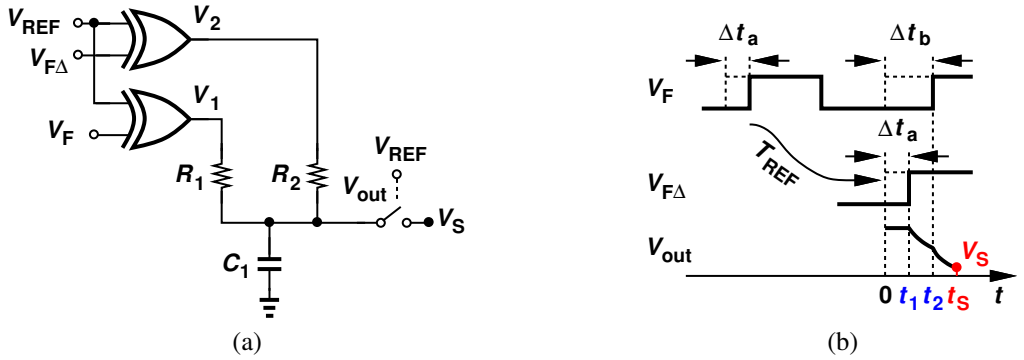


Figure 4.2: (a) Resistor-based 2-tap FIR summer, (b) input and response of the resistor-based FIR summer.

combined the next phase jump Δt_b. Initially, C_1 is charged to V_{DD}. From t_1 to t_2, one XOR PD discharges C_1 through R_2 and the other charges C_1 through R_1. The output resistance of the XORs is neglected to simplify the analysis. After t_2, both XOR PDs discharge C_1 and the output voltage, V_{out}, is sampled at t_s. With the help of superposition, the sampled output voltage is given by

$$V_s(t_s) = V_{DD}\left(\frac{R_2}{R_1+R_2}\cdot e^{-\frac{t_s-\Delta t_a}{\tau}} + \frac{R_1}{R_1+R_2}\cdot e^{-\frac{t_s-\Delta t_b}{\tau}}\right), \tag{4.1}$$

where $\tau = R_1R_2C_1/(R_1+R_2)$ is the time constant of the circuit. As shown in Eq. 4.1, the expression of V_s contains a linear combination of two exponential terms. If Δt_a and Δt_b represent the phase noise introduced by the $\Delta\Sigma$ modulator, the exponential action introduces nonlinearity

and applies *before* the FIR action. The nonlinearity distortion comes from two reasons. First, the charge delivered to the load capacitance, C_1, is not linear with respect to the each phase error because the current flowing through the the resistors changes with the output voltage, V_{out}. Second, the branches are never "tristated". For example, when R_2 discharges C_1 from t_1 to t_2, it is desirable to disconnect R_1 from C_1 to isolate V_{F} from charging C_1. Here we also give the expression of an N-tap resistor-based FIR filter:

$$V_s(t_s) = V_{DD} \sum_{k=1}^{N} \left(\frac{R_{||}}{R_k} \cdot e^{-\frac{t_s - \Delta t_k}{\tau}} \right), \tag{4.2}$$

where $R_{||} = \frac{1}{\sum_{k=1}^{N} \frac{1}{R_k}}$ is the equivalent output resistance of the resistor-based FIR filter.

4.2.2 Switched-current FIR filter

The linearity analysis of the resistor-based FIR filter in Sec 4.2.1 leads us to the idea of a switched-current FIR filter that achieves better linearity.

Figure 4.3(a) shows a simplified 2-tap resistor-based FIR filter. In this topology, V_{F} and $V_{\text{F}\Delta}$ control two current sources. C_1 begins with a zero initial condition. As illustrated in Figure 4.3(b), at $t = t_1$, $V_{\text{F}\Delta}$ turns on I_2 and V_{out} increases with a slope of I_2/C_1. At $t = t_2$, V_{F} turns on I_1 and

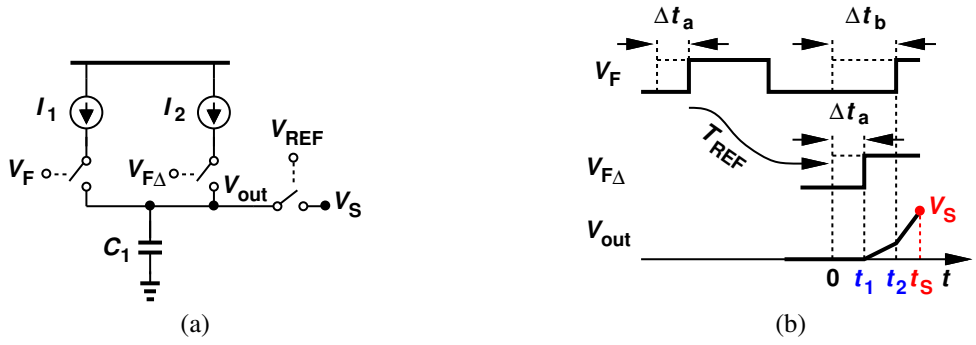


Figure 4.3: (a) A two-tap Switched-current FIR filter, (b) input and response of the switched-current FIR summer.

V_{out} increases with $(I_1 + I_2)/C_1$ because both I_1 and I_2 charges C_1. We derive the expression of

V_{out} after t_2:

$$V_{\text{out}}(t) = -\frac{I_1}{C_1} \cdot \Delta t_b - \frac{I_2}{C_1} \cdot \Delta t_a + \frac{I_1 + I_2}{C_1} \cdot t. \tag{4.3}$$

If we view Δt_b as $x(t)$ and Δt_a as $x(t - T_{\text{REF}})$, we observe that V_{out} provides a two-tap FIR response, with normalized filter coefficients $\alpha_1 = -I_1/(I_1 + I_2)$ and $\alpha_2 = -I_2/(I_1 + I_2)$. In order to perform phase comparison with the reference, we sample V_{out} by V_{REF} at $t = t_s$. The sampled voltage, V_s, is given by

$$V_s = \frac{I_1 + I_2}{C_1} \left[\alpha_1 \cdot x(t) + \alpha_2 \cdot x(t - T_{\text{REF}}) + t_s\right]. \tag{4.4}$$

Thus, V_s contains an integrated value from $t = 0$ to t_s representing the reference phase minus the a linear combination of two terms involving Δt_a and Δt_b. From Eq. (4.4), we conclude that the switched-current FIR exhibits no nonlinearity with ideal current sources. This is because in this case, we do tristate the current sources so that C_1 stores the charge that represents the phase difference between the reference clock and each feedback clock. We write the expression of $V_s(t_s)$ in the case of an N-tap FIR filter:

$$V_s(t_s) = \frac{\sum_{k=1}^{N} I_k}{C_1} \sum_{k=1}^{N} \alpha_k \cdot (t_s - t_k), \tag{4.5}$$

where $\alpha_k = \frac{I_k}{\sum_{k=1}^{N} I_k}$ is the normalized filter coefficient.

The foregoing analysis is based on the assumption of an ideal current source. However, in practice, MOSFETs have finite output impedance introduced by the channel-length modulation effect. In the case of the FIR filter, the current delivered by the current sources is no longer constant, but a function of the FIR filter output voltage (V_{out}). Let us again start with a simple case of a two-tap switched-current FIR filter with the output resistance associate with I_1 and I_2 denoted by R_1 and R_2 included (Figure 4.4). We note that the output resistance of a current branch is inversely proportional to its output current. Therefore, we have $I_1 \cdot R_1 = I_2 \cdot R_2 = (I_1 + I_2) \cdot R_{||}$, where $R_{||} = R_1 R_2/(R_1 + R_2)$. We redo the calculation of V_{out} for the 2-tap switched-current FIR filter with the input signal shown in Figure 4.3(b). Let us assume that C_1 begins with an zero initial

condition. At t_1, $V_{\mathrm{F}\Delta}$ turns on I_2 so both I_2 and R_2 charges C_1. The voltage of C_1 is given by

$$V_{\mathrm{out}}(t) = (V_{DD} + I_2 R_2)\left(1 - e^{-\frac{(t-\Delta t_a)}{R_2 C_1}}\right), \quad (\text{ for } t_1 < t < t_2\ ) \tag{4.6}$$

At t_2, V_{F} turns on I_1 and both two current sources, i.e., I_1, I_2, and two resistors, i.e., R_1, R_2, charge C_1. The expression of V_{out} is given by

$$V_{\mathrm{out}}(t) = (V_{DD} + I_1 R_1)\left(1 - e^{\frac{\frac{R_{||}}{R_2}\Delta t_a + \frac{R_{||}}{R_1}\Delta t_b - t}{R_{||} C_1}}\right). \quad (\text{ for } t_2 < t\ ) \tag{4.7}$$

By comparing Eq. 4.7 with Eq. 4.2, we note that one advantage of the proposed switched-current FIR filter over the resistor-based FIR is the nonlinearity from the exponential action applies after the FIR filtering action.

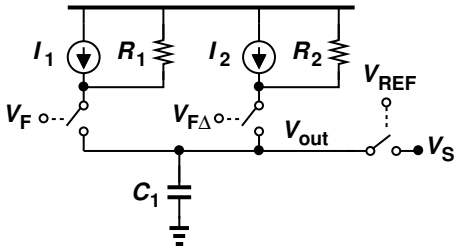


Figure 4.4: A two-tap switched-current FIR filter with finite output resistance.

4.3 Proposed PLL architecture

The proposed PLL architecture is shown in Figure 4.5. A switched-current FIR circuit acts as both a quantization noise filter and a phase detector, and is followed by a sampler, a Gm stage, a loop filter and a VCO. The Gm stage provides a gain of 30 dB at DC, relaxing the voltage compliance at the FIR filter output. The feedback path consists of a low-power, compact divide-by-8 circuit and an MMD driven by a 1-1-1 MASH $\Delta\Sigma$ modulator. Despite the limited speed of the 28nm CMOS devices, the PLL employs only in inductor (in the VCO) so as to occupy a small footprint. Here we need to answer two questions. First, how many taps do we need for the FIR filter? Second, do we need a $\div 8$ or $\div 4$ circuit between the VCO and the MMD?

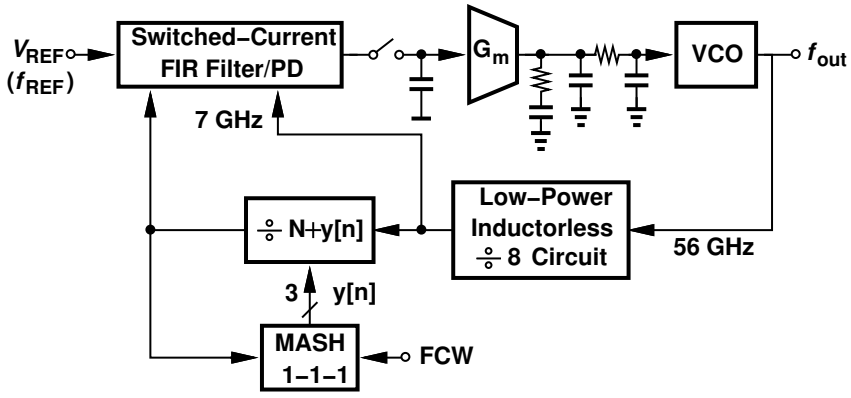


Figure 4.5: Proposed PLL architecture.

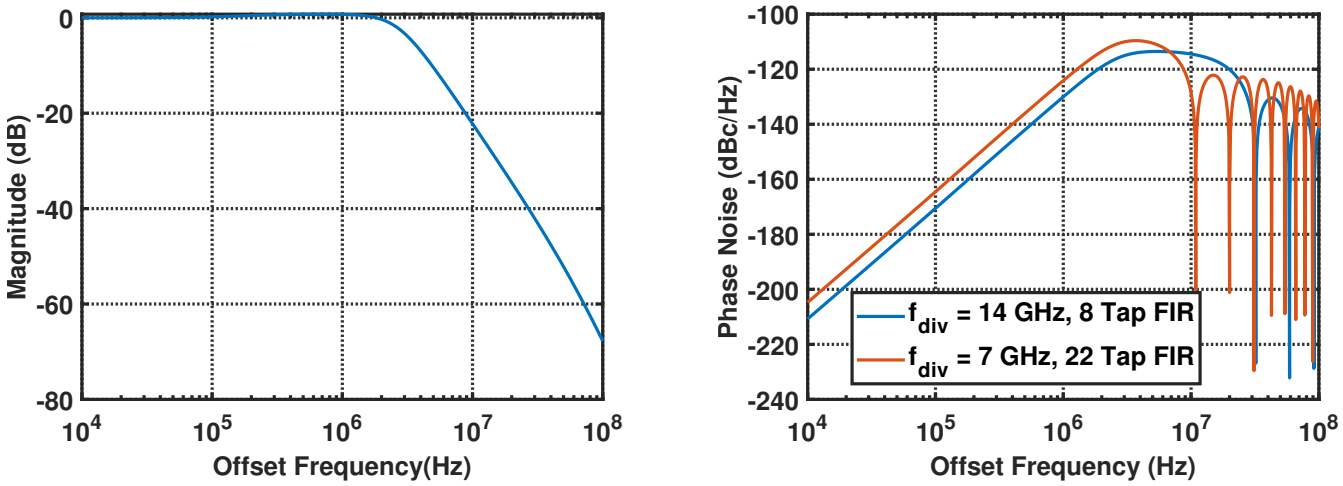
4.3.1 Divide ratio

As mentioned in Section 4.1, a divider needs to be inserted between the VCO and the MMD because of the limited speed of the latter. Here we compare two cases: a 56-GHz VCO followed by a divide-by-4 and then by a MMD running at 14 GHz vs the same VCO followed by a divide-by-8 and then by a MMD running at 7 GHz. Without an FIR filter, the phase noise at the PLL output introduced by the MASH 1-1-1 DSM [34] is

$$S_{\Phi_{\Delta\Sigma}} = \frac{N^2}{12 f_{REF}} \cdot |G(f)|^2 \left((2\pi)^2 \left(2sin(\pi \frac{f}{f_{REF}}) \right)^4 \right) \tag{4.8}$$

where N is the divide ratio of the divider in front of the MMD, $G(f)$ is the normalized closed-loop response of a PLL with a low-pass profile and a DC gain of one and plotted in Figure 4.6(a). We note that in the second case, the phase noise increases by 6 dB referred to the PLL output and the integrated jitter doubles, compared to that of the first case. In other words, the higher the frequency of the MMD input clock is, the less the DSM introduces phase noise to the PLL output. Here we assume the same BW in this comparison.

Now we include the FIR filter in both cases. In the first case, an 8-tap Chebyshev FIR filter is added to the output of the MMD. The integrated jitter from the $\Delta\Sigma$ noise is 31 fs_{rms}. In the second case, the length of the FIR filter needs to be increased to 22 taps to achieve the same amount of jitter. At the output of a PLL with the BW of 3 MHz, the DSM phase noise at the PLL output is



(a) (b)

Figure 4.6: (a) Normalized PLL closed-loop response and, (b) PLL output $\Delta\Sigma$ phase noise spectrum with $\div 4$ and $\div 8$ circuit.

shown in Figure 4.6(b).

The power consumption of clock buffer driving the flipflops in the FIR merits attention. The number of flipflops in the FIR is given by $f_{div}/f_{REF} \cdot (N_{taps} - 1)$, where N_{taps} is the number of the FIR taps. The power of the clock buffer can be estimated as $C_{CK} \cdot V_{DD}^2 \cdot f_{MMD}^2/f_{REF} \cdot (N_{taps} - 1)$, where C_{CK} is the capacitance of the clock input node for each flipflop and V_{DD} is the supply voltage of the clock buffer.

Here is the trade-off. If we use a $\div 8$ circuit, the FIR must be longer and hence presents more capacitance in its clock path, conversely with a $\div 4$, the FIR can be shorter but its clock frequency and the number of flipflops in each tap doubles. The power consumption of the flipflop clock path is given by $f_{\mathrm{div}}^2/f_{\mathrm{REF}} C_{\mathrm{CK}} V_{\mathrm{DD}}^2 (N_{\mathrm{tap}} - 1)$, where C_{CK} is the capacitance of the clock input of a flipflop in the FIR delay element and N_{tap} is the number of FIR taps. Based on the transistor level implementation of the FIR, we obtain these power number for the 2 cases ($\div 4$: 8 mW, $\div 8$: 6mW), which means the $\div 8$ option is preferable.

The MASH 1–1–1 modulator in Figure 4.5 employs a word length of 20 bits for a frequency resolution of 2 kHz at 56 GHz.

4.3.2 Switched-current FIR/PD Implementation

The complete FIR filter and phase detector is depicted in Figure 4.7(a). The core consists of 22 cascode current sources, with integer weighting factors k_1 to k_{22} chosen to create a Chebychev response having zeros at 11 MHz and its harmonics. In this work, the minimum k factor is 3 and maximum is 10. The coefficients of the FIR filter is given by $h_0 = h_{21} = 0.1, h_1 = h_{20} = 0.03, \ldots, h_{10} = h_{11} = 0.05$.[1] The proposed topology incorporates 21 delay elements and 22 NAND gates to apply FIR filtering to the phase difference between the reference and the MMD output. Among the available windows to implement the FIR filter, the Kaiser and the Chebyshev

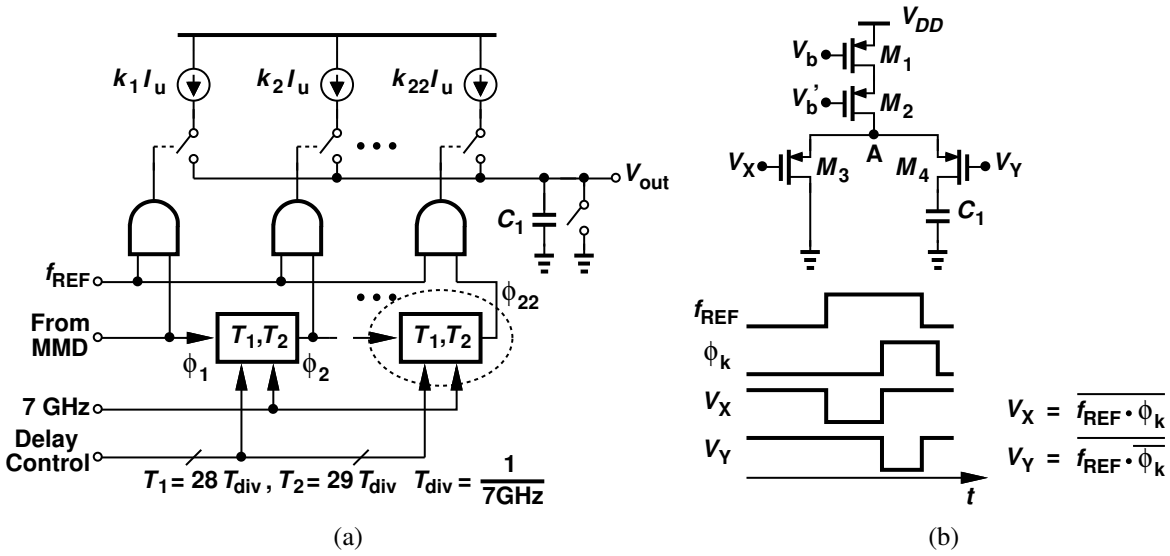


Figure 4.7: (a) Implementation of the 22-tap FIR/PD and, (b) waveforms of the FIR control signal.

filter provides the minimal $\Delta\Sigma$ jitter. Since the actual filter coefficients are realized by the ratio between integer multiple of current sources over the total number of current sources, the quantization error alters the filter coefficients and hence the response. We find that the minimum coefficient of the Kaiser window is relatively smaller (e.g. $h_1 = 0.015$ for $\beta = 2.9$) than that of the Chebyshev window and its response is more sensitive to coefficient quantization error. Thus we choose Chebyshev filter in this design.

[1] The coefficients of the FIR filter = $\frac{k_n}{\sum_{n=1}^{n=22} k_n}$.

The cascode switched-current cell employs a timing scheme (Figure 4.7(b)) that halves the power consumption and yet achieves high linearity. Initially, both M_3 and M_4 are off. Next, at the rising edge of f_{REF}, M_3 turns on, bringing V_{A} down to its desired value and finally, M_4 turns on and M_3 turns off at the rising edge of ϕ_k, allowing C_1 to charge.

In a typical analog layout, PMOS mismatches can be readily maintained below about 10%. We thus perform Monte-Carlo simulations to determine the variation of the $\Delta\Sigma$ jitter. Figure 4.8 shows the variation of the $\Delta\Sigma$ jitter at the PLL output. The FIR filter response is not sensitive to the current mismatches because the filter coefficient is determined by the ratio of the current in a tap over the total current in the FIR.

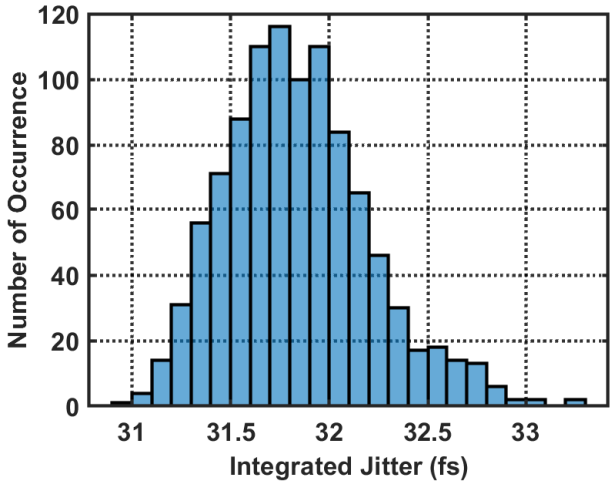
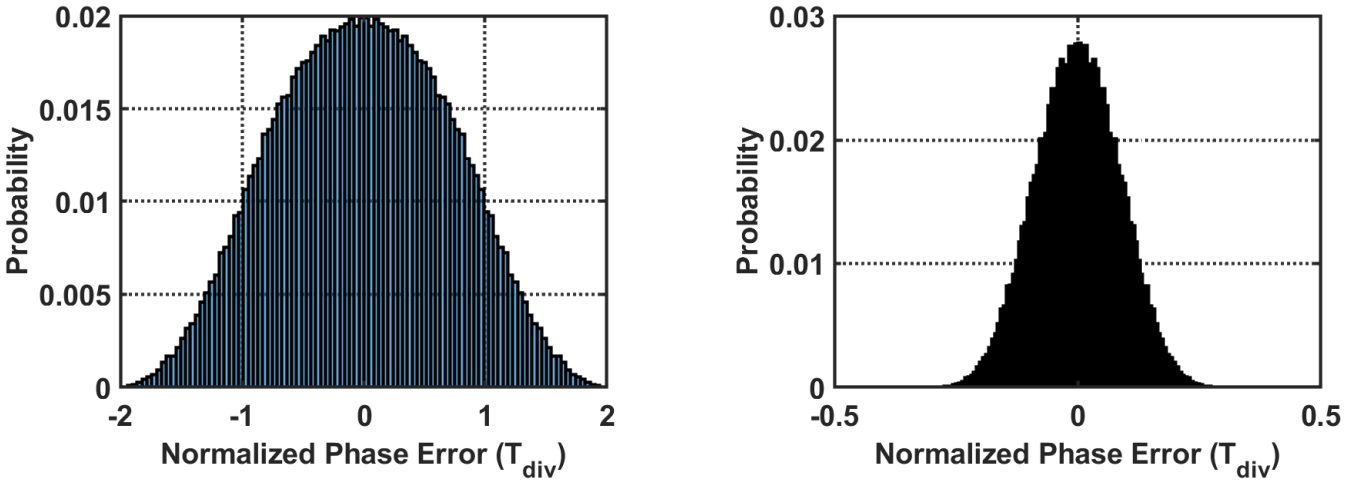


Figure 4.8: Monte-Carlo results showing variation of $\Delta\Sigma$ Jitter.

Another merit of the proposed FIR is that the probability density function of the phase error is narrowed from $\pm 2\,\mathrm{T}_{div}$ (Figure 4.9(a)) at the MMD output to $\pm 0.3\,\mathrm{T}_{div}$ (Figure 4.9(b)) equivalently at the FIR output.

4.3.3 Phase Detection

We analyze the phase noise the switched-current FIR filter/PD in the integer-N operation of the PLL for simplicity. In the integer-N mode, the output delay element, ϕ_j, is aligned with the MMD



(a) (b)

Figure 4.9: (a) $\Delta\Sigma$ phase error probability distribution without FIR filtering and, (b) with FIR filtering.

output, $V_{\rm F}$, because the delay of each tap is equal to $T_{\rm REF}$. Therefore, all of the current branches are turned on at the rising transition of $V_{\rm F}$. The current sources charge C_1 until the falling edge of $V_{\rm REF}$ arrives. The sampler samples $V_{\rm out}$ at the falling edge of $V_{\rm REF}$. As a result, the sampled voltage V_S is proportional to the phase difference between $V_{\rm REF}$ and $V_{\rm F}$. The slope of $V_{\rm out}$ is given by I_{tot}/C_1 and a phase deviation of $2\pi f_{REF}\Delta t$ translates to a sampled voltage of $\Delta t I_{tot}/C_1$. So the phase detection gain is

$$\begin{aligned} K_{PD} &= \frac{SR_{V_s}}{2\pi f_{REF}} \\ &= \frac{I_{tot}}{2\pi f_{REF} C_1}. \end{aligned} \tag{4.9}$$

The current source deposits noise to C_1 during the ramp-up time of $V_{\rm out}$, denoted by Δt, and this noise voltage is sampled by means of $V_{\rm REF}$. We note that the sampled noise voltage $V_{n,s}$ translates to the output phase noise of the PLL. The noise current $i_n(t)$ is integrated from 0 to Δt and sampled at the end of the integral. Similar to the phase noise analysis of an inverter [23], the spectrum of

the sampled noise voltage is written as

$$S_{V_n}(f) = \sum_{m=-\infty}^{m=+\infty} \frac{1}{C_1^2} \Delta t^2 \frac{\sin^2(\pi(f - mf_{REF})\Delta t)}{(\pi(f - mf_{REF})\Delta t)^2} S_{In}(f - mf_{REF}), \tag{4.10}$$

where $S_{In}(f)$ is the total spectrum of the noise current of the FIR filter and $f_{REF} = 1/T_{\rm REF}$ is the reference frequency. Referred to the input of the FIR by dividing $S_{Vn}(f)$ with K_{PD}^2, the phase noise of the FIR filter is

$$S_\phi(f) = \frac{4\pi^2 S_{Vn}(f) f_{REF}^2 C_1^2}{I_{tot}^2}. \tag{4.11}$$

If $S_{In}(f)$ is white, the phase noise is a sampled and shaped white noise with a spectrum given by

$$S_\phi(f) = 4\pi^2 \frac{\Delta t}{T_{\rm REF}} \frac{S_{In}(f)}{I_{tot}^2}. \tag{4.12}$$

We note that $S_{In}(f) = 4kT\gamma I_{tot}/(V_{GS} - |V_{TH}|)$, every doubling of the current improves the phase noise by 3 dB. For the flicker noise current, noise folding effect is neglected, the phase noise spectrum is

$$S_\phi(f) = 4\pi^2 \frac{\Delta t^2}{T_{\rm REF}^2} \frac{S_{1/f}(f)}{I_{tot}^2}. \tag{4.13}$$

One would reduce Δt to improve $S_\phi(f)$ by increasing the charging slope of $V_{\rm out}$. But the $\Delta\Sigma$ phase error applies a lower limit to Δt. When the PLL operates in the fractional-N mode, the instantaneous phase of $V_{\rm F}$ is modulated and the rising edge arrives earlier or later than it does in the integer-N mode. For a 1-1-1 MASH $\Delta\Sigma$ modulator, the phase error is with $[-2\,T_{\rm div}, +2\,T_{\rm div}]$. So the worst case happens when the rising edge of $V_{\rm F}$ arrives two $T_{\rm div}$ later than . The minimum Δt should guarantee the rising edge of $V_{\rm F}$ comes earlier than the falling edge of $V_{\rm REF}$.

4.3.4 PD Gain Limit

There are two factors limiting the slope of $V_{\rm out}$ and hence the PD gain. First, The actual current source has limited voltage headroom for the devices to operate in the saturation region. For the PMOS devices used in the current source, the voltage of C_1 should be lower than $V_{DD} - (V_{GS} - |V_{THP}|)$. Second, the charging time is limited by the spread of $\Delta\Sigma$ phase error. We explain this

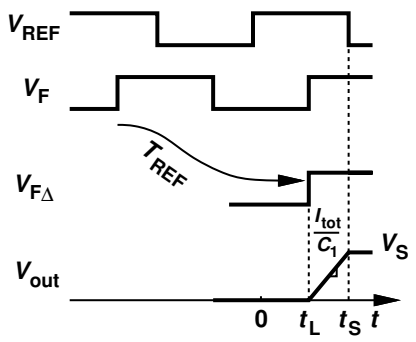


Figure 4.10: Switched-current FIR operation in the integer-N mode.

point in detail and start with the integer-N mode operation. In Figure 4.10, t_L represents the locking point of the PLL in the integer-N mode. At $t = t_L$, all the current branches are turned on and $V_{\rm out}$ increases at a rate of I_{tot}/C_1. At $t = ts$, all current branches are turned off. The time interval from t_L to t_S is called "charging time". In the fraction-N mode, the feedback clock, $\rm V_F$ and its delay copy, $\rm V_{F\Delta}$ are not aligned due to $\Delta\Sigma$ modulation. But we can imagine $\rm V_F$ and $\rm V_{F\Delta}$ moves around the locking point, t_L when the PLL is locked. From the distribution of $\Delta\Sigma$ phase error plotted in Figure 4.9(b), we can expect the maximum phase deviation of $\rm V_F$ (or $\rm V_{F\Delta}$) with respect to t_L to be $\pm 2T_{\rm div}$. Therefore, the charging time should be at least $\pm 2T_{\rm div}$ to make sure the all the current branches contribute to the charging of C_1 for proper FIR operation. From the analysis above, the voltage headroom and the charging time requirement together applies an upper limit on the slope and hence the PD gain.

4.3.5 Cascode current source

As discussed in Section 4.2.2, the output resistance of the current sources degrades the linearity of the switched-current FIR filter. Figure 4.11(a) plots the simulated I-V characteristics of two PMOS current sources delivering about 6.5 mA to its output node. The output resistance of a PMOS current source drops from 3.3 kΩ to 500 Ω (calculated at $V_{\rm out} = 0.5$ V) if the cascode device is removed. Figure 4.11(b) plots the simulated $\Delta\Sigma$ phase noise spectrum of a FIR filter with and without cascode devices. The cascode current source reduces the $\Delta\Sigma$ noise floor by 14

dB at 100 kHz offset and 10 dB at 1 MHz offset.

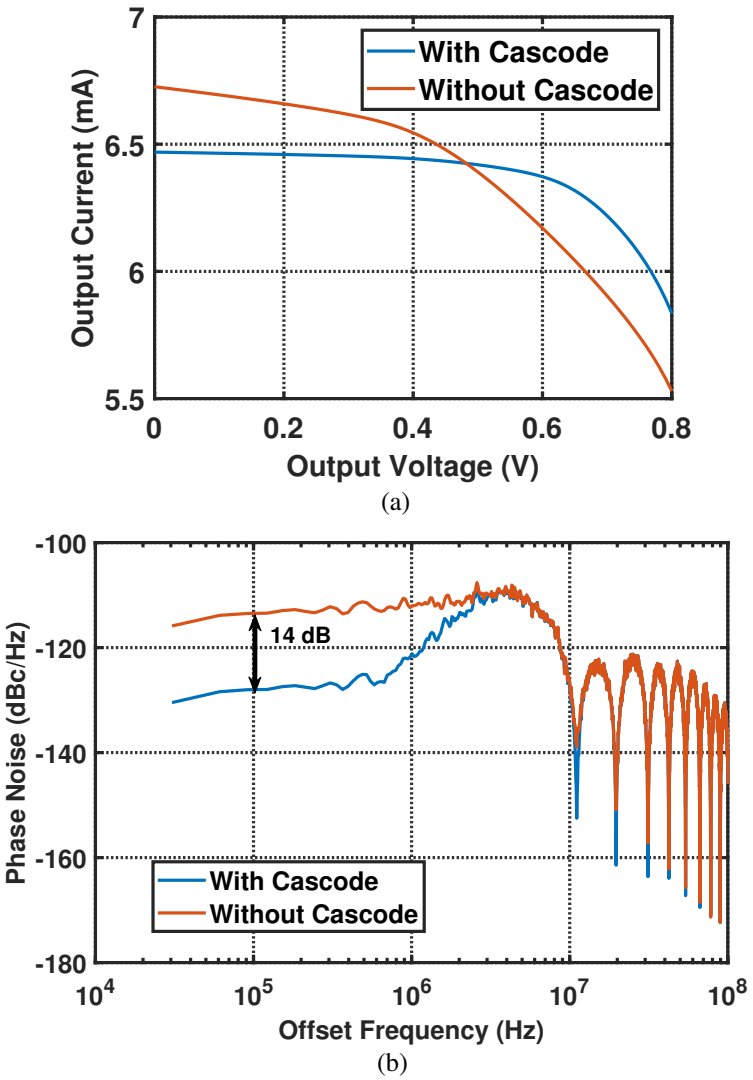


Figure 4.11: (a) I-V characteristic of a current unit with and without cascode and, (b) simulated $\Delta\Sigma$ phase noise spectrum of switched-current FIR with and without cascode.

4.3.6 Binary Delay Line

In the delay element of the FIR filter, we can place a chain of 28 TSPC flipflops in each delay stage clocked by the $\div 8$ circuit, providing discrete values equal to integer multiples of T_{div}.

With this clocking method, ϕ_1 to ϕ_{22} all carry the feedback information for the PLL to lock [33]. However, this approach leads to phase error accumulation. As illustrated in Figure 4.12(a), the delay from ϕ_1 to ϕ_2 is equal $\frac{N}{N+\alpha} \cdot T_{\mathrm{REF}}$ and not equal to T_{REF}, where α is the frequency command word (FCW). Therefore, this negative phase error accumulates, creating a large error by the time we get ϕ_{22}. As analyzed in Section 4.3.3, the phase detection gain is inversely proportional to the charging time of the FIR filter, the lower bound of which is limited by the distribution of the $\Delta\Sigma$ phase error. Now, the phase error accumulation further increases the charging time and reduces the phase detection gain for proper FIR operation. As a result, the phase noise contribution from the FIR and the following Gm stage increases.

To resolve this issue, the delay elements assume a binary value of either $T_1 = 28T_{\mathrm{div}}$ or $T_2 = 29T_{\mathrm{div}}$ so as to create a tight bound for this error. Programmed individually in conjunction with α, the delay of Stage j is set according to the following rules: if the accumulated error from Stage 1 to Stage j is less than T_{div}, then $T_1 = 28T_{\mathrm{div}}$ is selected; otherwise, $T_2 = 29T_{\mathrm{div}}$ is used. The accumulated error is predicted by $(j-1)\alpha T_{\mathrm{div}}$. As shown by the waveforms in Figure 4.12(b), the delay from ϕ_2 to ϕ_3 is compensated by one more T_{div}. In this way, the last FIR phase, ϕ_{22}, experiences a difference of only about T_{div}, with respect to the others.

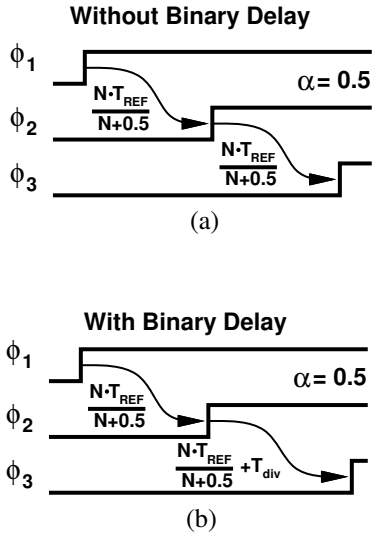


Figure 4.12: (a) FIR delay output without binary delay, and (b) FIR delay output without binary delay.

The flipflops in the FIR delay elements employ a true single-phase clock (TSPC) structure (Figure 4.13). The extracted total capacitance of the clock input is 1.4 fF for a single flipflop. In this design, we employ 609 flipflops. The clock path is driven by the $\div 8$ output at 7 GHz and consumes a power of 6 mW.

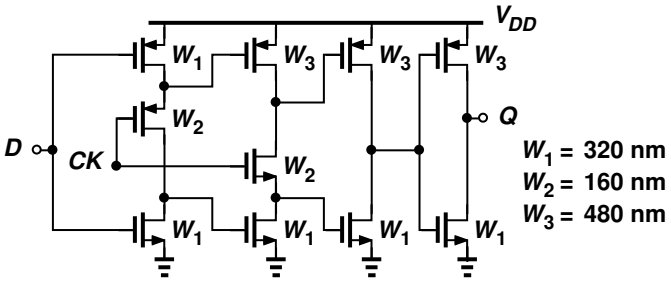
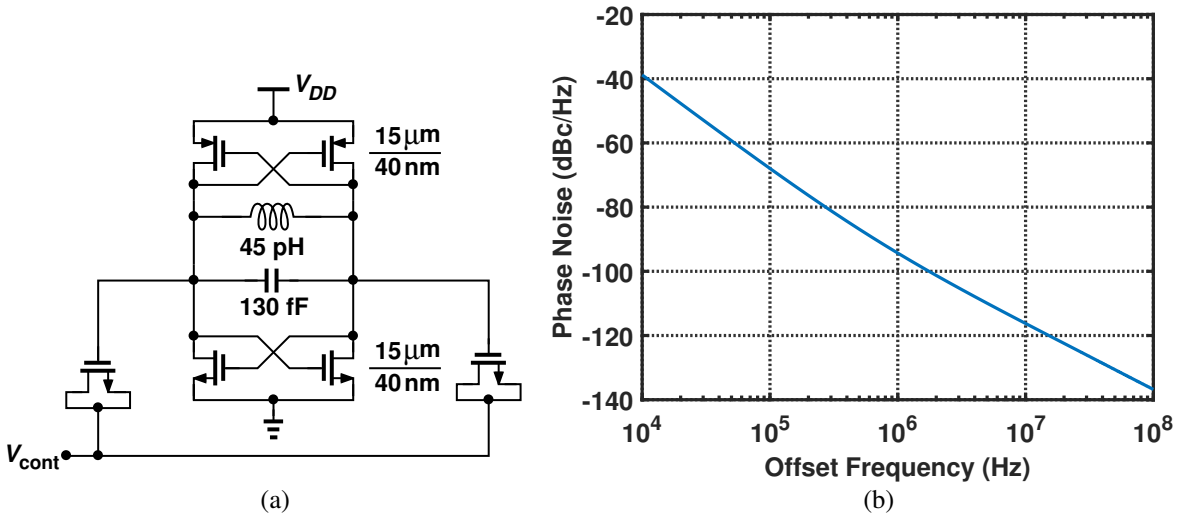


Figure 4.13: TSPC flip-flop.

4.3.7 VCO and ÷ 8 circuit[2]

Shown in Figure 4.14, the VCO employs a complementary LC topology. Due to the lack of ultra-thick-metal layers, the 45-pH inductor is realized as two metal-8 and metal-9 octagons in parallel. The quality factor of the tank is around 10, yielding the simulated phase noise profile shown in Figure 4.14(b) for a power consumption of 7.2 mW.

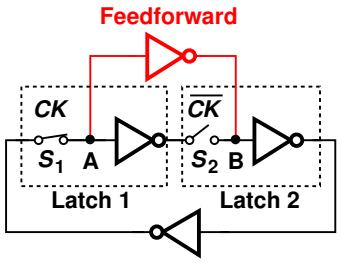
The $\div 8$ circuit between the VCO and the MMD can potentially consume high power and a large area if it employs inductors [35, 36]. We use a $\div 8$ topology that significantly reduces both [37]. As shown in Figure 4.15(a), the circuit is based on two dynamic latches and a third inverter in the feedback path for proper toggling. The performance is dramatically improved by introducing a feed-forward path from A to B so that the signal arrives at the latter before S_2 turns on. Proper scaling of this path with respect to the main inverters allows the upper end of the lock range to be extended, with some limitation on the lower end. As plotted in Figure 4.15(b), the feedforward path raises the divider's maximum speed from 55 GHz to 68 GHz while imposing a lower end of 43 GHz. This $\div 2$ stage draws 1.8 mW at 56 GHz.



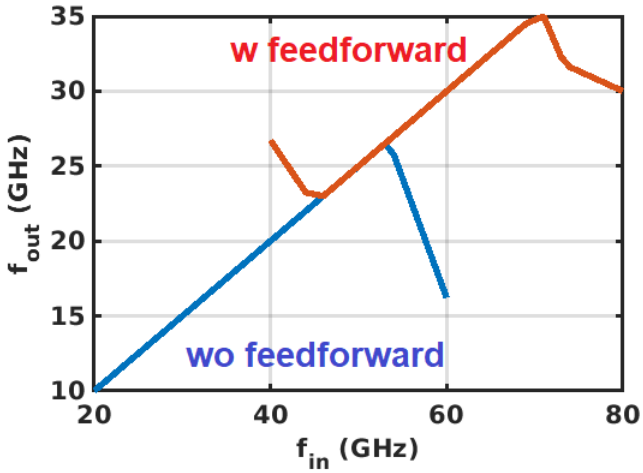
(a) (b)

Figure 4.14: (a) VCO implementations, and (b) its simulated phase noise.

[2]The $\div 2$ circuit is proposed and designed by Onur Memioglu. The rest of the PLL is designed by the author of this dissertation.



(a)



(b)

Figure 4.15: (a) $\div 2$ circuit with feedforward, and (b) its simulated frequency range.

4.4 Experimental Results

The proposed PLL has been fabricated in 28-nm CMOS technology. Figure 4.16 shows a photograph of the die, where the active area measures approximately $540\,\mu\text{m} \times 290\,\mu\text{m}$. The prototype consumes 23 mW: 11 mW in the FIR filter, 7 mW in the VCO, 3.1 mW in the $\div 8$ stage, 1 mW in the multi-modulus divider, 0.5 mW in the reference buffer, and 0.4 mW in the $\Delta\Sigma$ modulator and is supplied at 1 V. The external 250-MHz reference is provided by a low-noise crystal oscillator from Crystek corporation.

For ease of measurement, the output of the $\div 8$ circuit following the VCO is used for testing. Fig. 4.17 shows the measured $\div 8$ output spectrum. The fractional spur at 2 MHz offset has a level

of -66 dBc, which translates to -48 dBc at the VCO output and hence 16 fs of rms deterministic jitter. Fortunately, with receive clock and data recovery (CDR) bandwidths of tens of megahertz [38, 39] or above 100 megahertz [25, 40], such low-frequency spurs are rejected. Figure 4.18 plots the fractional spur levels as the FCW varies from 0.004 to 0.06 and the offset frequency varies from 1 MHz to 15 MHz.

Table 4.1 presents the measured performance of our prototype and compares it to that of other 60 GHz and 30 GHz fractional-N PLLs. With a power consumption of 23 mW and a jitter of 110 fs, we observe a nearly twofold reduction in jitter, an 8.3 dB improvement in the FoM, and a more than threefold reduction in area.

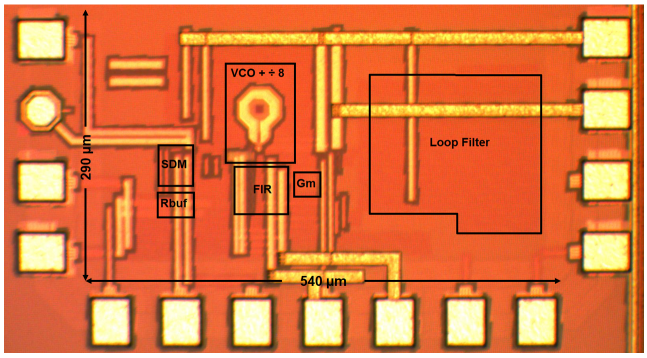


Figure 4.16: Die photograph.

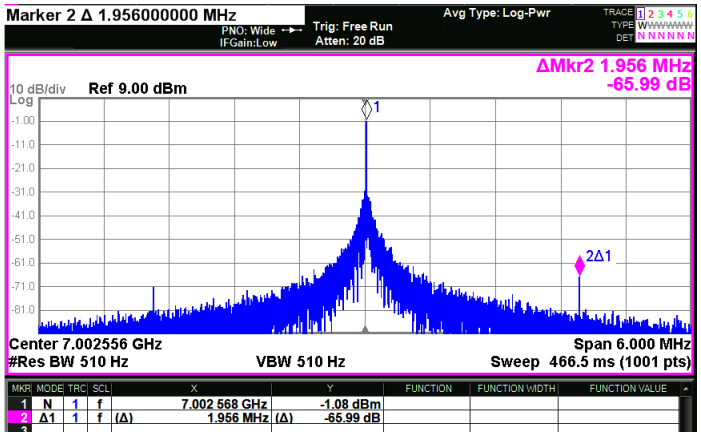


Figure 4.17: Measured PLL output spectrum.

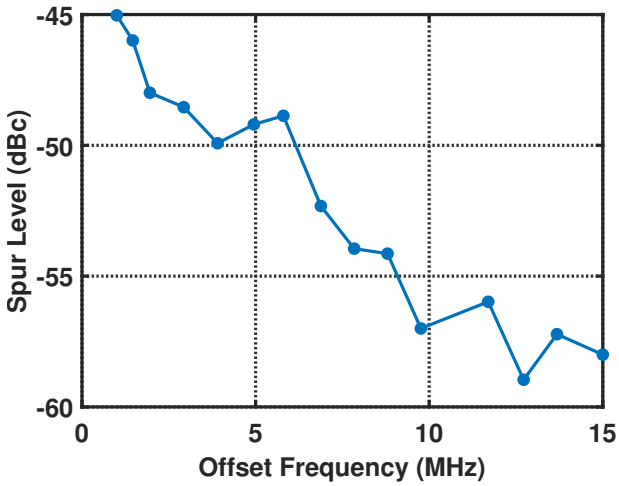


Figure 4.18: Measured PLL fractional spur levels.

Table 4.1: Performance summary and comparison to prior art

	Wu ISSCC 2013	Grimaldi ISSCC 2014	Hussein ISSCC 2017	Zong JSSC 2019	This Work
Freq. Range (GHz)	56.4~63.4	50.2~66.5	30.6~34.2	57.5~67.2	52.3~56.8
RMS Jitter (fs) Integ. range (MHz)	522.9 (0.01~10)	223 (0.001~40)	197.6 (0.001~10)	213 (0.01~30)	110 (0.01~40)
Frac. Spur (dBc)	N/A	–68	–42.2	–38	–48
Ref. Spur (dBc)	–74	–N/A	N/A	–65	–50
Ref. Freq.(MHz)	100	100	100	100	250
Tech. (nm)	65	65	65	28	28
Power (mW)	40	46	35	31	23
Area (mm^2)	0.48	0.45	0.55	0.38	0.1
FoM[1] (dB)	–229.6	–236.4	–238.6	–237.2	–245.5

1: $\text{FoM} = 10\log_{10}[(\frac{\text{Jitter}}{1\text{ s}})^2(\frac{\text{Power}}{1\text{ mW}})]$

CHAPTER 5

Conclusion

In this dissertation, we demonstrate design techniques for both integer-N and fractional-N high-speed PLLs for wireline and wireless applications. The crystal oscillator, the reference buffer, and the VCO become the main contributors for low-jitter integer-N PLL design. We introduce a new phase detector and a self-retimed frequency divider that ease the trade-offs in PLLs. We also propose a novel current-mode FIR filter to avoid phase and frequency detectors (PFDs) and charge pumps and to suppress the DSM quantization noise with negligible noise folding for low-jitter fractional-N PLLs. To provide a compact solution suited to multi-lane systems, the PLL also incorporates a low-power, inductorless $\div 8$ circuit.

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