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High Resolution Radiometer Electronics

Author

Ramos, Ian Howard

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High Resolution Radiometer Electronics

By

IAN HOWARD RAMOS
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Approved:

Neville C. Luhmann Jr., Chair

Anh-Vu Pham

Omeed Momeni

Committee in Charge

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Abstract

A high-resolution millimeter wave radiometer with 16 channels spaced 160 MHz apart is designed in KiCAD (an open-source PCB CAD program), fabricated, and characterized. The radiometer is intended for use in an electron cyclotron emission imaging system in which millimeter-wave radiation is emitted from a plasma and then down-converted in the radiometer to lower frequency radiation in the 3.0-5.5 GHz range. The radiometer electronic system consists of three circuit boards. The first is a radio frequency (RF) board that gathers the input signal and divides into 16 parts each of which covers a different portion of the input RF spectrum down-converted into intermediate frequency (IF) signals. The second is the IF board where its purpose is to take the 16 individual IF signals from the RF board and rectify them with a detector and then amplify the detector outputs. Each input IF signal is amplified, low-pass filtered (thereby fixing the RF/IF bandwidth of the channel), rectified, amplified once more, and low-pass filtered (thereby fixing the video bandwidth of the channel). The third board is the local oscillator (LO) board which houses the 16 local oscillators needed by the RF board for down-conversion. The boards were tested and installed together with instruments such as a function/frequency generator, attenuator, oscilloscope, multimeter, spectrum analyzer, and a power supply. The necessary equipment was used to measure factors such as dBm peaks and DC voltage to interpret signals due to frequency and attenuation. As a result, the radiometer was found to function suitably based on previous research as well as more channels and less frequency spacing. The research proposes further study on including more frequency channels and assembling the components and test setup in different ways.

Acknowledgements

First off, I would like to thank my major advisor, Professor Neville Luhmann, for his strong support during my graduate study and research at UC Davis. His enthusiasm and dedication have motivated me, and I feel much appreciated to be a part of his group and lab. I would also like to thank Dr. Calvin Domier for numerous helpful discussions and experimental support in the laboratory. With him, I have benefited and learned so much from his knowledge and carefulness throughout my research, design, testing, and further discussions. Next, I want to show my appreciation to Ms. Lynette Lombardo for her great and efficient work on helping me with important paperwork. Lastly, I greatly appreciate Professor Anh-Vu Pham and Professor Omeed Momeni for their patience and being a part of my thesis committee.

Table of Contents

Abstract ii

Acknowledgements iii

Chapter 1: Introduction and Motivation 1

1.1 Principles of Electron Cyclotron Emission Imaging (ECEI) 1

1.2 Motivation for High Resolution ECEI 4

1.3 KiCAD - Schematic Capture & PCB Design Software 6

1.4 Thesis Overview 7

Chapter 2: ECEI System Background 7

Chapter 3: Detectors and Detector Circuits 14

3.1 Types of Diode Detectors 14

3.2 Types of Detector Circuits 17

3.3 Detector Test Circuit Designs 20

3.4 Detector Test Circuit Measurements 25

Chapter 4: IF Board 33

4.1 Schematic Layout 33

4.2 PCB Layout 38

Chapter 5: RF Board 44

5.1 Schematic Layout 44

5.2 PCB Layout 48

Chapter 6: LO Board 50

6.1 Schematic Layout 50

6.2 PCB Layout 55

Chapter 7: Test Procedure and Results 57

7.1 Testing Board 57

7.1.1 Schematic/Design in KiCAD 57

7.1.2 PCB Layout 59

7.2 IF Board Measurements 62

7.3 RF Board Measurements 67

7.4 LO Board Measurements 72

7.5 Full System Measurements 76

Chapter 8: Final Remarks 80

8.1 Discussion and Summary 80

8.2 Future Work 82

References 84

Chapter 1: Introduction and Motivation

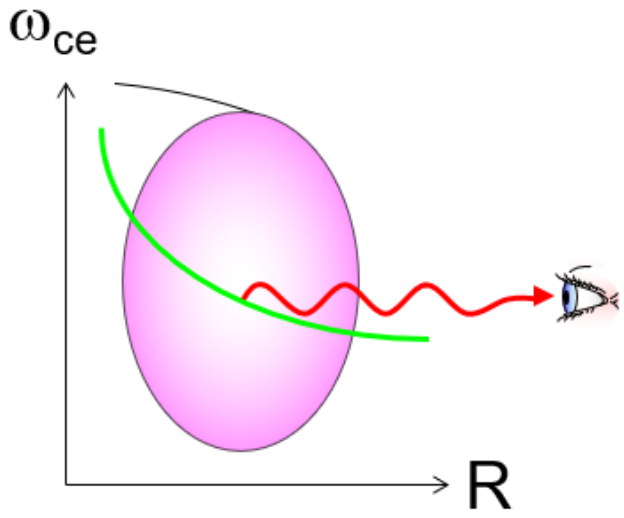
1.1 Principles of Electron Cyclotron Emission Imaging (ECEI)

Electron Cyclotron Emission Imaging (ECEI) is a passive diagnostic, collecting the radiation emitted by free electrons orbiting about magnetic field lines. The ECEI instrument also characterizes plasma instabilities. The imaging of the electron cyclotron radiation provides insight into the spatial and temporal behavior of electron temperature fluctuations and instabilities, providing a powerful diagnostic for investigations into basic plasma physics and nuclear fusion reactor operation. Plasma consists of charged particles, neutrals, and fields exhibiting collective effects; it is subject to electromagnetic (EM) wave radiation. ECE imaging signifies a major advancement in diagnostic techniques for magnetic confinement fusion. It relies on the passive acquisition of millimeter wave radiation and therefore requires no coupling to illumination sources or energetic particle beams, and achieves excellent signal to noise resolution and video bandwidth. Moreover, the measurement is localized, simplifying the interpretation of diagnostic data and resulting in a unique solution which represents the evolution of electron plasma temperature in space and time [2].

The University of California, Davis has pioneered the development of ECEI systems which are able to remotely measure and image plasma electron temperature and its fluctuations with high spatial and temporal resolution onto a 1-D detector array (receiver) by detecting the intensity of the electron cyclotron radiation emission from the plasma [3]. Another important engineering aspect of ECEI is in the optical coupling of radiation to the receiver antenna array where boundary conditions for an ECEI optical system are determined by evaluating the access constraints for the vacuum vessel and assuming a 1:1 magnification factor with parallel rays and beams that fill the window aperture as much as possible [2].

ECEI collects broadband blackbody radiation in the millimeter wave region on each element of the imaging antenna array, which is subsequently separated by an appropriate frequency spacing for post-processing to form a 2-D temperature image [3]. Additionally, the ECE diagnostics operate in the region where the plasma is optically thick which means the plasma is in a blackbody state [1] in which the radiation intensity is proportional to the electron temperature. In a magnetized plasma, the gyro motion of electrons trapped on magnetic field lines emits radiation at harmonics of the electron cyclotron frequency $\omega_{ce} = eB/\gamma m_e$ plus the harmonics. In a tokamak, the toroidal magnetic field, and hence the cyclotron frequency, is proportional to 1/R. For a horizontal chord viewing the plasma, there is now a 1:1 mapping between the emission frequency and the emission location as a result of this 1/R frequency scaling as illustrated in Fig. 1.1.

Fig. 1.1: The graph displays the one-to-one mapping between frequency and radial position where ω_{ce} is proportional to 1/B and 1/R.



ECEI acquires signals for data by following a two-stage down-conversion process (see Fig. 1.2) where the signal is down-converted once, amplified, divided into multiple channels with each

of the subdivided sections down-converted a second time with the resultant signals amplified, converted into DC voltages using detectors, and finally video amplified before digitization. Illustrated in Fig. 1.2, this second down-conversion process involves dividing the RF signal into 8 parts and fed to frequency mixers pumped by 2.4-8.9 GHz LO signals spaced from 600 or 900 MHz apart [1]. The addition of sharp cut-off low pass filters between the mixers and detectors converts the highly overlapping frequency coverage illustrated in Fig. 1.3 into the near-optimally separated frequency bands of Fig. 1.4.

Fig. 1.2: Two-Stage Down-Conversion Process Separating 8 RF Signals with 2.4-8.9 GHz LO Signals Spaced 600 or 900 MHz

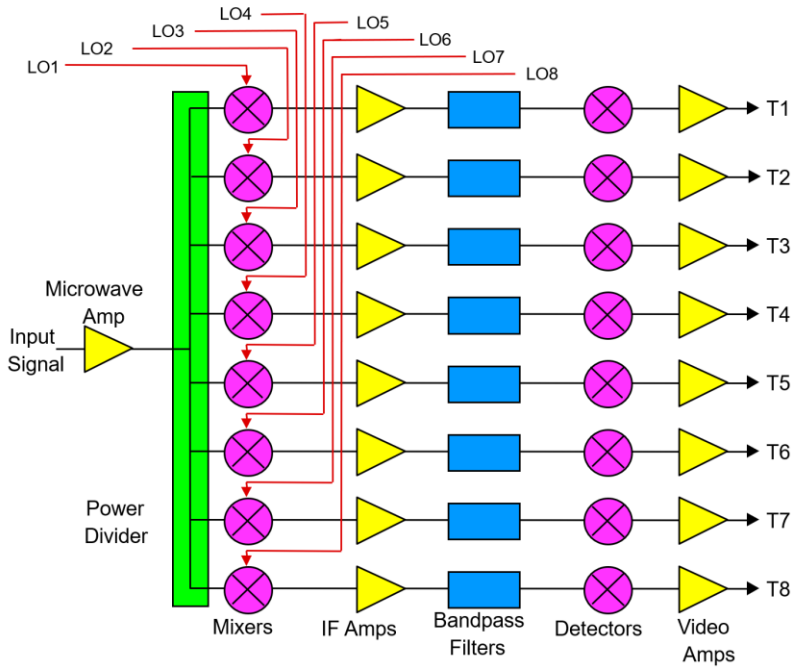


Fig. 1.3: Frequency versus Voltage without Low Pass Filters

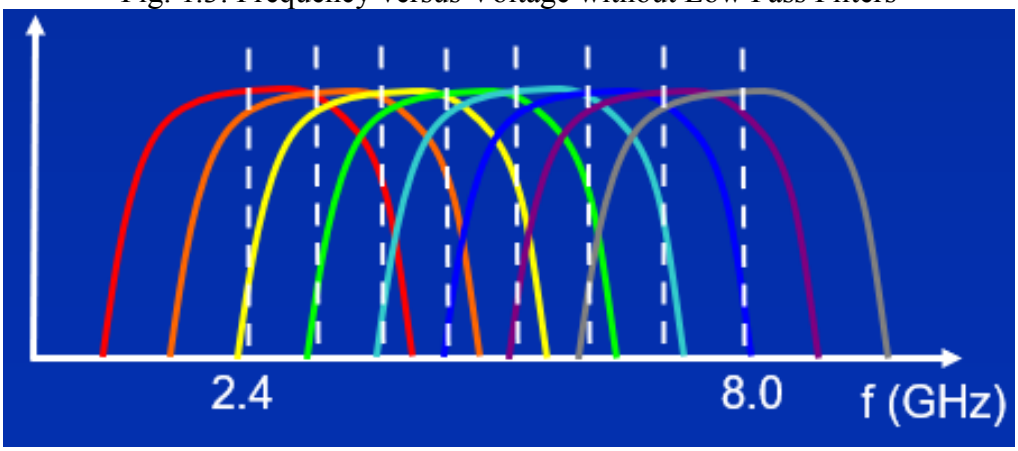
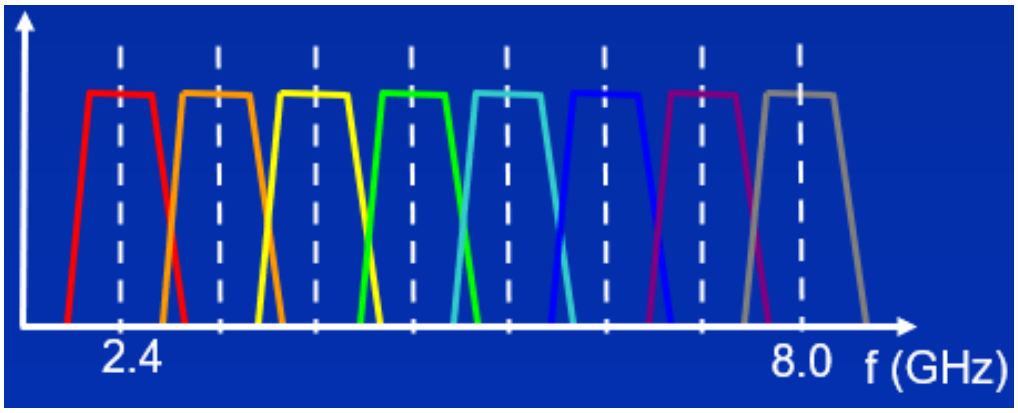


Fig. 1.4: The next figure shows the frequency versus voltage with low pass filters where there is reduction of radial spot size and provides sharp band edges for cross correlation.



1.2 Motivation for High Resolution ECEI

The first ECEI system was a 1-dimensional system developed at UC Davis in 1995 and installed on the TEXT-U tokamak in the University of Texas at Austin [6]. This 16x1 system had 16 vertically separated channels acquiring data at just one emission frequency. This was followed by 16x1 systems on the Rijnhuizen Tokamak Project (RTP) [7] in the Netherlands in 1997 and on the Torus Experiment for Technology Oriented Research (TEXTOR) tokamak in Germany in 2001 [6].

The first 2-D system was a 16x8 system for TEXTOR in 2004, which was later transferred to the Hefei Tokamak (HT-7) in China in 2009 [8]. This had channels spaced 500 MHz apart. This

was supplanted by a similar system in which the LO sources for the individual RF boards were placed directly on each RF board as opposed to being placed on a separate LO board and connected via low-loss cabling. The biggest advantage of this new arrangement was to make each ECEI module (consisting of an RF board and a companion IF board within a single enclosure box) extremely easy to remove/replace/install without having to deal with all of the individual LO cables. All ECEI systems developed since this time, while they may differ in terms of the receiving antenna, employ back-end electronics which all follow the same basic architecture as the second TEXTOR ECEI embedding LO sources on each RF board. The frequency spacing between channels varies from 600 MHz to 900 MHz. Strong interest has been expressed recently about developing the RF bandwidths of each channel that are generally set smaller than the frequency spacing, with narrower bandwidths leading to higher resolutions, albeit at the cost of higher black body noise (which scales as 1/bandwidth).

The Wendelstein 7-X (W7-X) is a stellarator in Greifswald, Germany by the Max Planck Institute for Plasma Physics (IPP). The name refers to the mountain called Wendelstein in Bavaria decided at the end of the 1950s, referencing the preceding project from Princeton University from the name Project Matterhorn. The stellarator will employ ECEI systems from the Davis Millimeter Research Center (DMRC) at UC Davis. The nominal magnetic field of W7-X is 3 Tesla (30,000 G) with a major plasma radius of 5.5 meters and as discussed, $B \sim 1/R$. The magnetic field geometry of a stellarator is more complicated than that of a tokamak, but it does have some tokamak-like ports in which the field drops off monotonically with radius much like a tokamak.

The higher resolution radiometer for the W7-X ECEI system is intended to be a proof-of-principle module which can explore what new physics can be obtained with the higher frequency resolution (which corresponds to a higher radial resolution on the device). The goal is to generate

high resolution 16-frequency detection electronics modules with an input frequency range of 3.0 to 5.5 GHz with channels spaced 160 MHz apart and channel bandwidths of 150-155 MHz. With a nominal array of 10 vertical elements, this would generate time-resolved 10x16 electron temperature images of a subset of the W7-X plasma. Although not needed for the prototype high-resolution boards, they should be compatible with installation into well-shielded enclosure boxes as in the J-TEXT ECEI system. The J-TEXT system in Wuhan, China is a representation of all these systems which will be discussed in further detail in the next chapter.

1.3 KiCAD - Schematic Capture & PCB Design Software

KiCAD is a free and open source software suite for Electronic Design Automation (EDA). The programs handle Schematic Capture integrated circuit simulation, Printed Circuit Board (PCB) Layout, 3D rendering, and plotting/data export with Gerber and IPC-2581 output. The suite runs on Windows, Linux, and macOS and is licensed under GNU GPL v3. The goal of the KiCAD project is to provide the best possible cross platform electronics design application for professional electronics designers [10].

The benefits of using KiCAD is that it has perfect workflows, a clean interface, customizable hotkeys, and great toolkits. In addition, it has an excellent project manager and users will also be able to use git to interface with it. The tools present that include Symbol Editor, Schematic Editor, PCB Editor, Image Converter, Gerber View, and the Footprint Editor can all be found under one specific tool and in an environment that is integrated. This means that when there is a change in a specific file, i.e. the Schematic, it helps in updating the data in the other project files automatically. It features a large and very good library that has great benefits when designing the PCB. Furthermore, it has a user-friendly interface for both the professionals and the beginners. Also, multilayer PCB design can be done very efficiently.

The Schematic Editor of KiCAD supports virtually everything from the very basic schematic to the complex designs having about hundreds of sheets. With this, there is opportunity to create personalized symbols, or make use of the KiCAD EDA official library. After this, there is the ability to make use of the electrical rules checker in verifying design. The PCB Editor is self-explanatory and made the entire process of printed circuit board designs come easy. Hence, it is strong enough to serve complex and modern designs and with its improved visualization, selection tools, and strong interactive router, there is ability to make the layout tasks much easier.

1.4 Thesis Overview

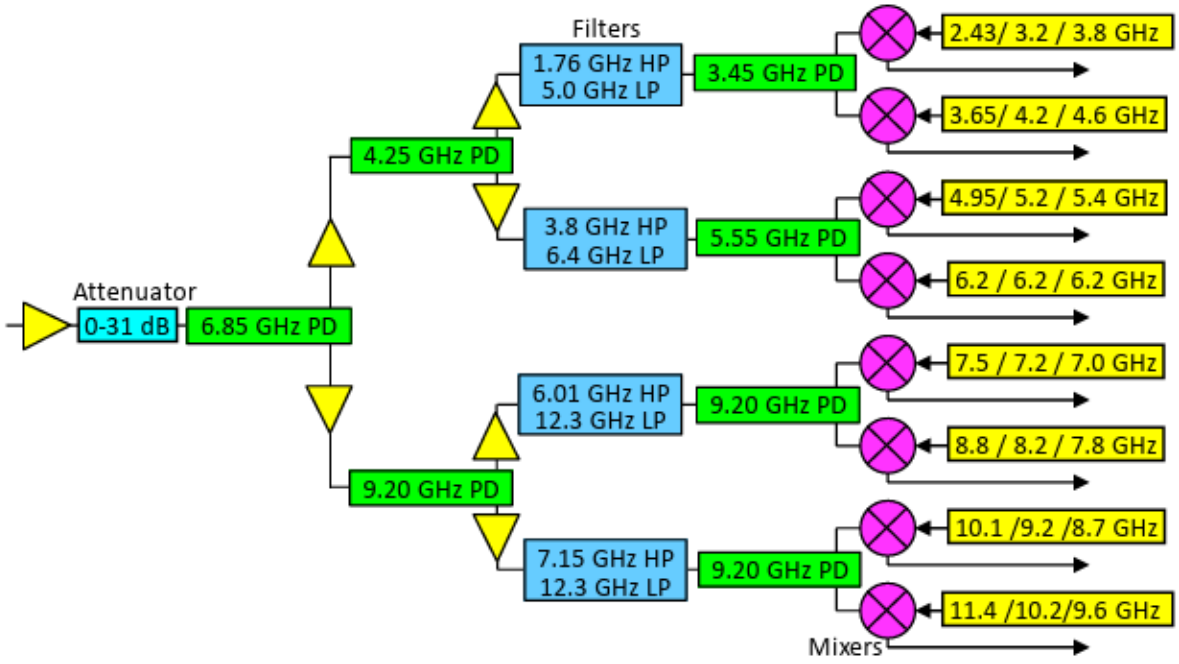
The goal of this thesis, as mentioned briefly in Section 1.3, is to develop a prototype high-resolution ECEI module. PCB boards will be developed using KiCAD. Chapter 2 describes the schematic, configuration, and results of the J-TEXT ECEI system while Chapter 3 covers detectors and detector circuits. The small surface mount detectors were used early, beginning with the different kinds of detector diodes including Schottky and bias/zero-bias. Detector circuits such as typical detector and Schottky circuits as well as the detector circuit design and test within the IF board for the next section. The IF board chapter will go over the schematic, design, and PCB layout for 16 channels followed by the RF and LO board sections. It will then describe the testing directions for the three circuit boards and the observations found. The paper will end off elaborating on the overall findings and future upgrades of the whole system.

Chapter 2: ECEI System Background

In this chapter, we will review the basic structure of an ECEI system, to better understand how they are organized and how to best realize the changes needed to form a set of back-end electronics.

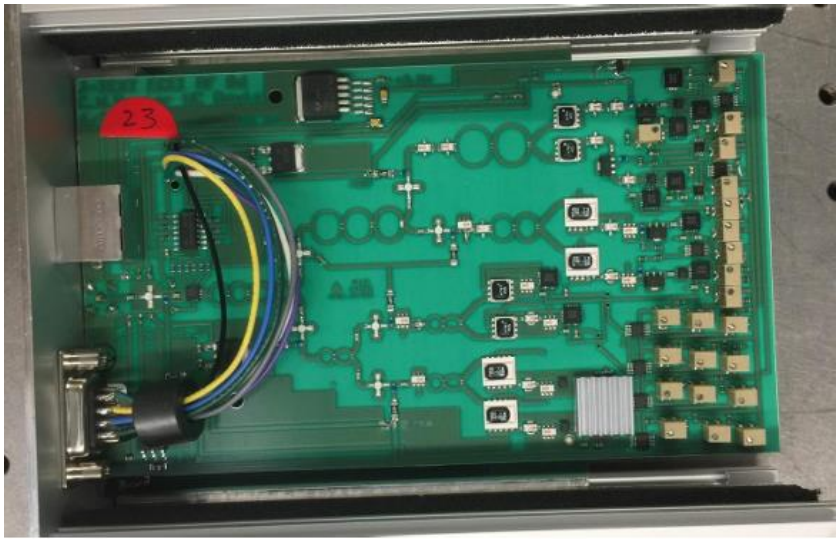
A simplified schematic of the J-TEXT RF board is provided in Fig 2.1. The board uses seven Wilkinson power dividers where divider #1 is a 4-ring divider centered at 6.85 GHz that separates channels 1-4 from channels 5-8. The Wilkinson power dividers split the input signal into multiple bands and achieve separation between two output ports when all ports are matched. Divider #2 is a 3-ring divider centered at 4.25 GHz that separates channels 1-2 from 3-4. Divider #3 is a 2-ring divider centered at 9.2 GHz that separates channels 5-6 from 7-8. Finally, four 2-ring additional power dividers are used to contribute RF signals to the 8 separate mixers. These dividers are centered at 3.45 GHz, 5.55 GHz, and two more centered at 9.20 GHz [9]. The mixers perform a second down-conversion of the input ECEI signals, where the first down-conversion is in the ECEI array box which performs a single sideband conversion of mm-wave signals (typically > 75 GHz) to microwave signals (in the range of 2-18 GHz). For the J-TEXT RF board, the microwave signals input to the RF board have frequencies that fall between 2.0 GHz and 11.8 GHz with output IF signals in the range of 5 to 400 MHz.

Fig. 2.1: Schematic of the J-TEXT RF Board



One of the J-TEXT RF boards, mounted within its enclosure box, is provided in Fig 2.2. The DB9 connector control wires pass through a ferrite bead for enhanced noise shielding. There are 22 small trimmers mounted to this board where each controls the tuning voltage of one of the VCOs on this board. These have been fixed at UC Davis to deliver the LO frequencies set out in Fig 2.1, but can be adjusted with a screwdriver as needed. The amount of tuning that each trimmer can provide is restricted [9].

Fig. 2.2: J-TEXT RF Board within its Module Case



A schematic layout of the J-TEXT IF board is in Fig 2.3. Distinctive to J-TEXT, the IF spacing between channels are switchable between 0.8 GHz, 1.0 GHz, and 1.3 GHz. This signifies that the IF signals have 3 separate low pass filters (180, 225, and 435 MHz cutoff frequencies) relating to these IF channel spacings. Usual IF board responses are shown in Fig 2.4 as the channel 1 low frequency response is narrowed to minimize noise spikes from the RF board corresponding to Wi-Fi signals picked up in the range of 2.4 to 2.5 GHz [9].

Fig. 2.3: Schematic of one of the J-TEXT IF Board Channels

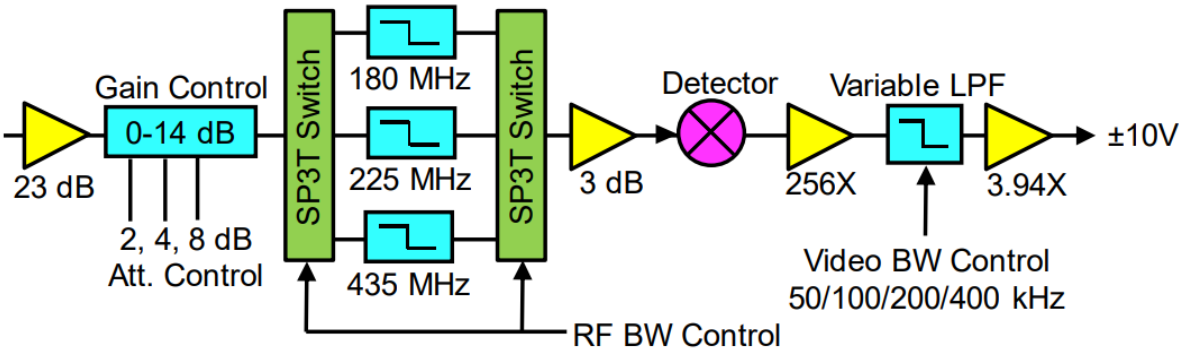
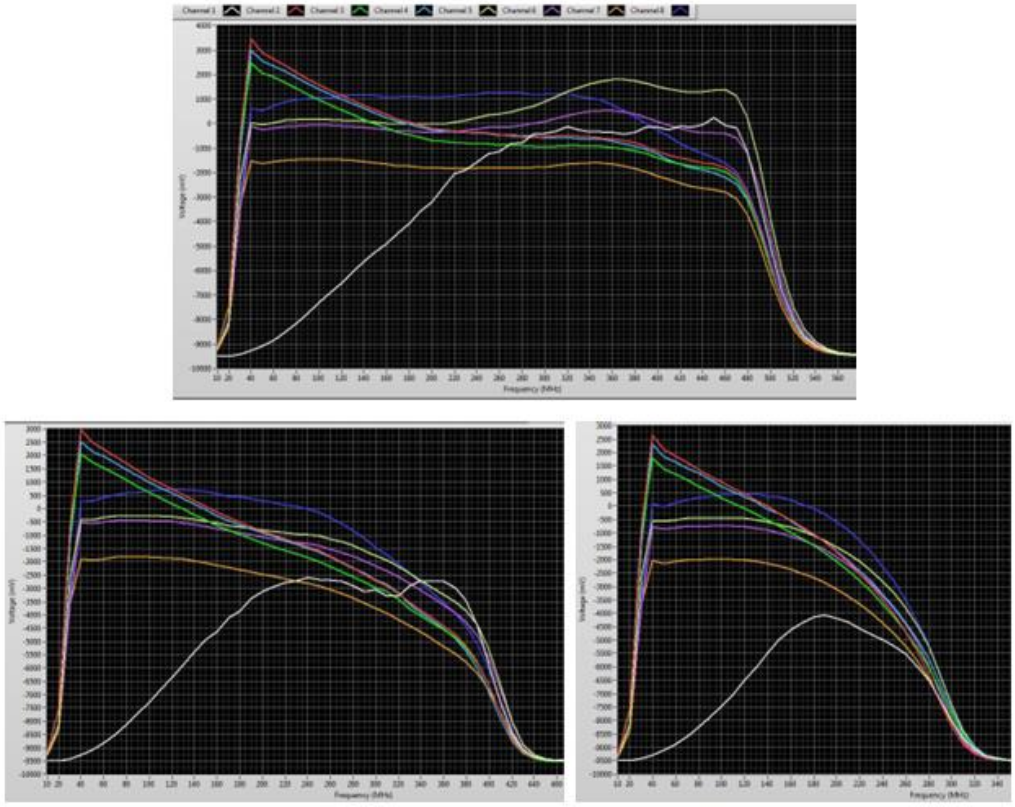


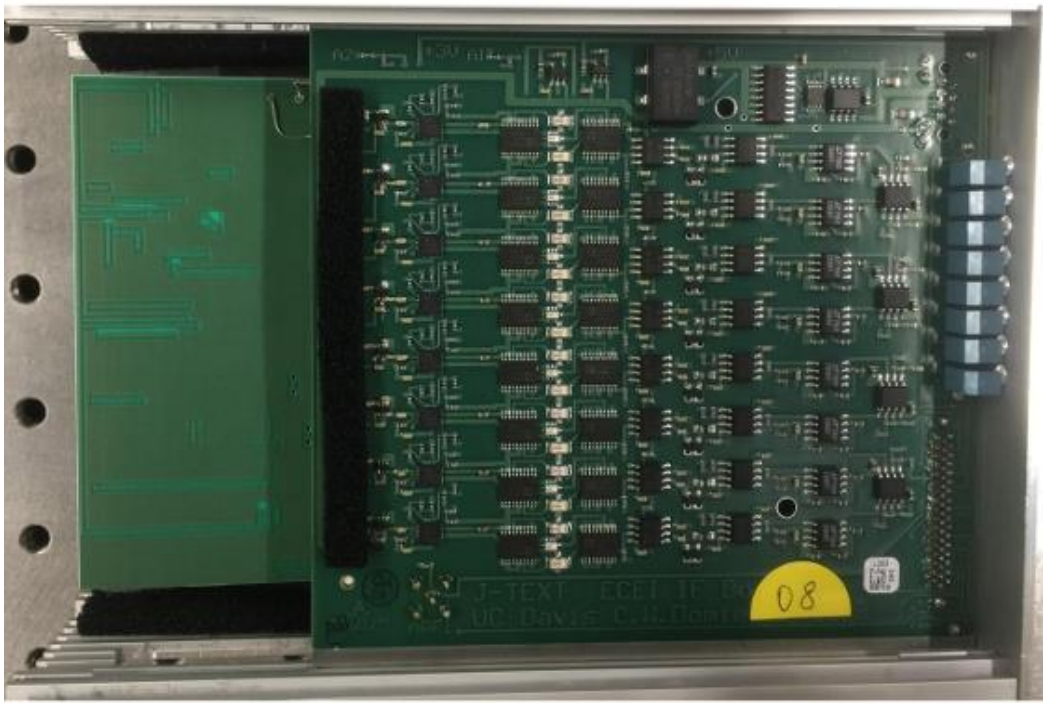
Fig. 2.4: Frequency versus Voltage Responses Showing Wide Zoom (Top), Medium Zoom (Bottom Left), and Narrow Zoom (Bottom Right)



A picture of one of the J-TEXT IF boards is provided in Fig 2.5. There are 8 trimmers, accessible through small holes in the front panel of the enclosure box that are used to change the

DC offset voltages of the 8 analog output signals that are relayed to the NI data acquisition module [9].

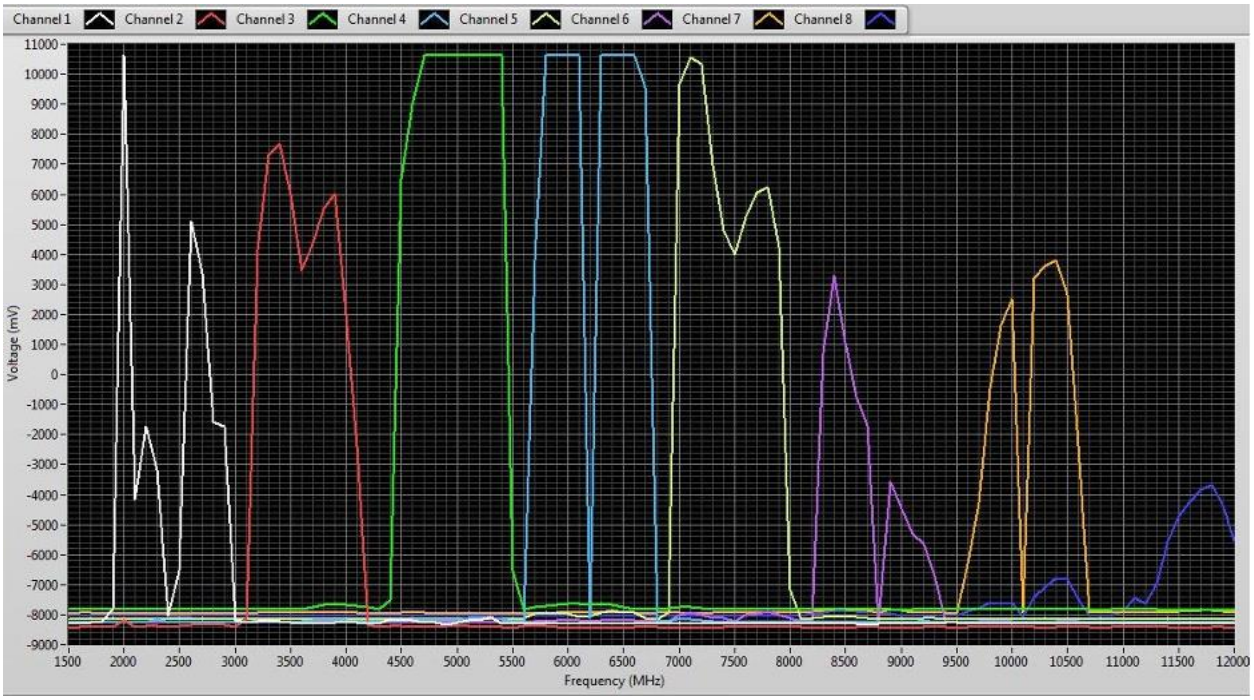
Fig. 2.5: J-TEXT IF Board



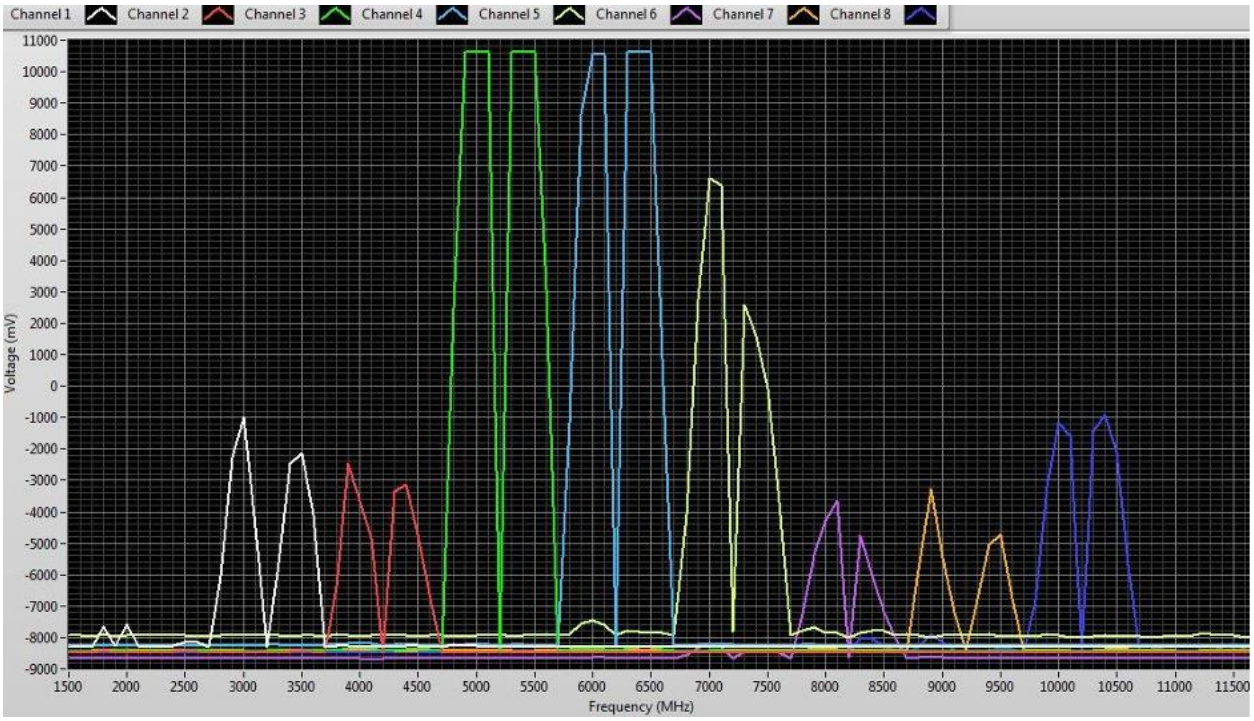
In Figure 2.6, the RF plugs into the back of the IF board through a 120-pin connector, and the two boards link to a custom front panel. On the front panel are entry to the IF and RF power connectors (RJE473), the RF control connector (DB9), the 15 digitizer connector (VHDCI), the RF input and optional trigger connectors (SMA), and 8 small holes to provide access to the IF board DC offset trimmers. The top and bottom of each module have long slots which allow forced air cooling to remove heat from the modules during operation. Microwave absorbers are placed around these slots, on the back panel, on the IF board above the 120-pin connector, and on the side panel that faces the RF board. Some RF boards will also have small absorber pieces attached to significant areas of the board, which dampen RF pickup from other VCOs which can result in significant DC offsets (particularly in wide zoom mode) [9].

Fig. 2.6: One of the J-TEXT ECEI Modules with Side Plates Removed

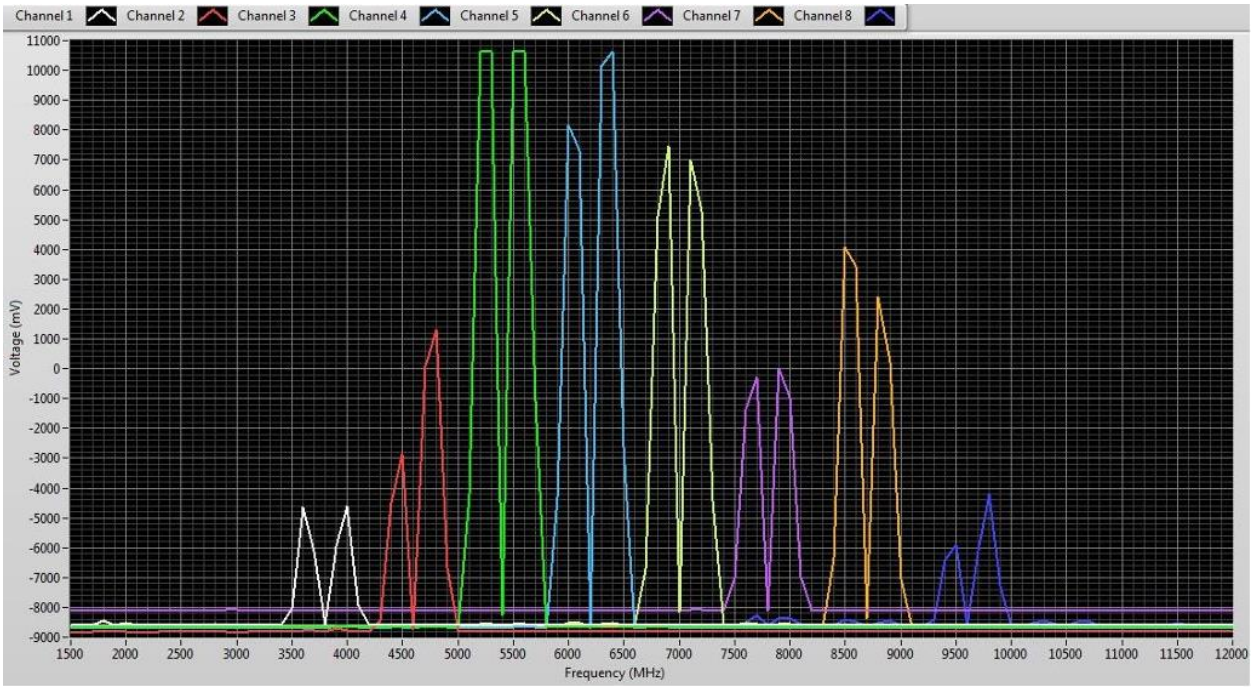
Fig. 2.7: Frequency versus Voltage Responses for One of the J-TEXT ECEI Modules Showing (a) Wide Zoom, (b) Medium Zoom, and (c) Narrow Zoom



(a)


Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Channel 6
Channel 7
Channel 8
Voltage (mV)
Frequency (MHz)

(b)


Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Channel 6
Channel 7
Channel 8
Voltage (mV)
Frequency (MHz)

(c)

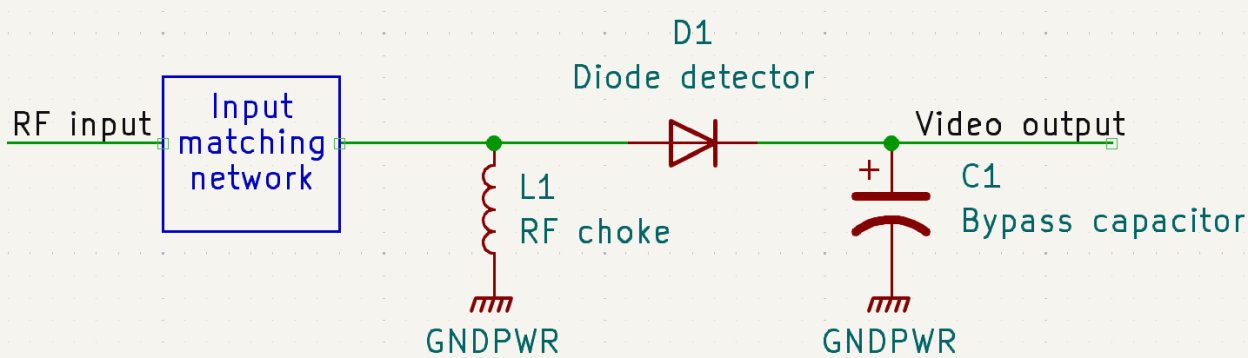
Chapter 3: Detectors and Detector Circuits

3.1 Types of Diode Detectors

The diode detector is the simplest form of detector or demodulator used for amplitude modulated (AM) demodulation as it detects the AM signal envelope. As such, the diode detector or demodulator can provide an output proportional to the amplitude of the envelope of the amplitude modulated signal. In other words, the AM diode detector provides an output equivalent to the envelope of one half of the signal and therefore is an envelope detector in rectifying the RF signal. The diode detector takes an incoming signal, passing current in one direction and blocking current in the reverse direction, thereby rectifying the signal. The AM diode detector can be built from just a diode and a few other components and as a result it is a very low-cost circuit block within an overall receiver.

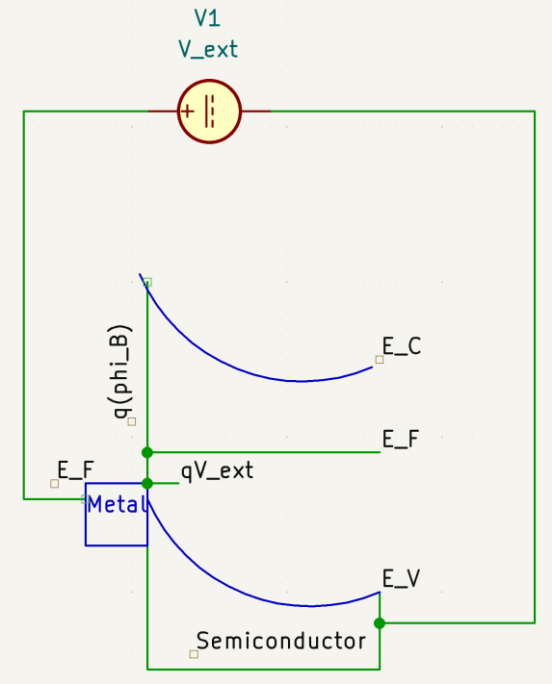
The main specifications for the ECEI detector are operating in the square law region (where the output detector voltage is proportional to the square of the input RF voltage), with an input RF range from 5-200 MHz, and the output frequency to be from DC to 1 MHz. A low pass filter is generally required to remove any high frequency elements that remain within the signal after detection or demodulation. The filter usually consists of a simple RC network (see Fig. 3.1), but in some cases it can be provided by relying on the limited frequency response of the circuitry following the rectifier. As the capacitor in the circuit stores the voltage, the output voltage reflects the waveform peak. Sometimes these circuits are used as peak detectors.

Fig. 3.1: The detector circuit depends on the detector diode with a nonlinear behavior. The diode rectifies incident power giving a signal that is all positive or negative polarity to the bypass capacitor with the amplitude equivalent to the input power level (square-law). Here, the positive voltage will be developed and typical detectors provide negative voltage which happens by reversing the diode in the schematic [11].

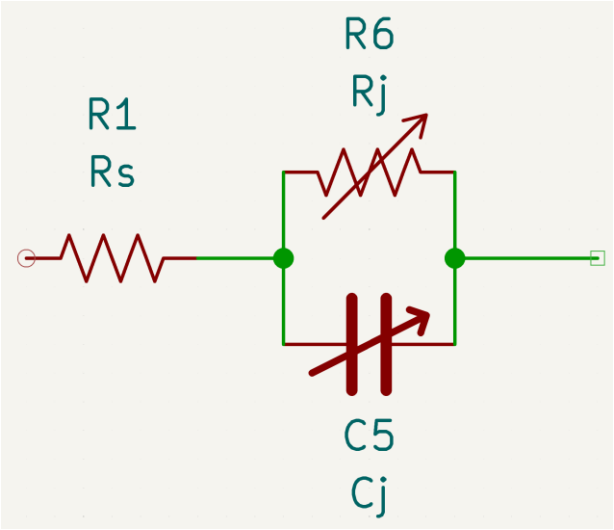


Schottky diode detectors have been used as RF detectors from low frequency to low/sub millimeter compared with other room temperature detectors like pyroelectric detectors or bolometers [12]. A schematic of Schottky diodes composed of a metal-semiconductor junction with a potential barrier is shown in Fig 3.2 (a). Also, a simplified equivalent circuit model of the Schottky diode is shown in part (b) where the series resistance, R_s, and the junction capacitance at zero bias, C_{j0}, determine the cutoff frequency of the Schottky diode ($f_c = 1/2\pi R_s C_{j0}$) [13]. The higher the cutoff frequency, the higher the RF frequency is for the diode where the goal is to get up to 1 MHz.

Fig. 3.2: (a) Energy Diagram of Schottky Barrier, (b) Circuit Model



(a)



(b)

For the nonlinear I-V plot, the turn-on voltage at which a typical metal-semiconductor junction diode begins to conduct is around 0.4 V. Due to this lower value, the forward current of a silicon Schottky diode can be much larger than that of a typical pn-junction diode, depending on

the metal electrode used. This also varies on how it was doped during manufacturing and whether the device is a small signal diode or a much larger rectifying diode [14]. The main difference between the PN junction and the Schottky diode is that the p-type layer of the PN junction is replaced in the Schottky diode with a metal like aluminum, with minority carrier transport replaced with majority carrier transport yielding lower turn-on voltages and faster switching speeds. The turn-on voltage may be lowered by increasing the doping level of the semiconductor, and can be made "zero" by an appropriate doping choice, resulting in a zero-bias detector which switches between conducting and non-conducting states with no DC bias applied.

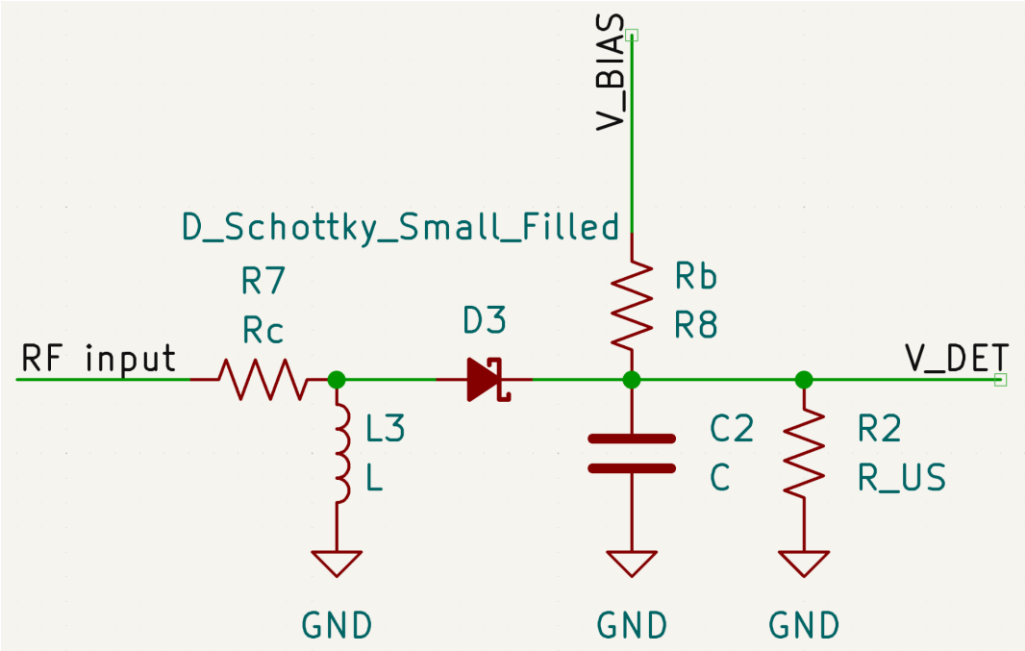
3.2 Types of Detector Circuits

The figure of the circuit below is the schematic of a popular diode-based RF detection circuit. This is similar to a half wave rectifier with output filtering. In the case of an ideal diode, the positive half cycles of the input signal forward bias the Schottky diode, which then charges the capacitor. On the negative half cycle, the diode reverse biases, causing the voltage on the capacitor to be held and yielding a DC output that is proportional to the input signal [18]. A resistor in parallel to the capacitor provides a discharge path to allow this voltage to drop when the input signal decreases or is turned off. There is an inductor, since at low frequencies, the impedance goes to zero which means that the capacitor goes to zero as well. From the input to pass the detector where the capacitor is, the circuit goes from open to short where there is a small distance from the detector.

Since the Schottky diode requires DC bias, this conveys that R_c, where c is the charge time, serves to make the circuit at a resistance of around 15 Ω and in series. The purpose of the inductor is to also handle DC current and to support the bias detector. If there was a zero-bias detector, then there would be no inductance. The current between the bias voltage and diode could be solved by

taking the difference between the bias and diode voltage and dividing by the bias resistor (R_b). The bias detector circuit does not comply with the detector circuit for design since there is no need for the capacitor since the frequencies tested are close together. Also, it is due to the square law region not demonstrating a large dynamic range, thus creating a higher slope at different temperatures.

Fig. 3.3: Schottky Diode-Based RF Detector Circuit



For a zero-bias detector, it has a wider dynamic range, increased thermal stability, and more accurate square law response. The zero-bias Schottky diode detector is a type of RF power detector that does not need a bias voltage to operate and is widely used in RFID and other applications where no primary (DC) power is available. Diodes which are normally biased do not appear to detect when the bias is eliminated and the load resistance is less than a megohm. When the load is a high impedance digital voltmeter, the voltage sensitivity is better when the bias is eliminated [21]. The video impedance of a zero-bias diode is temperature independent and without bias resistance, it simplifies the design of impedance matching networks for small band and high sensitive detectors. A zero-bias diode also has no 1/f noise and is implied for audio frequency

output like motion detectors. It is important to be cautious when picking zero-bias detector circuits due to deviation from the square-law behavior that can occur at low levels [19]. With zero bias, the diode resistance is much higher than the load so most of the detected voltage appears across the diode rather than across the load. However, at higher input levels rectified current flows through the diode and reduces the junction resistance. The voltage divider is no longer significant and the output approaches the detected voltage of the biased diode [20].

With Schottky-bias diode detectors, they can accomplish excellent frequency response and bandwidth when they are improved to have a low forward turn-on voltage [15]. For a typical bias detector I-V curve, it uses the forward current equation, $I = I_{SAT}(e^{[(q/nkT)(V-IR_S)]}-1)$ where $I_{SAT} = \tau A^*T^2 e^{[(q\phi_B)/(kT)]}$ [16]. Moreover, I_{SAT} is the saturation current, q is the electron charge, n is the ideality factor, k is Boltzmann's constant, T is room temperature, V is the forward voltage, and R_S is the series resistance. For the saturation current formula, τ is the tunneling probability, A* is the effective Richardson constant, and ϕ_B is the Schottky barrier height in potential units. In comparison to the zero-bias detector, there is no Schottky barrier height and subtraction of 1.

Graphically, the Schottky-bias detector is characterized close to the equation depending on various I_{SAT}, n, and R_S values. The diode expresses a nearly square-law relationship between I and V over a small range of bias voltages. The relationship is neither square or linear (crossover region) and hence, Schottky diode detectors have limited operating range [17].

Comparing the bias and zero-bias detector, the biased diode lessens noise temperature of the resistance R_B at video frequencies and the resistance supplements temperature variation of absolute temperature in °K for constant current. Moreover, R_B will be steady over temperature if the resistance is inversely proportional to T. If a mixer diode or a detector diode not designed for zero-bias operation is used without bias, the small signal resistance, R_B, (video impedance) will be

too high. Hence, the RF voltage at the junction will be much less than it should be, resulting in lower tangential signal sensitivity (TSS) and voltage sensitivity at very low signal levels. When the signal level is increased, the diode self-biases to a lower resistance, R_B, and more of the power reaches the diode. Therefore, the voltage sensitivity increases. The result is that the detected response is faster than square law at very low signal levels, approaching fourth law or fifth law in many cases [19]. This establishes a substantial error if a square-law characteristic is assumed, as in many power level measurement applications. This effect does not happen if a zero-bias Schottky diode is used, properly matched, in a low loss detector mount [19].

Furthermore, it would be beneficial to use the zero-bias detector because of the advantages of eliminating the inductor to ground and the bias resistor such as from the previous Schottky diode detector circuit to use less components. This is especially for the RF and IF video frequencies close to each other where the inductor might affect the signal level. If the circuit is DC biased correctly, it is operating at the turn-on voltage and we would get the square law region immediately.

3.3 Detector Test Circuit Designs

Previous ECEI detector circuits employed both conventional Schottky diodes (Agilent HSMS-2820) and zero-bias Schottky diodes (Agilent HSMS-2850). Both of these Schottky diodes are now obsolete, hence the need to develop a new detector circuit employing detector diodes that are still being manufactured. A zero-bias detector is preferred due to (a) its simpler design, and (b) the narrow frequency gap between the input RF bandwidth (5-77 MHz) and the output video bandwidth (DC-1 MHz). Detector circuits were therefore designed for both zero-bias and biased detectors, with laboratory testing to identify the type of circuit to be duplicated in the resultant ECEI IF board. Schottky diodes chosen for these boards included the Macom MA4E2200B1-287T (zero-bias) detector series pair and the Toshiba CUS520 (biased) Schottky barrier diode.

In general, detector circuits work best with operational amplifiers (OPAs) both before (to provide a 50 Ω input impedance to the RF driver) and after (to provide a high impedance load) the detector. Two detector test circuits have been designed in KiCAD, with and without a pre-detector OPA. The circuit without the input OPA was intended to study detectors with RF inputs in the range of 3 to 5.5 GHz, i.e. without a second down-conversion step as is standard in ECEI systems and which is presented in Chapter 2. This was a possible option when the high-resolution ECEI electronics project was first proposed, but was later rejected as being both more complicated and more expensive to implement and without any significant benefits in terms of system performance. While OPAs are commercially available with 3-dB bandwidths as high as 7 GHz (i.e. the LMH3401), they offer little benefit over a much lower cost RF amplifier such as the BGA2851 employed for both the OPA and non-OPA test circuits.

While KiCAD is a very useful and versatile program, there were several instances in which a particular circuit element or symbol (such as an OPA) was not part of the KiCAD library. In these cases a new symbol had to be drawn up (or modified from an existing symbol) and saved into a user library for use on these and other circuits. Passive component values (resistors, capacitors) were largely taken from active component datasheets, with some modifications to achieve a particular circuit gain or because of the availability of on-hand components (such as replacing a 4.7 μF power line capacitor with an available 6.8 μF capacitor).

The first test board begins with a coaxial connector connected to a BGA2851 wideband amplifier that is internally matched to 50 Ω with a gain of 24.8 dB. This RF amplifier was chosen for its low noise figure and low cost. The two block capacitors of 330 pF at the input and output isolate the DC voltages on the amplifier's input and output pins. Then comes the operational amplifier where the input impedance is set to 50 Ω with a resistor to ground and the output

impedance is set to 50 Ω with a series output resistor and a 50 Ω load. The detector is next and it then connects to a 5 V source through a 5M Ω resistor to provide a DC bias current for use with biased detectors. Finally, the detector output connects to an ADA4610-2ARZ dual OPA and then to the output coaxial connector.

Unit A of the dual amplifier is designed with a voltage gain of 16. Next, the output shifts to unit B which has a similar voltage gain of 16, but with a DC offset circuit controlled by a 200 Ω trimming potentiometer. The purpose of the DC offset circuit is to convert the detector circuit from unipolar (output varies from zero to +2.5 V as the input RF power increases) to bipolar (output varies from -2.5 V to +2.5 V as the input RF power increases). Finally, there is duplication of the exact same circuit (see Fig. 3.4), but without the OPA circuit configuration (see Fig. 3.5).

Fig. 3.4: Detector Circuit Type 1 Schematic (with OPA) in Schematic Editor

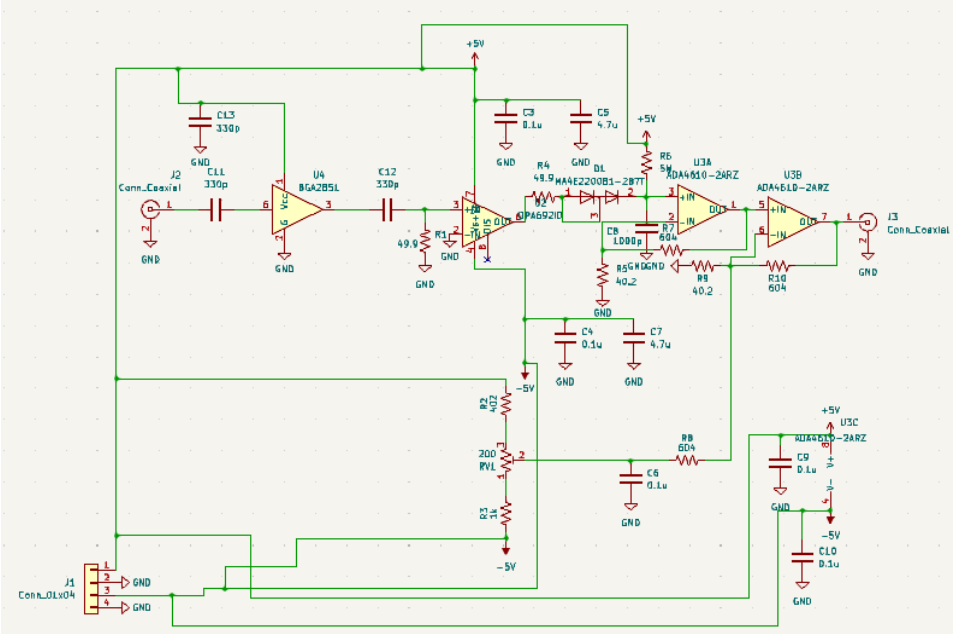
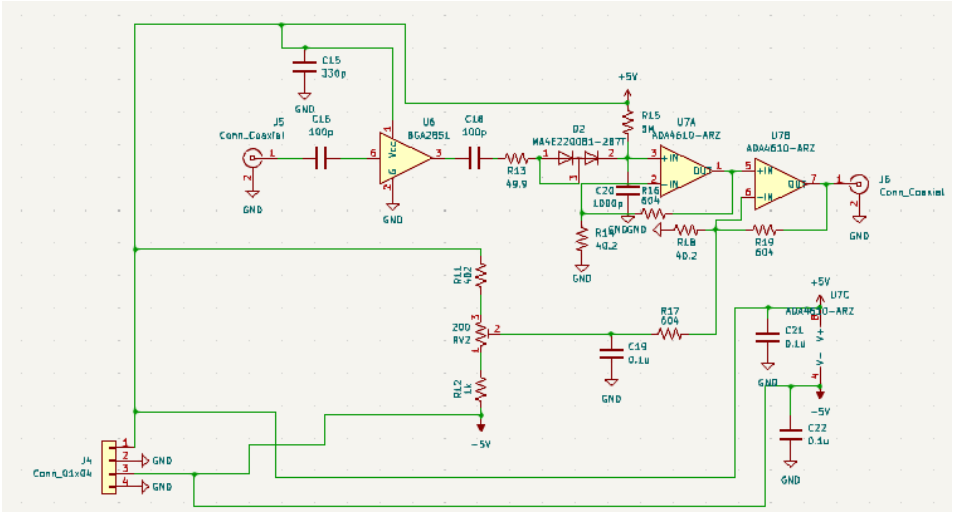
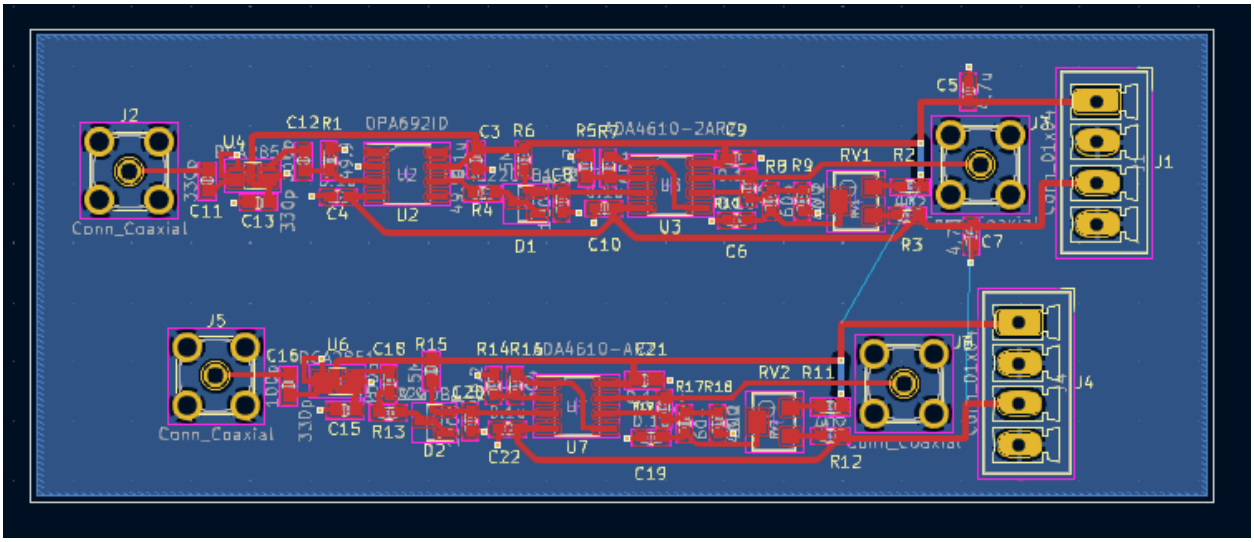


Fig. 3.5: Detector Circuit Type 1 Schematic (without OPA) in Schematic Editor



With the schematic completed, work then began on laying out the actual PCB. We found component footprints already installed in KiCAD for both designs. Standard PCB layout procedures were followed, with power line capacitors placed in close proximity to their respective amplifiers. Size 0603 packages were chosen for the passive resistors and capacitors, balancing ease of manual soldering (where larger packages are easier) with minimizing board sizes (where smaller packages result in smaller boards). Hand solder footprints, distinct from more compact footprints designed for machine assembly, were chosen where possible. A back-side ground plane was employed for improved noise performance, using vias as needed to transfer power lines between the front- and back-sides of the board [22]. The silkscreen component references were carefully placed on open spaces on the board to not overlay any of the footprints. Shown in Fig. 3.6 is the PCB layout for the two Type 1 detector boards, both with and without the pre-detector OPA. This board was fabricated on standard FR4 laminate, after which the components were hand soldered to the board and testing commenced (see Sec. 3.4).

Fig. 3.6: PCB Layout of Detector Type 1 Board with OPA (Top Circuit) and without OPA (Bottom Circuit) in KiCAD PCB Editor



Laboratory testing of the Type 1 circuit revealed problems with the zero-bias detector diode being oriented in the wrong direction leading to a detector voltage that decreased with increasing RF input power. Rather than design a new board to fix these issues, the already fabricated Type 1 circuit with OPA was modified to remove trimmer RV1 and therefore eliminate the DC offset correction circuit (which would have biased the output to roughly -2.4 VDC) such that with no input RF the output sits at 0 VDC. An AD8672 dual OPA replaced the ADA4610-2 due to its better noise performance. The resultant Type 2 circuit schematic is shown in Fig. 3.7, with a photograph of the modified board shown in Fig. 3.8. This circuit and board were subsequently used in all detector circuit testing (see Sec. 3.4).

Fig. 3.7: Detector Circuit Type 2 Schematic in Schematic Editor

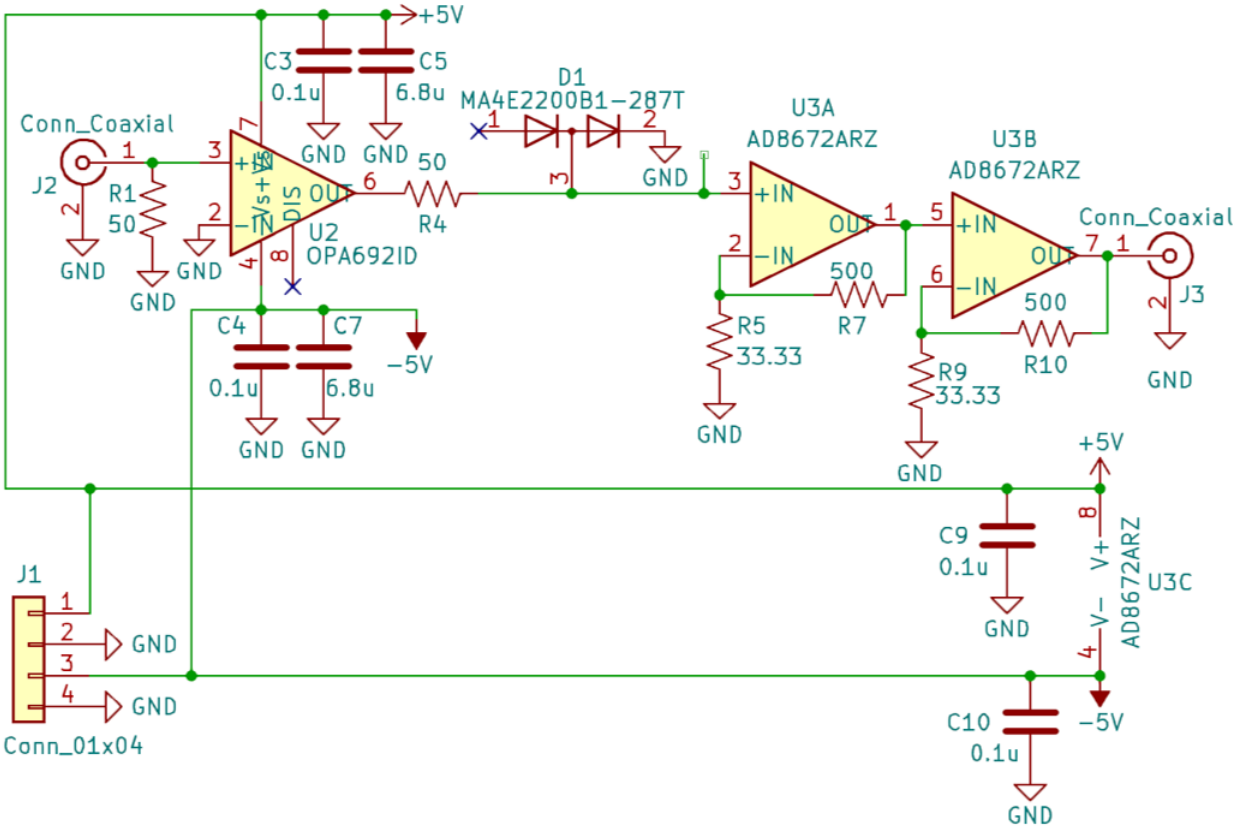


Fig. 3.8: Photograph of Modified Detector Circuit Type 2 Board

3.4 Detector Test Circuit Measurements

The basic detector testing arrangement is shown schematically in Fig. 3.9 and in a photo in Fig. 3.10. A tunable RF signal is generated by an HP 8665B synthesized signal generator, whose output is first low-pass filtered (to remove any harmonics generated by the source) and attenuated

before being input to the test board. The detector board DC output is measured by an HP 3457A multimeter and its video modulation output by both a Rigol DS1054 oscilloscope and an Agilent E4407B spectrum analyzer.

Fig. 3.9: Schematic Diagram of the Basic Detector Board Instrument Setup

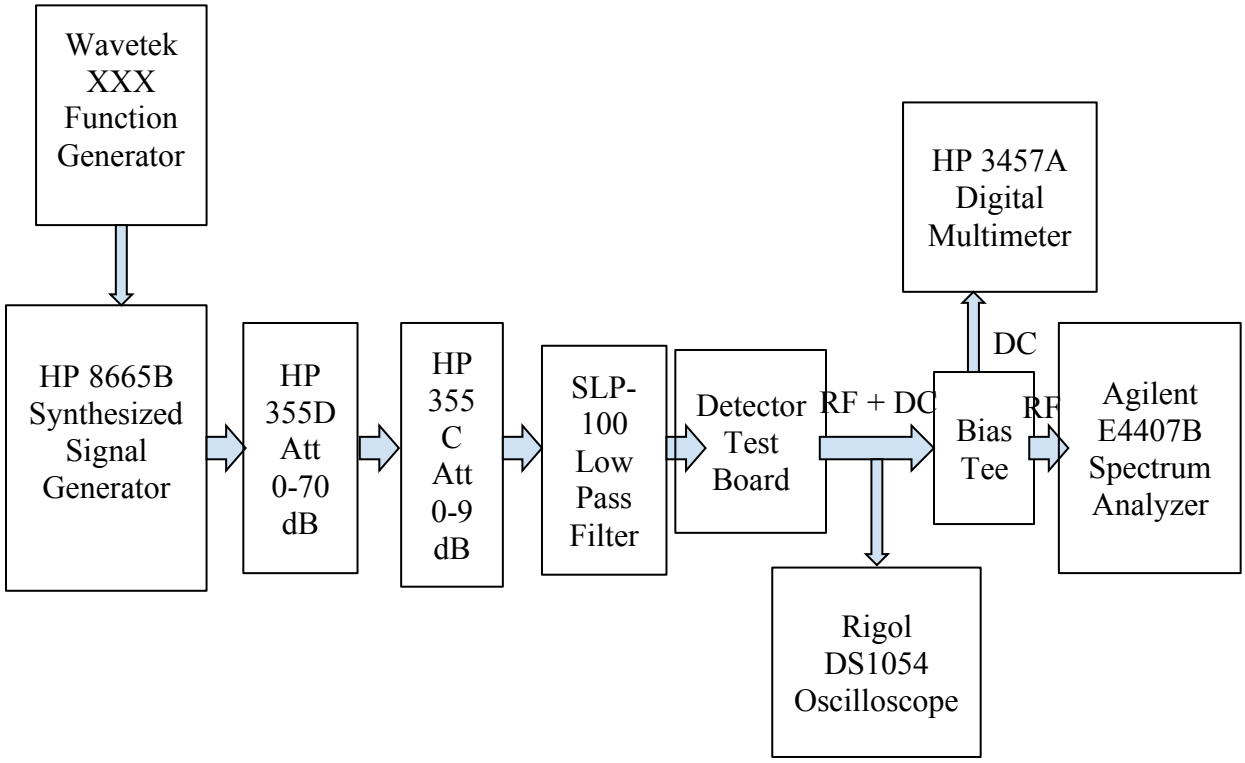
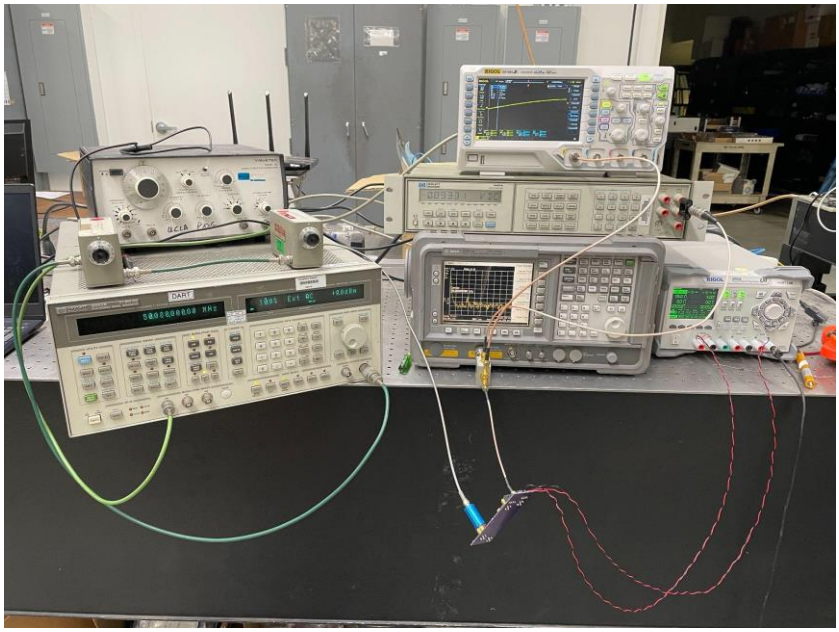


Fig. 3.10: Photograph of the Basic Detector Board Instrument Setup



A Wavetek function generator connects to the AM input of the HP 8665B, allowing it to impose a controlled amplitude modulation on the RF signal. What was not immediately clear, however, was determining the level modulation being imposed on the RF signal. This is important as we want to verify if the detector circuit passes this modulation on to the detector output. The first test was therefore to measure the modulation level using the spectrum analyzer, bypassing both the low pass filter and the detector board. Our primary inputs are the RF signal frequency set by the RF signal generator, the modulation signal frequency set by the function generator, and the AM signal amplitude set by the RF signal generator. Here, the RF signal generator displayed warning messages if the AM signal level was either too low or too high; the amplitude of the function generator signal was therefore manually adjusted at each modulation frequency to maintain optimal modulation. The resultant modulation was then determined using the spectrum analyzer, by measuring the modulation sideband level, i.e. the power difference between the carrier/center frequency and the adjacent sideband frequency. From this we calculate the Amplitude Modulation Index $m = M/A$ where A = the carrier amplitude and M = the modulation

amplitude (not be confused with modulation sideband level). Using the spectrum analyzer measurements, this yields $m = 200\% \cdot 10^{(M-A)/20}$ where A-M is the modulation sideband level in dB and *m* in this case expressed in %. Table 3.1 displays the measured modulations observed with modulation frequencies varying from 10 kHz to 400 kHz, with center frequencies varying from 5 to 150 MHz. The results shown in this table demonstrate that the setup is indeed capable of supplying an amplitude modulated RF signal with which to test the detector board.

Table 3.1: Measured AM Imposed on RF Signal Source

Center Frequency (MHz)	**AM Frequency (Hz)**	**dBm Drop between Peaks**	**Modulation Index (%)**
5	10k*1	20.155	19.65
	100k*0.5	24.22	12.3
	100k*1	29.32	6.84
	100k*2	41	1.78
	1M*0.4	54.7	0.37
50	10k*1	19.565	21.03
	100k*0.5	21.36	17.1
	100k*1	24.55	11.84
	100k*2	34.79	3.64
	1M*0.4	49.9	0.64
100	10k*1	19.59	20.97
	100k*0.5	20.665	18.5
	100k*1	23.66	13.12
	100k*2	33.95	4.01
	1M*0.4	48.13	0.78
150	10k*1	19.71	20.68

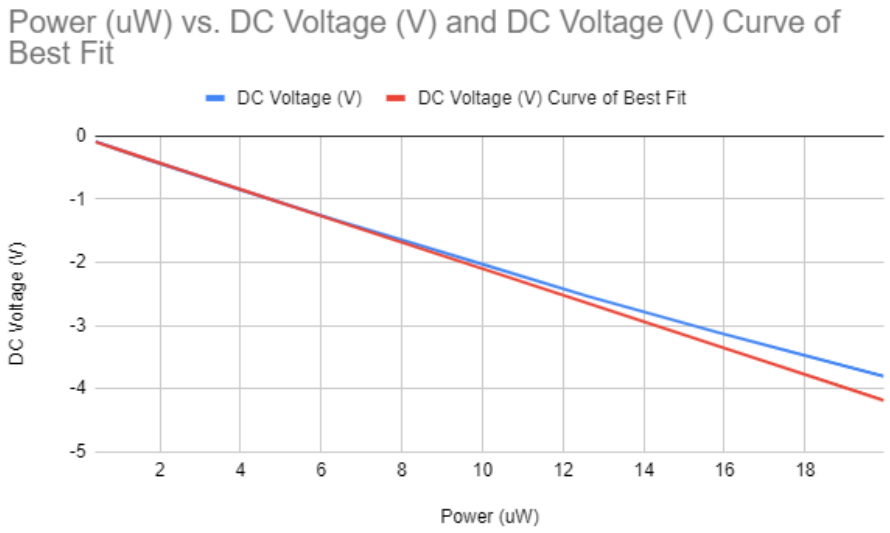
	100k*0.5	21.26	17.3
	100k*1	23.83	12.87
	100k*2	34.19	3.9
	1M*0.4	49.56	0.665

The first test consisted of measuring the response of the test board to the RF input power, keeping the RF frequency fixed at 50 MHz and the AM modulation turned off. Measurement results are presented in Table 3.2. The circuit shows clear signs of compression at the higher input signal levels, so a linear curve fit was made to the experimental data for output voltages between around 0 and -1 V. The experimental data, along with this curve fit (y = -0.209x - 0.0114), are plotted in Fig. 3.11.

Table 3.2: Detector Circuit Output Voltage as a Function of RF Input Power

Attenuation (dB)	**Power (μW)**	**DC Voltage (V)**
-34	0.3981071706	-0.088
-32	0.6309573445	-0.137
-30	1	-0.22
-28	1.584893192	-0.35
-26	2.511886432	-0.54
-24	3.981071706	-0.85
-22	6.309573445	-1.32
-20	10	-2.03
-19	12.58925412	-2.53
-18	15.84893192	-3.11
-17	19.95262315	-3.8

Fig. 3.11: Detector circuit output voltage as a function of RF input power, showing raw data (blue) and curve fit (red).



Using this curve fit, we can then calculate the percentage error between the detector circuit response and the square law (defined by where the output voltage is linearly proportional to the input power or the square of the input voltage) response, as shown in Table 3.3. Highlighted in yellow are identified regions in which the circuit deviates from square law, i.e. suffers from signal compression.

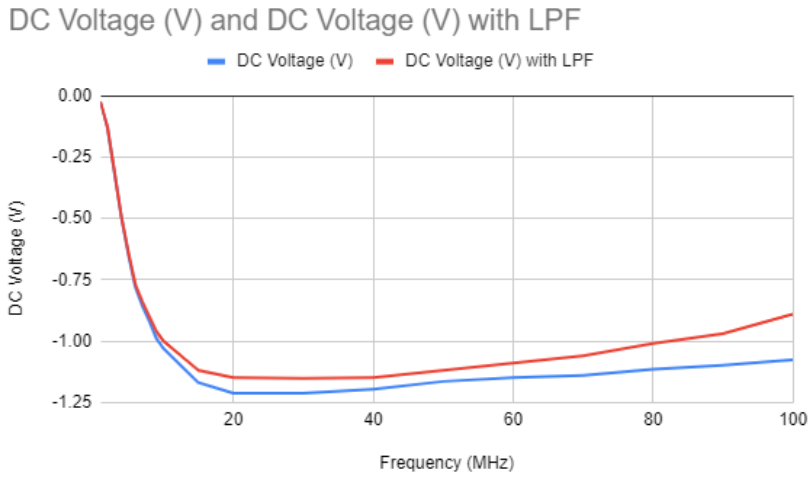
Table 3.3: Comparison of the detector circuit response to the calculated square law curve fit.

DC Voltage (V)	DC Voltage (V) Curve of Best Fit	%=(VDC/VDC Best Fit)*100	Actual %=100-%
-0.088	-0.09460439865	93.01893068	6.981069316
-0.137	-0.143270085	95.62359093	4.376409071
-0.22	-0.2204	99.8185118	0.1814882033
-0.35	-0.3426426772	102.147229	-2.147228954
-0.54	-0.5363842642	100.6740943	-0.6740943118
-0.85	-0.8434439865	100.7772909	-0.7772909225
-1.32	-1.33010085	99.24059518	0.7594048199
-2.03	-2.1014	96.60226516	3.397734843

-2.53	-2.642554111	95.74070744	4.259292561
-3.11	-3.323826772	93.56684969	6.433150308
-3.8	-4.181498238	90.87651802	9.123481981

As the channel spacing of our eventual high-resolution ECEI system will be 160 MHz, we require a double-sided bandwidth (DSB) < 160 MHz to maintain this high resolution. In terms of the detector circuit, this translates to the need for a low pass filter whose 3 dB bandwidth is < 80 MHz. The SLP-100 in Fig. 3.9 was therefore replaced with a VLF-45+ filter (with the LFCV-45+ being the surface mount equivalent) with a 3 dB cutoff frequency of 77 MHz, and the RF frequency response of the circuit with this low pass filter was measured. Here, the input attenuation was set at -18 dB and the OPA feedback resistor R10 set to 200 Ω such that the output voltage is roughly -1 VDC to have a strong but not compressing point to maintain signal levels within the square law region as the RF input frequency is swept. Plotted in Fig. 3.12 is the measured RF frequency response with and without the low pass filter.

Fig. 3.12: RF Frequency Response of Detector Circuit



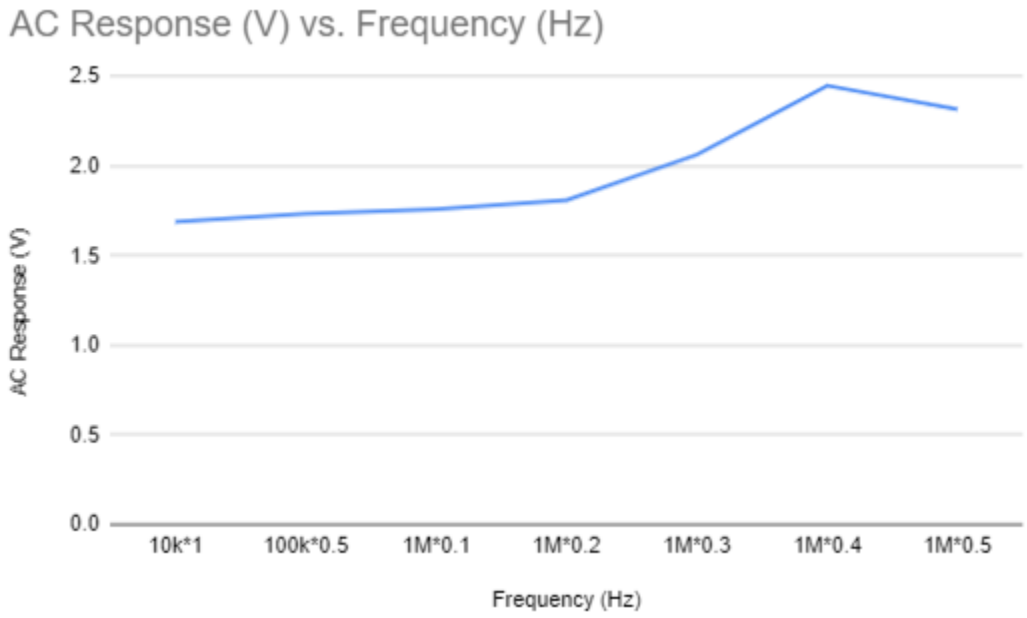
The final measurement made with this detector circuit was to characterize the AC response, i.e. the response of the circuit to an AM modulated RF input. We set up our results by first adding a power divider and adjusting the attenuation to 19 dB at a center frequency of 50 MHz with 10%

AM depth. At each of the modulation frequencies, we took the dBm between spectrum analyzer peaks and set it equal to 20log(*m*/2) to find the modulation index *m*. For the AC response, we took the measured AC voltage peak-to-peak from the oscilloscope and divided it by the modulation index for each frequency ranging from 10 kHz to 500 kHz (the test equipment proved unable to operate properly with modulation frequencies above 550 kHz). The measurements are tabulated in Table 3.4, with the AC response plotted in Fig. 3.13. While a flat response was expected, possibly falling off at higher frequencies, the plotted results show a slight increase in sensitivity as the modulation frequency increases above 200 kHz. This boost, however, is likely due to sidelobe amplitude measurement errors at the extremely low (< -40 dBc) sidelobe levels observed above 200 kHz.

Table 3.4: Detector Circuit AC Response Measurements

Frequency (Hz)	**AC Response (V)**	**m**	**m Calculation (dB=20log(m/2))**	**V = AC Response Calculation ((VACp-p)/m)**
10k*1	1.69	0.102	-25.81 dBm=20log(m/2)->m=0.102	0.172V/0.102 = 1.69
100k*0.5	1.736	0.087	-27.23dBm=20log(m/2)->m=0.087	0.151V/0.087 = 1.736
1M*0.1	1.76	0.066	-29.61dBm=20log(m/2)->m=0.066	0.116V/0.066= 1.76
1M*0.2	1.81	0.021	-39.41dBm=20log(m/2)->m=0.021	0.038V/0.021= 1.81
1M*0.3	2.065	0.0092	-46.77dBm=20log(m/2)->m=0.0092	0.019V/0.0092= 2.065
1M*0.4	2.45	0.0049	-52.16dBm=20log(m/2)->m=0.0049	0.012V/0.0049= 2.45
1M*0.5	2.32	0.0031	-56.15dBm=20log(m/2)->m=0.0031	0.0072V/0.0031= 2.32

Fig. 3.13: Measured AC Response of Detector Test Circuit



These measurements have shown that the chosen zero-bias Schottky diode detector, the Macom MA4E2200B1-287T, functions well and meets all of the requirements for use in ECEI. While the test boards are suitable for also testing the biased Toshiba CUS520 Schottky diode detector, it was deemed unnecessary as use of the zero-bias detector eliminates the need for the more complicated DC biasing circuitry.

Chapter 4: IF Board

4.1 Schematic Layout

The basic structure of the IF board is similar to that of previous ECEI systems such as the J-TEXT system described in Chapter 2 and is laid out in Fig. 4.1. A schematic diagram for one channel of this system, drawn in KiCAD, is shown in Fig. 4.2. Like the detector circuit board designs, we had to make some modifications using the Symbol Editor to match with the pin alignment and electric type based on the components' data sheet. For instance, components such as the low pass filters, amplifiers, FX input connector, and the MAAV attenuator.

IF signals from the companion RF board are transferred to the IF board via a 120-pin connector. The connector also serves to transfer DC power from the IF board back to the RF board. From this connector are coupled 16 independent IF signals, each originating from a frequency mixer pumped by a different LO signal on the RF board. These signals couple to a Mini-Circuits MAR-6SM LNA which has 22 dB of gain, a noise figure of 2.1 dB and an output compression point of +4 dBm. As the MAR-6SM amplifier provides DC to 2 GHz, we will only be implementing and experimenting from 5-100 MHz due to the 160 MHz spacing and the local oscillators where we may still alter the frequencies from the tests and responses. 500 pF was chosen for the block capacitors because it will limit the low frequency end. At the output, there is also a connection to the required bias resistance, V_{cc}, and the bypass capacitor where the bias resistance depends on the V_{cc}. The bias resistance is chosen to be 560 Ω for V_{cc} = 12 V since 12 or 20 mA is good for the chip.

Fig. 4.1: Block Diagram of One Channel for IF Board

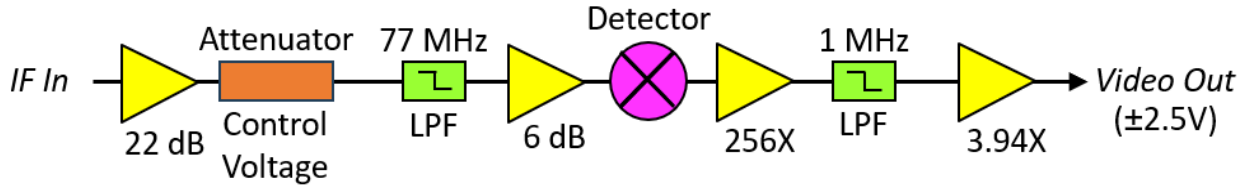
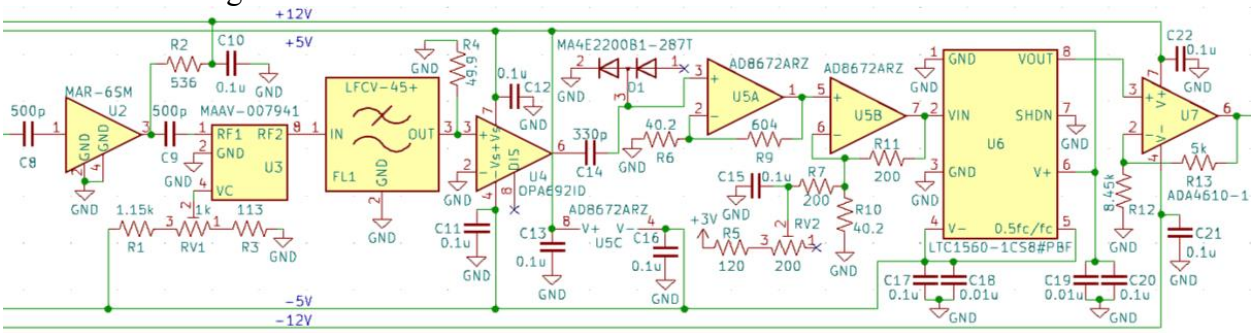


Fig. 4.2: One Channel for IF Board Schematic in Schematic Editor



Each LNA drives an attenuator, to provide a means to control the IF signal level into the detector part of the circuit. Both digital and analog attenuators were originally considered, but space constraints associated with the 16-channel IF board led to an analog approach. Here, the

MAAV-007941 attenuator provides up to 12 dB of attenuation as the control voltage is varied between -2.5 and -0.25 V. The control voltage from the attenuator is wired to a 1kΩ trim potentiometer which is in series with a 1.15kΩ and a 113 Ω resistor calculated to achieve the desired -2.5 V to -0.25 V tuning range.

The attenuator output is next low-pass filtered by a Mini-Circuits LFCV-45+ with a 3 dB cutoff frequency of 77 MHz which increases to 15 dB at 100 MHz and 40 dB at 150 MHz.

After the low pass filter comes the OPA692ID buffer amplifier with 6 dB of gain (A_V=2), with an input impedance of 50 Ω as required by the low pass filter. The OPA provides a good drive signal to the detector subcircuit, independent of the load impedance of this subcircuit. Note that the detector polarity is switched from that of the test circuit, as we require an output voltage that increases with increasing IF input power.

As was the case in the test circuit, an AD8672ARZ dual operational amplifier is employed after the detector, with a voltage gain of 16 for unit A and 6 for unit B. The lower gain for unit B is due to the replacement of the 604 Ω feedback resistor with a 200 Ω resistor needed by the DC offset correction circuit which is incorporated into unit B. The DC offset circuit consists of a 200 Ω resistor (matching that of the feedback resistor) connected to the rotor of a 200 Ω trimmer which in turn is connected to the output of a +3 V voltage regulator (providing a low noise, constant voltage reference to the DC offset subcircuit) through a 120 Ω resistor. The DC offset subcircuit provides a roughly −1.55 V DC offset to the OPA output signal, controlled by adjustments made to the 10-turn trimmer. It should be noted that a unit B gain of 16X is preferred over the current 6X for signal-to-noise reasons, but was incompatible with the 200 Ω trimmers that had been purchased for the project. Increasing the trimmer resistance to 1.0 kΩ, and that of the regulator

series output resistor to 332 Ω, would allow this modification and is something that needs to be considered for future work.

The signal next passes through a LTC1560 low pass filter for antialiasing. The Nyquist theorem states that signals must be sampled at no less than twice the highest frequency component of the signal for accurate digitization. Intended to be connected to a 2 MS/s digitizer, the 1.0 MHz cutoff frequency of this filter eliminates higher frequency noise to satisfy the Nyquist theorem requirements. The filter has a maximum output voltage swing of ±1.75 V, which is why the DC offset of the previous stage was set at roughly −1.55 V and the OPA output designed to fall between −1.55 V and +1.55 V. The final stage of the circuit is an ADA4610-1 amplifier with 1.6x the gain, to boost the output voltage from ±1.55 V to ±2.45 V for use with a ±2.5 V digitizer input range. We set the power line voltages for the ADA4610-1 to ±12 V rather than ±5 V to have a future option of increasing the output voltage range from ±2.5 V to ±5 V without need for a board redesign.

Lastly, we required connectors to bring DC power (±5.0 V and ±12.0 V) to the board and to transfer the 16 output signals to external digitizers, as shown in Fig. 4.3. A RJ45 modular connector is used for the input power connector. The RJ45 connector can handle a maximum current of 1.5 A without overheating, with each pin rated to at least 0.8 A which exceeds the current draw calculated for this board. The particular version employed here has two internal LEDs that can be used to verify the presence of some of the input power lines. Using a 1 kΩ resistor to limit the current to each LED, the +5V and -5V lines were connected to the LED inputs with the other end grounded such that the LEDs are energized when the appropriate power is present. Also shown here is the +3.0 V regulator circuit employed in the DC offset circuit. On the output side, we wired the output signals to a 68-pin VHDCI connector that could in principle connect directly to the

digitizer via standard VHDCI cables. As pin-outs vary slightly depending on the multichannel digitizer brand, no effort was made to match the pin-outs to a particular make or model digitizer with pins instead selected based on proximity to the respective circuit outputs.

Fig. 4.3: IF Board First Channels with Power Connector and Regulator Circuit Schematic

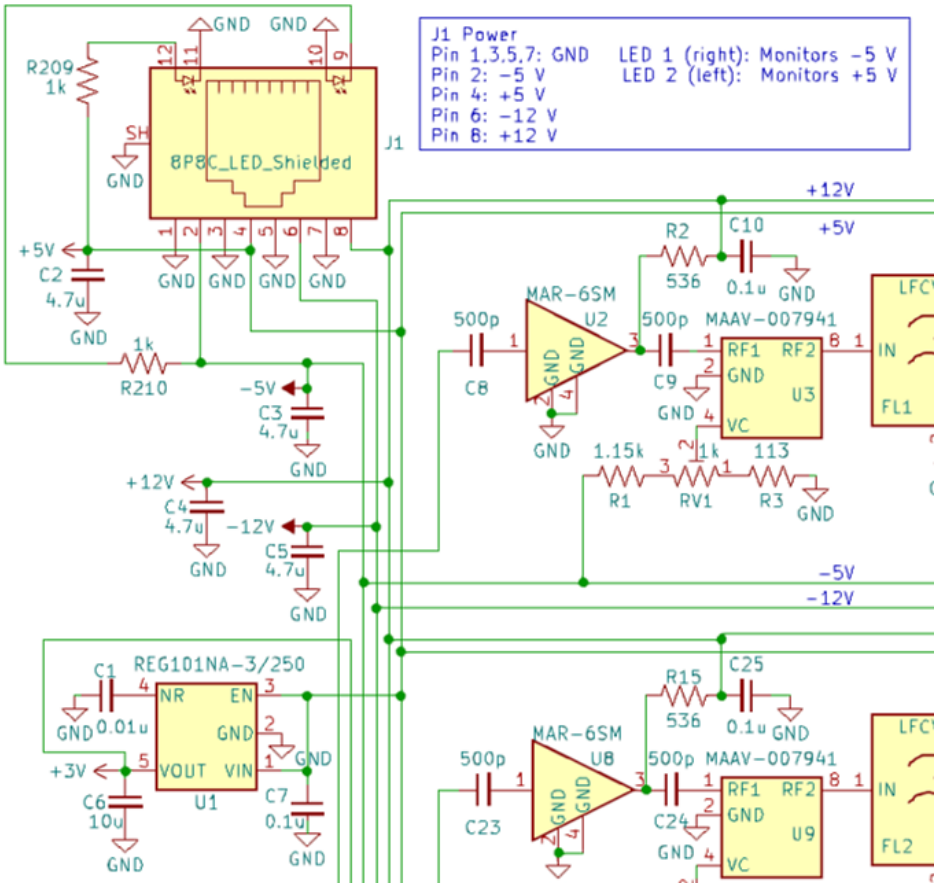
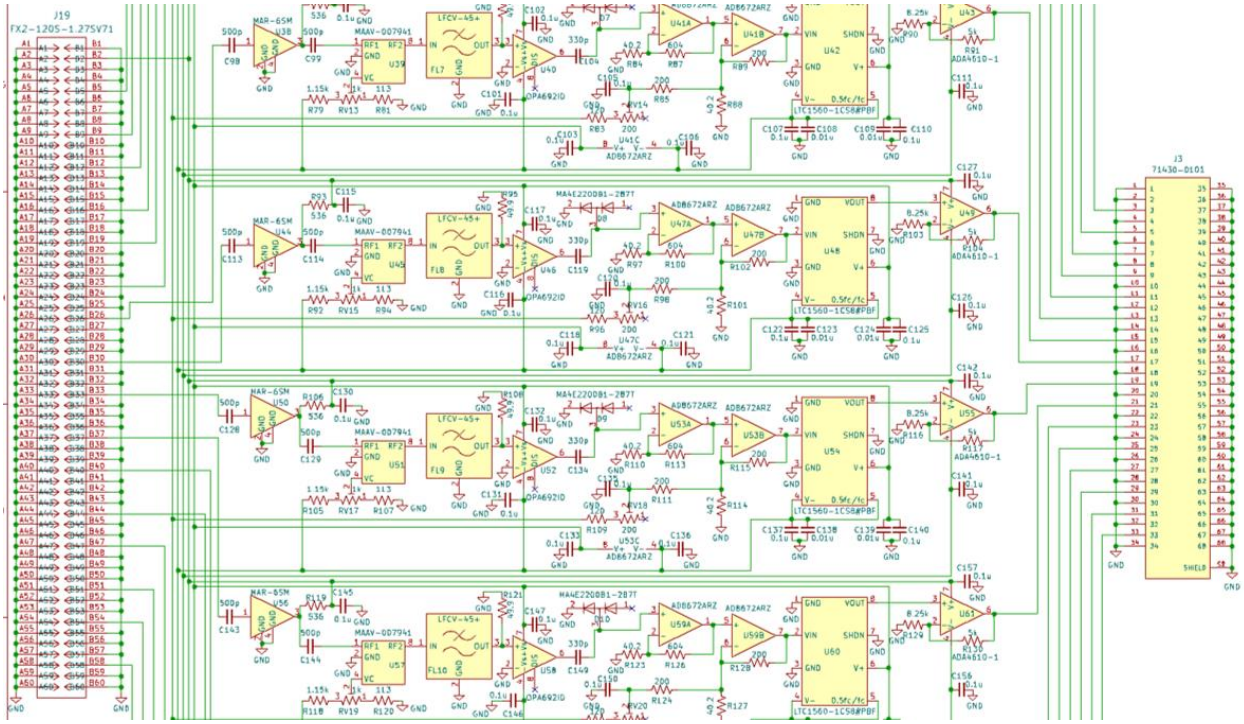


Fig. 4.4: IF Board Input (Left) and Output (Right) Connector Schematics



4.2 PCB Layout

Previous 8-channel ECEI boards, such as those described in Chapter 2, were designed to be mounted within a shielded module case that mounts within a 3U VectorPak subrack. The maximum board dimensions for these boards were 4.500 inch high by 6.500 inch wide. For the 16-channel ECEI boards under development here, the intent is to fit these boards within shielded module cases that mount within a 6U VectorPack subrack, with maximum board dimensions of 9.187 inch high by 6.299 inch wide. A further constraint is that the boards should have the top and bottom 0.100 inch clear of any components or signal traces such that the boards can slide into the card guides installed into the subrack. Best is if the top and bottom of the boards are grounded on at least the backside of the board for enhanced shielding. Meeting these very tight space constraints dictated the use of a 4-layer FR4 board (with two inner metallic layers in addition to the two outer layers), as illustrated in Fig. 4.5. In KiCAD, the two inner layers are labeled In1 and In2. In our

design, the In1 layer was used primarily for power lines while the In2 layer was used for interconnecting traces which required crossing existing top and bottom layer traces. Signal lines were placed almost exclusively on the top layer to better connect to the top-level components as well as for ease of debugging (not possible to manually probe a trace that is buried within the board stack-up).

Fig. 4.5: 4-Layer Rigid PCB Stack-up for a 0.062 Inch FR4 Board

LAYER	MATERIAL	THICKNESS
1	Cu 0.5oz + Plated Cu	0.0021
	Prepreg 2113, No. of Pcs. = 1	0.0035
	Prepreg 2116, No. of Pcs. = 1	0.0040
2	Cu 1 oz	0.0014
	Core Thickness 0.040	0.0400
3	Cu 1 oz	0.0014
	Prepreg 2116, No. of Pcs. = 1	0.0040
	Prepreg 2113, No. of Pcs. = 1	0.0035
4	Cu 0.5oz + Plated Cu	0.0021
	TOTAL THICKNESS	0.0620

The RJ45 power connector and the VHDCI output connector should be located at the front of the module (right board edge in KiCAD) so that cables can easily connect to the module. The module will have an aluminum front panel (not in the scope of this thesis) to which the board is attached, with the connectors protruding through the front panel. Likewise, the trimmers that control the IF attenuation and DC offset voltage for each channel should also be placed at the front of the module (right board edge in KiCAD) so allow access via a precision screwdriver whose tip can be inserted through small holes in the front panel aligned with each trimmer. Note that this requires all trimmers to be side adjustment rather than top adjustment, as the top of the trimmer would be unavailable when mounted within the shielded module case. The 120-pin input IF

connector, through which the companion RF board will mount and connect to the IF board, should be located near the back of the module (left side in KiCAD) and on the back side of the PCB such that the two boards mount back-to-back. The exact distance between the 120-pin connector and the right board edge needs to be identical for both the IF and RF boards to ensure the RF board will fit within the module and the SMA input connector of the RF board is mounted to the same front panel as the IF board.

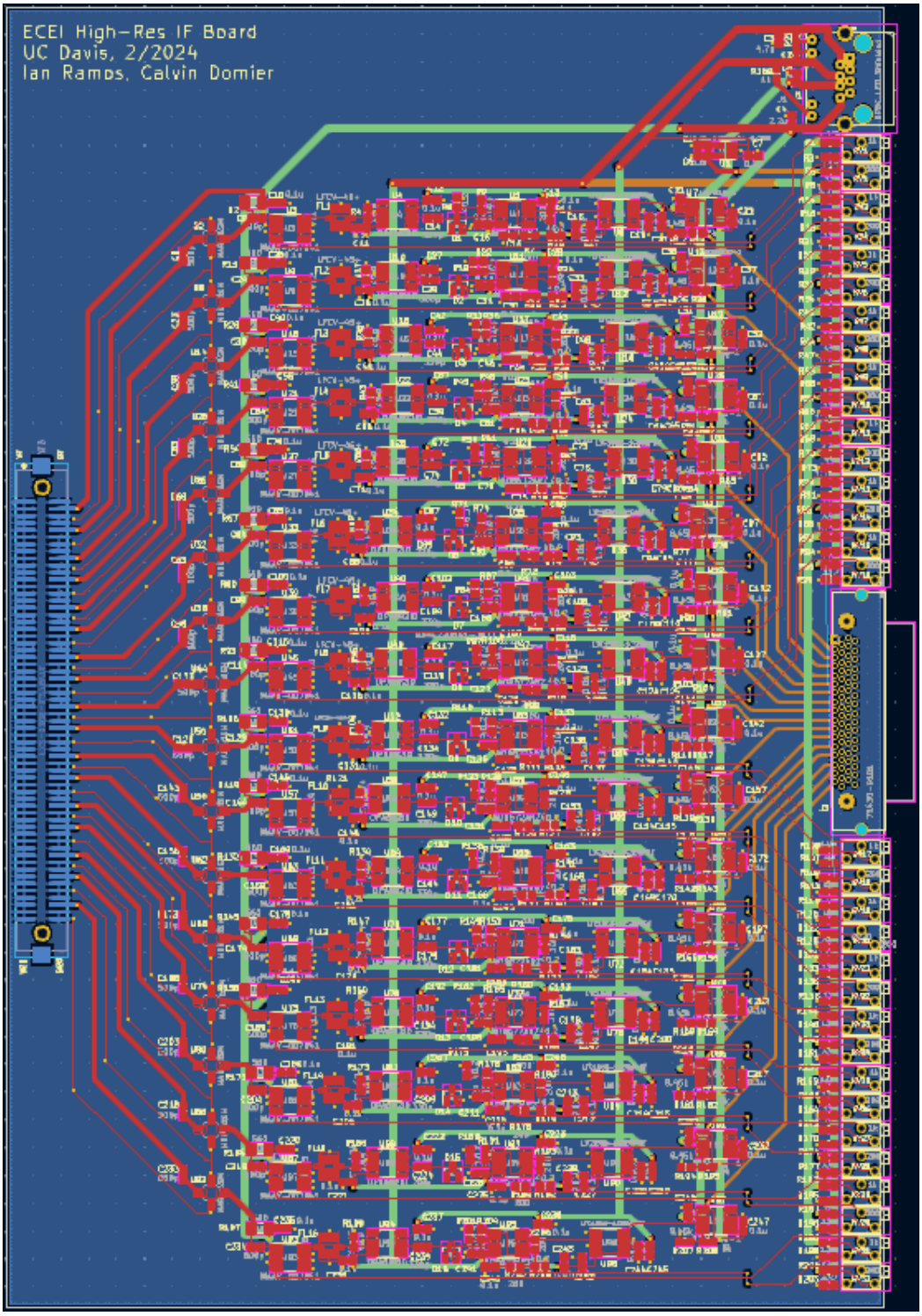
The first step in the PCB layout process was to assign footprints to each of the components in the schematic design. While most of the components are industry standard and already located in the KiCAD libraries, some were not. For footprints like the input and output connector, they were installed from vendor websites such as Digikey. For Mini-Circuits components like the LFCV-45+ and MAR6SM, we had to make sure the pads and pad arrangements match with their respective data sheets. 0603 footprints were assigned to nearly all capacitors and resistors. One exception was the DC biasing resistor required by the MAR6SM amplifier in which its power handling rating of 100 mW was insufficient to handle the heat generated within the resistor. We calculated the power by multiplying the operating current (16 mW) and voltage drop (12 V - 3.5 V) from the data sheet, yielding 136 mW. Here, a larger 1206 footprint (250 mW) was chosen to provide a sufficient safety margin. Through-hole trimmers were chosen rather than surface-mount to increase their adhesion to the PCB and better withstand the forces that could be exerted by the screwdriver when adjusting the trimmer wiper position. Through-hole versions of the RJ45 power connector and the VHDCI output connector were also similarly chosen.

As was the case with the detector board, power line bypass capacitors were placed near active components. Where available, hand-soldering footprints were chosen over machine-

soldering footprints as their larger areas were much more conducive for the hand soldering that was performed with this prototype board.

The PCB layout of the IF board is presented in Fig. 4.6. The board is 9.184 inch high by 6.194 inch wide, within the space constraints discussed earlier. From the input connector through the attenuator to the RF amplifier, a track width of 30 mils was used with 15-mil ground traces run between each of the signal lines to minimize cross-talk between adjacent channels. Top level signal traces after that were generally maintained at 15 mils, while In2 interconnecting traces between the output OPAs and the output connector were 24 mils. Vertically-aligned In1 power line traces were 60 mils wide, falling to 30 mils for horizontally aligned traces connecting to individual components. All traces (including the ground pour) are kept at least 14 mil from the edge cut layer, to meet the ≥12 mil requirement by the PCB manufacturer.

Fig. 4.6: IF Circuit Board in PCB Editor



Photographs of the populated IF board are provided in Figs. 4.7 and 4.8. Soldering for the IF board was straightforward as we first soldered the input connector, bigger chips such as the

amplifiers and filters, resistors and capacitors, power connector, trimmers, and then lastly the output connector. We soldered the 120 pins for the input connector in the back of the PCB as well as the pins for the power connector, trimmers, and 68 pin output connector. We realized that we chose the wrong footprint for the ADA amplifier resulting in incorrect pin assignments, so traces were cut and jumper wires installed to relocate signals to the appropriate pins. We also failed to extend the +3 V power line all the way down to channels 9-16, resulting in the need to manually jumper the power line on the board.

Fig. 4.7: Photograph of the Front Side of the Populated IF Circuit Board

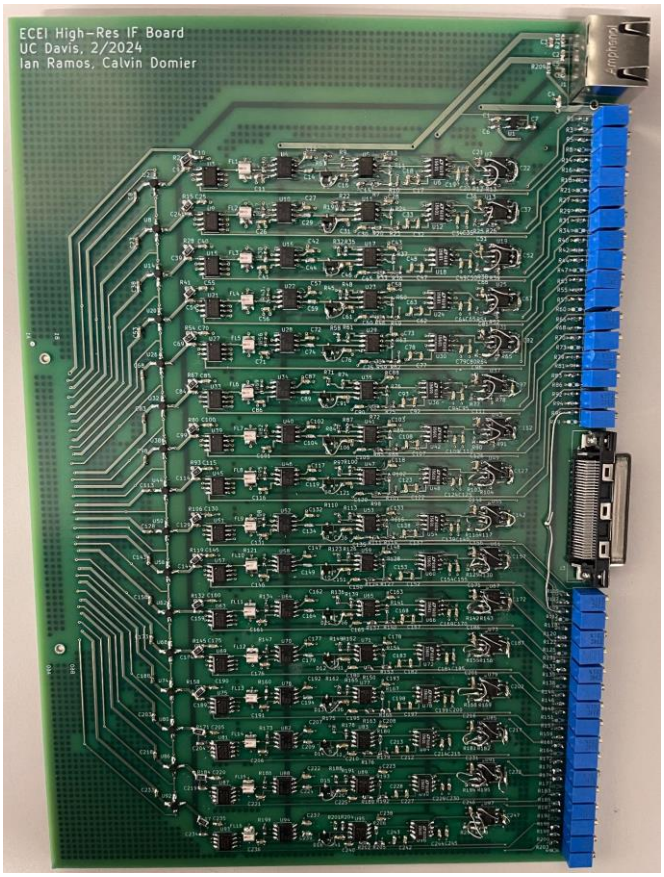


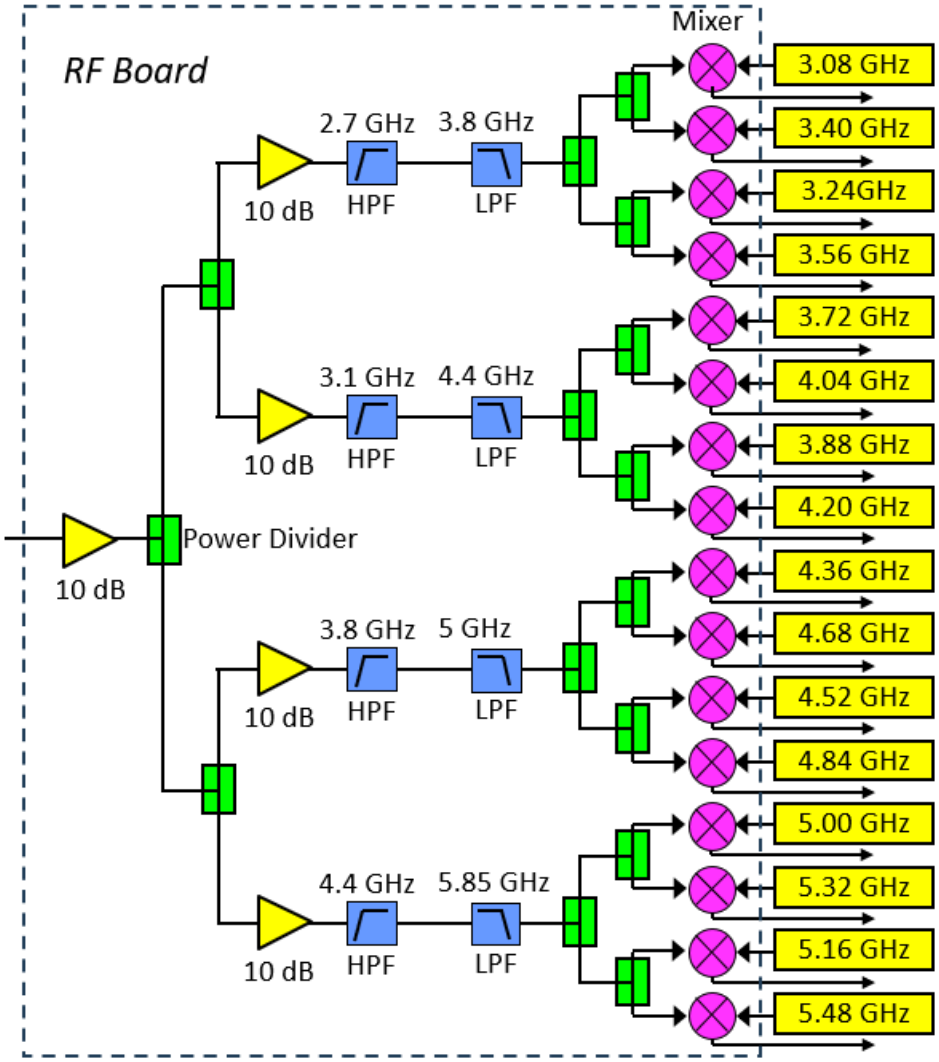
Fig. 4.8: Photograph of the Back Side of the Populated IF Circuit Board

Chapter 5: RF Board

5.1 Schematic Layout

A block diagram of the 16-channel RF board is provided in Fig. 5.1. RF signals in the range of 3.0 to 5.5 GHz enter the board via an SMA connector and are immediately amplified before connecting to two stages of power dividers to generate 4 equal signals. Each of these signals is amplified once more (providing both gain and isolation) and then propagated through a band pass filter, formed by a high pass filter followed by a low pass filter, yielding 4 reduced bandwidth sub-bands. Each of these sub-bands passes through another pair of power dividers to generate 4 equal signals that are input to 4 double balanced mixers. LO signals to the 16 mixers are generated on a separate LO board (see Chapter 6) ranging from 3.08 GHz to 5.48 GHz, with a channel spacing of 160 MHz. The down-converted outputs of each mixer are then directed to the companion IF board (see Chapter 4) for amplification and detection.

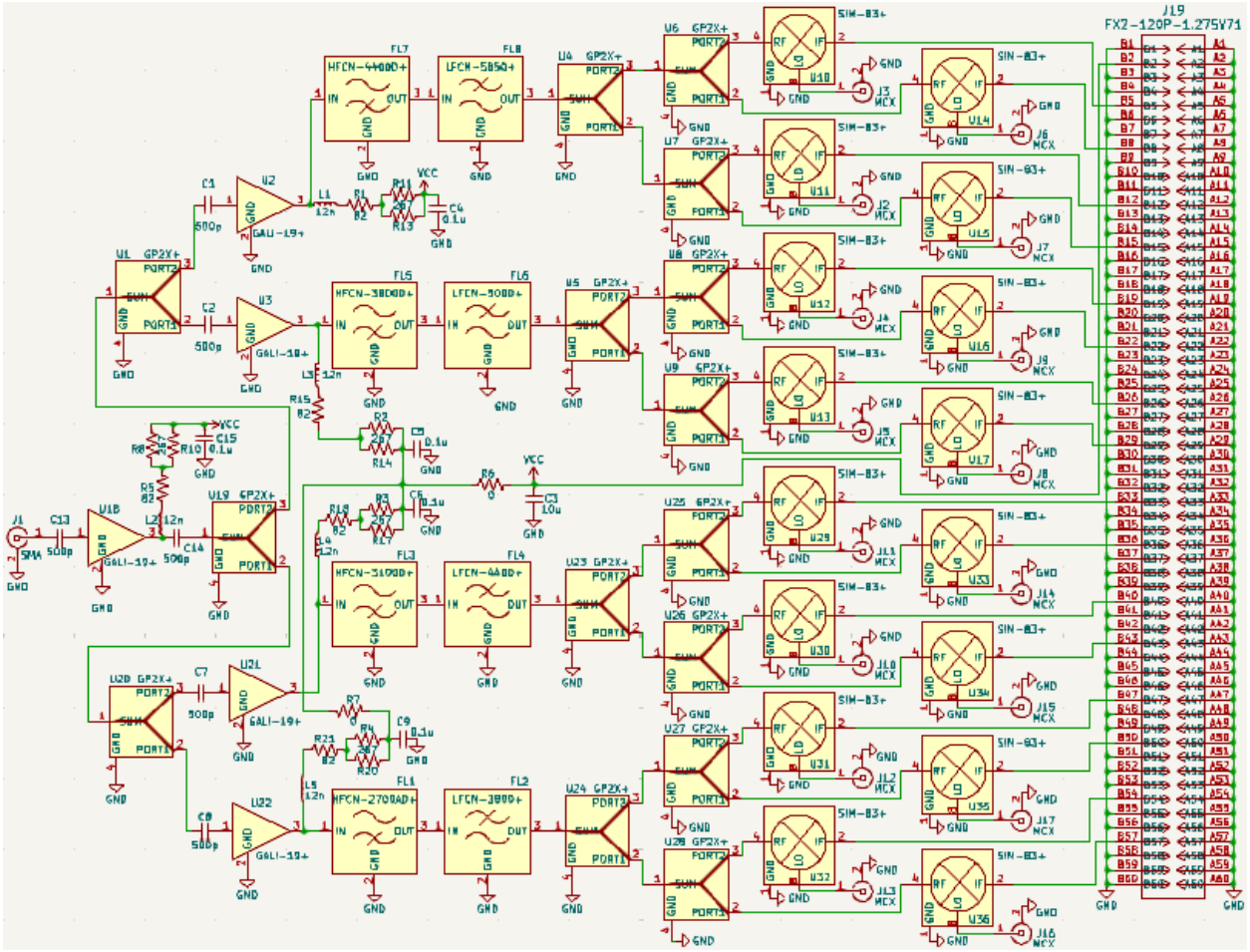
Fig. 5.1: Block Diagram of RF Board



A GALI-19+ amplifier (10 dB gain, DC to 7 GHz) is used for each amplifier stage. DC power is supplied to the amplifier through the output pin through a 12 nH inductor, 82 Ω resistor, and two resistors of 267 Ω in parallel due to microwave concepts and the amount of heat that the resistors can handle. The inductor acts as a low pass filter and stops the high pass frequencies going to resistors. It then connects to a power divider called GP2X+ which splits to two more of the same power divider from the output. The outputs of these power dividers would now connect to the same amplifier circuit and onto the high and low pass filters. The high pass filter was assembled first since it does not need DC and therefore does not need a capacitor between the

output of the amplifier and the input of the filter. Each of these filters go to another GP2X+ split to two more power dividers and their outputs to a mixer called SIM-83+ for the other board connections for a total of 16 mixers for 16 channels. The purpose of the frequency mixer is to shift signals from one frequency range to another. It also mixes the two input signals where the output signal frequency is the sum or difference frequency of inputs [4]. The IF pin flows onto the 120-pin output connector for the IF board. The local oscillator pin of the mixer would connect to a coaxial connector for the LO board, and the V_{cc} inside the circuit connect to two 0-Ω resistors with a capacitor to ground and to one channel of the output connector. In general, the amplifiers, low pass, and high pass filters are used to better isolate signals feeding each mixer.

Fig. 5.2: RF Board Schematic in Schematic Editor



We got 82 Ω after the amplifiers by starting at a high value where we ended up with 82 depending on the appropriate amount of power. Since the bias resistance for the amplifier is 215 Ω at 12 V, we found the difference between that and 82 Ω which was 133 Ω and doubled that to get around 267 Ω so two 267 Ω are in parallel. We chose 12 V because we will connect this board to the IF board which also uses a V_{cc} of 12 V. We also decided on the GP2X+ since we wanted a 2-way surface-mount 50 Ω splitter from at least 3000-5000 MHz. High and at least 20 dB of isolation was needed where this model seemed to be the easiest to solder. After the second set of amplifiers, we decided on the high and low pass filters depending on their frequencies for the RF board (Refer to the block diagram of the RF board). More specifically, at each set of low and high pass filters, there are four frequencies where we took the low-end and subtracted 0.08 GHz and the high-end and added 0.08 GHz where that range determines which high and low pass filters are needed. The range of frequencies for the 16 channels is essentially the RF bandwidth from about 3 to 5.56 GHz and 160 MHz of spacing. To add on, the 12 nH for the inductors from the 6 GHz (5.56 GHz) was chosen and chose the filters based on low cost, narrow frequency range, flat response, and high pass filters that do not short the DC. We stuck to the SIM-83+ mixer for the same reason as choosing the GP2X+ in that the RF and LO were from at least 3000-5000 MHz and needed high isolation for a small footprint to reduce the size of the board. We were also looking for a 7 dBm mixer and an IF range from at least 1-100 MHz for testing purposes. The V_{cc} inside the circuit would connect to a 0-Ω resistor because it will be useful for debugging when making tests. For the symbols, all the main components were edited to replicate with their data sheet except the resistors, inductors, and capacitors.

5.2 PCB Layout

The PCB setup was set up similarly with the schematic where it was diagonal and had the high frequency filters on top due to cable loss and the high frequency filters needing short wires. It was also diagonal due to the PCB length needing to be shorter. The footprint of the capacitors, resistors, inductors, amplifiers, and filters were found in the KiCAD libraries. The coaxial connector, power divider, and mixer were adjusted to match with the footprint layout on the data sheet or manufacturer site. We also installed the FX output connector footprint from Digikey. The 805 footprint capacitor was picked since it applies to the value of 10 μF and the 2512 resistor for 0 Ω for the ground plane. The 1206 footprint was for the 82 and 267 Ω resistors due to having a bigger resistor for power since there is increased power to 12 V. The Amphenol input was for the edge launch and the panel mount and chose the MCX vertical for the coaxial connector due to the internal 50 Ω impedance and through hole solder. The 0-Ω resistors would be placed in the back of the PCB to allow ground connection and power to be transmitted where it is in between the connection of the first power divider and top power divider. Consequently, the V_{CC} trace is outside of the board to connect to one of the top pins of the output connector and there are capacitors near the side of the amplifier. There is a 45-degree trace connection due to a 50 Ω transmission line with traces depending on the size of the pad. The excessive amount of ground thermal vias and front copper from the components are modeled from their PCB layouts and the coaxial connectors are 320 mils spaced apart from the middle. From the IF trace from the mixers and ground trace of the connector coaxials, they are spaced widely apart flowing to the output connector in the back. Again, we spaced the ground fill and edge cut layer border to 14 mils apart for the manufacturer. There is also a cost-efficient dielectric of 3.68 for ε_R, 0.0092 for the loss tangent, and a 20 mil dielectric thickness which is better for transmission line and microwave purposes. The board size

is 6122 mils in width and 4758 mils in height to connect with the IF board as well as considering the thickness of the RF board input connector which is 63 mils. We glued the components to the RF board starting with the IC components such as the amplifiers and filters and then came the mixers, resistors, capacitors, and the inductors. Next came the power dividers, Amphenol input connector, MCX connectors, and finally the FX output connector.

Fig. 5.3: RF Circuit Board in PCB Editor

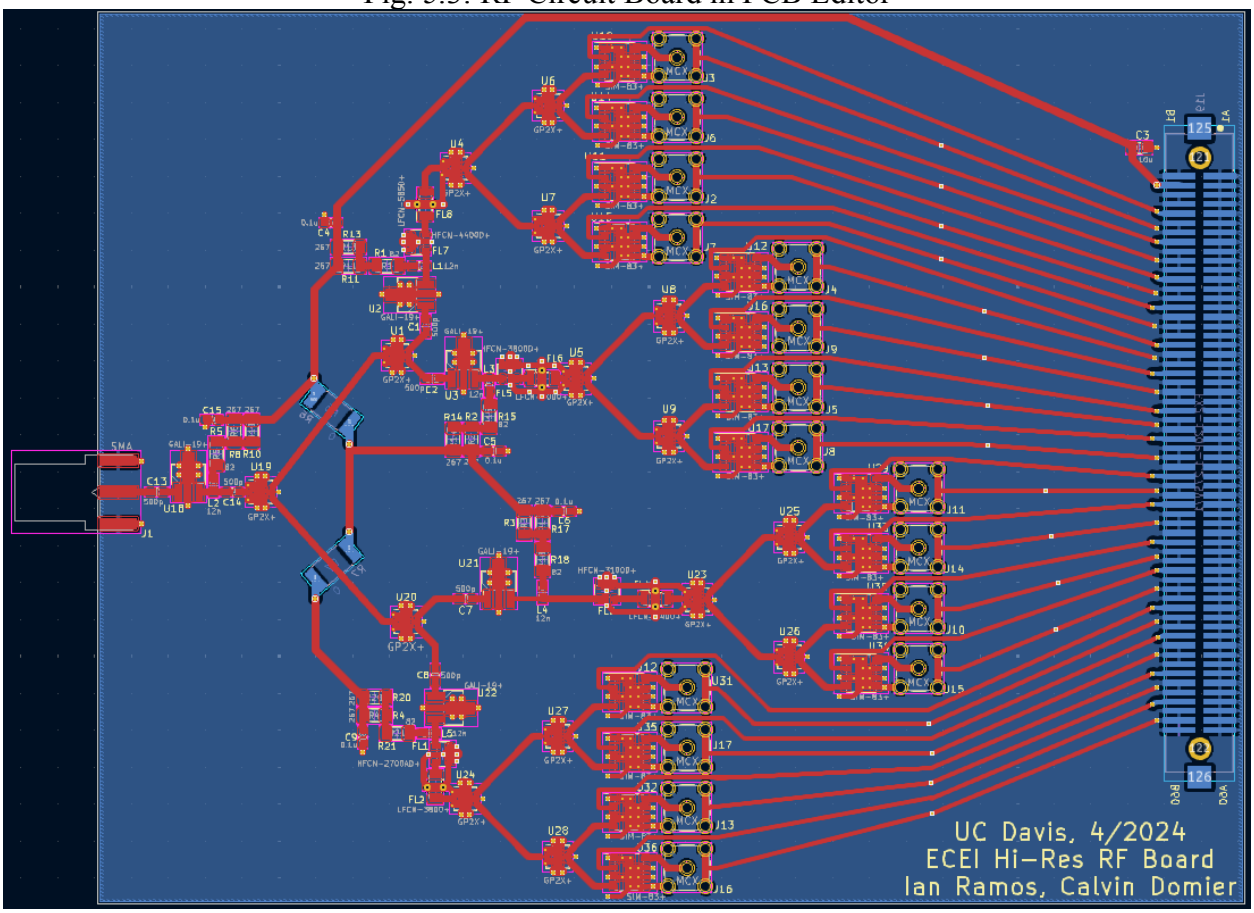


Fig. 5.4: RF Circuit (Front)

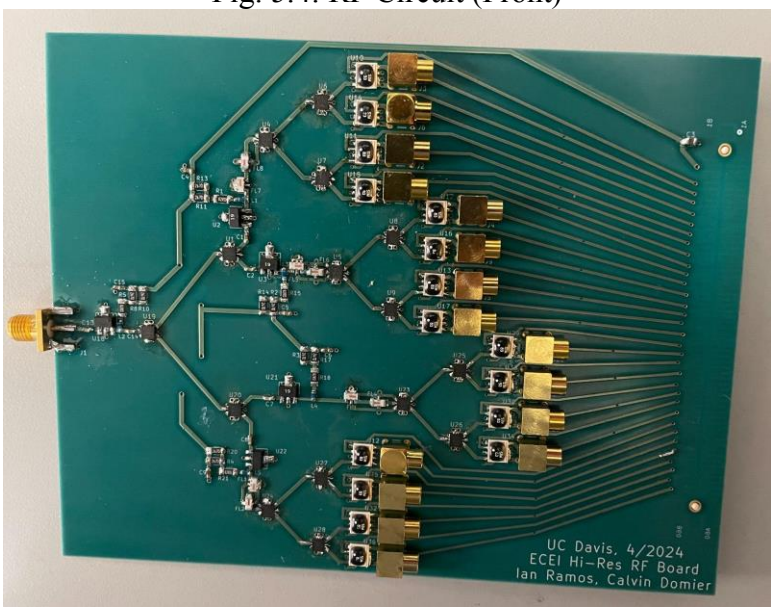
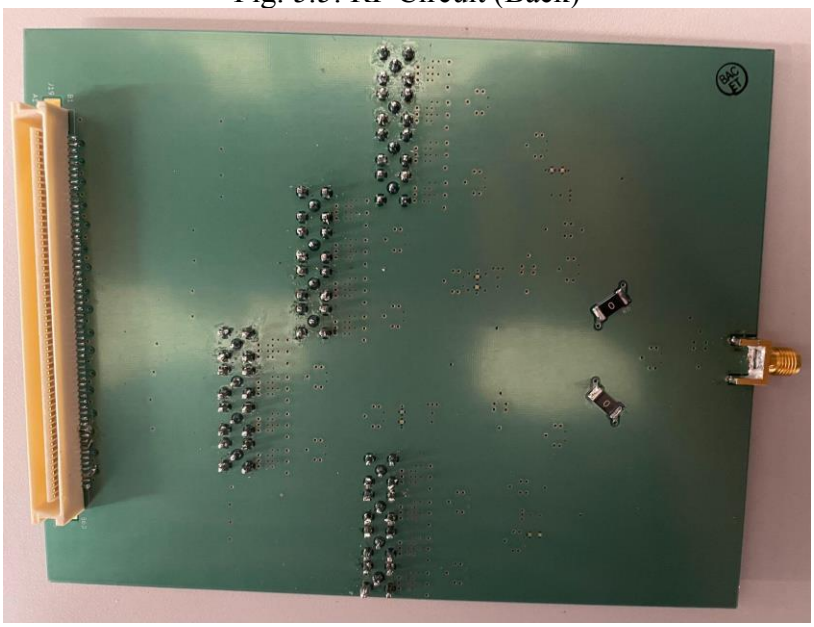


Fig. 5.5: RF Circuit (Back)



Chapter 6: LO Board

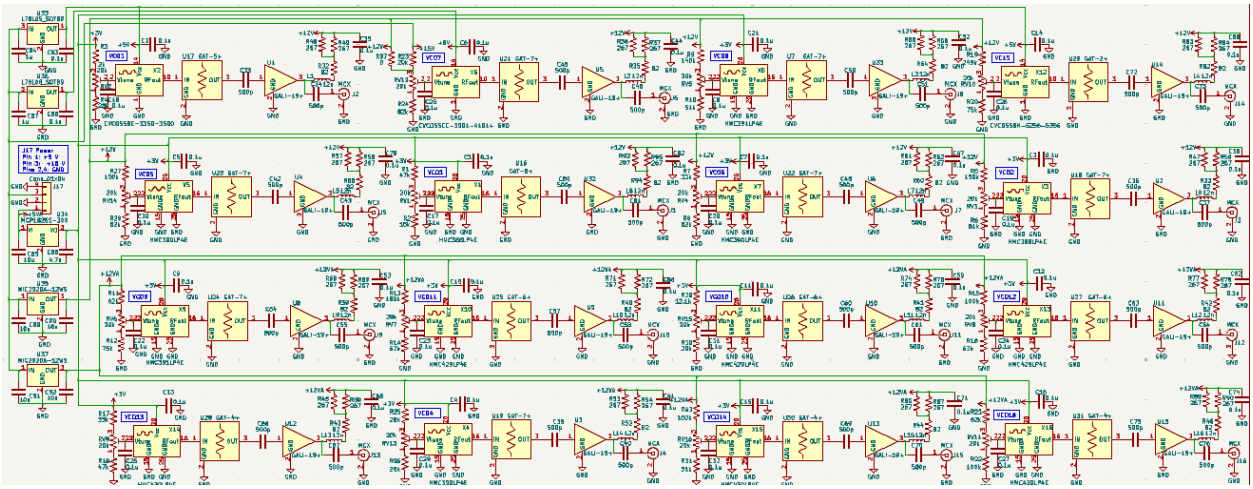
6.1 Schematic Layout

First, the inputs of the 5, 8, and 12 V regulators were connected for the 15 V power from pin 3 of a 1x4 connector. The input of the 3 V regulator connects to the 5 V power from pin 1

where we also added a +5VA flag to separate from the 5 V regulator and the +5V flag. The inputs then wire to their associated capacitors from their data sheets or to capacitors that were in the lab as well as ground, all to the outputs. We initially set the 20k-Ω resistor potentiometers with the calculated resistors with 3 or 12 V where we then connected it to a capacitor with each VCO chosen. The trimmers and resistors were connected together in order to tune the VCOs to the right frequency where too big of a tuning range in voltage would make it hard to adjust the trimmers to the correct voltage and too narrow could result in being unable to obtain the correct frequency. The VCOs could also potentially differ in their performance compared to the data sheet. The VCOs provide LO power to the individual frequency mixers which downconvert radiation to an IF from 5-100 MHz.

From the RF output comes the attenuator depending on the calculated attenuation to control the power level and distortion. It then goes through the GALI-19+ where there are block capacitors with a 12 nH inductor, 82 Ω resistor, and two resistors of 267 Ω in parallel. They now connect to the coaxial connector for the RF board and the outputs of the regulators connect to their corresponding Vccs from the VCOs with power lines. Also, placed two different 12 V flags for the first and bottom two rows to eliminate the error in the electrical rules checker and to dissociate the two 12 V regulator connections. We then made a text box mentioning the power and ground for the pins as well as the VCO and a number from 1-16 where 1 is the lowest and 16 is the highest VCO frequency. Overall, we made the schematic more compact horizontally with the VCOs at a 4 by 4 arrangement.

Fig. 6.1: LO Board Schematic in Schematic Editor



Before going over the specifications of the LO design, we decided to separate the LO board with the RF unlike the original design to enable improvement of multiple high-resolution radiometer boards where each board will have the same frequency channels. In other words, we are able to do and utilize multiple channels simultaneously and not create a larger board in size. We also want to explore the local oscillator frequencies and conduct experiments with small frequency spacing of 160 MHz apart compared to an adjustable 600-900 MHz like before.

For the current design, the voltage regulator provides a constant voltage to which each of the varactor input circuits connect. This is so that any change in the power supply voltage will not affect the VCO frequency. The regulators were based on the total current at each V_{cc} of the 16 VCOs. There was 435 mA for the 3 V, 40 mA for 5 V, and 30 mA for 8 V where we would choose regulators that cover more than the total amount of current. The 12 V regulators were also due to the amount of current where the first regulator was connected to the first two rows which have eight 40-mA amplifiers for a total of 320 mA and the same for the second regulator for the bottom two rows. We wanted to do this because this regulator was in the lab and each of these regulators can hold about 400 mA. Next, we found the maximum voltage drop for the regulators in order to

decide where the regulator inputs connect to on the power connector and how much power needs to be supplied. For the 3 V regulator, for example, the first step taken was finding the difference between the maximum continuous junction temperature (125 degrees C) and maximum ambient temperature (60 degrees C) and dividing by the thermal resistance from the junction to the ambient (29.3 degrees C per Watt) for a maximum allowable power dissipation of about 2.22 W. The last step was dividing the power by the total amount of current which was 435 mA, where there was a maximum voltage drop of about 5.1 V or 5 V from the input of the regulator to the power connector. The 5 and 8 V regulator had a maximum voltage drop of 45.45 and 60.61 V which is enough for a power of 15 V supplied as well as for the 12 V regulator.

We first decided which voltage controlled oscillators to use based on the original 16 frequencies from the RF board which are from 3.08-5.48 GHz. We decided based on low cost and in between good and narrow frequency range. For the design, we set the voltage with the calculated resistors to 3 V or V_{dd} = 3 V if the maximum voltage or nominal tuning voltage plus the varied voltage of the tune for V_{min} and V_{max} is less than 3 V. It is also 12 V if V_{max} or nominal tuning voltage plus the varied voltage of the tune for V_{min} and V_{max} is greater than or equal to 3 V. For the Analog Devices (HMC) VCOs, the V_{min} and V_{max} were determined by looking at the tuning voltage versus its specific frequency and spotting the minimum and maximum from the 85 and -40 degree C traces. For the Crystek Corporation (CVCO) VCOs, we looked at the nominal tuning voltage from the tuning curve at their specific frequencies. The varied voltage of the tune for V_{min} and V_{max} was determined by taking 10% of the nominal tuning voltage. 12 V was chosen because the highest nominal tuning voltage was 11.5 V. The GAT attenuators were used since we were searching for a surface-mount 50 Ω attenuator that was inexpensive and had no ground paddle since they are hard to hand solder.

To calculate each set of resistors, first determine the minimum voltage for the CVCOs by taking its nominal tuning voltage and subtracting by the varied voltage of the tune for V_{min} and V_{max}. For the maximum voltage, we added them instead of subtracting as mentioned earlier. Consequently, used a system of equations to solve the resistors using V_{dd} = 3V or 12V where the first equation was $V_{dd}(R_2/(R_1+R_2+20k\ \Omega)) = V_{min}$ and the second was $V_{dd}((R_2+20k\ \Omega)/(R_1+R_2+20k\ \Omega)) = V_{max}$ where R_1 was the top resistor connected to V_{dd} and R_2 was the bottom connected to ground. With the V_{min} and V_{max} determined already for the HMC VCOs, we used the same system of equations to solve the resistances. For VCO2, we connected R_1 to 15 V and in parallel to 0 Ω to 12 V due to the CVCO having a V_{max} of 12.65 V. With that being said, V_{dd} in this case is 15 V. The resistance values were rounded to resistors and resistor values in the lab and bought from Mouser. The attenuation was solved from the GAT attenuators by taking the output power from each of the VCOs, adding the gain based on the GALI-19+ looking at each of the VCO's frequency, and then subtracting by 8 dBm. We rounded the attenuation in dB down to the nearest whole number due to possible losses in the cables. That whole number determines which attenuator is used so if we got 7 dB, we would use a GAT-7+ attenuator.

The key symbols such as the VCOs, attenuators, and amplifiers were adjusted. More specifically, we rearranged the pin layout for the HMC to match with the layout from a previous design. We also changed the name of the coaxial connector symbols to MCX for specification and rearranged the CVCO VCOs to be in the first row of the board due to having a different supply voltage of 5 and 8 V which is why the 5 and 8 V regulator was on top as well.

Initially, there was thought of using the same low pass filters from the RF board to place after the VCOs to each of the LO signals to remove the second harmonic signals which in some

cases are as low as -7 dBc meaning 7 dB below that of the main output frequency. As a result, the difference in insertion loss is greater than 22 dB, and therefore no need for low pass filters.

Table 6.1: The table represents the low pass filters from the RF board and their insertion loss for the 16 channels from 3.08-5.48 GHz and double that frequency along with the difference in insertion loss.

LPF	Insertion Loss (dB at 25 deg C) at Frequency (GHz)	Insertion Loss (dB at 25 deg C) at Double Frequency (GHz)	Difference in Insertion Loss (dB)
LFCN-3800+	0.32 dB at 3.08 GHz	26.95 dB at 6.16 GHz	26.63
	0.32 dB at 3.24 GHz	25.79 dB at 6.48 GHz	25.47
	0.32-0.49 dB at 3.4 GHz	28.94 dB at 6.8 GHz	28.45-28.62
	0.49 dB at 3.56 GHz	33.34 dB at 7.12 GHz	32.85
LFCN-4400+	0.4 dB at 3.72 GHz	29.32 dB at 7.44 GHz	28.92
	0.53 dB at 3.88 GHz	32.78 dB at 7.76 GHz	32.35
	0.53 dB at 4.04 GHz	32.78 dB at 8.08 GHz	32.35
	0.53-0.61 dB at 4.2 GHz	34.39 dB at 8.4 GHz	33.78-33.86
LFCN-5000+	0.54 dB at 4.36 GHz	28.72 dB at 8.72 GHz	28.18
	0.89 dB at 4.52 GHz	29.19 dB at 9.04 GHz	28.3
	0.89 dB at 4.68 GHz	29.19 dB at 9.36 GHz	28.3
	0.89 dB at 4.84 GHz	27.96 dB at 9.68 GHz	27.07
LFCN-5850+	0.55 dB at 5 GHz	27.9 dB at 10 GHz	27.35
	0.55 dB at 5.16 GHz	27.9 dB at 10.32 GHz	27.35
	0.95 dB at 5.32 GHz	23.35 dB at 10.64 GHz	22.4
	0.95 dB at 5.48 GHz	23.35 dB at 10.96 GHz	22.4

6.2 PCB Layout

We assigned the 603 footprint capacitor and resistor for the varactor circuits and again the MCX vertical for the coaxial connector. For the 4.7 and 10 μF capacitors, a 805 footprint was used

for the high power and voltage. We ended up using the PVG5A footprint for the trimmer because of the large amount of turns on the physical trimmer knob which will give accuracy in setting it to the value desired. The HMC footprint is also installed from a previous design and used a 9 mil trace width line to connect two of the same pads next to each other for the HMC VCO and used one 24 mil trace width line to connect from in between the two same pads to their individual components.

The PL-126 footprint was modified for the attenuators which contains extra front copper and ground vias due to the component layout and in the PCB layout, the arrangement of footprints were also analogous to the schematic. In addition, the 3, 5, and 8 V regulator footprints were altered from their data sheets such as their pad shapes. The horizontal 40-mil trace width power lines of +3 V in the top and +12 V in the bottom of each row from the power connector and regulators will help in isolating pickup between the different LO signal channels. Front copper was used for +3 V and bottom for +12 V except that we used front copper in the bottom row for +12 V because we would have to use vias which will take up more board space. We also separate the voltage lines on the left side for the ground planes and power to go through, especially on the right side of the board. We then labeled the VCOs with VCO and its corresponding number using silkscreen text. Additionally, mounting holes were added on the sides of the board. We spaced the ground fill and edge cut layer border to 14 mils apart and like the RF board, there is a dielectric of 3.68 for ε_R, 0.0092 for the loss tangent, and a 20 mil dielectric thickness. The LO board is 6808 by 3428 mils in size and we soldered the LO board by beginning with IC components again like the regulators and amplifiers, then the attenuators, VCOs, resistors, capacitors, and inductors. We finished off soldering the trimmers, power connector in the back, and coaxial connectors in the back.

Fig. 6.2: LO Circuit Board in PCB Editor

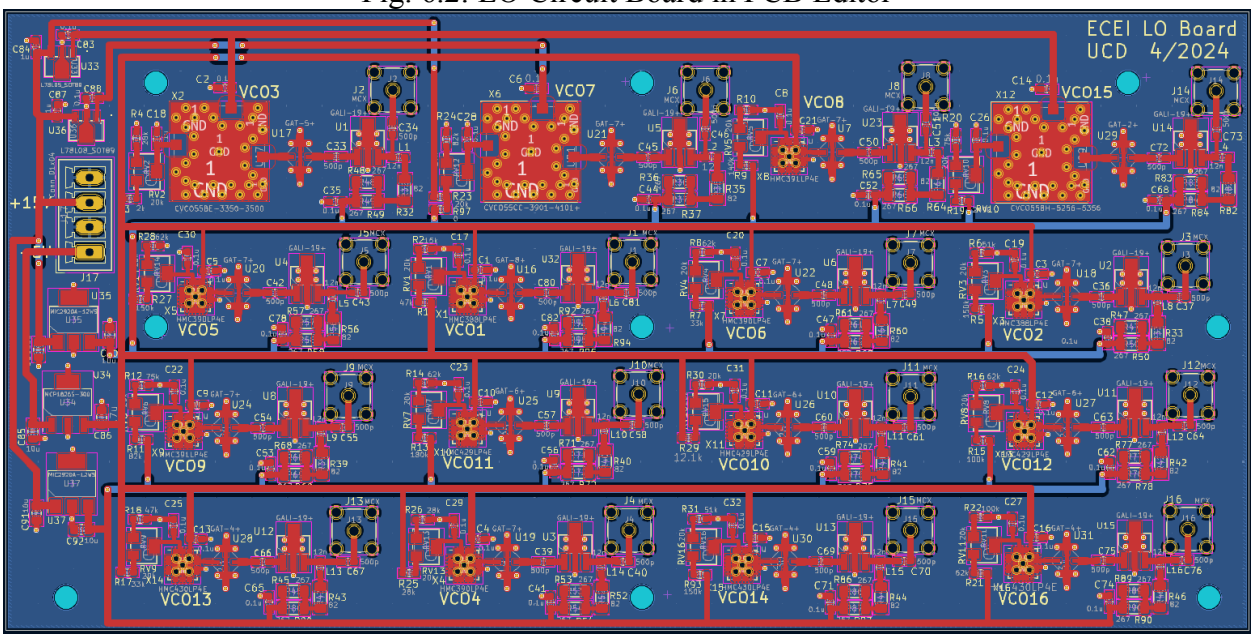
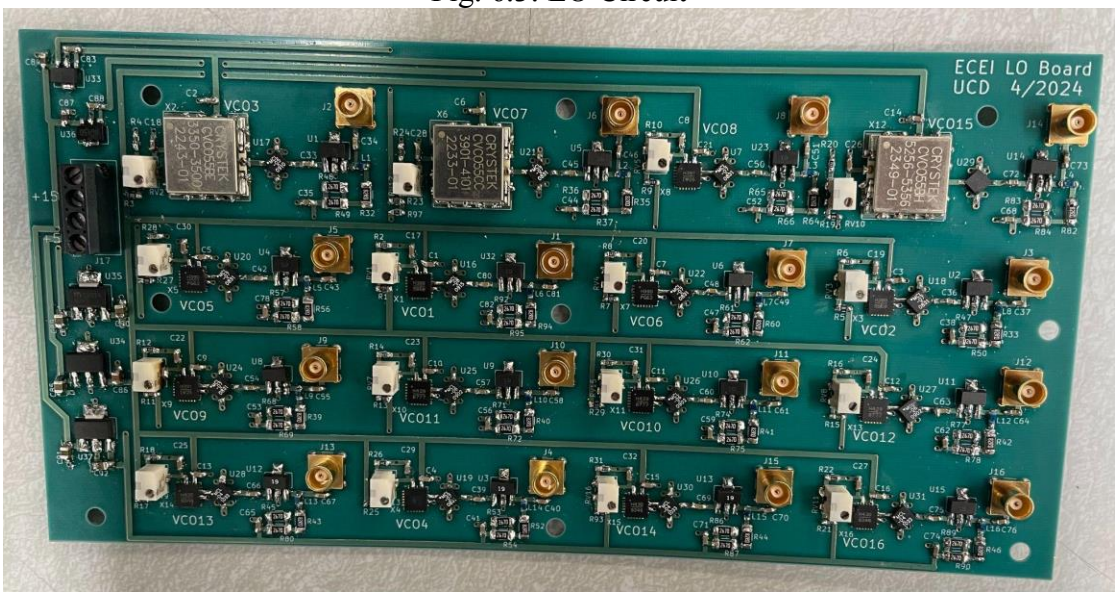


Fig. 6.3: LO Circuit



Chapter 7: Test Procedure and Results

7.1 Testing Board

7.1.1 Schematic/Design in KiCAD

A testing board was made to connect with the other boards and cables which includes the two different FX connectors used for the IF and RF board where the RF board FX connector was

flipped around the y-axis. The 16 input channels from each connector would connect to SMA connectors where we connected one channel of the IF board FX connector to +12 V and one channel of the RF board FX connector to no connection since we do not want to interfere with the V_{cc}. There is also a 1x8 connector to +12 V, -12 V, +5 V, and -5 V to a similar RJ45 power connector circuit with the resistors and capacitors. We then made two text boxes stating the power and ground for the pins and LEDs from the power connectors.

Fig. 7.1: Testing Board Schematic (Top Half) in Schematic Editor

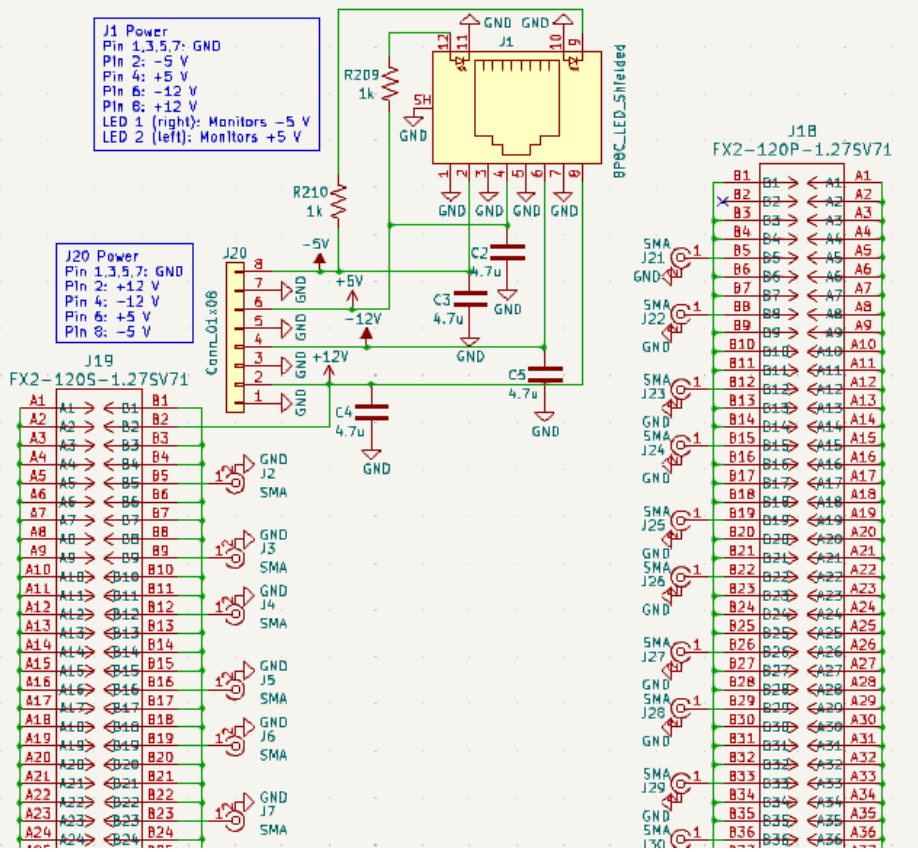
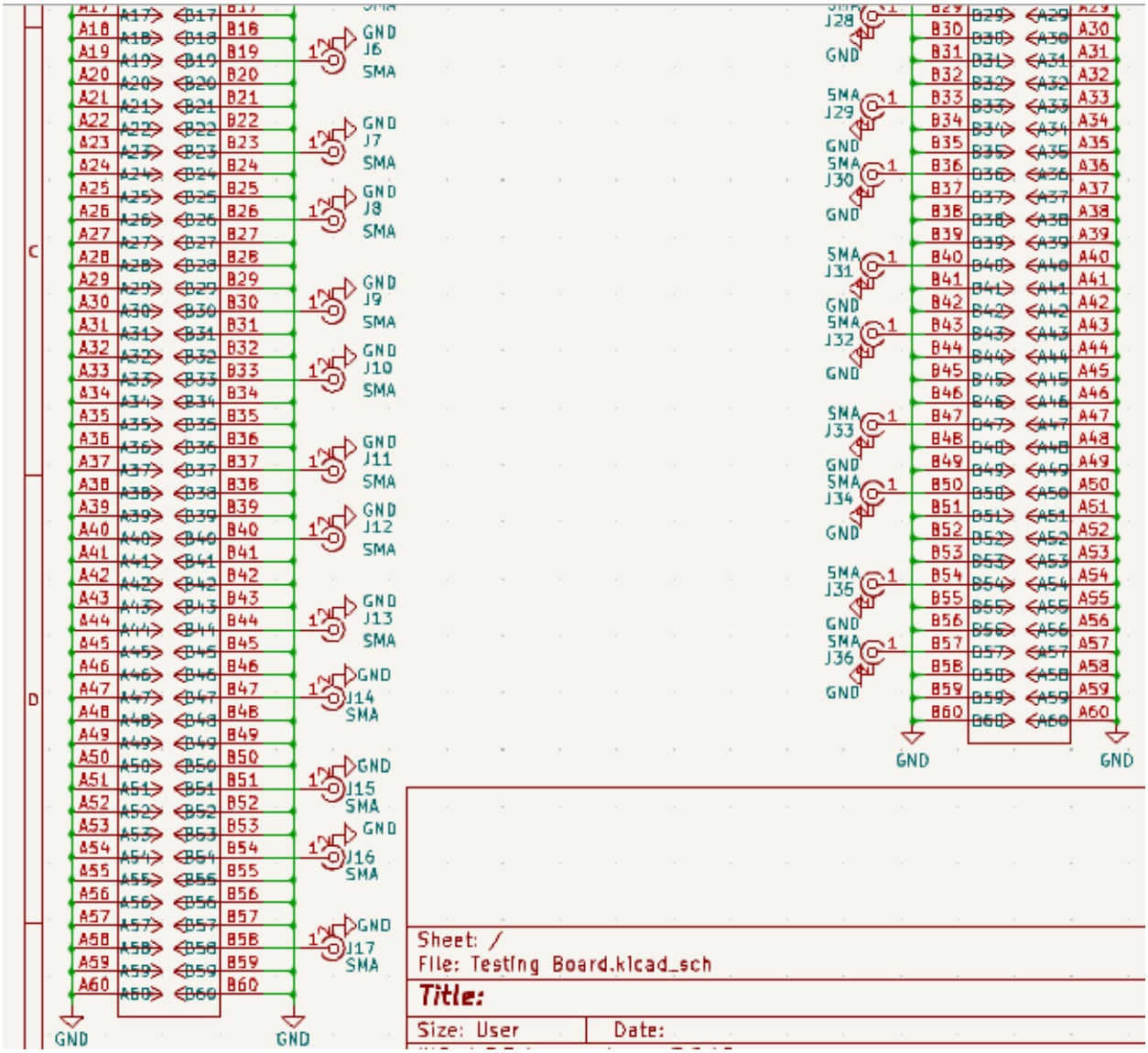


Fig. 7.2: Testing Board Schematic (Bottom Half) in Schematic Editor



7.1.2 PCB Layout

For the PCB design, we placed the RF board FX connector on the back of the PCB and connected the FX connectors to the SMAs by first using bottom copper of 34 mils due to the constraint to a via to the SMAs with front copper. The SMAs are 500 mils spaced apart from the middle in the x direction in rows of 3, with space in the y direction going down to prioritize connecting the first and third SMA for each row so that the connection is horizontal. We then

connected the RJ45 power connector circuit similar to the IF board but with the 4.7 µF capacitor with the 805 footprint for the +/- 12 V due to shielding, where the power lines were 40 mils of trace width. We labeled the ground and power with silkscreen next to the 1x8 connector and labeled a similar description for the RJ45 power connector from the schematic. Lastly, we made sure the references were in an open space and that the ground and edge cut layer were 14 mils apart. Other options are that we used standard 2-layer dielectric for FR4 and added two mounting holes where the board is non-plated. For the physical board, we soldered the resistors and capacitors as well as the FX connectors for the back of the PCB.

Fig. 7.3: Testing Board in PCB Editor

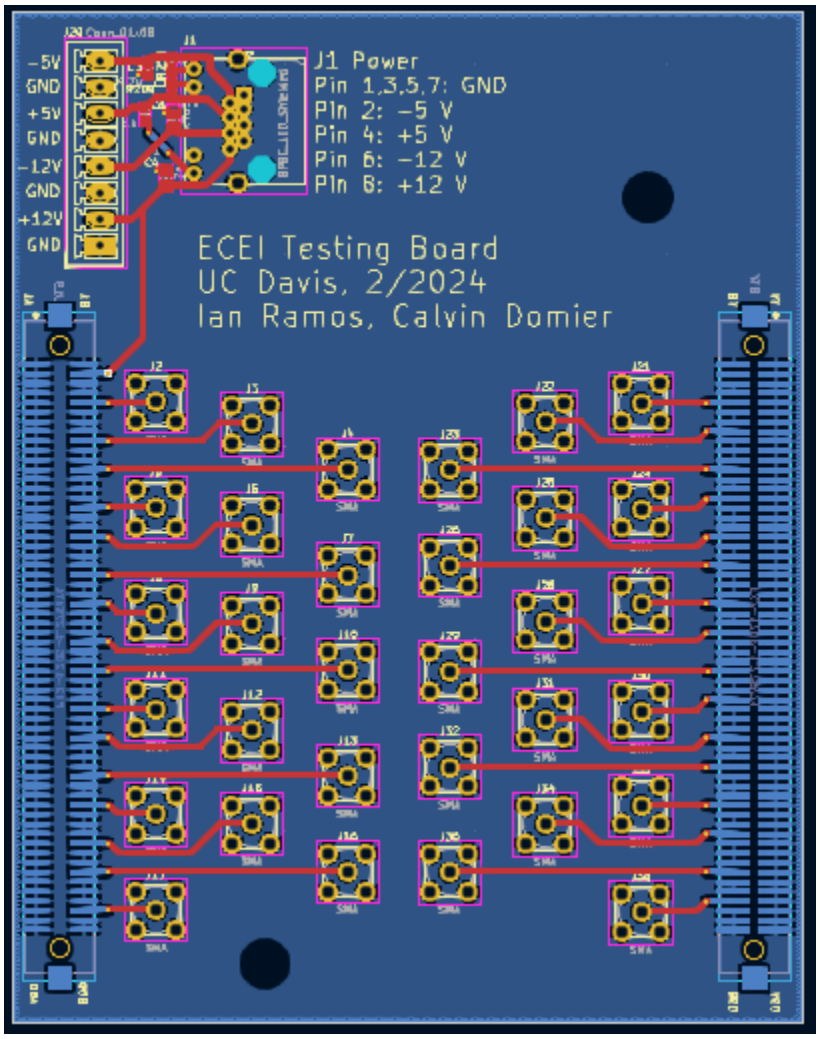
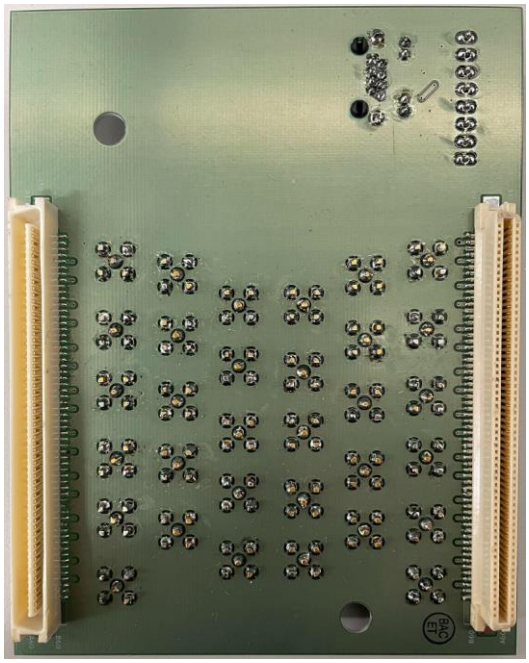


Fig. 7.4: Testing Board (Front)

Fig. 7.5: Testing Board (Back)



7.2 IF Board Measurements

Before setting up the testing for the major results, the currents were measured from the power supplies for the 16 channels to verify that the currents are equally distributed for each of the channels where we also set the current limits. There is a supply current of 40 mA per channel (5.1 + 3.5 + 29 + 2 from the components) for the -5 V line. Some extra draw will occur on the OPA depending on how much voltage/current gets delivered to the detector diode, so we assumed that there was about 44 mA per channel. Multiplied by 16, we obtain 704 mA where we then added 20% and this increases to 1.20 x 704 = 845 mA. Consequently, the current limit for the -5 V line is set to 845 mA. For the +5 V line, we added the current required by the +3 V regulator that drives the trimmer circuits. This means adding about 50 mA (3000 mV / 64 Ω (resistance of the 3 V line) = 47 mA) to make the current limit for the +5 V line at 895 mA. The total currents for each power in the power supplies is shown in Fig 7.7.

Throughout the IF testing, the major problem of some channels not getting the accurate results were adding too much or lack of solder on all the components, which meant that there was little to no voltage or resistance at those components. There were also some components that were burnt or broken where we had to replace them. Below is the overall schematic and picture for the board with the essential equipment.

Fig. 7.6: Schematic Diagram of the IF Board Instrument Setup

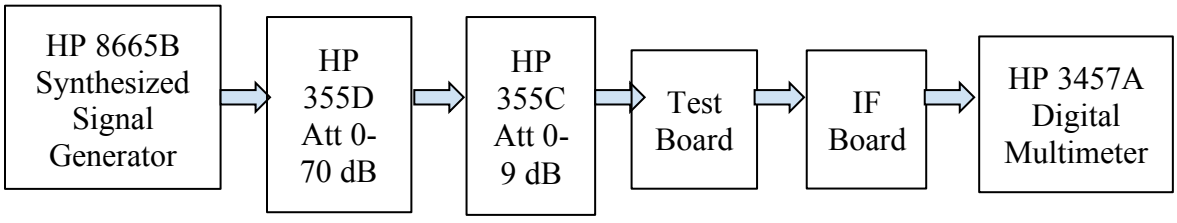
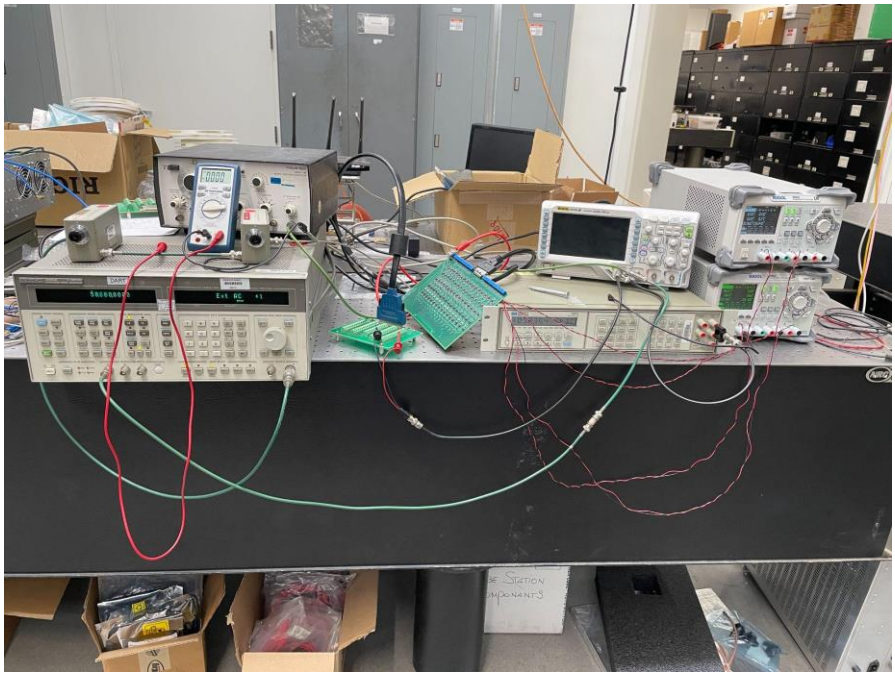


Fig. 7.7: Photograph of the IF Board Instrument Setup



First, we observed and confirmed that the DC voltage is around -2.45 V for the digitizer from the multimeter. We initially connected the output FX connector of the testing board on the back of the IF board where the input FX connector is. The ethernet cable was then connected from the IF to the testing board and connected all the voltages and ground from the testing board power connector to now two of the same power supplies as before for +/- 12 V. The input of this procedure is not currently used, but connected to an SMA cable from the first SMA of the testing board that sides where the FX connectors connect to the attenuators like the detector circuit. For the output, a low voltage computer cable was used for the 68-pin output connector onto an adapter to a board with power connectors. The connectors are hooked onto wires with the signal and ground lead to the multimeter and the purpose of this is to connect the individual channel output pins from the board to the same pins of that board so we can test individual channels.

Due to the circuit providing only around 1.2-1.5 VDC, we eliminated the bottom 332 Ω to the trimmer and changed the other 332 Ω resistor to 120 Ω. This is because the trimmer needs less

resistance and a resistance less than 240.2 Ω from the 40.2 Ω offset and 200 Ω. Hence, we were able to tune the trimmer for the DC offset to attain around -2.45 V and recorded the minimum and maximum DC voltage as shown in the chart.

Table 7.1: The table presents the range of the smallest and largest voltage at each channel from the trimmer or DC offset.

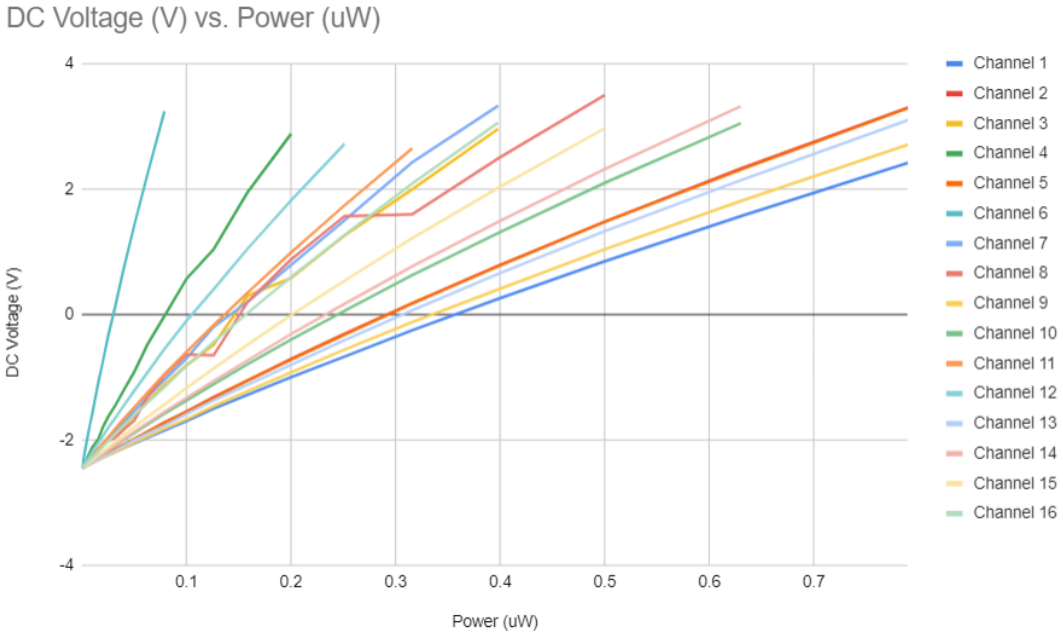
Channel #	DC Offset Minimum DC Voltage (V)	DC Offset Maximum DC Voltage (V)
1	-2.93	-1.78
2	-2.97	-1.8
3	-3.01	-1.86
4	-3	-1.85
5	-2.98	-1.8
6	-3.08	-1.95
7	-2.96	-1.83
8	-3.06	-1.9
9	-3.11	-1.96
10	-3.04	-1.88
11	-2.89	-1.71
12	-3.07	-1.91
13	-2.87	-1.72
14	-3	-1.85
15	-2.96	-1.82
16	-2.87	-1.71

Then, for each channel we set the control voltage to -2.3 V which was measured from the voltmeter probing the control voltage pin from the attenuator and ground while tuning the associated trimmer. The reason to do this is to provide as much signal and power through the attenuator before the detector and it corresponds to the smallest attenuation. Turning the trimmer

knob clockwise would decrease control voltage and would go as low as around -2.3 V where the trimmer starts clicking around that voltage.

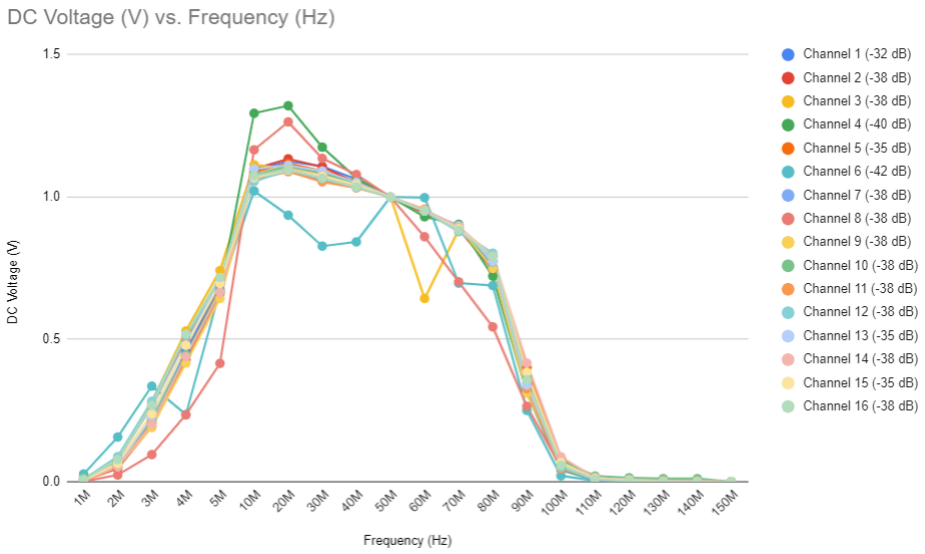
The diode was also reversed where pin 1 is now ground and pin 2 is not connected before producing results for the power (attenuation) versus DC voltage. When making initial tests of increasing attenuation, the voltage was decreasing which is opposite of what we want which is from -2.45 to around 2.5 or 3 V. We desire to run this test to determine how linear the detector response is. Furthermore, the attenuators and signal generator were hooked up like the detector circuit tests where we set the center frequency to 50 MHz, 10% AM depth, and RF of +10 dBm. Like the output connection, we connected an SMA wire from the RF source and attenuation to the individual SMA connectors on the test board that correspond to the individual channel input pins.

Fig. 7.8: The plot shows power in µW translated from attenuation against voltage DC for the 16 channels of the IF board. We located the attenuation at -2.4 V and increased it until we reached around 2.5 V. The total attenuation is calculated by 10 dBm from the RF minus the values from the attenuators.



With the same setup, we also did a frequency scan from 1-150 MHz due to voltages of -2.45 to somewhere less than 2.5 V where we made sure they were in this range by setting the attenuator to appropriate values where the voltage does not go at least 2.5 V. For the results, the data was normalized by adding the voltage at 150 MHz to all the voltages at the frequency points and dividing all the voltages by the voltage at 50 MHz to graph. Please refer to the following figure.

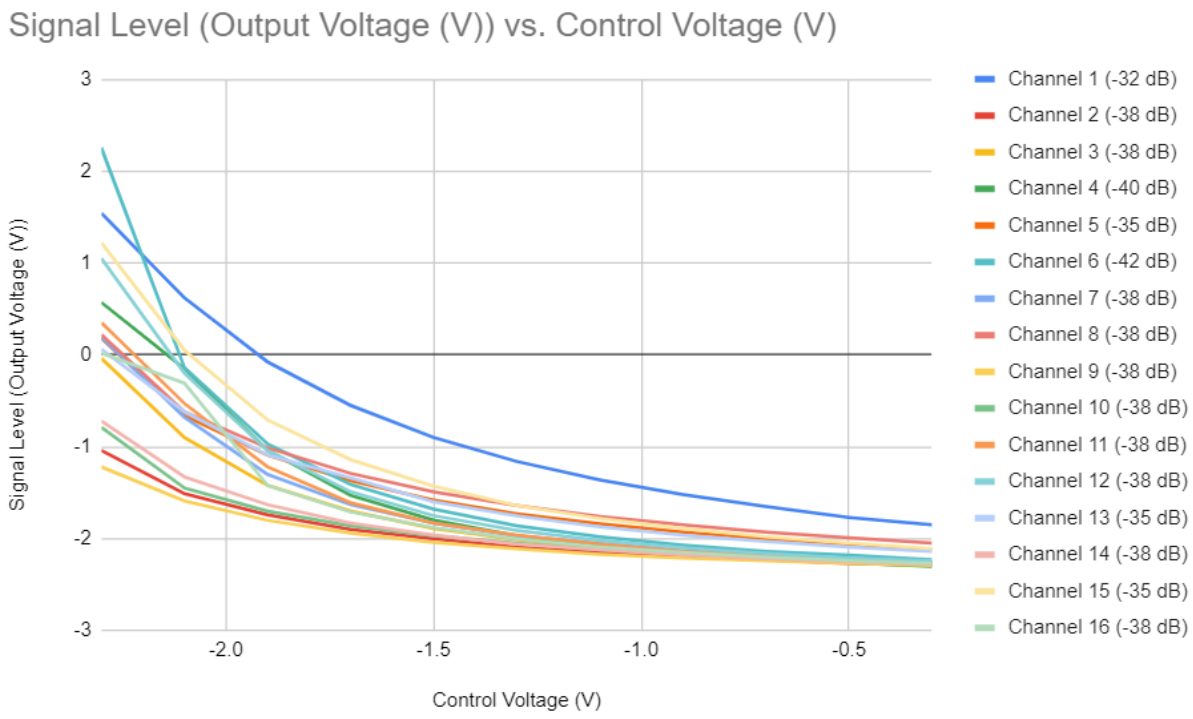
Fig. 7.9: Here is the frequency versus the normalized voltage response at attenuations where the voltage did not exceed 2.5 V. The range of frequency is determined by testing from 5-100 MHz where we would also check what happens below 5 MHz and over 100 MHz. As seen, the voltage is 1 V at 50 MHz and at 1 MHz and 100-150 MHz, the voltage is near 0 V.



The final testing was comparing the DC control voltage and signal level of the output voltage at 50 MHz and the same attenuation as seen in Fig 7.2.5. Similar to setting the control voltage to -2.3 V, we were able to tune the trimmer at control voltages from the voltmeter. The output voltage reading was recorded from the multimeter and again, the output voltages should be below 2.5 V. The control voltage scan allows calibrated curves of the attenuator response which

is significant in plasma so that we know the control voltage needed to reach a certain amount of attenuation. Lastly, we set the control voltage back to -2.3 V.

Fig. 7.10: Last but not least, the graphs portray the voltage output in comparison to the control voltage. The control voltage scale was determined from the attenuation versus control voltage plot from the MAAV-007941 attenuator datasheet where the control voltage went up to near -0.3 V.



7.3 RF Board Measurements

The RF board testing was performed after the LO board testing so we can use the LO board to test the RF board. Again, we inserted the current limits for the 12 V power for the amplifiers in the RF board and the 5 and 15 V power line from the LO. We obtained a current limit of 522 mA for the 5 V line and 852 mA for the 15 V line (see page 72-73 for the explanation). For the 12 V line, there are 5 amplifiers with 40 mA of operating current each for a total of 200 mA and multiplied by 1.2 to obtain 240 mA for the current limit.

The issues for the RF board and testing were from the complex soldering to the mixers and power dividers where we had to line up the power dividers on the board as precisely as possible and make sure the ground paddles were placed and configured properly. Hence, the RF board output would connect to the test board where the 12 V line is to the power connector. Similar to the IF board, there is an SMA cable from the SMA connector of the test board for individual VCO channels from the LO board to a bias tee for the mixers due to no capacitors onto the spectrum analyzer. Since we placed the smaller frequencies for the low and high pass filters in the bottom of the RF board, the SMA connector for VCO1 is in the bottom row of the test board and going up to the top of the test board would be VCO2-VCO16. The Amphenol input from the RF board goes to the HP 8491B and A 20 dB fixed attenuator for a high frequency range directly to the signal generator. Finally, like the SMA connectors for VCO1-16, the MCX connector from VCO1 of the LO board would connect to the very bottom MCX connector of the RF board where VCO2-16 follows as we work our way up the RF board. Shown is the block diagram and photo of the instrument system.

Fig. 7.11: Schematic Diagram of the RF Board Instrument Setup

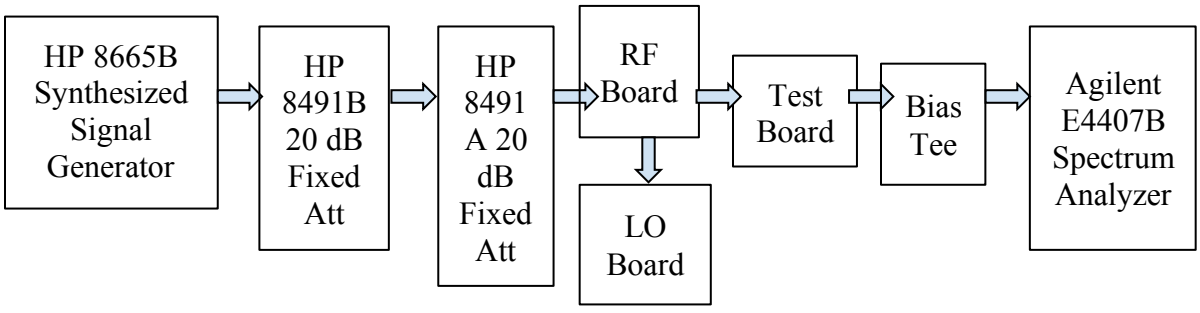


Fig. 7.12: Photograph of the RF Board Instrument Setup

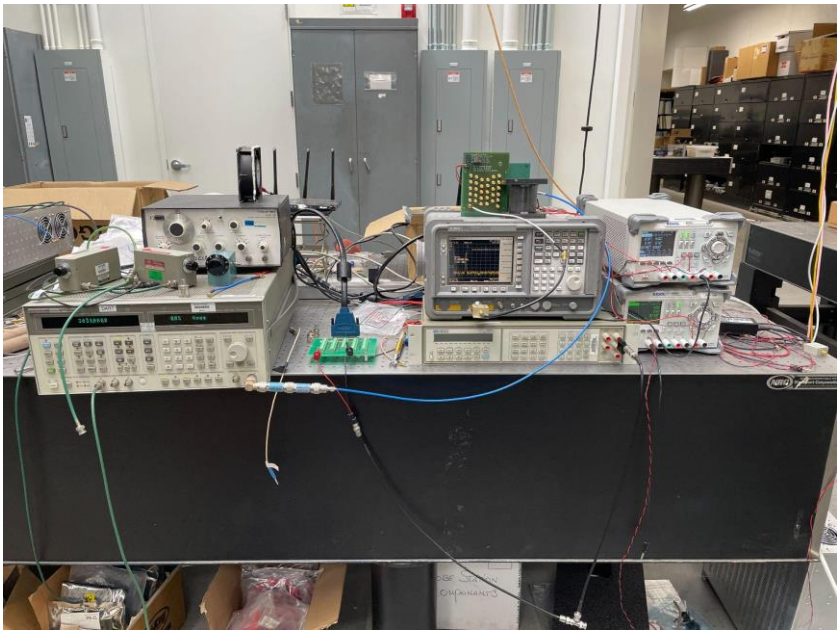
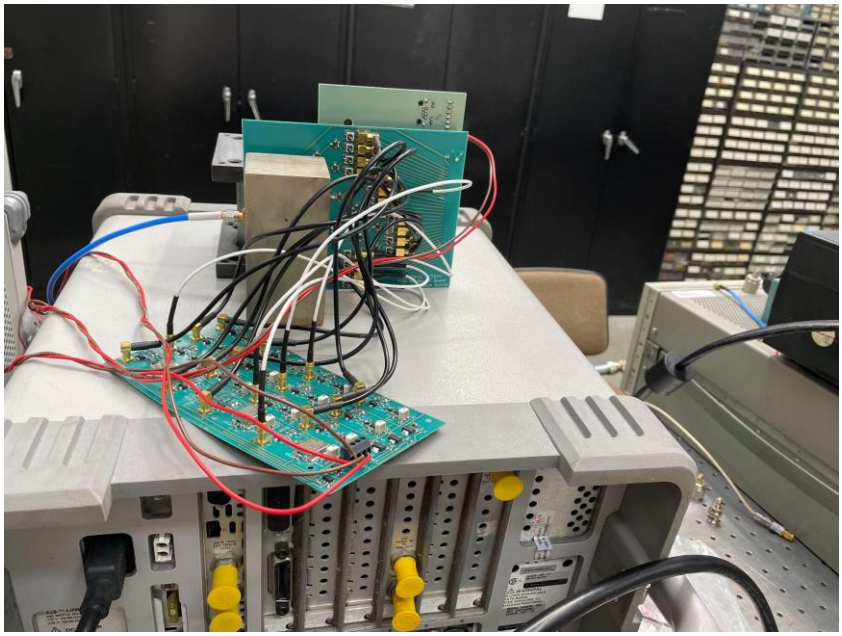


Fig. 7.13: RF Board Connected to LO Board with MCX Cables



The experiment is designed to determine a large steady power or dBm peak due to the VCOs and the RF frequency from the signal generator. This will confirm that the RF board is functioning properly and obtains as much power as possible. We determined the RF frequency

source by taking each VCO frequency and subtracting and adding 50 MHz. For example, for VCO1 which has 3.08 GHz, the RF frequency used is 3.03 and 3.13 GHz to collect the dBm peak at those frequencies. Furthermore, for VCO1 after connecting its SMA connector from the test board, turning on the 5 and 15 V power, adjusting the 3.03 GHz on the signal generator with no modulation frequency but with 10 dBm for a total of -30 dBm, and turning on the 12 V power, we turned on the RF to note the peak from the spectrum analyzer and then increased the frequency to 3.13 GHz to again note the peak. We would then turn off the RF and then the 12 V power and repeat for the next VCO channels. An example of how to determine the peak at frequencies is in the next two figures as well as a table of the peak at various VCOs and RF frequencies.

Fig. 7.14: The spectrum analyzer for VCO1 presents around 50 MHz versus the dBm peak around -41.89 dBm for 3.03 GHz. In order to locate the peak, we pressed the “Peak Search” button.

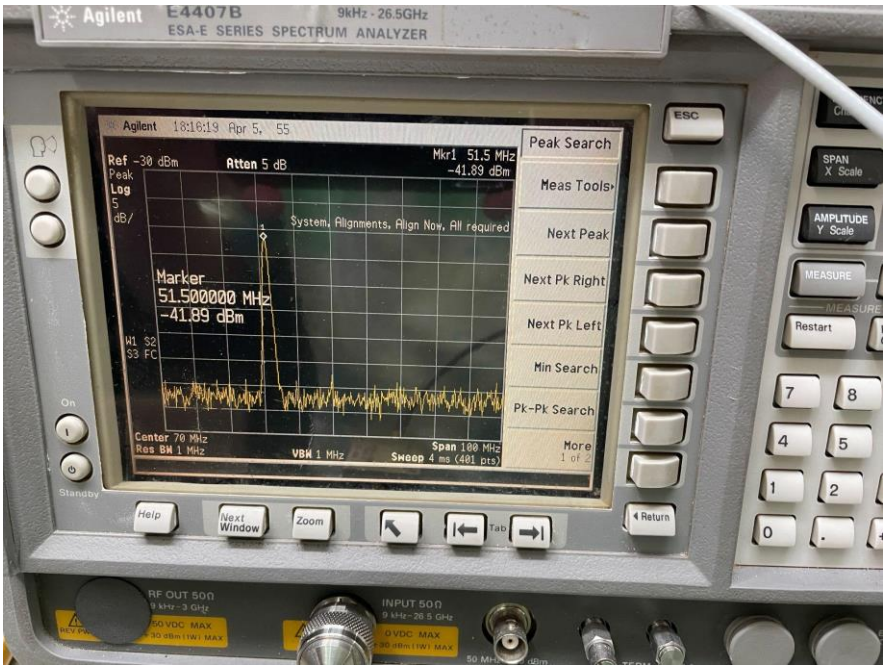


Fig. 7.15: The spectrum analyzer for VCO1 presents around 50 MHz versus the dBm peak around -42.12 dBm for 3.13 GHz.

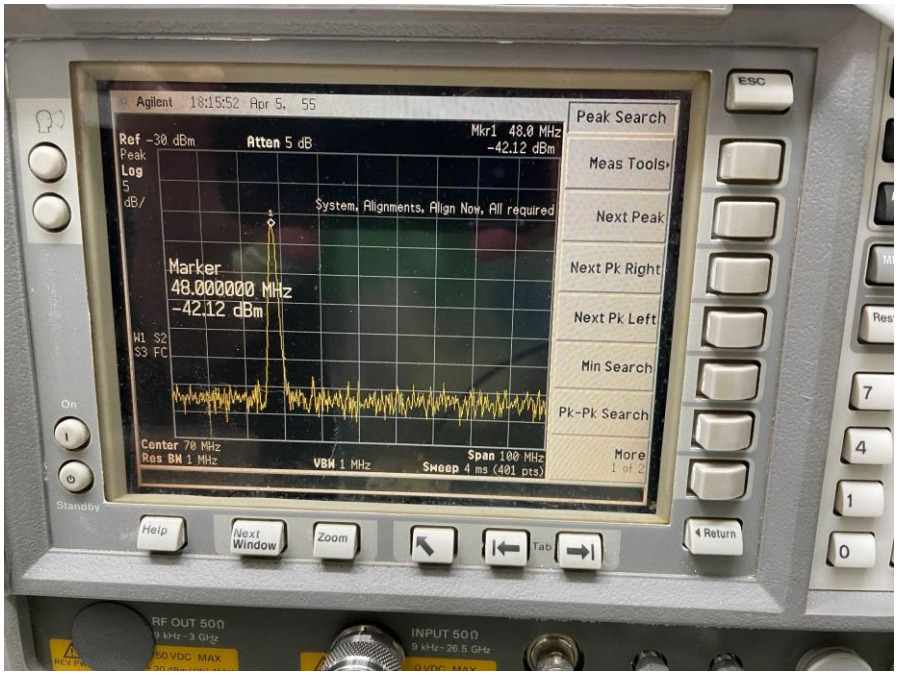


Table 7.2: The chart exemplifies the dBm/power peak at each RF frequency source from the frequency generator for all the VCOs where the peak is constant per VCO. The peak should ideally be larger than around -60 dBm which demonstrates a strong signal. The 6 VCOs with their dBm highlighted have poor performance, possibly due to the power splitters as discussed where there might be difficulty for the ground paddle to stay intact.

VCO # and Frequency (GHz)	**RF Frequency (GHz)**	**dBm Peak**
VCO1 (3.08 GHz)	3.03	-42
	3.13	-42
VCO2 (3.24 GHz)	3.19	-36
	3.29	-34
VCO3 (3.4 GHz)	3.35	-36
	3.45	-35
VCO4 (3.56 GHz)	3.51	-33
	3.61	-33

VCO5 (3.72 GHz)	3.67	-66
	3.77	-68
VCO6 (3.88 GHz)	3.83	-46
	3.93	-48
VCO7 (4.04 GHz)	3.99	poor performance, -70s
	4.09	poor performance, -70s
VCO8 (4.2 GHz)	4.15	-55
	4.25	-53
VCO9 (4.36 GHz)	4.31	-66
	4.41	-65
VCO10 (4.52 GHz)	4.47	-56
	4.57	-54
VCO11 (4.68 GHz)	4.63	-58
	4.73	-60
VCO12 (4.84 GHz)	4.79	-64
	4.89	-65
VCO13 (5 GHz)	4.95	-64
	5.05	-67
VCO14 (5.16 GHz)	5.11	-53
	5.21	-54
VCO15 (5.32 GHz)	5.27	-68
	5.37	-68
VCO16 (5.48 GHz)	5.43	-49
	5.53	-47

7.4 LO Board Measurements

We first calculated the current limits for 5 and 15 V power before testing the LO board. There is a total current of 435 mA from the VCOs going through the 3 V regulator which goes to the 5 V line. Subsequently, this is multiplied by 1.2 like before to obtain a current limit of 522 mA for the 5 V line. For the 15 V line, it ran through the 12 V regulator to the 16 GALI-19 amplifiers

which had 40 mA for a total of 640 mA where we then added 70 mA from the VCOs that connected to the 5 and 8 V regulator. This is multiplied by 1.2 to get 852 mA for the 15 V power line.

The only trouble we had with testing the local oscillator board was the poor soldering of a few of the VCOs where we also had to line up the components correctly and heat up the ground paddles. The beginning setup consisted of the +5 and +15 V power from the power supply onto the LO board with the total current near the calculated current limit. We then would turn the trimmer knobs while probing the output of the trimmer to read DC voltage from the voltmeter where turning the knob clockwise would increase voltage. The goal was to confirm that the voltages were changing as we tuned the trimmer. Next, each VCO's frequency was graphed by adjusting the trimmer so the dBm peak was at that frequency. We incorporated the spectrum analyzer to each MCX connector using a MCX and SMA cable as displayed below.

Fig. 7.16: Schematic Diagram of the LO Board Instrument Setup

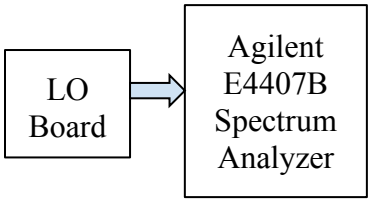
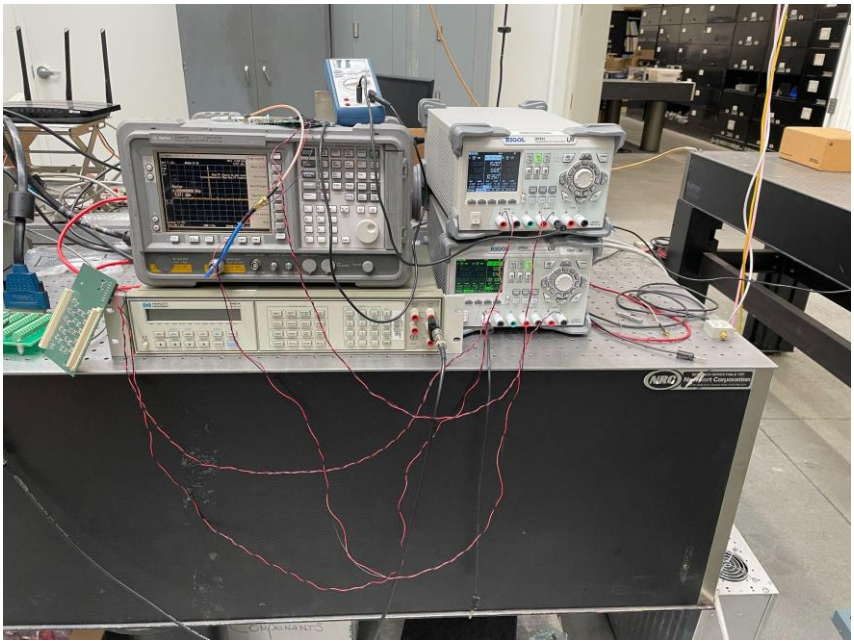


Fig. 7.17: Photograph of the LO Board Instrument Setup



For channels where the dBm peak was before or after the frequency where we cannot set the trimmer knob more clockwise or counterclockwise due to the voltage, we had to decrease the resistance connected to ground from the varactor circuits. The DC voltage and dBm peak were recorded where the plot reached the frequency to verify that the voltage was within the minimum and maximum voltage from the VCOs as well as the updated minimum and maximum voltage ideally after replacing the resistor with a lower resistor value. The first two pictures exemplify the frequency against the power peak at different scales per division in addition to the table for the VCO frequencies at their respective voltage and dBm peak.

Fig. 7.18: Here is an example of the center frequency versus dBm for one channel at a scale per division of 10 dB. In order to locate the peak to confirm the frequency, we pressed the “Peak Search” button.

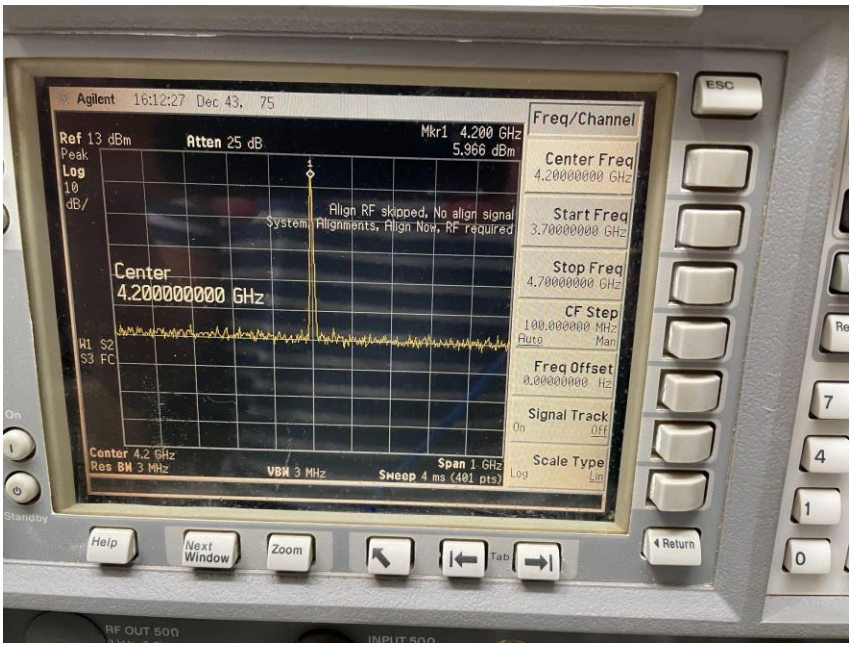


Fig. 7.19: Example of Center Frequency versus dBm for One Channel at Scale/Div of 5 dB Plot

Table 7.3: The table presents the tuned voltage and dBm peak at each frequency of the VCOs.

VCO #	Frequency (GHz)	Voltage (V)	dBm Peak
3	3.4	2.896	12.33
7	4.04	10.47	11.36
8	4.2	3.302	8.7
15	5.32	2.787	9.7
5	3.72	3.564	10
1	3.08	0.608	7.89
6	3.88	6.92	9.34
2	3.24	2.907	10.12
9	4.36	5.76	8.11
11	4.68	2.996	8.1
10	4.52	1.392	8.6
12	4.84	4.494	8.65
13	5	1.646	8.68
4	3.56	1.142	8.63
14	5.16	3.091	9.8
16	5.48	7.38	9.74

7.5 Full System Measurements

For the final testing arrangement, another frequency scan was taken for all boards connected where we varied the RF frequencies due to the 16 VCO frequencies. At the specific VCO frequency, we measured voltages up to 0.17 GHz less and more than the VCO frequency. The reason is to evaluate the peaks less than 2.5 V and curves as well as how stable and constant the graph is before and after each VCO frequency. Similar to before, we provided all the same current limits going 20% over the exact currents for all the power from the boards tested such as the +/-5 V and +/-12 V for the IF board, 12 V for the RF board, & 5 and 15 V for the LO board. Since the RF board output is connected directly to the IF board input, we added the 12V current

limit of 240 mA from the RF board with the 12V current limit of 500 mA from the IF board for a total of 740 mA.

After connecting the power supply to the power connectors, we again inserted the low voltage computer cable from the IF board output to an adapter to a board with power connectors. The connectors are hooked onto wires with the signal and ground lead to the multimeter for individual channel/VCO testing. Also, the input of this whole configuration comes from the Amphenol connector of the RF board to the fixed attenuators onto the signal generator where this time we would change the amplitude power or remove one of the fixed attenuators for each VCO where the peak was negative and/or the plot seemed flat since we want to increase voltage and observe a larger bandwidth. Consequently, like the RF board procedure, the MCX connector from VCO1 of the LO board would connect to the very bottom MCX connector of the RF board where VCO2-16 follows as we work our way up the RF board since VCO1 is the lowest frequency and placed the lowest frequency filters on the bottom of the RF board. With that said, channel 16 of the IF board would be for VCO1 where we would place the signal lead onto the corresponding power connector like testing the IF board. The resistor trimmer was also tuned on the LO board to obtain around -2.45 V at some VCO frequencies to eliminate spike dips of -2.45 V at other frequencies close to the VCO frequency and to have the power peak at precisely the VCO frequency like when testing the LO board. Below is the instrument setup for the IF, RF, and LO board connected.

Fig. 7.20: Schematic Diagram of the Instrument Setup for All Boards

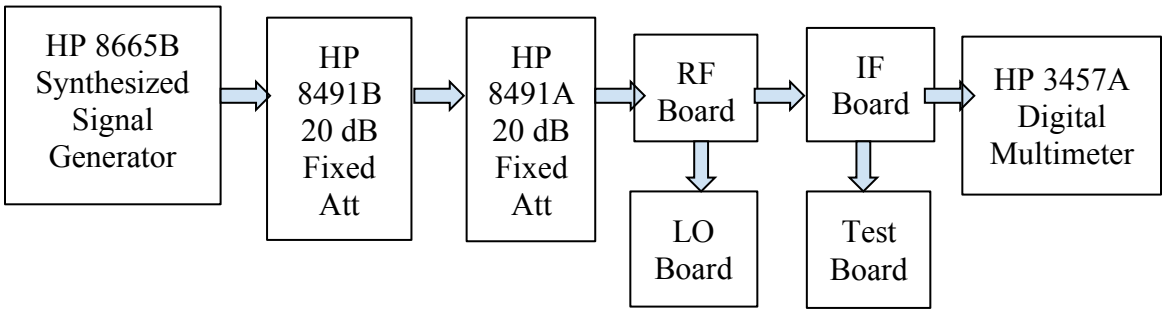


Fig. 7.21: Photograph of the Instrument Setup for All Boards

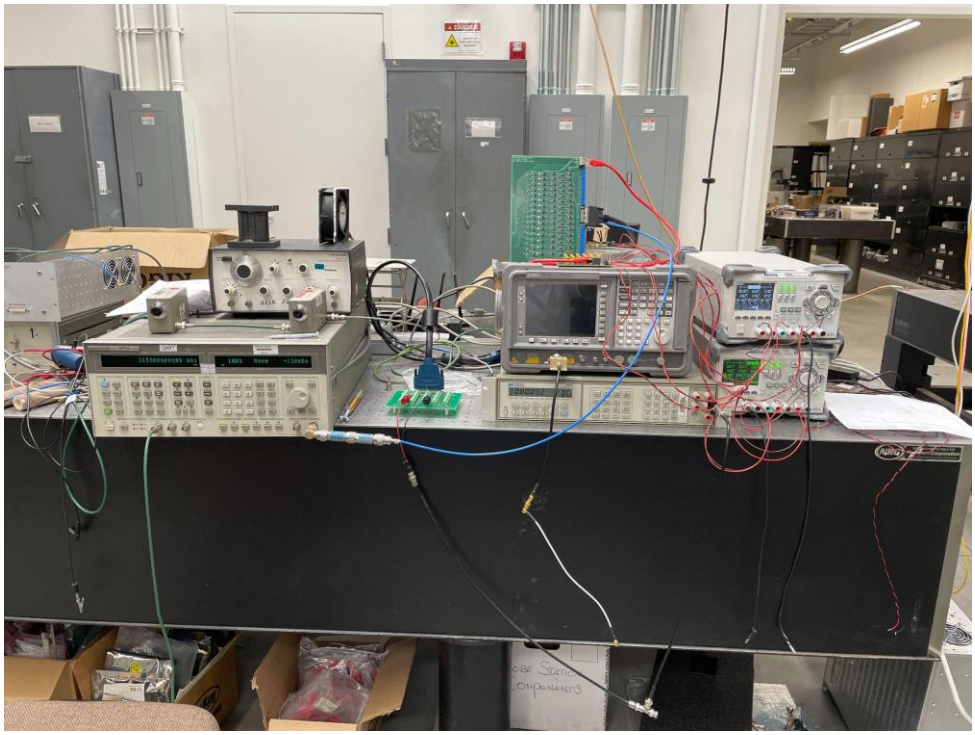
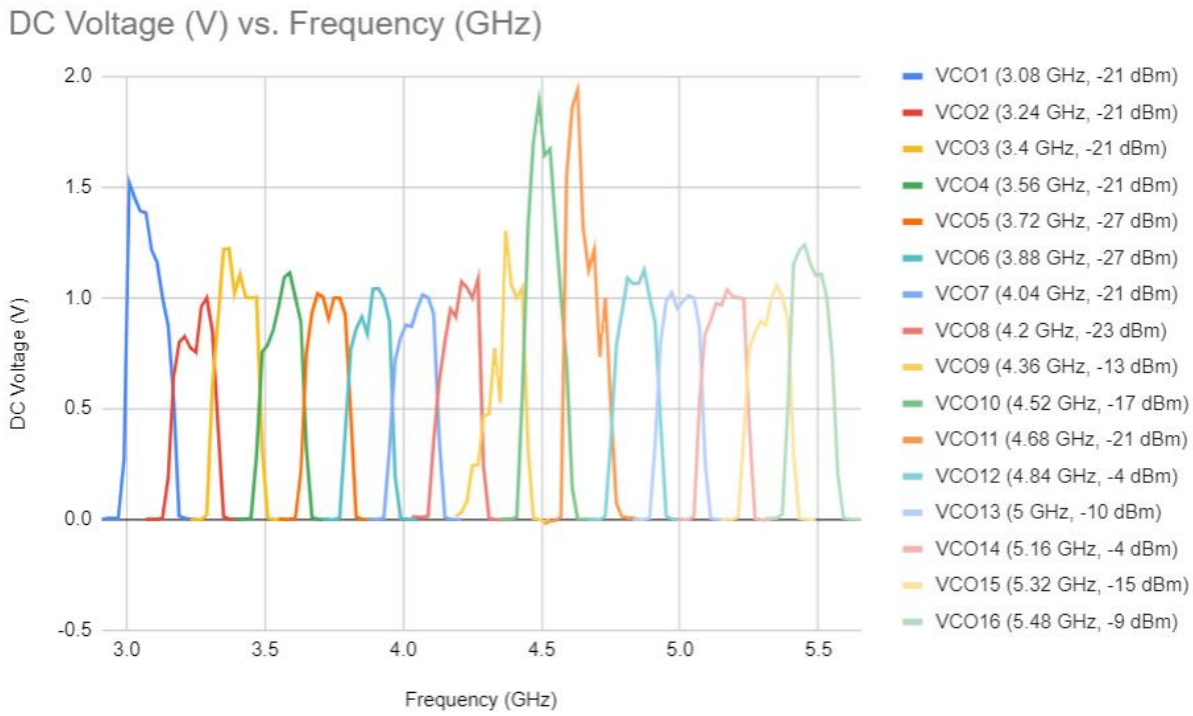


Fig. 7.22: RF Board Connected to LO Board with MCX Cables

Similar to the IF board data for the frequency scan, we normalized the data by adding the voltage at the last frequency point to all the voltages at the frequency points and dividing all the voltages by the voltage at 50 MHz more than the VCO frequency to graph. The plot below demonstrates the frequency scan for the full system.

Fig. 7.23: The detailed plots represent the frequency versus DC voltage for the full system of all boards connected. The whole graph illustrates a frequency range expected of around 3-5.5 GHz due to the center frequency of the VCOs. As previously, the voltages remained less than 2.5 V.



Chapter 8: Final Remarks

8.1 Discussion and Summary

The details of the findings based on the test approach exemplify accurate results as both trimmers on the IF board were easily adjusted and tuned where some issues of tuning to the DC offset voltage range or not getting around -2.45 V were due to a soldering error for components after the detector. The DC offset range was similar for all 16 channels from approximately -3 to -1.8 V. All channels were linear based on a power scan with voltage and for the frequency scan graphs, the channels were able to form a shape with similar bandwidth after normalizing and had an input attenuation from about -40 to -30 dB. The signal levels with respect to the control voltage

created curves that were decreasing which validates with the behavior from the control voltage versus attenuation graph from the MAAV attenuator datasheet. The problems that arose from these tests were also soldering issues from the components but this time before the detector.

For the LO board testing, the data displayed preciseness as the VCOs were able to reach the highest power at its frequency from tuning the trimmers and adjusting resistance values. The measured voltage for all VCOs was within its own range of the minimum and maximum values and the power peaked as high as about 12 dBm. Referring back to the incorporation of the low pass filter after the VCO, there was realization that the lowest frequency VCO had a large harmonic, so the use of filters from the RF board would supplement the system as well and hence the low pass filter is not required and the frequency did not have much loss.

The RF board was also a successful circuit configuration for 10 out of the 16 channels. The RF frequency source generated large and constant peaks for these channels within the VCO's frequency range. Some difficulty of getting correct measurements from other channels besides the power splitters could be from the heating and cooling system where the boards were hot as a fan is placed to cool them, affecting the VCO frequencies.

Last but not least, the 16 individual graphs of the VCOs/channels from all boards connected together depict strong voltage and near the VCO frequency due to the 3-5.5 GHz of space and within the 2.5 V digitizer. Tuning the trimmer when necessary could have also been from the temperature drift. Up to the maximum power it was used in order to attain these signals.

All in all, the boards throughout were schematically designed, assembled, and manufactured properly for the most part. This high-resolution ECEI module was designed and characterized efficiently with high resolution channels where the frequency channels are closely spaced 160 MHz apart from a RF bandwidth of 3.0-5.5 GHz for the overall ECEI system. The

design, boards, and results comply with previous research and work such as ECEI systems, double heterodyne down-conversion process, and the 8 discrete frequency bands. They also relate to previous ideas involving the W7-X ECEI plasma and zoom device.

8.2 Future Work

More towards the future, there can be work with a second ECEI system which would engage with similar wideband electronics but with 24×8 channels, a 1.0 GHz channel spacing, and a tunable RF bandwidth extending from 130 to 153 GHz. The number of ECEI channels in the present ECEI system could also be easily increased from 16×8 to 20×8. This can be done by fabricating four additional IF electronics modules and installing an additional 4×8=32 digitizers [5].

During the design with the RF and LO board, we could have used two sets of two 215 Ω resistors in parallel for the GALI-19 amplifier circuit for less components and space on each board. The amplifier circuit from the datasheet closely matches this configuration and the specification of a typical amplifier circuit. Due to the power dividers for the RF circuit not providing sufficient signal and strong power performance for specific VCOs, it is recommended to have the power dividers pre soldered or assembled from a manufacturing company. Using Wilkinson power dividers to split the input signal into multiple bands like from the past radiometer electronics is also a potential solution but does take up more space. In addition, the RF board should be supplied with a high pass filter between the mixer and local oscillator to eliminate signals with 160 and 320 MHz. The local oscillator board also needs more increase of shielding from the pickup of the power lines. This is so that there is more power line filtering as well as ground connection or more space apart.

In terms of the physical boards, in the time ahead there can be an implementation of a case or metal box when testing the boards so that the components could not be affected by the heat or cold. A more efficient fan or cooling system/equipment would benefit the temperature of the power supplied and components during testing. Instead of the adapter, low voltage cable, and power connector board for the 68-pin VHDCI output connector for the IF board, an alternative connection would be with the NI BNC-2090 breakout accessory with pinouts that match with the pins of the VHDCI connector pins. Within 10 of the IF and RF boards, it is suggested to develop a method to take the output of the oscillators for a buffer so each local oscillator signal can drive 10 outputs.

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