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A design study on the scaling limit of ultra-thin silicon- on-insulator MOSFETs

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A Design Study on the Scaling Limit of Ultra-Thin Silicon-on-Insulator MOSFETs

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

Wei-Yuan Lu

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2007

The dissertation of Wei-Yuan Lu is approved, and it is acceptable in quality and form for publication on microfilm:

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University of California, San Diego

2007

DEDICATION

This dissertation is dedicated to my wife, parents and sister.

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The text of Chapter 3, in part, is the reprint of the material as it appears in "On The Scaling Limit of Ultrathin SOI MOSFETs" by Wei-Yuan Lu and Yuan Taur, IEEE Transaction on Electron Devices, May 2006. The dissertation author was the primary researcher of this paper.

The text of Chapter 4, in part, is the reprint of the material as it appears in "Effect of Body Doping on the Scaling of SOI MOSFETs" by Wei-Yuan Lu and Yuan Taur, Proceedings of SISPAD, Sep. 2006. The dissertation author was the primary researcher of this paper.

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PUBLICATIONS

1. **W.-Y. Lu** and Y. Taur, "On the scaling limit of ultra-thin body SOI MOSFETs", *IEEE Trans. Electron Devices,* vol. 53, no. 5, May 2006.

2. **W.-Y. Lu** and Y. Taur, "Effect of body doping on the scaling of SOI MOSFETs", *SISPAD*, 2006.

3. M. Liu, **W.-Y. Lu**, W. Wang and Y. Taur, "Scaling to 10nm: Bulk, SOI or Double-Gate MOSFETs?", *ICSICT*, 2006.

4. B. Yu, **W.-Y. Lu**, H. Lu and Y. Taur, "Analytic charge and capacitance model for surrounding-gate MOSFETs", *IEEE Trans. Electron Devices,* vol. 54, no. 3, 2007.

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6. B. Yu, J. Song, **W.-Y. Lu**, and Y. Taur, "A unified drain current model for multiple-gate MOSFETs", to be submitted.

ABSTRACT OF THE DISSERTATION

A Design Study on the Scaling Limit of Ultra-Thin Silicon-on-Insulator MOSFETs

by

Wei-Yuan Lu

Doctor of Philosophy in Electrical Engineering (Applied Physics)

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Professor Yuan Taur, Chair

As bulk CMOS is approaching its scaling limit, SOI CMOS is gaining more and more attentions and is considered as a potential candidate for achieving 10-nm CMOS. Fully-depleted SOI MOSFETs have several inherent advantages over bulk MOSFETs-low junction capacitance, no body effect and no need for body doping to confine gate depletion. This dissertation presents a comprehensive, 2-D simulation-based design study on the scaling limit of ultra-thin silicon-on-insulator MOSFETs .

Starting with the lateral-field analysis of fully-depleted (FD) SOI MOSFETs, it is shown that the general scale-length model is inapplicable for predicting the minimum scalable channel length $L_{\min}$ when the buried-oxide is very thick. The scaling of FDSOI MOSFETs is independent of the buried-oxide thickness. An empirical $L_{\min}$ prediction equation is developed by approximating the constant $L_{\min}$ contours in a design plane of silicon-film and gate-dielectric thickness. Ultimately, $L_{\min} \sim 5\,t_{Si}$ with a high-k gate dielectric. Other factors such as body doping, substrate biasing, and buried-insulator permittivity ε_{BOX} and bandgap affecting short-channel scaling of FDSOI are also investigated. Empirical $L_{\min}$ prediction equations are developed for FDSOI devices with body doping and low-k buried-insulators. In principle, the $L_{\min}$ can be improved from $\sim 5\,t_{Si}$ to $\sim 2\,t_{Si}$ by body doping. The $L_{\min}$ can also be reduced 15% shorter from $\varepsilon_{BOX} = 3.9\varepsilon_0$ to $\varepsilon_{BOX} = \varepsilon_0$.

Finally, the scaling limit of FDSOI MOSFETs is discussed. From the electrostatic perspective 10-nm FDSOI CMOS requires scaling both high-k gate-dielectric and silicon-film thickness to their limits of ~2 nm. However, silicon-film thickness cannot below ~3 nm to avoid severe mobility degradation. The scaling limit of FDSOI MOSFETs with a feasible HfO_2 gate dielectric is then projected to be ~17 nm. 10-nm FDSOI CMOS can be achieved only if there is a breakthrough on thin silicon-film mobility.

CHAPTER 1

Introduction

1.1 History and future trends of CMOS logic scaling

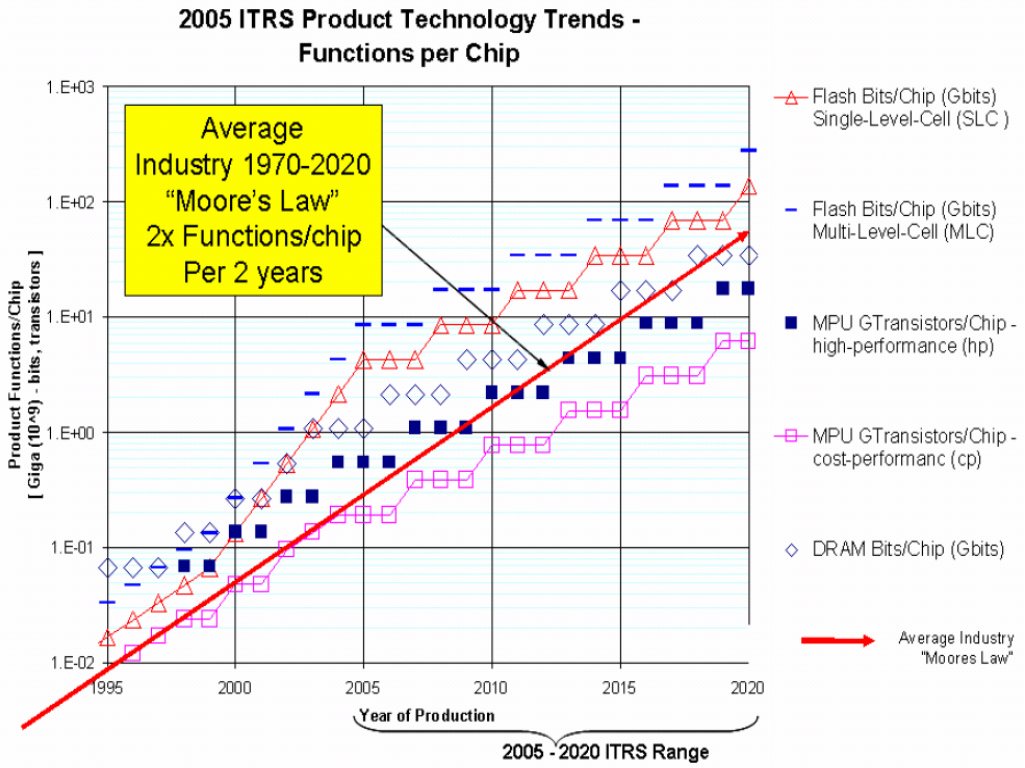

Fig. 1.1 2005 ITRS product technology trend: product functions/chip and industry average "Moore's Law" trends. Adapted from [1.1].

Over the past few decades, successful attempts have been made at decreasing the physical dimensions of MOS transistors to achieve density, speed, and power

improvements in CMOS technology. The number of transistors on a chip has consistently doubled every two years, as shown in Fig. 1.1, and the observation is popularly known as Moore's law. In order to sustain the historical trends of device performance improvements, continued aggressive scaling efforts have been made recently for leading-edge logic technology. The most obvious consequence of such scaling efforts is the shrinking MOS transistor gate length, as shown in Fig. 1.2, which presents the observed and predicted viable MOS transistor gate length versus time.

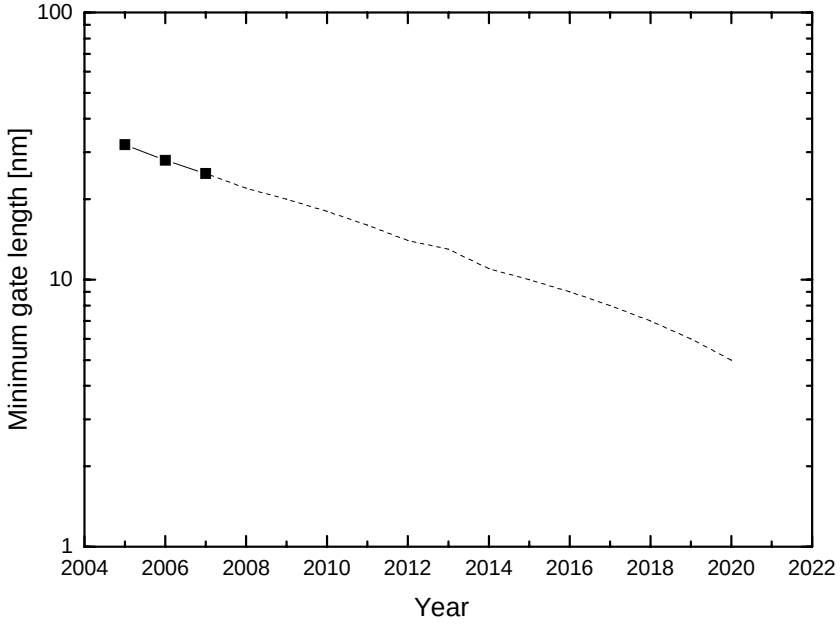

Fig. 1.2 Predicted and observed minimum MOS gate length versus time showing the exponential decreasing of physical gate length with the passage of time. Adapted from [1.1].

The scaling concept of MOSFETs stems from Dennard's research work published in 1974. Fig. 1.3 schematically illustrates the basic idea of constant-field scaling for MOS transistors. Scaling can achieve the same electric-field patterns in the smaller device by reducing the applied voltage along with all the key dimensions and by increasing the impurity doping concentration by the same factor α. Therefore, a larger MOS transistor can then be scaled down to a smaller one with similar

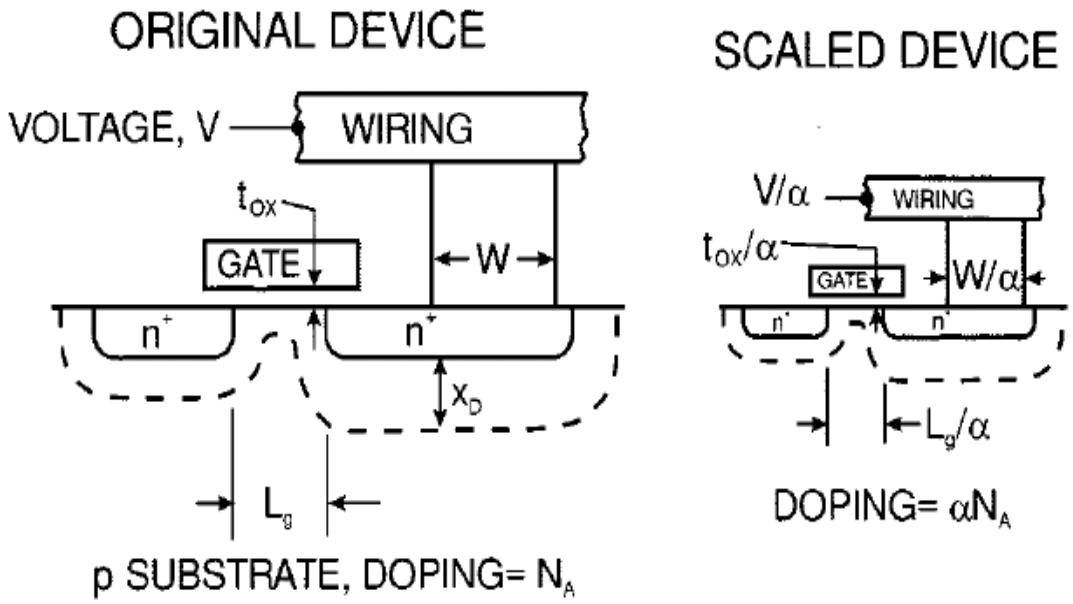

Fig. 1.3 Schematic illustration of the scaling of Si technology by a factor α. Adapted from [1.2].

electrostatic behavior. Table 1.1 shows scaling rules for MOSFETs and physical parameters of three different scaling behaviors. According to the constant-filed scaling rule, the circuit speed increases in proportional to the scaling factor α and the circuit density increases by a factor of α^2. The technology scaling principles in table 1.1 only provide a guideline how to shrink a known good design of a MOSFET. It does

not tell a device designer how short channel length of a MOSFET he can make for given doping profiles and layer thickness. Moreover, the device channel length cannot be arbitrarily scaled due to short-channel effect (SCE), i.e., threshold voltage roll-off and drain induced barrier lowering (DIBL).

Table 1.1 Technology scaling rules for three cases. Adapted from [1.3].

Physical parameter	Constant-Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_D and α_W are separate dimensional scaling parameters for the selective scaling case. α_D is applied to the device vertical dimensions and gate length, while α_W applies to the device width and the wiring.

In addition to the channel length scaling limit imposed by short-channel effect, there

are nonscaling effects limiting the applicability of the scaling principles to shrink MOS transistors. For example, the nonscalability of thermal voltage KT/q leads to subthreshold nonscaling, i.e., the threshold voltage cannot be scaled down like other physical parameters. The nonscalability of the silicon energy bandgap leads to the nonscaling of the built-in potential, depletion-layer width, and short-channel effect. The scaling limit of physical dimensions is imposed by quantum mechanical effect. Details of those scaling limits are summarized in [1.3]. There are several ways to circumvent those scaling limits: employing novel device structures to further scale down MOS transistors with the SCE being under control; installing high-k gate dielectrics in MOS transistors to reduce the effective oxide thickness without scaling down the physical thickness below the quantum mechanical tunneling limit.

1.2 Background

1.2.1 SOI CMOS

Silicon-on-insulator (SOI) CMOS involves building conventional MOSFETs on very thin layers of crystalline silicon and is illustrated in Fig. 1.4. The thin silicon layer is electrically isolated from the substrate by a thick (typically 100 nm or more) buried-oxide layer. The inherent advantages of SOI devices over bulk CMOS will be addressed in Section 1.2.3. SOI substrates fabricated by oxygen-ion implantation (SIMOX) and wafer bonding are particularly suitable for VLSI applications due to their compatibility with established CMOS processing technology.

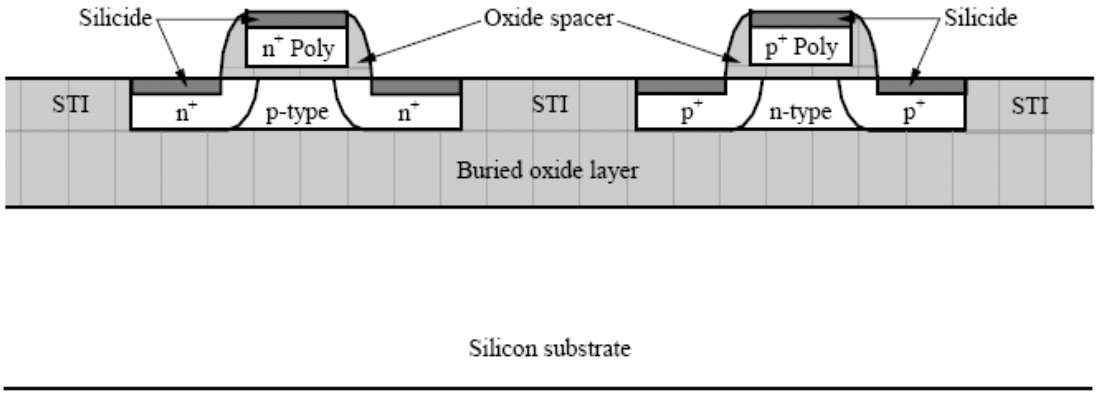

Fig. 1.4 A schematic cross section of SOI CMOS, with shallow trench isolation (STI), dual polysilicon gates, and self-aligned silicide.

1.2.2 Partially-depleted SOI MOSFETs

SOI MOSFETs are distinguished as partially-depleted (PD) when the silicon film is thicker than the maximum gate depletion width and the devices exhibit a floating-body effect [1.4], and fully-depleted (FD) when the silicon film is thin enough that the entire film is depleted before the threshold condition is reached. In PDSOI MOSFETs, there is a neutral body region below the gate depletion boundary. The body of PDSOI devices are not tied to the ground as in bulk devices and can float to different potentials depending on the drain and gate voltages. The floating-body effect occurs when carriers of the same type as the body, generated by impact ionization near the drain, are stored in the floating body, which alters the body potential and hence the threshold voltage [1.4]. This effect is especially strong in nMOSFETs, due to the higher impact ionization rate of electrons. Floating body effect is dynamic in nature since it takes some finite time, which is much longer than the device switching time,

for the body to charge or discharge to a steady potential. Consequently, the body potential of PDSOI MOSFETs has significant history dependence. Depending on the history, the body potential of a PDSOI MOSFET may be at different levels in the beginning of a switching event and affects the threshold voltage and delay. History dependence of transient output characteristics of PDSOI MOSFETs has been reported in [1.5]. The body recovery time is strongly affected by the generation time (impact ionization during on-time or thermal generation during off-time). Because of the slow thermal generation process, it takes long off-time (~1ms [1.5]) to replenish holes in the body (for nMOSFET) at low-drain voltages (~<1.5 V [1.5]) which impact ionization does not take place. At high-drain voltages which impact ionization occurs, the body of a PDSOI device can be charged up within a few nanoseconds. This poses great difficulties in circuit design. The history effect can be minimized by optimizing the key PDSOI device parameters which are summarized in [1.6, 1.7]. The PDSOI CMOS technology is the most popular SOI technology at present due to its several advantages over bulk devices- reduced junction capacitances and better performance. Although it is still a technological challenge to fabricate an ultra-thin silicon film sub-20nm FDSOI device today, FDSOI technology is gaining more and more attentions and considered as a potential candidate for achieving 10-nm CMOS.

1.2.3 Fully-depleted SOI vs. bulk MOSFETs

According to the ITRS new roadmap in 2005, scaling of the conventional bulk MOSFET to the 32 nm technology generation (gate length=13 nm) will face several

significant challenges due to the use of high channel doping-which leads to band-to-band tunneling across the junction, gate-induced drain leakage (GIDL), and stochastic doping variations [1.1]. Since planar bulk CMOS technology is approaching its scaling limit, ultra-thin body fully-depleted (FD) silicon-on-insulator (SOI) MOSFETs have been considered as the potential candidate for developing high performance consumer electronics. The unconventional FDSOI device structure has reduced source/drain junction capacitances, lower leakage current, and immunity to

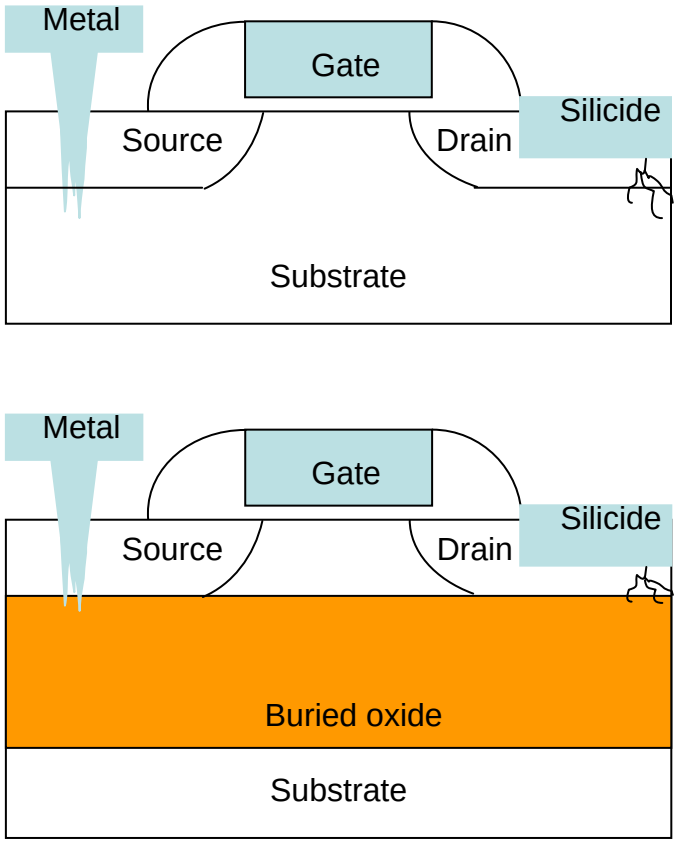

Fig. 1.5 Formation contact or silicide on shallow junctions in the case of (a) bulk silicon and (b) thin-film SOI.

radiation-induced photocurrents and latch-up effect. It has the potential for

manufacturing a modern CMOS circuit with higher speed, and lower power dissipation.

Another advantage of using FDSOI CMOS technology is because it suppresses some yield hazard factors which have been observed in bulk CMOS [1.8]. To illustrate this, we consider fabricating shallow junctions and making electrical contact in a bulk device and a FDSOI device (Fig. 1.5). The junction depth of a FDSOI device is equal to its silicon film thickness. Electrical contact to a shallow junction can be made by metal (e.g., tungsten), an alloy (e.g., Al:Si) or metal silicide (e.g., $TiSi_2$). In a bulk MOSFET, unwanted reactions can take place between the silicon and the metal or the silicide. The metal may punch through the junction (Fig. 1.5(a)), which can lead to uncontrolled leakage current. If the device is realized in an ultra-thin body FDSOI device structure, the source and drain active regions end at the thick buried-insulator layer. In that case, any uncontrolled metal-silicon reaction will not generate leakage current (Fig. 1.5(b)).

In addition, the short-channel effect in an ultra-thin body FDSOI MOSFET can be suppressed by thinning down the silicon body and BOX thickness. Furthermore, scaling down the BOX thickness of a FDSOI MOSFET below 5 nm can lead to a double-gate device structure on SOI substrate, although the process technology is still complex and immature. In contrast to BOX thickness scaling, the silicon film thickness scaling is more technically achievable [1.9], which generates a great deal of interest in ultra-thin body FDSOI MOSFETs. Previous published experimental studies

[1.10] already showed the viability of nanoscale ultra-thin body, undoped FDSOI MOSFETs with a standard thick BOX. However, there lacks a clear guideline on the scaling of ultra-thin body FDSOI MOSFETs. To find out the scaling rules for FDSOI MOSFETs, an extensive 2-D numerical simulation-based design study is carried out and analyzed in this thesis.

1.3 Outline

This thesis consists of seven chapters:

Chapter 1 introduces the scaling trend of CMOS technology, and the motivation of our design study.

Chapter 2 reviews the previous analytical models of bulk and fully-depleted SOI MOSFETs.

Chapter 3 discusses out the inapplicability of the general scale-length model in predicting the minimum scalable channel length of undoped FDSOI MOSFETs. Analysis of electric field distribution in the buried-oxide is carried out by 2-D numerical simulations. Constant $L_{\min}$ contours are plotted in a $t_{Si} - t_{OX}$ plane, showing the design space of undoped FDSOI MOSFETs. A simple scaling rule is obtained empirically from the constant $L_{\min}$ contours.

Chapter 4 investigates several factors affecting the short-channel behavior of FDSOI MOSFETs. They are: substrate biasing, body doping, and the dielectric

constant of the buried-insulator layer. An empirical equation for predicting the L_{min} of doped FDSOI MOSFETs is obtained from the constant L_{min} contours. Short-channel effect can also be mitigated by applying a high reverse voltage to the substrate of a FDSOI device. The drawback of such a scheme is also discussed in this chapter.

Chapter 5 explores the scaling limit of gate insulator and silicon film thickness of FDSOI MOSFETs. Quantum mechanical effect on the short-channel behavior of FDSOI MOSFETs is discussed. The design space of sub-20 nm FDSOI MOSFETs is shown subject to the gate tunneling limit and the scaling limit of silicon film thickness. Carrier mobility degradation due to surface roughness and buried-oxide interface roughness in ultra-thin body FDSOI MOSFETs is investigated based on published data. Performance degradation of an extremely-scaled FDSOI device is assessed qualitatively in the last section.

Chapter 6 summarizes the thesis with some final remarks and suggestions for future work.

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CHAPTER 2

Review of Previous Analytical Models on Scaling of Bulk and SOI MOSFETs

2.1 Scale-length model for bulk MOSFETs

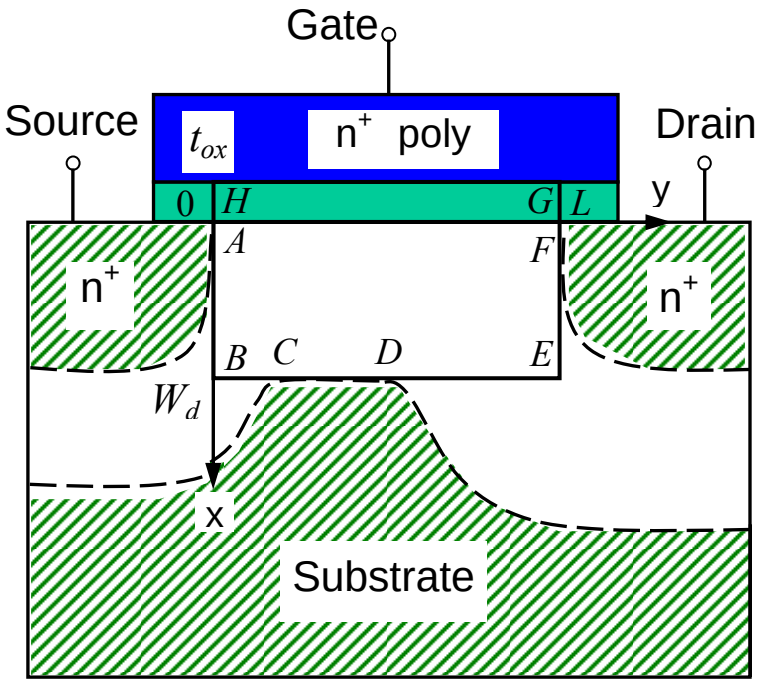

Fig. 2.1 Simplified geometry for analytically solving Poisson's equation in a short-channel MOSFET. Adapted from [2.1].

The analytical model of the short-channel effect in bulk MOSFETs has been developed by Thao N. Nugyen [2.1] in 1984. With a number of approximations while retaining the basic aspects of the short-channel effect, the electrostatic potential in

bulk MOSFETs was obtained by solving Poisson's equation in the simplified MOSFET geometry shown in Fig. 2.1. The x-axis is along the vertical direction, the y-axis is along the horizontal direction, and the origin at point A. A rectangular box is used to define the simplified boundary conditions for solving Poisson's equation which substantially reduces the complexity of the problem. The analytical solution of electrostatic potential has been verified by 2-D numerical device simulation results.

The normal component of the electric field changes by a factor of $\varepsilon_{Si}/\varepsilon_{OX} \approx 3$ across the silicon-oxide interface of a bulk MOSFET. In Nguyen's approach, the oxide is replaced by an equivalent region of the same dielectric constant as silicon, but with a thickness of $3t_{OX}$ so that both the potential and its derivatives are continuous at the silicon-oxide interface. Therefore, the entire rectangular region of interest can be treated as a homogeneous material of silicon with length L and depth $W_d + 3t_{OX}$.

In the oxide region, Poisson's equation becomes Laplace equation,

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = 0 \tag{2.1}$$

In the depletion region in silicon, Poisson's equation is approximated by

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}} \tag{2.2}$$

Equation (2.2) is only applicable to a bulk device in the subthreshold region which mobile charges are negligible. If we assume that the source and drain junctions are abrupt and deeper than W_d, we can define the following set of simplified boundary

conditions:

$$\psi(-3t_{ox}, y) = V_g - V_{fb} \qquad 0 < y < L \tag{2.3}$$

$$\psi(x,0) = \psi_{bi} \qquad -3t_{OX} < x < W_d \tag{2.4}$$

$$\psi(x, L) = \psi_{bi} + V_{ds} \qquad -3t_{OX} < x < W_d \tag{2.5}$$

$$\psi(W_d, y) = 0 \qquad 0 < y < L \tag{2.6}$$

By using the superposition principle and breaking the electrostatic potential $\psi(x, y)$ into the following terms, one can write:

$$\psi(x, y) = \upsilon(x, y) + u_L(x, y) + u_R(x, y) + u_B(x, y) \tag{2.7}$$

Here $\upsilon(x)$ is the 1-D solution to equation $\partial^2\psi/\partial x^2 = 0$, and satisfies the top boundary conditions. u_L, u_R, and u_B are solutions to the Laplace's equation and satisfy the boundary conditions at source side, drain side and bottom respectively. For example, u_L is zero on the top, bottom, and the right (drain side) boundaries, but $\upsilon + u_L$ satisfies the left (source side) boundary condition. Similarly, u_R is zero on the top, bottom, and the left boundaries, but $\upsilon + u_R$ satisfies the right (drain side) boundary condition.

$$\upsilon(x, y) = \begin{cases} \psi_s^0 - \dfrac{V_g - V_{fb} - \psi_s^0}{3t_{OX}} x & -3t_{OX} \le x \le 0 \\ \psi_s^0 \left(1 - \sqrt{\dfrac{qN_a}{2\varepsilon_{Si}\psi_s^0}} x\right)^2 & 0 \le x \le W_d \end{cases} \tag{2.8}$$

Here the long-channel surface potential ψ_s^0 is related to V_g by the requirement that

$\partial \upsilon / \partial x$ be continuous at $x = 0$.

$$\frac{V_g - V_{fb} - \psi_s^0}{3t_{OX}} = \sqrt{\frac{2qN_a\psi_s^0}{\varepsilon_{Si}}} \tag{2.9}$$

The rest of the solutions are in the form of a series product of hyperbolic and sinusoidal functions [1.6]:

$$u_L(x,y) = \sum_{n=1}^{\infty} b_n^* \frac{\sinh(\frac{n\pi(L-y)}{W_d + 3t_{OX}})}{\sinh(\frac{n\pi L}{W_d + 3t_{OX}})} \sin(\frac{n\pi(x+3t_{OX})}{W_d + 3t_{OX}}) \tag{2.10}$$

$$u_R(x,y) = \sum_{n=1}^{\infty} c_n^* \frac{\sinh(\frac{n\pi y}{W_d + 3t_{OX}})}{\sinh(\frac{n\pi L}{W_d + 3t_{OX}})} \sin(\frac{n\pi(x+3t_{OX})}{W_d + 3t_{OX}}) \tag{2.11}$$

$$u_B(x,y) = \sum_{n=1}^{\infty} d_n^* \frac{\sinh(\frac{n\pi(x+3t_{OX})}{L})}{\sinh(\frac{n\pi(W_d+3t_{OX})}{L})} \sin(\frac{n\pi y}{L}) \tag{2.12}$$

The high-order terms in u_R and u_L series can be neglected if the channel length is not too short. By making the thin-oxide assumption and dropping all the second-order terms in $3t_{OX}/W_d$, the simplified expressions for the coefficients can be obtained:

$$b_1^* = \frac{4}{\pi}\psi_{bi} - \frac{2}{\pi}(1 - \frac{4}{\pi^2})(1 + \frac{6t_{OX}}{W_d})\psi_s^0 \tag{2.13}$$

$$c_1^* = \frac{4}{\pi}(\psi_{bi} + V_{ds}) - \frac{2}{\pi}(1 - \frac{4}{\pi^2})(1 + \frac{6t_{OX}}{W_d})\psi_s^0 \tag{2.14}$$

The approximate analytical solution of potential in the silicon region under subthreshold conditions is

$$\psi(x,y) = \psi_s^0(1 - \sqrt{\frac{qNa}{2\varepsilon_{Si}\psi_s^0}})^2 + \frac{b_1^* \sinh(\frac{n\pi(L-y)}{W_d + 3t_{OX}}) + c_1^* \sinh(\frac{n\pi y}{W_d + 3t_{OX}})}{\sinh(\frac{n\pi L}{W_d + 3t_{OX}})} \sin(\frac{n\pi(x + 3t_{OX})}{W_d + 3t_{OX}}) \tag{2.15}$$

Under subthreshold condition, current conduction is dominated by diffusion, and is controlled by the highest potential barrier along the channel. The threshold voltage lowering in a short-channel device can then be expressed as

$$\Delta V_t = \frac{24t_{OX}}{W_{dm}} \sqrt{\psi_{bi}(\psi_{bi} + V_{ds})} e^{-\pi L / 2(W_{dm} + 3t_{OX})} \tag{2.16}$$

The subthreshold slope of a short-channel device is approximated as

$$S \approx 2.3 \frac{W_{dm} + 3t_{OX}}{W_{dm}} \frac{kT}{q}(1 + \frac{11t_{OX}}{W_{dm}} e^{-\pi L / 2(W_{dm} + 3t_{OX})}) \tag{2.17}$$

The simplification of boundary condition in silicon/oxide interface in Nguyen's approach is valid only when the oxide field is dominated by its normal component.

2.2 General scale-length model for 2- and 3-layer MOSFETs

Recently, Nguyen's model has been extended to the general scale-length model by D. J. Frank [2.2], based on a two-region (or three-region) model by matching the 2-D boundary conditions at the silicon/insulator interfaces. By using superposition, the potentials in the center of a bulk MOSFET ψ_1 and ψ_2 can be written as,

$$\begin{aligned}\psi_1(x,y) &= \upsilon_1(x) + u_{L1}(x,y) + u_{R1}(x,y)\\ \psi_2(x,y) &= \upsilon_2(x) + u_{L2}(x,y) + u_{R2}(x,y)\end{aligned} \tag{2.18}$$

, here $\upsilon_i(x)$ are the 1-D solutions to Poisson's equation satisfying the top, bottom and dielectric boundary conditions. u_{Li} and u_{Ri} are left and right solutions to Laplace's

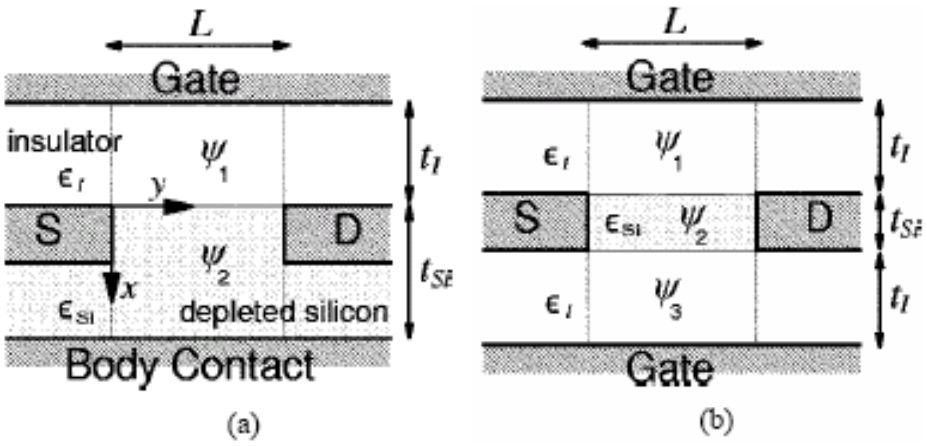

Fig. 2.2 Idealized schematic cross section diagram of (a) a bulk MOSFET (b) a double-gate MOSFET, defining the insulatorthickness t_I and the depleted Si thickness t_{Si}. ε_{Si} is the permittivity of Si and ε_I is the permittivity of gate insulator(s). Adapted from [2.2].

equation and satisfy the boundary conditions at the source and drain, respectively. The *u*'s can be written as infinite series in the form of sinh(ay)sin(bx). If the channel length is not too short, the lowest order term dominates the solution. Therefore, u_{Li} and u_{Ri} can be simplified to the following expressions:

$$u_{L1} \cong b_{11} \frac{\sinh(\pi(L-y)/\lambda_1)}{\sinh(\pi L/\lambda_1)} \sin(\pi(x+t_I)/\lambda_1) \tag{2.19}$$

$$u_{R1} \cong c_{11} \frac{\sinh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)} \sin(\pi(x+t_I)/\lambda_1) \tag{2.20}$$

$$u_{L2} \cong b_{21} \frac{\sinh(\pi(L-y)/\lambda_1)}{\sinh(\pi L/\lambda_1)} \sin(\pi(x-t_{Si})/\lambda_1 + \pi) \tag{2.21}$$

$$u_{R2} \cong c_{21} \frac{\sinh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)} \sin(\pi(x-t_{Si})/\lambda_1) \quad . \tag{2.22}$$

The b's, c's, and λ_1 are coefficients and can be determined by satisfying the boundary conditions. By matching the potential and field boundary conditions at the silicon-insulator interfaces, an eigenvalue equation for scale length λ_1 can be

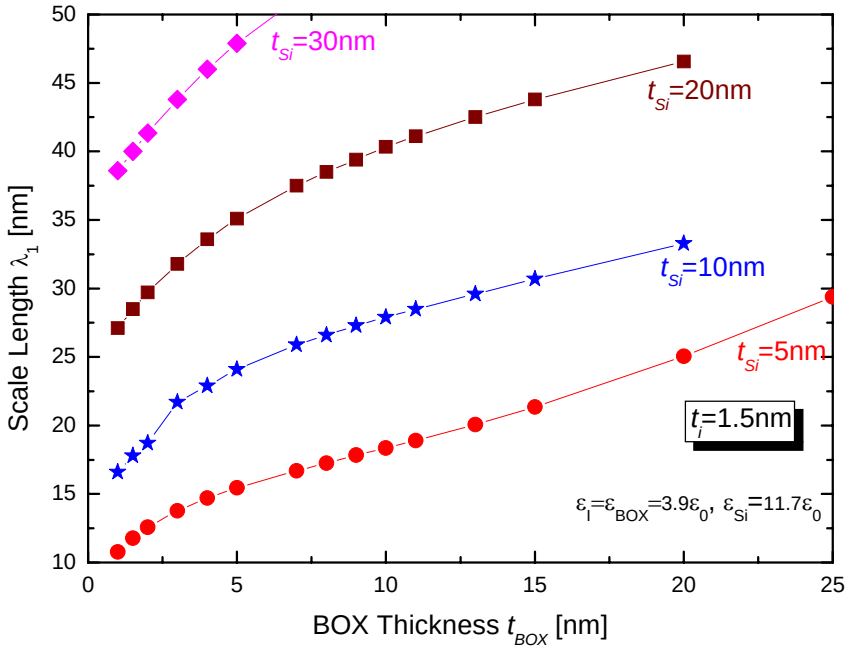

Fig. 2.3 The scale length λ_1 depends on gate dielectric, silicon film and buried oxide thicknesses.

obtained:

$$\varepsilon_{Si}\tan(\pi t_I/\lambda_1)+\varepsilon_I\tan(\pi t_{Si}/\lambda_1)=0\,. \tag{2.23}$$

The result is also generalized to any three-layer-dielectrics device with dielectric thickness t_1, t_2, and t_3 and permittivities ε_1, ε_2, and ε_3. The corresponding eigenvalue equation is,

$$\frac{\varepsilon_2}{\varepsilon_1\varepsilon_3}\tan(\frac{\pi t_1}{\lambda_1})\tan(\frac{\pi t_2}{\lambda_2})\tan(\frac{\pi t_3}{\lambda_3})=\frac{1}{\varepsilon_1}\tan(\frac{\pi t_1}{\lambda_1})+\frac{1}{\varepsilon_2}\tan(\frac{\pi t_2}{\lambda_1})+\frac{1}{\varepsilon_3}\tan(\frac{\pi t_3}{\lambda_1})\,. \tag{2.24}$$

For the first-order solution, the potential in the center of the channel varies as $(b_{21}+c_{21})\sinh(\pi L/2\lambda_1)/\sinh(\pi L/\lambda_1)$, where b_{21} and c_{21} are bias dependent. Since this gives a length dependence $\sim\exp(-\pi L/2\lambda_1)$, the L/λ_1 ratio is a key measure of the short-channel effect of a scaled MOSFET. The minimum scalable channel length $L_{\min}$ of a MOSFET is projected to be ~1.5-2 λ_1. The general scale-length model is applicable to bulk MOSFETs, double-gate MOSFETs and long-channel SOI MOSFETs with any gate dielectrics. The scale length λ_1 of a FDSOI MOSFET can be solved numerically from the eigenvalue equation (2.24). Fig. 2.3 shows that the scale length λ_1 increases with increasing t_{BOX}.

2.3 Review of other literature

In the 1980's, SOI technology was pioneered and advocated by J. P. Colinge [2.3]. 1-D Poisson's equation was solved to model the electrostatic behavior of SOI

MOSFETs. An ideal inverse subthreshold slope of 60mV/decade can be observed in a long-channel undoped FDSOI device. However, the ideal subthreshold slope cannot be obtained in short-channel, thick BOX FDSOI devices due to the lateral field coupling into the channel through the buried-oxide. The subthreshold slope advantages of SOI technology over bulk CMOS exist only in long-channel SOI MOSFETs. In the early 90's, R. H. Yan [2.4] followed K.K. Young's approach [2.5] and assumed a second-order polynomial function for the potential perpendicular to the channel surface. He derived a 2-D analytical potential distribution in the silicon body. The electric field inside a thick buried-oxide of a FDSOI device was assumed to be zero. This is incorrect for a short-channel FDSOI device. The scale length associated with

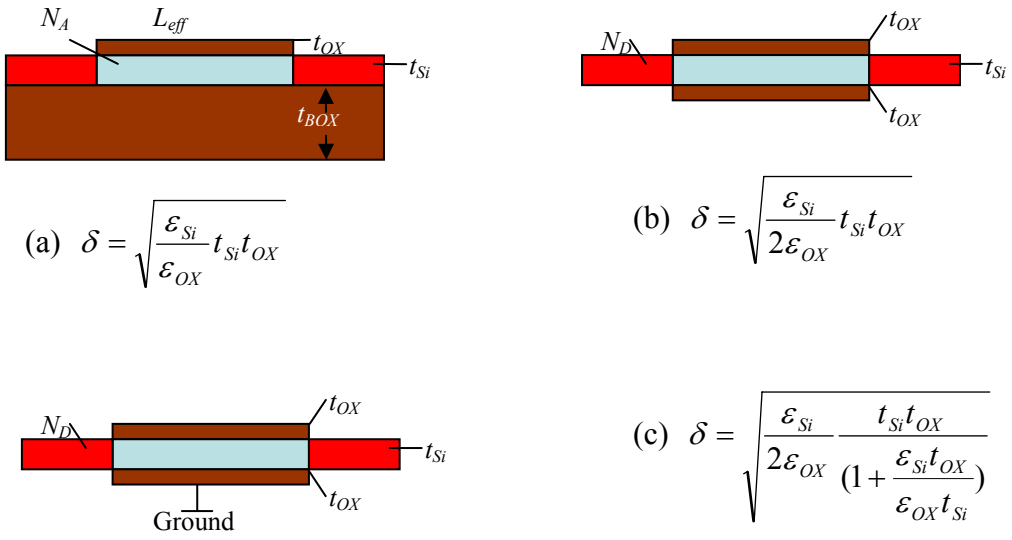

Fig. 2.4 The (a) conventional, (b) gate-all-around, and (c) ground plane SOI structures and the corresponding device scale length δ. Adapted from [2.6].

the short-channel effect for several advanced devices were developed by R. H. Yan (Fig. 2.4) [2.6]. They are proportional to the geometric mean of the oxide and silicon

film thickness. The minimum scalable channel length of a FDSOI device can be simply projected by its scale length. It was also pointed out for the first time that SOI CMOS cannot be scaled to as short a channel length as double-gate CMOS. Yan's model has large errors in minimum scalable channel length when one dielectric is much thicker than the other. Woo *et al.* [2.7] scaled up the gate oxide thickness of a FDSOI device by a factor of 3 and eliminated the boundary condition at the silicon/oxide interface by making the dielectric constant in the scaled oxide region the

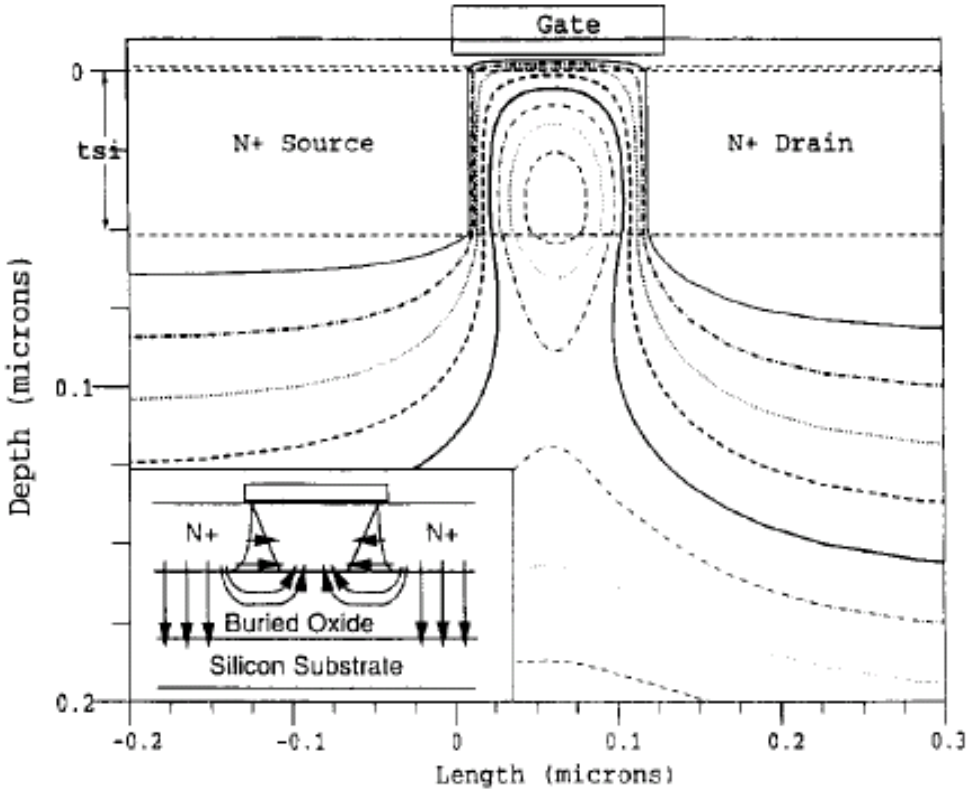

Fig. 2.5 Electric potential contours in a SOI device indicating 2-D field coupling through the buried oxide. Electric field lines (shown schematically in the inset) can be drawn perpendicular to the potential contours. Adapted from [2.8].

same as silicon. This assumes that normal electric field inside the BOX dominates. Those approximations are valid only when the gate insulator and the BOX are much

thinner than the silicon region. Lisa T. Su [2.8] explored the deep-submicron SOI MOSFETs design space by 2-D numerical simulations. She showed that the additional field coupling through the SOI buried-oxide (Fig. 2.5) further aggravates the short-channel effect. H.-S. Philips Wong *et al*. [2.9] investigated the severity of short-channel effect of 25-nm SOI and double-gate MOSFETs based on 2-D simulations. Even though [2.8] and [2.9] showed poor short-channel effects in FDSOI devices, the results were not generalized and a clear guideline on the scaling of FDSOI MOSFETs is still lacking. In the next chapter, we start with a discussion on the failure of general scale-length model in SOI MOSFETs. An empirical scaling rule for undoped fully-depleted SOI MOSFETs is presented based on simulation analysis.

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CHAPTER 3

Analysis of Short-Channel Effects in Undoped SOI MOSFETs

3.1 Device structures for 2-D numerical simulation

The design study of the scaling limit of SOI MOSFETs is carried out by TCAD simulation tools. TCAD is a synergistic combination of process, device and circuit simulation, and modeling tools. Instead of costly, time-consuming test wafer runs when characterizing or developing a new semiconductor device and technology, TCAD simulation tools are widely used by device engineers nowadays to efficiently support and optimize semiconductor technology and devices. The TCAD tool DESSIS used in our work is provided by SYNOPSYS. DESSIS is a device simulation tool which numerically simulates the electrical behavior of a single semiconductor device or several physical devices combined in a circuit. It solves fundamental and physical partial differential equations that describe the carrier distribution and conduction mechanism in discretized geometries, representing layer systems in a semiconductor device or small scale circuits with a few devices. This deep physical approach gives DESSIS simulation predictive accuracy.

DESSIS is used to calculate the low-drain threshold voltage shift, ΔV_T, and

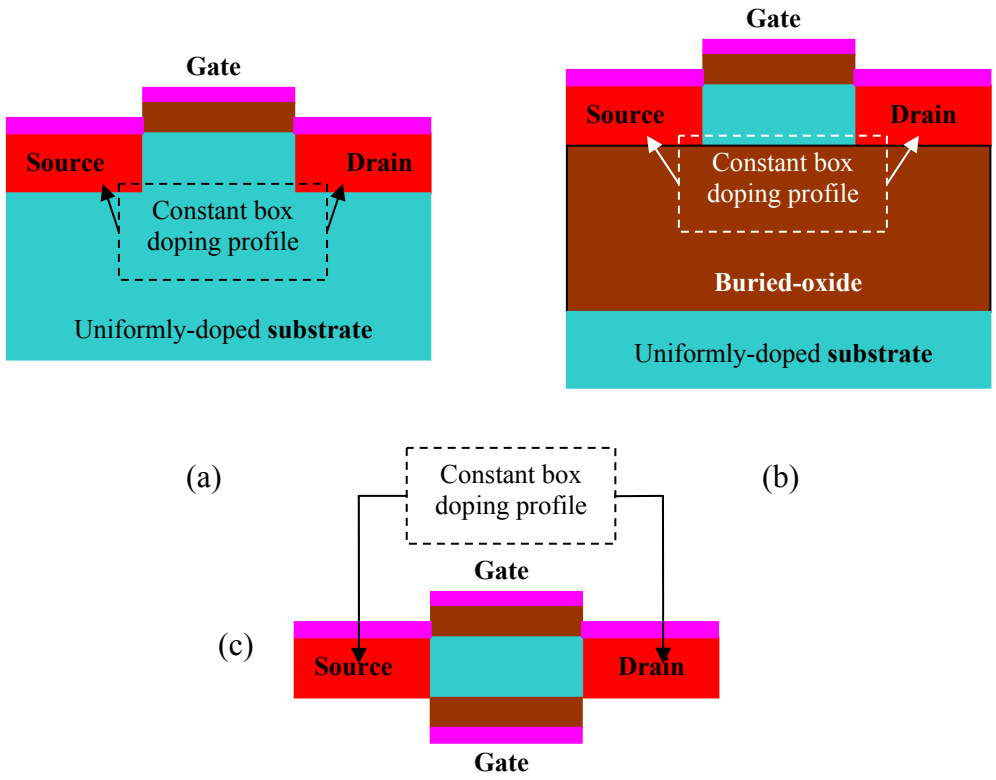


Fig. 3.1 Device structures of (a) bulk, (b) SOI, and (c) double-gate MOSFETs used in 2-D numerical simulations. Box-like doping profile is assumed in our design study.

drain-induced barrier lowering (DIBL) in the following discussions of the short-channel effect in bulk, double-gate, fully-depleted(FD) SOI MOSFETs as a function of device parameters. The simulated device structures are shown in Fig. 3.1. In our design study, we focus on FDSOI devices with a thick buried-oxide (thickness ~100 nm) since FDSOI devices with a thin buried-oxide (thickness <50 nm) are double-gate-like devices and the scaling limit of double-gate MOSFETs is already known. For future reference, all FDSOI devices in the rest of the thesis mean FDSOI devices with a thick buried-oxide. Box-like uniform doping profile is used in source and drain to keep the effective channel length L of the device at a constant value over a large range of channel doping. Since we only consider the electrostatic integrity of

bulk, double-gate, and SOI MOSFETs, constant mobility is assumed for carriers.

The use of polysilicon gates is a key advance in modern CMOS technology, since it allows the source and drain region to be self-aligned to the gate, thus eliminating parasitics from overlay errors [3.1]. However, the polysilicon-gate depletion effect occurs when it is not doped heavily enough in a MOSFET. The band diagram in Fig. 3.2 illustrates the polysilicon-gate depletion effect in a p-type MOS

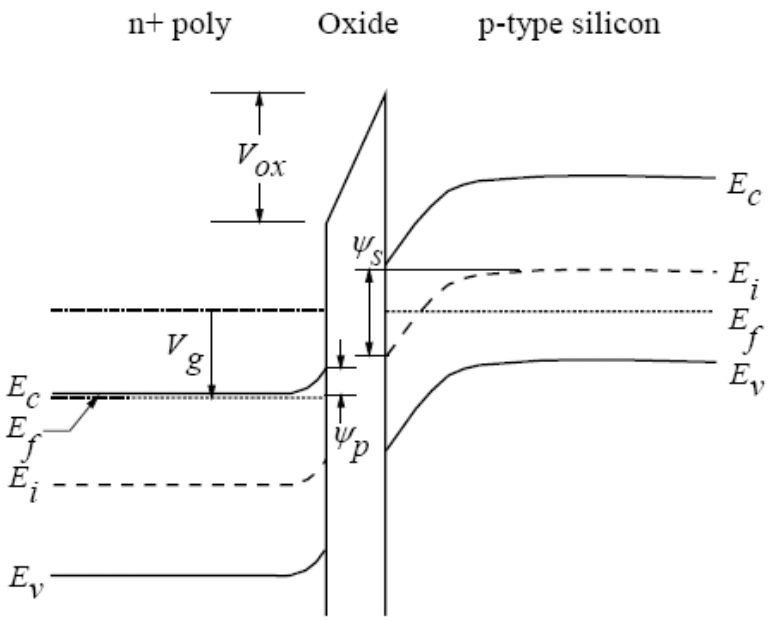


Fig. 3.2 Band diagram showing polysilicon-gate depletion effects when a positive voltage is applied to the N+ polysilicon gate of a p-type MOS capacitor. ψ_s is the amount of band bending in the bulk silicon. ψ_p is the amount of band bending in the N+ polysilicon gate.

capacitor biased into inversion. Since the oxide field points in the direction of accelerating a negative charge toward the gate, the bands in the N+ polysilicon bend slightly upward toward the oxide interface. This depletes the surface of electrons and

forms a thin space-charge region in the polysilicon layer. The depletion charges on both sides of the gate dielectric are equal and, therefore, one can obtain the depletion width t_p in the N+ polysilicon by $t_p = \frac{\varepsilon_{Si} E_s}{qN_p}$, where E_s is the surface field normal to the gate dielectric, and N_p is the doping concentration of the N+ polysilicon. For example, t_p is about ~1 nm with E_s equal to ~ 1.6MV/cm and N_p equal to ~10^{20} 1/cm^3. Since one can not dope the polysilicon gate to have a gate work function which locates outside silicon bandgap, t_p can be comparable to the gate dielectric thickness in a sub-20nm MOSFET design. The polysilicon-gate depletion results in an additional capacitance in series with the gate capacitance, which in turn leads to a reduced inversion-charge density and degradation of the MOSFET intrinsic capacitance and transconductance. Therefore, to obtain low-threshold MOSFETs, a metal gate with work function between mid-gap and N+ polysilicon (for nMOSFET) gate work function is assumed to be technically available so that the threshold voltage of long-channel MOSFETs is ~0.4 V and ~0.3 V for short-channel MOSFETs in our design study.

The low-drain threshold voltage shift of any short-channel device, ΔV_T, is calculated by $\Delta V_T = V_T$ (L=1μm)- V_T (short-channel device) and the DIBL=V_T (V_{ds}=50 mV)- V_T (V_{ds}=1 V). Both ΔV_T and DIBL are measured at $I_{ds}=10^{-8}$(W/L).

3.2 Short-channel effect

Short-channel effect emerging as the channel length of a MOSFET is aggressively scaled. When CMOS VLSI systems are fabricated on a wafer, channel length of any device on the wafer varies from chip to chip statistically. Therefore, one must ensure that the threshold voltage of the minimum-channel-length device on the chip does not become too low. The physics of short-channel effect can be understood by considering the surface potential barrier (to electrons for an n-channel MOSFET) in the channel region shown in Fig. 3.3. Under off condition, the potential barrier (p-type region) prevents electron current from flowing to the drain. For a long-channel

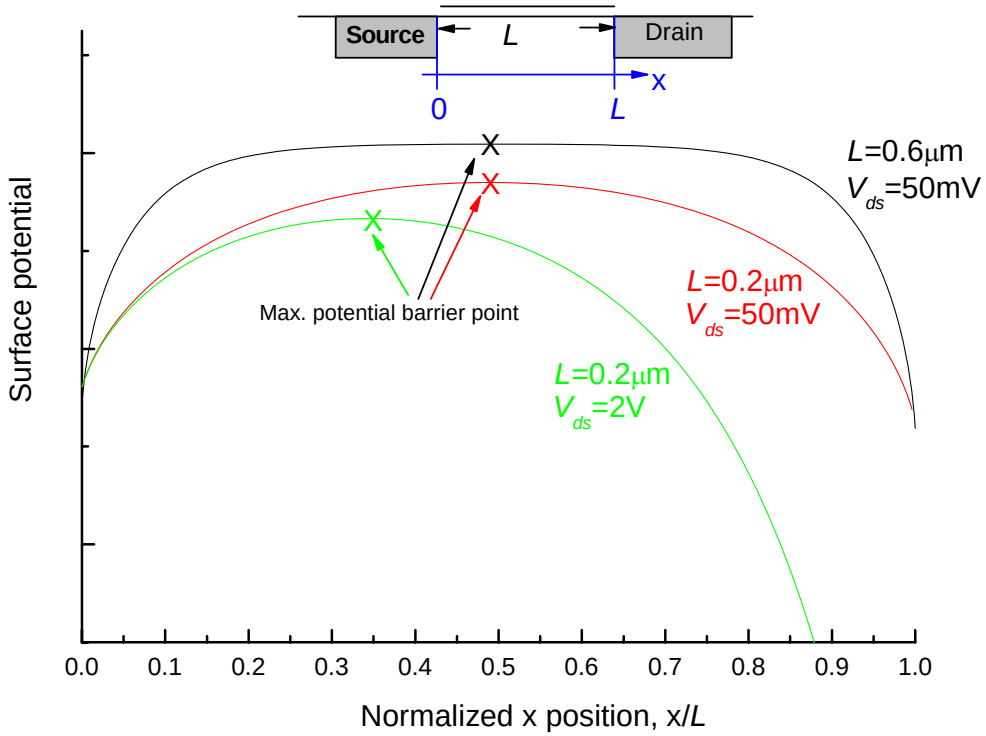


Fig. 3.3 Surface potential versus lateral distance (normalized to the channel length L) from the source to the drain for (a) a long-channel (L=0.6 μm) MOSFET biased at a low drain voltage, (b) a short-channel (L=0.2 μm) MOSFET biased at a low drain voltage, (c) a short-channel (L=0.2 μm) MOSFET biased at a high drain voltage. The gate voltage is the same for all three cases.

MOSFET, the potential barrier is flat in the most part of the channel region. Source/drain lateral-field coupling into channel only takes place in the very ends of the channel. However, for a short-channel MOSFET, the source/drain lateral fields penetrate deeply into the center of the channel and lower the potential barrier between the source and drain. The barrier-lowering in a short-channel MOSFET leads to threshold voltage roll-off and a substantial increase of the subthreshold current (Fig. 3.3). When a high drain voltage is applied to a short-channel MOSFET, the potential barrier is lowered even more, resulting in further decrease of the threshold voltage. The point of maximum barrier also shifts toward the source end as shown in Fig. 3.3.

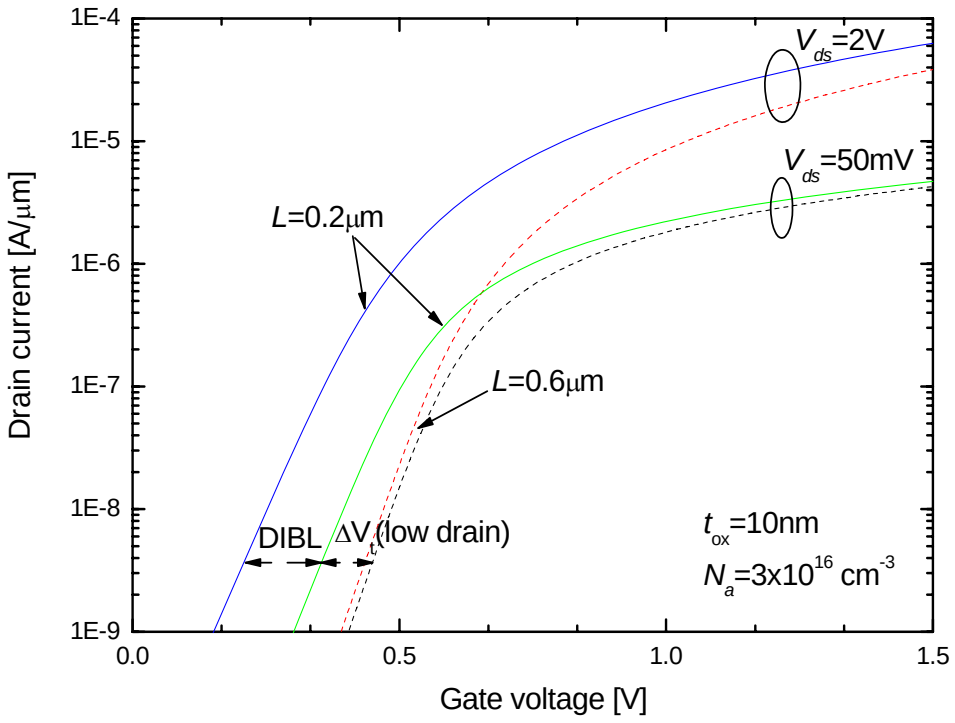


Fig. 3.4 Subthreshold characteristics of long- and short-channel MOSFETs biased at low and high drain voltages.

This effect is referred to as *drain-induced-barrier-lowering* (*DIBL*). Fig. 3.4 shows the subthreshold characteristics of long-channel (L=0.6 μm) and short-channel (L=0.2 μm) MOSFETs biased at different drain voltages. For the long-channel device, the subthreshold current is independent of drain voltage ($\geq 2kT/q$). However, for the short-channel device, a parallel shift of the curve to a lower threshold voltage at a high drain voltage can be observed. The subthreshold slope starts to degrade as the surface potential is more controlled by the drain than by the gate. Eventually, a short-channel MOSFET reaches the punch-through condition when the gate totally loses control of the channel and high drain current persists independent of gate voltage.

3.3 Inapplicability of the general scale-length model

3.3.1 Correlations between scale length and lateral field penetration

To understand the role of the lateral field in a short-channel MOSFET, the 2-D Poisson's equation is written in terms of electric field as:

$$\frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} = \frac{\rho}{\varepsilon_{Si}} \tag{3.1}$$

Here E_x is the electric field in the horizontal direction and E_y is the electric field in the vertical direction. The depletion charge density ρ can be considered as being split into two parts: $\varepsilon_{Si}\frac{\partial E_y}{\partial y}$ is controlled by the gate field in the vertical direction, and $\varepsilon_{Si}\frac{\partial E_x}{\partial x}$ is controlled by the source-drain lateral field. The lateral field is negligible in a

long-channel device and the gate vertical field controls almost all of the depletion charge. In contrast to a long-channel device, the lateral field becomes appreciable in a short-channel device. Fig. 3.5 illustrates the magnitude of the lateral field along the channel length direction of double-gate MOSFETs obtained from 2-D numerical simulations. Examples for bulk MOSFETs can be found in [3.2]. The lateral field is highest at the source and drain junctions and decreases exponentially toward the middle of the channel. At low drain voltages, the source and drain lateral fields cancel each other right at the center of the channel. The zero-field point is shifted toward the

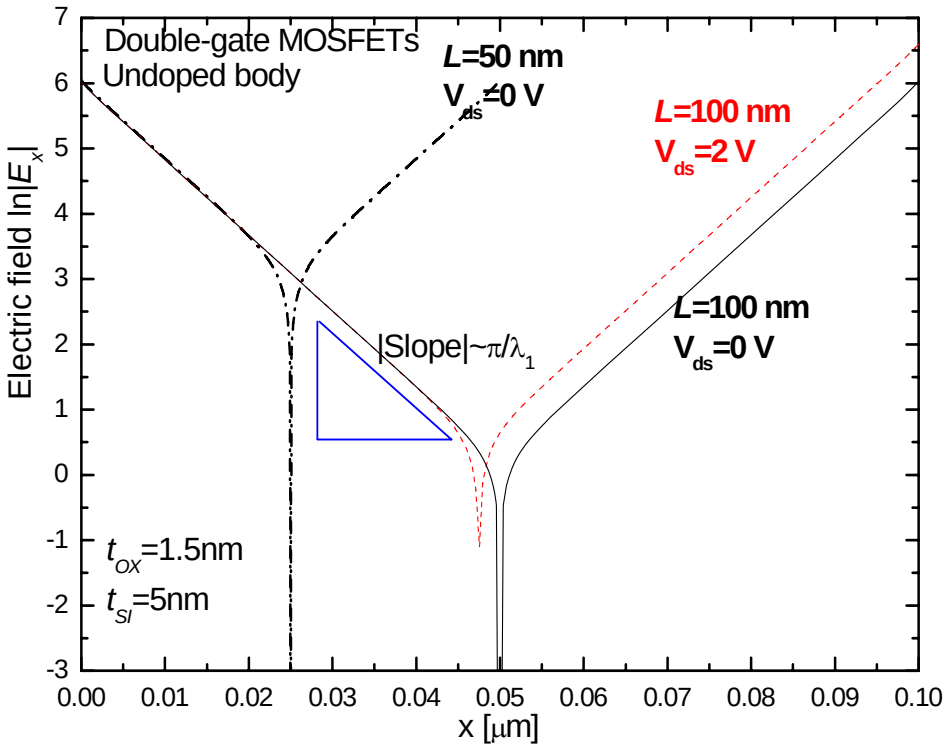


Fig. 3.5 Simulated lateral field as a function of lateral distance along a horizontal cut at the gate oxide/silicon body interface for two different devices biased at different drain voltages.

source side due to higher drain field as the device is biased at a high drain voltage. The curve becomes asymmetric and the lateral field intensity is increased even further by the application of a high drain voltage. The zero-field point corresponds to the point of maximum potential barrier in Fig. 3.3. The characteristic length of the exponential decay remains unchanged when the channel length becomes shorter. The magnitude of the lateral field near the middle of the device increases significantly. This depicts the penetration of source and drain fields into the channel region of a short-channel MOSFET. This magnitude of the lateral field along the channel direction is well

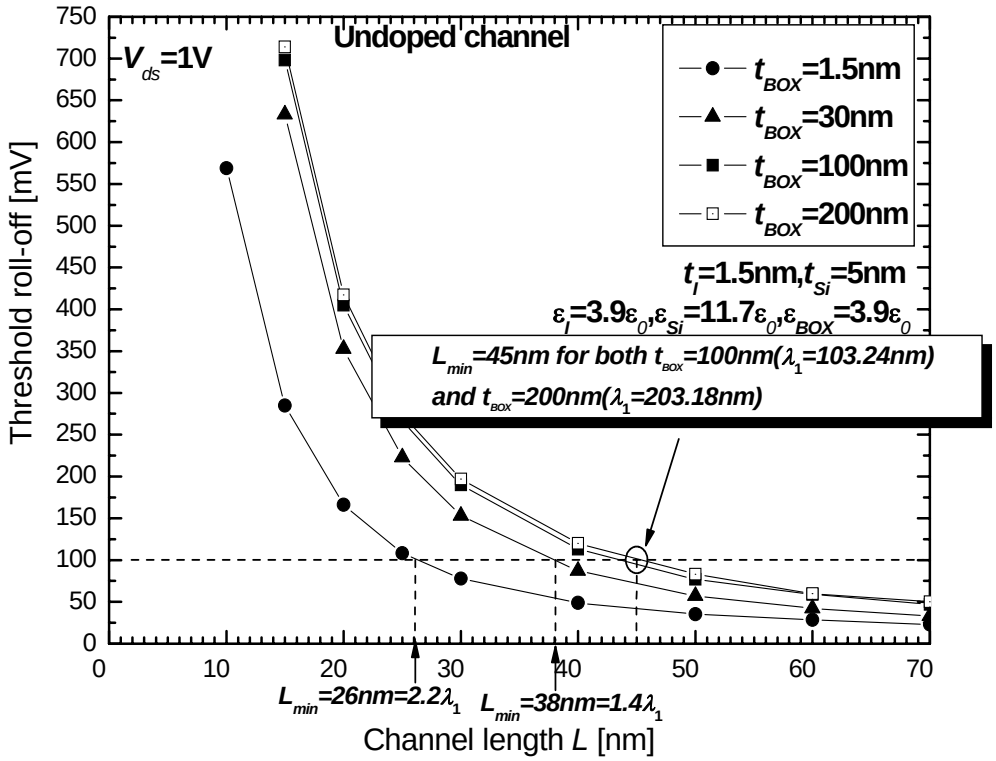


Fig. 3.6 High-drain threshold roll-offs for FDSOI MOSFETs with different BOX thickness. $L_{\min}$ is defined by setting a maximum tolerable high-drain threshold roll-off to be 100 mV. [3.4]

modeled by Nguyen and D. Frank in [3.2, 3.3]. By taking the first-order derivative of u_{L2} and u_{R2} in (2.21) and (2.22), one can find out that the magnitude of the lateral field is governed by the factor $\exp(-\pi x/\lambda_1)$. The slope of the curve in Fig. 3.5 of 3-layer dielectric MOSFETs is related to the scale length by

$$|\text{Slope}| \sim \frac{\pi}{\lambda_1} \tag{3.2}$$

Presumably, one can predict the minimum scalable channel length ($L_{min} \cong 2\lambda_1$) of 2-layer or 3-layer dielectric MOSFETs by extracting the scale length λ_1 from lateral-field analysis in a MOSFET, or by numerically solving λ_1 from the three-tangent equation (2.24). To test the L_{min} prediction of fully-depleted SOI MOSFETs with standard thick buried-oxide in general scale-length model, an extensive two-dimensional device simulation is carried out with the results shown in Fig. 3.6. A maximum allowable high-drain threshold roll-off is set to be 100 mV to define the L_{min} of a fully-depleted SOI device. All L_{min}'s in the rest of the thesis are obtained by this criterion. It is indicated in Fig. 3.6 that, for t_{BOX}=1.5 nm (DG-like), L_{min}=26 nm ($\approx 2.2\lambda_1$) is consistent with the $L_{min} \approx 1.5\lambda_1 \sim 2\lambda_1$ criterion in the general scale-length model. However, for t_{BOX}=30 nm, L_{min}=38 nm ($\approx 1.4\lambda_1$) starts to deviate from the scale-length model. In addition, for both t_{BOX}=100 nm (λ_1=103.24 nm) and t_{BOX}=200 nm (λ_1=203.18 nm), L_{min} remains at 45 nm, much shorter than $1.5\lambda_1$. These results show that the short-channel effect in a thick-BOX fully-depleted SOI MOSFET is not as poor as predicted by the general scale-length model. The general scale-length model works well only when the buried-oxide thickness is much smaller than the

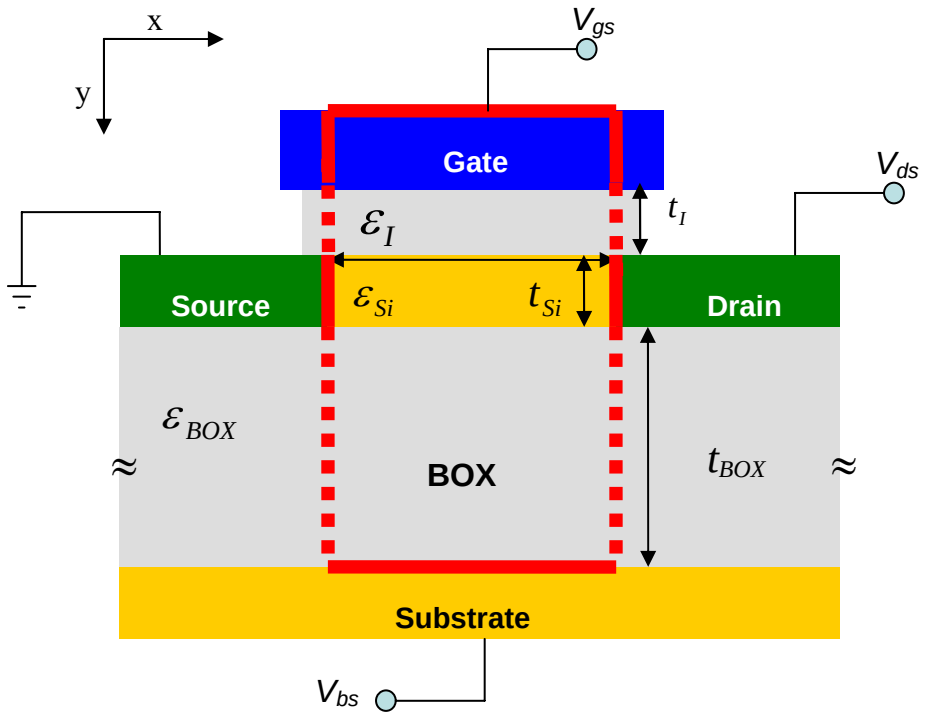
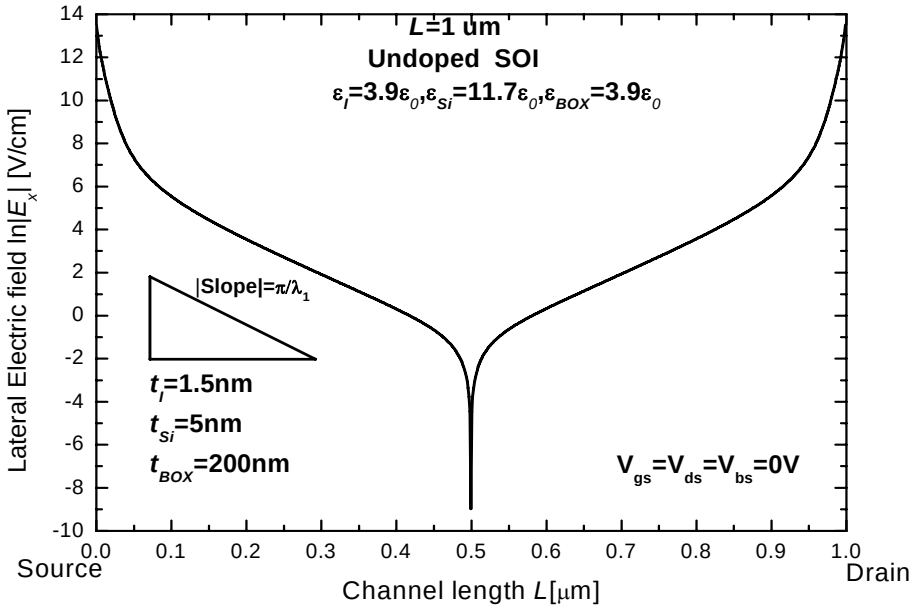


Fig. 3.7 Simplified geometry for analytically solving Poisson's equation in a short-channel FDSOI MOSFET. Dashed lines mean unspecified potential on the boundaries.

channel length. An enclosed BOX (see Fig. 3.7) with specified electrostatic potential on the boundaries can be defined for solving Poisson's equation as a 2-D boundary value problem. The potential in the insulator gap region between the source/drain and gates can be well-approximated by linear interpolation [3.4]. When the channel length of a FDSOI device is much smaller than the BOX thickness, the linear approximation fails and the potential on the boundaries of the enclosed box in the thick gap BOX region cannot be specified. To provide a further understanding of this observation, we need to do the lateral-field analysis and look into the field pattern in the buried-oxide region of long- and short-channel FDSOI devices.

3.3.2 Electric field distribution in thick buried-oxide

The lateral-field variation along the channel direction and the electric field pattern for long- and short-channel ultra-thin body FDSOI devices (n-channel MOSFETs) with standard thick BOX obtained from 2-D numerical simulations are shown in Fig. 3.8 and 3.9. Both cases are examined under subthreshold conditions. According to the discussion in section 3.3.1, the lateral field at the channel surface E_x is governed by the factor $\exp(-\pi x/\lambda_1)$. The characteristic length of the exponential decay is well-depicted by λ_1/π in long-channel FDSOI devices (Fig. 3.8(a)) because the field pattern in the BOX region is roughly one-dimensional (Fig. 3.8(b)). Source/drain-to-channel lateral-field coupling happens only near the very ends of the channel. However, the characteristic length of exponential decay for short-channel FDSOI devices (Fig. 3.9(a)) is shorter than expected from the general scale-length model. The 2-D field pattern (Fig. 3.9(b)) in the BOX suggests that the lateral-field penetration into the BOX depends on the channel length, i.e., the source-to-drain distance. This also implies that the "effective" BOX thickness (hence, the "effective" scale length) for short-channel SOI MOSFETs is much thinner than the physical thickness. To learn how the scale length varies with the channel length in FDSOI devices, the scale length λ_1^* of FDSOI devices with different channel lengths is calculated by $\frac{\pi}{|slope|}$, where the slope is measured from doing lateral-field analysis in each device. Fig. 3.10 shows that the scale length λ_1^* extracted from lateral-field analysis varies with channel length. When the channel length is long (L~1 μm), the



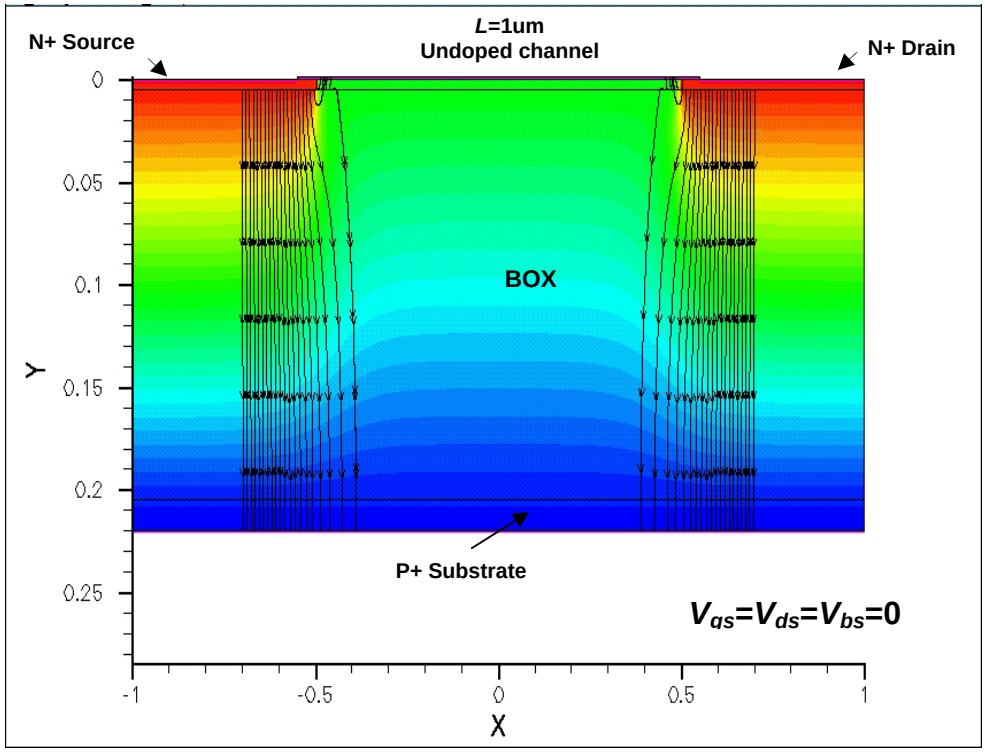


Fig. 3.8 Simulated (a) lateral-field variation along the channel surface and (b) field pattern for a long-channel thick-BOX FDSOI device [3.5].

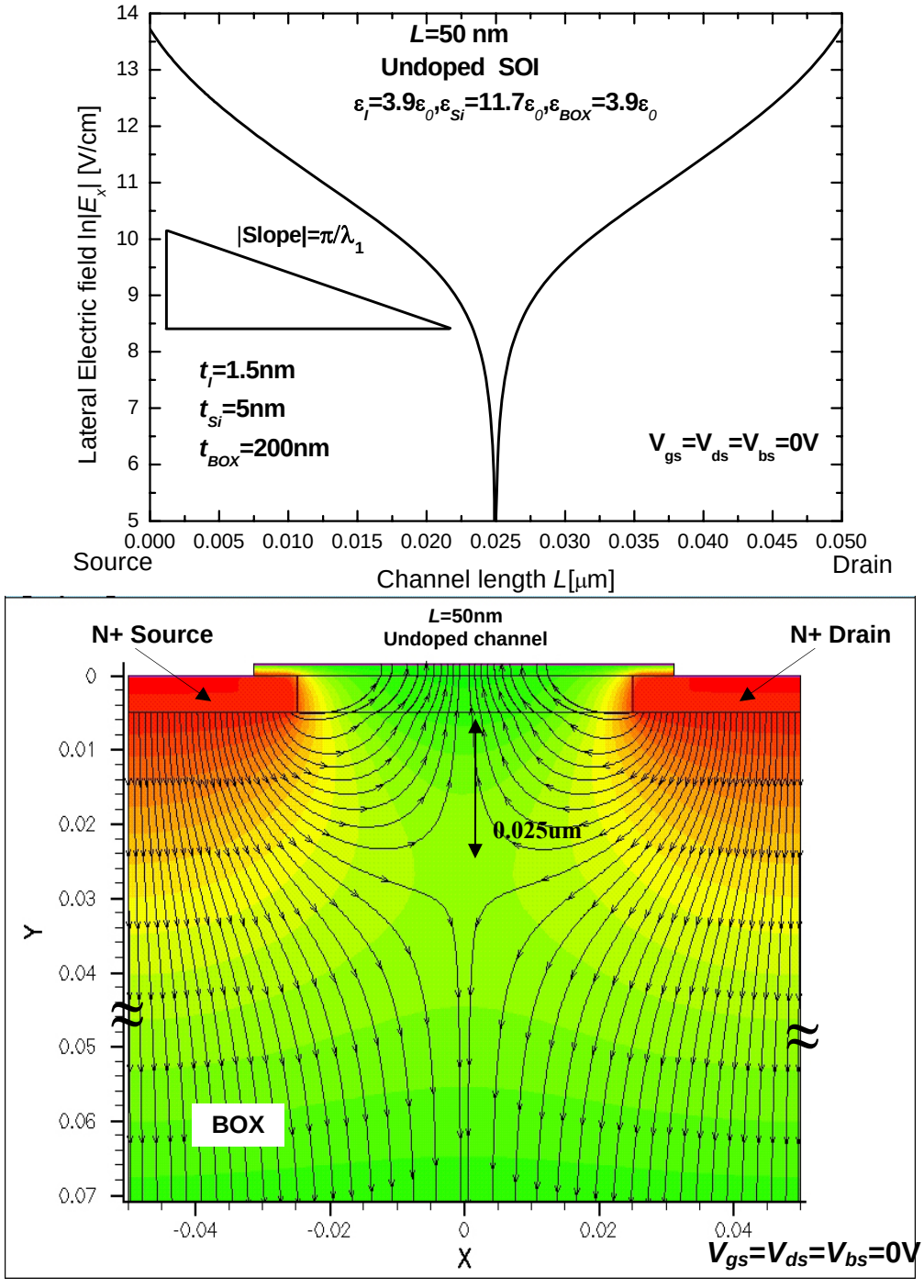


Fig. 3.9 Simulated (a) lateral-field variation along the channel surface and (b) field pattern for a short-channel thick-BOX FDSOI device [3.5].

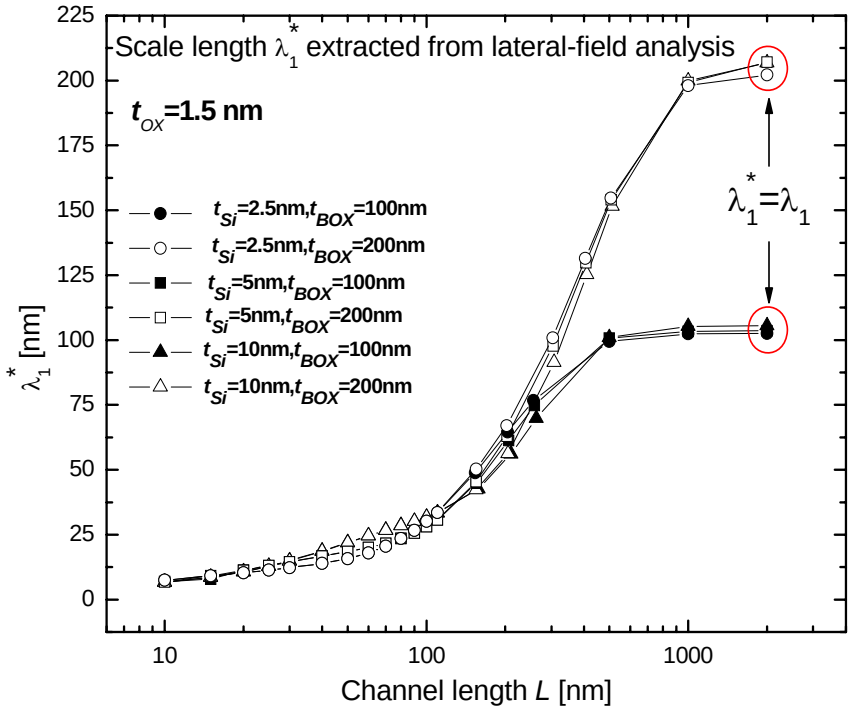


Fig. 3.10 The extracted scale length λ_1^* versus channel length. λ_1^* is calculated by $\frac{\pi}{|slope|}$, where the |slope| is obtained by lateral-field analysis.

curve saturates at the analytical solution of λ_1 obtained from the general scale-length model. For short-channel FDSOI devices, the extracted scale length λ_1^* is independent of the standard thick BOX thickness and decreases with channel length L. According to the results shown in Fig. 3.10, the scale length is no longer a good indicator to know the severity of short-channel effect and the scaling limit of a FDSOI device. Therefore, extensive device simulations are needed to investigate the scaling rule and limit of ultra-thin body FDSOI MOSFETs.

3.4 Short-channel scaling of undoped FDSOI MOSFETs

In the rule of generalized scaling for bulk MOSFETs, both the gate oxide thickness and the gate-controlled depletion width in silicon must be reduced in proportional to the channel length. The scaling rules of undoped FDSOI MOSFETs are governed by Poisson's equation and determined extensively by 2-D numerical simulations. According the results shown in Fig. 3.6, the high-drain threshold roll-off is independent of the buried-oxide thickness when the t_{BOX} is larger than 100 nm. From logic intuition, the short-channel scaling of FDSOI devices may depend on the

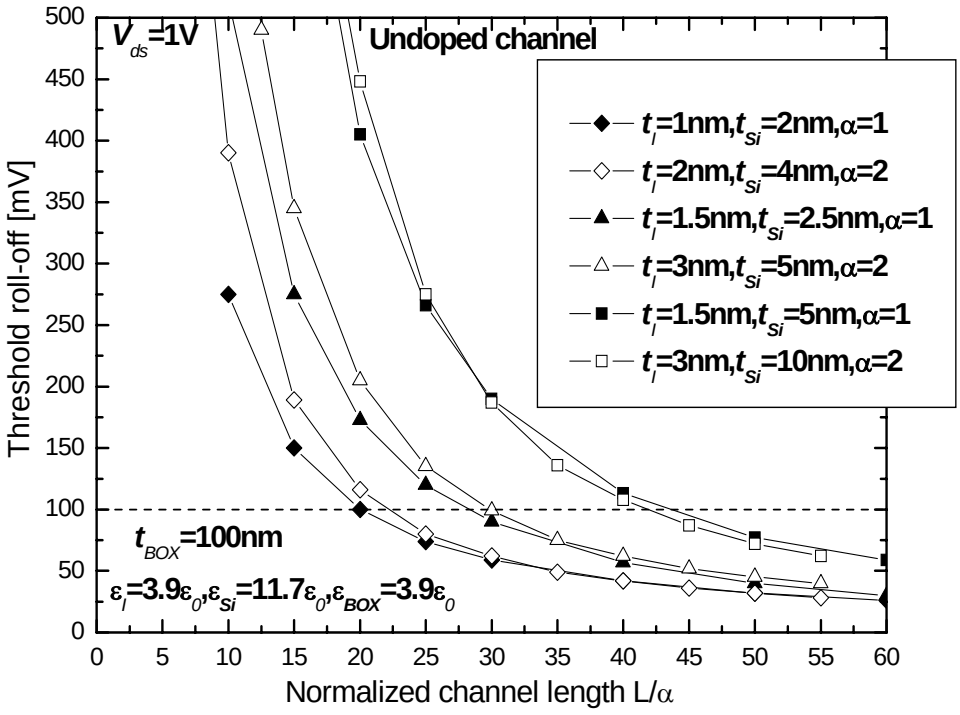


Fig. 3.11 General scaling rules of ultra-thin body FDSOI MOSFETs. For given permittivities ε_I and ε_{Si}, if (t_I, t_{Si}) are both scaled by a factor of α, $L_{\min}$ is scaled by the same factor α [3.5], regardless of the BOX thickness.

silicon-film thickness, gate-insulator thickness and their permittivities. One expects that $L_{\min}$ is scaled by a factor of α if both t_I and t_{Si} are scaled by a factor of α and the BOX thickness is not a factor. To confirm our hypothesis, the high-drain threshold roll-offs of six FDSOI devices listed in Fig. 3.11 are investigated. It is indicated in Fig. 3.11 that $L_{\min}$ is scaled by a factor of 2 if both t_I and t_{Si} are scaled by a factor of 2, regardless of the BOX thickness. Although the results shown in Fig. 3.11 give a guideline on the short-channel scaling of FDSOI devices, one can not predict the $L_{\min}$ of a FDSOI device with a given $(t_I, t_{Si}, \varepsilon_I, \varepsilon_{Si})$. Since the $L_{\min}$ is a

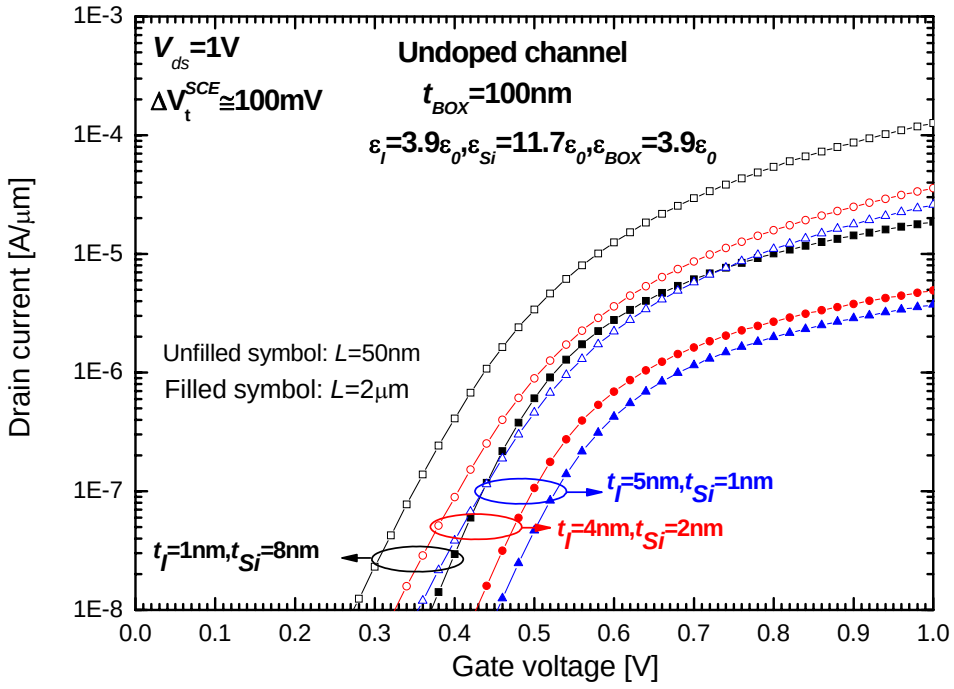


Fig. 3.12 Different combinations of (t_I, t_{Si}) which a yield 100-mV high-drain threshold roll-off at a given channel length of 50 nm and ($\varepsilon_I = 3.9\,\varepsilon_0$, $\varepsilon_{Si} = 3.9\,\varepsilon_0$).

function of (t_I, t_{Si}, ε_I, ε_{Si}), there are different combinations of (t_I, t_{Si}) which generate a 100-mV high-drain threshold roll-off at a given channel length L= L_{min} and (ε_I, ε_{Si}), as can be seen in Fig. 3.12. A FDSOI with L_{min}=50 nm can be achieved by setting (t_I, t_{Si})=(1 nm, 8 nm), (5 nm, 1 nm) or (4 nm, 2 nm). There are many other combinations of (t_I, t_{Si}) which are not shown in Fig. 3.12. Therefore, a constant L_{min} contour including different combinations of (t_I, t_{Si}, ε_I) is required to develop an empirical equation for L_{min} prediction. Fig. 3.13 illustrates how we find different combinations of (t_I, t_{Si}) for L_{min} =20 nm, 40 nm, and 60 nm. We set the gate dielectric

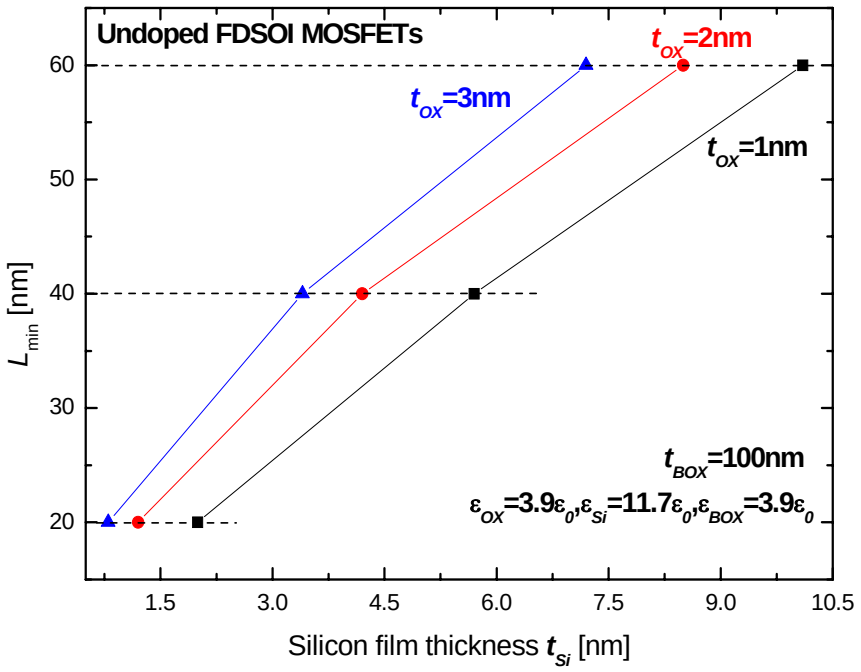


Fig. 3.13 Illustration of obtaining different combinations of (t_I, t_{Si}) for FDSOI devices with gate oxide at a given L_{min}. The gate-oxide thickness and channel length are fixed while the silicon-film thickness is adjusted to yield a 100-mV high-drain threshold roll-off. A constant L_{min} contour can be plotted by putting all combinations of (t_I, t_{Si}) in a $t_I - t_{Si}$ plane.

permittivity to $3.9\varepsilon_0$ and keep t_I=1 nm, 2nm, and 3 nm and adjust t_{Si} to have 100-mV high-drain roll-off at given channel length L=20 nm, 40 nm, and 60 nm. A constant $L_{\min}$ contour can be plotted by putting all combinations of (t_I, t_{Si}) in a $t_I - t_{Si}$ plane. By analyzing the data points in Fig. 3.13, one can find a simple relation between $L_{\min}$ and (t_I, t_{Si}), i.e., $L_{\min} \approx (t_{Si} + 3t_{OX})$. Presumably, the factor of 3 is the permittivity ratio $\frac{\varepsilon_{Si}}{\varepsilon_I}$. To confirm our assumption, constant $L_{\min}$=60 nm contours are plotted in a $t_I - t_{Si}$ plane for $\frac{\varepsilon_I}{\varepsilon_0}$=3.9, 11.7, and 35.1 in Fig. 3.14. Each $L_{\min}$

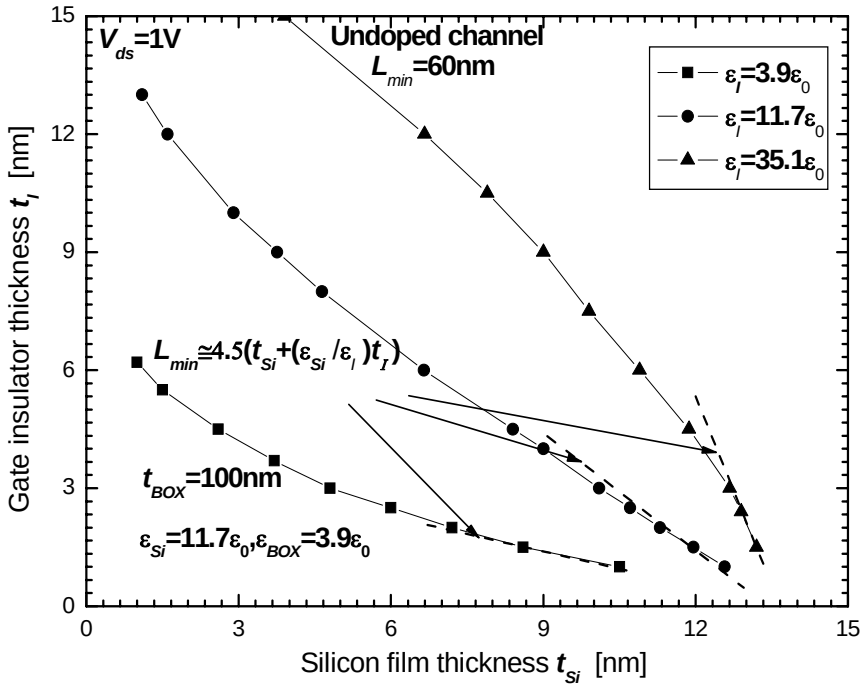


Fig. 3.14 Constant minimum scalable channel length ($L_{\min}$=60 nm) contours for undoped ultra-thin body FDSOI with three different gate dielectrics. Dashed lines at the lower right corner indicate the linear approximations for $L_{\min}$ [3.5].

contour is composed of different combinations of t_I and t_{Si}, which yield a 100-mV high-drain threshold roll-off at a given channel length of 60 nm. The results in Fig. 3.14 can be generalized to other values of $L_{\min}$ by scaling all t_I, t_{Si} and $L_{\min}$ by a common factor α, as demonstrated in Fig. 3.11. High-k gate insulators allow thicker t_I for given t_{Si} and $L_{\min}$. The decreasing slope of the constant $L_{\min}$ contour with $\frac{\varepsilon_I}{\varepsilon_0}$ =35.1 toward the upper left corner suggests that less benefits can be gained from thick high-k dielectrics. For a given ε_I, same $L_{\min}$ can be achieved with a thin t_{Si} and thick t_I or with a thin t_I and thick t_{Si}. Because of the difficulty in manufacturing ultra-thin silicon films, it is of more practical interest to consider the $t_I < t_{Si}$ regime in the lower right corner of Fig. 3.14, where $L_{\min}$ can be well approximated by:

$$L_{\min} \cong 4.5(t_{Si} + \frac{\varepsilon_{Si}}{\varepsilon_I} t_I) \tag{3.3}$$

Equation (3.3) is valid for a wide range of $\frac{\varepsilon_{Si}}{\varepsilon_I}$ studied. For ε_I =3.9ε_0 and 11.7ε_0 in Fig. 3.14, the applicability of the linear approximation of $L_{\min}$ requires $\frac{t_{Si}}{t_I} > \sim 2$ and $\frac{t_{Si}}{t_I} > \sim 4$ for the high-k dielectric ε_I =35.1ε_0. For very high permittivity gate insulators, the second term in (3.3) becomes negligible and $L_{\min}$ is limited by the silicon film thickness to ~ 5t_{Si} this is in good agreement with the experimental results for $L_{\min}$ at DIBL ~ 50 mV in [3.6].

3.5 Summary

In this chapter, we pointed out the failure of the general scale-length model in the $L_{\min}$ prediction of FDSOI MOSFETs. An empirical $L_{\min}$ expression is developed by extrapolating the constant $L_{\min}$ contours of FDSOI devices. The factor $L_{\min}/(t_{Si}+\frac{\varepsilon_{Si}}{\varepsilon_I}t_I)\sim 4.5$ in (3.3) suggests that undoped FDSOI MOSFETs have worse short-channel effect than bulk CMOS, which has the factor $L_{\min}/(W_d+\frac{\varepsilon_{Si}}{\varepsilon_I}t_I)\sim 2$, where W_d is the depletion width. FDSOI devices can not be scaled as a short channel length as bulk devices with given ε_I, W_d (t_{Si} in FDSOI) and t_I. For a sub-20-nm FDSOI device design, it requires $(t_{Si}+\frac{\varepsilon_{Si}}{\varepsilon_I}t_I)<\sim 4$ nm which means both the gate-insulator and silicon-film thickness must be reduced in order to scale to shorter channel length. High-k gate dielectrics help to reduce the $(\varepsilon_{Si}/\varepsilon_I)t_I$ term in (3.3) so that ultimately $L_{\min}\approx 5t_{Si}$.

There are other factors such as body doping, substrate biasing, and the permittivity of buried-insulator ε_{BOX} which can improve the short-channel scaling of FDSOI MOSFETs. The impact on the short-channel scaling of FDSOI MOSFETs caused by those factors will be addressed in next chapter.

The text of Chapter 3, in part, is the reprint of the material as it appears in “On The Scaling Limit of Ultrathin SOI MOSFETs” by Wei-Yuan Lu and Yuan Taur,

IEEE Transaction on Electron Devices, May 2006. The dissertation author was the primary researcher of this paper.

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CHAPTER 4

Other Factors Affecting Short-Channel Scaling of FDSOI MOSFETs

4.1 Effect of body doping

In the previous chapter, the design space of fully-dpeleted SOI MOSFETs has been explored based on the assumption that the silicon body is undoped. In contrast to a bulk MOSFET, a SOI MOSFET can be undoped because it does not need doping to confine depletion width. The depletion width equals to the physical thickness of the silicon film. Scaling down the depletion width can be achieved by thinning down the silicon film thickness directly. Body doping can degrade carrier mobility owing to the impurity scattering and the depletion charges which can significantly increase the effective normal field. It also leads to dopant fluctuation problems which affect the operation of VLSI circuits.

However, there are several disadvantages of the undoped silicon body. Firstly, the undoped FDSOI MOSFETs need tunable metal gate work functioin to achieve multiple threshold-voltage requirements in a VLSI system design. Without the use of

the body doping as an approach to adjust the threshold voltage, it is a technical challenge to implement a VLSI system with undoped FDSOI MOSFETs. The tunable metal gate technology has not been well-developed because of technological difficulties [4.1, 4.2]. Nowadays body doping remains as an alternative method to appropriately adjust the threshold voltage. Secondly, the minimum scalable channel length $L_{\min}$ of undoped FDSOI MOSFETs with high-k gate dielectrics is limited by ~5x silicon film thickness (or "depletion width"), which is much worse than the $L_{\min}$ of bulk MOSFETs which is about ~2x depletion width. Compared to uniformly-doped FDSOI devices, the absence of depletion charges in undoped FDSOI MOSFETs gives rise to severe charge-sharing effect at the source/drain and worsens the short-channel effect.

To understand the body doping effect on short-channel effects, the high-drain roll-off of FDSOI nMOSFETs with different doping concentrations is investigated. A metal gate with N+ polysilicon gate work function (for nMOSFET) is assumed to be technically available to obtain a low threshold-voltage device. The effect of different body doping level on high-drain threshold roll-off of fully-depleted SOI MOSFETs is shown in Fig. 4.1. Light body doping only leads to the first-order effect on threshold voltage. Threshold-voltage shift due to light doping concentrations ($N_a = 3.9\times10^{15} cm^{-3}$ and $7.2\times10^{17} cm^{-3}$ cases in Fig. 4.1) can be estimated by $\frac{qN_a t_{Si} t_{OX}}{\varepsilon_{OX}}$ (for long-channel doped FDSOI devices), which is similar to bulk MOSFETs. The high-drain threshold roll-off of heavily doped FDSOI devices is close

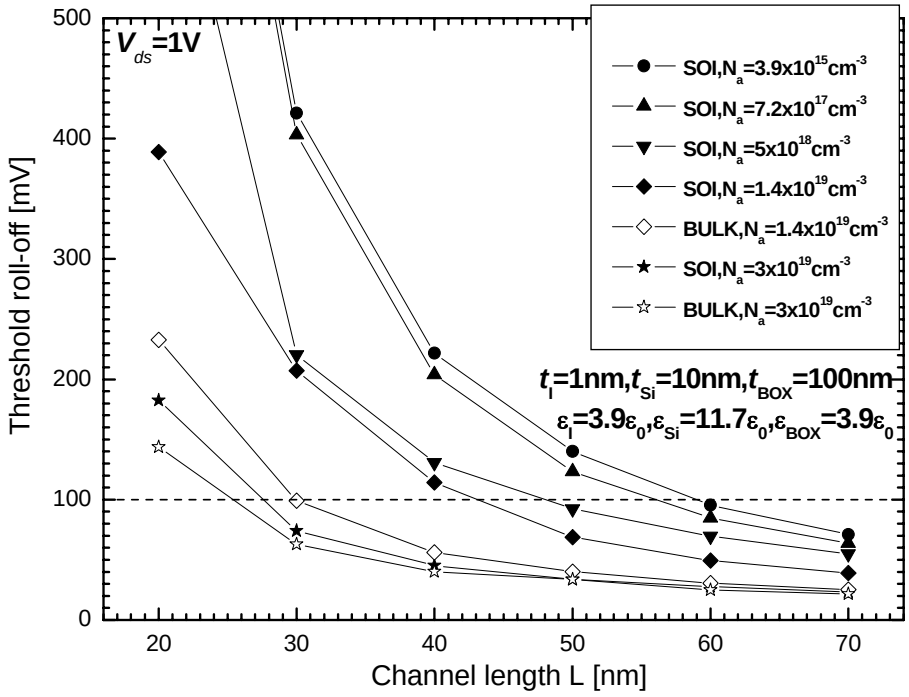


Fig. 4.1 High-drain threshold roll-offs for FDSOI and bulk nMOSFETs with different channel doping concentrations. The $L_{\min}$ of lightly doped FDSOI device can be reduced by a factor of 1.3 with a moderate channel doping concentration.

to that of bulk devices because the depletion width is thinner than the silicon film thickness. In other words, the silicon body is partially-depleted. For SOI MOSFET with $N_a = 3\times10^{19} cm^{-3}$, the short-channel effect is slightly worse than that of the bulk MOSFET because of a higher body potential caused by the floating-body effect.

The short-channel effect can be mitigated by the moderate body doping while the silicon body remains fully-depleted. Fig. 4.1 shows that the $L_{\min}$ of the lightly doped FDSOI device with $N_a = 3.9\times10^{15} cm^{-3}$ can be reduced by a factor of 1.3 by a doping concentration of $1\times10^{19} cm^{-3}$, which is different from the observation in [4.3].

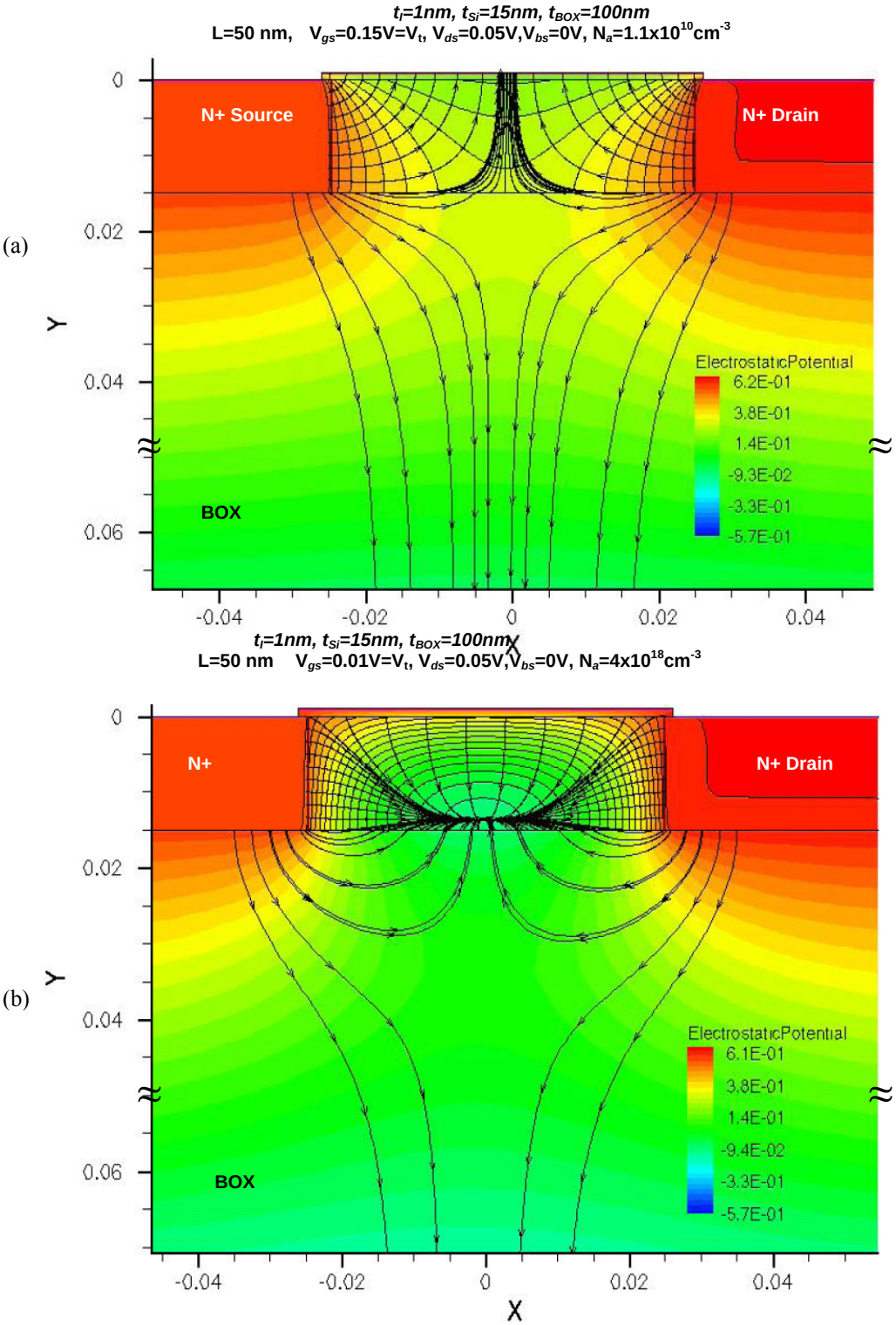


Fig. 4.2 Comparison of constant-potential contours and electric field patterns inside silicon body between (a) undoped and (b) doped FDSOI MOSFETs. Both devices are biased at the same off-current level.

The physical reason for the alleviation of short-channel effects in p-type doped FDSOI nMOSFETs can be explained by Fig. 4.2, which plots the potential contours and electric field lines for undoped and p-type doped FDSOI nMOSFETs biased at the same off-current level. The potential contours are equally spaced in both figures. For the undoped FDSOI MOSFET, a large portion of the source/drain lateral-field lines penetrate into channel through the undoped silicon body and buried-oxide and end at the gate electrode. In contrast to the undoped FDSOI MOSFET, the electric field lines inside p-type doped body emanating from source/drain are drawn by the negative space charges towards and end at the bottom of the silicon body. Thus the source/drain lateral field coupling into channel is minimized in a p-type doped FDSOI MOSFET. On the other hand, the small curvature of the potential contours in the p-type doped FDSOI MOSFET suggests that more ionized acceptors are controlled by the gate field in the vertical direction. The constant-potential contours in the undoped FDSOI device in Fig. 4.2(a) are more curvilinear than in the p-type doped FDSOI device in Fig. 4.2(b), which means the electric field in the lateral direction is appreciable. Consequently, p-type doped FDSOI MOSFETs show better short-channel effect.

The scaling rule of bulk CMOS is governed by Poisson's equation. To scale down the physical dimension of a bulk MOSFET with a substrate doping concentration N_a by a factor of α, one need to keep the Poisson's equation invariant under the transformation, $(x, y) \rightarrow (x, y)/\alpha$,

$$\frac{\partial^2\psi}{\partial(x/\alpha)^2}+\frac{\partial^2\psi}{\partial(y/\alpha)^2}=\frac{qN_a^{'}}{\varepsilon_{Si}}, \tag{4.1}$$

$N_a^{'}$ should be scaled up to $\alpha^2 N_a$. In other words, the substrate doping concentration of a bulk device needs to scale up by a factor of α^2 if the channel length, maximum depletion width, and gate dielectric layer thickness are scaled down by a factor of α. The short-channel scaling of doped FDSOI devices is independent of the BOX thickness because the lateral field coupling into channel via BOX does not go deep down to the bottom of the thick buried-oxide layer (Fig. 4.2). Following the same

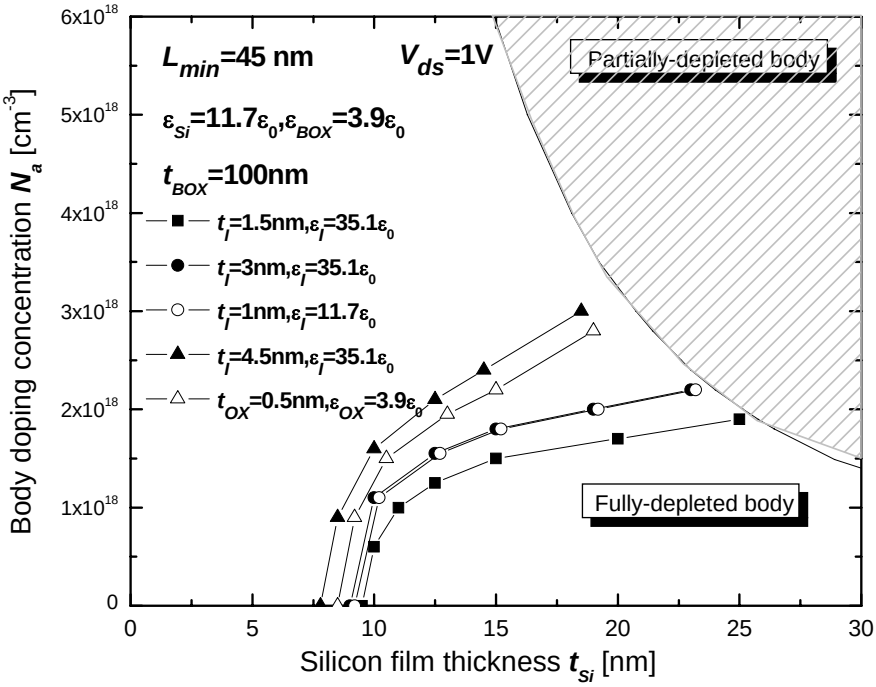


Fig. 4.3 Constant minimum channel length (L_{min}= 45 nm) contours for doped FDSOI devices with three different gate dielectrics [4.4].

approach to find the scaling rule of undoped FDSOI devices discussed in section 3.4,

one can find that the scaling rule of doped FDSOI devices is similar to bulk CMOS with the maximum depletion width replaced by the silicon film thickness.

To obtain a clear picture for the design space of doped FDSOI devices, constant $L_{\min}$ contours are plotted in a $N_a - t_{Si}$ plane with different gate dielectrics taken into account. The partially-/fully-depleted SOI boundary is given by using the depletion approximation for different body doping concentrations,

$$\max.\ \textit{depletion width}\ \ W_d = \sqrt{\frac{4\varepsilon_{Si} kT \ln(N_a / n_i)}{q^2 N_a}} \quad . \tag{4.2}$$

Equation (4.2) is valid for long-channel SOI MOSFETs. In Fig. 4.3, each $L_{\min}$ contour is composed of different combinations of N_a, t_I, and t_{Si} that yield a 100-mV high-drain threshold roll-off at a given channel length of 45 nm. The simulation results in Fig. 4.3 can be generalized to other values of $L_{\min}$ by scaling all t_I, t_{Si}, and $L_{\min}$ by a common factor of α but $1/\alpha^2$ for N_a, which is similar to the scaling of the bulk CMOS. High-k gate dielectrics allow thicker t_I for given N_a, t_{Si}, and $L_{\min}$ because of their thinner effective oxide thickness (EOT=$\frac{\varepsilon_{OX}}{\varepsilon_I} t_I$). According to the data points in Fig. 4.3, the $L_{\min}$ of doped FDSOI MOSFETs can be approximated by,

$$L_{\min} \cong (4.5 - \frac{\gamma t_{Si}}{W_d})(t_{Si} + \frac{\varepsilon_{Si}}{\varepsilon_I} t_I) \tag{4.3}$$

, where the fitting factor γ is given by,

$$\gamma = -14.33(\frac{\varepsilon_{Si}t_I}{\varepsilon_I t_{Si}})^2 - 2.14(\frac{\varepsilon_{Si}t_I}{\varepsilon_I t_{Si}}) + 2.88 . \quad (4.4)$$

The $\frac{\varepsilon_{Si}t_I}{\varepsilon_I t_{Si}}$ term in (4.4) can also be expressed in the form of the ratio between the depletion capacitance and the gate insulator capacitance of a doped FDSOI device. When the body of a FDSOI device is undoped, the $\frac{\gamma t_{Si}}{W_d}$ term is negligible because the calculated depletion width is much larger than the silicon film thickness in a sub-100 nm FDSOI device design. As a result, equation (4.3) becomes equation (3.3) for undoped FDSOI devices.

When the silicon body is doped toward the partially-/fully-depleted SOI boundary ($t_{Si} \approx W_d$) in Fig. 4.3, the $(4.5 - \frac{\gamma t_{Si}}{W_d})$ term equals ~2 and equation (4.3) becomes similar to the $L_{\min}$ prediction equation of bulk CMOS, which is $L_{\min} \cong 2\lambda_1 = 2(W_d + \frac{\varepsilon_{Si}}{\varepsilon_I} t_I)$. For extremely scaled high-k gate dielectrics, the design space of the silicon film thickness can be relaxed to a large extent by doping the body toward the partially-/fully-depleted SOI boundary in Fig. 4.3. In chapter 3 we know that the $L_{\min}$ of undoped FDSOI MOSFETs is limited to ~$5\,t_{Si}$ even with high-k gate dielectrics. The $L_{\min}$ limitation can be relaxed to ~$2\,t_{Si}$ by body doping which becomes

the same as the ~$2W_d$ limitation in bulk MOSFETs with high-k gate dielectrics.

Body doping helps improve the subthreshold slope (Fig. 4.4) and reduce the threshold-voltage sensitivity to silicon-film thickness. At present, it is a technological challenge to manufacture an atomically flat, ultra-thin silicon layer (t_{Si} ~< 5 nm) on a SOI wafer. The threshold-voltage shift due to quantum-mechanical effect becomes appreciable when the t_{Si} of a FDSOI device is scaled below 5 nm [4.5]. Therefore, the threshold voltage is sensitive to variations of the silicon layer thickness. Body doping

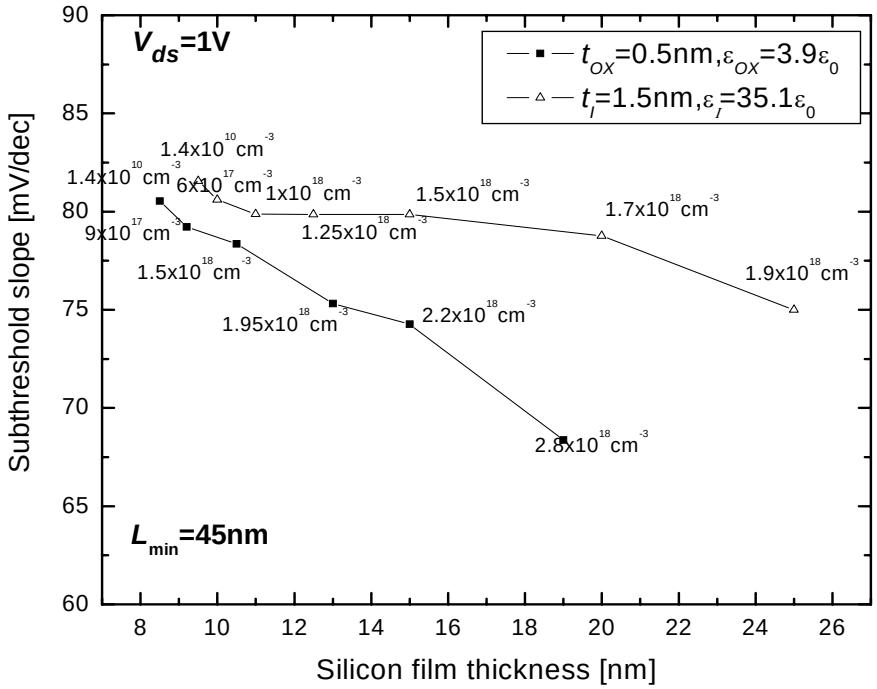


Fig. 4.4 Subthreshold slopes for the corresponding data points of the $L_{\min}$ contours with t_{OX} = 0.5 nm and t_I = 1.5 nm in Fig. 4.3.

can minimize the threshold-voltage fluctuation due to variations of the silicon layer thickness. For instance, an average -0.5-nm thickness variation in a 3-nm silicon body

of a long-channel, doped FDSOI device with t_{OX}=1.5 nm and $N_a = 1.2 \times 10^{19} cm^{-3}$ gives rise to a 42-mV threshold increase (ΔV_t^{QM}) [4.5] because of quantum mechanical effect. The 42-mV threshold increase can be offset by $\Delta V_t = \frac{qN_a \Delta t_{Si}}{C_{OX}} \approx 42$ mV due to the decreased depletion charges. Short-channel FDSOI MOSFETs may require a higher body doping to offset the ΔV_t^{QM} because the charge-sharing effect occurs at the source and the drain. Although body doping is beneficial to the short-channel effect in a FDSOI MOSFET, it has deleterious effects which can not be overlooked. Body doping needs to be high enough to have an appreciable effect on the suppression of short-channel effects. High body doping can lead to band-to-band tunneling from the body to the drain, which causes a significant increase of the leakage current in the device. Dopant fluctuation effect can take place and result in threshold-voltage variations. Carrier mobility is degraded by the impurity scattering and the high effective field introduced by the high body doping concentration [4.6]. Overall, benefits of body doping are likely to be offset by the aforesaid deleterious effects.

4.2 Effect of buried-insulator bandgap and permittivity

4.2.1 Effect of bandgap

The effect of buried-insulator bandgap and dielectric constant on short-channel effects in FDSOI MOSFETs is investigated. In principle, the electrostatics of

short-channel FDSOI MOSFETs are governed by the Poisson's equation and mobile charges inside the channel are negligible under subthreshold condition. The short-channel behavior of FDSOI devices is presumably independent of the bandgap of the buried-insulator. To confirm our hypothesis, the bandgap and the electron affinity of the buried-insulator with a silicon permittivity are adjusted and illustrated in Fig. 4.5. The difference between the conduction-band of the buried-insulator and the silicon intrinsic level, ΔE_{c2-i}, is set to be the same as the difference between the silicon

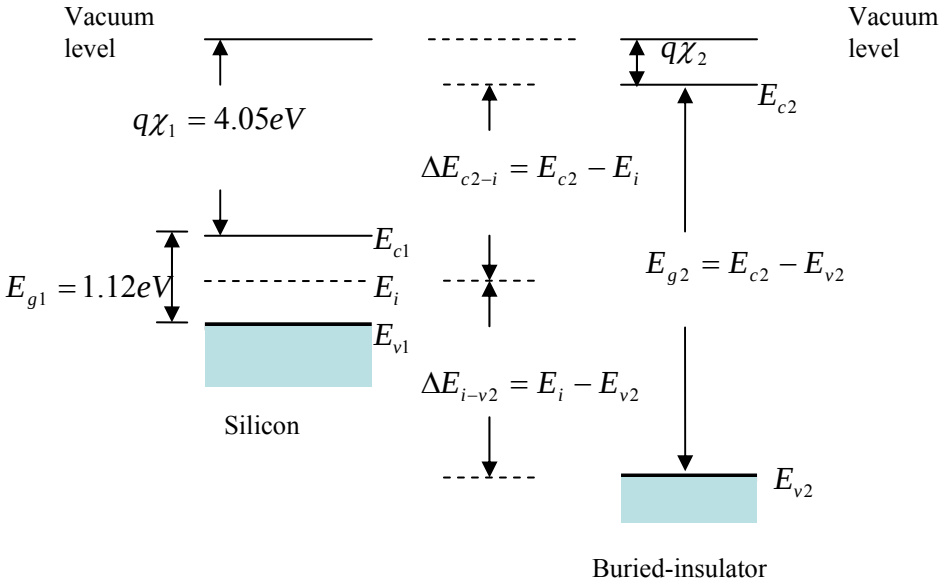


Fig. 4.5 Buried-insulator bandgap adjustment illustrated by energy-band diagram of the silicon and buried-insulator. The conduction-band difference and valence-band difference between the buried-insulator and silicon are adjusted symmetrically ($\Delta E_{c2-i} = \Delta E_{i-v2}$).

intrinsic level and the valence-band of the buried-insulator, ΔE_{i-v2}. For example, the $q\chi_2$ is set to be 3.55eV for E_{g2}=2.12eV and to make ΔE_{c2-i} and ΔE_{i-v2} equal. Fig. 4.6 shows the high-drain threshold roll-off in FDSOI devices with three different buried-insulator bandgap values. The high-drain threshold roll-off curves of FDSOI

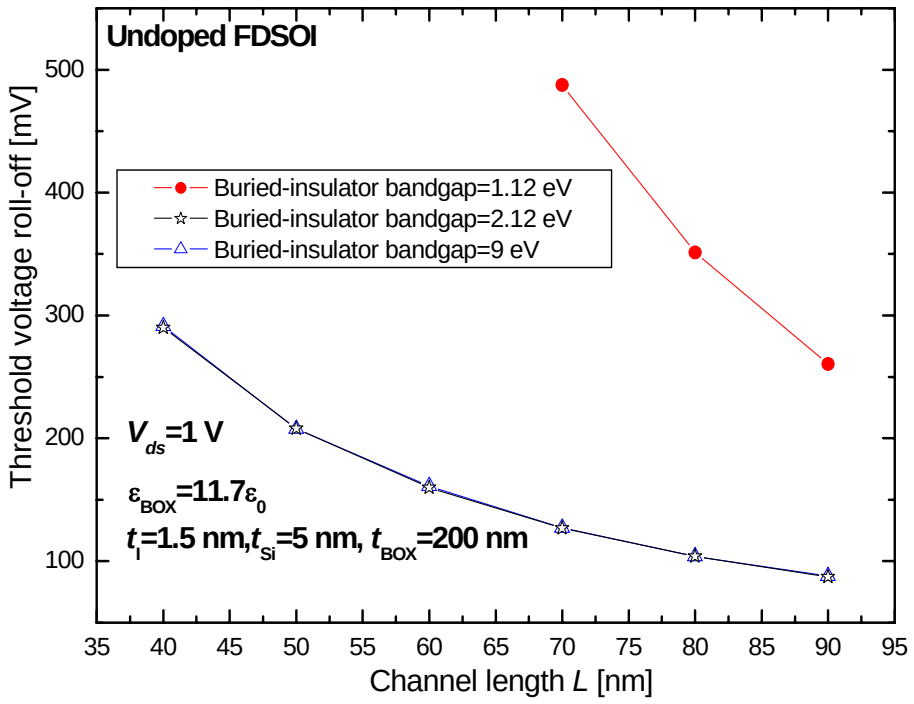


Fig. 4.6 Threshold voltage roll-offs for different FDSOI devices with different buried-insulator bandgap values.

devices with a buried-insulator bandgap of 2.12eV or larger do not show much difference. However, the short-channel effect in the FDSOI device with a 1.12-eV buried-insulator bandgap is severe. Our observation implies that the short-channel effect is aggravated by some other factor. The I_{ds}-V_{gs} curves, energy band diagrams at the channel surface, and current densities of the FDSOI devices with 1.12-eV and 2.12-eV buried-insulator bandgap are plotted in Fig. 4.7. The two devices are biased at the same off-current level of $10^{-8} A$ when the energy band diagrams and current densities are simulated. The FDSOI device with a 1.12-eV buried-insulator bandgap shows larger leakage current in the subthreshold region (Fig. 4.7(a)) than the one with

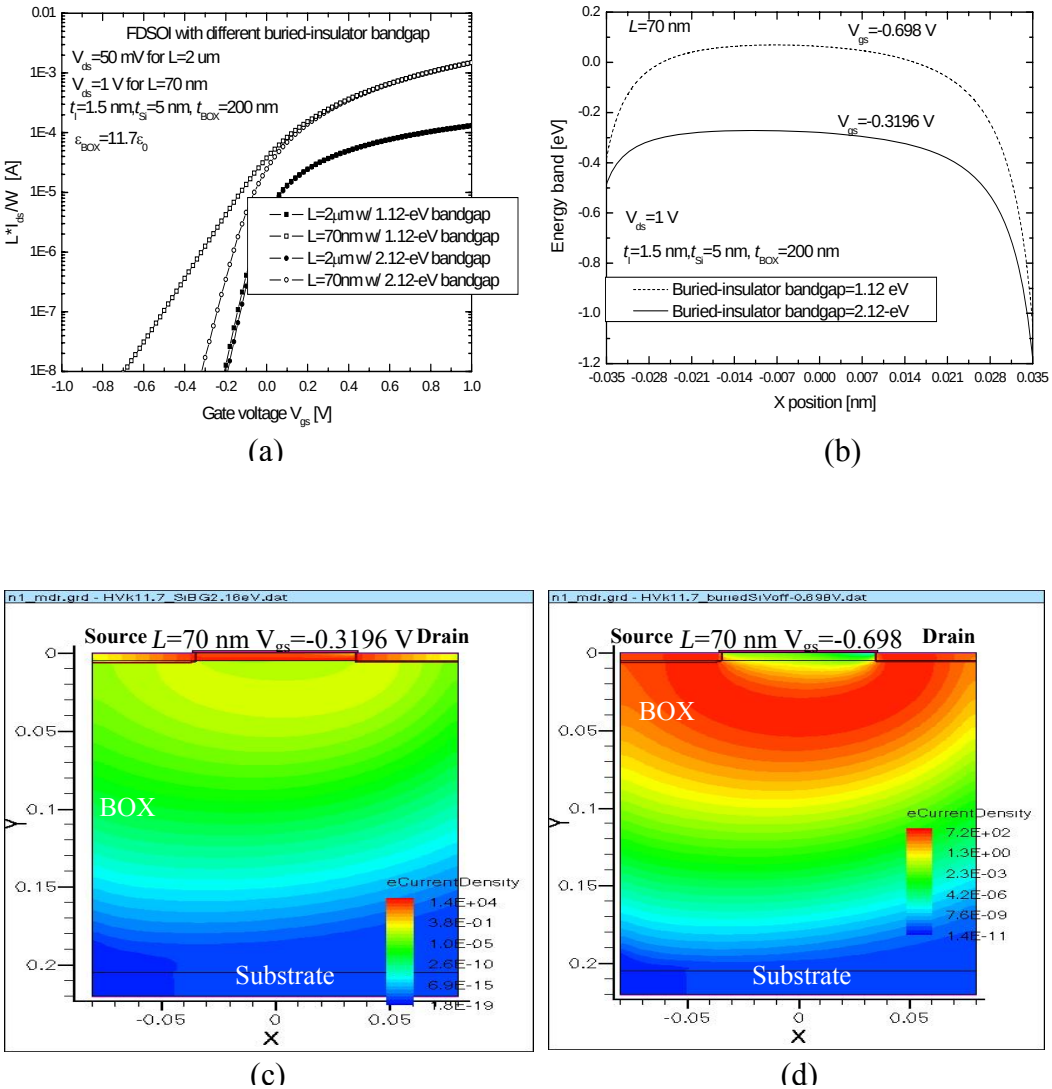


Fig. 4.7 (a) Threshold voltage roll-off comparisons between FDSOI devices with $\varepsilon_{BOX} = 11.7\varepsilon_0$ and the buried-insulator bandgap equal to 1.12eV and 2.12eV. (b) Potential barriers at device channel surface at V_{gs}=-0.3196 V and -0.698 V for buried-insulator bandgap equal to 1.12eV and 2.12eV, separately. (c) Electron current density of *L*=70 nm SOI device conducting in the buried-insulator with a silicon dielectric constant and bandgap=2.12eV at V_{gs}=-0.3196 V. (d) Electron current density of *L*=70 nm SOI device conducting in the buried-insulator with a silicon dielectric constant and bandgap=1.12eV at V_{gs}=-0.698 V.

a 2.12-eV buried-insulator bandgap, even though the former device has a higher potential barrier at the channel surface than the later device (Fig. 4.7(b)). There exists additional leakage current conducting beneath the silicon body (Fig. 4.7 (d)) in the FDSOI device with a 1.12-eV buried-insulator bandgap which has severe short-channel effect. A buried-insulator with a bandgap larger than 2.12 eV can significantly reduce the additional leakage current conducting beneath the silicon body and improve the short-channel effect of FDSOI MOSFETs.

4.2.2 Effect of permittivity

Since the normal component of electrical displacement is continuous across the silicon/buried-oxide interface, a simple relation exists between the vertical field at the bottom of the silicon body, E_{Si}, and the vertical field in the buried-oxide, E_{BOX}, that is, $\varepsilon_{Si}E_{Si} = \varepsilon_{BOX}E_{BOX}$. The vertical field E_{BOX} can be enhanced in a low-k buried-insulator. The lateral field in the buried-insulator is not affected by the permittivity. Consequently, the short-channel effect is improved in a FDSOI device with a low-k buried-insulator. In contrast to a thick buried-insulator FDSOI device, a thin buried insulator FDSOI device (or a double-gate like device) still needs a high-k material to reduce the effective oxide thickness of the bottom gate dielectric, and to improve the short-channel effect. To understand the effect of the buried-insulator dielectric constant on the scaling of FDSOI devices, constant $L_{\min}$=60 nm contours for FDSOI devices with different buried-insulator permittivities are plotted in a $t_I - t_{Si}$ plane in Fig. 4.8(a). By extrapolating the constant contours in the lower-right region of

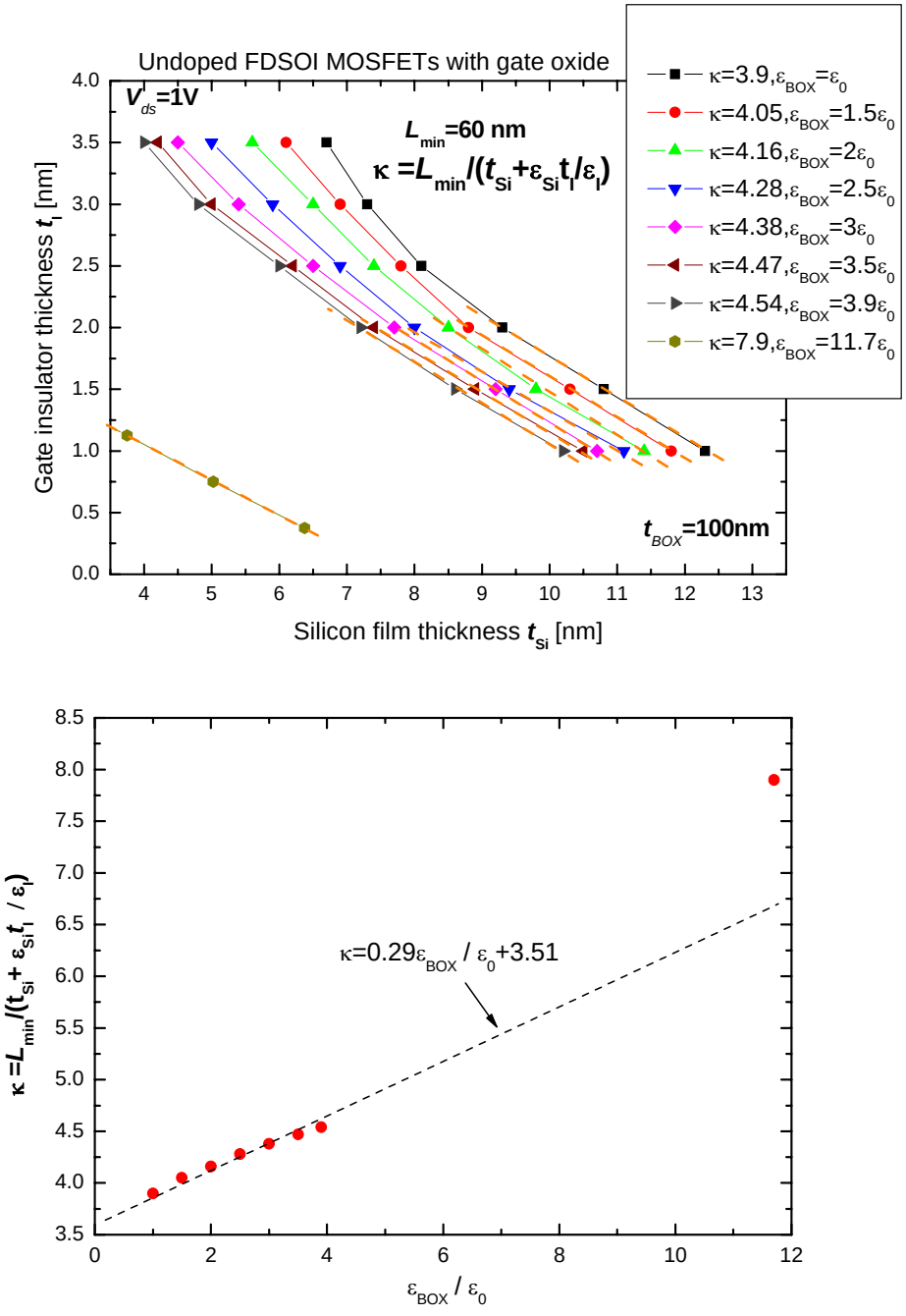


Fig. 4.8 (a) Constant $L_{\min} = 60\,\text{nm}$ contours for FDSOI devices with different permittivities. (b) The linear relation between κ and $\frac{\varepsilon_{BOX}}{\varepsilon_0}$.

Fig. 4.8(a), one can write the $L_{\min}$ equation of a FDSOI device with a specific ε_{BOX} in the form of $\kappa(t_{Si} + \frac{\varepsilon_{Si}}{\varepsilon_I} t_I)$. A smaller κ means a better short-channel effect in the device and a shorter $L_{\min}$ can be achieved with a given (t_I, t_{Si}).. A linear relation between the factor $\kappa = L_{\min} / (t_{Si} + \frac{\varepsilon_{Si}}{\varepsilon_I} t_I)$ and ε_{BOX} is approximately expressed by (Fig. 4.8(b)):

$$\kappa = 0.29 \frac{\varepsilon_{BOX}}{\varepsilon_0} + 3.51. \tag{4.5}$$

Equation (4.5) is valid for $\frac{\varepsilon_{BOX}}{\varepsilon_0} = 1 \sim 3.9$. It is inapplicable to a high-k buried insulator because of a more severe 2-D effect and the rapid increase of κ. The $L_{\min}$ of a FDSOI device with a buried-oxide can be reduced by 15% based on our empirical data if the BOX is replaced by a buried-insulator with $\varepsilon_{BOX} = \varepsilon_0$

4.3 Effect of reverse substrate biasing

In a VLSI system, the threshold voltage of a MOSFET without a grounded substrate varies with the applied substrate bias voltage. To avoid too much threshold voltage variation, it is important to design the device to be less sensitive to the substrate biasing. In long-channel bulk nMOSFETs, applying $-V_{bs}$ ($V_{bs}>0$) to the substrate is equivalent to raising all other voltages (namely, gate, source, and drain voltages) by $+V_{bs}$ while keeping the substrate grounded. The effect of reverse

substrate bias is to widen the bulk depletion region, increase depletion charge, and threshold voltage. Fig. 4.9 plots the threshold voltage V_t of long-channel bulk devices as function of $|-V_{bs}|$. The slope of the curve,

$$\frac{dV_t}{dV_{bs}} = \frac{\sqrt{\varepsilon_{Si} q N_a}}{C_{OX}\sqrt{2(2\frac{kT}{q}\ln\frac{N_a}{n_i} + V_{bs})}} \tag{4.6}$$

,is referred to as the substrate sensitivity. The slope equals to the ratio between the

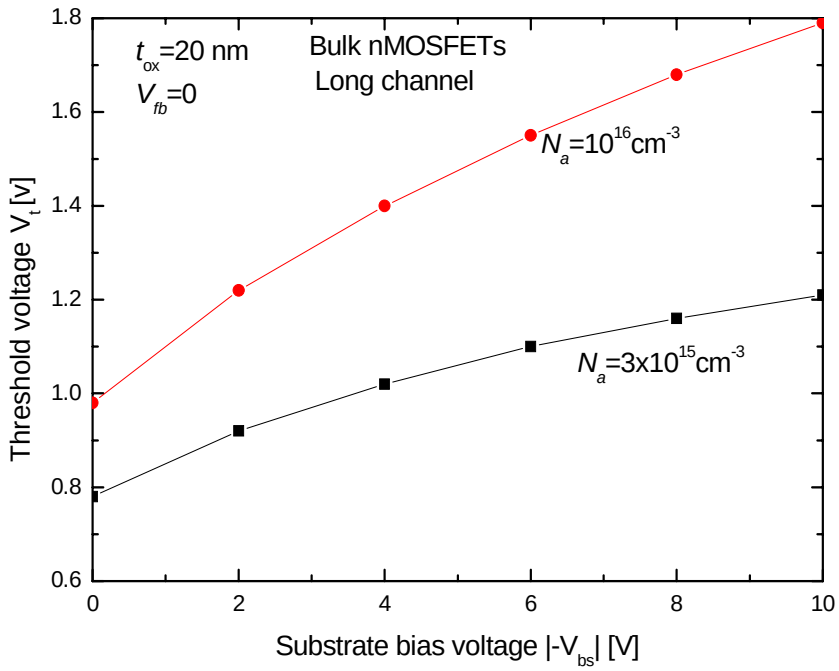


Fig. 4.9 Threshold-voltage variation with reverse substrate bias for two uniform substrate doping concentrations.

maximum depletion capacitance (per unit area) and gate capacitance (per unit area) C_{OX} at zero reverse bias voltage. The substrate sensitivity is higher for a higher

substrate doping concentration. The substrate sensitivity decreases as the $|-V_{bs}|$ increases in Fig. 4.9. For a short-channel bulk nMOSFET, the substrate sensitivity is slightly lower (better) than that of a long-channel device. This is because some of the substrate depletion charge terminates on the source and drain instead of on the gate in a short-channel device. The short-channel effect in a bulk MOSFET is aggravated by a high reverse bias voltage which leads to a wider depletion width.

Fig. 4.10 plots the threshold voltage V_t of long-channel FDSOI nMOSFETs as a function of $|-V_{bs}|$. The substrate sensitivity depends only on the physical thickness

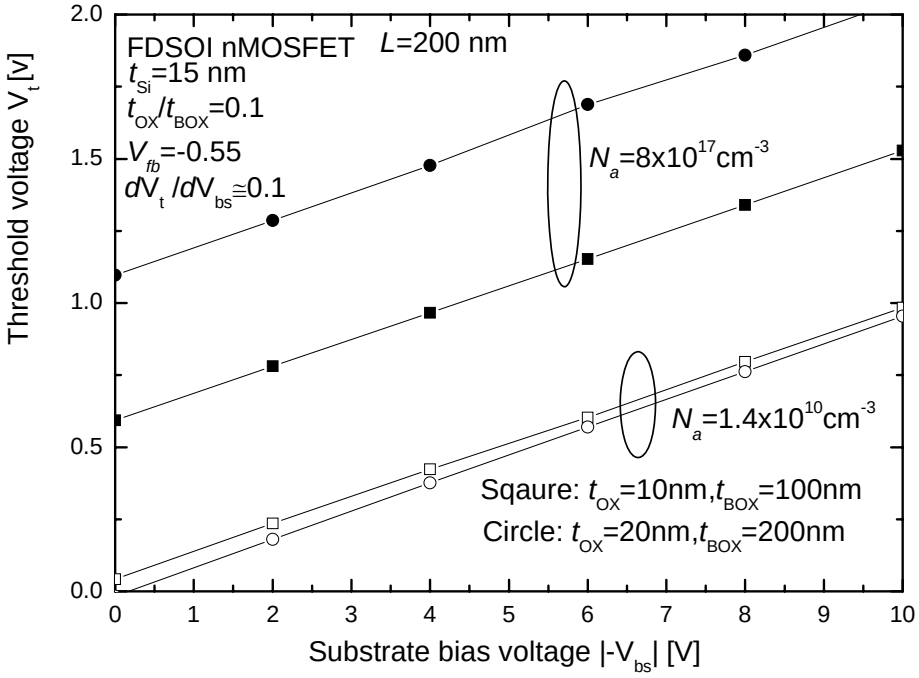


Fig. 4.10 Threshold-voltage as function of reverse substrate bias voltage in thick buried-oxide FDSOI devices with constant t_{OX}/t_{BOX} ratio equal to 0.1.

ratio between gate oxide and buried-oxide layers and is independent of body doping. The threshold voltage can become insensitive to a very high reverse substrate bias voltage because holes accumulate at the bottom of the silicon body and the high substrate field is gradually screened by holes. The substrate sensitivity of short-channel devices is studied by plotting the threshold voltage as a function of the channel length at different substrate biasing conditions in Fig. 4.11. The threshold voltage of long-channel devices is more sensitive to a reverse substrate bias voltage

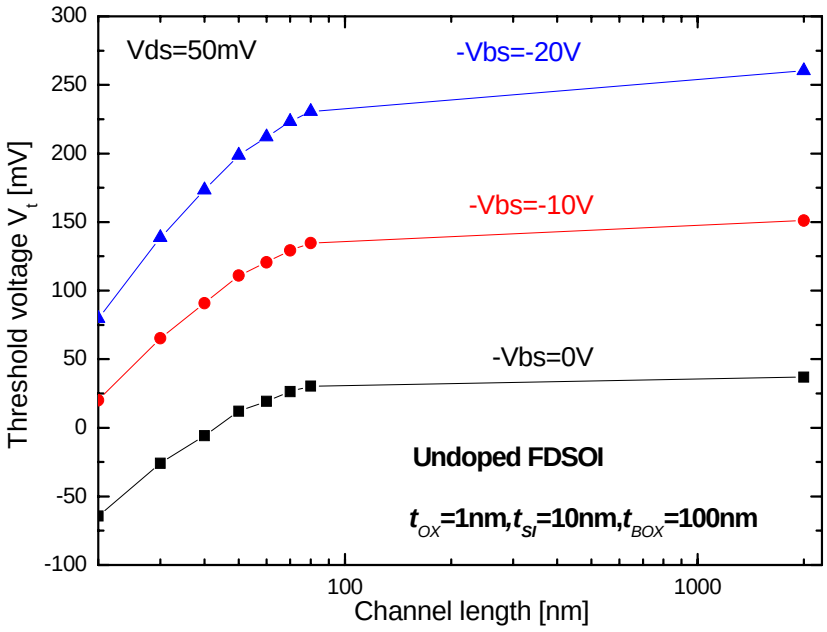


Fig. 4.11 The threshold voltage of undoped FDSOI devices as a function of the channel length at different substrate biasing conditions.

than that of short-channel devices. This is because the threshold voltage is affected by the charge-sharing effect at the source and the drain more than by the reverse substrate bias voltage in short-channel devices. Although the substrate sensitivity of

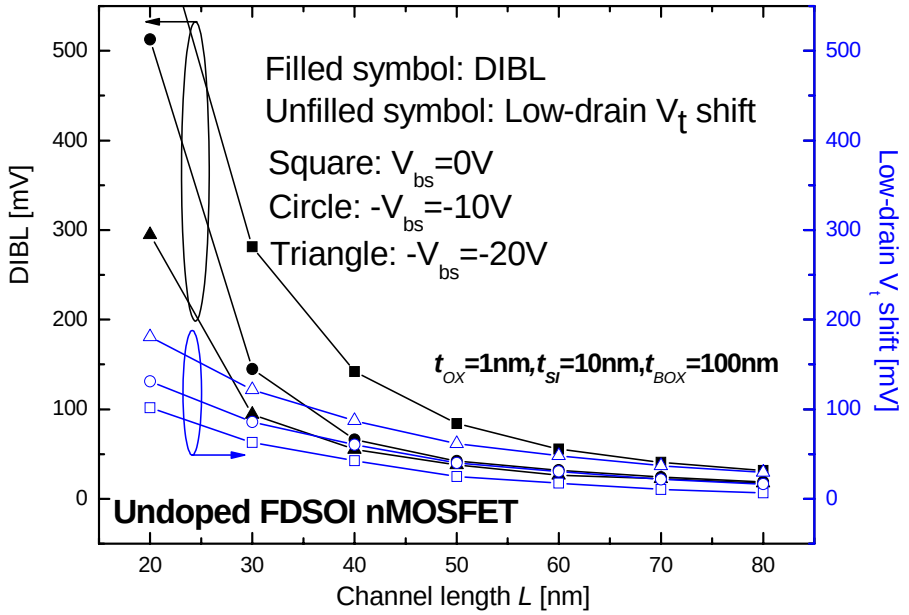


Fig. 4.12 The effect of the reverse substrate bias voltage on low-drain V_t shift and DIBL. Applying $-V_{bs}$ to short-channel devices acts on low-drain and high-drain short-channel behaviors in two different ways. The low-drain V_t shift becomes worse while the DIBL is improved.

short-channel devices is lower (better) than that of long-channel devices, applying $-V_{bs}$ to a short-channel device can worse the low-drain threshold-voltage shift. In contrast to the degradation of low-drain short-channel behaviors by $-V_{bs}$, DIBL of short-channel devices can be greatly improved by applying $-V_{bs}$ to the substrate (Fig. 4.12). This is because a high reverse substrate bias voltage forces a large amount of electric field in the BOX going in the vertical direction, i.e., more vertical field and less lateral field in the BOX (Fig. 4.13). Therefore, the short-channel effect is reduced due to less source/drain lateral field coupling into the channel. The high-drain threshold roll-off of FDSOI devices with and without reverse substrate biasing is investigated in Fig. 4.14. It is indicated in Fig. 4.14 that applying a small $|-V_{bs}|$ to the

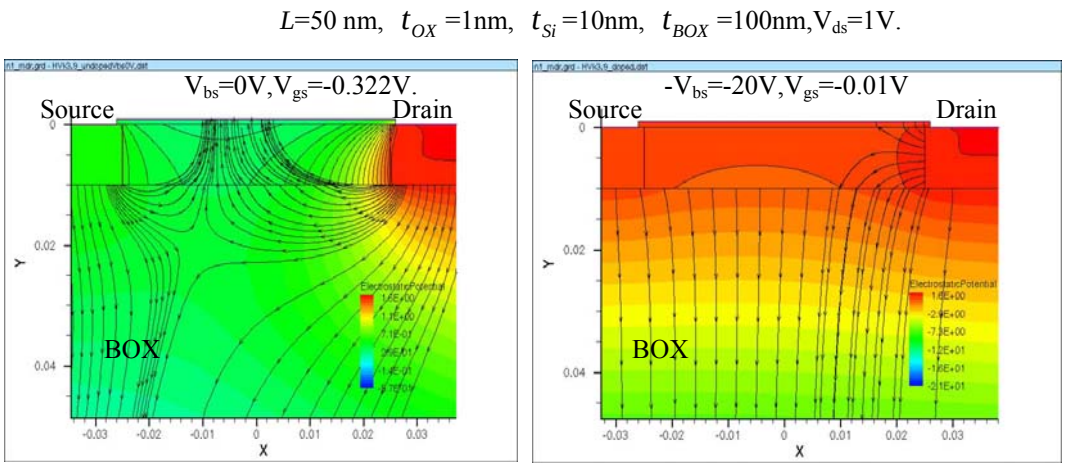


Fig. 4.13 Comparison of the electric field pattern in the BOX between L=50nm FDSOI devices with and without reverse substrate biasing. A high-drain voltage (V_{ds}=1V) is applied to both devices. The gate voltage is biased under the same off-current condition (normalized I_{ds} = 1e-8 A) in both devices. The source/drain lateral field coupling into the channel can be reduced by applying a high reverse substrate bias voltage to the device.

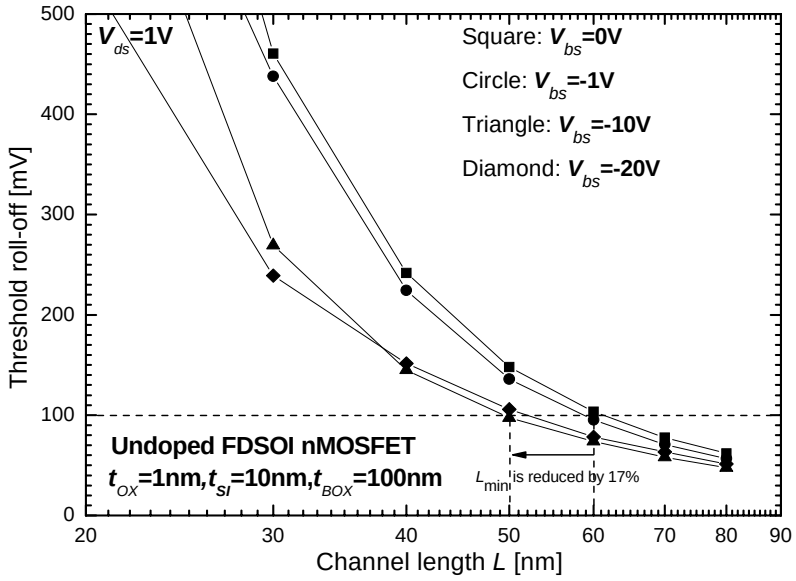


Fig. 4.14 High-drain threshold roll-offs for FDSOI nMOSFETs with the substrate reverse biased at different voltages. The L_{min} is reduced by 17% from V_{bs}=0 V to -V_{bs}=-10V. -V_{bs}=-20 V has insignificant effect on the short-channel effect.

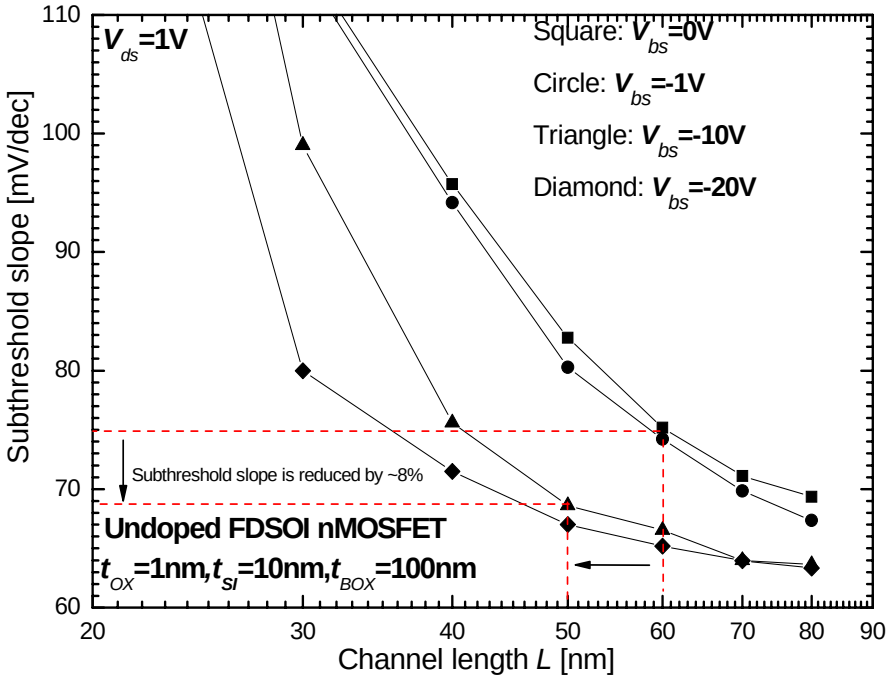


Fig. 4.15 Subthreshold slopes for FDSOI nMOSFETs with the substrate reverse biased at different voltages. The subthreshold slope of the FDSOI device with L_{min}=60nm is reduced by 8% from V_{bs}=0 V to -V_{bs}=-10V.

substrate has insignificant effect on the improvement of the L_{min} due to the thick BOX. The L_{min} can be reduced by 17% from -V_{bs}=0 to –V_{bs}=-10V for FDSOI devices. Adjusting the substrate bias voltage from -10 V to -20 V does not show significant improvement on the L_{min}. Fig. 4.15 shows the effect of the reverse substrate bias voltage on the subthreshold slope of FDSOI devices. The subthreshold slope of FDSOI devices is not affected by a small |-V_{bs}| due to the thick BOX. The subthreshold slope of the FDSOI device at L=L_{min}=60 nm can be reduced by 8% from -V_{bs}=0 to –V_{bs}=-10V. Even though the short-channel effect can be mitigated by

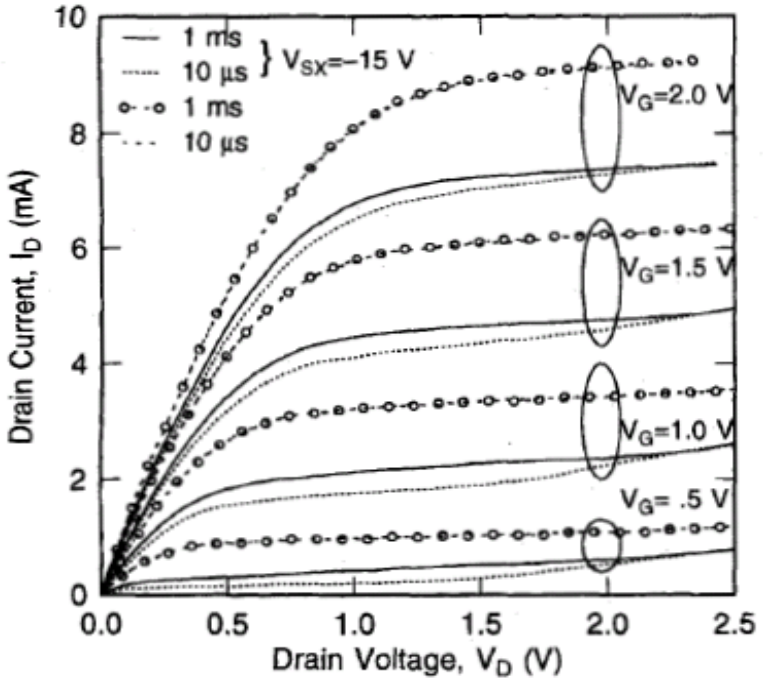


Fig. 4.16 Output curves of a fully depleted nFET operated with the normally grounded substrate (backgate), and with the substrate biased below the source voltage, at two pulse periods. The device has nominal silicon thickness of 70 nm, and a channel doping of $2x10^{17}$ /cm^3. Adapted from [4.7].

applying a reverse substrate biasing, there is a drawback which can not be overlooked. Applying a large reverse bias voltage to the substrate can cause a large amount of holes which accumulates at the bottom of the silicon body (for nMOSFET). The presence of holes makes the device behave as though partially depleted. This is confirmed in [4.7] and the I-V characteristic of FDSOI nMOSFETs with applied DC and pulsed gate voltages is shown in Fig. 4.16. With the substrate grounded, the normal condition, the FDSOI nMOSFET I-V characteristic is not influenced by the pulse period of input gate voltage. When the substrate of the FDSOI nMOSFET is reverse biased at a high voltage, the drain current shows the same history dependence as partially-depleted SOI nMOSFET (Fig. 4.16). Therefore, strong reverse biasing of

the substrate with respect to the source causes accumulation of holes in the body, has limited improvement on SCEs and leads to history effect in FDSOI devices. One should be careful to use a reverse substrate bias voltage appropriately to reduce the short-channel effect and avoid the history effect in a FDSOI device.

4.4 Effect of Si-BOX interface traps

At Si-gate-oxide and Si-BOX interfaces of a FDSOI MOSFET, the lattice of silicon and all the properties associated with its periodicity terminate. Therefore, localized states with energy in the forbidden energy gap of silicon are introduced at or near the Si-SiO_2 interface. The localized surface states are illustrated schematically in Fig. 4.17. Interface trapped charges are electrons or holes trapped in these states. As the interface traps are filled and emptied in response to changes in the surface potential, they give rise to an interface-trap capacitance. For example, the Si-gate-oxide and Si-BOX interface-trap capacitances (per unit area) are defined by

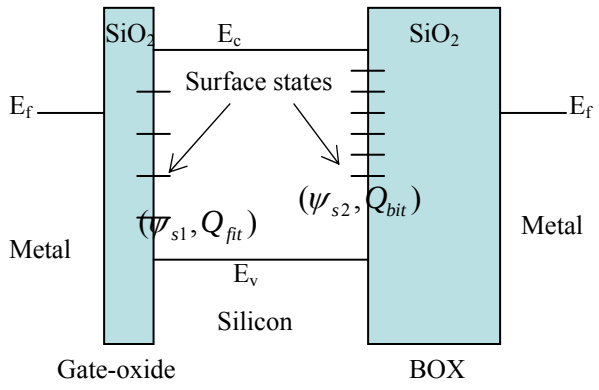


Fig. 4.17 Schematic energy-band diagram of an SOI MOS structure, illustrating the presence of surface states.

$C_{fit}(\psi_{s1}) = \dfrac{dQ_{fit}(\psi_{s1})}{d\psi_{s1}}$ and $C_{bit}(\psi_{s2}) = \dfrac{dQ_{bit}(\psi_{s2})}{d\psi_{s2}}$, separately. Q_{fit} is the trapped charges per unit area at the Si-gate-oxide interface and Q_{bit} is the trapped charges per unit area at the Si-BOX interface. ψ_{s1} and ψ_{s2} are the surface potential at the Si-gate-oxide interface and the Si-BOX interface. An equivalent circuit of a lightly-doped FDSOI MOS capacitor (Fig. 4.18) has been developed in the 1980's [4.8] and the effect of interface trapped charges on the subthreshold slope $S = \dfrac{mkT}{q}$ of long-channel FDSOI MOSFETs can be qualitatively analyzed. The body factor m then can be formulated as follows:

$$m = \frac{dV_g}{d\psi_{s1}} = \frac{\dfrac{1}{C_{OX}} + \dfrac{1}{C_{fit} + \dfrac{1}{\dfrac{1}{C_d} + \dfrac{1}{C_{bit} + C_{BOX}}}}}{\dfrac{1}{C_{fit} + \dfrac{1}{\dfrac{1}{C_d} + \dfrac{1}{C_{bit} + C_{BOX}}}}}. \tag{4.7}$$

When C_{fit} and C_{bit} both are zero, equation (4.7) becomes:

$$m \cong 1 + \frac{\dfrac{1}{C_{OX}}}{\dfrac{1}{C_d} + \dfrac{1}{C_{BOX}}}. \tag{4.8}$$

m in (4.8) is close to 1 and the ideal inverse subthreshold slope 60 mV/dec m can be observed since C_{BOX} ($\sim 3.45 \times 10^{-8} F/cm^2$ for t_{BOX} =100 nm) is much smaller than

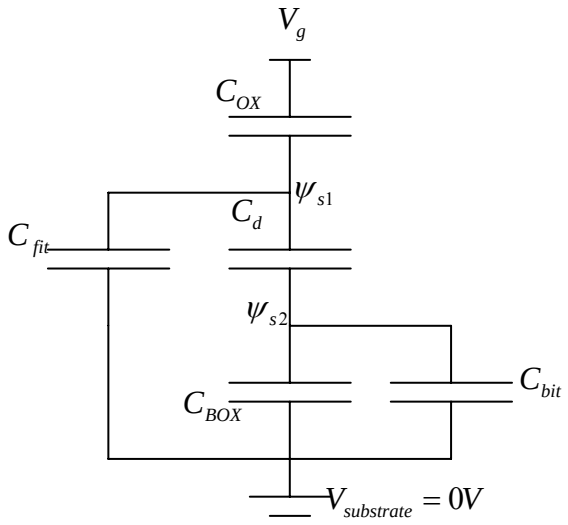


Fig. 4.18 Equivalent circuit of the FDSOI MOS capacitor. Adapted from [4.8].

C_d ($\sim 2.08\times10^{-6} F/cm^2$ for t_{Si}=5 nm) and C_{OX} ($\sim 1.7\times10^{-6} F/cm^2$ for t_{OX}=2 nm) in a thick BOX FDSOI MOSFET and the second term in equation (4.8) is ~0. When an ultra-thin Si film is implemented, then $\frac{1}{C_d}$ term in (4.7) can be ignored. If the density of Si-BOX interface traps is much larger than that of Si-gate-oxide interface traps, equation (4.7) becomes:

$$m \cong 1 + \frac{C_{bit}}{C_{OX}}. \tag{4.9}$$

The body factor (or subthreshold slope) is not affected by the Si-BOX interface trapped charges if $C_{OX} >> C_{bit}$. The effect of Si-BOX interface trapped charges on subthreshold slope is insignificant in nowadays since the gate oxide thickness is aggressively scaled (~2-nm thin). Short-channel effects have more influences on the subthreshold slope than the interface trapped charges. The body factor of a PDSOI

MOSFET is not influenced by the trapped charges at the Si-BOX interface because those charges are screened by the neutral body.

From the process viewpoint, the density of interface traps is a strong function of the device fabrication process. For instance, a post metallization in a hydrogen-containing ambient, at temperatures around 400°C is quite effective in

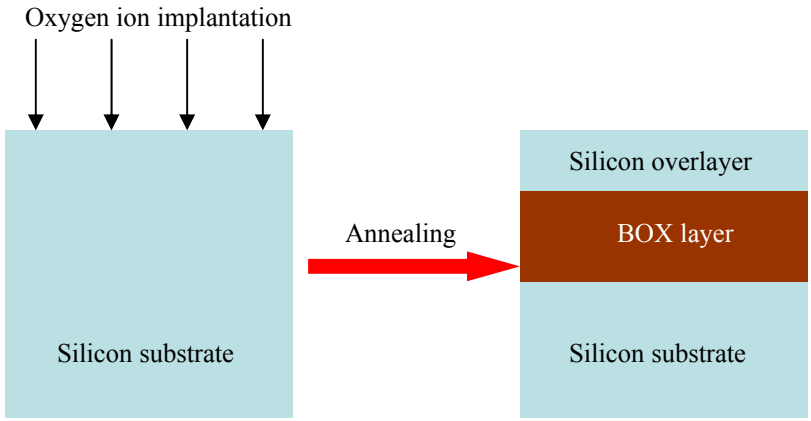
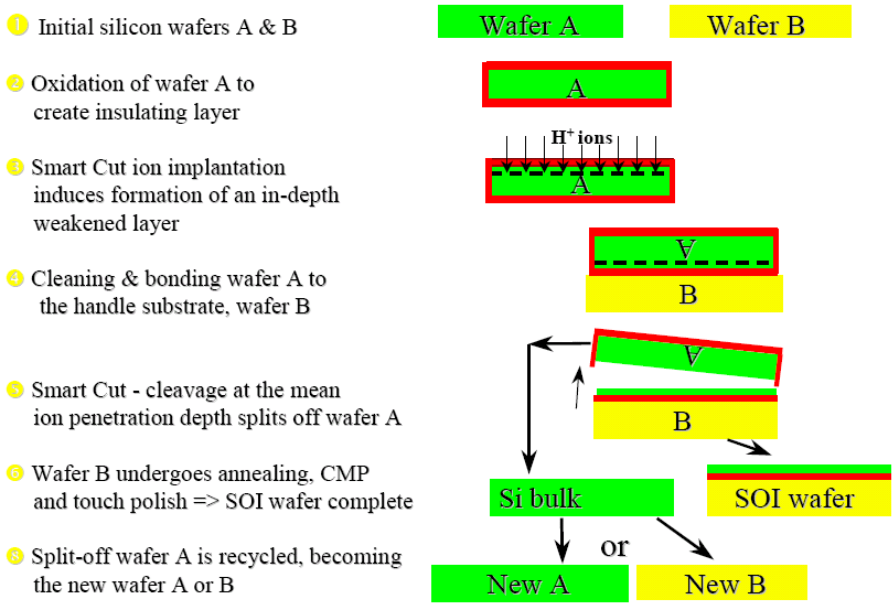


Fig. 4.19 Buried-oxide layer formation in SIMOX technology.

minimizing the density of Si-gate-oxide interface traps [4.9, 4.10]. At present, there are several promising technologies for the formation of silicon-on-insulator structures. They are SIMOX (Separation by Implanted Oxygen), UNIBOND®, and ELTRAN® (Epitaxial Layer Transfer). The SIMOX technique was innovated by K. Izumi, M. Doken and H. Ariyoshi in 1978 [4.11]. The principle of SIMOX technology is illustrated in Fig. 4.19. A high dose of oxygen ions is implanted in a silicon wafer followed by high-temperature annealing to form the buried-oxide layer. The uniformity of the buried-oxide layer is sensitive to the implanted oxygen dose, and implantation temperature. According to the reported literature, the quality of BOX and

(a)



(b)

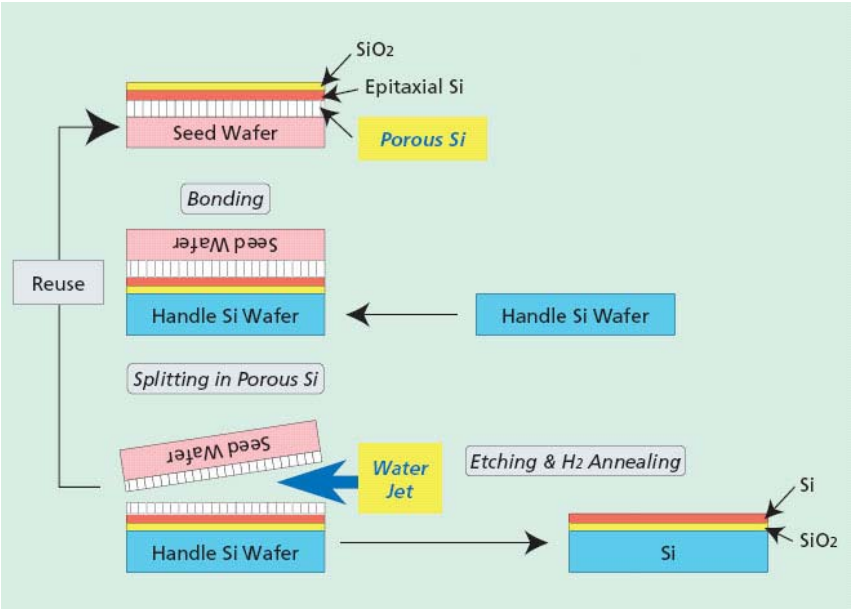


Fig. 4.20 Process flows of (a) Unibond® [4.16] and (b) Eltran® [4.17] technology.

silicon layers of SIMOX wafer is worse than that of UNIBOND®, and ELTRAN® wafers [4.12-4.15]. The process flow of UNIBOND® and ELTRAN® is illustrated in Fig. 4.20 [4.16, 4.17]. Both process technologies are based on seed wafer re-usage.

The buried-oxide layer is grown by thermal oxidation, which is similar to gate-oxide layer formation in conventional bulk CMOS technology. In other words, the Si-BOX interface quality is as good as the Si-gate-oxide interface quality of a bulk device. Moreover, when FDSOI MOSFETs enter sub-20-nm regime, the number of Si-BOX interface traps becomes smaller. For example, for a FDSOI MOSFET with a W/L of $1\mu m/20nm$ and with an average interface trap density of $10^{10} cm^{-3}$ [4.18-4.20] a total number of 2 traps is expected for the whole transistor area. The effect of Si-BOX interface traps on surface potential can be obvious due to trap charges fluctuation.

4.5 Summary

In this chapter, we investigated several factors which improve short-channel effects in FDSOI devices with a standard thick BOX. They are: body doping, the dielectric constant and the bandgap of the buried-insulator layer, and substrate biasing. The $L_{\min}$ can be reduced by ~15% from $\varepsilon_{BOX} = 3.9\varepsilon_0$ to $\varepsilon_{BOX} = \varepsilon_0$ but it is a technological challenge to manufacture an air gap underneath silicon body. A small reverse substrate bias voltage has insignificant effect on the short-channel scaling of FDSOI devices due to the thick BOX. One should be careful to use a reverse substrate bias voltage appropriately to reduce the short-channel effect and avoid the history effect in a FDSOI device. Body doping can improve the $L_{\min}$ from $\sim 5 t_{Si}$ to $\sim 2 t_{Si}$ when the silicon body is doped nearly partially-depleted, but it has deleterious effects such as carrier mobility degradation and dopant fluctuation effect which can not be overlooked. Quantum-mechanical effect and some other practical considerations will

impose limitations on FDSOI MOSFET scaling. The scaling limits of ultra-thin SOI MOSFETs will be discussed in next chapter.

The text of Chapter 4, in part, is the reprint of the material as it appears in "Effect of Body Doping on the Scaling of SOI MOSFETs" by Wei-Yuan Lu and Yuan Taur, Proceedings of SISPAD, Sep. 2006. The dissertation author was the primary researcher of this paper

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CHAPTER 5

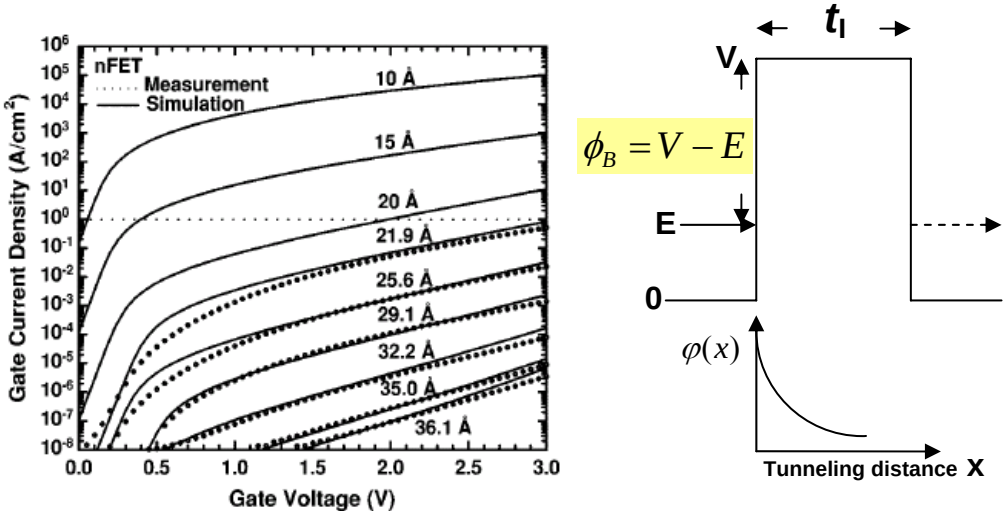
The Scaling Limit of Fully-Depleted SOI MOSFETs

In the previous two chapters, the design space of undoped and doped FDSOI MOSFETs has been explored in view of classical physics. Two simple L_{min} prediction equations have been empirically developed. However, there are physical effects and other practical considerations limiting the design space of the silicon-film and gate-insulator thickness in extremely-scaled FDSOI MOSFETs. For example, quantum-mechanical gate tunneling leakage becomes appreciable as the gate-insulator thickness is aggressively scaled. Quantum confinement of electrons (for nMOSFET) in the ultra-thin silicon body sandwiched between the top gate-insulator and the bottom buried-insulator layers leads to a threshold-voltage shift. Carrier-mobility becomes sensitive to the surface roughness due to process-induced t_{Si} variation in current fabrication technologies. How thin can the gate-insulator and silicon-film thickness be scaled? How short can FDSOI go? Factors affecting the exponential decay of the carrier wavefunction inside a gate insulator are discussed. The tunneling limit of a high-k dielectric is defined based on the barrier height relative to that of SiO_2. Quantum-mechanical effects on the short-channel behavior of FDSOI MOSFETs are studied by numerically solving coupled 1-D Schrödinger's and 2-D Poisson's

equations self-consistently in DESSIS. The effect of the silicon-film thickness on carrier-mobility is considered based on experimental data. The scaling limit of FDSOI MOSFETs will be derived from both the electrostatic and the performance perspectives in this chapter.

5.1 Scaling limit of gate-insulator thickness

If the gate oxide of a n-channel MOS device is very thin, say 4 nm or less, electrons from the inverted silicon surface can tunnel directly through the forbidden energy gap of the SiO_2 layer. Fig. 5.1(a) plots the measured and simulated thin-oxide



(a) (b)

Fig. 5.1 (a) Measured and simulated I_g-V_g characteristics under inversion conditions of n-FETs with oxides. Adopted from [5.1]. (b) Schematic diagram of direct-tunneling effect.

tunneling current versus voltage in polysilicon-gate nMOSFETs [5.1]. The current is

mainly a direct-tunneling current for the gate-voltage range shown in Fig. 5.1(a). Direct-tunneling current becomes appreciable when the gate-oxide thickness is scaled below 2 nm. According to the ITRS road map for the high-performance logic technology [5.2], the maximum allowable gate leakage current density for 45-nm technology node is ~1.22x10^3 A/cm^2 with a power supply voltage V_{dd} =1 Volt. Therefore, the scaling limit of the gate-oxide thickness for high-performance logic

Table 5.1 Dielectrics permittivities and barriers. Adopted from [5.3].

Dielectric	K	Φ_B [V]
SiO_2	~4	3.1
Si_3N_4	~8	2.1
Al_2O_3	8-12	~2.8
Ta_2O_5	16-26	>0.3 (2)
ZrO_2	12-20	~1.3
HfO_2	18-40	~1.4
TiO_2	40-80	>0.3
BST	200-300	-

applications is ~1-1.5 nm. To qualitatively estimate the tunneling limit thickness of different gate dielectrics, factors affecting the possibilities for electrons (for nMOSFET) passing through the gate insulator are investigated by solving the electron wavefunction $\varphi(x)$ from 1-D Schrodinger's equation. $\varphi(x = t_I)$ is proportional to

~exp(- t_I / t_0), where t_0 is the tunneling distance and equals to $\sqrt{\hbar/(2m^*\Phi_B)}$. $\Phi_B = (V - E)$ is the barrier height of the corresponding gate dielectric and illustrated in Fig. 5.1(b). A thicker gate-insulator thickness and a higher barrier height can help reduce the possibilities of electrons passing through the gate insulator. In our design study, the 1-nm minimum scalable gate-oxide thickness $t_{OX(min.)}$ is taken as a reference point to determine the tunneling limit thickness of high-k gate insulators. Table 5.1 [5.3] lists the barrier height of different gate dielectrics. Equation (5.1) is used to determine the tunneling limit thickness of high-k insulators with a tunneling current density comparable to $t_{OX(min.)}$=1 nm,

$$t_{high-k} \approx t_{OX(\min.)} \sqrt{\Phi_{B,oxide} / \Phi_{B,high-k}} \ . \qquad (5.1)$$

For example, the tunneling limit thickness of Si_3N_4 is ~1.2 nm and of HfO_2 is ~1.5 nm. High-k insulators usually have a larger tunneling limit thickness because of their lower barrier height than gate oxide. In our design study, we focus on the scaling limit of high-performance FDSOI devices. This is because for low power FDSOI devices, the gate insulator cannot be scaled down to the tunneling limit thickness in order to avoid large direct-tunneling gate leakage. Thus, the channel length of a low-power FDSOI device can not be scaled as short as that of a high-performance FDSOI device.

5.2 Scaling limit of silicon-film thickness

5.2.1 Quantum confinement of electrons

In conventional bulk nMOSFETs, electrons in the inversion layer are confined in a triangular potential well close to the channel surface. The triangular potential well is formed by the oxide barrier and the silicon conduction band which is severely bent toward the channel surface due to the applied gate field. The inversion-layer electrons must be treated quantum-mechanically as a 2-D gas [5.4] since the motion of electrons is confined in the direction normal to the channel surface. The energy level of electrons becomes discrete subbands and the ground-state energy of electrons is some energy above the bottom of conduction band at the channel surface. The centroid of electrons moves away from the channel surface. Therefore, the threshold voltage

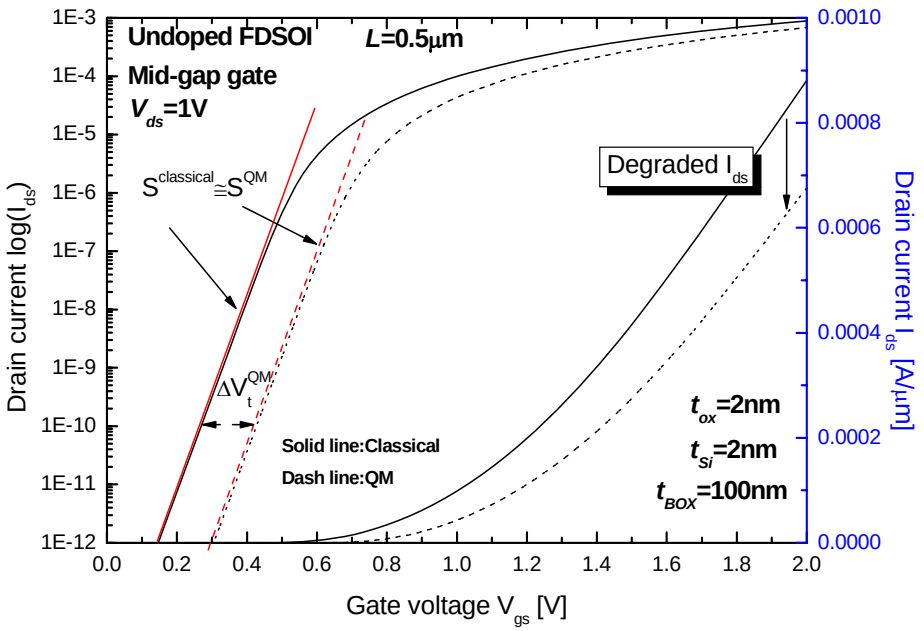


Fig. 5.2 I_{ds}-V_{gs} curves of a long-channel ultra-thin body FDSOI device obtained by classical and quantum simulations in ISE.

becomes higher and a higher gate-voltage overdrive is needed to produce a given level of inversion charge density. In other words, the effective gate-oxide thickness is thicker than the physical thickness. The transconductance and the current drive of the MOSFET are reduced as a result.

In ultra-thin body FDSOI nMOSFETs, electrons are confined in a square potential well formed by the barrier of the gate insulator and the barrier of the buried-oxide. According to the uncertainty principle, the momentum uncertainty of confined electrons increases with a thinner silicon film. Higher momentum uncertainty leads to higher electron ground-state energy, causing the threshold voltage to shift to a higher value. The quantum-mechanical electron density peaks away from the surface, in contrast to the classical electron density which peaks at the surface. The effective gate-insulator thickness becomes thicker than the physical thickness. Therefore, the drain current is reduced due to the degradation of inversion charge density. Fig. 5.2 shows the I_{ds}-V_{gs} curve of a FDSOI device obtained by numerically solving coupled 2-D Poisson's and 1-D Schrödinger's equations self-consistently in DESSIS. Constant carrier mobility is assumed. The I_{ds}-V_{gs} curve obtained by classical simulation is also plotted in Fig. 5.2. The threshold-voltage shift and drain current degradation due to quantum effect are obvious. The threshold-voltage shift can be modeled by considering the ground-state energy E_0 of electrons confined in a square well [5.5],

$$\Delta V_t^{QM} = \frac{E_0}{q} = \frac{h^2}{8qm^* t_{Si}^2} \tag{5.2}$$

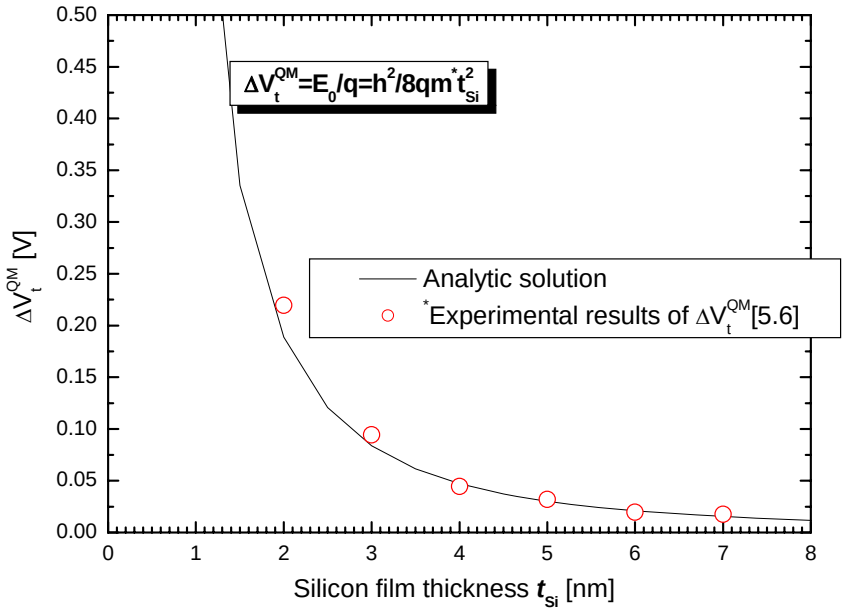


Fig. 5.3 Comparisons between the analytic solution and the experimental data [5.6] of V_t shift due to quantum confinement of electrons in a square potential well. The ΔV_t^{QM} is plotted as a function of the silicon-film thickness.

, where m^* is the electron effective mass. The analytical ΔV_t^{QM} of (5.2) fits the experimental results in Fig. 5.3 very well if m^* is set to half of the free electron mass. When t_{Si} is thicker than 5 nm, the threshold-voltage shift caused by quantum-mechanical effect is insignificant. The threshold voltage becomes very sensitive to the silicon-film thickness when t_{Si} is thinner than 3 nm. This means that process-induced variation of the silicon-film thickness can lead to a large variation of the threshold voltage. This will practically limit how thin the silicon-film thickness can be. For example, a 5% variation in a 2-nm-thick silicon-film thickness results in ~10% variation in threshold voltage. Therefore, to avoid large threshold-voltage

variation in ultra-thin body FDSOI devices, it is important to manufacture an atomically flat ultra-thin silicon layer. In our design study, the scaling limit of silicon-film thickness is set to ~2 nm to limit the quantum threshold-voltage shift ΔV_t^{QM} to <~0.2 V.

5.2.2 Quantum effect on the short-channel behavior of FDSOI MOSFETs

In the previous subsection, quantum-mechanical effects on the threshold-voltage shift and the degradation of the drain current in long-channel FDSOI devices have been investigated. However, several questions remain unanswered. For instance, it is indicated in Fig. 5.2 that the subthreshold slope of the long-channel FDSOI device is not affected by the quantum-mechanical effect. Does quantum effect have influence on the subthreshold slope of short-channel FDSOI devices? Does the charge (electrons for nMOSFET) redistribution in the depleted silicon region due to the quantum confinement of electrons affect the short-channel behavior and the design space of nanoscale FDSOI devices? To answer these questions, extensive device simulations are carried out. Quantum effect on the short-channel behavior of bulk MOSFETs is also investigated to compare with the simulation results of FDSOI devices. It is shown in Fig. 5.4(a) that the subthreshold slope of bulk MOSFETs is degraded by the quantum-mechanical effect. This can be simply explained by looking into the body factor *m* in the long-channel ($L = 1\mu m$) bulk device. The body factor is defined as $m = \frac{\Delta V_g}{\Delta \psi_s} = (1 + \frac{C_d}{C_{OX}})$ and is an indicator of how effectively the surface

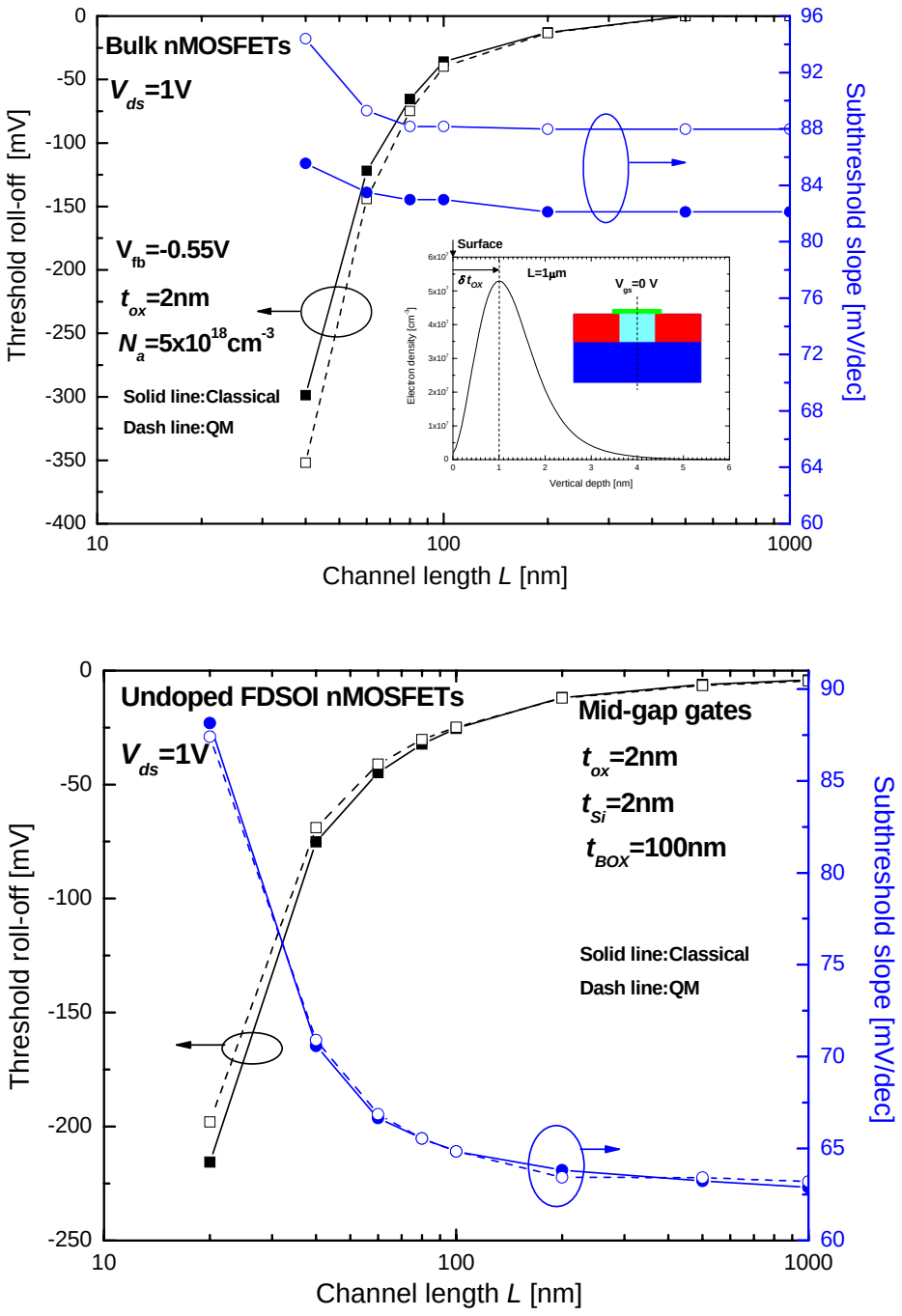


Fig. 5.4 The threshold roll-off and subthreshold slope of (a) bulk (b) FDSOI MOSFETs obtained by classical and quantum simulations. The inset shows the QM electron density distribution along a vertical cut of the L=1 μm bulk MOSFET at V_{gs}=0 V.

potential is modulated by the gate voltage. When the gate-oxide thickness of a bulk device is much less than the depletion width, *m* equals to 1, i.e., there is no body effect in the device. The classical solution of the inverse subthreshold slope of the long-channel bulk device is

$$S = (\frac{d(\log_{10} I_{ds})}{dV_g})^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}(1+\frac{C_d}{C_{OX}}) = 2.3\frac{kT}{q}(1+\frac{3t_{OX}}{W_d}). \qquad (5.3)$$

$S = 2.3\times 26mV\times(1+\frac{3\times 2}{16.286}) \approx 81.8mV/decde$ for the long-channel bulk device in Fig. 5.4(a), in good agreement with the classical simulation result. The inset in Fig. 5.4(a) illustrates the QM electron density distribution in the long-channel bulk device at V_{gs}=0 V (subthreshold region). The electron density distribution is plotted along a vertical cut in the center of the $L = 1\mu m$ bulk device in DESSIS. The electron density peaks at 1 nm away from the surface and leads to a thicker effective gate-oxide thickness $t_{OX,effective} = (t_{OX} + \delta t_{OX}) \approx (t_{OX} + \frac{\varepsilon_{OX}}{\varepsilon_{Si}}\times 1nm)$ and a thinner effective depletion width $W_{d,effective} \approx (W_d - 1nm)$. Therefore, the quantum solution of the subthreshold slope of the long-channel bulk device in Fig. 5.4(b) is $S^{QM} = 2.3\frac{kT}{q}(1+3\frac{t_{OX,effective}}{W_{d,effective}}) = 2.3\times 26mV\times(1+\frac{3\times(2+1/3)}{15.286}) \approx 87.4mV/decde$, which is also in good agreement with the simulation result. The subthreshold slope of bulk MOSFETs is degraded by the quantum-mechanical effect because of an increased body factor. In contrast, the subthreshold slope of FDSOI MOSFETs is not affected by

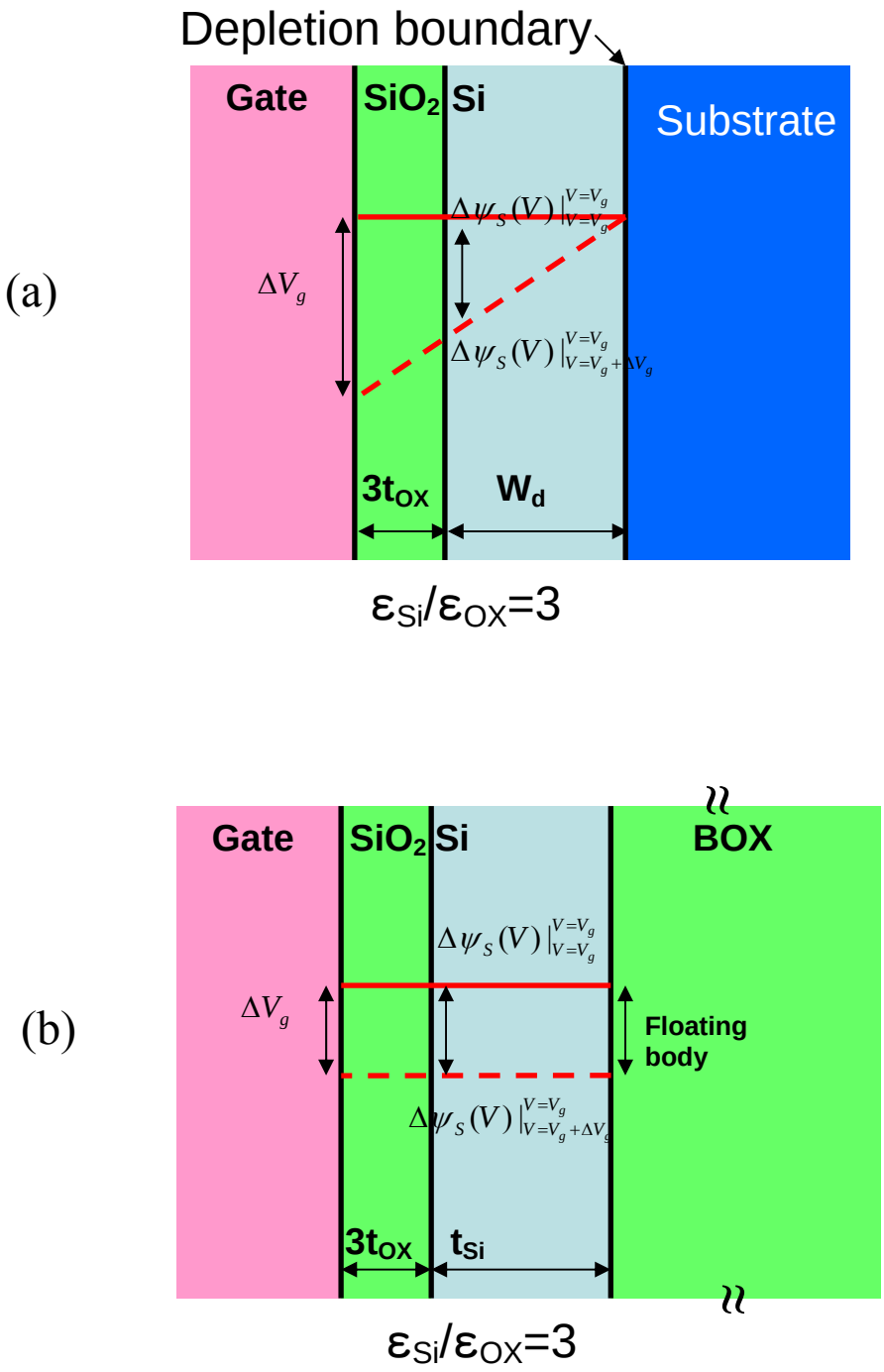


Fig. 5.5 Illustrations of body effects in (a) bulk and (b) ultra-thin body FDSOI MOSFETs.

the quantum-mechanical effect, as can be seen in Fig. 5.4(b). This is because the body factor of FDSOI MOSFETs is always one, as illustrated schematically in Fig. 5.5. For a bulk device, the surface potential can not completely follow the variation of the gate voltage due to a pinned body potential (Fig. 5.5(a)). Thus, the body factor is $\frac{\Delta V_g}{\Delta \psi_s} = (\frac{W_d + 3t_{OX}}{W_d})$, which is always larger than 1. For a FDSOI device, the surface potential follows 100% of the gate voltage variation due to a floating body potential (Fig. 5.5(b)). Therefore, the body factor is always one. This also explains why a long-channel undoped FDSOI device has a nearly ideal subthreshold slope of $60mV/decade$ in Fig. 5.4(b). Although the quantum-mechanical effect has different influences on the subthreshold slope of bulk and FSDOI devices, it has no significant impact on the high-drain threshold roll-off. As a result, the design spaces of FDSOI MOSFETs obtained by classical and quantum simulations are similar.

5.3 Scaling limit of ultra-thin FDSOI devices

The scaling limit of FDSOI MOSFETs depends on the limit of gate-insulator and silicon-film thickness. To avoid excessive threshold-voltage shift, e.g., $\Delta V_t^{QM} <$ 0.2V, the silicon-film thickness cannot be scaled below ~2 nm. On the other hand, quantum-mechanical gate-tunneling leakage limits the gate-insulator thickness to ~1 nm for oxide and ~2 nm for high-k insulators with typically lower barrier heights. Fig. 5.6 plots the design space of sub-20 nm undoped and doped-body FDSOI MOSFETs with gate oxide and high-k gate dielectrics. The blocked-out region in Fig. 5.6 is

forbidden due to excessive $\Delta V_t^{QM} > 0.2$V. The gate-tunneling limits for $\varepsilon_I / \varepsilon_0$ =3.9 and 35.1 are indicated by two dashed lines. The doping concentrations for doped body SOI devices are chosen such that the threshold voltage is ~0.3 V with ΔV_t^{QM} taken into account. Metal gates with gate work function between mid-gap and N+ poly-gate work

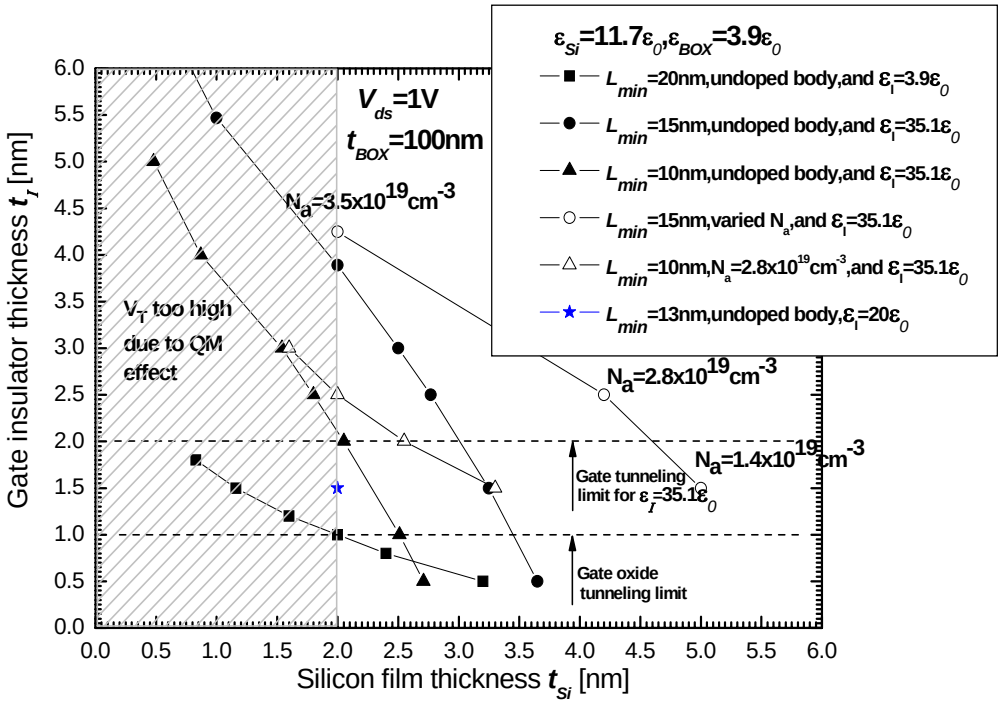


Fig. 5.6 Design space of sub-20 nm undoped and doped body ultra-thin FDSOI nMOSFETs with gate oxide and high-k gate insulators. The lower region is forbidden by the tunneling leakage limits of gate insulators. The left region is forbidden because of excessive high threshold voltage imposed by quantum confinement of electrons in the ultra-thin silicon film.

function are assumed to lower the threshold voltage of undoped and doped FDSOI devices. The scaling limit for undoped FDSOI MOSFETs with gate oxides is projected to be $L_{\min} \approx 20$ nm with both the gate-oxide and the silicon-film thickness scaled to

their limits of ~1 nm and ~2 nm, separately. For the high-k gate dielectric, $\varepsilon_I / \varepsilon_0$ =35.1, a 10-nm FDSOI MOSFET design is conceivable if both the silicon-film and gate-insulator thickness are scaled to their limits of ~2 nm. Compared to the L_{min} contours of undoped SOI (L_{min}=10 nm and 15 nm), body doping may allow the use of a thicker t_{Si} for the same L_{min}. However, body doping in general does not significantly help extend the scaling limit of FDSOI MOSFETs. Besides, carrier mobility is severely degraded by impurity scattering. For the feasible gate dielectrics today (HfO_2, HfSiON), the tunneling limit is ~1.5 nm since the corresponding barrier height is half of the oxide [5.3]. The scaling limit for FDSOI devices with $\varepsilon_I / \varepsilon_0$ =15~20 and t_{Si}= 2 nm is projected to be ~13 nm by DESSIS. To realize a 10-nm FDSOI device, atomically flat 2-nm silicon film need be manufactured to avoid carrier-mobility degradation and reduce device variability.

5.4 Mobility degradation in ultra-thin silicon film

Previously the scaling limit of ultra-thin body FDSOI MOSFETs has been investigated from the electrostatics point of view. However, the carrier mobility can be severely degraded due to surface roughness when the silicon-film thickness is thinned down toward its limit of ~2 nm. The buried-oxide interface roughness and quantum-mechanical effect may have influences on the carrier mobility. Factors affecting the carrier mobility are discussed based on the experimental data [5.6, 5.7, 5.9, and 5.10] in the following subsections. The scaling limits of the silicon-film

thickness and ultra-thin body FDSOI MOSFETs are reviewed from the performance perspective at the end of this section.

5.4.1 Influences of buried-oxide interface roughness on mobility

The effect of buried-oxide interface roughness on carrier mobility has been experimentally investigated in [5.7]. The SOI devices were fabricated by SIMOX process with a buried-oxide thickness of ~80 nm. The silicon body was left undoped to study the body thickness dependence of the intrinsic electron transport. The gate length and gate width of SOI devices being investigated were typically 200 μm and 100 μm. The interface state densities, D_{it}, of the front gate oxide and the backside BOX interfaces were measured separately [5.8]. The experimental results are summarized in Table 5.2. The backside BOX interface of SIMOX1 has much poorer

Table 5.2 Measured interface state density for bulk Si, SIMOX1, and SIMOX2 wafers. Adapted from [5.7].

D_{it} [$cm^{-2}eV^{-1}$]	Front	Backside
Bulk Si	$5x10^{10}$	----
SIMOX1	$5x10^{10}$	$6x10^{11}$
SIMOX2	$4x10^{10}$	$4x10^{10}$

quality that its interface state density is larger than that of SIMOX2 by more than an order of magnitude. Therefore, the effect of buried-oxide roughness on carrier

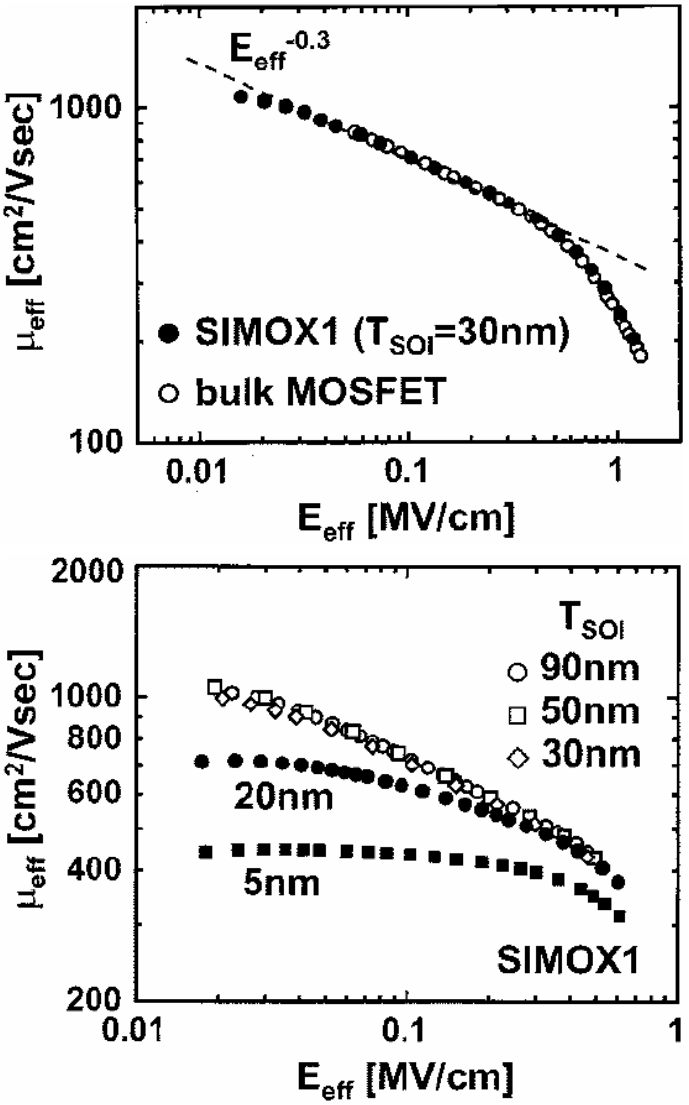


Fig. 5.7 (a) E_{eff} dependence of electron mobility in MOS inversion layer for SOI and bulk MOSFETs. (b) E_{eff} dependence of electron mobility for different silicon film thickness in SIMOX1 transistors having poor quality of buried-oxide interface. Adapted from [5.7].

mobility was investigated by comparing the carrier mobility of SOI devices fabricated on SIMOX1 and SIMOX2.

The electron mobility of SIMOX1 transistors with a 30-nm-thick silicon body was compared to the electron mobility of conventional bulk nMOSFETs. The channel

doping concentration of bulk nMOSFETs is $3x10^{15}$ cm^{-3}. It shows in Fig. 5.7(a) that the μ_{eff} behaviors for bulk and SOI devices agree very well with the universal curve in spite of the poor quality of the BOX interface in SIMOX1. This suggests that the phonon scattering and the front gate oxide surface roughness scattering are the dominant factors on the mobility behavior of SOI devices. The universal relationship is still valid in SOI devices with a 30-nm Si film thickness. The $E_{eff}^{-0.3}$ dependence of

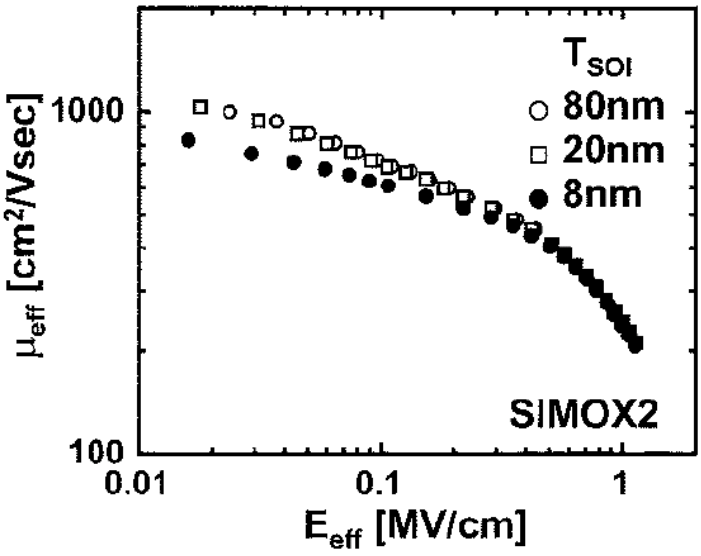


Fig. 5.7 (c) E_{eff} dependence of electron mobility for different silicon film thickness in SIMOX2 transistors having good quality of buried-oxide interface. Adapted from [5.7].

μ_{eff} [5.9] still holds at E_{eff} down to 0.01 MV/cm. Fig. 5.7(b) and (c) show the electron mobility μ_{eff} versus E_{eff} for the SOI devices fabricated on SIMOX1 and SIMOX2 wafers. The mobility degradation becomes significant with decreasing silicon-film thickness. The universal relationship breaks down for SIMOX1 with a silicon-film thickness thinner than 20 nm but it remains valid for SIMOX2 with a

20-nm silicon-film thickness. The results indicate that the interface quality at buried-oxide interface has great influence on the carrier mobility when the silicon-film thickness is thin. In the following section, we will discuss the quantum effect on carrier mobility when the silicon-film thickness is less than 5 nm.

5.4.2 Quantum mechanical effects on low-field carrier mobility

The design of sub-20nm ultra-thin body FDSOI MOSFETs requires a silicon-film thickness less than 5 nm. Quantum-mechanical effect becomes significant when the silicon-film thickness is scaled down to sub-5-nm where the ground-state

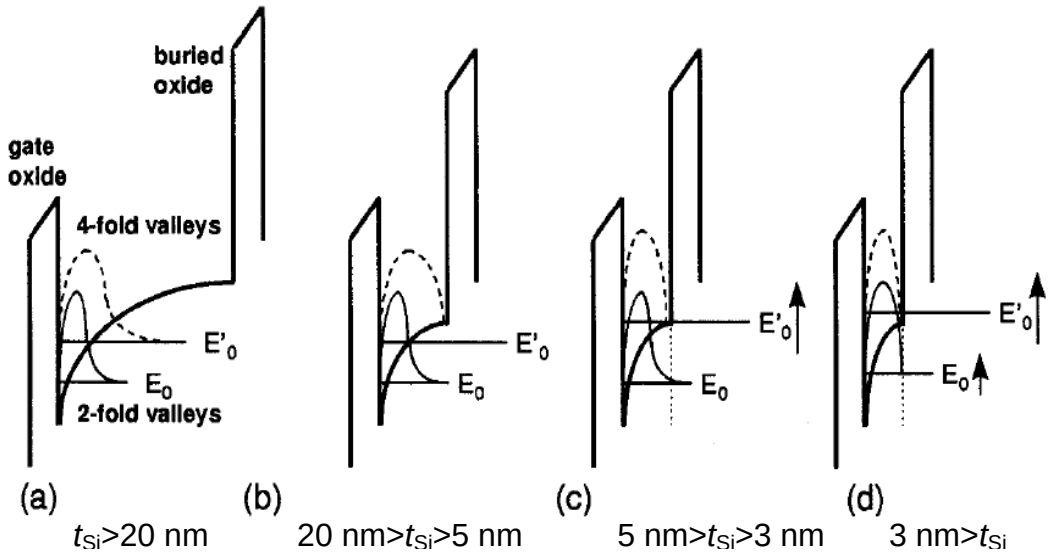


Fig. 5.8 Schematic diagrams of the band structure of SOI MOSFETs with different silicon film thickness. Adapted from [5.10].

electron energy is high. When the silicon-film thickness is reduced to ~3nm, quantum-mechanical effect lifts the degeneracy of the ground-state energy level such that electrons in the 4-fold valleys have a higher energy than those in the 2-fold

valleys [5.10]. This means more electrons populate the 2-fold valleys with a lower effective mass when t_{Si} is ~3 nm. Fig. 5.8 schematically shows the band structures of SOI devices with different silicon-film thickness [5.10]. The mobility enhancement with t_{Si} ~3 nm at E_{eff} of around 0.3MV/cm is experimentally observed in [5.6] and shown in Fig. 5.9. Although mobility enhancement is observed for electrons, no

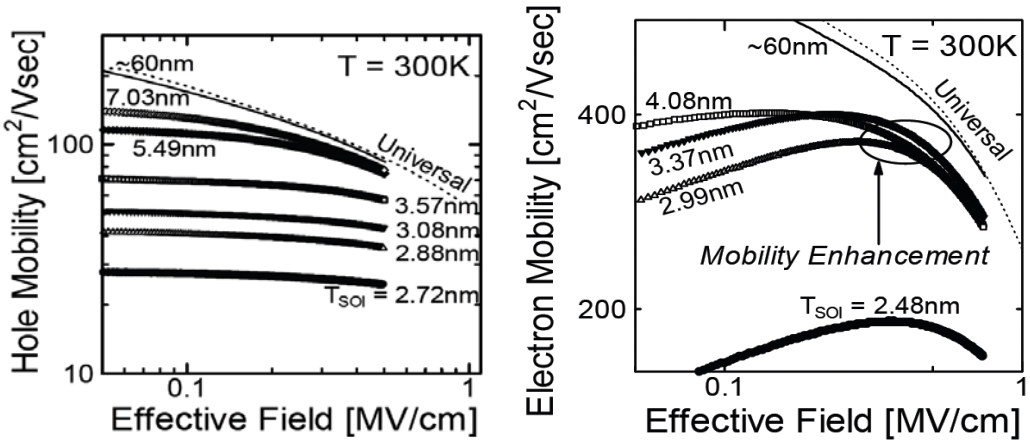


Fig. 5.9 (a) Hole mobility versus effective field for different Si film thickness (T_{SOI}) at 300 K. (b) Electron mobility versus effective field for different Si film thickness (T_{SOI}). The electron mobility enhancement is observed at E_{eff} ~0.3 MV/cm. Adapted from [5.6].

enhancement is observed for holes with decreasing silicon-film thickness. The mobility degradation for both electrons and holes becomes very severe when t_{Si} is scaled down toward ~2 nm. Therefore, the scaling limit of FDSOI MOSFETs needs to take the mobility-dependent device performance into consideration.

There are two key factors governing CMOS performance-current and capacitance. Higher on currents can be obtained by scaling down channel lengths. Shorter channel lengths also help reduce intrinsic capacitances. To assess the scaling limit of FDSOI MOSFETs from the performance point of view, we consider FDSOI devices with $L_{\min}$=10 nm and $L_{\min}$=17 nm. The 10-nm device has t_{Si}=2 nm and t_I=2 nm with $\varepsilon_I/\varepsilon_0$=35.1. The 17-nm device has t_{Si}=3 nm and t_I=1.5 nm with $\varepsilon_I/\varepsilon_0$=20 ($HfO_2$). Although the intrinsic capacitance of the 10-nm device is ~40% smaller than that of the 17-nm device, the drain current of the 10-nm device can be ~>70% smaller than that of the 17-nm device due to the severe mobility degradation (Fig. 5.9(b)) and the intrinsic capacitance degradation due to the quantum-mechanical effect. Consequently, from the performance point of view, the scaling limit of the silicon-film thickness is ~3 nm. The scaling limit of FDSOI MOSFETs with HfO_2 gate dielectric is ~17 nm. However, if there is a technology breakthrough on atomically thin t_{Si} with high mobility, then 10-nm FDSOI device is achievable with a 2-nm silicon-film thickness.

5.5 Summary

In this chapter, we explored the design space of sub-20 nm ultra-thin SOI MOSFETs by taking the gate tunneling limit and silicon-film scaling limit into account. From the electrostatics point of view, both the gate-insulator and silicon-film thickness must be thinned down to their limits ~2 nm to achieve acceptable SCE's in a

10-nm FDSOI device. High body doping allows the use of a thicker t_{Si}, but it does not significantly improve the scaling limit of ultra-thin body FDSOI MOSFETs. High doping also degrades carrier mobility. On the other hand, carrier mobility is severely degraded when the silicon-film thickness is reduced to 2 nm due to surface roughness scattering. From the performance point of view, then silicon-film thickness should not be scaled below 3 nm. The scaling limit of FDSOI MOSFETs is ~17 nm with a 1.5-nm HfO_2 gate dielectric and a 3-nm silicon-film thickness. This conclusion is based on the assumption that one cannot improve upon mobility beyond what was reported. If there is a breakthrough on thin t_{Si} mobility, then 10-nm FDSOI device is achievable with a 2-nm silicon-film thickness.

The text of Chapter 5, in part, is the reprint of the material as it appears in "Scaling to 10nm-Bulk, SOI or DG MOSFETs?" by Minjian Liu, Wei-Yuan Lu, Wei Wang and Yuan Taur, Proceedings of ICSICT, Oct. 2006. The dissertation author was the co-author of this paper.

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CHAPTER 6

Conclusion

In this dissertation, a detailed study on the scaling limit of ultra-thin silicon-on-insulator MOSFETs is presented. Extensive two-dimensional simulations are carried out by using the 2-D TCAD tool from SYNOPSYS, including finite boundary editor MDRAW, and device simulator DESSIS.

By reviewing the scaling trend and the fundamental factors limiting bulk CMOS scaling, the inherent advantages of SOI CMOS technology over bulk CMOS technology are discussed. The analytical models for 2-layer- and 3-layer-dielectric MOSFETs are reviewed to understand how the minimum scalable channel length $L_{\min}$ can be predicted from the effective height of the dielectric layers (or the scale length λ_1). The $L_{\min}$ for a fully-depleted SOI MOSFET predicted by the scale-length model increases with increasing buried-oxide thickness. It is pointed out that there is no acceptable short-channel FDSOI MOSFET models in the current literature.

Starting with the definition of short-channel effects, the high-drain threshold roll-off of a MOSFET is used to evaluate the severity of the short-channel effect. A maximum allowable 100-mV high-drain threshold roll-off serves as the basis for the

determination of the $L_{\min}$ in our design study. The failure of the general scale-length model in predicting the $L_{\min}$ of the fully-depleted SOI device is pointed out by looking into the high-drain threshold roll-off and lateral-field distribution with different buried-oxide thickness. It is shown that the scaling of FDSOI MOSFETs is independent of the BOX thickness when the BOX thickness is much larger than the Si thickness. An empirical $L_{\min}$ prediction equation for undoped FDSOI MOSFETs is given by approximating the constant $L_{\min}$ contours. In the limit of very high-k gate insulators, $L_{\min} \sim 5 t_{Si}$.

Other factors affecting short-channel scaling in FDSOI MOSFETs studied are: body doping, buried-insulator permittivity and bandgap, and substrate biasing. An empirical equation predicting $L_{\min}$ for doped FDSOI MOSFETs is given. By doping the silicon body such that the entire depletion region is within the silicon film, $L_{\min}$ can be improved from $\sim 5 t_{Si}$ to $\sim 2 t_{Si}$. However, the benefits of body doping are offset by the deleterious effect such as dopant fluctuation effect and carrier mobility degradation due to impurity scattering. A buried insulator with bandgap higher than 2.12 eV is needed to prevent additional leakage currents underneath the silicon body. Since the normal component of displacement is continuous in the Si/BOX interface, lower buried-insulator permittivity can enhance the vertical field and reduce SCE. An empirical equation predictiing $L_{\min}$ for undoped FDSOI with different buried-insulator permittivities is developed. $L_{\min}$ is reduced by 15% from

$\varepsilon_{BOX} = 3.9\varepsilon_0$ to $\varepsilon_{BOX} = \varepsilon_0$. A reverse substrate bias voltage (for nMOSFET) can improve the short-channel effect in FDSOI MOSFETs. However, holes accumulate at the bottom of the silicon body when a very high reverse bias voltage is applied to the substrate. This leads to history effect in FDSOI MOSFETs.

Finally, the scaling limits of FDSOI MOSFETs are discussed from both the electrostatic and the performance perspectives. 10-nm FDSOI MOSFET requires scaling both high-k gate-dielectric and silicon-film thickness to their limits of ~2 nm from the electrostatic perspective. However, carrier mobility is severely degraded by surface scattering in a 2-nm silicon film based on published experimental data. The scaling limit of the silicon-film thickness is ~3 nm from the performance viewpoint. The scaling limit of FDSOI MOSFETs with, e. g., HfO_2 gate dielectric is then ~17 nm unless there is a breakthrough on the mobility of thin silicon-film.

For suggestions of future work, it would be appropriate to update the thin silicon-film mobility data to include recent technology advances such as strained-Si-directly-on-insulator, and then re-consider the feasibility of 10-nm FDSOI MOSFET. A more hardware-calibrated mobility model would be helpful in the performance assessment of 10-nm FDSOI MOSFET.