Title
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A SIMPLE MULTIFUNCTION DISCRIMINATOR FOR
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A SIMPLE MULTIFUNCTION DISCRIMINATOR FOR MULTICHANNEL TRIGGERS* LBL-14456

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Abstract

A simple version of a multifunction timing discriminator using only two integrated circuits is presented. It can be configured as a leading edge, a constant fraction, a zero cross or a dual threshold timing discriminator. Since so few parts are used, it is well suited for building multichannel timing discriminators. Two versions of this circuit are described: a quadruple multifunction discriminator and an octal constant fraction trigger. The different compromises made in these units are discussed. Results for walk and jitter obtained with these are presented and possible improvements are discussed.

Introduction

The Plastic Ball Experiment at the Bevalac[1] is an experiment which uses a 4π detector to look at all particles coming from reactions with relativistic heavy ions. To trigger the Plastic Ball a trigger counter--the plastic wall--was built. It consists of 160 plastic scintillators coupled to photomultipliers. A trigger signal is generated using timing signals from the plastic wall. To make these timing signals independent from the widely varying amplitudes, a constant fraction trigger[2] had to be used. Therefore, for this application, a very simple, low cost and low power circuit suitable dense packing had to be developed.

Basic Concept

The original circuit of the constant fraction trigger[2] can now be implemented with a minimum of Integrated Circuits (IC). It needs basically two fast comparator ICs, a coincidence, a oneshot IC and a line driver IC. The coincidence can be implemented as a wired AND connection if ECL is used, as in Fig. 1 or with a separate AND gate IC.

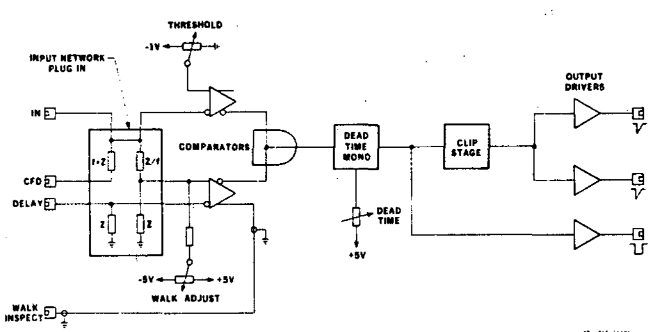

Fig. 1. Block diagram of the simplied constant fraction discriminator. Note the wired AND used as coincidence.

Three versions of these simplified circuits have been considered using ECL logic: the simplest implementation can be built with a fast dual ECL comparator--the SP9687 was used--an ECL oneshot (MC10198) and an ECL to NIM translator (MC10192). However, the current needed for this version at -5.2 V is about 250 mA excluding pull down resistors. This exceeded the limitation for the Plastic Ball experiment, where as many as eight discriminator channels had to be packaged into a single width NIM module. A design using these ICs for a quad constant fraction discriminator has been published elsewhere confirming the high power requirement[3].

Therefore, two other versions were studied. One used the SP9687 as the fast comparator, a SP16F60 gate as the coincidence, a 11C70 flip flop with appropriate feedback and two ECL to NIM translators built with NPN transistors wired as current sources. Whereas this version resulted in the best performance--as will be discussed later--the fact, that it needs three ICs and about 160 mA excluding pull down resistors at -5.2 V made it very difficult to squeeze eight channels into a single module.

The final version, built with the SP9687, a MC10130 dual flip-flop wired as a oneshot and a clip stage, and PNP transistor emitter followers as ECL to NIM translators, needs only 85 mA at -5.2 V. Since only two ICs are needed, it proved possible to design an octal constant fraction discriminator for the plastic wall (dubbed wall box)and squeeze it into a single width NIM module.

Design

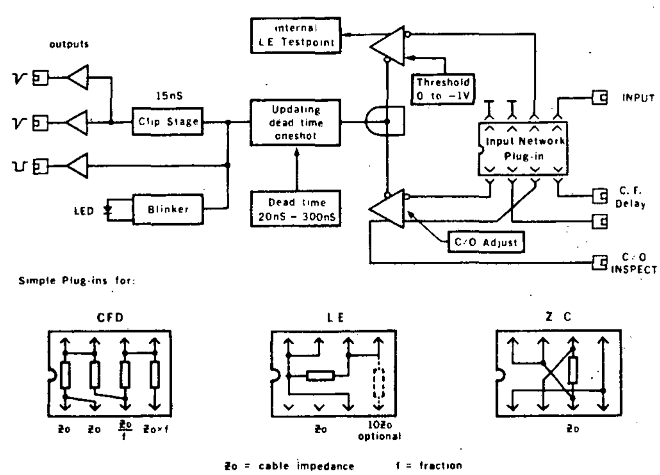

Fig. 2. Block diagram of one channel of the quad "constant fraction discriminator," showing plug ins for the constant fraction (CFD), leading edge (LE), and zero cross (Z/C) discriminator functions.

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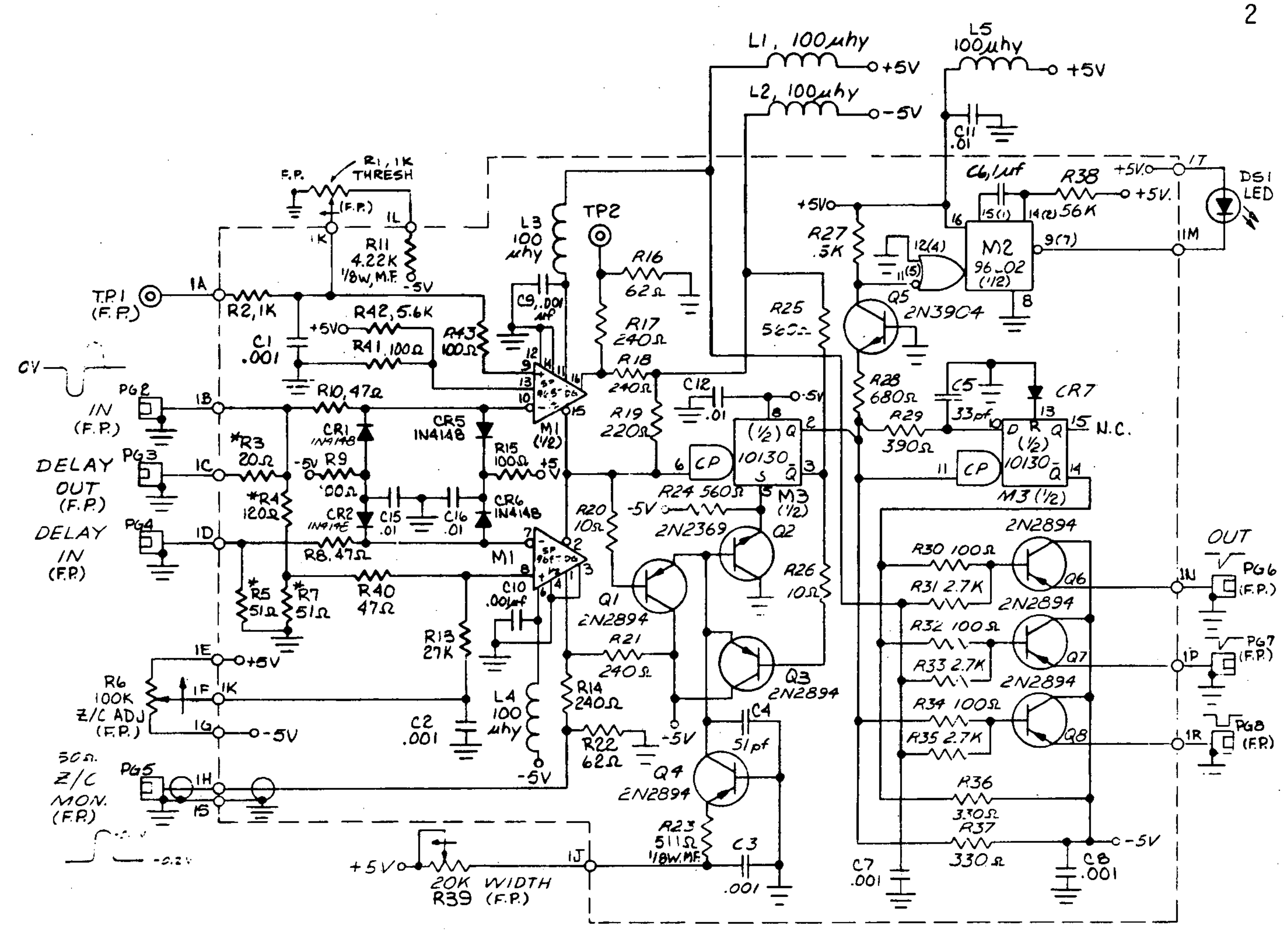

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Fig. 3. Schematic of one channel of the quad constant fraction discriminator

The block diagram of a quad constant fraction trigger using the SP9687 and the MC10130 is given in Fig. 2. Since there are two comparators per discriminator channel in this design, a flexible arrangement of the input connections these two comparators was chosen. This allows to configure the inputs of the comparators to implement some of the many schemes to derive timing information from fast analog pulses. The input network was placed on a IC header plug-in, which allows to set up different input connections very easily. An input network arrangement with switches similar to the design of Ref. (4) would have taken too much space. Here the wired AND connection at the outputs of the comparators acts as a coincidence. Since this produces the AND condition only for negative going ECL signals, the input connections to the comparators have to be made accordingly. The detailed circuit diagram of the quad constant fraction discriminator is given in Fig. 3. The wired AND connection at the comparator output triggers one half of the MC10130 dual latch. When it has been set, a capacitor which was clamped to -.8 V by a PNP emitter follower (Q3) is charged positive by a current source. When the voltage there reaches -.4 V which is translated to ECL levels via a NPN (Q1) emitter follower, it resets the latch and discharges the capacitor to -.8V again.

The second half of the MC10130 is used to clip the wide dead time pulse coming from the first half to 15 nsec width. The outputs of both stages drive pnp emitter followers which translate the dead time pulse (one output) and the clipped pulse (two outputs) to NIM levels. Each of the four channels has individual adjustments for the leading edge discriminator threshold, the zero cross discriminator offset control and the dead time. There is an inspect output on the zero cross discriminator to set the zero cross discriminator offset reliably. As a convenience to the user a blinker stage has been added, consisting of a TTL oneshot (96LS02) and a LED. This produces light flashes of 10 ms duration whenever the channel has fired, allowing easy visual inspection. The unit uses 650 mA at -5 V and 250 mA at +5.0 V.

To work as a constant fraction discriminator, the appropriate plug-in given in Fig. 2 has to be used, and a delay cable of a length of t delay = t rise x (1 - fraction) has to be connected between the CF delay connectors (for a full discussion see Ref. 2). For the leading edge trigger the leading edge plug-in given in Fig. 2 biases the zero cross comparator such that its output is negative, then the firing of the leading edge comparator triggers the channel. In the zero cross trigger mode, the

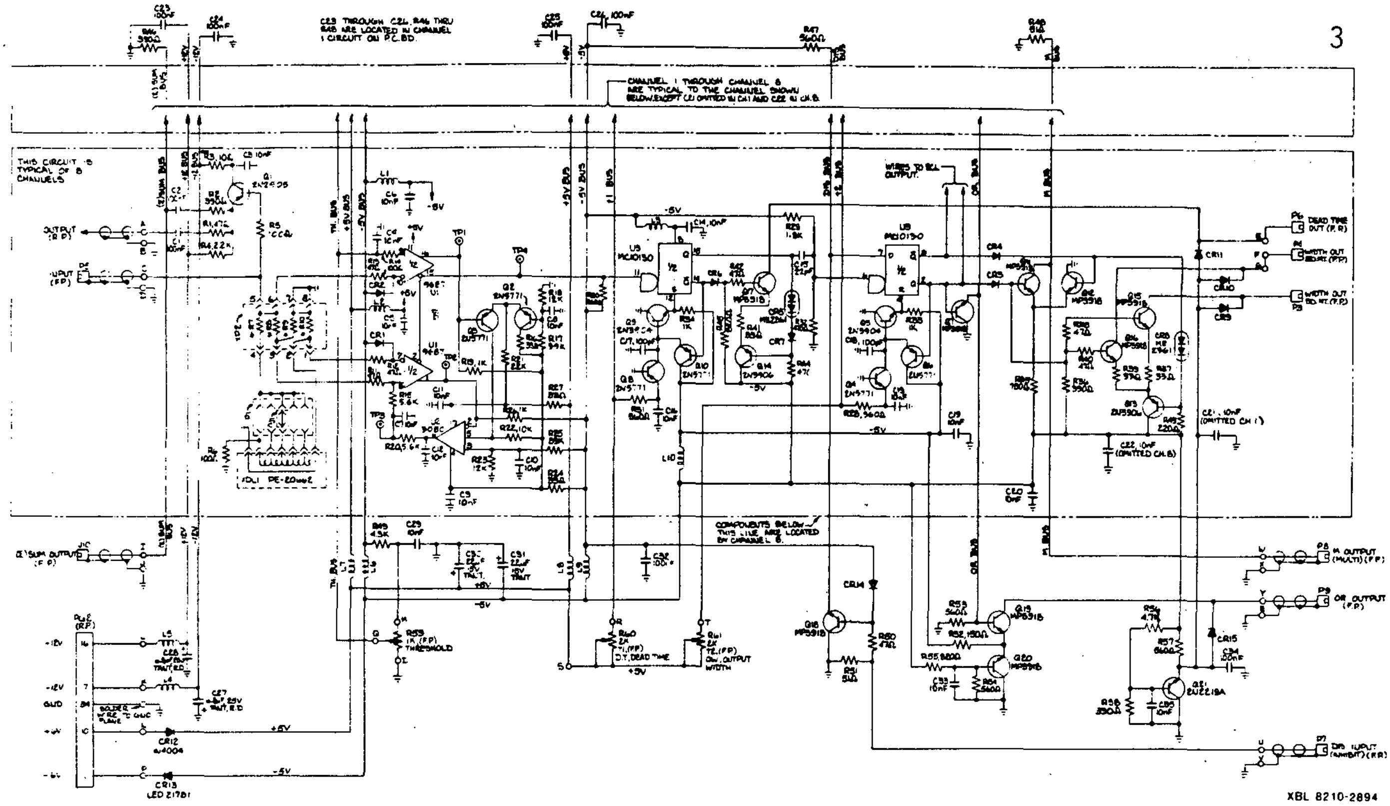

Fig. 4. Schematic of the octal constant-fraction discriminator (wall box), showing the OR, multiplicity (M), and the linear (E) output, as well as the disable output.

plug-in in Fig. 2 is shown assuming a bipolar wave form with the negative lobe leading. The inputs to the zero cross comparator are reversed compared to the constant fraction trigger, and a delay cable equal to the time from the negative peak of the input pulse to its zero crossing has to be connected between the delay connectors.

The schematic of the octal constant fraction discriminator is given in Fig. 4. Here the constant fraction delay is obtained by using a lumped constant tapped delay line, fed at the tap and terminated at both ends. The off-set adjustment of the zero cross comparator is done with a gated base line resistor. This is built with CA3080 transconductance amplifier gated off when the leading edge comparator fires. In its active state it forces the output of the zero cross comparator to -1.3 V, i.e., the threshold voltage of the following MC10130 latch. The dead time and clip stages use the same circuit connections as the dead time stage in the quad constant fraction trigger. The CLIP stage is triggered by the differentiated leading edge of the dead time pulse.

The output stages are "complementary transistor current sources" built with PNP and NPN transistors. These stages draw no standing current, and can sink up to 40 mA in the active state. To make the "wall box" more useful as a trigger device, an OR output of the clipped pulses of all channels is provided, as well as a current sum output which sinks 4 mA per fired channel with an internal termination of 50 Ω. Also a disable input is provided which will inhibit the clip stages with a negative pulse.

In the Plastic Ball experiment, the amplitudes of the signals going into these wall boxes had to be measured also. Therefore, AC coupled emitter followers were placed in parallel with the discriminator inputs. Their outputs can be connected to external ADCs.

Performance

As already discussed elsewhere[5] walk and jitter of these discriminators depend mainly on the characteristics of the comparators. The choice of the SP9687 resulted in a walk of less than 100 ps for input signals between -50 mV and -3 V[6]. The quad constant fraction trigger as described here displayed a jitter of less than 20 ps for pulses larger than -1 V. Double pulse resolution was 20 ns. To check what improvements could be obtained by using ECL III devices, a prototype discriminator with a SP9687 was built, using a 16F60 as the coincidence and a 11C70 flip flop wired as a oneshot the same way as the 10130. This improved the walk by 20% and reduced jitter to less than 10 ps, at a double pulse resolution of 5 ns[7].

Further improvements seem presently possible only by building faster comparators than the SP9687 which requires very fast transistors (f_T > 10GHz). Especially the performance with very narrow input pulses (< 1 ns) can only be improved with faster comparators was well as a faster oneshots. It is obvious that this requires much more effort than using presently available IC which seem to be adequate for most applications.

Acknowledgment

This paper would not have been written without the encouragement of and the long discussions with Helmuth Spieler.

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