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Heteroepitaxial Growth And Deposition Of Semiconductor And Metallic Nano-Materials With Intermediate Layers

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HETEROEPITAXIAL GROWTH AND DEPOSITION OF SEMICONDUCTOR AND METALLIC NANO-MATERIALS WITH INTERMEDIATE LAYERS

A dissertation submitted in partial satisfaction
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

Junce Zhang

December 2015

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Abstract

HETEROEPITAXIAL GROWTH AND DEPOSITION OF SEMICONDUCTOR AND METALLIC NANO-MATERIALS WITH INTERMEDIATE LAYERS

by

Junce Zhang

Research of heteroepitaxial growth and deposition of semiconductor and metallic nano-materials is significant in materials science and engineering for numerous applications due to the significant flexibilities in designing distinctive material systems it offers.

Semiconductor nanowires on mechanically flexible metallic substrates by heteroepitaxial growth, as a novel material platform, could be very promising for many applications. The epitaxial growth of semiconductor (indium phosphide and silicon) nanowires by metal organic chemical vapor deposition and plasma enhanced chemical vapor deposition are developed with the goal of understanding their electrical, thermal and optoelectronic properties while developing scalable, manufacturable solutions for thermoelectric devices at a low cost. However, it is extremely difficult to grow semiconductor nanowires directly on the metallic substrates mainly because of the reaction between the growth precursors and the substrates. Aluminum-doped zinc oxide thin film on polycrystalline copper foil was proposed and demonstrated for indium phosphide nanowire growth, as well as

establishing a reliable electrical contact by utilizing conductive oxide thin films as a template layer. A thin film of titanium nitride barrier layer was utilized to assist silicon nanowire growth on copper foils by forming an Ohmic contact between the nanowires and the substrates.

On the other hand, heteroepitaxy of metallic thin films on semiconductor substrates was extensively studied as a method of electrode plating for various devices. Significant drawbacks still existed in this relatively matured material system, e.g. the rough surface of ultra thin silver film on silicon substrates as a significant obstacle for optoelectronics devices. A thin germanium nucleation layer was introduced to adjust the surface roughness of the silver thin films. This demonstration of ultrasmooth silver thin films offers an advantageous material platform with scalability for applications such as optics, plasmonics, and photonics.

To my parents,
Fucheng Zhang and Shuping Jin
For their endless love
致我的父親母親
張福成 和 晉淑苹
感謝父母的養育之恩

To Prof. Luca Trevisan,
Who encourages and supports me consistently.

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2. Zhang, J., Wei, M., Fryauf, D. M., Leon, J. J. D., Norris, K. J., Deng, H., & Kobayashi, N. P. Single-crystal indium phosphide nanowires grown on

polycrystalline copper foils with an aluminum-doped zinc oxide template.*Journal of Materials Science*, *50*(14), 4926-4932.

3. Zhang, J., Fryauf, D. M., Garrett, M., Logeeswaran, V. J., Sawabe, A., Islam, M. S., & Kobayashi, N. P. (2015). Phenomenological Model of the Growth of Ultrasmooth Silver Thin Films Deposited with a Germanium Nucleation Layer.*Langmuir*, *31*(28), 7852-7859.

Chapter 1

Introduction

1.1 Heteroepitaxy of semiconductor and metallic materials

Heteroepitaxy has been extensively implemented for numerous applications[1,2] as it offers significant flexibilities in designing distinctive material systems, which require both high-performance electrodes and the novel properties of semiconductor nanostructures.

For instance, heteroepitaxy of metal on semiconductor was viewed as an ultimate form of electrodes for various devices[3,4], while the rough surface of the metallic thin films is a significant drawback for optical applications such as superlenses and hyperlenses. Ultra smooth metallic thin film deposition on semiconductor is highly desired to achieve high quality optical devices.

The opposite scenario, heteroepitaxiy of semiconductor on metals or metallic surfaces is less common[5,6]. At present, deposition, rather than heteroepitaxy, of semiconductor on metal merely results in non-single crystal semiconductor films[7,8]. If single-crystal semiconductor nanostructures (e.g. quantum dots and nanowires) could be directly formed on metallic substrates, they would offer scalable and cost-effective material platforms for a variety of devices which require both high-performance electrodes and the novel properties of semiconductor nanostructures. A new way of growing single-crystal semiconductor nanostructures on metallic substrates using Intermediate Layers can be very meaningful for various applications. Since the Intermediate Layer inserted between semiconductor nanostructures and a metal substrate is electrically conductive and electrically connected to both the metal substrate and the semiconductor nanostructures, using such a template does not invalidate the objective of growing semiconductor nanostructures on metallic surfaces; in fact, devices fabricated on an electrically conductive template film could benefit from additional functionalities brought by the template film.

1.2 Thermoelectrics

More than 57 exajoules of energy is lost to the environment in the United States annually in transportation and electricity generation[9]. A large portion of waste heat lost industrially is low grade heat, below ~260°C, where efficiency undergoes significant drops in a conventional heat engine, such as the Rankine cycle[10]. Thermoelectrics (TE) is a technology to convert heat into electrical energy directly through the Seebeck effect. TE devices can function as solid state coolers, heat pumps and energy harvesting devices in a wide range of applications[11]. Energy harvesting is anticipated to be the largest market for TEs. Presently, an estimated 15 terawatts of waste heat is generated in industry, transportation and commercial systems[12].

Recovery of even a fraction of this energy would have a large impact on energy savings in the US, as well as reduce dependence on imported oil and reduce greenhouse gas emissions. High efficiency TE devices could also provide localized cooling for personnel and electronic systems, as well as localized temperature control for medical and scientific applications. Replacing closed cycle refrigeration systems with high efficiency TEs would save energy and eliminate the need for environmentally unfriendly refrigerants. The Figure of Merit (ZT) for a TE device is defined as:

$$ZT = T\sigma S^2/\kappa$$

where T is the temperature, σ is the electrical conductivity, κ is the thermal conductivity, and S is the Seebeck coefficient or thermopower (conventionally in $\mu V/K$). Higher values of ZT mean higher efficiency and larger amounts of electrical power harvested per given amount of thermal energy.

Typical TE modules based on bulk materials are composed of an arrangement of two types of TE legs. A p-type semiconducting leg and an n-type semiconducting leg are arranged in parallel relative to the flow of heat across the device but in series relative to the flow of electricity as shown in Figure 1.1[13]. Connecting the legs in series electrically allows the small voltage from each individual leg to sum to a useful quantity at the outputs of the module. Alternatively, an electrical current can be supplied to the electrical leads of the module and a temperature gradient will develop across the device which can be used in either heating or cooling.

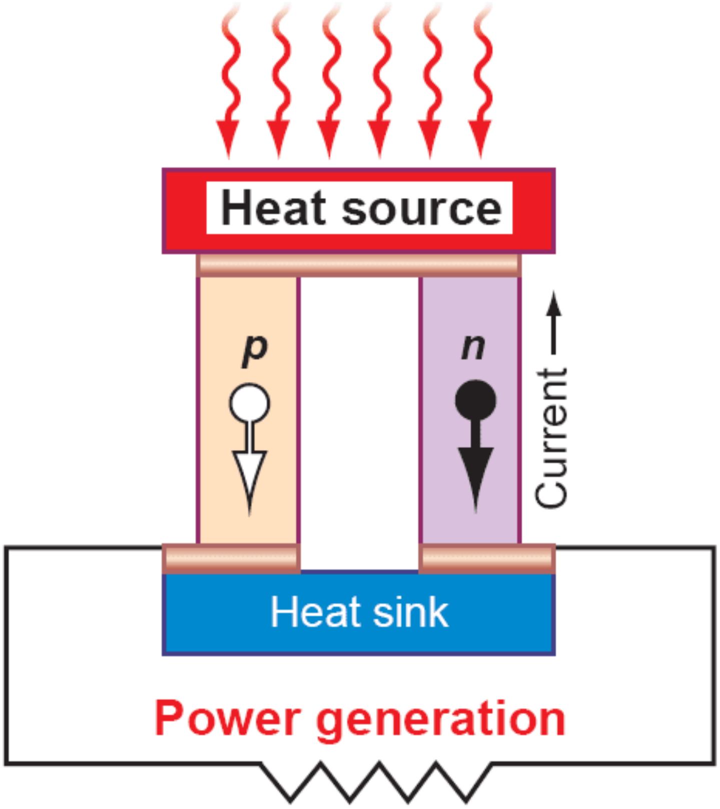


Figure 1.1 Illustration of a conventional TE device based on bulk materials

Conventional TE devices based on bulk semiconductors have two major limitations; (1) limits on scalability of the device for large-scale implementation, and (2) limits on performance of the device due to the interplay of electronic and phonon behavior. These two limits are a direct consequence of the fact that conventional solid-state TE devices are built using very expensive, single-crystal bulk semiconductors, which dominate overall manufacturing cost and offer very limited scaling. The total output for a TE device scales with the effective device volume, which in turn is limited by the size and availability of single-crystal semiconductor substrates. Therefore, the ultimate approach would be to develop TE devices based on low-cost materials with large scale manufacturing, which unfortunately cannot be done with conventional bulk semiconductors. The limits on the performance of TE devices are primarily associated with the TE material's figure of merit, as defined above. Thus, a good TE material should have high electrical conductivity to minimize Joule heating, low thermal conductivity to prevent thermal shorting, and a high Seebeck coefficient for maximum conversion of heat to electrical power. Unfortunately, these physical properties are all inter-related in bulk semiconductors and cannot be optimized independently. It is apparent that a disruptive non-conventional material platform needs to be developed, for large-scale implementation of high-performance TE power generation devices. Two previous nanoscale architectures have been proposed to develop TE materials with ZT higher than 1, including superlattice structures within a bulk semiconductor matrix, and metallic nanoparticles embedded in a bulk semiconductor matrix. These two architectures still require high-quality bulk semiconductors to start with, therefore their scalability and cost are still issues.

1.3 Semiconductor nanowires

Nanomaterials have many unique properties which are not seen in the traditional bulk materials. When the dimension of the structures shrinks into the scale of tens of nanometers or less, within the same magnitude of the De Broglie wavelength of the charge carriers, quantum confinement occurs with an altered density of states (DOS).

Nanowires (often referred to as one-dimensional or 1-D materials) have many unique and interesting characteristics not seen in bulk materials. Electrons in nanowires are quantum confined laterally and thus occupy energy levels that are different from the continuum energy bands in bulk materials. Nanowire materials have been investigated for a wide range of electronic, optical and mechanical applications. Nanowires have also shown promise for TE applications. The growth of many different Group IV (e.g. silicon) and Group III-V compound (e.g. indium phosphide) semiconductor nanowires has previously been demonstrated. Most of the nanowire growth studies reported in the literature were done on single-crystal semiconductor substrates. However, for the applications of TE devices, single crystal semiconductor substrates are not necessary. Inexpensive substrates offer the potential for lower manufacturing costs and greater scalability for TE devices. By tuning the parameters in ZT, it is possible to create materials with superior performance. Increasing ZT has proven difficult, but through the use of nanowires it is possible to get performance comparable to the best bulk materials from materials that are safer and less expensive. By developing nanowire materials from traditionally good TE materials it will be possible to push beyond the current barriers in performance.

1.4 Ultra thin and smooth silver films

Silver (Ag) thin films have been the most frequently employed material for innovative applications in a wide range of fields including nanoplasmonics,[14,15,16] solar energy,[17,18,19] optical waveguides,[20] OLEDs,[21] and superlenses[22]. This is mainly due to its lower contact resistance, lower refractive index (~0.1), [23] lower extinction coefficient and higher reflectivity in the visible wavelength range when compared with other practical metals. The conventional methods of depositing Ag thin films on insulators by e-beam evaporation,[24] chemical vapor deposition,[25] ion-beam sputtering,[26] RF/DC sputtering,[27] electroless plating,[28] and pulsed laser deposition[29] tend to proceed in Volmer-Weber mode[30], thus resulting Ag thin films often exhibit rough surface morphologies. Such rough surface morphology combined with large grains contained in these films leads to a significant surface plasmon polariton scattering loss,[31] which severely lowers performance and yield of, for instance, plasmonic devices and metamaterials.[32,33] In previous research, the root-mean-square (rms) roughness of Ag films decreased from ~6nm to 0.6-0.8nm with a thin (0.5-5nm) germanium (Ge) nucleation layer atop a SiO_2 layer on Si (100) substrate[34]. Many studies followed and showed that thin films of metals such as nickel,[18] copper,[35] and chromium[36, 37] also work as a nucleation layer that achieve sub-nanometer rms roughness of Ag thin films. Furthermore, polymers such as poly(3,4-ethylenedioxythiophene): poly (styrenesulfonate) (PEDOT:PSS)[18,19] were also found to work as a nucleation layer. Ultrasmooth Ag films with a grain size smaller than the electron mean free path in the bulk material (~52 nm) would increase the collision rate and damping rate to enhance the optical loss[38], which is a significant disadvantage for optical applications such as superlenses and hyperlenses. W. Chen et al[39]. reported that post-deposition annealing treatment under optimized conditions can significantly reduce the optical loss to the value of bulk Ag while maintaining the ultrasmooth Ag film surface with the Ge nucleation layers.

The morphological and crystallographical characteristics of Ag thin films with thin film assistant layers studied with understanding of the physical and chemical roles played by the Intermediate Layers[40] will be devoted in Chapter 6.

Part I:
Growth of Semiconductor nanowire networks

Chapter 2

Fundamentals of Semiconductor Nanowire Growth

2.1 Metal Organic Chemical Vapor Deposition

Metal Organic Chemical Vapor Deposition (MOCVD) was developed by Dr. H.M. Manasevit in 1968 to grow single crystal gallium arsenide (GaAs) on insulating substrates with a metallic and an organic precursor at the same time[41]. Nowadays, MOCVD is the most widely used bottom-up method for thin film and nanomaterial epitaxial growth for a variety of large scale manufacturing processes due to its relatively fast growth rate and high degrees of growth control. The ability of MOCVD to grow very thin layers and to alternate different precursors within a very short time can create high-quality quantum wells. The atoms to be deposited are transferred by a carrier gas to the growth chamber in the vapor phase bound to organic species. While the precursors are flowing in the chamber, the organic bonds are broken by thermal cracking at the substrate or in a plasma, and the metal atoms can react with each other or with the substrates. The drawbacks of this epitaxial growth method is the expensive and hazardous precursors it requires to utilize.

The indium phosphide (InP) nanowires studied in this work were grown by

MOCVD showed in Figure 2.1, which was installed at Delaware 2300 Lab, UC Santa Cruz.

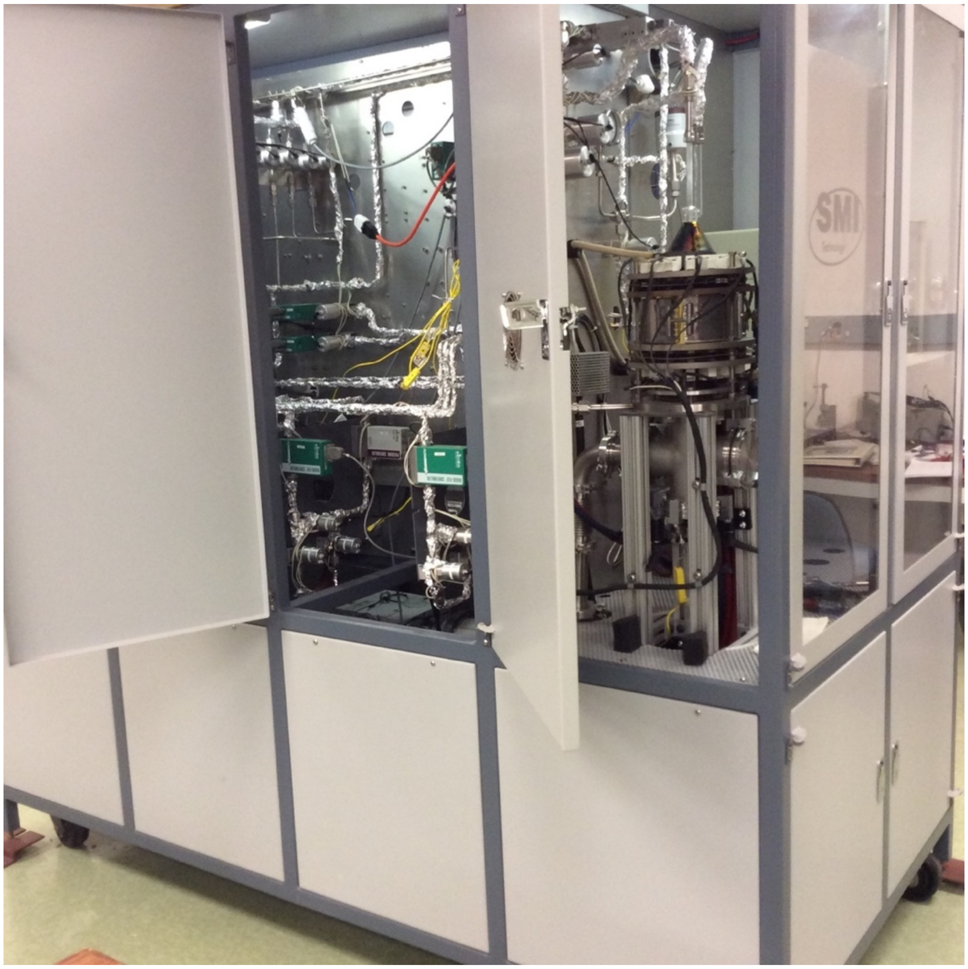


Figure 2.1 MOCVD installed at NECTAR Thin Films Lab, UC Santa Cruz.

As illustrated in Figure 2.2[42], the main screen of the Programmable Logic Controller (PLC) shows the schematic of the MOCVD reactor. PLC enables us to create recipes and adjust growth parameters (valves open and close, plasma on and off, process time, flow rate, mass flow, pressure, temperature etc.) directly in the software to control the hardware. The red dot indicates the valve is closed and the white one means it is open. Four precursors or dopants can be installed in the system. Various gases (e.g. hydrogen, nitrogen, argon) can be transported in to the reactor chamber for different purposes.

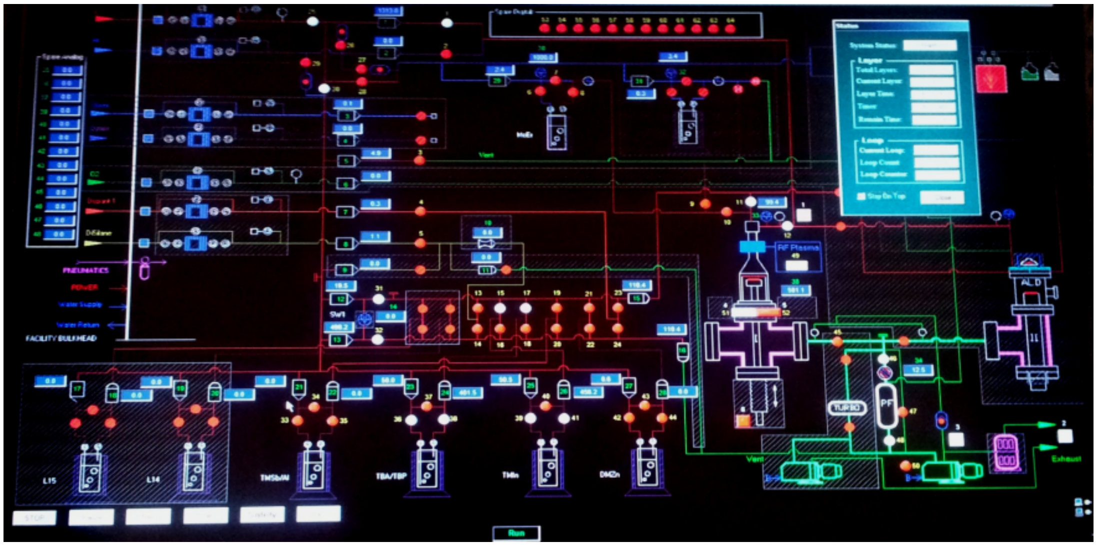


Figure 2.2: Schematic of the reactor of the control system.

The reactor chamber we are using shown in Figure 2.3 is a vertical chamber made of quartz, which makes it easier to replace and clean. A two-inch stage is installed in the chamber to hold the substrates with the gas flowing from the top to create a uniform layer along the stage. A halogen lamp heater, made of twelve high power halogen lamps, generates light and dissipates heat to produce a smooth temperature profile along the stage.

Figure 2.3 A photograph of the vertical MOCVD reactor chamber

The Low Frequency Radio Frequency - 501 (LFRF-501) Plasma Source, a model created by Dr. Kobayashi from UCSC in conjunction with Oak Ridge National Laboratories (ORNL) and Structured Materials Inc. (SMI), was used in the MOCVD to supply plasma. This new designed low cost plasma source received one of the

R&D 100 Awards in 2012[43]. Figure 2.4 (left) shows the reactor chamber with the lamp heater on but plasma source off. Si wafer coupon substrates on the stage can be observed through the transparent chamber. With the plasma source on, argon ions are generating a characteristic purple glow as exhibited in Figure 2.4 (right). The plasma gas is produced by the ring that can be observed on the upper part of the chamber. A strong electric field is generated with the plasma source operating along the chamber. A heavy gas (i.e. Argon) flowing into the chamber is ionized to supply extra electric energy with the thermal energy from the heater.

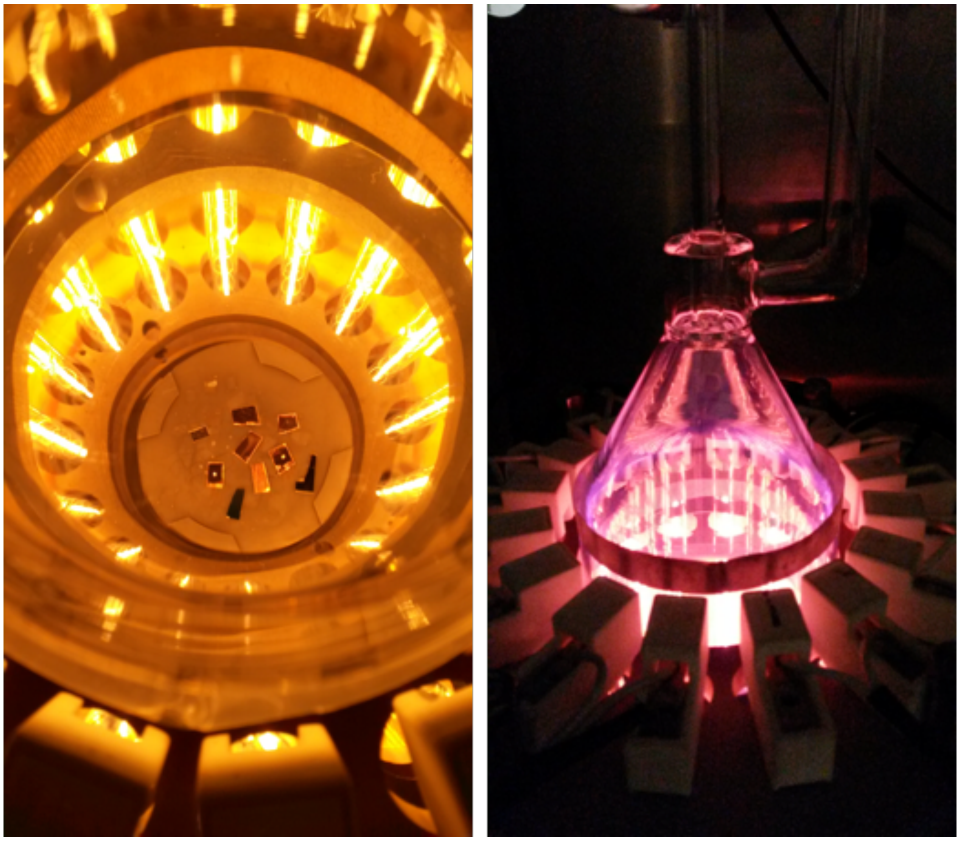


Figure 2.4 Photographs of reactor chamber with plasma source off (left) and on (right).

The silicon nanowires discussed in Chapter 6 were all epitaxially grown by plasma- enhanced chemical vapor deposition (PECVD), which is a chemical vapor deposition technique utilizing a plasma for cracking the precursors.

2.2 VLS growth mechanism

The epitaxial growth of III-V nanowires is normally utilizing the growth mechanism of vapor-liquid-solid (VLS)[44]. VLS is a bottom-up method of fabricating nanowires with assistance of catalysts. As the name indicates, the material to be deposited is introduced as a vapor from precursor then dissolved into liquid clusters with gold nanoparticles in our study. Once supersaturated, the nucleation of clusters within the liquid alloy droplet align with the substrate interface, and as the solid precipitates out below, it forces the liquid nanoparticle upward resulting in nanowire growth.

2.3 Nanowire networks

Conventional epitaxial growth requires single crystalline substrates as the nanowire align to the crystallographic direction of the substrate to form in the vertical direction. The drawbacks of single crystalline substrates are lack of mechanical flexibility and high cost. While nanowires are grown on non-single crystal surfaces, the growth cannot be completely controlled along one specific crystallographic direction. Since the orientations of the nanowires are not normal to the surface any more, nanowires grown fuse together during growth with intersections to form nanowire networks.

Figure 2.5 shows SEM images of the InP nanowire networks grown on Si (111) substrates by MOCVD. A large number of intersections can be observed.

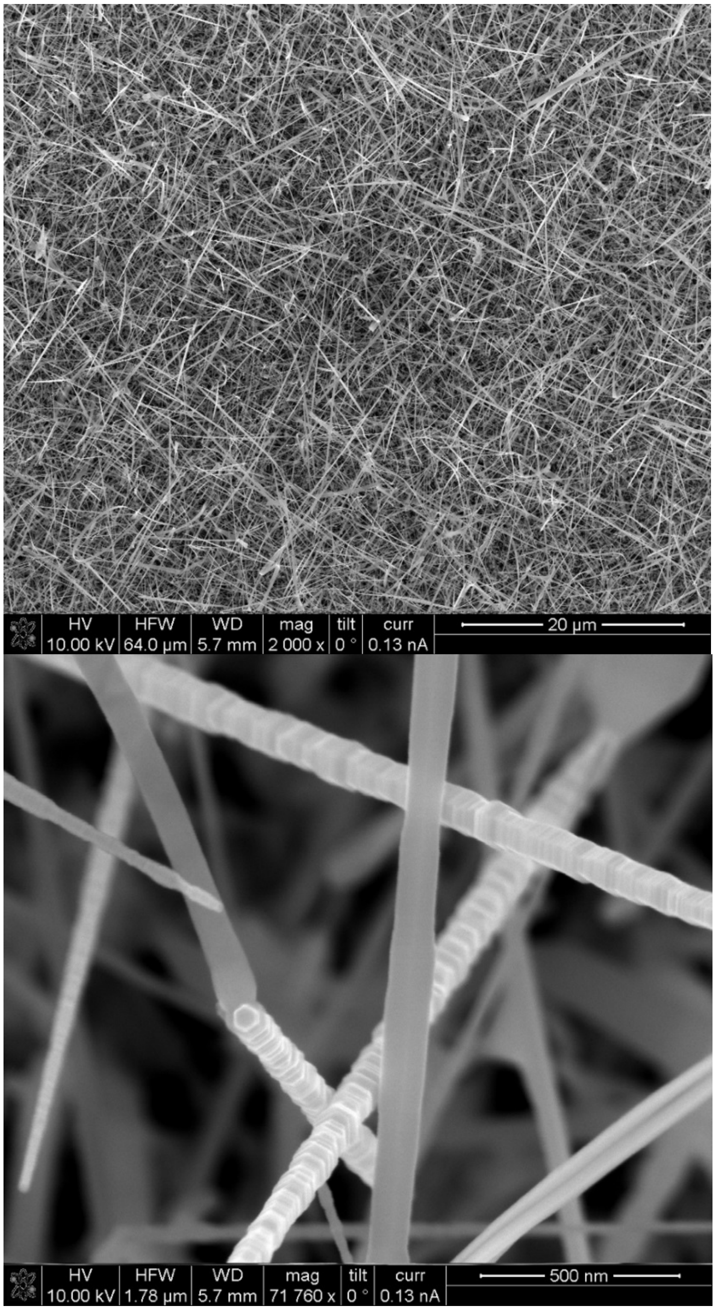


Figure 2.5: Scanning electron microscope (SEM) images of InP nanowire networks grown on Si (100) substrates by MOCVD with different fields of view.

When a phonon travels along the intersection part, it might experience a direction change from one nanowire to another, which can reduce the thermal conductivity for the nanowire networks[45]. Additionally, the intersection could behave as a virtual surface to photons, which is different from continuous bulk materials. Therefore, surface phonon modes could be excited, which results in many different phonon polarizations than those found in bulk materials[46].

Finite element simulation of Comsol multi-physics was utilized to to simulate the thermal conductivity of two types of basic building blocks that form nanowire networks. Two intrinsic indium phosphide nanowires with diameter and length of 50 nm and 1 μm respectively without (shown in Figure 2.5a)) and with intersections (shown in Figure 2.5a)) were compared with temperature profiles along the left nanowire. One bottom Cu plate (kept at 303.15 K) and one top Cu plate (kept at 323.15 K) were attached at the bottom and top of the nanowires as contacts. As shown in Figure 2.6a), the temperature monotonically decreases along the length of the nanowire without any irregularities. In comparison, the temperature decreases along the length of the intersecting nanowire with a deviation that appears approximately 0.4 μm along the nanowire corresponding to the location of the intersection, exhibited in Figure 2.6b). The slope change at the intersection indicates a lower thermal conductivity within the region where the intersection is present.

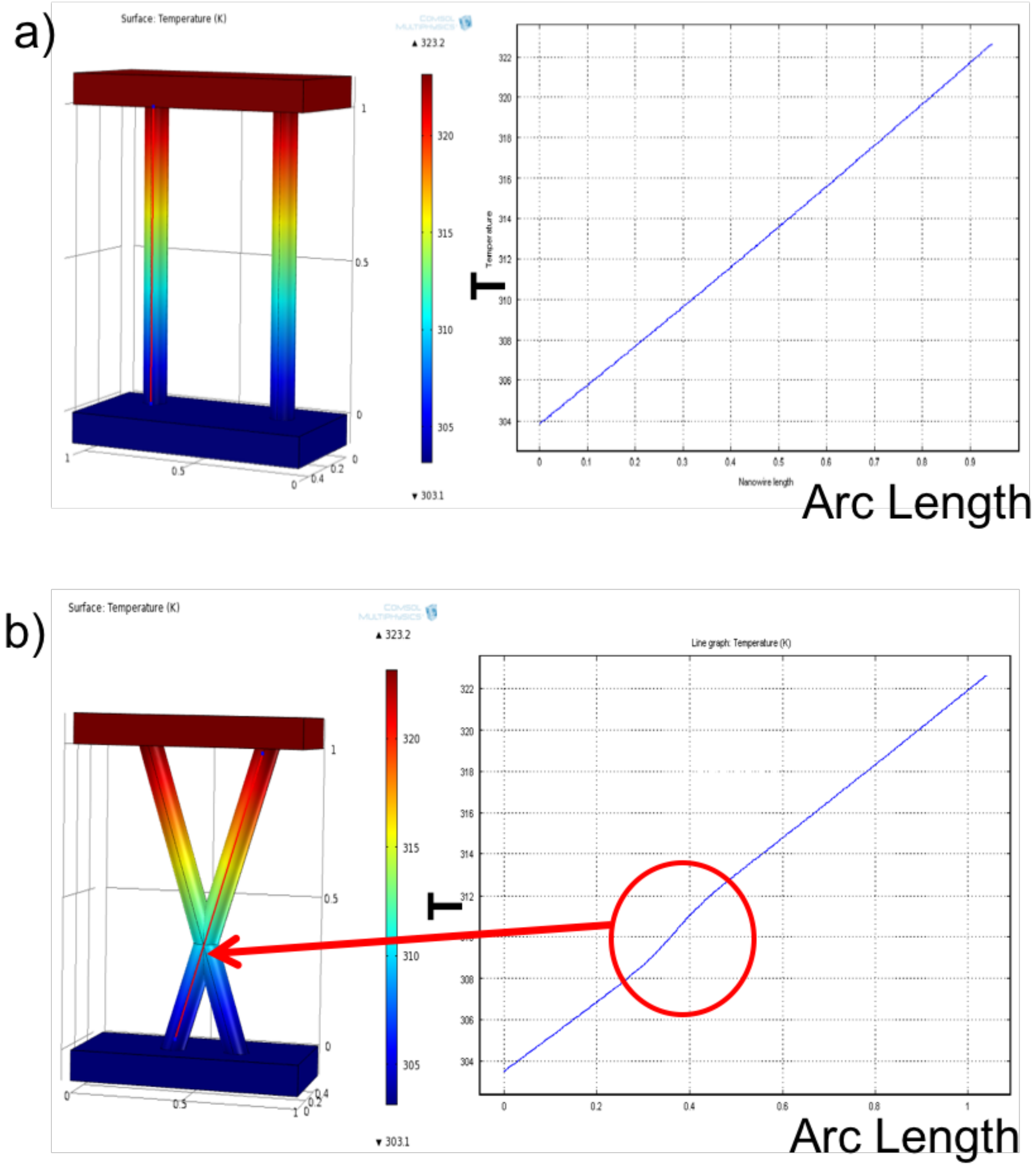


Figure 2.6: Comsol modeling of two types of arrangements of two nanowires; (a) two separated nanowires and (b) two intersecting nanowires, each with modeled temperature profile across the length of a wire.

In this study, the optical properties of InP nanowire networks grown by MOCVD with assistance of gold coating is discussed in Chapter 3. In Part II, growth of InP and Si nanowire networks grown on flexible metallic substrates (i.e. Cu foils) with Intermediate Layers is studied in Chapter 4 and 5 respectively.

Chapter 3

Raman Spectroscopy of Indium Phosphide Nanowire Networks Coated with Gold Clusters

Enhanced Raman signal of the longitudinal optical phonon mode in indium phosphide nanowire networks with gold coating of up to 5 nm thickness was observed experimentally to further study the phonon spectrum of nanowire networks. Indium phosphide nanowire networks coated with different nominal thicknesses of gold were prepared and optically studied. Scanning electron microscopy, photoluminescence spectroscopy and Raman spectroscopy were used to study the dependence of surface morphology and phonon modes of the nanowire networks on the nominal thickness of the gold coating. The Raman peak of longitudinal optical phonon mode for as grown sample was negligible, while the peak intensity for 1nm and 5nm gold coated sample reached to 1379 and 792 a.u. respectively. Electromagnetic enhancement and extinction coefficient are discussed to qualitatively assess the role of the gold coating on indium phosphide nanowire networks.

3.1 Background

In recent years, indium phosphide (InP) in the form of nanowires, especially isolated individual InP nanowires, has been studied with the view toward advanced material platforms for future optoelectronic devices based on extended material concepts that cannot be built on traditional bulk and thin film materials. However, it is highly likely that production-scale devices will utilize ensembles of a large number of nanowires. For instance, dense arrays of nanowires would be needed to increase the external quantum efficiency in a photodetector[47,48] to compromise inherently small absorbing volume of a single nanowire. A unique material system, InP nanowire networks pursued in our research group, uses randomly oriented and intersecting InP nanowires, which form three-dimensional (3D) nanowire networks. Connectivity over distance beyond the length of a single nanowire in nanowire networks allows long-range carrier transport throughout the network and enables nanowire-based optical devices to be designed with added functionality including free carrier and phonon transport in directions nominally perpendicular to the surface normal of a substrate on which the nanowire network is formed. Therefore, it is necessary to understand the collective optical characteristics of physically interacting nanowires that have different sizes, shapes, orientations, areal densities, and crystallinities.

In our previous studies, aluminum oxide deposited by atomic layer deposition was used to study collective optical characteristics of nanowire networks by photoluminescence (PL)[49]. PL was also used to assess dynamics of photo-generated carriers within the nanowire networks[50]. Nanowire networks were also implemented as a part of photoconductors[51]. Apart from PL, Raman spectroscopy has been applied to a wide range of materials due to its versatile accessibility of a broad spectrum of information on solid state excitations (phonons, plasmons, magnons, polarons) and single electronic excitations[52]. However, it was found that Raman spectroscopy was not a practical technique for our InP nanowire networks because of low cross-section and collection efficiency of Raman scattering within the networks made of randomly oriented nanowires (i.e., no unique crystallographic orientation that represents nanowire networks, as a whole, exists) in contrast to Raman spectroscopy on single-crystal bulk InP. It is well known that Raman scattering cross-section is enhanced resonantly (i.e., resonance Raman) when the excitation photon energy is close to that associated with one of electronic transitions in materials under investigation[53]. However, the resonance Raman also increases fluorescence such as PL from samples which hampers Raman signals. Surface-enhanced Raman spectroscopy (SERS) has been widely used to increase Raman signal by placing target molecules on such SERS-enabling surfaces as gold, silver or copper[54,5556], which does not work for our InP nanowire networks that cannot be grown on these metallic surfaces. Post-growth placement of nanowire networks on SERS-enabling metal surfaces would be another route. However, such a transfer process would cause structural damages on the nanowire networks. In one way of utilizing SERS, gold nanoparticles or clusters on which a material of interest is placed are often used. However, for those materials, such as our InP nanowire networks that cannot be placed on gold nanoparticles, there are only few reports on explicitly placing gold nanoparticles on prepared materials of interest. In this chapter, InP nanowire networks covered with different nominal thicknesses of gold were prepared and used to study collective characteristics of their Raman modes.

3.2 Experiments

InP nanowire networks were grown on a 4-inch n-type silicon (100) wafer by low-pressure metal organic chemical vapor deposition (LP-MOCVD) with colloidal gold nanoparticles with a nominal diameter of 10nm. Two metal organic precursors, tertbutylphosphine (TBP) and trimethylindium (TMIn) were used with H_2 carrier gas. Typical growth conditions are as follows; molar flow rates of TBP and TMIn were 4.01×10^{-4}moles/min and 8.34×10^{-5}moles/min. Growth temperature, pressure and time were 425°C, 76torr, and 30 minutes, respectively. InP nanowire networks grew uniformly over the wafer. The as-grown sample was cut into multiple small coupons (~1cm^2) for further sample preparation steps. Gold was deposited on the InP nanowire network coupons by DC sputtering with a deposition rate of approximately 0.1nm per second at room temperature. Three variations were prepared by varying nominal thickness (1, 5, and 10nm) of gold deposited on the coupons (these three samples are referred to as 1, 5, and 10nm gold-coated samples). Subsequently, the three gold-covered samples were annealed under vacuum at 300^{o}C for 30 minutes, and as a result, total four samples including as-grown InP nanowire networks without Au coverage (this sample is referred to as as-grown sample) were obtained for the study.

Field emission scanning electron microscope (FE-SEM, Hitachi S4800) was used to obtain morphological and geometrical characteristics of the samples. PL spectra were collected from the four samples at room temperature using a 532nm CW laser of 6.7mW focused on a nominal spot size of approximately 2mm in diameter.

Raman spectroscopy was performed using an upright confocal Raman microscope (Horiba Jobin Yvon T64000) equipped with a nitrogen-cooled multichannel charge-coupled device (CCD) detector. In Raman spectroscopy, a 784.6nm solid state laser was used as the excitation source with a measured power of 300µW at sample surfaces with a focal spot of approximately 2µm in diameter. All Raman spectra were collected through a 100× objective lens at -122^{o}C, which was the lowest temperature the sample stage could reach.

3.3 Results and discussion

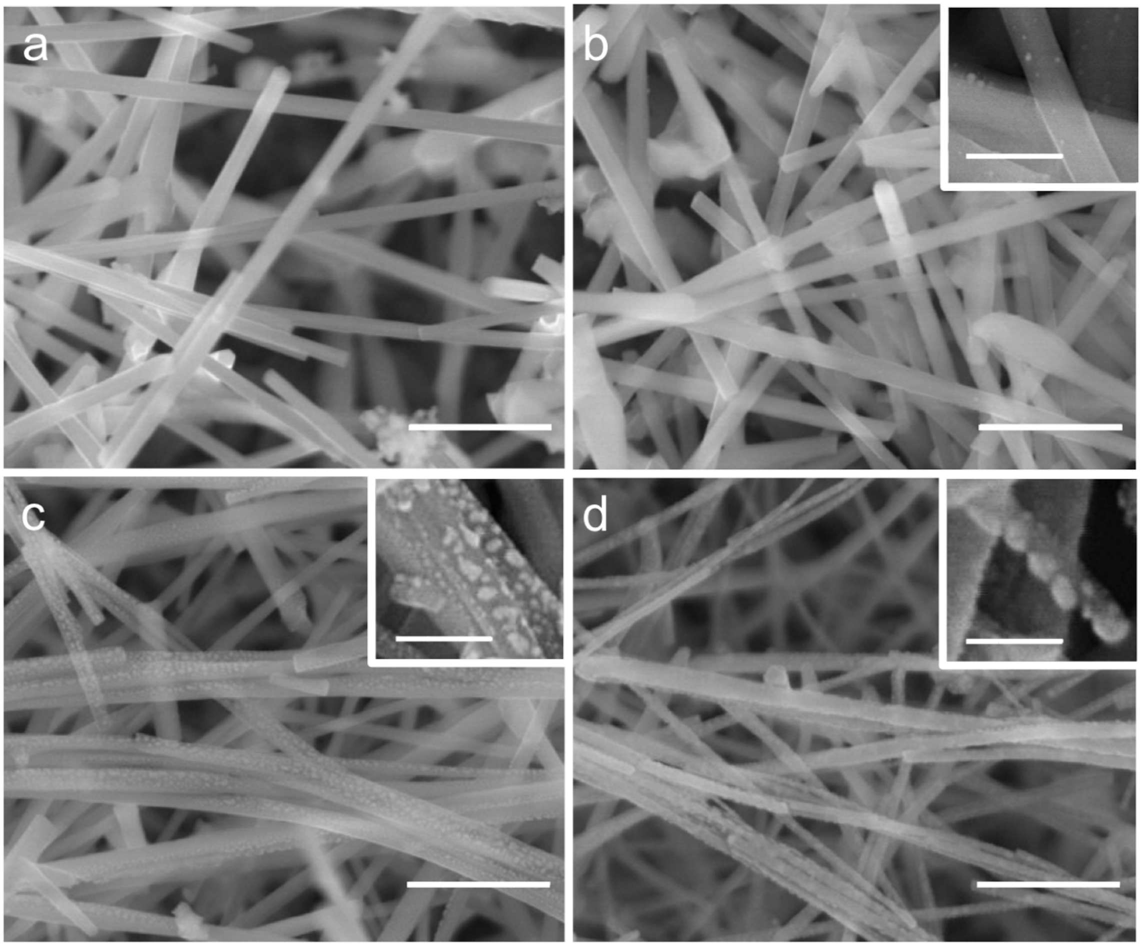


Figure 3.1. FE-SEM images of the four InP nanowire network samples (a) as-grown sample (b) 1nm gold-coated sample after annealing (c) 5nm gold-coated sample after annealing (d) 10nm gold-coated sample after annealing. The scale bars of the main images and the inserts are 500nm and 100nm, respectively.

Figure 3.1 shows FE-SEM images of the four InP nanowire network samples. Figure 3.1(a) shows the as-grown sample in which nanowires with the diameter ranging from 50 to 100nm co-exist. The nanowires are randomly oriented and form intersects when single or multiple nanowires cross at a point in space. Figure 3.1(b), (c) and (d) represent the 1, 5, and 10nm gold-coated samples, respectively and each inset in its respective panel shows a magnified image collected from a representative nanowire in each sample. As seen in Figure 3.1(b), overall morphology of the 1nm gold-coated sample appears to be comparable to that seen in Figure 1(a) of the as-grown sample. However, the inset reveals the presence of gold clusters resulted from the coverage of 1nm gold after annealing. In Figure 3.1(c) and (d), gold clusters can be clearly seen as patches with light contrast attached to the nanowire networks. Various shapes and sizes of gold clusters on the surface of nanowires and the intersections are identified in the insets of Figure 1(b), (c) and (d). The average size and distribution of gold NPs were determined using SEM. The gold clusters in the 1nm gold coated sample can be treated as spheres with diameters from 4nm to 8nm (5nm average); the 5nm gold coated sample has both sphere and cylinder shaped clusters in the diameter range of 12 nm to 38nm (27nm average); the clusters in the 10nm gold coated sample can be considered as cylinders with the length from 23nm to 45nm (37nm average). In other words, the size of gold clusters becomes larger as the nominal thickness of gold deposition increases.

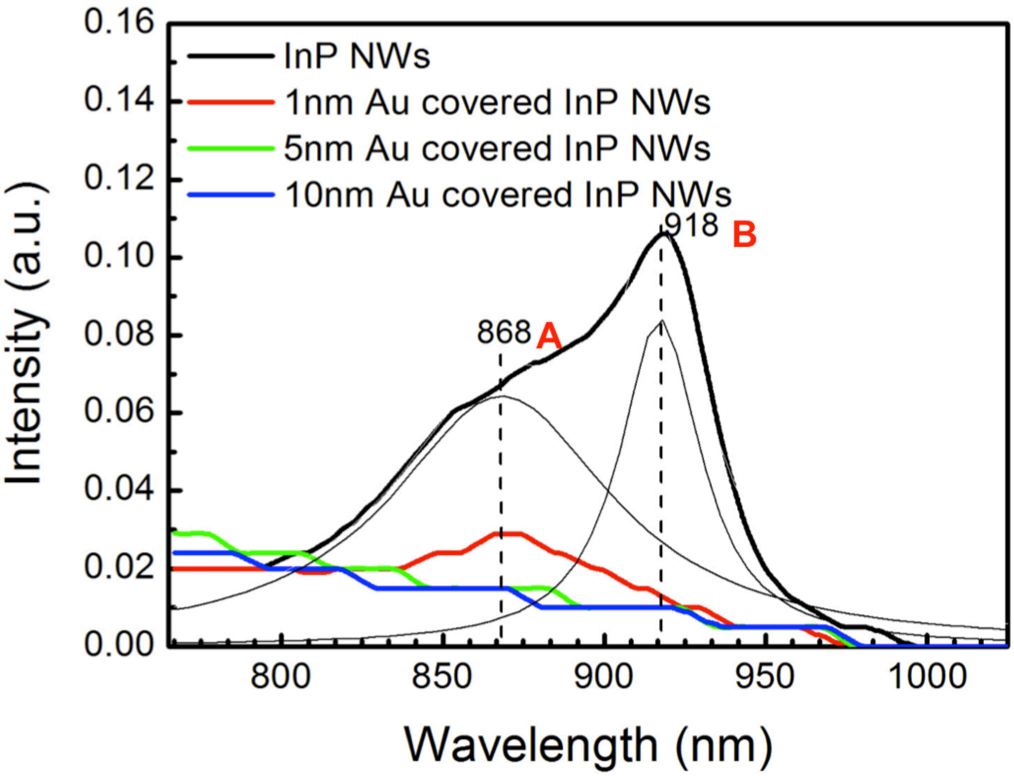


Figure 3.2. Photoluminescence spectra of InP nanowire networks with different gold coating thicknesses.

PL spectra of the samples are shown in Figure 3.2. The PL spectrum of (a) the as-grown sample exhibits the maximum intensity at 918nm with an apparent shoulder on the shorter wavelength side and can be deconvoluted into two spectra with peaks at 868nm denoted by A and 918nm denoted by B. Guided by our previous study[2], we concluded that these two deconvoluted spectra are associated with two types of nanowires characterized by two type of crystal structures; zincblende (ZB) and wurtzite (WZ) InP co-existing in the networks. Upon the deposition of gold, the

918nm peak intensity decreased significantly for all of the 1, 5 and 10nm gold-coated samples and the 868nm peak could be observed only on the 1nm gold-coated sample. This fluorescence quenching can be explained partly by the excitation laser light being absorbed and scattered by the gold clusters and converted into heat[57]. As the size of gold clusters increases, the fluorescence quenching becomes more pronounced.

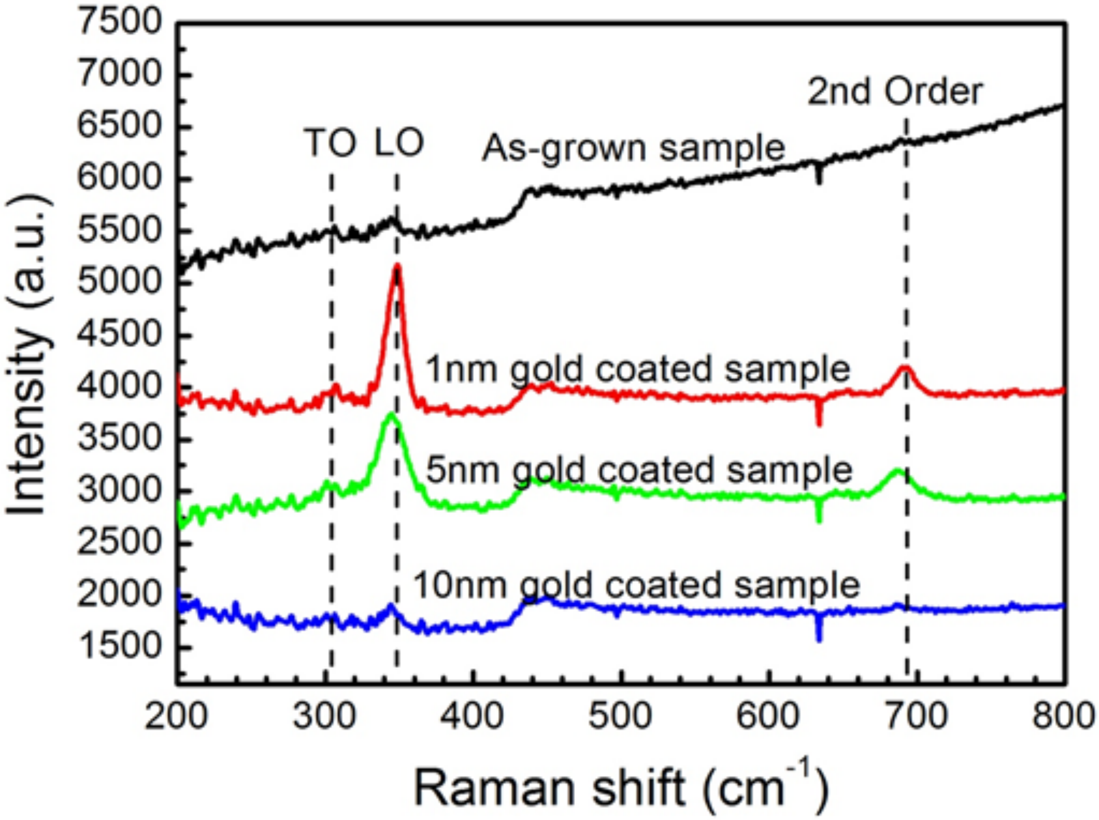


Figure 3.3 Wide-range Raman spectra of the four samples.

Raman spectra collected from the four samples are shown in Figure 3.3. In all spectra, the rise at 443cm^{-1} was caused by the spectrometer that switched optical gratings, and the spikes at 498cm^{-1}and 637cm^{-1} resulted from merely system noise.

On the spectrum of the as-grown sample, two peaks at ~345cm^{-1} and ~305cm^{-1} correspond well to the longitudinal optical phonon (LO) and the traverse optical phonon (TO) modes of bulk InP and are associated with respective Brillouin zone center (Γ). The 1nm and 5nm gold-coated samples show a peak at around 690cm^{-1} identified as a second order peak corresponding to 2TO (Γ) mode phonons[58], while, for the as-grown sample, this mode is hardly observed because it overlaps with the side robe of the 868nm PL peak as seen in Figure. 2. The 2TO (Γ) mode peak of the 10nm gold-coated sample is much weaker than that of the 1nm and 5nm gold-coated samples, which is consistent with the weaker TO mode peak of this sample at ~345cm^{-1}. In Figure 3.4, the Raman spectra are plotted in the range from 200cm^{-1} to 400cm^{-1} after monotonically varying background was subtracted from each spectrum. In the inset of Figure 4, the peak intensities of the LO mode of the samples are plotted as a function of the nominal thickness of the gold coating. It can be observed that the as grown sample showed no obvious peak while the peak intensity for 1nm and 5nm gold coated sample reached to 1379 and 792 a.u., but the peak intensity for 10nm gold coated sample was negligible again. So the LO mode signal is significantly increased on the 1nm gold-coated sample, but as the gold cluster size increases for the 5nm and 10nm gold-coated samples, the signal diminishes rapidly.

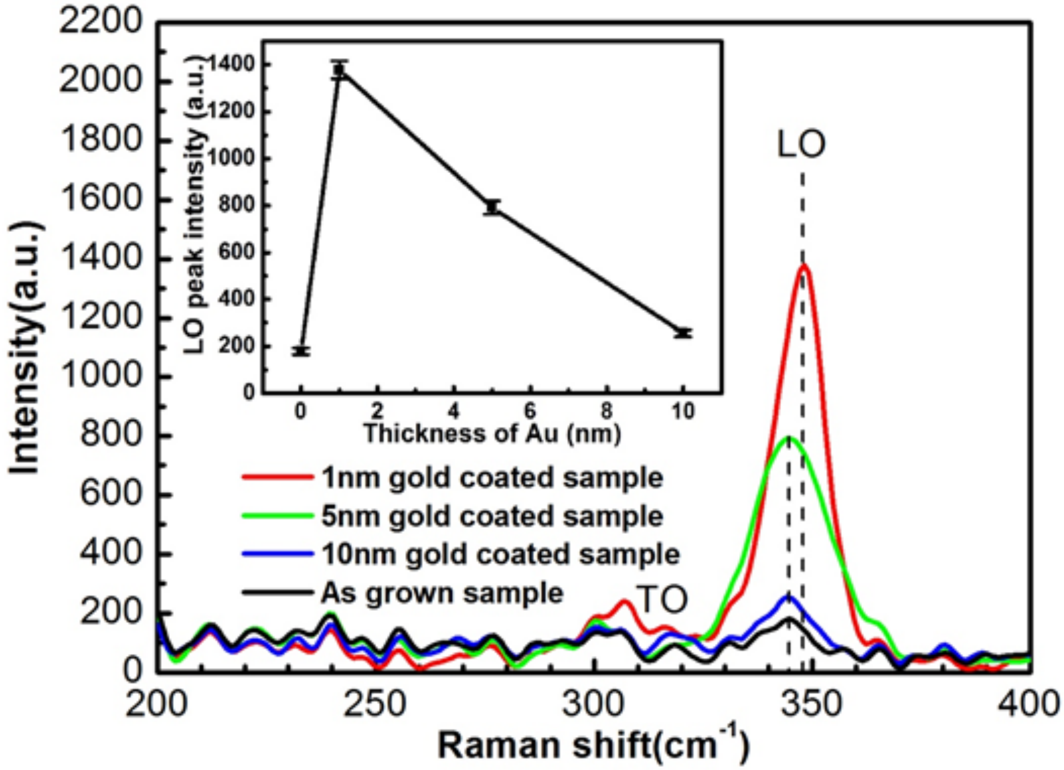


Figure 3.4. Raman spectra plotted in the range of 200cm^{-1} to 400cm^{-1} after the baseline was removed. The inset is peak intensities of the LO mode plotted as a function of nominal thickness of the gold coating.

Since Raman intensities are measured mostly as the product of the incident field density, Raman signal intensities increase as the excitation light intensity increases[59], we invoke the electromagnetic (EM) interaction model to account for the increased LO Raman mode observed for the 1nm and 5nm gold-coated samples in which gold clusters are smaller than those seen on the 10nm gold-coated sample. Gold clusters such as those seen on our InP nanowire networks can increase the inelastic Raman scattering signal by inducing the localized surface plasmon resonance (LSPR) to enhance the electro-magnetic field[60]. The Raman signal can also be locally increased when metallic clusters are closely packed on the nanowire surface, a coherent interference of the enhanced field around each particle will result in increasing the EM field between them[61,62]. In the mean time, fluorescence quenching as a result of light blocking and absorbing by gold clusters also favors the detection of Raman signal by removing the overwhelming part from the fluorescence in the spectra.

In addition to these intensification mechanisms for the 1nm and 5nm samples, a reduction mechanism can be also invoked for the 10nm sample. As seen in Figure 4, the increase of the LO mode signal diminished sharply as the size of the gold clusters increased. As the gold cluster size gets larger, the shape of the gold clusters becomes more ellipsoid and the surface convex shape becomes flatter. As a result, less inelastic scattering occurs on the surface, which will weaken the EM field on the surface and then decrease the Raman intensity[63].

3.4 Conclusions

The gold clusters present on InP nanowire networks were found to increase the Raman signal when the size was within a narrow range of approximately ~27nm diameter. The increase in the Raman signal was discussed by invoking the electromagnetic interaction model in SERS and the reduction mechanism of the flatter surface convex shape. By implementing post-growth deposition of gold followed by a low-temperature annealing step that results in gold clusters with appropriate sizes, Raman spectroscopy can be a powerful material analysis technique for the InP nanowire networks. Understanding the optical properties of the InP nanowire networks grown on silicon by MOCVD is a significant and instructive fundamental study for nanowires grown on different substrates, i.g. copper foils of various applications.

Part II

Semiconductor nanowires grown on metallic substrates with intermediate layers

Chapter 4

Indium phosphide nanowires grown on copper foils with aluminum doped zinc oxide thin films

The growth of indium phosphide (InP) nanowires on transparent conductive aluminum-doped zinc oxide (AZO) thin films on polycrystalline copper (Cu) foils was proposed and demonstrated. AZO thin films and zinc oxide (ZnO) thin films, as comparison, were deposited on Cu foils by radio frequency (RF) magnetron sputtering. Subsequently, InP was grown by metal organic chemical vapor deposition (MOCVD) with gold catalysts. InP nanowire networks formed on the AZO thin films while no InP nanowires grew on the ZnO thin films. Morphological, crystalline, and optical properties of the InP nanowires on AZO thin films were compared with those of InP nanowires grown on silicon (Si) substrates. Zinc diffusion from AZO thin films into InP nanowire networks was suggested as the cause of substantial modifications on the optical properties of the InP nanowires on AZO thin films; red-shift in photoluminescence spectra and a larger relative TO/LO intensity ratio in Raman spectra were observed, in comparison to those of the InP nanowires grown on Si substrates. In this chapter, we proposed and demonstrated a new route to grow semiconductor nanowires on metals that potentially provide low-cost and mechanically flexible substrates and establish a reliable electrical contact by utilizing conductive oxide thin films as a template, which could offer a new material platform for applications such as sensors and thermoelectric devices.

4.1 Introduction

Three material components: metal substrate, template film, and semiconductor nanostructures, are required in this demonstration. Copper (Cu) foil was chosen for a metal substrate because of its maturity as an industrialized material with high thermal and electrical conductivity and relatively low cost. For a template film, conductive metal oxides such as zinc oxide doped with aluminum (AZO) appear to be reasonable choices because they have been widely used as electrodes in various devices and their physical properties are easily tuned by controlling deposition parameters and doping conditions to manipulate stoichiometry and crystallinity[64,65]. We have chosen AZO as a template film due to its high electrical conductivity and relatively low cost in an attempt to take full advantage of the desirable metallic properties of the Cu foil. Indium phosphide (InP) nanowire networks have been formed on various substrates in our previous work[66]; therefore, we have chosen InP nanowire networks as semiconductor nanostructures in this demonstration.

Semiconductor nanowires (e.g. InP nanowires) directly formed on electrically conductive substrates (e.g. Cu) would benefit many potential applications including thermoelectric devices and optical sensors; however epitaxial growth of single-crystal semiconductors on metals has been found nearly impossible because of undesirable reactions that occur between two dissimilar materials. For instance, in our previous attempt of growing InP nanowires on Cu, the formation of Cu_3P prohibited InP nanowire from growing. In this chapter, AZO films were introduced as a barrier layer between InP nanowires and Cu foils By controlling the doping with aluminum, AZO can be a practical thermoelectric (TE) material, in particular, at higher temperatures (≥600K)[67] with a relatively high power factor (0.26W/m•K at 740 K[68]). In addition, semiconductor nanowires are a promising TE material platform with rough surfaces and their small diameters that cause phonon scattering to enhance the figure of merit, ZT[69]. Therefore, InP nanowire networks coupled with conductive AZO films were chosen to form a unique material platform on mechanically flexible Cu substrates to fabricate TE devices at low fabrication and material costs. The combination of these two materials, InP and AZO, would enable a full utilization of a large temperature gradient in designing TE devices for harvesting waste heat from a wide range of applications including residential, industrial (e.g. metal refinery, fossil fuel-based power station), and even solar thermal power generation).

4.2 Experiments

Cu foils were cleaned with acetic acid, rinsed with DI water, and dried in air. Subsequently, ZnO and AZO films with a nominal thickness of ~500nm were deposited on the prepared Cu foils by radio frequency (RF) magnetron sputtering with the following conditions: substrate temperature at 450°C, sputtering pressure of 0.28Pa, RF power of 100W, and sputtering gas of 5N argon, and deposition time of 120 minutes. Sintered ZnO mixed with Al_2O_3 was utilized as a sputtering target for

AZO films while ZnO was used as a sputtering target for ZnO films. Two prepared substrates, referred to as AZO/Cu and ZnO/Cu substrates, were further covered with a gold film with a nominal thickness of 4nm deposited by electron-beam evaporation. As a reference, silicon (Si) (100) substrates were also prepared with a 4nm gold thin film. Finally, InP was deposited on these three types of substrates by MOCVD at chamber pressure of 100Torr and growth temperature of 500°C for 20 minutes. Trimethylindium (TMI) and di-tert-butylphosphine (DTBP) carried by hydrogen (H_2) were utilized as indium and phosphorous precursors with the V/III molar flow rate ratio of ~3:1. A 10-minute “indium bath” (IB) process was implemented during the pre-growth annealing at 500°C to avoid the reaction of phosphine and copper substrates. The indium affluent environment in the chamber introduced by IB was expected to enhance the formation of gold indium (Au-In) alloys as catalysts for InP nucleation and nanowire growth afterwards. Without the IB process, no InP grew on AZO/Cu substrates due to the lack of available indium on the substrate during the early stage of the InP growth and the reaction of phosphine with the substrates.

Field emission scanning electron microscope (FE-SEM, Hitachi S4800) was used to obtain morphological and geometrical characteristics of the samples. Photoluminescence (PL) spectra were collected from the samples at room temperature using a 6.7mW 532nm CW laser with a nominal spot size of ~2mm in diameter. Raman spectroscopy was performed at room temperature by a JY Horiba Raman 800UV spectrometer with a 600 g/mm grating and a 632nm laser excitation source focused through a 100x objective lens with a focal spot of approximately 2μm in diameter. Hitachi H9500 Transmission Electron Microscope (TEM) operating at 300kV was used for structural analysis.

4.3 Results and Discussion

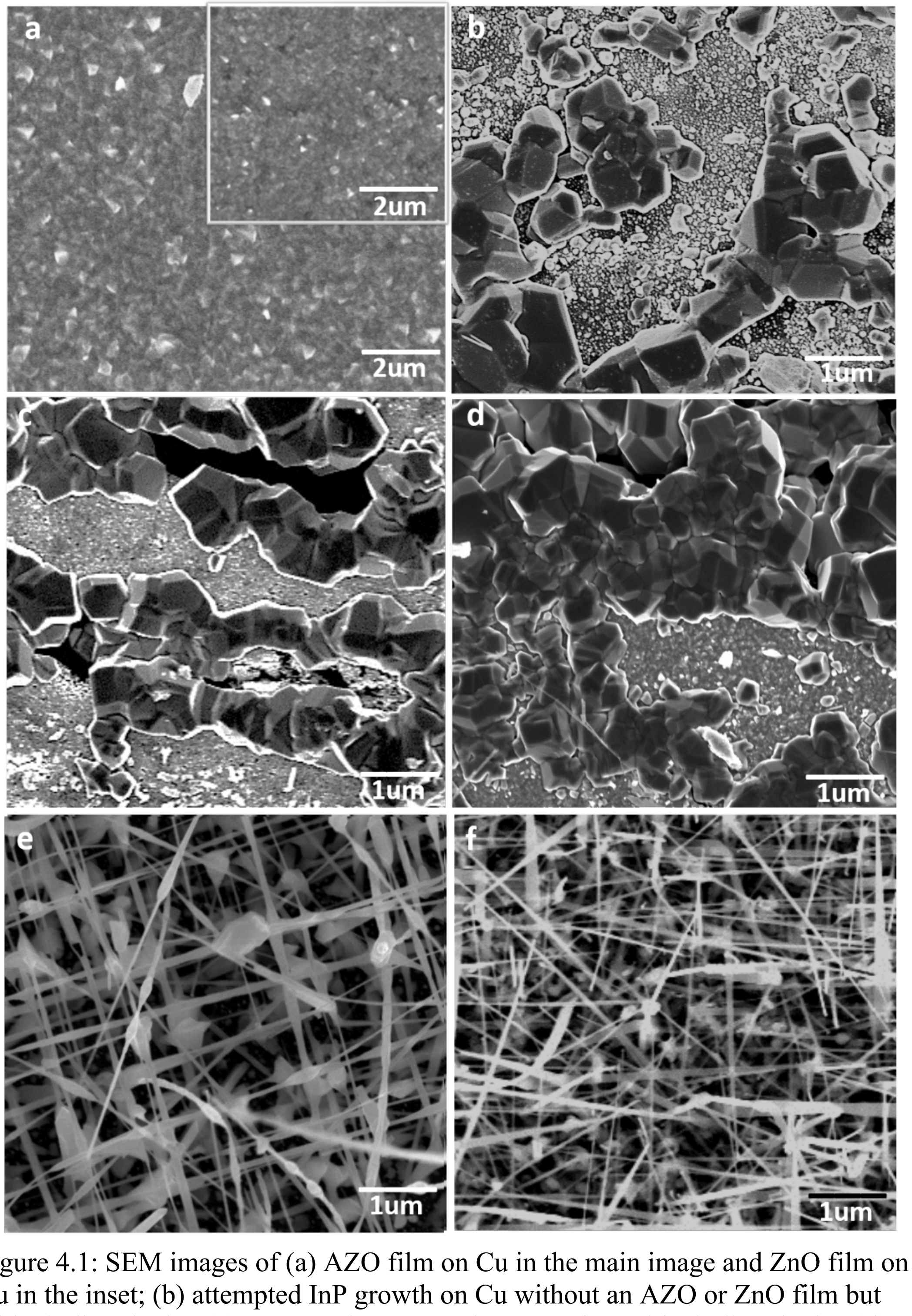


Figure 4.1: SEM images of (a) AZO film on Cu in the main image and ZnO film on Cu in the inset; (b) attempted InP growth on Cu without an AZO or ZnO film but with “indium bath”; (c) attempted InP growth on ZnO/Cu with “indium bath”; (d) attempted InP growth on AZO/Cu without “indium bath”; (e) InP nanowire sample

grown on AZO/Cu with “indium bath”; (f) InP nanowire sample grown on Si substrate.

Plan-view SEM images of the AZO/Cu and ZnO/Cu substrates and InP grown on these two types of substrates as well as on the Si (100) substrate are shown in Figure 4.1. Figure 1a reveals surface morphology of the AZO/Cu substrate. The surface of the AZO/Cu substrate appears to be made of grains with size ranging from 220 to 350nm with average of ~275nm. Shown in the inset is a plan-view SEM image of the ZnO/Cu substrate, indicating that the surface of the ZnO/Cu substrate consists of grains with an average size of ~90nm. The increased grain size of the AZO films than ZnO films can be understood by recognizing the substitutional incorporation of Al^{3+} ions into Zn^{2+} sites and the incorporation of Al ions in the interstitial positions[70]. At the same time, the larger grain size of AZO can be also related to the defects brought by the Al doping and the oxygen deficiency[71]. The increased grain size decreases grain boundary density, behaving as traps for free carriers and barriers for carrier transport. As a result, larger grain size leads to the grain boundary scattering and increase the carrier lifetime, consequently leading to increased electrical conductivity by increasing carrier concentration and Hall mobility[72].

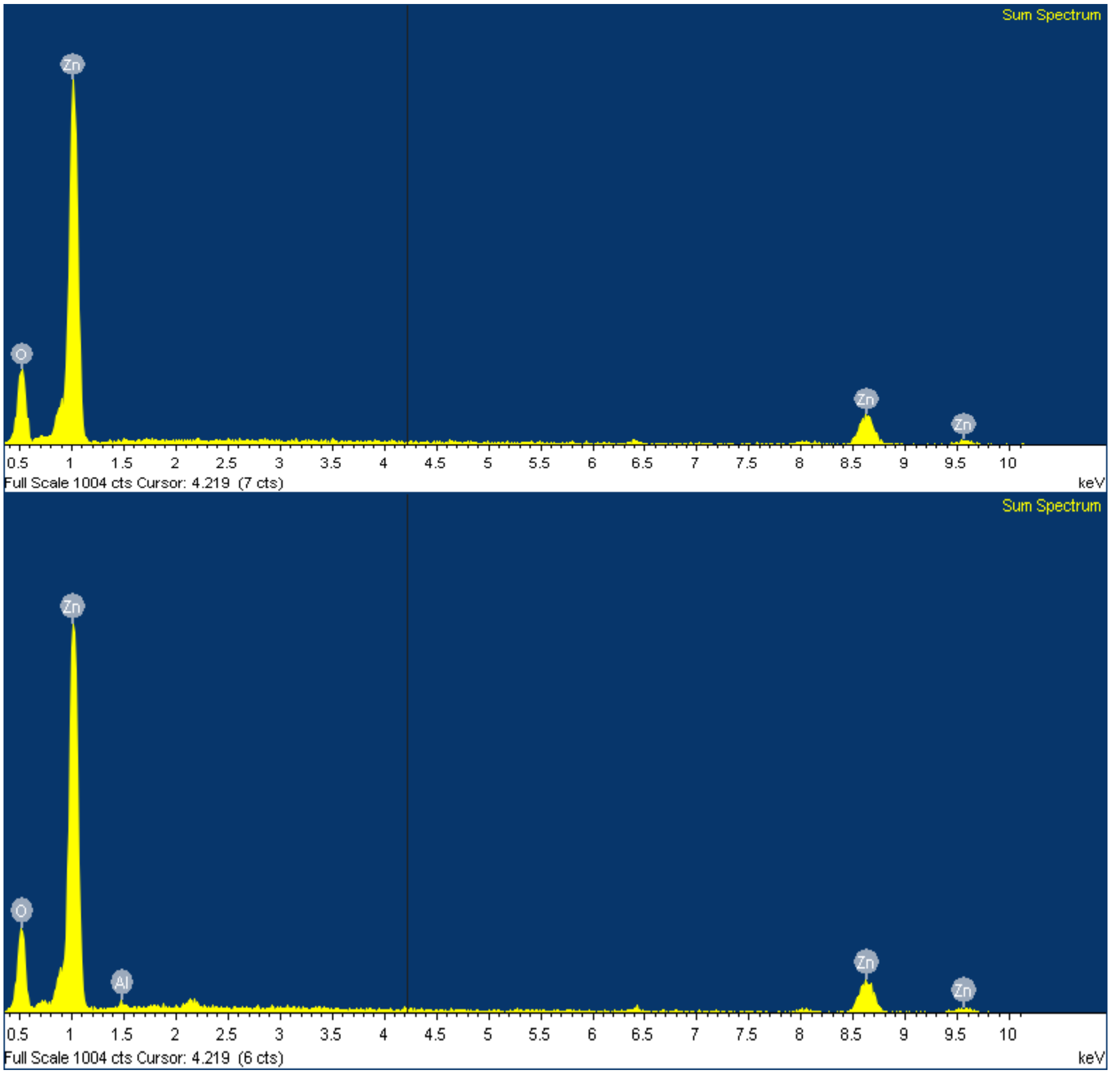


Figure 4.2: Energy-dispersive X-ray spectroscopies of ZnO on Cu (top) and AZO on Cu (bottom).

Energy-dispersive X-ray spectroscopy (EDX) analysis (shown in Figure 4.2) on the top surface of the AZO/Cu substrate indicates that the fraction of aluminum is approximately 1.25 wt%. Figure 4.1b, 1c, 1d are SEM images of attempted InP growth on plain Cu foil, ZnO/Cu with IB, and AZO/Cu without IB, and InP nanowires did not grow on these samples. EDX analysis indicates that the characteristic structures seen in Figure 4.1b, 1c and 1d mainly contain copper phosphide (Cu_3P) rather than InP. As shown in Figure 4.1e, nanowires with an average diameter of ~165nm and diameter ranging from ~100 to 200nm were observed, and intersections were found to form when two or more nanowires crossed in a free space during the growth. Substantial differences in InP growth morphology on the two different substrates, as seen in Figure 4.1c and 4.1e, clearly suggest that the presence of aluminum in AZO contributes to the formation of InP nanowires. In comparison of Figure 4.1d and 4.1e, IB process before the growth played a significant role of assisting InP nanowire growth on AZO/Cu. The "indium bath" (IB) process introduces an indium rich environment in the chamber and, in our understanding, formed In-Au, Al-In and In-Al-Au alloys as reaction catalysts for InP nanowire growth before phosphorous precursor is introduced to the surface of the Cu substrates. Without IB process, the phosphorous precursor would react with Cu substrates through AZO film and form copper phosphide (Cu_3P) on the surface (as seen in Figure 4.1d) which prohibits the indium to form alloys with gold particles, and therefore prevents the InP growth from occurring on AZO/Cu. On the Si substrate, as in Figure 4.1f, InP grew as nanowires with intersections, as usual, ranges from 80 to150nm with the average diameter of ~110nm[73].

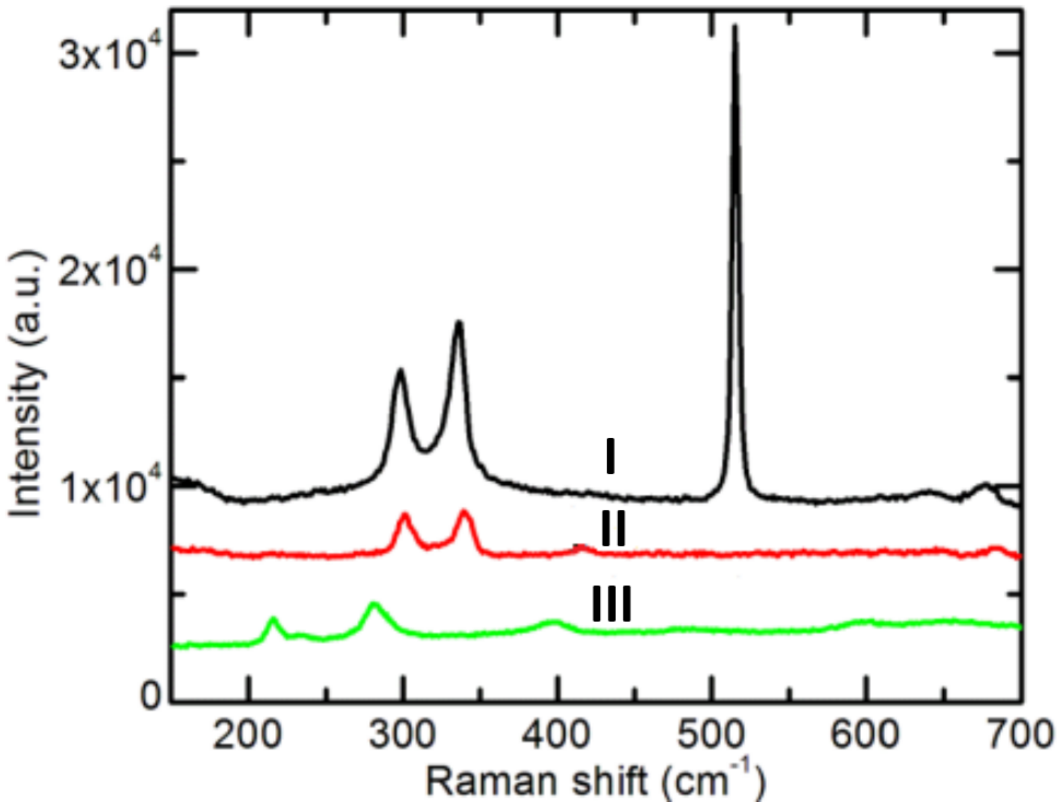


Figure 4.3: Raman spectra collected at 300K from the three samples: I, InP nanowires grown on Si substrate, with obvious LO and TO peak corresponding to bulk InP; II. InP nanowires grown on AZO/Cu also with InP LO and TO peak and with a higher TO/LO intensity ratio comparing to I; III, InP nanowires grown on ZnO/Cu, no InP peaks were found.

Backscattered Raman spectra collected from the three samples are shown in Figure 4.3. Spectrum I (InP nanowires on Si) shows two peaks at ~298 and ~337cm^{-1} which are attributed to the transverse optical phonon (TO) and the longitudinal optical (LO) phonon modes of bulk InP and are associated with respective Brillouin zone center (Γ), and a peak associated with the Si substrate is also seen at ~515 cm^{-1}. Correspondingly, spectrum II (InP nanowires on AZO/Cu) has peaks associated with the TO and LO modes at 301 and 340 cm^{-1}, respectively, showing small (3~4cm^{-1}) shifts with respect to those expected for bulk InP. In addition, the peak intensities of the TO and LO modes are much lower in spectrum II than those of spectrum I, which is likely to be associated with the lower nanowire density on AZO/Cu than that on Si and the lower collection efficiency of Raman scattered light on the nanowires on a curved and wavy Cu foils. Furthermore, the TO/LO peak intensity ratio reveals a noticeable difference between the two spectra; the TO/LO peak intensity ratio of spectrum I is ~0.67 while it is ~0.91 for spectrum II. As a previous research in our group[74], X-ray photoelectric spectroscopy (XPS) indicated that zinc contained in AZO out-diffused into InP nanowires grown on the AZO films. Thus, the two features seen in spectrum II: the shift in the TO and LO phonon mode peaks and the higher TO/LO peak intensity ratio, compared to those in spectrum I, are also attributed to zinc out-diffusion into InP nanowires grown on the AZO/Cu substrates as Zn incorporated in InP nanowires is expected to make the nanowires more ionic and defective. No peak related to InP was found in spectrum III as the surface of the ZnO/Cu substrate was covered with blocks of Cu_3P (two unknown peaks at ~223 and ~285 cm^{-1} appearing in spectrum III could not be identified conclusively.)

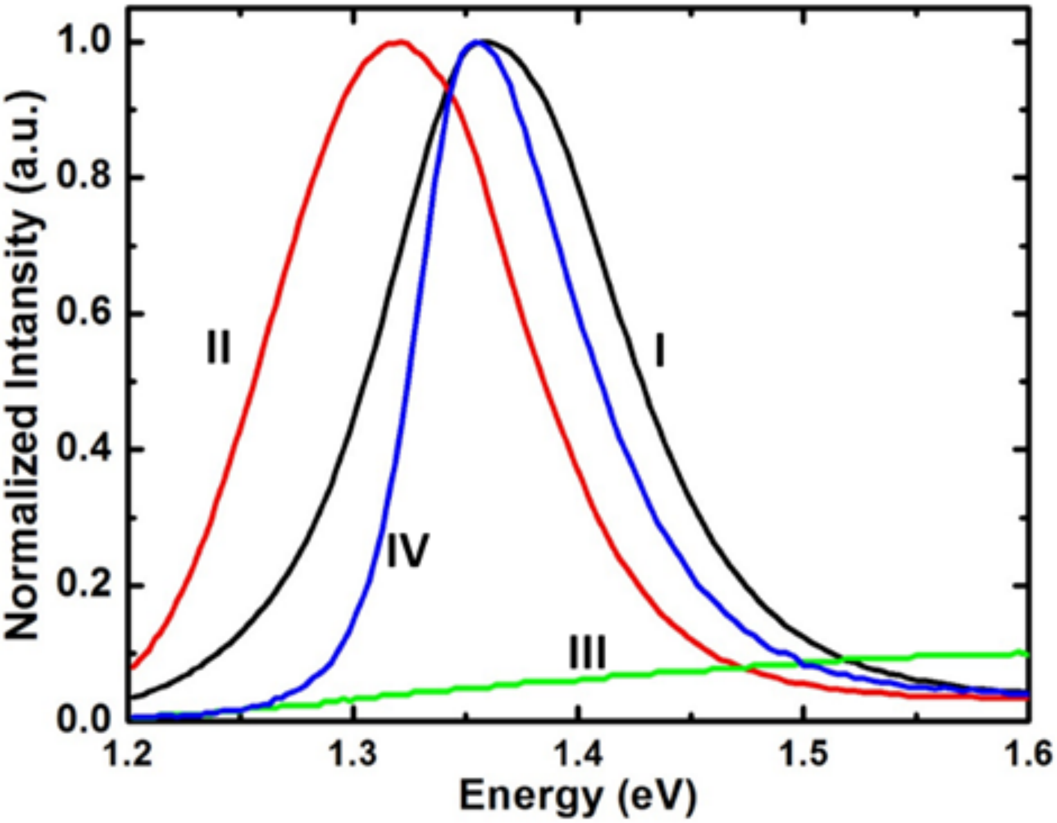


Figure 4.4: Normalized photoluminescence spectra collected at 300K from the samples with the standard photoluminescence of InP nanowires grown on Si substrate: I, InP nanowires grown on Si substrate in the growth chamber with the AZO/Cu and ZnO/Cu substrates showing a peak at 1.357eV; II. InP nanowires grown on AZO/Cu with a peak at 1.321eV; III, samples grow on ZnO/Cu; IV, standard sample of InP nanowires grown on Si substrate in a zinc-free environment with a peak at 1.353eV. The zinc diffusion into InP makes spectra I and II more "symmetric" with a wider FWHM comparing to IV and with higher zinc diffusion concentration, II has an obvious redshift. No peaks were found in spectrum III. The redshift in spectrum II of ~35meV can be a reason of higher Zn diffusion concentration into InP nanowires.

In addition to the zinc out-diffusion from AZO to InP nanowires described above, a trace of zinc was also found in InP nanowires grown on Si substrates[14]. The XPS analysis suggested that zinc from neighboring AZO films that co-existed in the same growth chamber during the nanowire growth diffused into the nanowires, presumably through the growth environment (i.e. vapor phase), even when the nanowires were grown on Si substrates. Therefore, in the following section that describes PL characteristics of the three samples, a PL spectrum of InP nanowires grown on a Si substrate without zinc contaminants in the growth environment is also shown as a reference. Normalized PL spectra of the three samples and the reference sample (i.e. zinc-free InP nanowires on a Si substrate) are shown in Figure 4.4. The peak of spectrum II (i.e. InP nanowires grown on AZO/Cu) at 1.321eV shows a large redshift (~35meV) with respect to the peak of spectrum I (i.e. InP nanowires, with a trace amount of zinc, grown on Si substrate) at 1.357eV and of spectrum IV (i.e. the reference zinc-free InP nanowires grown on Si) at 1.353eV. This redshift would further suggest, in addition to the distinguishable features seen in the Raman spectrum in Figure 4.4, the presence of zinc (i.e. acceptors) in the InP nanowires grown on AZO/Cu, which would cause the bandgap to decrease due to a large amount of ionized impurities[75]. Full-width-at-half-maximum (FWHM) of spectra I and II are broader than that of spectrum IV, which could be attributed to local potential fluctuations induced by random distributions of the out-diffused zinc present in the InP nanowires on AZO/Cu[76,77]. Spectrum IV collected from the reference zinc-free InP nanowires grown on Si shows conventional asymmetric appearance with a steep cut-off on the low-energy side and an extended slope on the high-energy side[78,79]. The asymmetric appearance indicates that the low-energy side is well-defined by the band-edges, while the high-energy side is broadened due to the thermal excitation of carriers[80]. In contrast, for spectra I and II collected on the InP nanowires containing zinc, the low-energy side lacks a sharp cut-off presumably due to the band-tailing added to the valence band edge caused by zinc impurities which allowed the emission of photons with energy smaller than that of the band edge recombination, making spectrum I and II appear more symmetric than spectrum IV. Spectrum III shows no PL emission, which is consistent with the SEM and Raman results.

As suggested in Figures 4.1b and 4.1c, the presence of aluminum in AZO/Cu substrates is responsible, at least partly, for the different InP growth mechanisms on the two types of substrates (i.e. AZO/Cu and ZnO/Cu). Apart from inherent differences between these two types of substrates, we also noticed that implementing the IB process described earlier is necessary even on AZO/Cu substrates to induce the growth of InP nanowires. Therefore, based on our systematic and comparative studies on growing InP nanowires on Cu with/without AZO films and with/without the IB process, we concluded that AZO serves as a blocking film that prevents the reaction between phosphine and Cu substrates to form Cu_3P seen in Figure 1c. Concomitantly, the characteristic surface morphology on the AZO films that consists of crystallites with size ~275nm much larger than those with size ~90nm observed on the ZnO surface could act as templates that provides more effective nucleation sites for InP nanowire growth[81]. InP nanowire growth follows the catalyst-mediated vapor–liquid–solid (VLS) process. The VLS catalyst system works with Au particles absorbing In in vapor phase, which forms In/Au alloy above the eutectic point in liquid phase. Continued feeding of vapor In into the liquid alloy causes oversaturation of the alloy, and the reaction of oversaturated In with P precipitates out as InP in form of nanowires, with the Au staying on the tip of InP nanowires[82]. Mattila and coworkers reported the In(As)P nanowire growth on SiO_2 films on Si substrates, where indium droplets could penetrate into SiO_2 films and form In-Si interfaces that assist the nanowire growth[83]. Similarly, in our case, besides Au catalysts, Al could also act as a catalyst for InP growth with the penetration of indium into AZO film from the AZO/Cu sample. Based on the phase diagram, Al/In system forms liquid with FCC Al at the growth temperature of 500°C. With indium precipitated at the Al/In liquid/solid interface, liquid Al/In alloy could oversaturate and precipitate In out to react with P, resulting in nucleation and nanowire growth of InP. While, the phase diagram of In/Zn eutectic system indicates a eutectic temperature of 150°C with ~5% Zn in the alloy. At 500°C, In/Zn system is completely in liquid phase and it can hardly oversaturate with flowing of In, which results in Zn from ZnO cannot mediate the InP nanowire growth on ZnO/Cu sample. The fact that the AZO surface consists of crystallites much larger than those seen on the ZnO surface could be largely associated with the incorporation of Al[84]. Furthermore, AZO normally has thermal stability better than that of ZnO, especially at low pressure and high temperature,[85] which is the similar environment established during the MOCVD growth; thus, thermally less stable ZnO would not provide an effective barrier against phosphine reaching Cu foils, allowing Cu_3P to form, which suppresses the formation of InP nanowires. Further study is required to provide conclusive understanding on the role of an AZO film in the growth of InP nanowires on AZO/Cu.

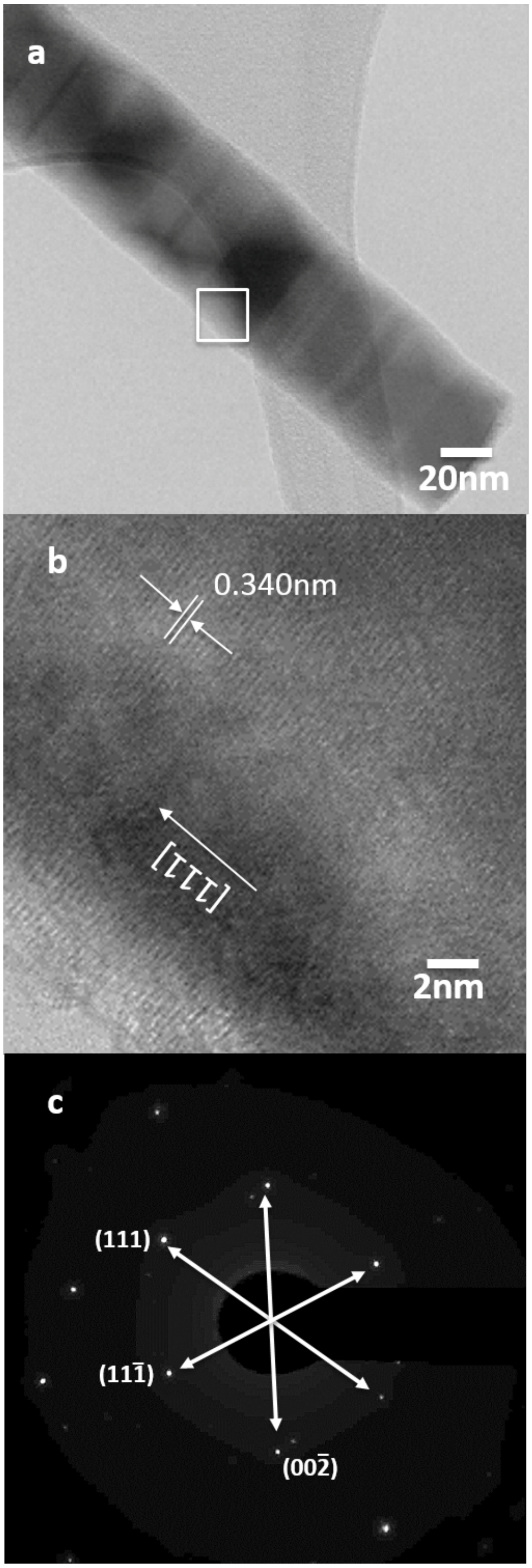

a
20nm
b
0.340nm
[111]
2nm
c
(111)
(11$\bar{1}$)
(00$\bar{2}$)

Figure 4.5: (a) TEM images of a single InP nanowire grown on AZO/Cu. Gray stripes and black stripes are two different orientations of ZB segments due to the rotational twinning; (b) Magnified TEM image of the square area from (a), indicating InP nanowire grown along [111] direction with plane spacing of 0.340 nm; (c) SAD pattern of the InP nanowire shown in (b).

Bright field TEM images of a representative InP nanowire grown on AZO/Cu are exhibited in Figure 4.5. The nanowire reveals multiple sections with varying contrast and various diameters along the nanowire's growth direction as seen in Figure 4.5a. The series of streaks indicate the presence of twinning in zinc blende (ZB) crystal structure of InP, which is regarded as the insertion of multiple stacking faults associated with wurtzite (WZ) crystal structure[86,87]. The rotational twinning occurring during the growth of a (111) plane of the ZB crystal results in WZ structure,[88] which leads to the coexistence of both ZB and WZ crystal structures within the single InP nanowire. Figure 4.5b, collected at higher magnification, depicts atomistic details of the InP nanowire, clearly showing lattice fringes along the [111] growth direction with plane spacing of 0.340nm. According to JCPDS (card No. 50642) data, the corresponding planes are indexed as the (111) planes of zinc blende InP. The selective area diffraction (SAD) analysis based on Figure 4.5b is shown in Figure 4.5c with a zone axis of [110] f.c.c. The lattice constants along InP [111] and the overall crystallographic symmetry indicate that the InP nanowire grown on AZO/Cu is single-crystal.

1.1 Conclusion

A film of AZO prepared on Cu foils was found to provide a template for the growth of InP nanowires while a film of ZnO prepared on Cu foils did not yield nanowires. Based on the microscopic characteristics of the InP nanowires on AZO/Cu, we found that the InP nanowires were single-crystal and grew along f.c.c. [111]. The optical properties observed in Raman and PL were found to be modified by the zinc out-diffusion from AZO into InP nanowires, in comparison to those of the InP nanowires grown on Si. We have proposed and demonstrated the material system; single-crystal semiconductor nanowires grown on a transparent conductive oxide film prepared on a mechanically flexible metallic substrate would offer a unique material platform for such devices as thermoelectric devices in which both electrical and heat transport through electrodes and semiconductor govern overall device performance.

Chapter 5

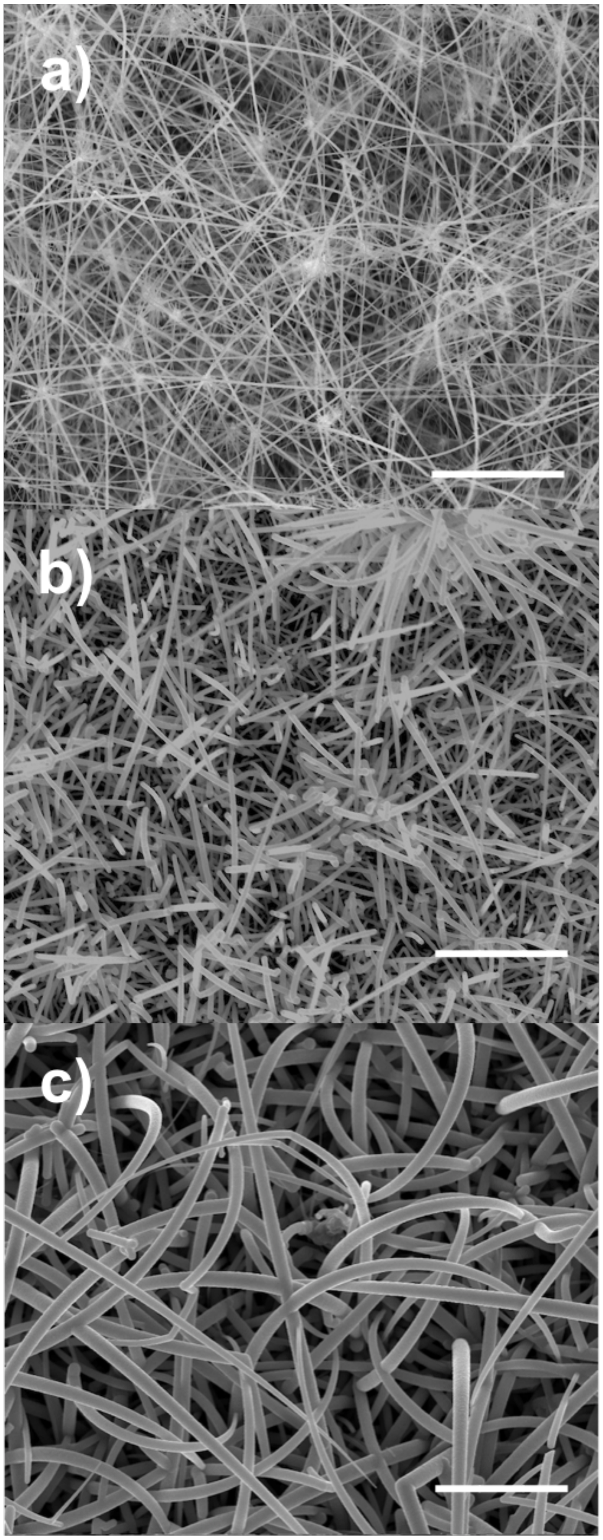
Silicon Nanowire-Thin Film Coupled Architecture on Copper with Titanium Nitride Barrier Layer for Flexible Thermoelectric Modules

A unique material platform in which a doped semiconductor thin film (two-dimensional material) is coupled with semiconductor nanowires (one-dimensional material) that form three-dimensional networks grown on a mechanically flexible metallic substrate was designed and demonstrated. Silicon (Si) nanowire networks were grown by plasma enhanced chemical vapor deposition (PECVD) on mechanically flexible copper (Cu) substrates (e.g. copper foils). A thin film titanium nitride (TiN) barrier layer was introduced to assist the nanowire growth on Cu foils. Subsequently, a Si top layer was grown on the nanowire networks to form a poly Si film providing a nearly continuous surface. Morphological and structural properties of the unique material system were studied by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). The thermoelectric (TE) properties of current-voltage curves, Seebeck coefficient and electrical conductivities of p-type doped Si TE modules at various temperature gradients were obtained. A maximum power generation of ~7nW at 65K temperature gradient is presented.

5.1 Background

Single-crystal semiconductor nanowires directly formed on metallic substrates would offer scalable and cost-effective material platforms for a variety of devices which require both high-performance electrodes and the novel properties of semiconductor nanostructures, e.g. TE devices.

To achieve practical and scalable TE modules based on semiconductor nanowires, a unique material platform of a doped semiconductor thin film with semiconductor nanowire networks grown on mechanically flexible metallic substrates was demonstrated. Advantages of our module architecture include its large area, mechanical flexibility, and vertical stacking potential. To demonstrate the viability of this design for flexible applications, our samples utilize Si nanowire networks grown on copper (Cu) foils. Copper foils were chosen as the substrate because Cu has physical properties (e.g. high electrical and thermal conductivities, relatively low cost, and mechanical flexibility) highly suitable for TE applications. Roll-to-roll (R2R) processes, for example, can be employed for large area TE devices at low-cost with the flexible Cu foils. Cu foils are also preferred due to their non-single crystalline characteristics, leading to randomly oriented nanowires that form a three-dimensional nanowire network and create a semi-continuous substrate to support an additional film (i.e. top layer). Such a top layer attached to a bundle of randomly oriented nanowires provides a good electrical contact to the nanowires. However, growing Si nanowires directly on Cu foil was not achieved in research before due to two reasons: 1) the high reactivity of Cu foils with gold (Au) catalysts for Si nanowire growth; 2) the Si precursor of silane (SiH_4) or disilane (Si_2H_6) reaction with the Cu foil to form copper silicide (Cu_5Si)[89]. Therefore, stainless steel has been used as the metallic substrate for Si nanowire growth for most of the previous work in this field[13]. A thin film titanium nitride (TiN) barrier was introduced to prevent the undesired reactivity and to assist the Si nanowire growth on Cu foils.


a)
b)
c)

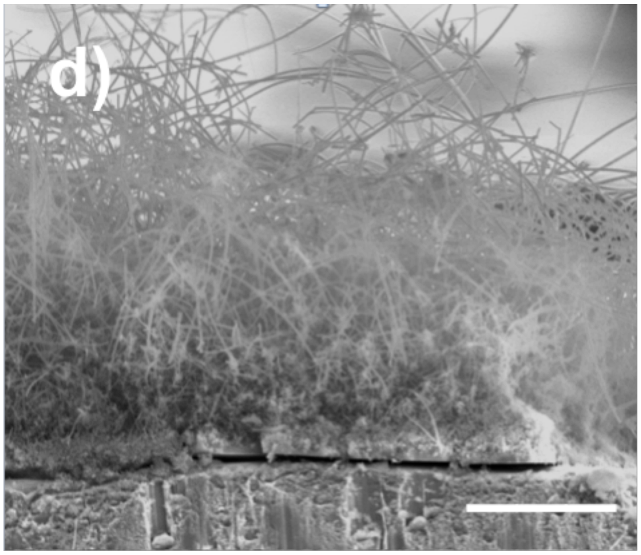


Figure 5.1 SEM images of Si nanowire networks grown on Cu foils: a) plan view of intrinsic Si nanowires; b) plan view of n-type doped (Sb doped) Si nanowires c) plan view of p-type doped (B doped) Si nanowires; d) cross session view of p-type doped Si nanowires. The scale bar represents 10μm for a), b) and c) and 50μm for d).

With the assistance of TiN thin films, three types of Si nanowires grown on Cu foils: intrinsic, n-type antimony (Sb) doped and p-type boron (B) doped are exhibited in Figures 5.1 a), b) and c), respectively. As shown in Figure 5.1 d), the p-type doped Si nanowires have length larger than 50 μm.

In this chapter, we assess the characteristics of TE devices built on a p-type Si nanowire network covered with a p-type Si thin film deposited on a Cu foil at different temperature gradients.

5.2 Experiments

The TE devices studied in this chapter were fabricated in the following processes. Cu foils with area of 2cm×2cm were cleaned with acetic acid, acetone, methanol, and DI water then dried in air. Subsequently, a TiN film with nominal thickness of 40nm was deposited on the prepared Cu foils by atomic layer deposition (ALD) with an inductively coupled plasma source at 300°C. Nitrogen (N_2) plasma and titanium tetrachloride ($TiCl_4$) carried by N_2 were introduced as the nitrogen and titanium precursors, respectively for the TiN film. A 4nm thick Au film, as catalyst, was deposited by e-beam evaporation on the TiN film, as well as on a prepared Cu foil substrate without TiN film as a growth reference substrate.

P-type Si nanowires were attempted to grow on three prepared substrates (two with TiN thin films and one without) by PECVD at 500°C with chamber pressure of 0.3 Torr for 15 minutes. A disilane (Si_2H_6) diluted with hydrogen (H_2) and diborane (B_2H_6) were used as precursor and p-type dopant with flow rates of 10sccm and 0.01sccm, respectively. After the growth of Si nanowires, the growth chamber was evacuated and cooled down to 50°C in argon for 60 minutes. Subsequently, two of the three samples (one with TiN and one without) were taken out of the chamber and a p-type Si layer was deposited with the same precursor and dopant conditions but at temperature of 400°C for 10 minutes on the remaining sample in the chamber. The sample without TiN layer and the one without p-type Si top layer were referred as growth reference sample and TE reference sample, respectively. The sample of Si nanowires grown on TiN/Cu substrate with a Si top layer is the designed sample.

Field emission scanning electron microscope (FE-SEM) (Hitachi S4800) was used to obtain morphological and geometrical characteristics of the two samples, i.e. the designed sample and the growth reference sample. Transmission electron microscope (TEM) (Hitachi H9500) operating at 300kV was utilized for structural analysis. The TE properties of the reference TE sample and the designed sample were studied using a home-built TE measurement system. Cu foils were attached on the surface of the samples as the top contact. Pressure was consistently applied to the measurement to ensure electrical and thermal contact. Heat was supplied by a resistive joule heater to the top side of the device while a heat sink removed heat from the bottom side to maintain a constant temperature gradient. The tested devices were placed between two Cu plates with embedded thermocouples and electrical wires to form a thermally and electrically conductive device. Current–voltage (I-V) measurements were collected at different temperatures by an HP 4155A Semiconductor Parameter Analyzer in the same direction of heat flow, i.e. parallel to the surface normal of the Cu foil. The interface between the top Cu contact and the Si top layer was found to have large electrical resistance, therefore, the thermal conductivity across the device was not measured in this study, and as a result, the *ZT* was not obtained. The electrical conductivity, Seebeck coefficient, and power factor were measured, calculated and discussed in this study.

5.3 Results

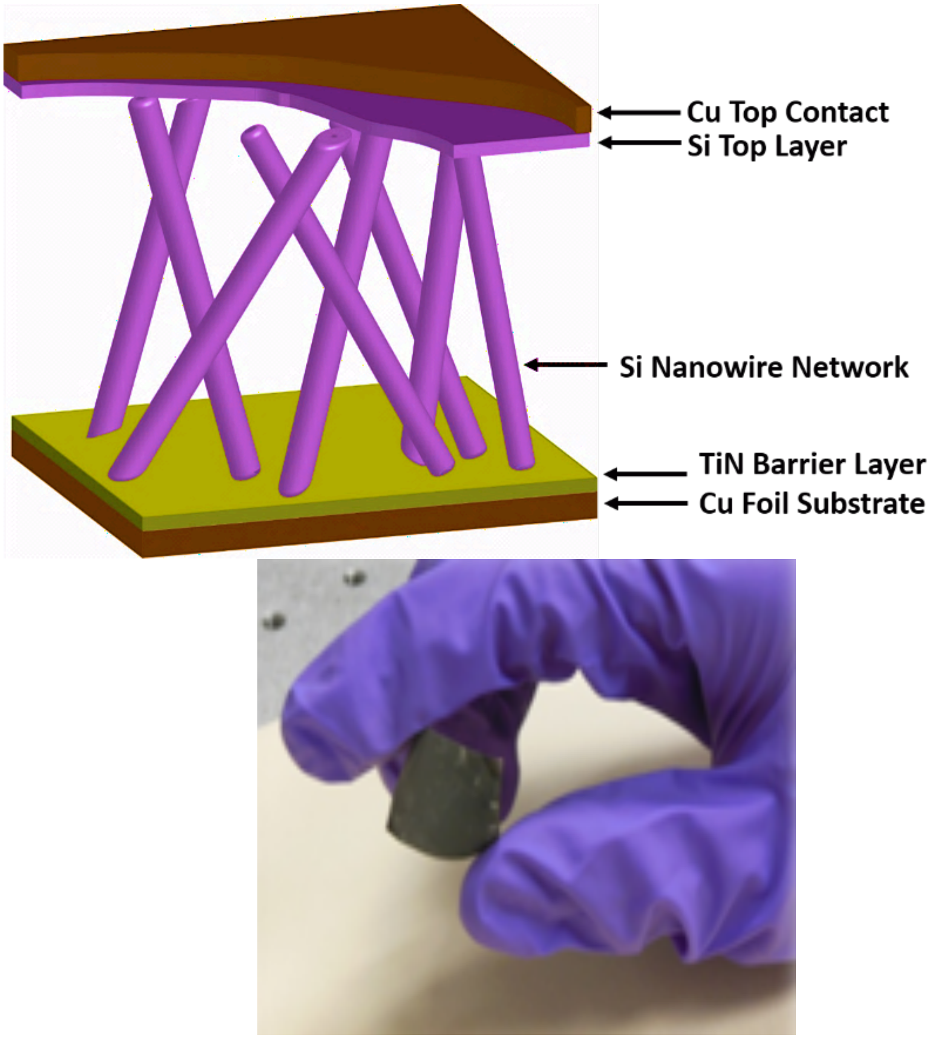


Figure 5.2: a) Schematic of the device design (up). The structure from bottom to top is Cu substrate, TiN barrier, Si nanowire networks, Si top layer and Cu top contact; b) photograph of the device of Si nanowire networks with a Si top layer before addition of Cu top contact (down). The device has an area of 2cm×2cm and good flexibility.

The designed TE device structure is exhibited in Figure 5.2a): flexible Cu foil substrate /TiN barrier layer /Si nanowire network /Si top layer /Cu top contact. Figure 5.2b) shows a photograph of the designed sample, without the Cu top contact, exhibiting its mechanical flexibility. The color of the exposed Si top layer appears to be black as it has a rough surface and the film scatters and absorbs light[90,91].

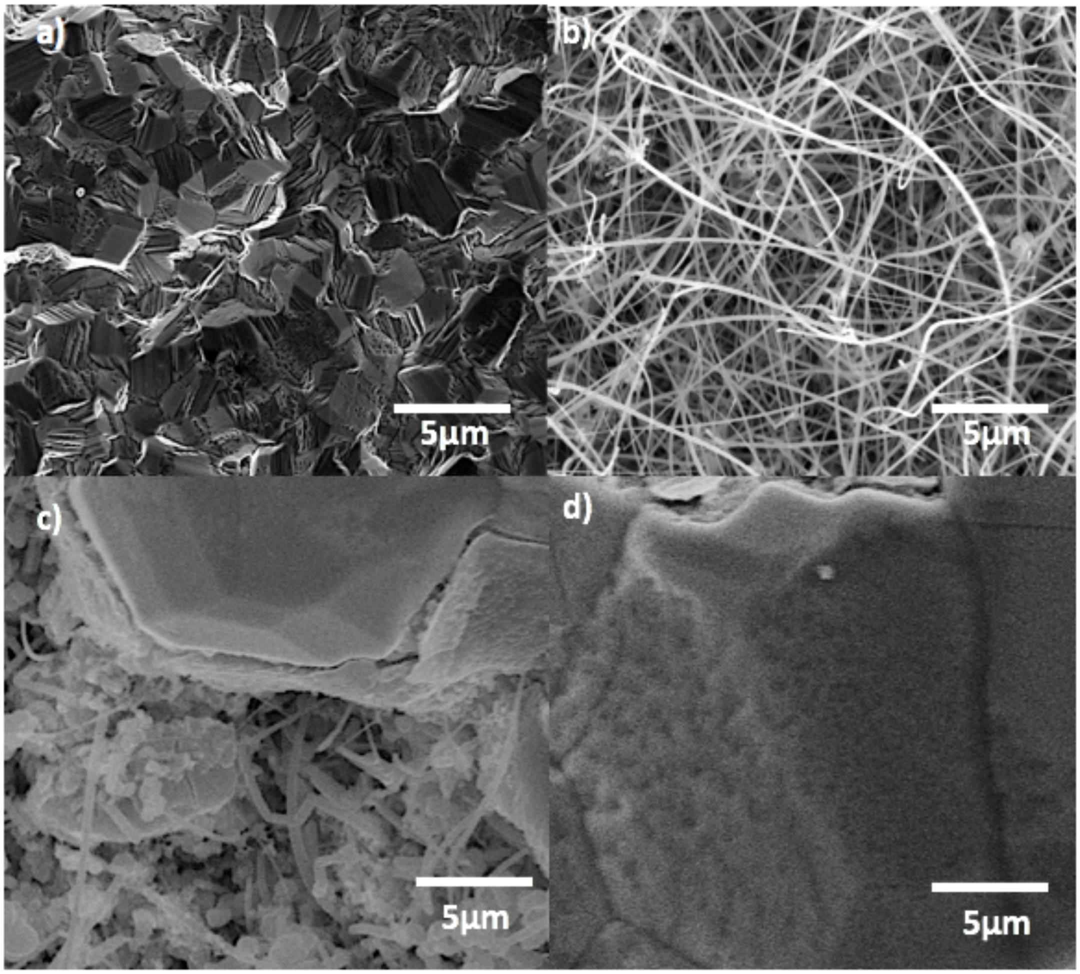


Figure 5.3: SEM images of a) the sample without the TiN barrier layer after Si nanowire growth; b) top view of Si nanowire networks with the TiN barrier layer but without the Si thin film top layer; c) the designed sample of Si nanowires with partial coverage by the Si top layer; d) the top view of the Si nanowire networks fully covered by the Si top layer. The diameters of nanowires after Si top layer deposition in c) were observed larger than the ones before, shown in b).

Shown in Figure 5.3a) is a SEM image of the surface of the reference sample (i.e. the sample without a TiN barrier layer). No Si nanowires were observed but only blocks of Cu_5Si. By contrast, as exhibited in the representative SEM micrograph of Figure 5.3b), with assistance of the TiN barrier layer, Si nanowires with diameters ranging from 100 to 500 nm were observed with a high density, and the average length is ~50μm.The random orientations are due to growth on the non-single crystalline TiN/Cu substrate. Intersections were found to form networks when two or more nanowires crossed in free space during the growth. This geometry allows heat and charge to be transported longer distances than the constituent nanowires alone. The nanowire networks have a large amount of intersections, and phonon waves could potentially experience deformation potential associated with the distortion in atomic arrangement at the intersection. This could result in decreased lattice thermal conductivity at the intersection while electron waves can experience a finite reflection at a potential barrier created by a different environment at the fused portion[92], leading to an improvement in the thermoelectric properties of the nanowire networks by increasing ZT[93]. Figure 5.3c) displays a plan-view SEM image of the surface of the Si nanowire network partially covered with a Si top layer. The diameters of nanowires in Figure 5.3c) were observed larger than the ones shown in Figure 5.3b), which indicates surface coating on nanowires happened while the top layer was deposited on the surface of nanowires. Figures 5.3d) shows the plan-view of the Si top layer fully covering the Si nanowire surface.

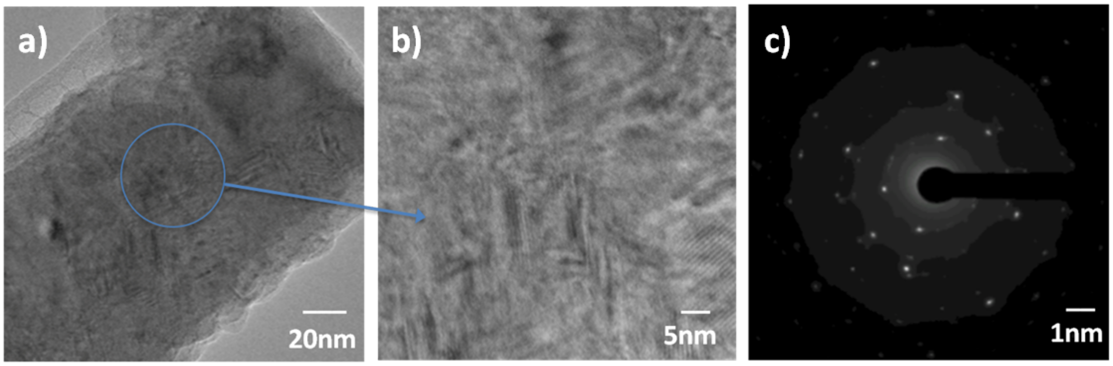


Figure 5.4: Bright field TEM micrograph with corresponding indexed selective area diffraction (SAD): a) Lower magnification bright field image of one Si nanowire, b) Higher magnification bright field image of associated selected area c) SAD pattern of the Si nanowire shown in a) and b).

Figure 5.4a) and 5.4b) illustrate the bright field TEM micrographs of the internal structure of a segment from a representative as-prepared Si nanowire of the designed sample. A core-shell structure with core diameter of ~130nm and a shell thickness of ~15nm and substantial surface roughness with magnitude of ~5nm appears in Figure 5.4a, which can be explained by the Si coating on the nanowires during the top layer deposition. As displayed in Figure 5.4b), multiple lattice fringes can be observed within the field of view. The corresponding SAD pattern from the Si nanowire exhibited in Figure 5.4c consists of scattered spotty and faint ring patterns, which indicate a monocrystalline portion and a polycrystalline portion within the nanowire due to the core and shell structure. The core was found to be single crystal and oriented in the f.c.c. [111] direction.

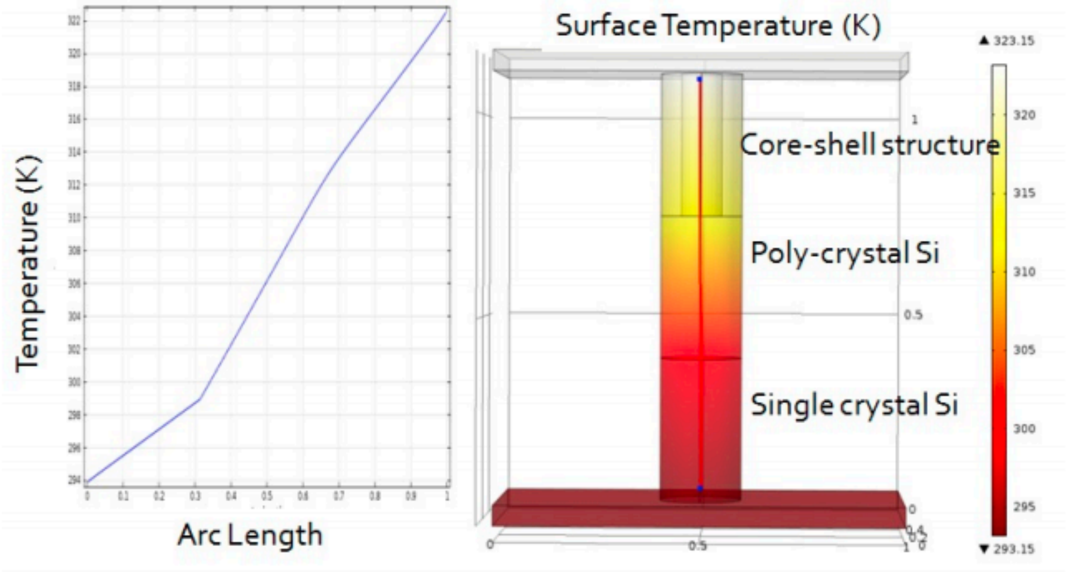
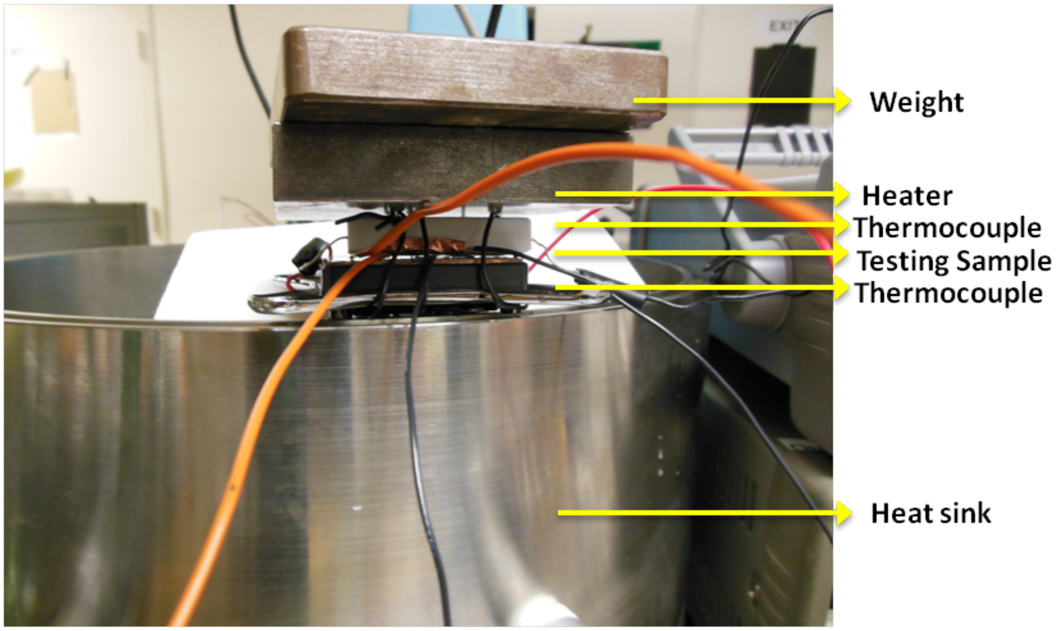


Figure 5.5: Finite element analysis of three segments of different structures. A large thermal gradient was shown across a polycrystalline segment indicating low thermal conductivity, and small thermal gradient across a single crystalline segment indicating high thermal conductivity, and another large thermal gradient across a silicon segment with the core-shell structure seen in TEM image of the sample of interest indicating a low thermal conductivity.

Finite element analysis was preformed to gauge whether the single-poly-crystalline core-shell nanowires would exhibit physical properties advantageous to thermoelectrics[94]. Figure 5.5 shows temperature plotted along a hypothetical nanowire composed of three segments for a given temperature difference. The top segment is made of the single-poly-crystalline core-shell structure described above. A Si nanowire with a single crystalline core and a poly-crystalline shell parallel to the temperature gradient that is dropped along that segment, with a core of 50nm and a total diameter of 100nm. The middle section is made of poly-crystalline Si with a thermal gradient of 42.42°C/μm, and the bottom segment is made of single-crystalline Si with a thermal gradient of 15.15°C/μm. The specific temperature gradient across a segment is related to thermal conductivity of the segment. The single-crystalline segment has the smallest gradient among the three, which indicates that the segment has the largest thermal conductivity, as expected. As seen, the single-poly-crystalline core-shell segment shows a larger gradient than that of the single-crystalline segment, indicating a reduction in thermal conductivity. This analysis was also performed in the opposite order (i.e., the single-poly-crystalline core-shell segment was connected to the low-temperature side) to confirm that the result was intrinsic and not associated with the geometrically asymmetric structure of the hypothetical nanowire.



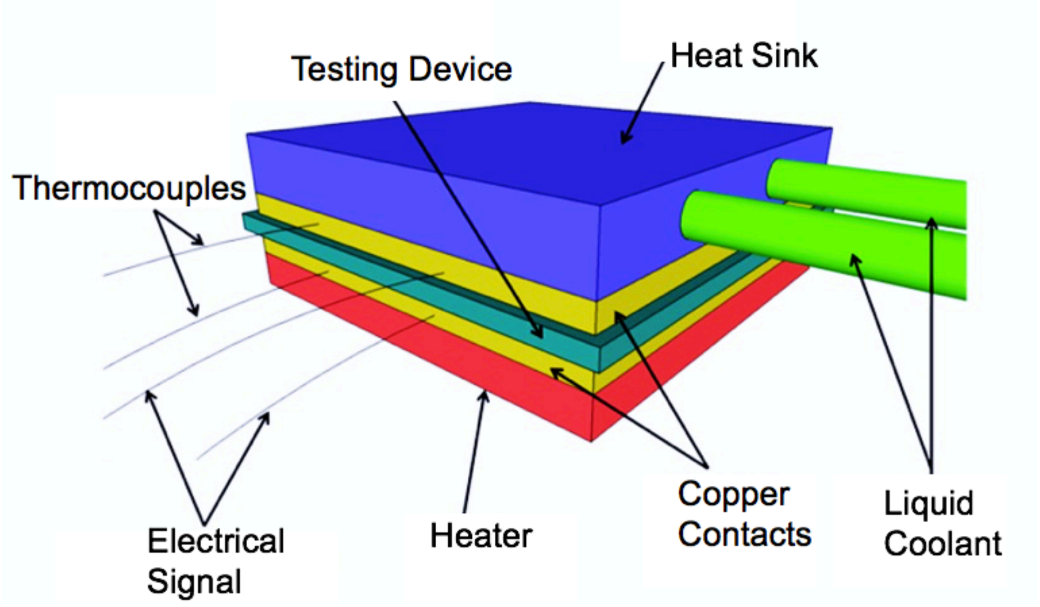


Figure 5.6: Photograph (up) and schematic (down) of nanowire thermoelectric device characterization system.

Both designed sample and reference TE sample were measured by the home-built thermoelectric measurement system shown in Figure 5.6. The reference TE sample with the Cu top contact directly attached on the Si nanowire network did not generate power because of electrical shorting between the Cu top contact and the TiN/Cu substrate. In contrast, the designed TE devices functioned and generated electrical power when a temperature gradient was provided, suggesting the significance of the Si top layer for this TE device.

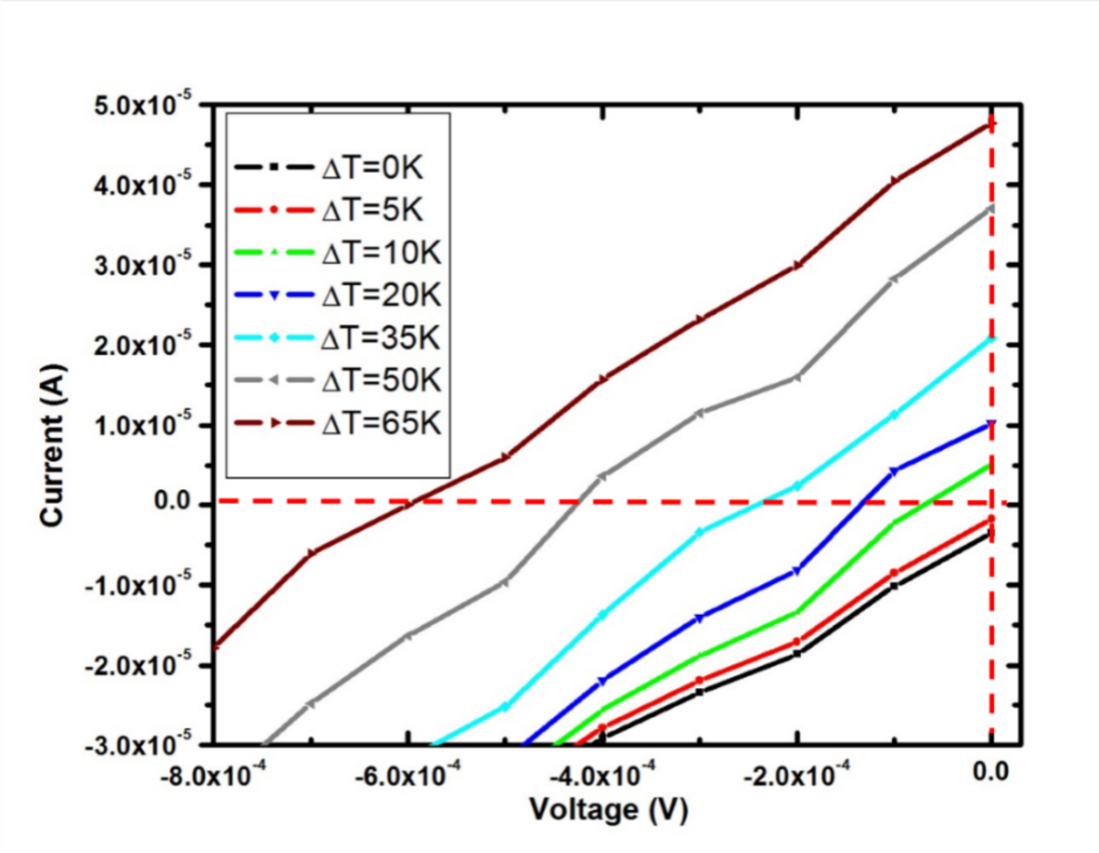


Figure 5.7: Current versus voltage curves with different temperature gradients at 0K, 5K, 10K, 20K, 35K, 50K, and 65K.

The I-V curves collected with various temperature gradients(ΔT) are exhibited in Figure 5.7. Current is produced across the device from the hot side to the cold side due to the thermally activated majority carrier (i.e. hole) diffusion. As the temperature gradient increases, both open circuit voltage (V_{OC}) and short circuit current (I_{SC}) increase, indicating that the electrical power generation increases accordingly.

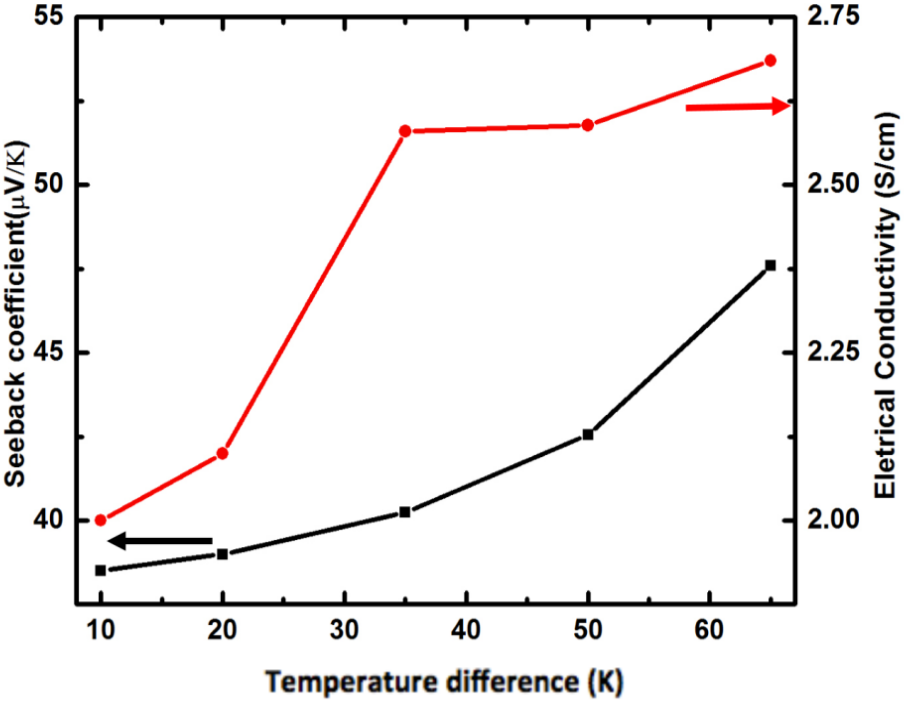


Figure 5.8: Seebeck coefficient and electrical conductivity versus temperature gradients of 10K, 20K, 35K, 50K, and 65K.

The dependence of Seebeck coefficient (S) and electrical conductivity (σ) on T is shown in Figure 5.8. Both Seebeck coefficient and electrical conductivity increase as the temperature gradient increases. At the temperature gradient of 65K, S and σ are 47.6 μV/K and 2.685 S/cm, respectively, and therefore, the power factor σS^2 is 6.08×10^{-9}W/K^{2}cm. The obtained Seebeck coefficient is consistent with those reported for p-type Si materials[95].

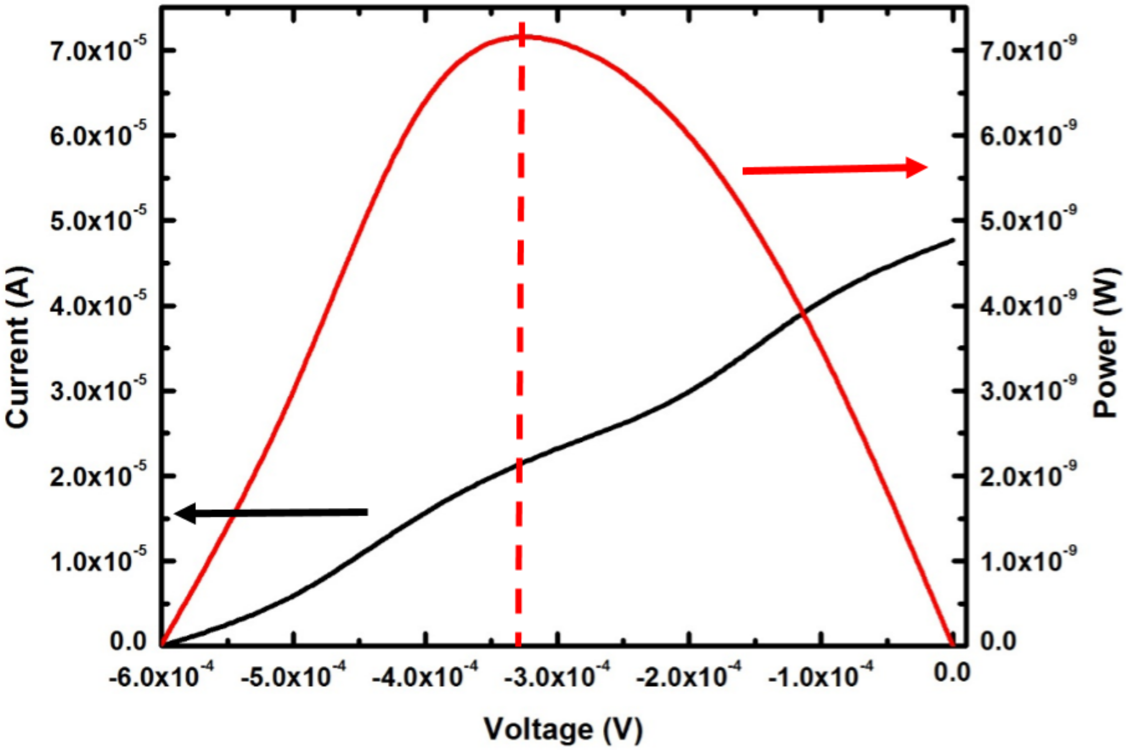


Figure 5.9: Current and generated power versus voltage are shown with the sample at a gradient of 65K across the device. The maximum generated power is ~7nW, which is indicated by the vertical dashed red line.

The current and power generation versus voltage at ΔT of 65K are plotted in Figure 5.9. The approximately linear I-V curve shows relatively low resistance of ~0.09 Ω and the power curve is nearly symmetrical with respect to the midpoint of the swept voltage range. The maximum power generation reaches ~7nW for ΔT=65K, with a normalized power of 1.1×10^{-10} W/K. The power generation presents an inexpensive and environment-friendly method to achieve electrical power generation through a new material platform. The Si top layer provides a doped semiconductor surface for the top electrode of Cu foil with a larger surface area and prevents electrical shorting. Additionally, the other attributes, i.e. mechanical flexibility and resulting scalability given in this three-dimensional TE devices, present a viable option for specific device applications for heat sources with an unusual shape and a large area. Meanwhile, different material doping conditions can be introduced to the nanowire and top layer structure to optimize the TE device by utilizing specific materials at different appropriate operation temperature ranges to enable to apply a large temperature gradient over the device properly.

The major source of the large electrical resistance that adversely affected the TE characteristics was identified as the interface between the top Cu contact and the Si top layer. Deposition of metallic electrode (for example, aluminum) thin films on the Si top layer to form Ohmic contact with Si will be studied for future research in order to properly demonstrate our novel nanowire/thin film device architecture for large area flexible TE power generation.

5.4 Conclusions

A unique material platform of Si nanowire networks grown on Cu foils was employed for the demonstration of flexible TE devices. A barrier layer of TiN was introduced to prevent reactions of Au catalyst and Si precursor with Cu, therefore enabled the growth of Si nanowires indirectly on Cu foil substrates. A Si top layer grown on the nanowire networks was used to prevent the TE devices from electrically shorting. I-V curves collected at various ΔT showed electrical power generation with a maximum power generation of ~7nW at ΔT=65K, while the reference TE device without a Si top layer failed due to electrical shorting. While the series resistance must be reduced to improve the TE characteristics for practical uses, this unique material platform would lead to realistic TE power generation systems at low cost.

Part III

Ultrasmooth metallic thin films deposited on Semiconductor substrates with assistance of a nucleation layer

Chapter 6

A phenomenological model of the growth of ultrasmooth silver thin films deposited with a germanium nucleation layer

The structural properties of optically thin (15nm) silver (Ag) films deposited on SiO_2/Si(100) substrates with a germanium (Ge) nucleation layer were studied. The morphological and crystallographical characteristics of Ag thin films with different Ge nucleation layer thicknesses were assessed by cross-sectional transmission electron microscopy (XTEM), reflection high energy electron diffraction (RHEED), X-ray diffractometry (XRD), grazing incidence X-ray diffractometry (GIXRD), X-ray reflection (XRR) and Fourier transform infrared spectroscopy (FTIR). The surface roughness of Ag thin films was found to decrease significantly by inserting a Ge nucleation layer with a thickness in the range of 1-2nm (i.e. smoothing-mode). However, as the Ge nucleation layer thickness increased beyond 2nm, the surface roughness increased concomitantly (i.e. roughing-mode). For the smoothing-mode, the role of the Ge nucleation layer in the Ag film deposition is discussed by invoking the surface energy of Ge, the bond dissociation energy of Ag-Ge, and the deposition mechanisms of Ag thin films on a given characteristic Ge nucleation layer. Additionally, Ge island formation, precipitation of Ge from Ag-Ge alloys and penetration of Ge into SiO_2 are suggested for the roughing-mode. This demonstration of ultrasmooth Ag thin films would offer an advantageous material platform with scalability for applications such as optics, plasmonics, and photonics.

In this chapter, we have extended our previous study to understand physical and chemical roles played by a thin layer of Ge in establishing ultrasmooth Ag thin film deposition.

6.1 Experiment

The samples were prepared as follows. Si (100) covered with a ~3nm native oxide (SiO_2) layer was used as the substrate. The SiO_2/Si substrates were treated in a cleaning bath of H_2SO_4:H_2O_2 (3:1), rinsed with deionized water, and dried with nitrogen (N_2). Subsequently, Ge and Ag were sequentially deposited onto the substrates, without breaking vacuum, in an electron-beam evaporation system (CHA Mark 50 ISS). The evaporation chamber was held at a base pressure of ~1μTorr and at ambient temperature during the deposition. The deposition rates of Ge and Ag were 0.01nm/s and 0.1nm/s, respectively. The thickness of Ge was varied (0, 1, 2, 5, and 15nm) while the thickness of Ag was fixed at 15nm.

The effects of varying thickness of the Ge nucleation layer on the physical characteristics of the Ag films were visually studied using cross-sectional transmission electron microscopy (XTEM). Further analysis of the crystalline structure of the Ag films was performed by reflection high energy electron diffraction (RHEED) with an acceleration voltage of 120kV and a camera-sample distance of

50cm. The structural characteristics of the Ag thin films were analyzed by two complementary X-ray diffraction methods: conventional X-ray diffractometry (XRD) with a 4-bounce monochromator and grazing incidence X-ray diffractometry (GIXRD). To obtain an independent estimate of surface-interface roughness of the Ag thin films, X-ray reflection (XRR) was used under a specular reflection geometry varying the incidence angle from 0.5 to 2.5^{o}, using a collimated Cu Kα (40kV, 45mA) X-ray source. To further assess the characteristics of surface roughness of the Ag thin films, self-assembled monolayers (SAMs) of CH_3-terminated alkanethiolate (CH_3-$(CH_2)_{17}$-SH) were formed by immersion into an ethanol solution containing the alkanethiolate (molar concentration of 0.01M) for extended times (>24h) at room temperature to obtain a strong hydrophobic surface[96] on Ag thin films deposited with and without a 2nm Ge nucleation layer. Since the degree to which SAMs organize on a surface depends on surface roughness, Fourier transform infrared spectroscopy (FTIR) (Nicolet Nexus 870 FTIR) with incident and exit glancing angles of 80° with respect to the surface normal of Ag films was used to evaluate the level of deformations introduced to CH_2 chains in the SAMs.

6.2 Results and Discussion

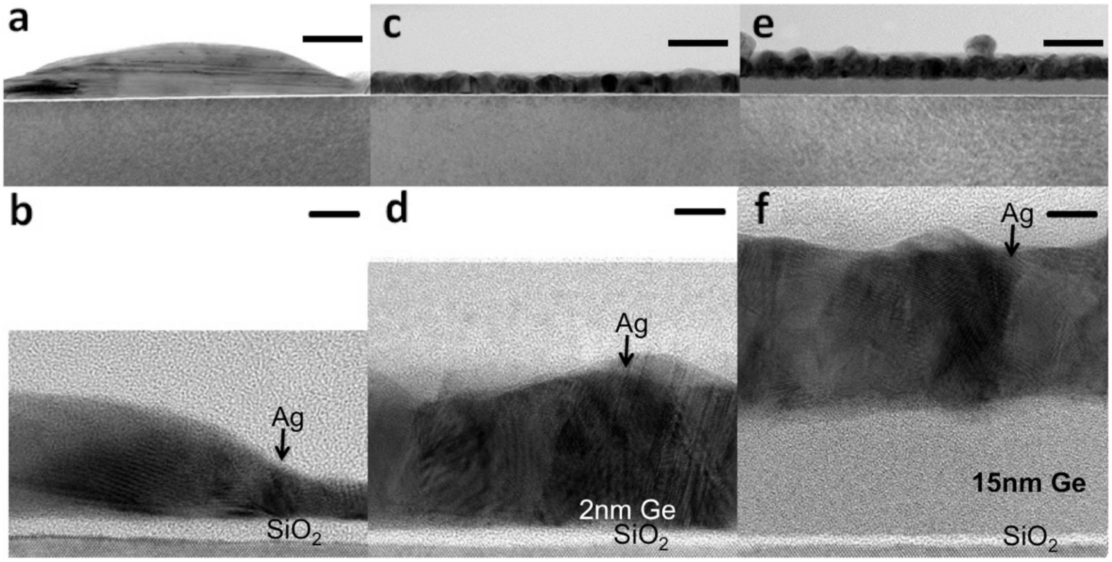


Figure6.1: XTEM images of Ag/Ge/SiO2/Si (100) for various thicknesses of Ge at two different magnification settings: (a) and (b) with no Ge nucleation layer; (c) and (d) with a 2nm Ge nucleation layer; (e) and (f) with a 15nm Ge nucleation layer. The scale bar for (a) (c) (e) is 50nm and for (b) (d) (f) is 5nm.

15nm of Ag film was chosen to be studied because it turned out to be the minimum thickness required for the formation of microscopically continuous Ag films on SiO$_2$ surfaces without a Ge nucleation layer under the deposition conditions comparable to those we used in this study. The XTEM image of Figure 6.1(a) shows that the Ag film deposited directly on the native oxide SiO$_2$ exhibits a considerable thickness variation across the film that contains "mound" features with heights varying from ~5nm to ~35nm. With a 2nm layer of Ge deposited on the SiO$_2$ surface prior to Ag deposition, the Ag surface roughness substantially decreased and the film was found to be made of segments with size ~5-10nm as seen in Figure 6.1(c). The Ag thin film with a 15nm Ge layer in Figure 6.1(e), however, exhibits its internal structure with a number of segments with size of ~25nm and shows the presence of apparent "protrusions" on the surface. Those features are not seen in Figure 6.1(c). At the same time, in Figure 6.1(b), a clear one-directional lattice fringe is observed, revealing, without a Ge layer, evident polycrystalline characteristics of the Ag film over an extended ~15nm length scale associated with the overall size of crystallites. In contrast, in Figures 6.1(d) and 6.1(f), lattice fringes running along multiple directions appear to be mixed over a length scale much shorter than that seen in Figure 6.1(b), indicating that the Ge layer promotes the formation of crystallites with sizes (~5nm) much smaller than those seen in Figure 6.1(b). Such Ag films made of fine crystallites can be referred to as quasi-amorphous in terms of their microscopic structures over a linear scale larger than 15nm. Also noticed in Figures 6.1(b), (d), and (f) is that the thickness of the native oxide SiO_2 appears to have decreased from ~3nm to ~2nm and ~1nm after the deposition of a 2nm and 15nm Ge layer, respectively.

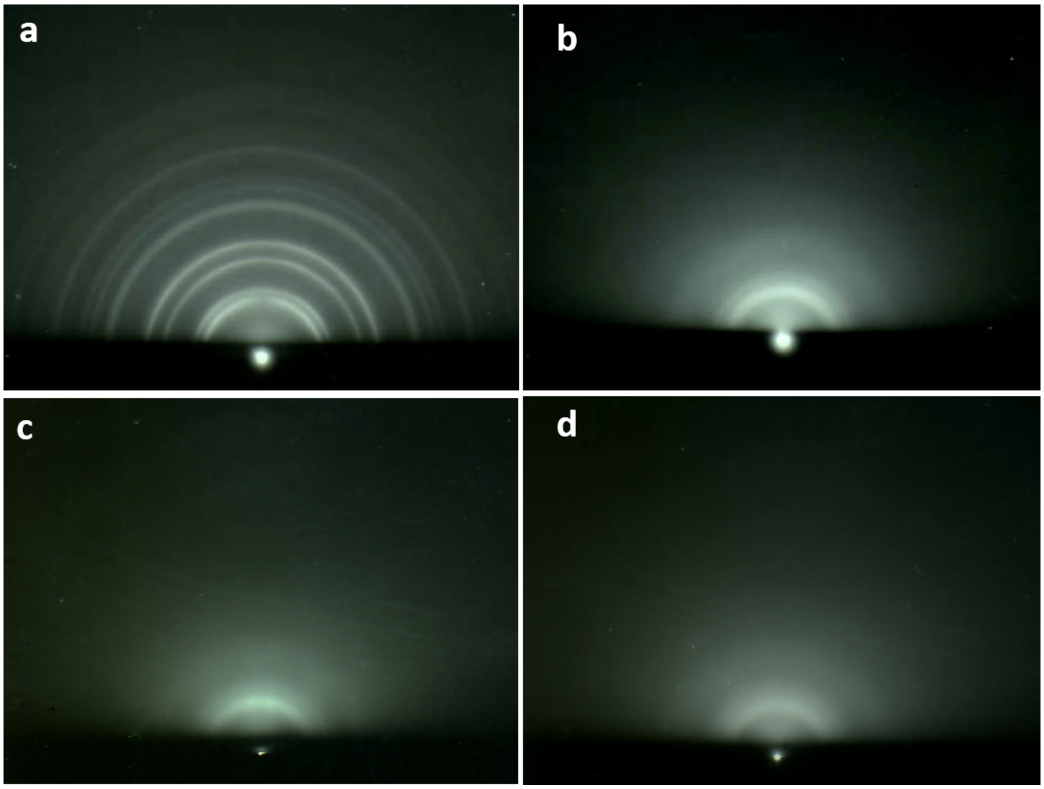


Figure 6.2: RHEED patterns of Ag/Ge/SiO_2/Si stacks for near-optimal Ge thickness: (a) with 0 nm Ge, (b) with 0.5 nm Ge, (c) with 1 nm Ge, (d) with 2 nm Ge. The RHEED pattern of sample without Ge layer shows many distinct Laue rings, indicative of a polycrystalline Ag surface. As thicknesses of Ge progress from 0.5nm to 1nm to 2nm, the rings became more diffuse, evincive of a smoother Ag surface.

RHEED performed on the Ag surfaces further exposed the dependence of structural transitions of the Ag thin films upon the addition of a Ge layer. The RHEED pattern in Figure 6.2(a) collected on the Ag film deposited without a Ge layer shows well-defined Laue rings, indicative of polycrystalline characteristics of the surface,[97,98] which is consistent with the one-directional lattice fringes seen in Figure 6.1(b). As the thickness of the Ge nucleation layer progressively increases from 0.5nm to 2nm, corresponding Laue rings became more diffuse, evincive of a smoother Ag surface[99]. The RHEED analysis clearly indicates that surface roughness of the Ag layer progressively decreases as the thickness of a Ge nucleation layer approaches its optimal thickness of 2 nm, while microscopic structures of these Ag films simultaneously change from polycrystalline to quasi-amorphous. The differences seen in the RHEED patterns in Figure 6.2 could be attributed to the variations in the level of oxidation on Ag surfaces; however, all of the samples were handled equally throughout the analysis to ensure that any oxidation could not skew the RHEED analysis. Formica et al.[24] reported that ultrasmooth Ag thin films with a Cu seeding layer significantly decreased the oxidation of the Ag thin films over the period of time of four months due to the reduction of surface area exposed to O_2/H_2O in the atmosphere, which further supports our statement that morphological transition (i.e. rough to smooth) and accompanying transition from poly-crystalline to quasi-amorphous is the main contribution to the transition seen in the series of RHEED patterns.

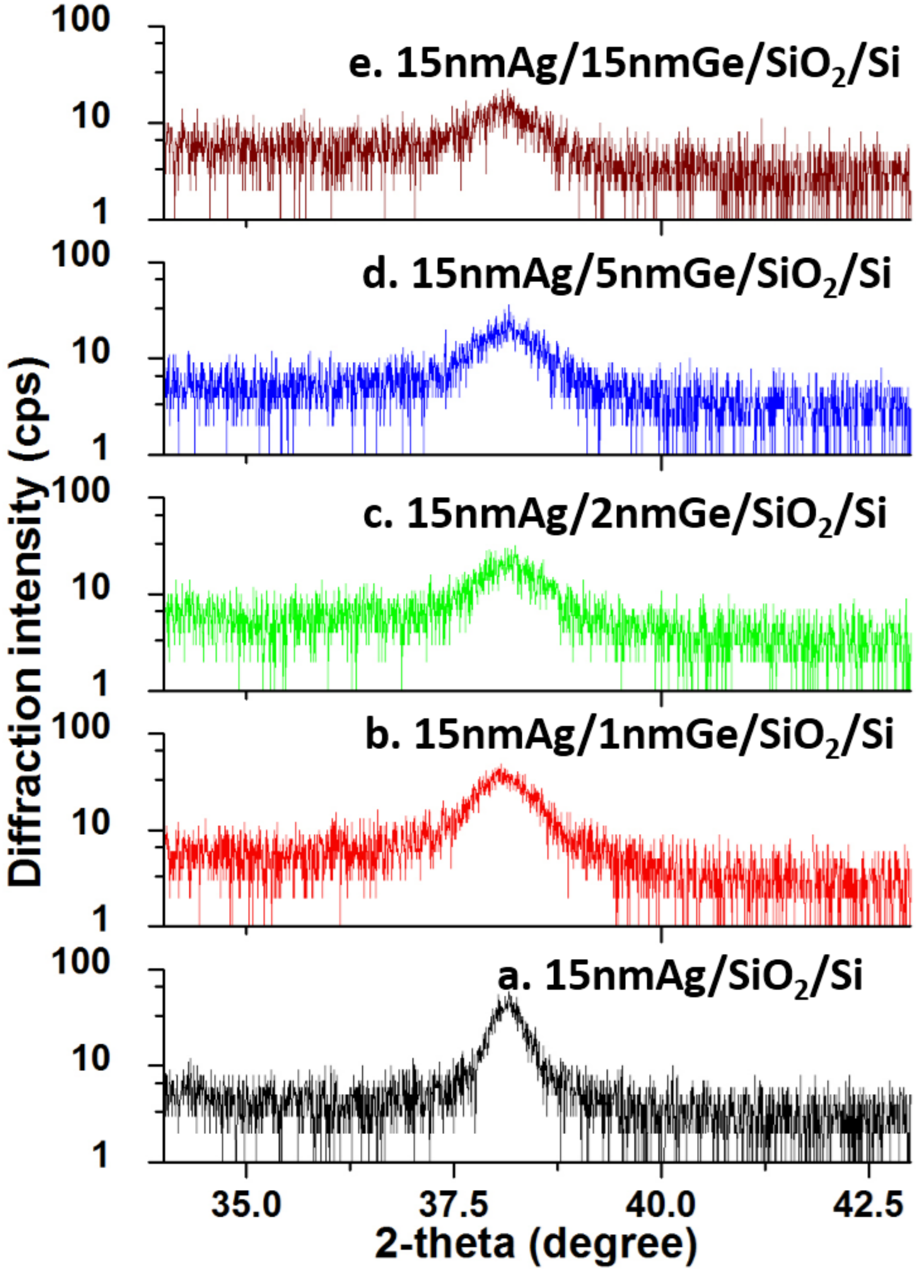


Figure 6.3. X-ray diffraction (XRD) of five Ag/Ge/SiO2/Si samples with different Ge thicknesses. The sample without Ge layer has the smallest FWHM of Ag (111) peak at 38.2^o indicating the largest crystallite size in these five samples. The samples with thin Ge layer (1-5nm) exhibit broadening Ag (111) peaks manifesting the Ag film

contained smaller grains. With thicker Ge layers (5-15nm), the crystallite sizes increased again leading to rougher surface of Ag thin films.

Table 6.1: FWHM and corresponding average crystallite sizes from XRD

Samples	**XRD**	
	FWHM (degree)	Crystallite Size (nm)
1. 15nmAg/SiO_2/Si sample	0.365	27.7
2. 15nmAg/1nmGe /SiO_2/Si sample	0.719	14.0
3. 15nmAg/2nmGe /SiO_2/Si sample	0.933	10.7
4. 15nmAg/5nmGe /SiO_2/Si sample	0.747	13.5
5. 15nmAg/15nmGe /SiO_2/Si sample	0.603	16.7

To better gauge the Ag surface roughness as a function of the Ge nucleation layer thickness (d_{Ge}), we performed XRD. Figure 6.3 illustrates the XRD spectra with a peak of 38.2° corresponding to Ag (111). The full-widths at half maximum (FWHM) of the Ag (111) peak for the samples with five variations in d_{Ge} are given under the "XRD" column in Table 6.1. Assuming that a Ag layer consists of crystallites with an average size *t*, *t* can be estimated by the Debye-Scherer equation

$$t = \frac{0.89\lambda}{\beta cos\theta_B},$$

where λ is the X-ray wavelength (1.5406 Å), θ_B is the Bragg diffraction angle, and β is the FWHM. The estimated average crystallite sizes *t* for each sample are also given in Table 6.1. The largest crystallite size ~27.7nm (i.e. the narrowest FWHM) was obtained for the Ag thin film with no Ge nucleation layer, which is consistent with the observations in Figure 6.1. Two trends clearly observable from the numbers given in the XRD column in Table 1 include: (1) the inception of a Ge nucleation layer results in a Ag film that contains crystallites with a size much smaller than a Ag film without a Ge nucleation layer, and (2) there is a break point at d_{Ge} ~2nm. In other words, there exists a critical value (i.e. 2nm) of d_{Ge} that minimizes surface roughness of the Ag layer. Beyond the critical d_{Ge}, the crystallite size increases, leading to rougher Ag surfaces.

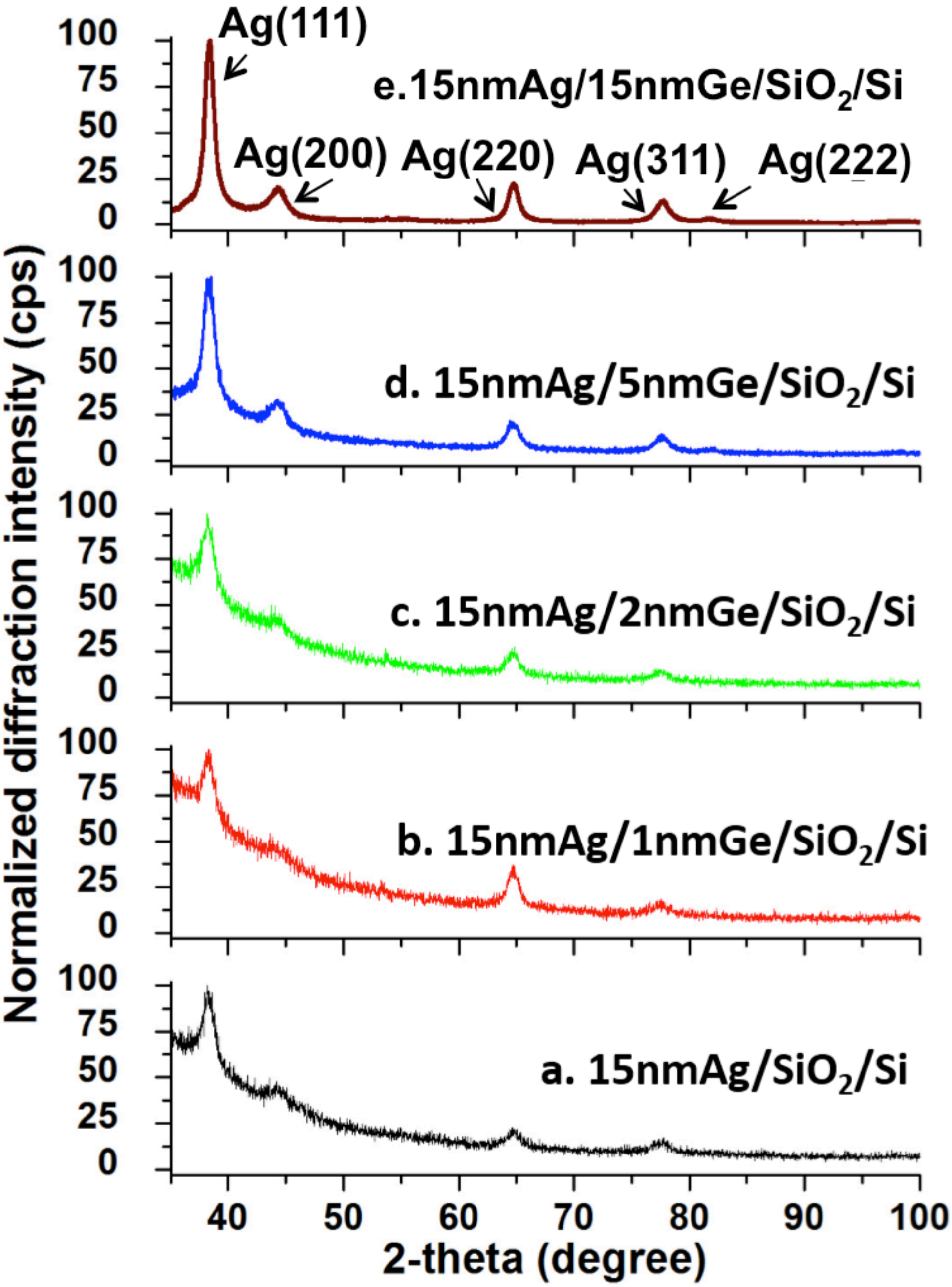
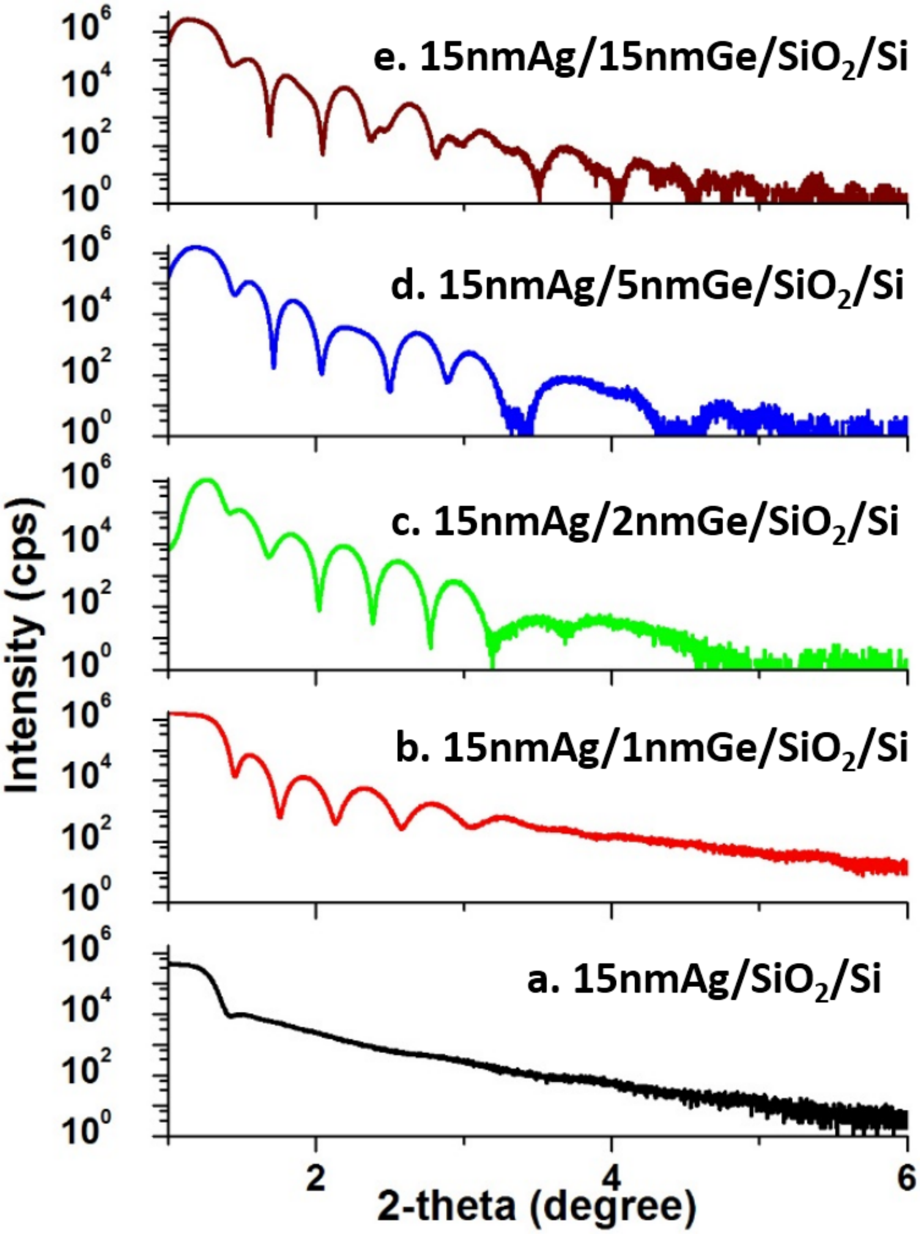


Figure 6.4. Grazing incidence X-ray diffraction (GIXRD) of five Ag/Ge/SiO$_2$/Si samples with different Ge thicknesses.

Table 6.2 Relative intensity of the peaks associated with each lattice plane from GIXRD for the five samples

Samples	**GIXRD**				
	(111) (38.2°)	(200) (44.3°)	(220) (64.3°)	(311) (77.6°)	(222) (82.2°)
1. 15nmAg/SiO$_2$/Si sample	100	40	25	26	0
2. 15nmAg/1nmGe /SiO$_2$/Si sample	100	0	65.4	16.5	0
3. 15nmAg/2nmGe /SiO$_2$/Si sample	100	13	32	13.2	0
4. 15nmAg/5nmGe /SiO$_2$/Si sample	100	26.8	31.3	17.6	2.9
5. 15nmAg/15nmGe /SiO$_2$/Si sample	100	18.8	13.6	12.8	2.2

GIXRD results collected with a wide range 2-theta scanning, shown in Figure 6.4, allows us to analyze peaks not observable in the XRD spectra. Since all GIXRD profiles are dominated by the Ag (111) peak, each profile is normalized to its respective Ag(111) peak intensity, allowing us to directly compare the intensities of the remaining four peaks: (200), (220), (311), and (222), shown in Table 6.2. The relative intensities of the GIXRD peaks for the sample without the Ge layer match those of polycrystalline Ag films[100]. It is clearly seen that the presence of a Ge layer decreases the intensity of both the Ag (200) peak and the Ag (311) peak. With a 1nm Ge layer, the intensity of the Ag (220) peak increased. However, the intensities decreased with larger d_{Ge} (2-15nm). The total intensity (i.e the sum of the four peak intensity) decreases and reaches a minimum as d_{Ge} increases from 0 to 2nm, suggesting that the poly-crystalline Ag film with d_{Ge}=0nm becomes quasi-amorphous with d_{Ge}=2nm; this is consistent with the XTEM and RHEED results. Beyond d_{Ge}=2nm, with thicker (5-15nm) Ge layers, the Ag (222) peak emerges, indicating the transition from the quasi-amorphous Ag film to poly-crystalline films with characteristics different from those of the poly-crystalline Ag film with no Ge layer.


e. 15nmAg/15nmGe/SiO$_2$/Si
d. 15nmAg/5nmGe/SiO$_2$/Si
c. 15nmAg/2nmGe/SiO$_2$/Si
b. 15nmAg/1nmGe/SiO$_2$/Si
a. 15nmAg/SiO$_2$/Si
Intensity (cps)
10^6
10^4
10^2
10^0
2
4
6
2-theta (degree)

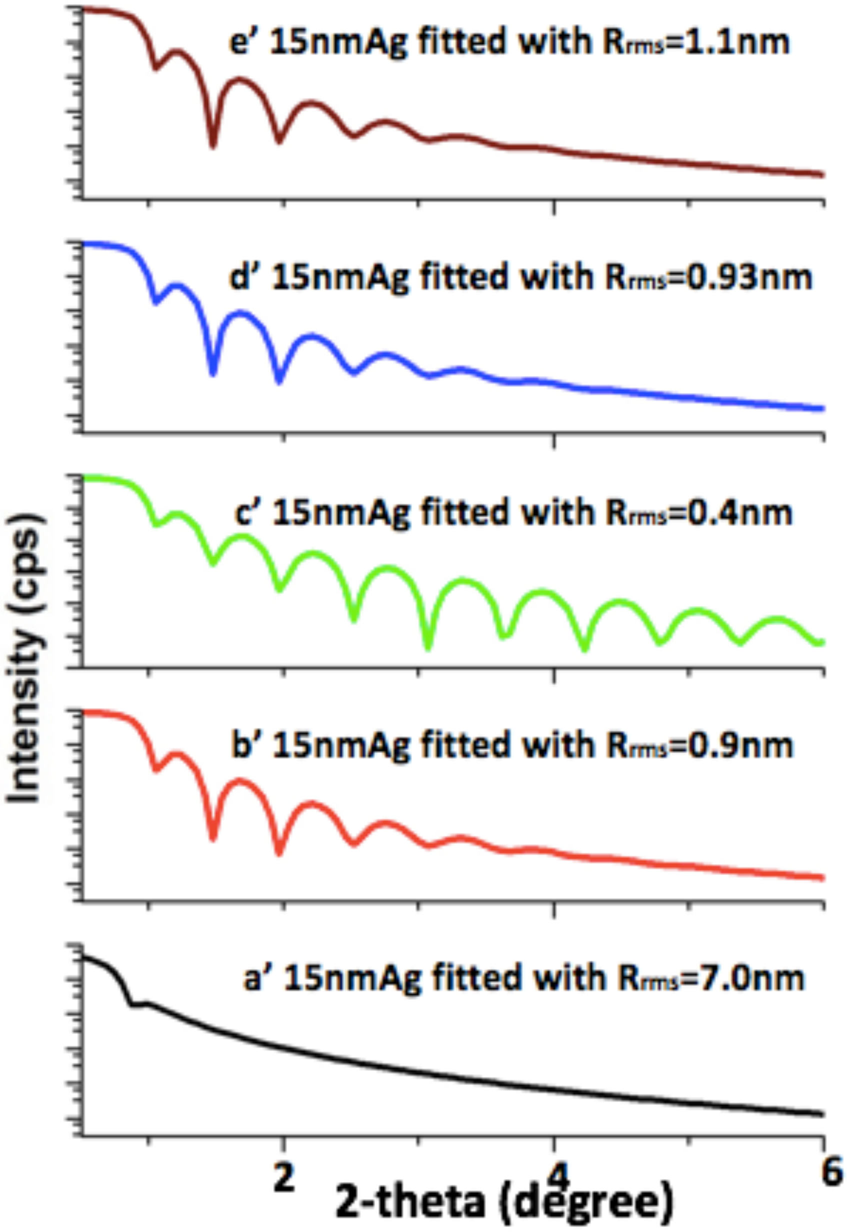


Figure 6.5. X-ray reflection (XRR) of five Ag/Ge/SiO_2/Si samples with different Ge thicknesses (up). The XRR spectrum of the sample without a Ge layer exhibits a damped oscillation amplitude, indicating the presence of a rough surface. For samples, with 1 and 2nm of Ge layers, the oscillations in the reflected X-ray intensity show rather persistent and consistent oscillation in the reciprocal space indicating the presence of much smoother surfaces. With an increased Ge thickness to 5nm and then 15nm, the oscillation becomes less persistent, suggesting that the surface roughness increases with a Ge layer thicker than 2nm. The experimental XRR profiles were fitted by

varying thickness and interfacial roughness for the Ag/Ge/SiO_2 stacks by employing genetic algorithm model. The obtained R_{surf} of Ag surfaces with different Ge thicknesses are shown in the figure (down).

In addition, XRR measurements over a large area (1cm ×1cm) were acquired from the five samples to confirm the smoothing effect of the Ge layer. The obtained XRR profiles are shown in Figure 6.5. As seen in Figure 6.5(a), the XRR profile of the sample with d_{Ge} = 0nm exhibits no intensity oscillation, indicating that the surface is too rough to even observe the oscillation. In the profiles shown in (b) and (c), the intensity oscillations are well defined. In particular, the oscillation amplitude of the profile in (c) is much larger than that in (b), demonstrating the significantly smoother surface of Ag deposited on a 2nm Ge layer, as compared to the Ag surface on a 1nm Ge layer. The reflected X-ray intensity in reciprocal space decreases more rapidly for greater interfacial roughness [22]; thus, the large interference oscillations present in these two samples clearly indicate that their surfaces are much smoother than that of (a). With an increased d_{Ge} beyond 5nm, the intensity oscillations become less persistent and appear to be more disturbed with smaller modulation amplitude, confirming that the thicknesses of Ge have passed the transition point (i.e. d_{Ge}=2nm) where the Ag films begin developing substantial surface roughness. The experimental XRR profiles were fitted by varying thickness and interfacial roughness associated with the Ag/Ge/SiO_2 stacks with different Ge thicknesses by employing a genetic algorithm[101]. The resulting roughness of Ag surfaces are 7.0, 0.8, 0.4, 0.9, 1.1nm for samples with 0, 1, 2, 5, 15nm, respectively, of Ge layers, which is consistent with surface roughness R_{surf} obtained from the AFM results: R_{rms} = 6-8nm for Ag films without Ge layers and R_{rms} = 0.6-0.8nm with Ge layers.

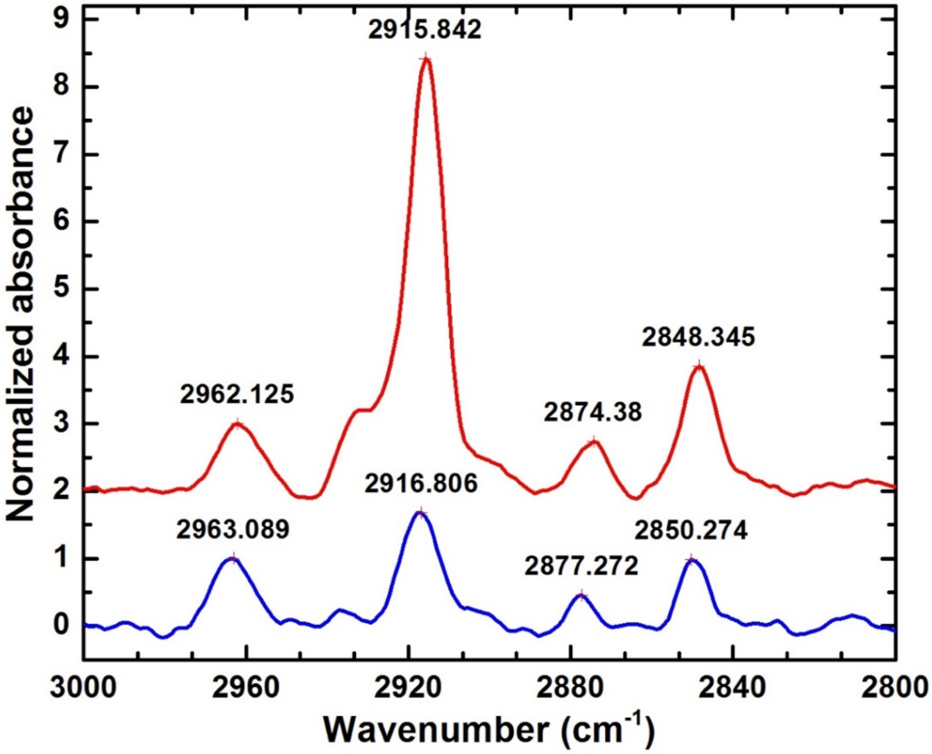


Figure 6.6. Fourier transform infrared spectroscopy (FTIR) of two silver thin film samples with an alkanethiolate self-assembled monolayer (SAM) coating. The blue plot shows SAM/Ag/SiO_2 absorbance and the red plot shows SAM/Ag/2nmGe/SiO_2 absorbance. In both cases, Ag nominal thickness was 15 nm. The stronger absorbance and narrower CH_2 peak at 2916.806cm^{-1} show a more ordered arrangement of alkanethiolate complexes, indicative of a less rough surface in the sample with a 2nm Ge layer.

Two FTIR spectra in Figure 6.6 provide indirect proof of the role played by a 2nm Ge nucleation layer, and although it is indirect, this proof is more relevant to many potential applications of Ag film surfaces. As seen in Figure 6.6, our reference sample without Ge yielded a FTIR spectrum with four distinct peaks characteristic of vibrational modes previously reported: asymmetric CH_3 (a-CH_3), asymmetric CH_2 (a-CH_2), symmetric CH_3 (s-CH_3), and symmetric CH_2 (s-CH_2) [102,103,104]. The sample with a 2 nm Ge layer resulted in stronger absorbance at all four peaks and a narrower a-CH_2 peak, suggestive of a more orderly arrangement of alkanethiolate complexes[105], which was presumably caused by a smoother Ag surface established on the 2nm Ge layer.

Although a coherent model that can be applied to all the observations appears to be difficult to devise, we bring several pieces within the scope of conventional nucleation and surface energy together to provide qualitative plausible views. The representative surface energies (γ) of Ag, Ge and SiO_2 are 1.12 J/m^2 (fcc(111)),[106] 1.32-1.71 J/m^2,[30] and 0.106 J/m^2,[107] respectively. The relatively high surface energy provided by Ge, therefore, would offer a favorable nucleation surface for the subsequent Ag deposition, due to the fact that a deposited film tends to wet on a high energy surface[108]. Thus, the Ag thin films grown on the surface of a thin Ge layer would be smoother and exhibit a lower percolation threshold than those of Ag films deposited directly on the surface of SiO_2.

Bond dissociation energies (H, enthalpy) can be also introduced: $H_{Ag\text{-}Ag}$= 162.9±2.9 kJ/mol and $H_{Ag\text{-}Ge}$ =174.5±21 kJ/mol.[109] The higher bond energy in Ag-Ge indicates that Ag atoms would prefer to bond more tightly to an underlying Ge surface than to neighboring Ag atoms, which is not prevalent at the Ag-SiO_2 interfaces. A 2nm Ge layer could supply more Ge atoms than the 1nm Ge sample to form more Ag-Ge bonds, which would lead to more uniform wetting of Ag on a Ge surface rather than the formation of Ag aggregates on a SiO_2 surface.

At the same time, growth mechanisms of metal thin films can be introduced to explain the interfacial nucleation effects. The rough Ag surface without a Ge layer agrees with previous findings in which Ag deposited on SiO_2 formed as patches of three-dimensional (3D) Ag clusters, as described by Volmer-Weber (VW) growth mode[110]. In VW growth mode, Ag atoms tend to coalesce with each other with a more robust adatom−adatom cohesive force and a weaker surface adhesive force. This leads to 3D islands nucleating on the substrate at the initial phase of the deposition process and therefore gives rise to Ag thin films with rough surfaces. In contrast, with a Ge nucleation layer (d_{Ge} = 2nm), the Ag thin film deposition would follow the Stranski-Krastanov (SK) growth mode, which begins with a uniform layer-by-layer deposition before transitioning to the 3D island growth mode. The initial layer-by-layer growth is attributed to a stronger surface adhesive force, which prevents the adatoms from coalescing and therefore substantially decreases the surface roughness[19].

The deposition of Ge on SiO_2/Si(100) would also follow the SK growth mode (The term "SK growth mode" used in our present context merely represents the deposition process that changes from layer-by-layer to islanding even without obvious involvement of strain associated with lattice mismatch at the Ge/SiO_2 interface) and the increased stresses imposed by successive monolayers of Ge encourage Ge island formation in the SK growth mode after the critical thickness of 3-4 monolayers (~1nm for Ge[111]) has been exceeded[112]. It is known that island growth occurs even in the deposition of Ge onto SiO_2, thus estimating island density would provide more insights for our experimental results. Island density, *n*, is governed by the equation

$$n = \frac{k_r}{va^2} e^{(E_d - E_r)/kT}$$

where k_r is the reaction rate constant prefactor, a is a constant dependent on the substrate (~0.3nm for SiO_2), v is the frequency factor, E_r and E_d are the reaction activation energy and diffusion activation energy, respectively[113]. Since E_r is roughly equal to E_d, the explicit temperature dependence of this equation is very weak, and the equation can be approximated as $\approx \frac{k_r}{va^2}$. The frequency factor is given by $v = \frac{k_B T}{h}$, where h is Plank's constant and k_B is the Boltzmann constant[114]. Therefore, $v = 10^{11} s^{-1}$ for room temperature deposition, or $v = 10^{13} s^{-1}$ for deposition around 500°C. Shklyav et al.[41] calculated and observed an island density of $n = 10^{12} cm^{-1}$ for Ge on SiO_2 deposition performed in the 500°C range, and therefore we would expect an island density of approximately $n = 10^{12} \times \frac{500}{25} = 2\times 10^{13} cm^{-1}$ for our room temperature deposition.

It has been reported[115] that Ge atoms segregate into Ag grain boundaries and tend to concentrate on the Ag free surface due to grain boundaries of Ag films providing sites where Ge solute atoms have lower Gibbs free energy than on the Ge-SiO_2 interface. However, because Ag and Ge are fully immiscible at room temperature in the thermodynamic theories,[116] Ge atoms tend to stay at low coordination Ag surface sites rather than high coordination Ag grain boundary sites

Flötotto et al.[117] reported that the Ag adatoms on the Ge or SiO_2 surface compete with existing Ag islands during film nucleation. The surface of Ge has a much higher activation energy of Ag adatom diffusion (~0.45eV)[118] than the surface of SiO_2 (~0.32eV)[119], and therefore the average diffusion length of Ag adatoms is significantly shorter on Ge than SiO_2 surface. Hence, formation of new Ag islands over diffusing of Ag adatoms into the existing Ag islands is more pronounced on the surface of Ge than SiO_2. As a result, the lower Ag adatom diffusion and relatively high initial Ag island density contribute to formation of a compacted Ag film with smaller grain sizes, which corresponds well with our XRD and XRR results.

After exceeding the critical thickness of 1nm, within a small increment of the amount of Ge, uniformed Ge islands[120] start forming a surface with effectively larger surface area and, as a result, larger total surface energy (the product of surface area and unit surface energy of Ge). Therefore, with higher total surface energy, 2nm of Ge offers a surface energetically more favorable for the subsequent Ag thin film than that provided by 1nm of Ge, resulting in a smoother Ag thin film.

Beyond d_{Ge}=2nm, new contributions are expected to dominate the Ag deposition. Three of them are described as follows: (1) Köhler et al[121] reported that when depositing up to ~3nm (12 monolayers), Ge grew islands, free of defects (i.e. coherent), on Si. Beyond 3nm of Ge, islands with a larger size emerging with V-shaped defects were observed. Similarly, in our case, with d_{Ge}>2nm, Ge islands would begin to exhibit roughness induced by defects associated with a larger island size. The resultant surface roughness of Ge translates to a rougher Ag thin film; (2)

Based on the Ag-Ge phase diagram from studies by Olesinski et al.,[122] at the ambient room temperature during our deposition, Ge has ~2% solubility into Ag to form the Ag-Ge FCC alloy at the Ge-Ag interface, which can explain why the 2nm Ge layer cannot be clearly observed on the XTEM image of Figure 1(d). This Ag-Ge alloy would provide gradual transition from Ge to Ag, resulting in a smooth Ag thin film. After exceeding 2% of the weight percentage, Ge starts precipitating, therefore with a Ge layer thicker than 2nm, even after the formation of Ag-Ge alloy is completed, the excess Ge precipitates at the Ag-Ge interface, which would cause the subsequent Ag thin film to increase surface roughness; (3) The observation that the thickness of the SiO_2 layer appears to progressively decrease as a Ge layer becomes thicker as observed in Figure 1(b) (d) and (f) can be explained by possible excess Ge that penetrates into and reacts with SiO_2:

$$SiO_2\,(S)+Ge(ad)\rightarrow SiO(g)+GeO(g)$$

In the presence of a thick Ge layer, the formation of rough GeO negates the benefit of inserting Ge between Ag and SiO_2.

6.3 Conclusion

In summary, we have performed experiments on the fabrication and characterization of thin (15nm) Ag films electron-beam evaporated atop Ge nucleation layers of different thicknesses on SiO_2/Si(100) substrates. The surface roughness of Ag thin films significantly decreases with a thin Ge nucleation layer, reaching its minimum with a 2nm Ge. As the Ge layer thickness increases, however, the Ag thin film surface roughness was found to increase. For the constructive factors introduced by a Ge nucleation layer for smoothing Ag thin films, the surface energy of Ge, the bond dissociation energy of Ag-Ge, and the deposition mechanisms of Ag thin films on a given characteristic Ge nucleation layer were discussed in this work. Additionally, Ge island formation in the SK growth mode, precipitation of unconsumed Ge from Ag-Ge alloy and penetration of Ge into SiO_2 are invoked for the destructive roles of a Ge layer to the Ag thin film smoothness.

Chapter 7
Conclusion

The Intermediate Layers supply an effective method to solve the existing problems for heteroepitaxial growth of semiconductor nanowires on metallic substrates and deposition of metal thin films on semiconductor substrates.

The conductive AZO and TiN thin films enabled the epitaxial growth of InP and Si nanowire networks on flexible Cu foils. In TE devices, a primary concern for converting heat to electricity is the thermal interface. Ensuring efficient heat transfer between the device, heat sources, and sinks is a challenging task particularly because traditional TE materials are rigid crystals that cannot adapt their shape to that of the specific application. These TE nanowires are one of the most promising advanced materials for high efficiency TE conversion, and for nanowire network devices as opposed to single nanowire devices, the path to scale up is reasonably clear. By developing these materials as flexible devices their intrinsic advantages combine with unprecedented practicality that no other current or advanced material can match due to their reliance on large crystals. This unique design with the Intermediate Layers, e.g. AZO and TiN etc., will investigate the use of nanowires to design, fabricate and commercialize flexible metallic substrates that can be applied simply to any surface with arbitrary geometry for energy scavenging or temperature control. Additionally, the high efficiency and ease of use of flexible and compressible metallic substrates should effect widespread adoption of TE devices and therefore significant energy savings and related environmental conservations.

Thermoelectric testing on these designed devices displays large series electrical resistance but Seebeck voltages comparable to its bulk counterpart. The preliminary results indicate that if series electrical resistance can be decreased, doped semiconductor nanowire networks could be an excellent candidate for thermoelectric applications. A better way to deposit the top contact on the surface of the semiconductor nanowires to significantly reduce the series electrical resistance is the future research.

By introducing a nucleation layer, the surface roughness of ultra thin metallic films on semiconductor substrates was decreased significantly, which is well suited to various applications where ultrathin metallic films with low surface roughness are required without post-processing (e.g., annealing or polishing). The structural properties, morphological and crystallographical characteristics of silver thin films with different germanium nucleation layer thicknesses were assessed by various characterization methods. The surface roughness of silver thin films was found to decrease significantly by inserting a germanium nucleation layer with a small thickness in the smoothing-mode. However, as the germanium nucleation layer thickness increased, the surface roughness increased concomitantly in the roughing-mode. This ultra-smooth deposition technique can be easily integrated into conventional device fabrication processes, and may be implemented in several important areas of emerging nanoscale devices.

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