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Fused InGaAs–Si Avalanche Photodiodes With Low-Noise Performances

Y. Kang, P. Mages, A. R. Clawson, P. K. L. Yu, M. Bitter, Z. Pan, A. Pauchard, S. Hummel, and Y. H. Lo

***Abstract*—A fused InGaAs–Si avalanche photodiode (APD) with a low excess noise factor of 2.3 at a gain of 20 is reported. This corresponds to a k factor of 0.02 for the silicon avalanche region. Dark current density as low as 0.04 mA/cm^2 at -5 V and 0.6 mA/cm^2 at a gain of 10 are measured; a small thermal coefficient, 0.09%/°C, of the breakdown voltage is observed for this APD.**

***Index Terms*—Avalanche photodiode (APD), noise, optical communication, photodetectors, wafer bonding.**

As an alternative to optical amplifiers, the avalanche photodiode (APD) is considered for high-sensitivity optical receivers in wide spectral range, high-bit-rate fiber communication networks. Current APDs employ a separate absorption and multiplication (SAM) design in which a high-bandgap avalanche multiplication region is used to suppress the tunneling current during avalanche breakdown. However, in order to limit the excess noise, a small k (defined as the ratio of hole to electron ionization potentials) is required [1]. Several material engineering approaches that utilize dead space effect, superlattice structures, and heterojunctions have been investigated to achieve small effective k values [2]–[4]. A simple approach is the wafer fused InGaAs–Si SAM-APD which exploits the small k value in Si. A high gain–bandwidth product of 315 GHz had been reported [5], however, there is no mention of excess noise property in the fused APD. This paper reports the low excess noise performance of the wafer-fused InGaAs–Si APD that uses special measures employed during the device design and fabrication to reduce the dark current to a low level [6].

Fig. 1 shows a schematic layer structure of the fused InGaAs–Si SAM-APD investigated in this work. The p-n junction in the silicon side is formed by epitaxy or ion implantation. The sheet charge density of the p-Si layer is around 1.8–3 $\times 10^{12}$ cm^{-2}. During operation, most of the voltage is dropped across the Si junction where multiplication takes place, while the electric field in InGaAs is sufficient to fully deplete the layer and to sweep out the photogenerated electron–hole pairs. Electrons drifting into the multiplication region initiate the impact ionization. Inside the high-field region, electron ionization dominates the impact ionization due to a highly asymmetric multiplication process in silicon. Consequently, the avalanche multiplication can be more statistically ordered and low-excess-noise multiplication can be obtained in this APD structure.

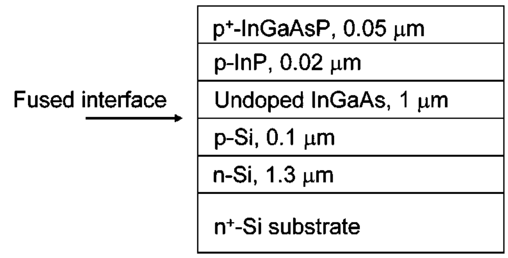

Fig. 1. Schematic layer structure of the fused InGaAs–Si APD. The top InGaAsP is transparent to 1.3–1.55-μm light.

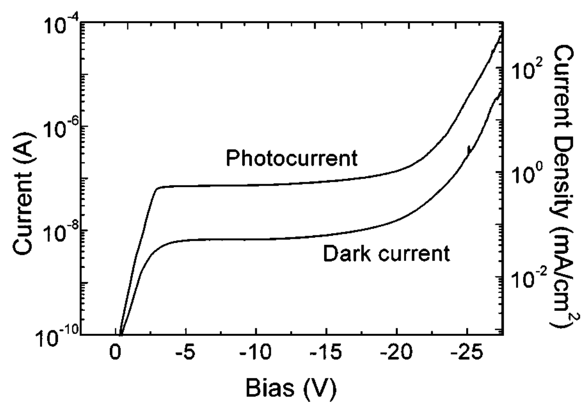

Fig. 2. Dark current and photocurrent of the fused InGaAs–Si APD versus bias voltage.

The device is obtained through a fusion of III–V and Si layers [7]. The fabrication and design of the fused APD have been reported previously [6], [8]. The fused APD has a 130-μm diameter mesa with 80-μm window for topside illumination. A polyimide film was spun around the etched mesa sidewall and also underneath the contact pad for isolation. The polyimide was cured in forming gas at 300 °C for 1 h.

Fig. 2 shows dark and photo current characteristics of a fused InGaAs–Si SAM-APD with a sheet charge density Q_m of 2.5 $\times 10^{12}$ cm^2 in p-Si. The device exhibits a dark current of 6 nA at -5 V and 79 nA when the gain M is 10. These correspond to dark-current densities of 0.04 mA/cm^2 and 0.6 mA/cm^2, respectively. This device I–V characteristic shows a hard reverse breakdown as normally observed in silicon APDs, in contrast to previous InGaAs–Si APDs which showed a soft breakdown, possibly due to a sizable tunneling current in the InGaAs layer [5]. The dark currents at room temperature are plotted versus M in Fig. 3 for three APDs with

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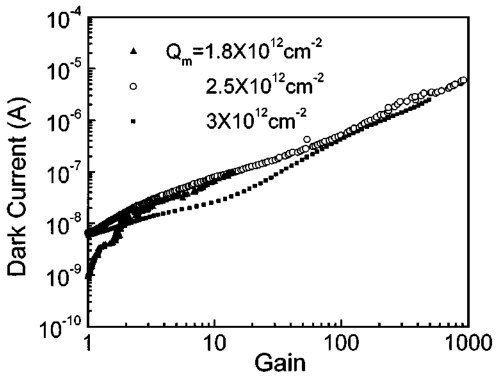

Fig. 3. Dark current of the InGaAs–Si APD versus M for three different values of the sheet charge density, Q_m.

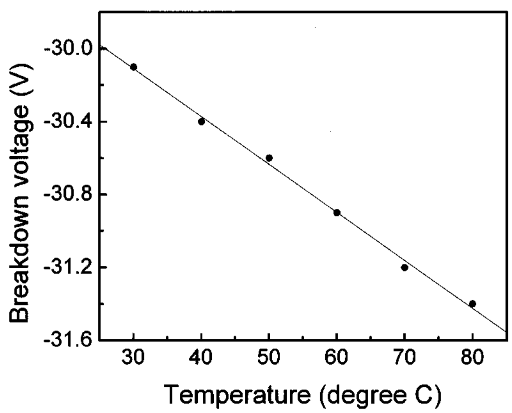

Fig. 4. Temperature dependence of the breakdown voltage, $V_{\rm BR}$ (the bias voltage when the dark current reaches 100 μA) for fused InGaAs–Si APD.

different Q_m's.The unity gain is referred to the point when the electric field extends into and fully depletes the undoped InGaAs layer. At unity gain, the responsivity of the APD without antireflection coating is 0.64 A/W at 1.31-μm wavelength.

The dark current of an APD can be expressed as $I_{\rm dark} = I_{\rm DU} + MI_{\rm DM}$, where $I_{\rm DU}$ is the unmultiplied dark current (e.g., surface leakage current), and $I_{\rm DM}$ is the primary dark current that undergoes multiplication [9]. For $I_{\rm DU} \sim I_{\rm DM}$, the dark current at large M is dominated by $I_{\rm DM}$. $I_{\rm DM}$ values extracted from the curves in Fig. 3, which correspond to APDs with different Q_m, are in the range of 4–7 nA. The insensitivity of $I_{\rm DM}$ to Q_m in these samples suggests that $I_{\rm DM}$ is dominated by dark current generated in the III–V region.

The 3-dB bandwidth of the device is measured at 1.5 GHz, which is a result of a large device capacitance ($\sim$ 1 pF). This capacitance is attributed to the Zn diffusion from the p$^+$-InGaAsP into the InGaAs absorption layer during material growth and wafer fusion, as confirmed by a Secondary Ion Mass Spectrometry (SIMS) measurement of the dopant profiles.

The temperature dependence of breakdown voltage $V_{\rm BR}$ (reverse bias when the dark current reaches 100 μA), is measured and depicted in Fig. 4. Defined as $\delta = (\Delta V_{\rm BR}/V_{\rm BR})/\Delta T$, the thermal coefficient of $V_{\rm BR}$ is 0.09%/°C for InGaAs–Si APD. The δ depends mainly on the temperature dependence of the ionization rates of carriers. This δ value is half of that observed in a typical InGaAs–InP APD and is consistent with the relatively lower thermal dependence of ionization coefficients in silicon [10].

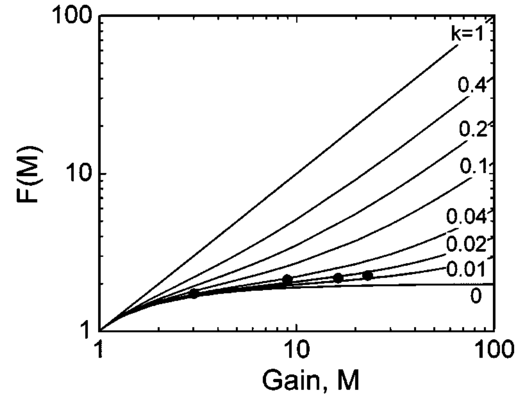

Fig. 5. Measured excess noise factors of the fused InGaAs–Si APD. The circles are the excess noise factor values obtained from measurements, and solid lines are those calculated from McIntyre's model at different k's.

The noise spectrum density at 130 MHz for different reverse-bias voltages of the InGaAs–Si SAM-APD was measured using low-noise RF amplifiers and an RF spectrum analyzer with a low relative intensity noise diode-pumped YAG laser ($\lambda = 1310$ nm) as optical source. Fig. 5 shows the excess noise factor $F(M)$ extracted from a room-temperature noise measurement of the InGaAs–Si SAM-APD (circle symbols). The solid lines are $F(M)$ versus M plots for different k's obtained from McIntyre's local field model [11]. The $k = 0.01, 0.02$ and 0.04 curves are typical for conventional silicon APDs; while the $k = 0.2$ and 0.4 ones are typical for InGaAs–InP SAM-APDs. The measured excess noise factor of the InGaAs–Si is much smaller than that of conventional InP-based APDs, and is 2.2 at a gain of 10 and 2.3 at a gain of 20. These fall on the curve with effective $k \sim 0.02$, indicative of the avalanche process inside the silicon p-n junction.

The sensitivity of a receiver based on this InGaAs–Si APD is modeled in [9, eq. (27)]. At 2.5 Gb/s, 1.3-μm wavelength and a bit-error rate of 10^{-11}, the sensitivity is estimated at -41.4 dBm at an optimal gain of 70 when $k = 0.05$. The sensitivity penalty due to the nonzero primary dark current $I_{\rm DM}$ is less than 0.4–0.7 dB, which gives an overall sensitivity improvement in excess of 5 dB over similar InGaAs–InP APD receiver.

In summary, using a wafer fusion technique, we have demonstrated a low-dark-current, high-gain, wafer-fused InGaAs–Si APD that is potentially useful for present fiber communication networks. The low dark-current level allows the extraction of a k factor of 0.02 for the silicon avalanche region and the examination of the primary dark current behavior of the device. The small thermal coefficient 0.09%/°C of the breakdown voltage observed for this APD is consistent with the avalanche process in silicon.

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