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Journal

IEEE Transactions on Biomedical Circuits and Systems, 10(5)

ISSN

1932-4545

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Publication Date

2016-10-01

DOI

10.1109/tbcas.2016.2614845

Peer reviewed

HHS Public Access

Author manuscript

IEEE Trans Biomed Circuits Syst. Author manuscript; available in PMC 2017 November 08.

Published in final edited form as:

IEEE Trans Biomed Circuits Syst. 2016 October ; 10(5): 990–1002. doi:10.1109/TBCAS.2016.2614845.

A Bidirectional Neural Interface IC with Chopper Stabilized BioADC Array and Charge Balanced Stimulator

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Abstract

We present a bidirectional neural interface with a 4-channel biopotential analog-to-digital converter (bioADC) and a 4-channel current-mode stimulator in 180nm CMOS. The bioADC directly transduces microvolt biopotentials into a digital representation without a voltage-amplification stage. Each bioADC channel comprises a continuous-time first-order ΔΣ modulator with a chopper-stabilized OTA input and current feedback, followed by a second-order comb-filter decimator with programmable oversampling ratio. Each stimulator channel contains two independent digital-to-analog converters for anodic and cathodic current generation. A shared calibration circuit matches the amplitude of the anodic and cathodic currents for charge balancing. Powered from a 1.5V supply, the analog and digital circuits in each recording channel draw on average 1.54 μA and 2.13 μA of supply current, respectively. The bioADCs achieve an SNR of 58 dB and a SFDR of >70 dB, for better than 9-b ENOB. Intracranial EEG recordings from an anesthetized rat are shown and compared to simultaneous recordings from a commercial reference system to validate performance *in-vivo.* Additionally, we demonstrate bidirectional operation by

recording cardiac modulation induced through vagus nerve stimulation, and closed-loop control of cardiac rhythm. The micropower operation, direct digital readout, and integration of electrical stimulation circuits make this interface ideally suited for closed-loop neuromodulation applications.

Index Terms

Closed-loop neuromodulation; neural recording; electrocorticography; electroencephalogram; vagus nerve stimulation; Delta-Sigma; chopper stabilization

I. INTRODUCTION

Biomarker extraction from physiological signals such as the electrocorticogram (ECoG) and local field potentials (LFP) is of paramount importance to the diagnosis and therapy for a large number of neurological disorders. This is nowhere more clear than for closed-loop neuromodulation therapies that drive stimulation or update stimulation parameters based on information obtained from detected biopotentials [1]. These types of systems hold potential to drastically improve the efficacy of open-loop neuromodulation, in applications such as deep-brain stimulation for Parkinson's disease [2] and cortical stimulation for epilepsy [3]. The success of closed-loop platforms will depend on the ability to process biopotential signals in real time, and use the information to tailor therapy. Ultra-low power processing of neural signals can be performed in the analog domain [4], but the flexibility inherent to digital processing makes its use much more common [5]–[7]. With closed-loop systems, like all implantable systems, a holistic approach is necessary as sensitivity, power consumption, and system size are all critical parameters.

A traditional biopotential measurement system adheres to a three step sequence: 1) low noise amplification and high pass filter, 2) variable gain amplification and bandpass or anti-aliasing filter, and finally 3) analog-to-digital conversion [8], [9]. If a single ADC is time-multiplexed across multiple channels, then an additional buffer per channel is required to drive the input capacitance of the ADC. Interestingly though, an increasingly popular design choice is to integrate an ADC into every channel [10]. This choice becomes even more favorable when designing with deep sub-micron processes, where very high power efficiency and very low area designs are obtained [11], [12]. Nevertheless, these designs still abide by the standard paradigm of amplify, filter, then quantize, and each step requires power and silicon area.

The bidirectional interface presented here builds upon previous bioADC designs [10], [13] for sensing functionality, and integrates everything from front-end sensing to back-end digital decimation in a single circuit per channel. Without explicit voltage amplification, this circuit digitizes microvolt level neural signals. Compared with previous works, we demonstrate (1) an improvement in bit resolution by decimating a first-order noise-shaped bit stream with a second-order decimation filter, and (2) an improvement in noise-power efficiency through chopper-stabilization.

The performance of the proposed circuits has benefited greatly from process scaling. The reported circuits in [10], [13] were fabricated in a 0.5 μm process, so the inclusion of the second order filter was prohibitive in terms of area. Implementation in a 180 nm processes permitted integration of a second-order decimation filter in-line with the sensing circuits.

Further, a major challenge with integrating chopper stabilization into a biopotential amplifier is the electrode DC differential offset which is addressed with a well-known and commonly used servo-loop technique. The single bit output of the sensing circuits makes the mixed-signal approach of [12] attractive due to both the challenge of filtering the noise shaped signal in the analog domain and the simplicity of filtering a single-bit signal in the digital domain.

Portions of this work were previously presented in conference form [14]. Here we present several significant extensions and improvements upon this earlier publication. In our earlier work, the dominant source of noise in the recording circuits was the $1/f$ noise from the OTA. Therefore, the chopper stabilization employed here improves noise-power efficiency. For stimulation functionality, we integrated additional circuits for digitally controlled current stimulation [15]. As illustrated in Fig 1, four channels of both sensing and stimulation were fabricated on a single 1.5 × 1.5 mm^2 chip, and offers a versatile platform for closed-loop neuromodulation. Finally, we present more thorough *in-vivo* validations. We demonstrate the simultaneous use of both recording and stimulating capabilities by (1) directly recording and detecting physiological effects due to vagus nerve stimulation (VNS), and (2) controlling heart rate with closed-loop VNS [16], [17].

The organization of this paper is as follows. In Sections II-A – II-D we describe the core elements of the ΔΣ bioADC, while the servo-loop used to cancel differential DC electrode offsets is described in Section II-E. The stimulator architecture is briefly described in Section II-F, but has been described in detail elsewhere [15]. Section III-A contains characterizations of the bioADC in terms of SNDR and input-referred noise, and Section III-C presents *in-vivo* demonstrations. Finally, Section IV provides a comparison of this work with the state of the art, and concludes the paper.

II. CIRCUIT DESIGN

The schematic for a single channel in Fig. 2(a) illustrates the main components of the system. An operational transconductance amplifier (OTA), loaded with a large output capacitor (13 pF), operates as a $G_m - C$ integrator. A latched comparator is used as a 1-bit quantizer, which drives an auxiliary transconductor supplying a feedback current to the integration capacitor, implementing a 1-bit digital-to-analog converter (DAC). As shown in Fig. 2(b), the loop operates as a continuous-time, first-order ΔΣ ADC which have inherent anti-aliasing properties [18]. The bitstream generated by the comparator (Q) is decimated by a second-order comb filter with a transfer function given by $((1 - z^{-N})/(1 - z^{-1}))^2$. The second-order decimation filter substantially extends the bit resolution obtainable from the first-order ΔΣ noise shaping, offering 1.5 bits for each two-fold in oversampling ratio (OSR) rather than a single bit per two-fold OSR for a conventional first-order (counter) decimator

or incremental ADC [19]. Hence 10-b resolution can be obtained with just 128 rather than 1,024 OSR.

Chopping switches are placed before and within the frontend OTA to mitigate $1/f$ noise. Chopper-stabilized amplifiers, when interfaced to electrodes, must remove the large differential DC offset of the electrodes that is up-modulated to the chopping frequency [8], [20]. This design uses the method of Muller *et al* [12]; the 1-bit output of the ΔΣ is filtered by a discrete-time integrator, and the output is fed back to the input through a ΔΣ DAC.

The frequency response of this circuit can be tuned as follows. The low-pass cutoff frequency is set by programming the oversampling ratio, and trades off resolution for bandwidth [10]. The high-pass cutoff frequency is set by the servo loop [12]. In this chip the cutoff frequency is fixed at 0.2 Hz but could be programmably tuned as described in Section II-E The chip additionally contains a four-channel neural-stimulation module and calibration circuit [15]. The calibration circuit can be used to charge-balance the stimulation waveform within each channel, spatially pattern stimulation into bipolar and tripolar patterns, and calibrate current DAC coefficients within each channel.

A. OTA

A fully differential, telescopic OTA, shown in Fig. 3(a) is used in the $G_m - C$ integrator. Chopping switches are placed before capacitors C_{in}, to up-modulate signals of interest, and within the OTA at the sources of cascodes $M4 - M7$, such that the chopper works by switching currents [20]. The chopping switches at the input in Fig. 2 are composed of complementary devices, while the switches in the OTA (Fig. 3(a)) are composed of either NMOS or PMOS devices. A commonmode control signal (V_{cmc}) is derived using a standard circuit consisting of two differential pairs (not shown) [21]. Bias voltages V_b, V_{tcas}, V_{ncas}, and V_n are generated on-chip, using a replica-biasing scheme. To maximize noise/power efficiency of the OTA, the input pair operate in subthreshold (W/L = 213μ/0.95μ), and the NMOS load (W/L = 95μ/3.6μ) are source degenerated. All other devices are sized with large W/L to maximize headroom as their contributions to noise are negligible compared to that of the input pair and the active loads.

Capacitors C_{in+}/C_{in-} (30 pF) and pseudoresistors form high-pass filters that set the common-mode input level of the OTA. To avoid a voltage division between $C_{in,+}$ and the parasitic input capacitance of the OTA, capacitive neutralization is used, where MOS capacitors C_{M+}, C_{M-} cancel the Miller multiplied C_{gd} of the input pair [21], [22].

Finally, to increase CMRR, the bias voltages for M4/M5 are set as a function of the source-coupled node voltage Vp. A small current source is used to drop a voltage consisting of $V_{gs,4}$ and $V_{ds,0}$. This works to keep the V_{ds} across the input pair constant in the presence of a common mode input [8].

B. Comparator

The latched comparator shown in Fig. 3(b) is based on that of Yin *et al* [23], which operates in three stages: reset, amplify and latch. During reset, the differential pair sets a small voltage difference across the reset switch that tracks the difference at the input. With a

falling edge on reset, both reset and latch are low, and the differential pair with a cross-coupled NMOS load amplify the difference at the input. A rising edge on latch causes the cross-coupled inverters to amplify further and bring the outputs to the supply rails. An S-R latch is used to hold the comparator result after the comparator is reset. The cascodes hold the drain of the input pairs relatively fixed which helps to reduce kickback noise during the latch phase. The offset and noise of the comparator are noise-shaped by the ΔΣ loop, hence the constraints on this block are fairly relaxed, so no additional pre-amplification or offset-reduction techniques are necessary.

C. Feedback DAC

A transconductor converts the comparator outputs to a feedback current, implementing a 1-bit DAC. As illustrated in Fig. 2(b), the magnitude of this current can be referred back to the input though the OTA's G_m, and sets the full-scale range of the ADC. The current is set with an on-chip programmable bias generator [24].

D. Decimation Filter

The simplest option to decimate the output of a 1-bit ΔΣ is a counter, reset after OSR cycles. However, this filter is approximately OSR times less effective at suppressing out of band quantization noise compared with an ideal filter [19]. A second order filter can be obtained by cascading an accumulator after the counter, which attenuates the out of band quantization noise to a level comparable to an ideal filter.

The impulse response of this filter can be obtained by taking the inverse z-transform of the transfer function, or graphically by convolving two rectangular pulses. This triangular impulse response can be implemented in a hardware-efficient manner as illustrated in Fig. 4 [19]. The positive ramp weighted sum is obtained with a counter and a data-gated accumulator (Fig. 4 top left). The negative ramp weighted sum is obtained by subtracting a positive ramp weighted sum from a rectangular weighted sum. A data-gated counter (Fig. 4 bottom) implements the rectangular weighted sum, and the positive ramp weighted sum is subtracted from it.

E. Mixed-Signal Servo Loop

An on-chip passive high-pass filter consisting of input capacitors and high resistance MOS pseudoresistors are used to set the common-mode input voltage. However, with chopping activated the system becomes DC-coupled, and large differential DC offsets at the electrodes can saturate the frontend. Several bioamplifier designs have used an active feedback loop to sense the DC level and cancel it at the input [8], [20], [25]. These designs use switched-capacitor integrators in the feedback loop to extract the DC level, and subtract it at the input. Mixed-signal designs, directly digitize each channel and can therefore use digital processing and DACs to filter out the DC component [11], [12]. Here, a DC-servo loop consists of a digital low-pass filter to extract the DC level, and a ΔΣ DAC subtracts that DC value from the input.

Referencing Fig 5, V_e represents the differential input signal at the electrodes, while V_{in} represents the differential input signal seen by the OTA in Fig. 3(a). The ΔΣ ADC encodes

V_{in} in Q, a 1-bit signal representing values of $\pm A_{fs}$, where A_{fs} is half the full-scale voltage. Q is filtered by a discrete time integrator with a transfer function of shown in Fig. 5. Because the integrator treats Q as ±1, an implicit scaling of $1/A_{fs}$ takes place.

The integrator output is scaled by a constant right-shift, and fed to a ΔΣ DAC. The DAC is a 5-bit, thermometer-coded capacitor array with N=31 unit capacitors C_u. The output of the ΔΣ (n in Fig. 5), switches n unit capacitors to a reference voltage V_{ref}, and $N - n$ unit capacitors to ground. Data-weighted averaging is used for mismatch error shaping [19]. On a given cycle, with $n > 0$, capacitors $C_i - C_{i+n-1}$ are switched to V_{ref}. For the following cycle, i is incremented to $i + n$ such that a different subset of capacitors are used for the next DAC value. As a result, errors due to mismatch is translated into high-frequency noise.

In Fig 5, treating the ADC and DAC as unity gains, the loop gain seen by V_{in} can be written as,

$$H(z) = K\frac{1+z^{-1}}{1-z^{-1}} \quad (1)$$

With K given by,

$$K = \frac{1}{A_{fs}}\frac{1}{2^B}\frac{V_{ref}}{2^{R-1}}\frac{NC_u}{NC_u + C_{in}} \quad (2)$$

Here, R is the DAC input word length. The maximum DC offset that can be canceled, $V_{os,max}$, is set by the voltage division of V_{ref} by NC_u and C_{in}. K can be rewritten as:

$$K = \frac{V_{os,max}}{A_{fs}2^B 2^{R-1}} \quad (3)$$

With the loop closed:

$$H(z) = \frac{1-z^{-1}}{1+K+(K-1)z^{-1}} \quad (4)$$

And with $F_c \ll F_s$, and $K \ll 1$, the cutoff frequency can be approximated as:

$$F_c \approx \frac{F_s}{\pi}K \quad (5)$$

With F_s = 128 kHz, V_{FS} = 5 mV, B = 3, and $V_{os,max}$ = 30 mV, a cutoff frequency of ≈ 0.2 Hz is obtained. Here, B is fixed as constant right shift of 3, but offers a mechanism to programmably control the cutoff frequency.

F Stimulator

The stimulator architecture implemented on this chip was previously fabricated as an 8-channel stand-alone neurostimulator, and is described in detail elsewhere [15]. In this work, a four channel version has been integrated on chip to enable bidirectional operation on the same silicon circuit. The salient features relevant to the present bidirectional interface are illustrated in Fig. 6.

Each stimulation channel contains two independent, subbinary radix, current-mode DACs that supply biases to regulated cascode current sources. The DACs are MOST R-βR ladders with $\beta = 3$ [26]. This structure provides redundancies in the input-output relationship making it robust to mismatch. The redundancies can be removed by a digital calibration method [15], [27]. A calibration circuit is shared across channels and consists of an integrator and comparator. This provides an analog-to-time-to-digital conversion; the time it takes for the integrator output to trip the comparator is digitized with an external counter. The output of the comparator was routed to a pad (V_{cmpr} in Fig. 6.) and this timing is performed externally. Because an external devices is required to program the chip and read out data, the overhead needed to perform the timing externally is negligible. With both current sources simultaneously activated, the difference between the source and sink, or residue, is routed to the calibration circuit. Either DAC can then be incremented to minimize this difference for charge balanced stimulation [28], [29].

With the calibration unit shared across channels, the residue nulling procedure described above can be applied to multiple channels at once. As a result, the stimulation currents can be matched and even ratioed to allow multipolar stimulation patterns. Multipolar stimulation can be used to shape the electric field *in-vivo* for targeted electrical stimulation [30]. This feature is particularly important for future closed-loop neurostimulation applications, where the electrophysiological effects of stimulation can be monitored and used to update stimulation parameters autonomously.

G. Stimulation Artifact

Simultaneous stimulation while sensing can induce artifacts in the recordings. Artifacts can be the result of intrinsic cross-talk between the stimulator and recording circuits as well as direct coupling through volume conduction *in-vivo*. Both the recording and stimulation blocks are enclosed by guard rings to minimize cross-talk through the chip substrate. Otherwise, artifact removal or mitigation circuits have not been implemented on this chip. Therefore, the hardware may not be suitable for simultaneous recording and stimulation from a single electrode array. However, for distant recording and stimulation electrodes, the artifact is predominantly a commonmode signal. In Sections III-A and III-C, characterizations of the intrinsic crosstalk and stimulation artifact *in-vivo* are presented respectively.

III. MEASUREMENT RESULTS

The circuits were fabricated in a 0.18 μm 6M1P CMOS process (Fig 7). The chip contains four channels; the analog circuits of Fig 2(a) occupy 320 $\mu m \times 580$ μm, the mixed-signal

servo loops occupy 380 μm × 580 μm and the decimation filters and output shift registers occupy 220 μm × 400 μm. The input, AC-coupling capacitors as well as the integration capacitor were realized with MIM devices. The active circuits were placed underneath these components, effectively cutting the required area in half. An additional layer of metal (M4) was sacrificed to shield the MIMs and distribute power.

A. bioADC Characterization

Fig. 8 shows the output spectrum of a tone test along with the theoretical NTF for a first-order ΔΣ. At low frequencies, the resolution is noise-limited, but at high frequencies ($f > F_s/64$) the noise-shaping is clearly visible, and follows the theoretical curve very closely. Furthermore, tones at the chopping frequency and its harmonics can be seen. Here and unless otherwise specified, a chopping frequency of 2 kHz was used. Note, since the chopping frequency is a factor of the sampling frequency, the decimation filter nulls these peaks, and no aliasing of the chopper ripple is observed.

Fig. 9 illustrates the measured the frequency response of the circuit with the OSR programmed to 128, 256, and 512. The decimation filter does provide attenuation in the passband. For the SNDR and noise measurements that follow, an equalizer was used to undo these in-band effects of the filter.

Fig. 10 shows the results of a tone tests for signal-to-noise-distortion-ratio (SNDR) measurements. The system clock was set to 128 kHz and the oversampling ratio set to 256, which gave a decimated data rate of 500 Hz. The input tone frequency was set to 24 Hz. Peak SNDR was measured to be 58.5 dB, at an input amplitude of 4 mV_{pp}. Fig. 10 illustrates that SNDR was limited by thermal noise and power in the 3rd harmonic, which is attributed to the tanh characteristic of the OTA's differential pair in subthreshold. There is no need to linearize the circuit for greater spurious-free dynamic range (SFDR) since 4 mV_{pp} is already above the range of most biopotentials. Fig. 10(b) also compares the spectrum recorded with and without chopping. In addition to the reduction of $1/f$ noise, chopping mitigates even-order distortions which are due to mismatch in the differential pair.

To measure the inherent circuit noise, the inputs of all channels were shorted to ground. Fig. 11 shows the measured power spectral density (PSD) referred back to the input with and without chopping. Chopping significantly improves noise performance, and the dominant in-band noise source is thermal noise. The thermal noise level appears approximately at 60 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Though it appears from Fig. 11 that the $1/f$ noise corner is below 1 Hz, this is not the case, as the HPF attenuates signals below 1 Hz. At higher frequencies, the ΔΣ quantization noise can be seen to rise above the thermal noise floor. This includes the quantization noise from the ADC and DAC. Integrating under the curve from 0.25 Hz to 250 Hz yields a total input referred noise of 1.0 μV_{rms}.

The differential input impedance of the bioADC was measured for chopping frequencies ranging from 500 Hz – 8 kHz. The measurements as a function of input frequency is illustrated in Fig 12. A 15 point log-spaced sweep from 5 Hz to 10 kHz was taken. Table I lists the measurement results at 76 Hz.

Common-mode rejection of the bioADC was measured without chopper stabilization and with chopping at 2 kHz. The measurement was made by applying a 90 mV_{pp} 50 Hz signal to both inputs. Without chopping, CMRR was measured to be 77 dB and increased to 97 dB with chopping enabled. The reason for the increase in CMRR is that chopping affects only the differential mode component of input signals. Hence the common-mode component of the input signal is passed unchanged. Due to mismatch in the OTA some of this common-mode signal is converted to a differential mode signal. However, this differential mode signal is then up-modulated by the chopper in the same way as $1/f$ noise. A more rigorous treatment of this issue can be found in [31].

Chopping affects only the differential mode component of input signals. Hence the common mode component of the input signal is passed unchanged. Due to mismatch in the OTA some of this common-mode signal is converted to a differential mode signal. However, this differential mode signal is then up-modulated by the chopper in the same way as 1/f noise. Therefore, a large portion of the differential output due to a common-mode input is transposed to the chopper frequency and removed by the decimation filter. A more rigorous treatment of this issue can be found in [X].

The use of an open-loop G_m stage leads to mismatch across channels. This mismatch was characterized by applying a 2.5 mV_{pp} tone to all channels and comparing the peak heights in amplitude spectra. This parameter was measured in the four channels across nine chips. Within chip variation was bounded by ±2%, and a histogram of the across channel variation, normalized to the average for each chip is illustrated in Fig 13.

Crosstalk between the bioADC and the stimulator blocks was measured by tying the front-end inputs to ground while pulsing the fullscale current though a dummy load (4.7 kΩ) on all channels with a pulse width of 10 ms and a 25 Hz frequency. Recordings from each channel were then time aligned to the onset of each stimulation pulse and averaged across 7500 pulses to extract any measurable crosstalk. Fig 14 illustrates the waveforms after averaging. Channels 1, 2 and 4 show a detectable artifacts, but the worst case is less than 1 μV_{pp}.

B. Power Consumption and Noise Efficiency

The average static current consumption of the analog components in Fig 2(a) was 1.41 μA with the following break-down: 1.05 μA for the OTA (including CMFB and V_{pcas} generation), 30 nA for the feedback transconductor, and 330 nA for the comparator. The comparator, S-R latch, and digital buffers (not shown) also consumed a small amount of dynamic power. During operation, the analog components consumed 1.54 μA on average. The decimation filters, discrete-time integrator and ΔΣ consume comparable amounts of power. Each channel drew an additional 2.13 μA from the digital supply to power the decimation filters, integrator, ΔΣ DAC, and for clock distribution. Both analog and digital circuits were powered from a 1.5 V supply, yielding a total power consumption of 5.5 μW.

To quantify the design's power and noise performance, we can calculate the noise efficiency factor (NEF) and the power efficiency factor (PEF). Furthermore, we can consider separately the front-end amplifier and the system as a whole. By considering only the power consumed

by the front-end OTA (1.05 μA at 1.5 V), and taking the bandwidth to be equal to the Nyquist rate, we calculate an NEF of 2.5, and a PEF of 9.4.

C. In-vivo Measurements

1) Comparison with Commercial System—Three sets of measurements were performed *in-vivo* to validate the performance of the circuits in a biomedical setting. All surgical procedures were approved by the Johns Hopkins Animal Care and Use Committee. In the first experiment, stainless-steel screw electrodes were implanted in the skull over the somatosensory cortex of a rat, and an additional screw was implanted over the occipital region to serve as a reference. Simultaneous intracranial EEG (iEEG) recordings were made with a commercial, bench-top neurophysiology system (Tucker-Davis Technologies, Alachua, FL), as well as the proposed circuits (Fig. 15(a)). Fig. 15(b) shows two 5-second clips of iEEG from a rat under isoflurane anesthesia. The signals obtained with the bioADC (red) were overlayed on the recordings from the reference system (blue). When deeply anesthetized, the iEEG displays a prominent burst-suppression waveform in which periods of quiescence are punctuated by high amplitude bursts of activity [33]; this pattern is observed in Fig. 15(b)(top). However, under light sedation, the iEEG becomes continuous and of lower amplitude. Fig. 15(c) compares the spectrograms recorded from the two systems. Power in each frequency bin was normalized to the median power over the entire recording.

2) Open-Loop Stimulation—We used the chip in a second experiment to demonstrate simultaneous sensing and stimulation capabilities. Illustrated in Fig. 16(a), we simultaneously stimulated the vagus nerve to artificially increase the parasympathetic input to the heart, and measured the resulting effects on heart rate by measuring the electrocardiogram. A male Wistar rat was anesthetized with 2% isoflurane in a 50:50 N2:O2 mixture through a nosecone. A ventral incision was made in the neck, muscles were retracted and the left carotid sheath was exposed. Then, the left cervical vagus nerve was carefully dissected from the carotid sheath. Fig. 16(a) illustrates the experimental setup. Electrical contact was made with the vagus nerve using a stainless steel, bipolar hook electrode. A single stimulator channel was connected to one of the hooks, and the other hook was connected to 1.5 V to bias the rodent and for the stimulation current's return path. The electrode was made from 250 μm stainless steel wire, with a 1 mm hook diameter, and 0.8 mm spacing (FHC, Bowdoinham ME), and had an impedance of 2 kΩ at 1 kHz. Biphasic pulse trains (cathodic first) were delivered through the electrodes with the following parameters: 250 μA amplitude, 50 μs us pulse width, and 10 s pulse train duration. The electrocardiogram (ECG) was measured differentially across the two forepaws using a single bioADC channel.

Figure 16(b) shows measured ECG before, during and after a 40 Hz stimulation train delivered to the vagus nerve. The heart rate responds almost immediately at the onset (black bar) and offset of stimulation. Increasing the frequency of VNS has been demonstrated to progressively slows heart rate [32]. Fig. 16(c) shows the calculated heart rate versus time as VNS frequency was increased. Each black bar indicates the onset of a 10 second train of stimulation, and annotated below the bar is the stimulation frequency. Stimulation frequency

was stepped up in 5 Hz increments from 5 Hz to 35 Hz; at 30 Hz the effect saturated at an approximately 30% decrease in heart rate.

3) Closed-Loop Stimulation—We used the proposed circuits to perform a closed-loop VNS experiment in one male Wistar rat. The surgical procedure was identical to the one above, except electrical contact with the vagus nerve was made with a tripolar micro-cuff electrode (Microprobes, Gaithersburg, MD). The cuff consisted of three 50 μm platinum/iridium contacts spaced 0.5 mm apart, embedded in a 300 μm diameter silicone rubber tubing. The impedance was 5 kΩ at 1 kHz.

This experiment demonstrated closed-loop control of cardiac rhythm. Fig. 16(c) illustrates the frequency of stimulation can be used to progressively slow cardiac rhythm. Therefore, we applied stimulus trains of constant amplitude and pulse width to the vagus nerve, and allowed the PC to autonomously modulate stimulation frequency such that the measured heart rate approached a user-defined target.

To accomplish this, as illustrated in Fig 17(a), the PC ran an R-wave detection algorithm to calculate heart rate in real-time, and implemented a proportional-plus-integral (PI) controller to modulate VNS frequency. The control loop minimized the error between the detected heart rate and a target set by the user.

Biphasic pulse trains (anodic first) were delivered through the electrodes with the following parameters: 110 μA amplitude, 225 μs pulse width (Fig. 17(a)). Two of the distally located electrodes were stimulated with adjacent stimulator channels, while the third, proximal electrode was used for the current's return path. For these experiments the analog supply voltage was increased to 1.8 V, to allow the rodent body bias to be at a higher potential. This provided an increase in headroom for the cathodic current source.

The target heart rate was set to a 10% decrease from baseline, and the system was allowed to run for ≈1200 seconds. Fig. 17(b) illustrates the measured heart rate and autonomously controlled stimulation frequency during the experiment. The difference between heart rate and target decreased over the course of 120 seconds. After a period of convergence, the mean heart rate was maintained within ± 10 bpm for the duration of the trial with one exception. During the experiment a paroxysmal arrhythmia was observed (two spikes in heart rate at ≈ t=1000). As illustrated in the inset, this was not artifactual. Due to the proportional gain in the controller this produced brief spikes in the stimulation frequency as well.

Fig 17(c) depicts the time-domain potential across one of the micro-cuffs during stimulation. Stimulation artifacts could be detected in the ECG recordings, and are depicted and annotated in Fig 17(d). Recordings were then time-aligned to all stimulation pulse onsets and averaged across the entire experiment. The extracted waveform illustrated in Fig. 17(e) has a peak-to-peak amplitude of 110 μV.

IV. COMPARISONS AND CONCLUSION

We have presented a low-power, low-noise, biopotential acquisition system with integrated stimulator [15] suitable for closed-loop electrocortical neuromodulation systems. Table II summarizes the recording front-end specifications of the reported circuits and compares the results with state-of-the-art designs. For fair comparisons across designs we use a "system-level" NEF that considers the current consumption of the entire recording chain including ADC. This design achieves the lowest system-level NEF compared with all works in Table II. The PEF is higher here than the design in [12] due to our relatively high supply voltage of 1.5 V compared with 0.5 V.

We also propose an additional figure of merit (FoM) for bioADC systems based on a traditional figure of merit in ADCs.

$$\mathrm{FoM}_{\mathrm{bioADC}} = \frac{\mathrm{Power}}{F_s \cdot 2^{\mathrm{ENOB}'}} \quad (6)$$

$$\mathrm{ENOB}' = \frac{20 \cdot \log_{10}\left(\frac{A_{fs}/\sqrt{2}}{V_{n,rms}}\right) - 1.76}{6.02} \quad (7)$$

This FoM allows fair comparisons between systems such as that proposed here and in [13] and more traditional systems by taking into account the effect of front-end noise and gain on the effective SNR in practice.

Specifically, the front-end amplifiers and back-end ADCs of typical biopotential acquisition systems are characterized separately. Moreover, it is common for the ADC to be over-designed in the sense that the quantization noise is much lower than the front-end amplifiers noise when referred back to the input. In this way, the process of digitization does not impact the noise performance and power efficiency. For example, a 10-bit ADC with a fullscale range 1 mV when referred back to the input would have a quantization noise level of 280 nV_{rms}. This is well below the noise level obtained in micropower neural amplifiers, hence, the ENoB in practice, when considering the entire signal chain, will be limited by the input referred noise of the front-end amplifier.

Note that our thermal noise level of 60 $\mathrm{nV}/\sqrt{Hz}$ is right in line with the state of the art; this is quantified by the low NEF. As ENoB is just a measure of signal to noise ratio, this means our ENoB will also be in line with the state of the art, and quantified with this figure of merit.

The bioADC presented here obtains an ENOB of 9 bits, with a dynamic range of 5 mV, which is much larger than the dynamic range of most biopotential signals. Therefore, the ENOB for signals of interest is lower due to the input-referred noise of the front-end OTA as explained above. For example, Fig. 10 illustrates that for a signal range of 1 mV_{pp}, an

ENOB of 7.7 is obtained. However, the high dynamic range has significant value. First, the circuits can be adapted for invasive LFP recordings which have amplitudes > 1 mV Second, EEG systems are plagued by all sorts of artifacts, from eyeblink, to scalp EMG, to movement artifacts. Increased dynamic range allows a certain safety margin to accommodate these artifacts and remove them non-destructively in post-processing.

SAR ADCs are typically the best choice for energy efficient analog-to-digital conversion. The work in Table II that achieves the best (lowest) FoM is a SAR ADC. In this case the FoM is driven low by the low power consumption despite a very high sampling frequency [34]. However, SAR ADCs are prone to aliasing distortion in the presence of high-frequency noise. This is of particular concern in bidirectional systems, as high frequency stimulation artifacts alias into the frequency bands relevant to biopotential sensing [35]. The oversampling in ΔΣ ADCs, as well as the inherent anti-aliasing properties of the continuous-time (CT) integrator make CT-ΔΣ ADCs particularly suited for this application. The integrated second-order decimator offers substantial improvement in resolution without the area and power expense of second-order noise shaping. While VCO based ADCs also provide inherent anti-aliasing, ΔΣ architectures offer enhanced linearity. Thus, the proposed system has a higher dynamic range and thus lower FoM compared with [12].

The proposed circuits were designed specifically for EEG/ECoG recording as demonstrated in Fig. 15. The major limitation in using the proposed circuit for spike recording is the power required to increase the sampling rate to one suitable to acquire action potentials. Typical commercial hardware sample at >20 kHz, and to achieve this sampling rate at the current 256 OSR, would require a 5.12 MHz clock rate. In the current implementation this would consume an unsuitable amount of power from the digital circuits.

Interestingly, the digital and analog circuits consume comparable amounts of power in this design. This could be addressed in two ways. First, two power domains could be utilized, a 1.5 V supply for the analog circuits and a <1 V supply for the digital circuits; minimal overhead in the form of level shifters would be the only requirement. Alternatively, further performance and energy efficiency improvements can be obtained by migrating the design to state-of-the-art 65nm technology. In this work a closed-loop neuromodulation system was demonstrated *in-vivo* using a PC to process the recorded data. However, the algorithms used (R-wave detection and PI controller) are suitable for on-chip implementation [36], [37]. Hence, merging on-chip R-wave and rhythm detection circuits and the PI controller with the recording-stimulation circuit should enable a fully integrated closed-loop neuromodulation platform.

Acknowledgments

Chip fabrication was provided though the MOSIS educational program.

This work was supported by the NIH grant RO1HL071568 to N. Thakor and the NSF EFRI-M3C grant 1137279 to G. Cauwenberghs. E. Greenwald was supported in part by an NIH training grant 5T32EB003383

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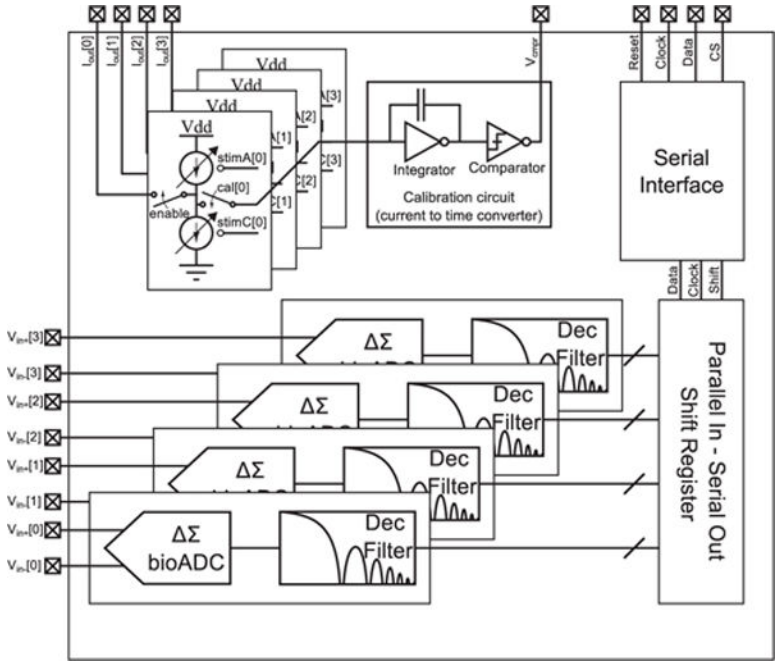

Fig. 1.

Overview of the proposed circuits. The designed chip contains four channels of recording and stimulation. An additional calibration circuit is used to match the anodic and cathodic current sources for charge balancing [15]. A serial interface facilitates communication between this chip and an external processor.

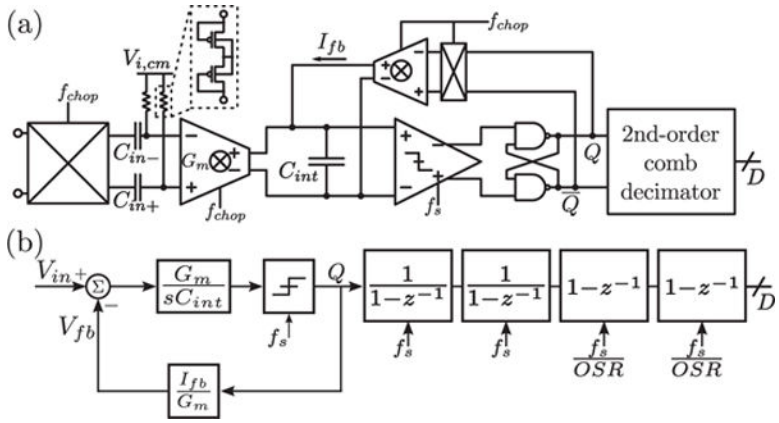

Fig. 2.

(a) Schematic of the system, consisting of a $G_m - C$ integrator, a latched comparator, a transconductor as a 1-bit DAC, and a decimation filter. Chopping switches before and within the OTA are used to reduce $1/f$ noise. (b) Block diagram representation of the system, with the DAC current referred back to the input. The second-order comb digital decimation filter implements two accumulators at the system clock f_s followed by two differentiators at the decimated clock f_s/OSR. It is realized in an alternative form for higher area and energy efficiency.

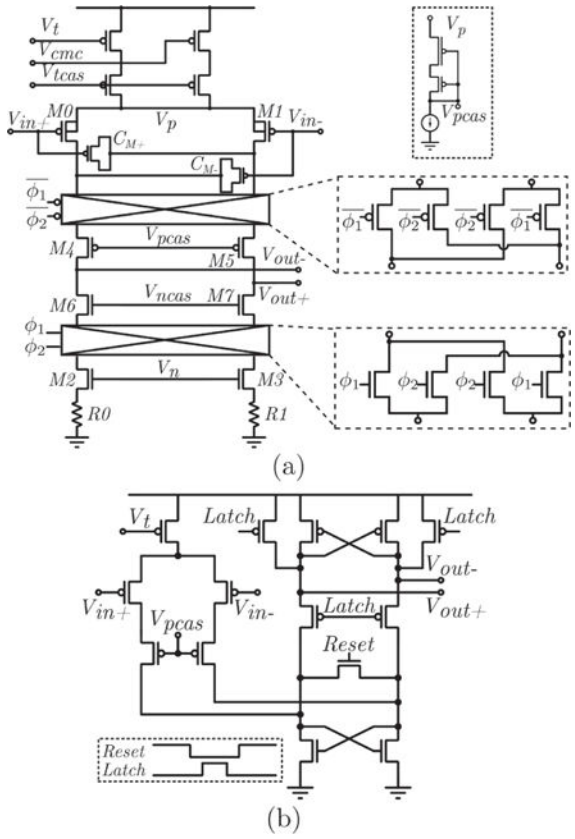

Fig. 3.

(a) Transistor-level schematics of the OTA and chopping switches. (b) Schematic and timing diagram for the latched comparator.

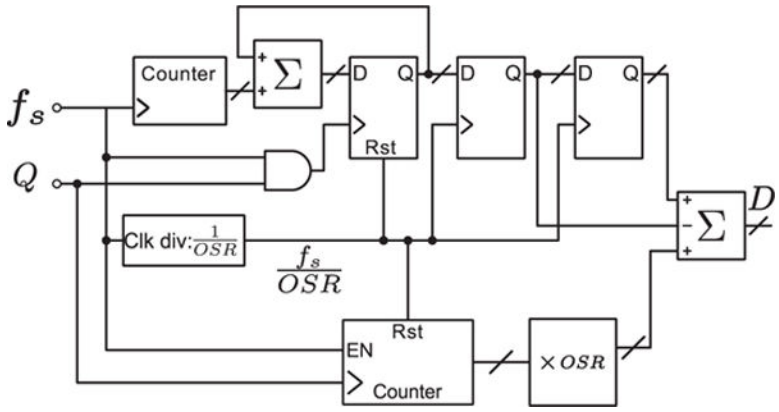

Fig. 4.
Decimation filter schematic [19].

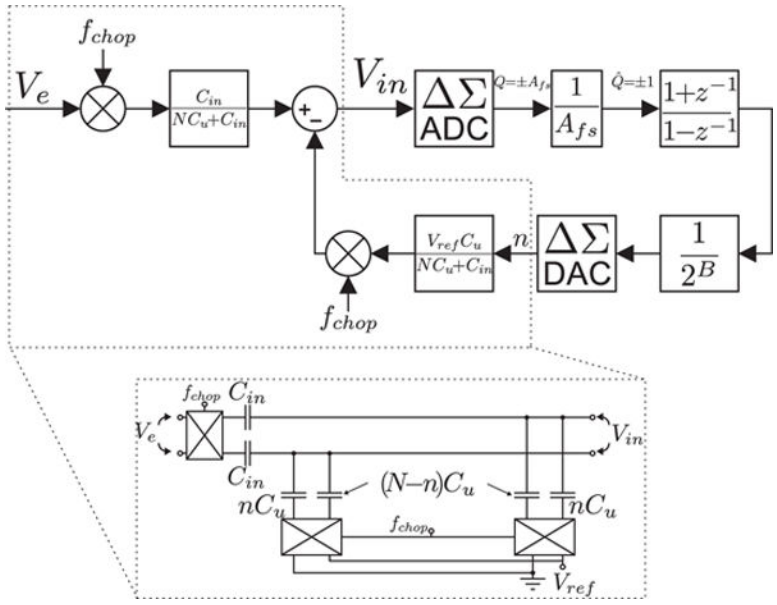

Fig. 5.
Servo-loop schematic

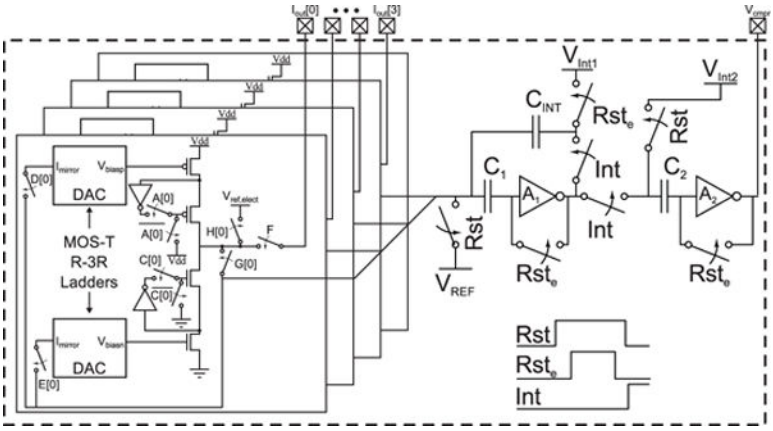

Fig. 6.

Schematic of the stimulator architecture used in this design [15]. Each channel contains a biphasic regulated current source with independent sub-binary radix DACs. Switches A and C turn on the anodic and cathodic current sources respectively. Switches D and E mirror the DAC currents to the calibration circuit to linearize the DACs using the procedure described in [15]. Switch F is used to disconnect the stimulator channel from the electrodes during calibration. Switch G routes the channel to the calibration unit, and switch H is used to short the electrode to a reference voltage ($V_{ref,elect}$) after each biphasic pulse to bleed off residual charge.

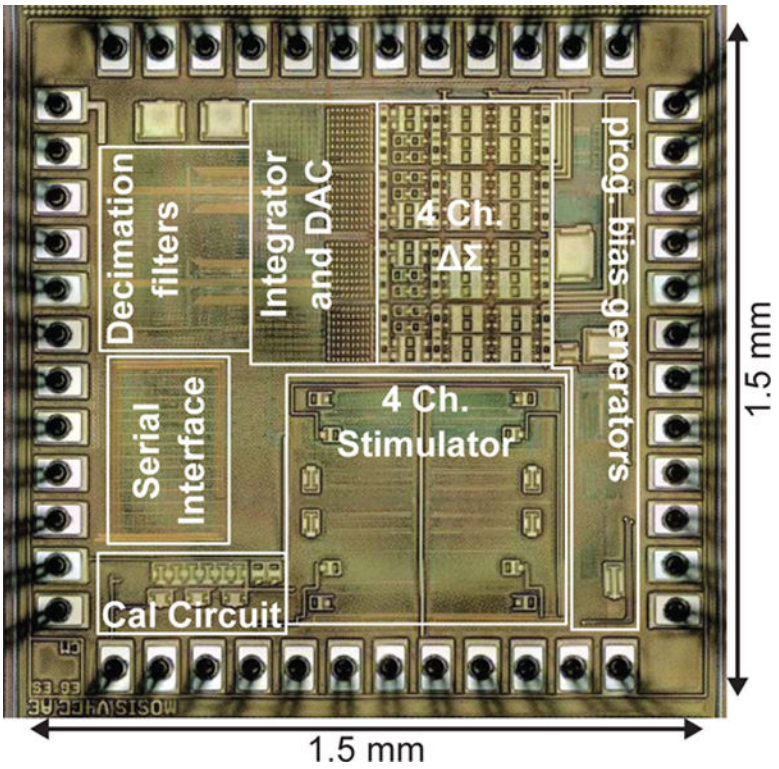

Fig. 7.
Micrograph of the fabricated circuits

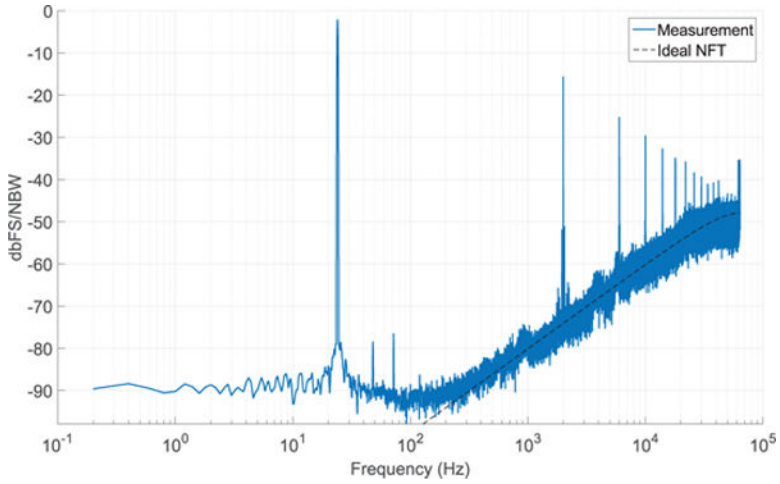

Fig. 8.

Raw output of bioADC for a 24 Hz tone, along with the ideal NTF for a first-order ΔΣ in black.

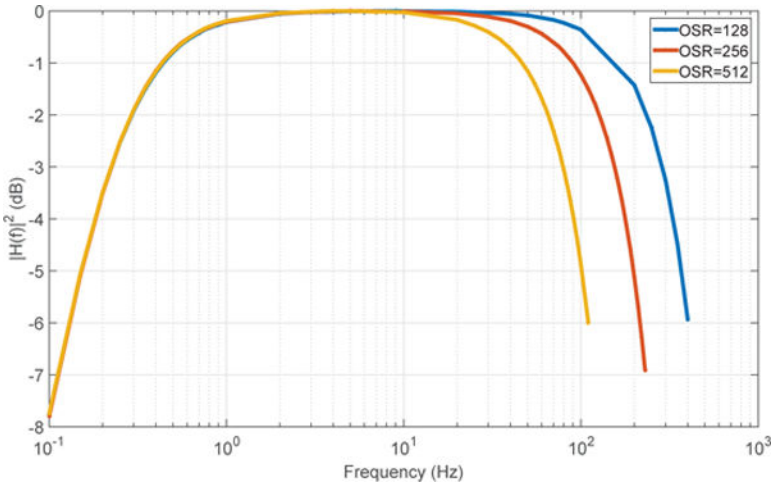

Fig. 9.
Frequency response for different settings of OSR

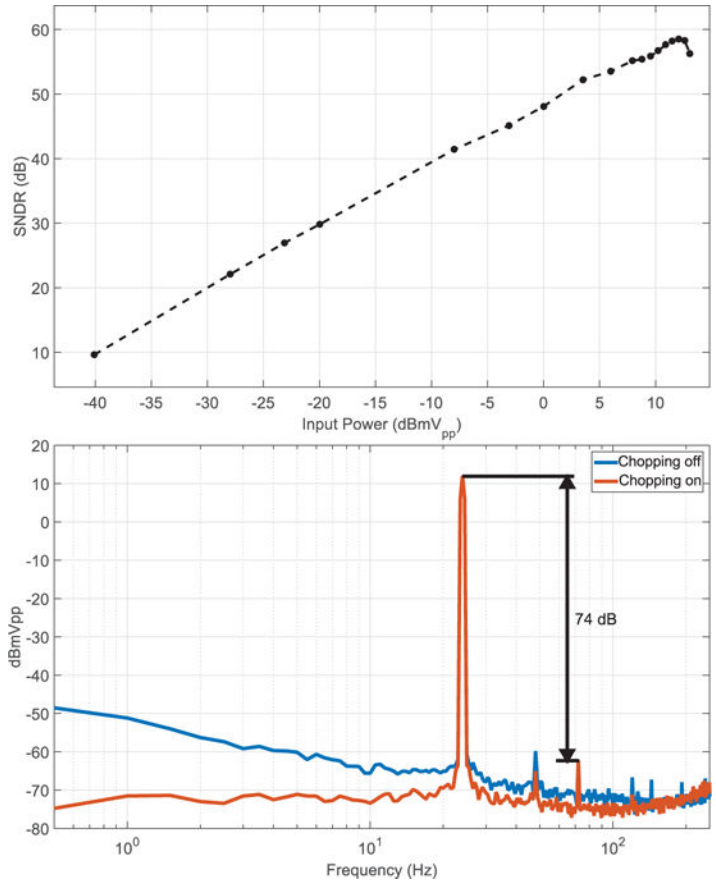

Fig. 10.

(top) Measured SNDR as a function of the input amplitude. (bottom) Output spectrum corresponding to the peak SNDR measurement ($4mV_{pp}$) with and without chopping

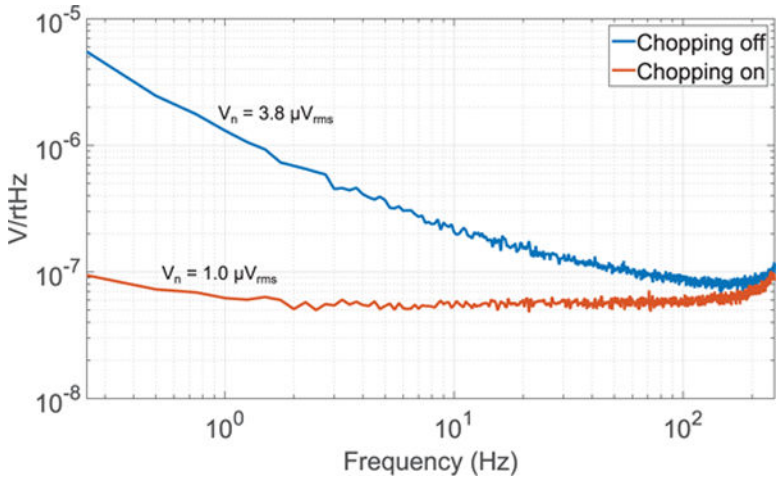

Fig. 11.
Input referred voltage noise PSD

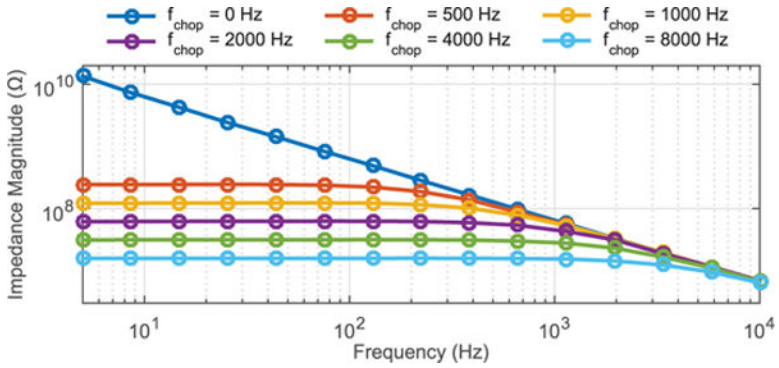

Fig. 12.

Differential input impedance as a function of frequency for different chopping frequencies.

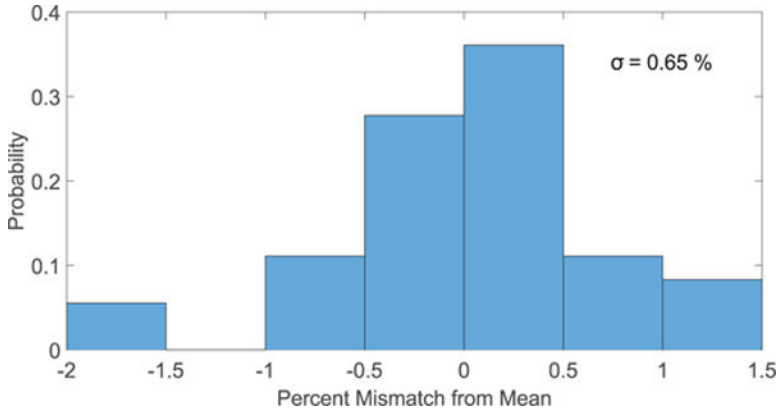

Fig. 13.

Percent variation in the gain across channels. Data accumulated from 9 chips for a total of 36 measurements. Data from each chip was normalized to the chip average.

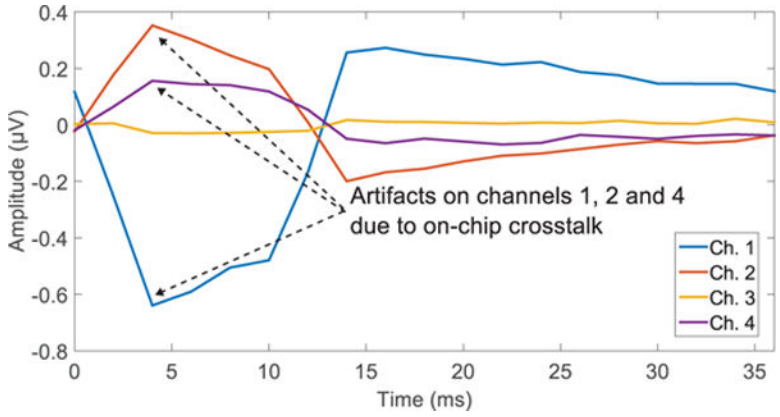

Fig. 14.

Crosstalk between the recording and stimulation blocks. Biphasic pulses with 10 ms cathodic-first pulse widths were applied to a resistive load (4.7 kΩ) on all four stimulator channels with the recording front-ends tied to ground. Recordings were time aligned to the onset of stimulation pulses (t=0) and averaged, extracting artifacts on channels 1, 2 and 4.

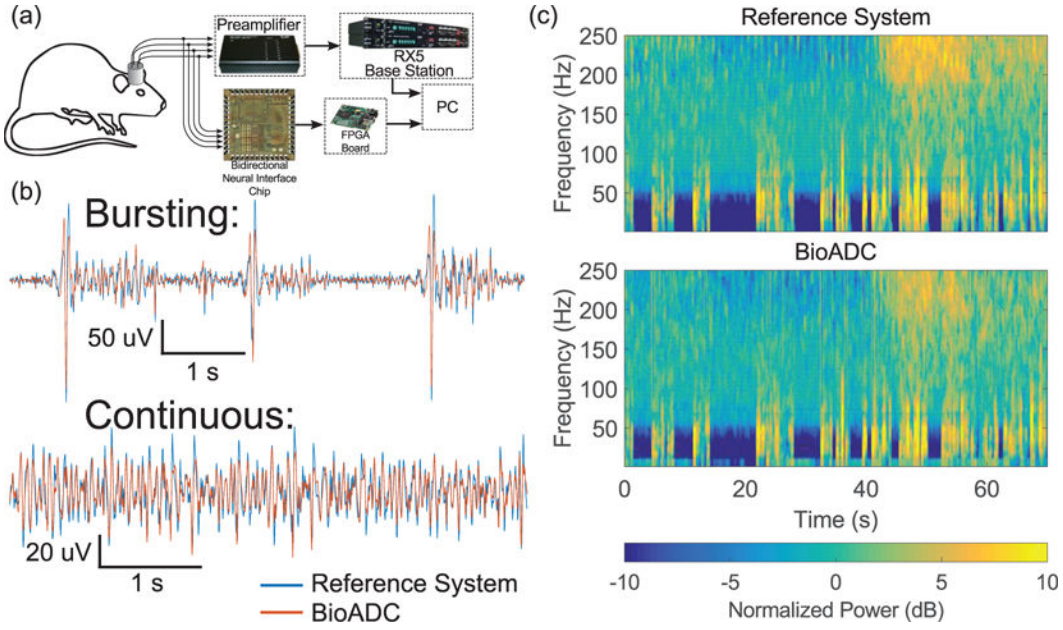

Fig. 15.

(a) Setup for in-vivo validation of the proposed circuits. A commercial electrophysiology workstation and the fabricated circuits were connected to screw electrodes implanted in a rat's skull, and the electroencephalogram was recorded while the rat was under anesthesia. (b) Comparison of time domain EEG. Burst suppression patterns (top) were recorded while the rat was heavily sedated. Continuous EEG was recorded during light sedation. (c) Frequency domain comparison.

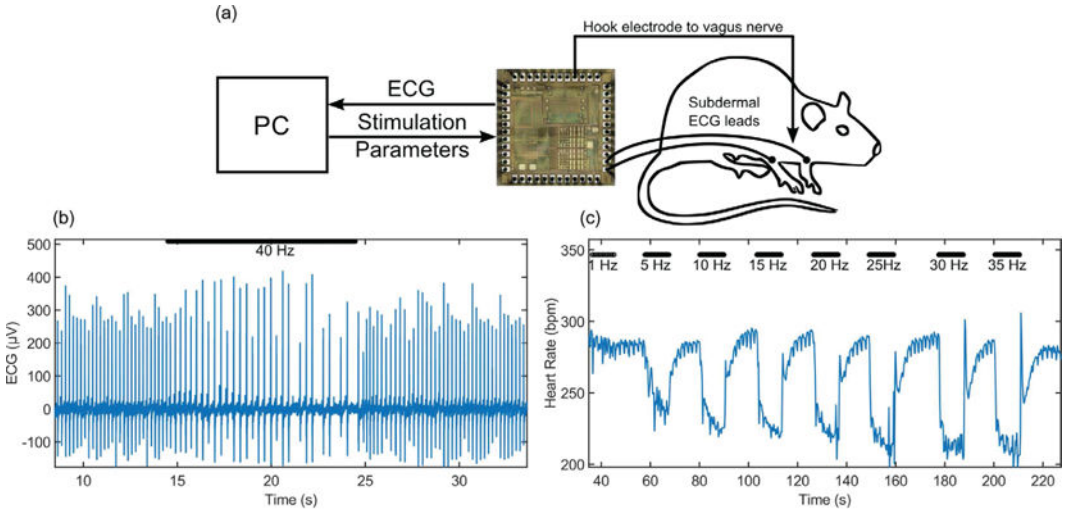

Fig. 16.

(a) Experimental setup to test the recording and stimulation capabilities simultaneously. A hook electrode was interfaced to the vagus nerve of an anesthetized rat and two subdermal needle electrodes were inserted at the left and right forepaws to measure resulting ECG changes.(b) Recorded ECG during vagus nerve stimulation (VNS). Black bar corresponds to the onset of VNS at a 40 Hz frequency. (c) Measured heart rate, extracted from recorded ECG, over time as VNS frequency was steadily increased. Over several trials we increased the stimulation frequency from 1 Hz to 35 Hz. The onset of each trial is indicated by the presence of a black bar, with the corresponding stimulation frequency labeled. Increases in stimulation frequency have a stronger effect on reducing heart rate as expected [32]

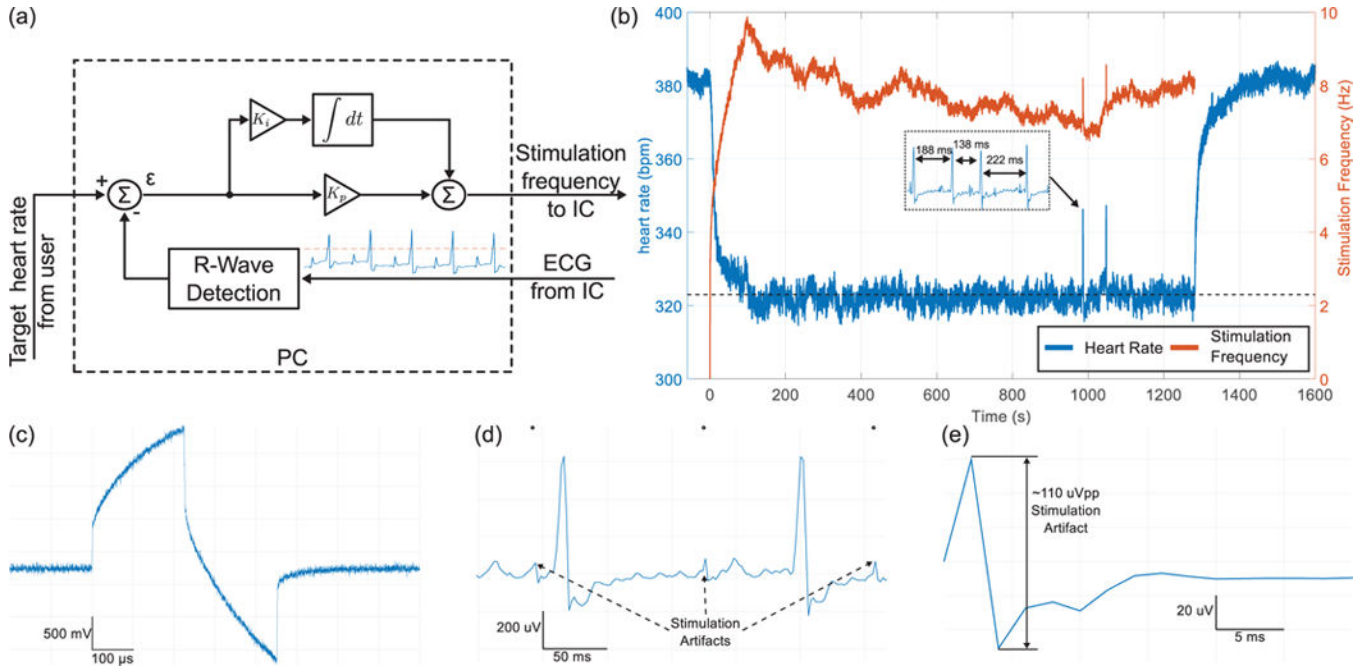

Fig. 17.

Closed loop neuromodulation of cardiac rhythm with the proposed integrated circuit (IC). (a) ECG recorded by the custom IC was streamed into a PC that calculated heart rate in real time, and implemented a PI controller that modulated vagus nerve stimulation frequency applied by the same IC such that the measured heart rate approached a target set by the experimenter. (b) Results of the closed-loop experiment. Heart rate (blue) and stimulation frequency (red) during a 1200 s closed-loop control trial. The target (dashed black line) was set to a 10% decrease from baseline. The inset shows the ECG and R-R intervals corresponding to the first spike in heart rate. The magnitude of the arrhythmia is attenuated due to smoothing applied to the heart rate data. (c) Potential recorded across a cuff electrode during a stimulation pulse. (d) Raw ECG during the closed-loop trial showing small stimulation artifacts. (e) Isolated stimulation artifact averaged across all stimulation pulses.

TABLE I

Input Impendence Across Chopper Frequencies at 76 Hz

Frequency (Hz)	Input Impedance (MΩ)
0 (chopper off)	827
500	237
1000	123
2000	62
4000	31
8000	16

TABLE II

Comparison of this work with prior art

Parameter	This Work	[12]	[34]	[13]	[10]	[8]
Year	2016	2015	2013	2010	2009	2008
Technology	180nm	65nm	130nm	0.5μm	0.5μm	0.5μm
Power/ch. (signal cond. + ADC) (μW)	5.5	2.3	10	20	72.6	14.2
Max Offset (mV)	±30 mV	±50 mV	AC-coupled	AC-coupled	AC-coupled	±45
Input Referred Noise (μV_{rms})	1.0	1.29	5.1	2.65	1.65	0.59
Bandwidth (Hz)	0.25–250	1 – 500	1 – 5k	1–1024	0.5 – 140	0.5 – 100
NEF (system level)	4.67	4.77	8.0	7.95	79.5	4.95
PEF (system level)	33	11	77	209	629	73.6
CMRR (dB)	97	88	75	–	76	128
ADC Architecture	ΔΣ	VCO	SAR	ΔΣ	ΔΣ	SAR
Sampling Rate per ch. (Hz)	500	1k	28k	512	500	1k
Resolution (ENOB)	9.4	–	7.6	9.5	8.8	10.5
SNDR (dB)	58.5	–	47.5[a]	59	55	64.9[a]
SFDR (dB	74	52	51	59	60	–
bioADC FoM (pJ/conv)	7.6	10.3	5.5	91.7	444	38.6
Stim Channels	4	–	64	–	–	–
Stim Supply Voltage	5	–	3.3	–	–	–
Max Current (mA)	0.25	–	1.2	–	–	–

[a] measurement for ADC alone