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Characterization of four readout circuits for an MR compatible, preclinical PET detector

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Abstract

We are building a high sensitivity preclinical PET/MRI insert using a highly multiplexed light sharing PET module. Each module incorporates four 19 × 19 arrays of 1 × 1 × 20 mm^3 LYSO crystals with dual-ended DOI encoding readout, requiring 32 readout channels for positioning and eight channels for timing. These constraints necessitate compact, robust electronics for digitization. We have characterized four linearized time-over-threshold circuits based on these detector requirements. The four circuits allow for high channel density and can digitize signals from highly multiplexed light sharing detectors. Each circuit digitizes one channel of a multiplexed SiPM array, yielding a binary output that interfaces directly with an FPGA. Using the optimal circuit, we have characterized the performance of a pair of PET modules. The four circuits were characterized based on linearity of the ^{22}Na photopeak positions and energy resolution at 511 keV, as well as separation of elements in a 10 × 10 array of 1.2 mm LYSO crystals coupled with a specular reflector. Practical measures of performance were comparable to those obtained with a DRS evaluation board, which served as a reference acquisition system. The ratio of the ^{22}Na photopeak positions was 2.0 for each circuit and the reference system, implying 20% saturation due to the SiPM. PET energy resolution of the optimal circuit was 11.8% FWHM for a single crystal versus 12.6% for the reference system, and crystals were equally well separated in all cases. PCBs implementing the optimal readout circuit were fabricated and used to construct two complete detector modules. Crystals in each of the four blocks in the module were well resolved, with a mean energy resolution of 24.4 ± 4.7%. Two modules operating in coincidence showed a single detector timing resolution of 3.0 ns, which is appropriate for preclinical applications.

Keywords

PET detector; dual-ended DOI; readout electronics; PET system development; PET/MRI

1. Introduction

We are developing a high sensitivity preclinical PET/MRI insert based on a block detector which we have previously characterized (Selfridge et al 2018). Briefly, the detector uses a 19

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× 19 array of 1 × 1 × 20 mm^3 lutetium-yttrium oxyorthosilicate (LYSO) crystals with dual-ended depth-of-interaction (DOI) encoding to maximize sensitivity without compromising spatial resolution. The crystal faces are polished and coupled with a diffuse reflector (Lumirror E60, Toray Industries, Tokyo, Japan) to promote DOI encoding. The front and rear faces are read out with asymmetric 4 × 5 and 6 × 5 silicon photomultiplier (SiPM) arrays, which are multiplexed into four channels each with an Anger resistive network. Four blocks are used to build a single detector module, 16 of which will be used to build the complete PET insert. Blocks within the module are arranged axially with a one crystal gap, yielding a 79 mm axial sensitive length and 100 mm block face-to-face distance.

A compact readout stack is necessary to digitize the high density of detector signals within the constrained geometry of a preclinical PET/MRI system. Digitization of signals within the MRI bore helps to minimize cabling complexity and reduce radiofrequency (RF) pickup. Furthermore, the readout must adequately handle signals from highly multiplexed light sharing detectors, where accurate positioning requires a wide digitizer dynamic range and must tolerate a high dark-current per channel. Four possible approaches to signal readout are:

- custom or commercial application specific integrated circuits (ASICs), potentially coupled to a field programmable gate array (FPGA)
- sample-and-hold circuits with low-speed analog to digital converters (ADCs)
- high speed free-running ADCs
- time-over-threshold (TOT) circuits with high speed amplifiers and shapers, coupled to an FPGA.

PET readout stacks based on ASICs are well suited to many modern applications where high channel density, low power consumption, and fast timing performance are all necessary (Anghinolfi et al 2003, Comerma et al 2013, Rolo et al 2013, Harion et al 2014, Shen et al 2018). ASICs can be designed to perform digitization, producing high-level representations of analog waveforms, or they may perform simplified operations like discrimination, yielding relatively unprocessed digital representations. Despite their merits, the primary drawback to ASICs is the cost and complexity of development and fabrication, limiting their ability to be incorporated into many small-scale projects (Thomke 1997). Although many commercial systems require the performance of dedicated ASICs, academic systems which excel in one domain can often make trade-offs in timing, sensitivity, or elsewhere to simplify readout (Weissler et al 2015, Goertzen et al 2016, Yang et al 2016). For these applications, cost and prototyping time may be better served by alternate solutions. For many preclinical or proof of concept systems, acceptable performance can be achieved with discrete electronic components. While a discrete configuration may increase noise, power consumption, and a circuit board size, the total cost is manageable for most research groups. Furthermore, the use of discrete components and FPGAs allows for better customizability, flexibility, and development time.

Low speed discrete ADCs, while affordable and accurate, are not always well suited for use with PET detectors. Conversion time, readout time, and complexity of sample-and-hold

circuits each contribute to detector dead time, cost, and performance. Many emerging research applications for PET systems are especially sensitive to dead time, including scans with short lived radioisotopes requiring high levels of activity (Wehrl et al 2013, Ouyang et al 2014). Complexity of the digital interface to discrete ADCs can also be a limitation at high channel densities, requiring three or more FPGA I/O pins per channel. Compared to TOT circuits requiring only a single I/O per channel, this increase in complexity may necessitate larger and higher density FPGAs, increasing system component and fabrication costs.

High density of readout channels makes high speed free running ADCs poorly suited for constrained geometries, despite their short dead time and excellent performance. This restriction is especially applicable to PET/MRI applications, where signal digitization within the MRI bore is favorable to eliminate long analog transmission lines, and where size and power consumption must be strictly constrained. Complexity of the digital interface to free running ADCs further contributes to system complexity, since each ADC requires several high speed serial lines to read out the large volume of detector data.

For both integrated and discrete readout circuits, a waveform's TOT is a common metric used to encode pulse amplitude. Readouts based on TOT measurement generally have simpler implementations compared to those relying on traditional ADCs, due to reduced component count and simplicity of the digital output signal (Grant and Levin 2014). The fundamental drawback to TOT measurement, however, is the nonlinear relationship between input amplitude and output pulse width due to the exponential pulse shapes produced by photodetectors (Orita et al 2011, Grant and Levin 2014, Yonggang et al 2014). TOT readouts can be linearized based on a lookup table or a correction factor, but this process requires calibration and increased back-end complexity. The shape of the input waveform can alternatively be linearized with respect to amplitude using various passive and active circuits, exchanging front-end simplicity for reduced back-end processing (Parl et al 2012). The sigma-delta ADC is one such circuit, producing a one-bit digital pulse whose length scales linearly with the integral of the input waveform. Implementations of a sigma-delta ADC coupled to LYSO and single SiPM diodes show linear behavior and energy resolution of 9.3% at 511 keV, which is sufficient for many PET applications (Zhao et al 2017, 2019, Cheng et al 2019).

While excellent performance has been demonstrated with TOT circuits for the readout of single diodes or small arrays, TOT readouts have not been broadly applied to the readout of large, highly multiplexed light sharing detectors. Such detectors require a readout circuit with a wide dynamic range, short conversion time, and high noise tolerance. Based on existing TOT designs, we have implemented four linearized TOT readout circuits which can accurately digitize signals from a large light sharing detector. The performance of each circuit was evaluated using signals both from a single SiPM diode and from large multiplexed SiPM arrays. These tests are intended to assess the basic performance of each circuit, as well as practical performance for common PET applications. Based on the optimal circuit we have designed and built two detector modules according to the constraints described above. The modules were operated in coincidence to demonstrate the expected system level performance.

2. Methods

A minimal sigma-delta encoding circuit, shown in figure 1, consists of an integrating amplifier and a comparator (Zhao et al 2017). The output of the comparator is fed back to the integrator input, supplying a constant current with polarity opposite of the input pulses. The output is a pulsed digital signal whose length scales in proportion to the integral of the input signal. The output may be sampled by an FPGA, which counts the duration of the digital pulses and may apply thresholds to reject dark counts or noise.

The minimal sigma-delta encoding circuit is useful for measurement of low noise current signals like those from single SiPM elements. When coupled to multiplexed SiPM arrays, dark counts contribute to quiescent current and create a high degree of baseline noise, obscuring waveforms and limiting the ability to detect true events. Based on the limited ability of the minimal sigma-delta circuit to digitize signals from multiplexed detectors, we have designed three modified circuits to reduce noise susceptibility in our applications (figure 2). The first modified circuit (SigDel1) resembles the minimal sigma-delta circuit, with an additional preamplifier and pulse shaping components to provide the appropriate polarity and shorten the pulse length. A short pulse length is critical to minimize the contribution of the waveform rising edge to the total measure TOT, which degrades linearity. A single transistor discharges the integrator, while a current divider sets the discharge rate (red). A diode may be placed parallel to the feedback capacitor to prevent the accumulation of negative charge in the integrator (grey, dashed). The second circuit (SigDel2) replaces the red feedback loop used in SigDel1, which connects the output of the comparator to the negative input of the integrator, with a constant current source (blue). This constant current source causes the integrator to discharge linearly. Unlike SigDel1, SigDel2 has the benefit that a small threshold can be used at the output comparator to reject small signals. The third circuit (SigDel3) combines these two approaches, using feedback from the comparator as a primary source of discharge following a scintillation event, and a current mirror to discharge small signals which do not exceed the threshold.

The fourth circuit uses a peak detector (figure 3) to create a similar linearized TOT encoding of the input pulse by a different approach (Horowitz and Hill 1994, Olcott and Levin 2008). The preamplifier shapes the signal and boosts gain, while the second buffer offsets the waveform by the diode voltage drop. The maximum voltage of the waveform is then captured as the voltage across the capacitor at the input to the third buffer. The series diode prevents the capacitor from discharging, except through the resistor to −5 V. This resistor could be replaced by a constant current source to improve linearity, but provides an adequate encoding for small signals. The third buffer drives the comparator, producing the digital output. A small positive value for V_{thresh} helps to reduce the frequency of noise triggers. In contrast to the sigma-delta circuits, the width of the output of the peak detector scales in proportion to the maximum amplitude of the input, rather than the integral.

Each analog front-end yields a one-bit digital output, the length of which scales with energy of the input pulse. Each circuit used the AD8056ARMZ (Analog Devices, Norwood, MA, USA), a dual-channel high speed amplifier, and the LT1721CGN (Linear Technology, Milpitas, CA, USA), a quad-channel high speed comparator. Digital signals were measured

using a CMod-A7 development board (Digilent, Pullman, WA, USA), which includes an Artix 7 FPGA (Xilinx, San Jose, CA, USA) and interfaces with a host computer over USB. To determine the length of each digital pulse, the FPGA sampled the input with a 500 MHz clock on both rising and falling edges, achieving an effective 1 GHz sampling rate. List-mode single event data encoding energy were transferred to the host computer over a high-speed USB-UART interface, where they were used to characterize each circuit based on energy resolution and linearity of single crystal ^{22}Na energy spectrum and quality of flood histograms generated with an Anger multiplexed SiPM array.

2.1. Single crystal measurement

A single 3 × 3 × 20 mm^3 lutetium fine silicate (LFS, Zecotek, Richmond, Canada) crystal was wrapped with Teflon tape and coupled with optical grease (BC-631, Saint Gobain, Courbevoie, France) to a single 3 × 3 mm^2 Sensl J-series SiPM (MicroFJ-30035-TSV, Sensl, Cork, Ireland). The SiPM was biased at 29.5 V, about 5 V over breakdown, and the detector was irradiated with an approximately 30 uCi (1.1 MBq) ^{22}Na point source at 50 mm distance. The SiPM signal was connected to the input of each of the four circuits, yielding a count rate of approximately 2.7 kcps. Approximately 1 million single events were acquired, and energy values were used to calculate a histogram. Energy resolution was calculated by fitting the 511 keV photopeak with a Gaussian function. Compared to LYSO, LFS has slightly higher light output although both have similar energy resolution at 511 keV and non-proportional light yield (Grodzicka et al 2011). Based on these similarities, we expect that the circuit performance observed with LFS will hold for LYSO.

To verify that any observed saturation originated from the SiPM rather than the readout, we performed a similar acquisition with a domino ring sampler (DRS), using the DRS4 chip and the version 5.1 evaluation board (Paul Scherrer Institute, Switzerland) (Ritt et al 2010). The SiPM signal was amplified and connected to the 50 Ω input of the DRS module, which was used to acquire 10 million events at 1 GS s^{-1} sampling rate. Energy was calculated as the integral of the waveform. The 511 keV and 1.275 MeV ^{22}Na photopeak positions were estimated for each of the five acquisition modes by fitting a Gaussian function, and the ratio of the two positions was used to estimate SiPM saturation.

2.2. Flood histogram measurement

A 10 × 10 array of 1.2 × 1.2 × 20 mm^3 pitch LYSO (Crystal Photonics Inc. Sanford, Florida, USA) crystals with rough lapped surface and specular reflector (ESR, 3M, Saint Paul, MN, USA) was coupled to a 5 × 6 array of SiPMs (MicroFJ-30035-TSV, Sensl) with a 1.59 mm thick, 25.4 × 25.4 mm^2 BK-7 glass light guide (Esco Optics, Oak Ridge, New Jersey, USA) Selfridge et al (2018). Edges of the light guide were polished. Optical grease was used to couple both the crystal and SiPM arrays to the light guide. The SiPM array was biased at 29.5 V and multiplexed into four corner channels with an Anger resistive network, where charge from each SiPM was divided among four resistors with values selected in proportion to the location in the array (Siegel et al 1996). Four readout channels, labelled A, B, C, and D, were used to digitize the amplitudes of each corner signal. Position was calculated as:

$$X = \frac{A + B}{A + B + C + D}, \; Y = \frac{B + C}{A + B + C + D}$$

X and Y values from all events were used to calculate a flood histogram and quantify crystal separation for each readout. A best-case acquisition was again performed with the DRS, to estimate the best possible flood quality for the setup. For each acquisition, the detector was irradiated side-on with an approximately 30 uCi (1.1 MBq) ^{22}Na point source at 50 mm distance. Single events were acquired for five minutes without collimation and used to generate flood histograms.

A figure of merit (FOM) was used to quantify crystal separation for each circuit (Lau et al 2010). The FOM was calculated as the average peak full width at half maximum (FWHM) in the X and Y directions for each crystal, divided by the mean distance between a crystal and each of its neighbors. Smaller FOM values indicate better crystal separation.

2.3. Detector module performance measurement

Two detector modules incorporating the SigDel3 circuit where constructed and used to characterize the expected performance of the proposed PET insert. A single detector module is shown in figure 4. The detector is described in (Selfridge et al 2018), with minor modifications to improve packing and reduce size. Briefly, acrylic light guides were cut to fit the dimensions of the SiPM arrays, and surfaces were coupled with silicone elastomer (SYLGARD 184, Dow Chemicals, Midland, MI, USA). Each module contained 32 readout channels used for position and energy estimation, and eight channels for timing estimation. The modules were built with MR compatible components and electronics, minimizing ferrous material near the imaging volume. Digital outputs of the positioning and timing channels were read-out by a custom Artix-7 FPGA board within the module. The FPGA packetized the front-end data into single events, transmitting them to a second back-end FPGA with a custom serial interface via a pair of Cat-6 ethernet cables, which were also used for power, clock, and reset distribution. Three data lanes were used for data transmission at 100 MHz. The back-end FPGA multiplexed data from the two modules, transmitting them to a workstation over ethernet.

Two timing channels were used for each block, corresponding to the front and rear arrays. The earliest detected signal was used for timing estimation for the whole block. The analog timing signal was summed from the four corner signals and was not shaped or linearized. To prevent timing violations in the FPGA firmware, the sampling clock was slowed to 300 MHz, yielding a best-case TDC timing resolution of 1.6 ns. Bias voltage for SiPM arrays within the module was set globally, although onboard DACs could potentially be used to set the bias for each block independently to compensate for variations in temperature.

To acquire data, the two modules were mounted on laser-cut acrylic rings which fixed the modules in opposition. The face-to-face distance of the modules was approximately 10 cm, based on the expected geometry of the proposed PET insert. A ^{22}Na point source was placed approximately midway between the modules, and singles data were acquired for five minutes and sorted to coincidences off-line. Singles data were used to define crystal lookup-

tables, and to assess per-crystal energy resolution. DOI performance was not assessed for the modules, but a detailed characterization for this detector geometry is given in (Selfridge et al 2018). Briefly, DOI position can be calculated as the energy of the front array divided by the summed energies of the front and rear arrays. Energy is calculated as the sum of the four positioning channels.

3. Results

3.1. Single crystal measurement

Figure 5 shows ^{22}Na energy spectrum for each of the circuits. The peak detector showed the poorest energy resolution, with a value of 17.5%. The sigma-delta circuits showed similar energy resolutions around 12.0%. Figure 6 shows the saturation of each circuit and of a DRS evaluation board. The DRS evaluation board showed an energy resolution of 12.6%, similar to the sigma-delta circuits. The ratio of the two photopeaks was between 2.01 and 2.04 for each of the four circuits and the DRS, compared to the true ratio of 2.50 for a detector without saturation, indicating approximately 20% SiPM saturation at 1.275 MeV.

3.2. Flood histogram measurement

Figure 7 shows flood histograms for each of the circuits, as well as the DRS evaluation board. Flood histograms are displayed with upper and lower energy thresholds of approximately 350 to 650 keV, and identical X and Y scales. All crystals were resolved for each of the circuits, with mean FOM ranging from 0.391 for SigDel 1 to 0.322 for SigDel 3.

3.3. Detector module performance measurement

Crystal elements within the two modules were well resolved, although some edge crystals in the axial direction were blurred due to the reduced axial extent of the SiPM arrays (figure 8). As above, flood histograms are displayed with a 350 to 650 keV threshold. Within the center two blocks of each module, the mean per-crystal coincidence energy resolution was 24.4 ± 4.7%, and the FWHM timing resolution was 4.3 ns, or 3.0 ns per detector (figure 9).

4. Discussion

4.1. Single crystal measurement

The circuits accurately digitize signals from single SiPM elements, with each spectrum having a clearly resolved photopeak, Compton edge and backscatter peak. Low energy features are most distinct for the DRS and peak detector, although they are still present for the sigma-delta circuits. Unlike other circuits, the peak detector has a large noise peak near zero energy. Saturation of each circuit is nearly identical, indicating a common cause of light collection at the SiPM rather than the electronics. The light sharing configuration in the detector module does not use direct coupling, limiting the impact of SiPM saturation for our proposed application.

4.2. Flood histogram measurement

Crystals in the flood histograms for each circuit are well separated, with a small degree of warping due to the charge sharing resistive network. Based on the Anger logic used for positioning, some degree of warping and blurring may result from nonlinearity of the TOT circuit, which has previously been characterized for related TOT circuits (Olcott and Levin 2008, Zhao et al 2017). This nonlinearity can cause energy to influence the positioning of events from a single crystal, and can cause the relative position of crystals within the array to deviate from the normal grid-like pattern. These effects are strongest for edge crystals, where the multiplexing network produces analog signals with large differences in amplitude. Non-ideal behavior of the constant current source used in the TOT circuit can contribute to nonlinearity, especially for the small signals necessary for localizing edge crystals (Olcott and Levin 2008).

4.3. Detector module performance measurement

Compared to measurement with the smaller 10 × 10 crystal array, the 19 × 19 array covers a larger fraction of the total SiPM array area, requiring the readout circuit to operate over a wider range of signal amplitudes. This configuration is more sensitive to linearity of the TOT circuit, since independent channels must maintain the relative signal amplitudes for each crystal over a wider dynamic range. Despite differences in the configuration, both center and edge crystals in the complete module are well separated without obvious positioning errors.

Differences in the energy resolution and photopeak position between the two modules may result from variation in the assembly process, causing differences in light collection. Other possible factors could be minor differences in the SiPM array bias voltage due to the behavior of system voltage regulators. Despite these differences, we do not expect the small change in energy resolution or light collection to impact system performance.

Two major contributors to the timing resolution of the detector module are low light output of the DOI encoding crystal array and the limited performance of the TDC. High aspect ratio arrays used for dual-ended DOI encoding generally have timing performance between 1.0 and 1.5 ns, even with high performance readout electronics (Kolb et al 2014, Du et al 2018). Together with the 1.6 ns due to the TDC sampling interval, these factors account for approximately half of the 3.0 ns observed single detector timing uncertainty. Other possible contributors include output capacitance of the large area SiPM array, analog electronic noise, the lack of time walk correction, and clock jitter between modules.

4.4. Readout limitations

Each of the four readout circuits can digitize a diverse range of signals, although each has unique limitations. Measurement of waveforms with an undershoot, for example, is not possible with the sigma-delta circuits due to integration of the signal. The peak detector, by contrast, can encode signals with undershoots. The maximum output pulse length, which dictates detector dead time, also impacts the optimal circuit for an application (Olcott and Levin 2008). The sigma-delta circuits can generally be adjusted to yield pulses shorter than one microsecond, while we found that peak detector requires pulses exceeding two

microseconds to achieve acceptable crystal separation and energy resolution. Finally, ease of implementation influences the optimal circuit for an application. Despite its slightly greater complexity, we found SigDel3 to be the most reliable circuit, simplifying the process of component selection compared to SigDel1 and 2. Furthermore, SigDel3 decouples various aspects of the shaped waveform like baseline noise and pulse discharge rate, allowing independent optimization of circuit components. These reasons contributed to our choice to incorporate SigDel3 into the larger module.

Although we have not independently evaluated timing performance of the four circuits, timing pickoff can occur at any section of the readout, as is demonstrated with the detector module. Timing pickoff can also be performed using any of the positioning channels, although performance may suffer due to position-dependent amplitude of the signals. To measure signal arrival time, various classes of time-to-digital converters (TDCs) can be implemented directly in FPGAs. Direct sampling of the input signal can reach 1 ns precision using a 500 MHz clock sampled on both rising and falling edges (Zhao et al 2017). While 1 ns is sufficient for applications with a small FOV, many FPGAs will suffer from severe timing violations at this clock rate, necessitating a slower driving clock. Tapped delay line TDCs are an alternative which can reach accuracies below 13 ps, although portability may be limited in some cases (Won et al 2016, Sui et al 2017).

A second relevant aspect of any TOT readout circuit that we have not directly addressed is count rate performance and pileup rejection. For the circuits described, pileup events appear as a single event with summed energy. In many cases the event will be pushed above the valid energy window and can be rejected. Nevertheless, as with any readout a fraction of pileups will be indistinguishable from valid single events, contributing to increased energy resolution and degraded crystal separation. This behavior can be mitigated by reducing the discharge time of the integrator, in turn shortening the window associated with each event and reducing the probability of pileups.

5. Conclusion

We have demonstrated the use of four linearized TOT encoding circuits capable of reading out highly multiplexed, light sharing PET block detectors. Three of these circuits were based on a sigma-delta ADC, modified to improve its reliability and expand the range of potential applications. The fourth was based on a peak detector, which encodes amplitude as the width of a digital pulse. Each circuit has a small enough footprint to be directly incorporated into a detector stack, allowing data to be processed and serialized with minimal signal routing and cabling. The simple digital interface for each circuit allows digital back-end electronics to be minimized, and for a single FPGA to process dozens of channels simultaneously. The SigDel3 circuit, when used to read out signals from a single crystal, yielded energy resolution of 11.8% and did not indicate any saturation beyond that of the SiPM. When used to read out a 10 × 10 array of 1.2 mm pitch LYSO crystals, elements were well separated with a mean FOM of 0.322, comparable to that of the reference acquisition system.

Performance of the complete detector module lends further validation to the optimal readout circuit. The 19 × 19 array of 1.0 mm crystal elements was well separated, with mean energy

resolution of 24.4 ± 4.7% and timing resolution of 3.0 ns, both of which are appropriate for preclinical applications. Crystal separation and energy resolution were consistent between the two modules, indicating reliable system-level performance. Based on these results, we expect both the analog digitization electronics and modular detector stack to be well suited for use in a high sensitivity PET/MRI insert.

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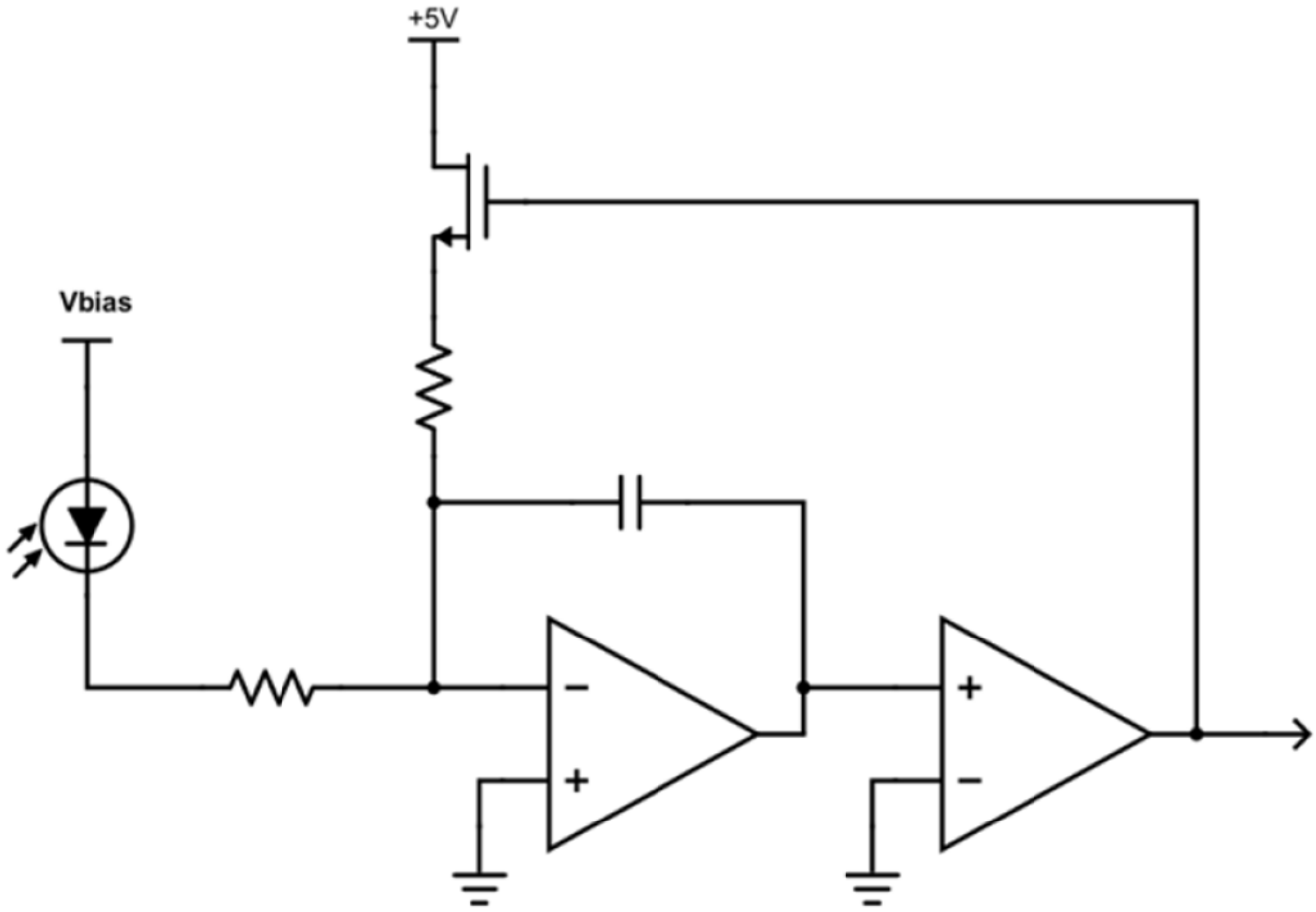

Figure 1.
A minimal sigma-delta encoding circuit, coupled to an SiPM.

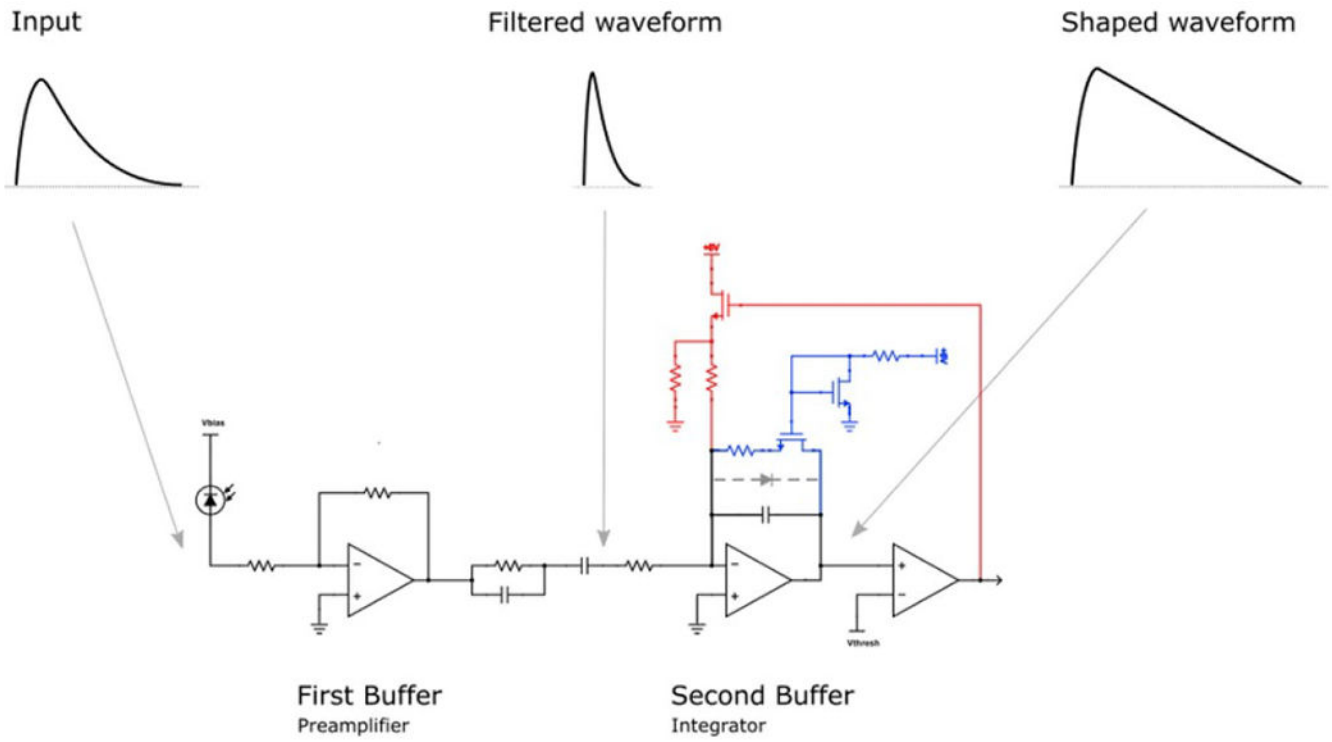

Figure 2.

Three modified sigma-delta encoding circuits were built, with both passive and active integrator discharge. Black components were common across all circuits. SigDel1 included only red components. SigDel2 included only blue components. SigDel3 included all components.

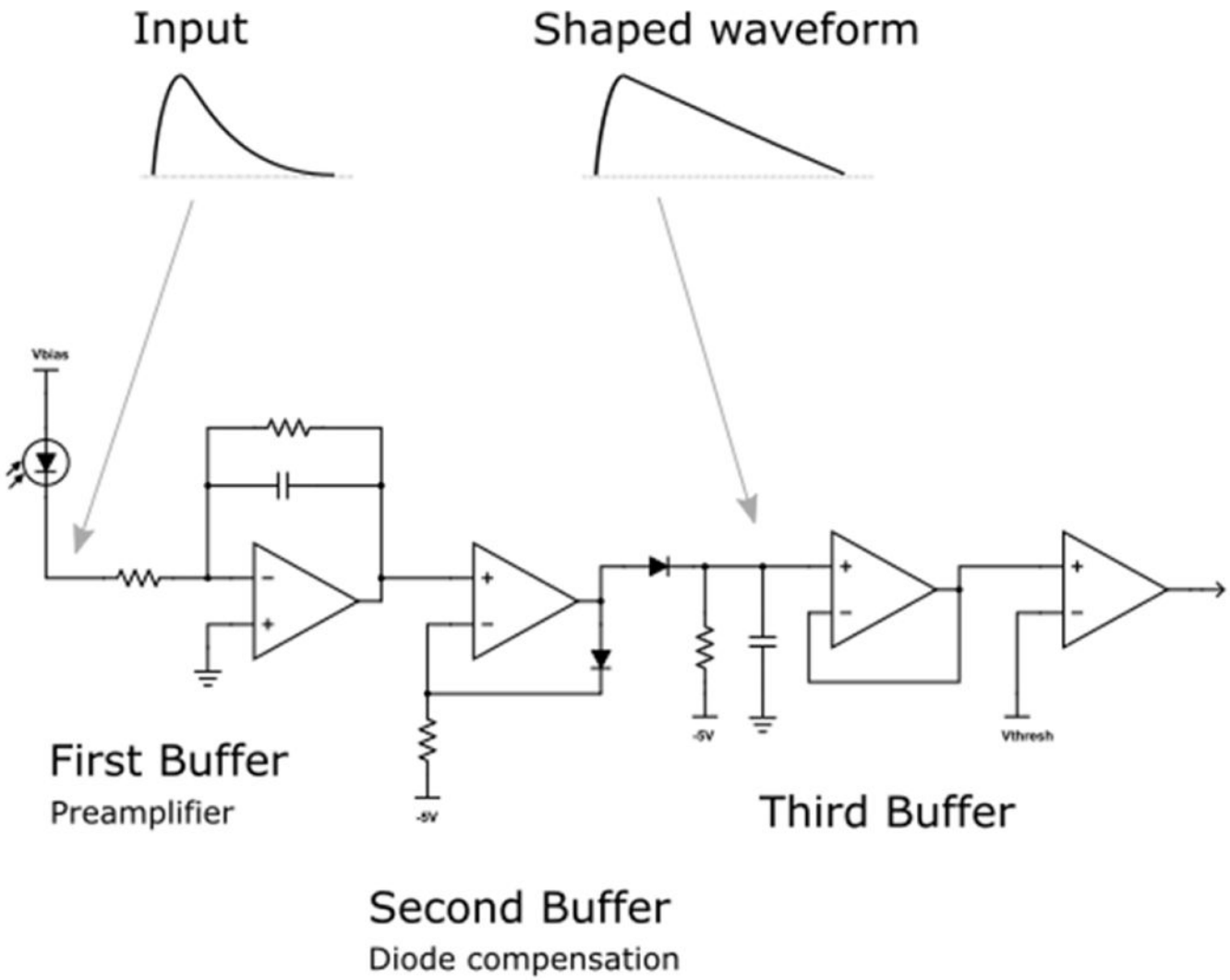

Figure 3.
An alternative linearized TOT encoding circuit, using a peak detector.

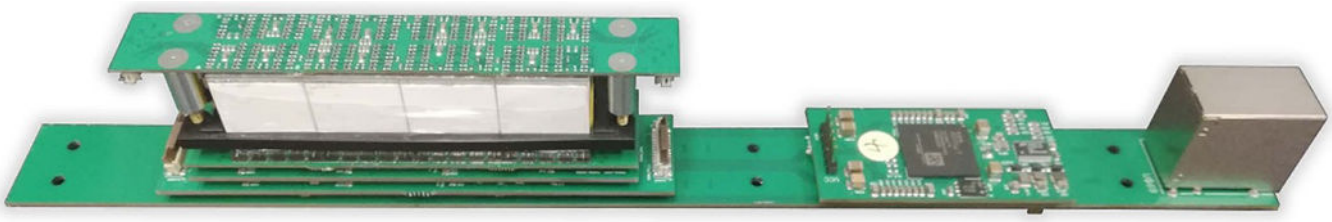

Figure 4.
A single detector module with four crystal blocks, front and rear SiPM arrays, analog readout board, FPGA board, and dual RJ-45 connectors for powering and communication.

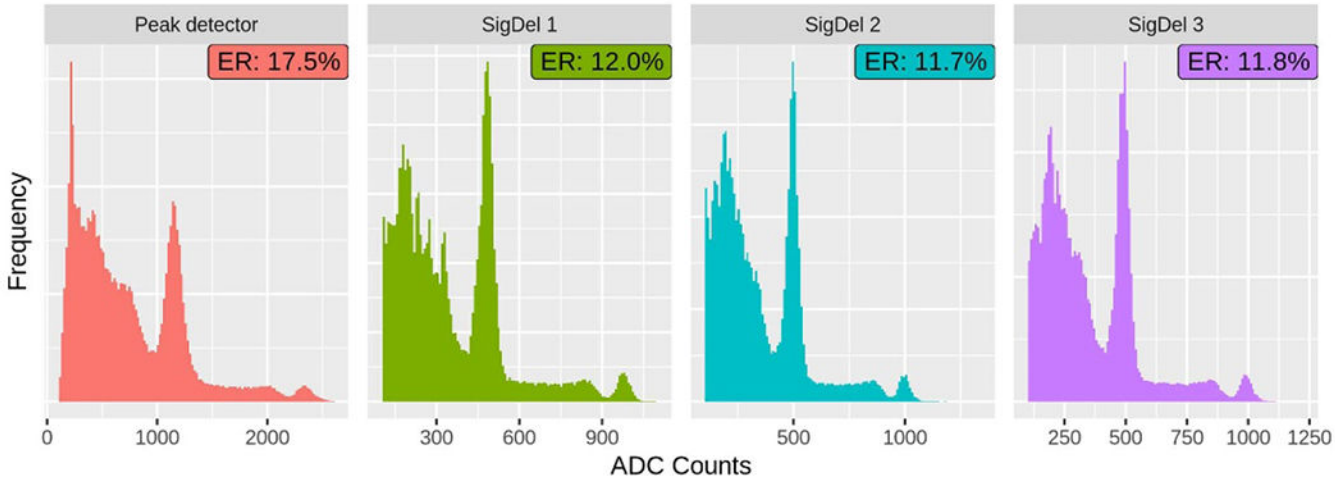

Figure 5.

^{22}Na energy spectra and energy resolution (ER) for each of the four ADC circuits, coupled to a single crystal and single SiPM element. Each ADC count corresponds to 1 ns duration of the digital output pulse.

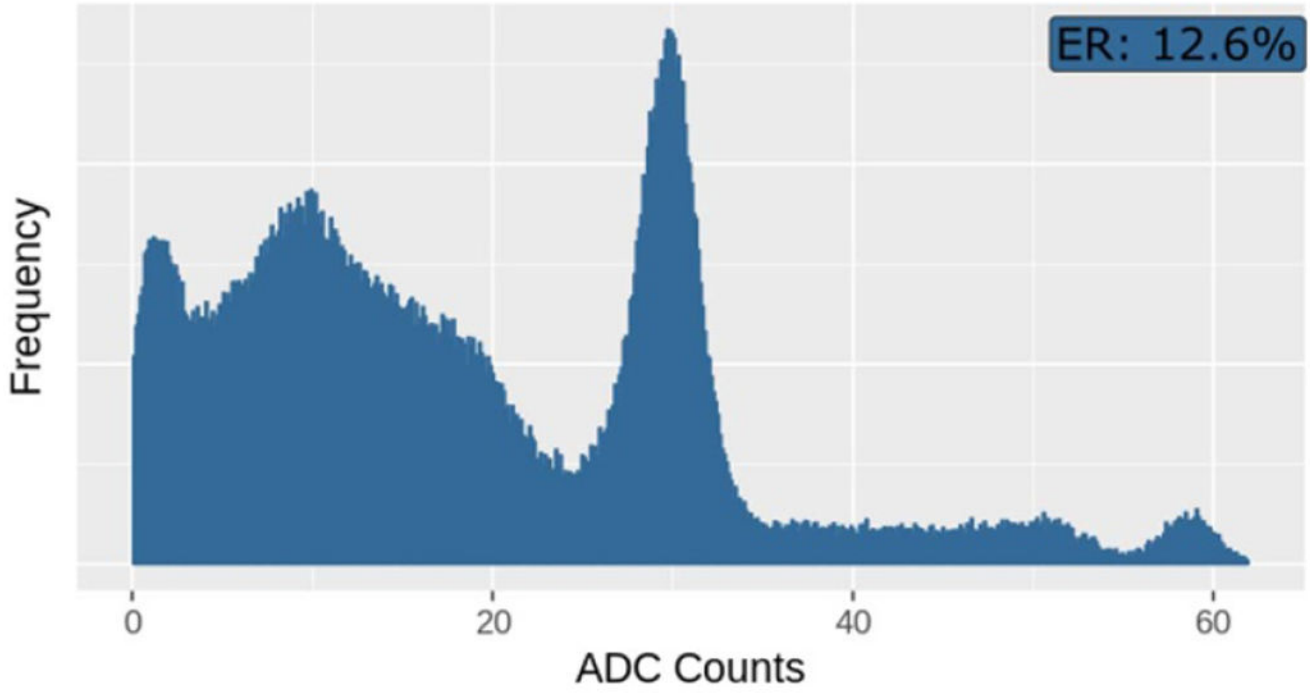

Figure 6.

Left: DRS evaluation board energy spectrum. Right: linearity of each acquisition circuit, comparing the measured amplitude (ADC counts) at 511 keV and 1.275 MeV. The true ratio should be 2.50.

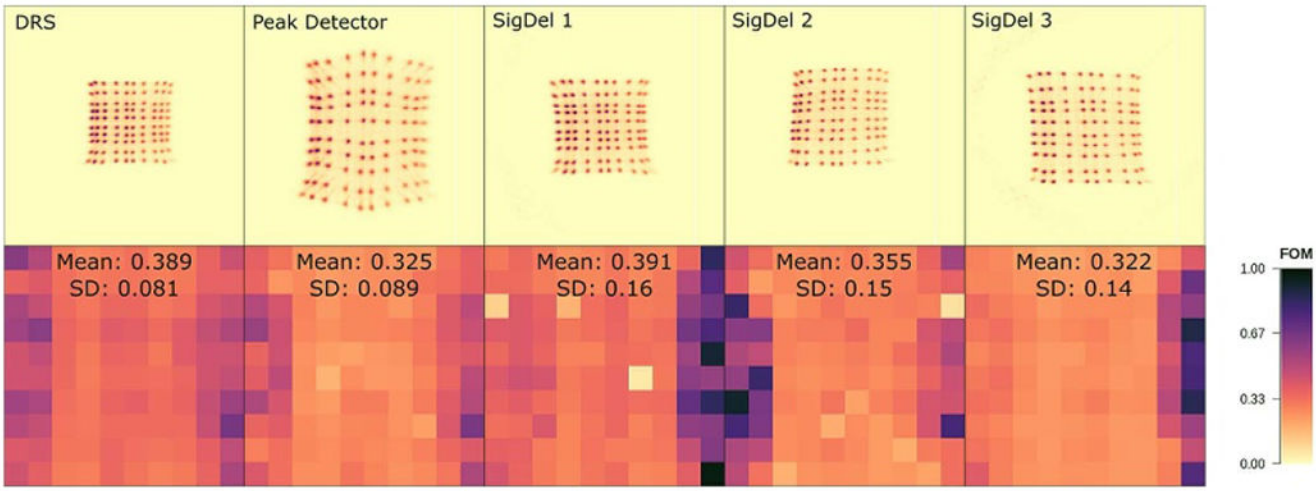

Figure 7.

Top: Flood histograms for each circuit when reading out a 10 × 10 LYSO array coupled to an Anger multiplexed SiPM array. Nonuniform count density results from side-on irradiation. Bottom: Crystal FOM for each of the circuits.

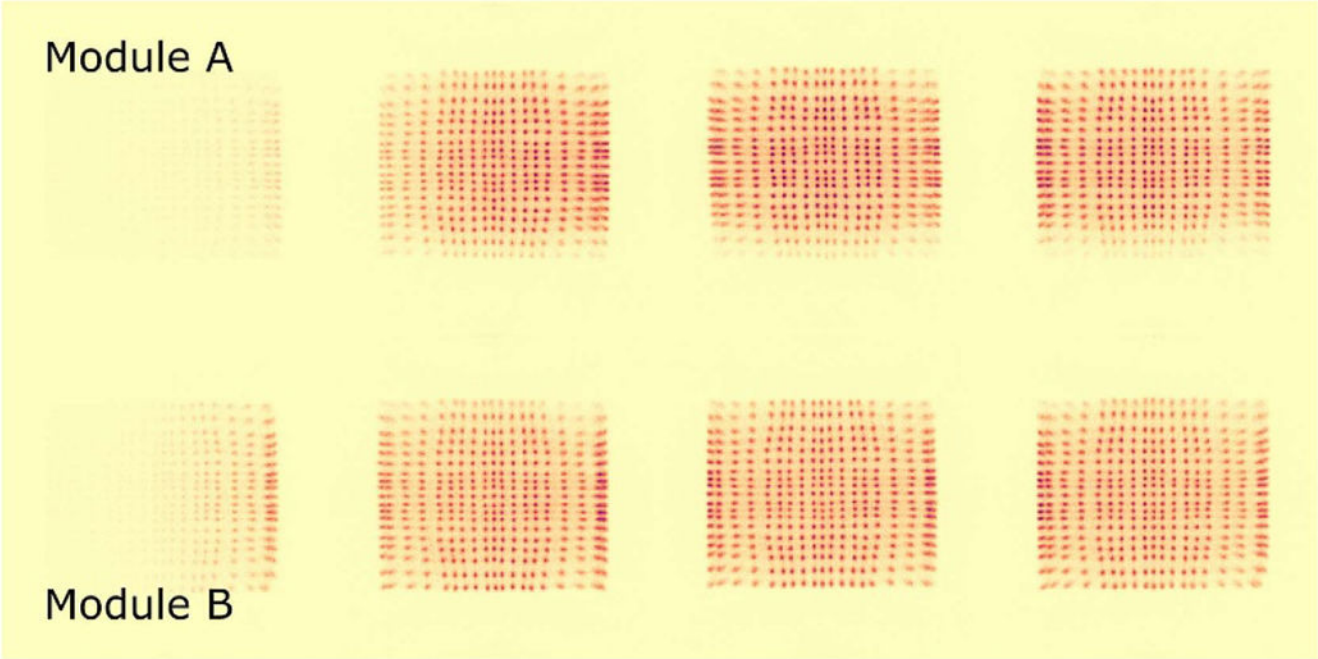

Figure 8.
Coincidence flood histograms for eight blocks across two complete modules. The nonuniform count distribution results from off-center placement of the point source, yielding few LORs which intersect both the leftmost crystals and the source.

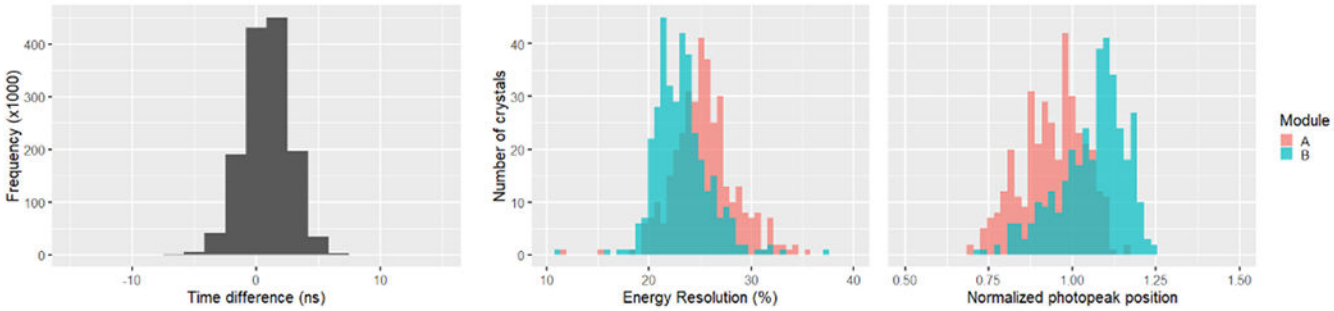

Figure 9.

(Left) Timing histogram for all LORs between the center two blocks of both modules. (Middle) Coincidence energy resolution for each crystal in the center two blocks of each module. (Right) Photopeak position of each crystal in the center two blocks of each module, normalized to the mean across all crystals.