UNIVERSITY OF CALIFORNIA SAN DIEGO

Application of Amorphous Silicon in High Sensitivity Optical Detection

A Dissertation submitted in partial satisfaction of the requirements
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in

Electrical Engineering (Nanoscale Devices and Systems)

by

Mohammad Abu Raihan Miah

Committee in charge:

Professor Yu-Hwa Lo, Chair
Professor Andrew C. Kummel
Professor Donald James Sirbuly
Professor Yuan Taur
Professor Paul K Yu

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The Dissertation of Mohammad Abu Raihan Miah is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

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DEDICATION

To my loving parents, my lovely wife, and my dear little brother

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LIST OF ABBREVIATIONS

a-Si	Amorphous Silicon
a-Ge	Amorphous Germanium
APD	Avalanche Photo Diode
AQC	Active Quenching Circuit
CEP	Cycling Excitation Process
DCR	Dark Count Rate
EHP	Electron-Hole Pair
EQE	External Quantum Efficiency
LWIR	Long Wave Infra-Red
PDE	Photon Detection Efficiency
PQC	Passive Quenching Circuit
SPAD	Single Photon Avalanche Diode
SPD	Single Photon Detector

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VITA

2013 Bachelor of Science in Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology

2015 Master of Science in Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology

2022 Doctor of Philosophy in Electrical Engineering (Nanoscale Devices and Systems), University of California San Diego

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ABSTRACT OF THE DISSERTATION

Application of Amorphous Silicon in High Sensitivity Optical Detection

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Professor Yu-Hwa Lo, Chair

This thesis offers the theoretical foundation of the defect assisted gain in amorphous Silicon and two applications of this gain for high sensitivity applications. A rigorous quantum mechanical model using 2nd order perturbation theory is presented in the thesis to model the defect assisted carrier multiplication rate in amorphous Silicon. The energy dependent multiplication rate can be

translated into the multiplication coefficients using distribution functions to model experimental measurable quantities. The methodology is valid for any other amorphous material.

After establishing the high gain in the amorphous Silicon, at first, a long wavelength infra-red (LWIR) absorber, amorphous germanium, is coupled with this gain medium to detect the LWIR signal at room temperature with a record detectivity and a decent responsivity. The high gain in amorphous silicon along with the photoconductive gain in amorphous silicon allows the device to operate at 20kHz which is higher than any thermal detectors, traditional room temperature IR detectors.

In second, amorphous silicon is used to develop a hybrid 180nm CMOS processed negative feedback avalanche detector (NFAD). At the beginning, a physics-based circuit model universal to both analog and Geiger-mode solid state photodetector is developed and implemented in SPICE. The model only requires the material and geometry of the gain medium as parameters. The model is then used for simulating different quenching circuits and designing an integrated active quenching circuit for the negative feedback avalanche detector (NFAD) in 180nm CMOS process. Next, design iteration steps, layout design and post-processing steps of the NFAD are presented. Experimental dark count rate, recovery time, photon detection efficiency and gain-bandwidth products are discussed for this device. The gain in the amorphous silicon allows the device to recover faster than the conventional NFAD.

CHAPTER 1: INTRODUCTION

1.1. Photodetectors

Photodetectors are optical sensors that can absorb optical signal and convert into a measurable electrical quantity. Generally, a photodetector will absorb light creating an electron-hole pair (EHP) and then flow of those electrons create an electrical current flow which can be detected via external instrument. Highly sensitive photodetectors are instrumental for biomedical imaging, deep space communication, LiDAR, autonomous driving and quantum information applications [1]–[3]. A brief overview of widely used three different types of solid state photodetectors, (a) Photoconductors (b) Photodiodes (c) Avalanche photodiodes, are discussed next.

1.1.1. Photoconductor

Photoconductors are generally made from either a n or p type of semiconductor connected in between two ohmic contacts. Figure 1.1 illustrates the general structure of a photoconductor.

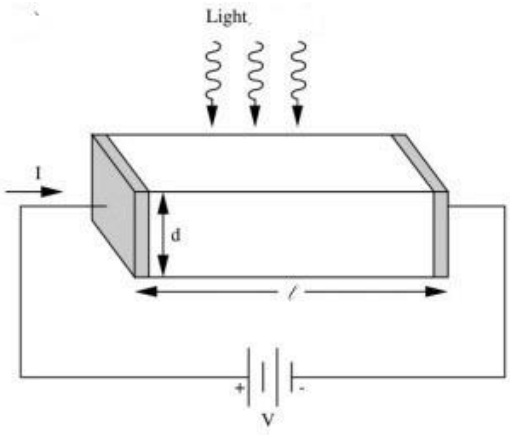

Figure 1.1: Schematic block diagram of a photoconductor. [4]

Light is absorbed within the exposed region of the semiconductor depending on the intrinsic absorption process mediated by the semiconductor bandgap or extrinsic defect mediated

long-wavelength absorption. For a p type semiconductor with 100% internal quantum efficiency, photocurrent I_{ph} of a photoconductor can be written as,

$$I_{ph} = qG\mu_n\tau_n \frac{AV}{l} \qquad (1.1)$$

Here, G is the optical generation rate, μ_n is electron mobility, τ_n is minority carrier electron's lifetime, A is the device area, l is the length of the photoconductor, V is applied bias and q is the elementary charge. Electron drift velocity, v_d,

$$v_d = \frac{\mu_n V}{l} = \frac{l}{\tau_{tr}} \qquad (1.2)$$

where t_{tr} is the transit time of the electron through the semiconductor. Combining equation (1.1) and (1.2) we can find,

$$I_{ph} = q\ (GAl)\frac{\tau_n}{\tau_{tr}} = q\ (GAl)\ G_{PC} \qquad (1.3)$$

Here, $G_{PC} = \frac{\tau_n}{\tau_{tr}}$ is called the photoconductive gain which represents how fast electrons can travel to the electrode before recombining with a hole.

1.1.2. Photodiodes

A photodiode has a structure similar to a semiconductor p-n junction or p-i-n diode operated under reverse bias. Upon light absorption, any EHP generated in the depletion region or close to the depletion region will traverse through the depletion region under the electric field and create a photocurrent. An intrinsic, i, layer is sometimes sandwiched between p and n layer to increase the light absorption within the depletion region and external quantum efficiency (EQE) as shown in Figure 1.2. However, thicker depletion region will increase the transit time of the carriers and in turn reduce the bandwidth of the device. Similarly, minority carrier diffusion length will also tailor the EQE of the device.

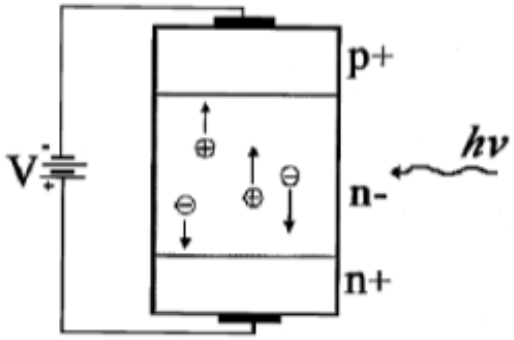

Figure 1.2: Schematics of a p-i-n photodiode [5]

1.1.3. Avalanche Photodiode (APD)

Avalanche photodiodes (APDs) are p-n or p-i-n diodes operated under a large reverse bias voltage employing avalanche multiplication as the operating principle [6]–[8]. Avalanche process or impact ionization governs by the high energetic electrons or holes losing their energy to the columbic interaction with the lattice and generating a new EHP. Figure 1.3 illustrates the avalanche process after an initial electron-hole pair generated by light absorption (left). The generated hole is collected by the electrode whereas the photogenerated electron will acquire kinetic energy upon accelerating under high electric field and create secondary EHP through impact ionization. The secondary electrons and holes and generate additional carriers, i.e. gain, until the device reaches a steady state or limited by the external circuitry [9].

Multiplication gain, M, of electrons in an avalanche diode with depletion layer width of W and electric field E can be written as [9]

$$M = \frac{1}{1 - \int_0^W \alpha_n(E) e^{\int_x^W (\alpha_n(E) - \alpha_p(E)) dx'} dx} \qquad (1.4)$$

Here, $\alpha_{n(p)}(E)$ are impact ionization coefficients of electrons (holes). These coefficients are field dependent and multiplication process is spatially dependent. Breakdown voltage of the

device is defined as the voltage when the resultant gain becomes infinity, i.e. the integral term in the denomination equals to one.

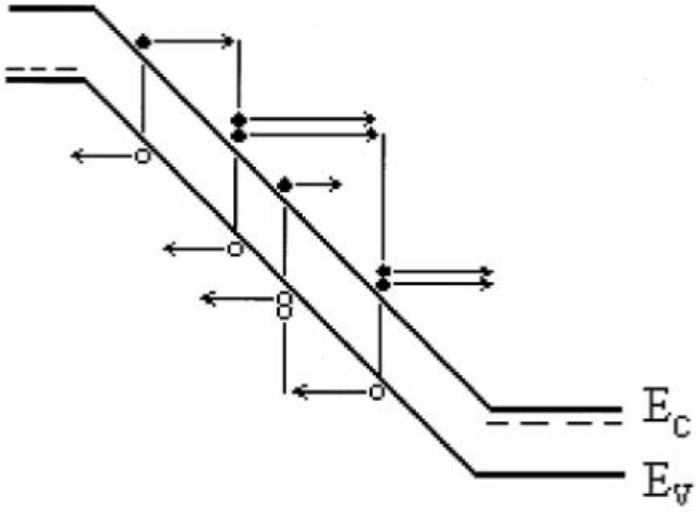

Figure 1.3: Avalanche multiplication process [5].

Depending on the bias voltages, the APDs can operate in three modes; (i) analog mode, when the bias voltage is way below the breakdown votlage, (ii) sub-geiger mode, when the bias voltage is close to the breakdown voltage and (iii) geiger mode, when the operational voltage is above the breakdown voltage. Random nature of the multiplication process introduces noise in APDs and characterized by the excess noise factor, F as

$$F = \frac{< M^2 >}{< M >^2} \qquad (1.5)$$

Excess noise factor, F depends on the ratio of the impact ionization coefficients α_n and α_p[10].

1.2. Cycling Excitation Process (CEP)

Cycling Excitation Process (CEP) is an internal gain mechanism developed in 2015 for a highly co-doped Si [11]. Since CEP uses localized states for the gain mechanism, the process was also observed in amorphous Si [12] with a high gain-bandwidth product. Conventional impact ionization or avalanche process involves extended Bloch waves from the mobile band [9] whereas CEP used both localized states and extended states for the process. Figure 1.4 shows the difference in the physical mechanism between the conventional avalanche process (a) and CEP process (b). CEP process is more efficient compared to the impact ionization due to the relaxation in the k selection which allows the hot carriers to initiate the multiplication process at a low initial energy.

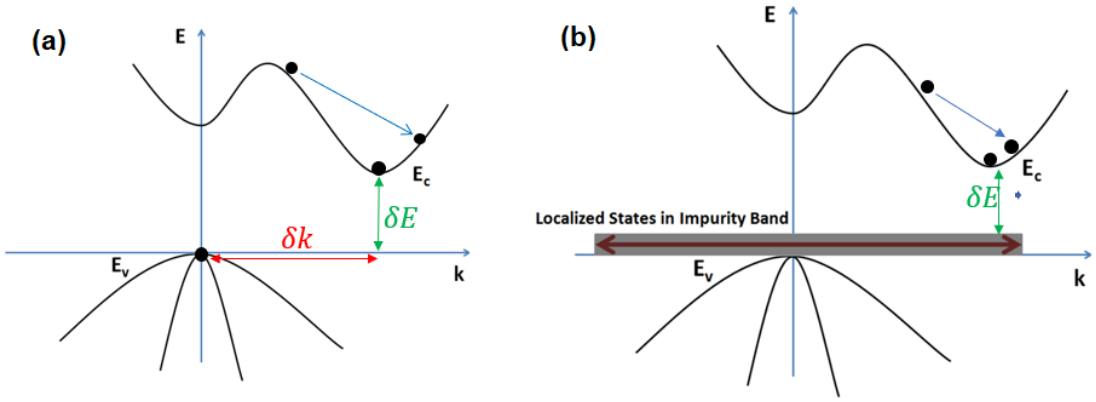

Figure 1.4: (a) Energy and momentum conservation for a traditional avalanche process in Si. (b) relax in the momentum conservation due to the localized states in the impurity band for CEP process.

As an illustration, consider a nSi/aSi/ITO device as shown in Figure 1.5. Absorbed light in nSi generate an electron-hole pair where electrons are collected by the electrode and holes traverse into the aSi region via tunneling in the nSi/aSi junction. These photo-generated holes accelerate by the potential drop in aSi and acquire sufficient energy to create a secondary electron-hole pair in the localized states (Figure 1.5(a)). Both electrons and holes in the localized states can reach the mobile band by means of field enhanced tunneling or temperature dependent phonon excitation

(Figure 1.5(b)). For a not, at high electric field, tunneling is the main mechanism for band-tail states. Once the carriers come into the mobile band, secondary holes will be collected in the electrode whereas secondary electrons will accelerate with the field and generate another electron-hole pairs in the localized states upon gaining sufficient kinetic energy (Figure 1.5(c)). These carriers again reach the mobile band by means of tunneling or phonon excitation (Figure 1.5(d)). After that, the process continues and generates additional electron-hole pairs until the gain is saturated or limited by the external circuitry.

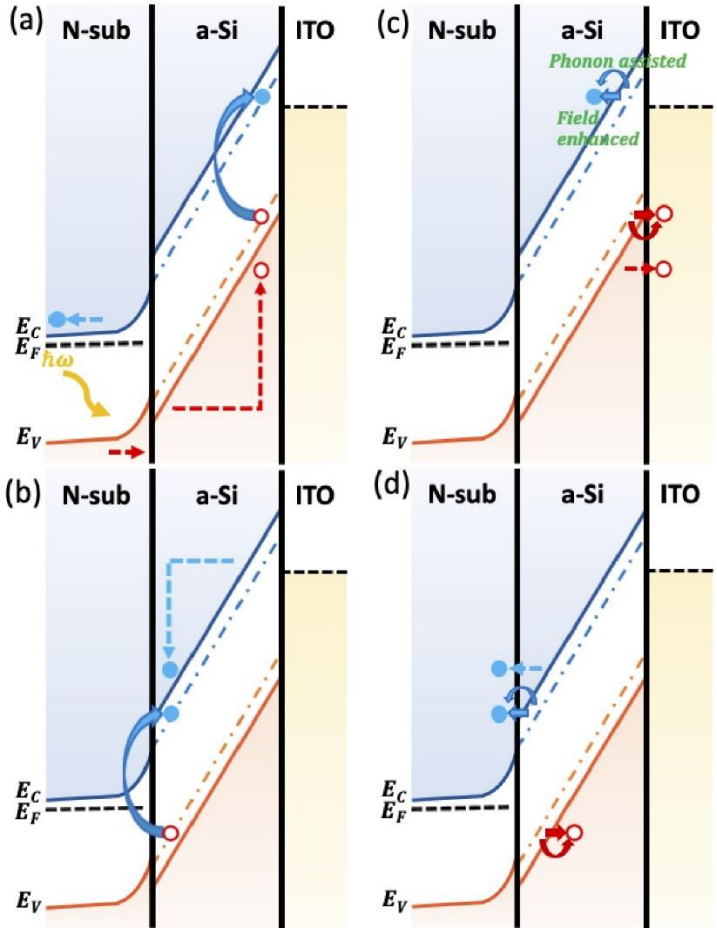

Figure 1.5: (a) Schematic illustration of the CEP process in amorphous Si (a) hole-initiated generation of e-h pair in localized states, (b) electron-initiated generation of e-h pair in localized states, (c), (d) excitation of localized states via field enhanced tunneling or phonon excitation [13].

1.3. Single Photon Detectors

In recent years, single photon detectors (SPD) gain immense interests due to its application in deep space communication, LIDAR for remote sensing, bioluminescence detection and quantum communication and information science [1], [2], [14]–[16]. Single photon avalanche detectors (SPAD) are commonly used due to the absence of the vacuum and high bias requirements like photo-multiplier tubes (PMT) or cryogenic cooling like super-conducting SPDs [17]–[20]. SPADs are made of a p-n or a p-i-n avalanche diodes with different semiconductor materials to operate in different wavelengths ranging from ultra-violet to near infrared region [21]–[28]. During the device operation, a high voltage is applied across the device allowing photo generated electrons (holes) to gain sufficient energy under the high electric field, and subsequently generate secondary electrons and holes from the initial carrier via avalanche or impact ionization process with or without the help of the defects and phonons [15], [29], [30].

SPADs based on the CMOS process technologies is an attractive solution to low cost photon-counting and photon-starved imaging applications [31]. Moreover, CMOS implementation of the SPADs allow it to integrate with the quenching circuits and amplifiers internally expunging the need of any external read-out circuits and parasitic associated with it. Additionally, CMOS process implemented SPADs show low dark count rate, high photon detection probability and low timing jitter [21], [22], [31]–[36]. Dead time or recovery time of the device is still high without any quenching circuit to operate the devices at high frequencies.

1.4. Motivation and Challenges

Avalanche or impact ionization process is the predominant multiplication process in the solid-state photodetector. However, due to the requirement of both energy and momentum

conservation, this process requires higher energy for the carriers to initiate the multiplication. CEP is an alternative to the avalanche process employing localized defect states in either highly compensated p-n junction or in amorphous material. A greater understanding of the physical mechanism behind the CEP process and the multiplication rate associated with it are required to utilize CEP gain mediums for highly sensitive optical detection applications.

Once both theory and the experimental validation are established for the CEP gain medium, amorphous Silicon, I dedicate myself to explore the potential applications of this low cost and highly efficient gain medium for the advancement of the current state-of-the-art technologies. In the long wave infra-red (LWIR) regime, all of the room-temperature detectors are based on the thermal nature and as a result, the detectors are inherently slow. Therefore, for the first application, a high-speed room-temperature quantum LWIR detector is proposed by coupling a LWIR absorber amorphous Germanium and CEP gain medium amorphous Silicon.

As discussed in the previous section, CMOS implementation of the SPAD is necessary for any commercial realization of the LiDAR or low light imager. However, SPADs require additional quenching circuits and sometimes, amplifiers for their operation. On the other hand, negative Feedback Avalanche Diodes (NFAD) were proposed to resolve the long recovery time of the SPADs but they are still not implemented in the CMOS technology. Additionally, a predictive circuit model is also needed to design and simulate the device with the CMOS circuit layouts. Therefore, for the 2nd application of the CEP, a CMOS implemented NFAD detector is explored is this thesis using amorphous silicon gain medium after the development of a new circuit model for any analog or single photon detector.

1.5. Dissertation Outline

This dissertation aims to physically model the CEP mechanism to have a deeper understanding and then use that to couple this gain for various applications such as long wave infra-red (LWIR) detection and a negative feedback SPAD in CMOS technology.

Chapter 2 shows the theoretical modeling of the defect assisted multiplication rate in amorphous silicon using 2^{nd} order perturbation theory.

Chapter 3 demonstrates the theory, fabrication and experimental characterization of a room-temperature Long-Wave Infra-Red (LWIR) detector coupling the CEP gain medium, amorphous Silicon, and absorber, amorphous Germanium.

Chapter 4 presents a unified circuit model for both analog and single photon detector. The model takes the material property and device geometry as parameters and can simulate devices with quenching circuits and amplifiers.

Chapter 5 reports a negative feedback avalanche diode in 180nm CMOS technology using a post-processed thin amorphous Silicon layer. The device has a 25% photon detection probability with ~8THz gain bandwidth product and 444Hz/μm^2 dark count rate.

Chapter 6 concludes the thesis and discusses a brief outlook of the prospective directions.

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CHAPTER 2: DEFECT ASSISTED CARRIER MULTIPLICATION RATE IN AMORPHOUS SILICON

In this chapter, theoretical framework of the carrier multiplication rate in the amorphous silicon will be established from a 2nd order perturbation theory. The multiplication rate can be coupled with Boltzmann transport equation or Monte Carlo simulation to relate the microscopic model to any measurable quantity.

2.1. Motivation

Cycling excitation process (CEP) is an internal gain mechanism that has been demonstrated in highly counter doped silicon p-n junction diodes [1] as well as amorphous silicon (a-Si) photodiodes [2]. It is particularly attractive to use amorphous silicon as gain medium since a-Si is a low-cost material that can be deposited on many kinds of substrate over a large area, including the possibility for integration with light emitters and CMOS electronics [3], [4]. However, questions arise why a thin layer of a-Si (30-50nm) with high defect density and very low carrier mobility can become such efficient gain medium and produce such high sensitivity to detect single photons and achieve record high (>2THz) gain-bandwidth product [2], [3]. In this chapter, we will explore how defects can play a role in the multiplication process and quantify the process by calculating defect assisted carrier multiplication rate in amorphous silicon.

2.2. Theoretical Framework

To reduce the computation complexity without losing the generality, in this work we have approximated the band tail states in conduction and valence bands by two discrete levels. We denote these levels as localized donor and acceptor states. An empty donor state is positively charged and near the mobile conduction band, and an occupied acceptor state is negatively charged

and near the mobile valence band. We calculate the donor-acceptor pair (DAP) assisted carrier multiplication rate in a-Si by assuming an energetic carrier in the mobile band is relaxed to a lower energy state to excite a donor-acceptor pair exciton which is then ionized into an e-h pair. Our current analysis does not include ionization of DAP exciton since under room temperature and high-field condition where the device operates, most DAP excitons are ionized into mobile bands rapidly. However, this simplification could overestimate the gain and ignore gain saturation, which is manifested in the comparison between the calculation and the experiment.

For the DAP before excitation (i.e. occupied acceptor and unoccupied donor states), we used 1s hydrogen wavefunction with corrected mass and dielectric constant to approximate their wavefunction. For the wavefunctions of the energetic carrier and the carrier after losing part of its energy to excite the DAP pair, we employed density functional theory (DFT) computation to calculate the Bloch wavefunctions where all bands of relevant energy levels (4 bands in conduction band and 4 bands in valence bands) were taken into account. This many-body calculation using Fermi's golden rule can produce carrier multiplication rate for amorphous material involving donor-acceptor pairs.

Another important remark we would like to make here is that momentum relaxation process is not that important for the amorphous silicon as with conventional semiconductors. This is because for disordered materials such as a-Si, the momentum relaxation time is extremely short (1-10 fs) compared to the energy relaxation time, verified experimentally [5] and manifested by their very low mobility [6], [7]. As a result, band tail states will be readily available at all k values and momentum conservation is relaxed for the amorphous silicon. On the other hand, since phonon scattering is not nearly as effective in relaxing carrier energy than it does with carrier momentum due to the large mass mismatch between ions and electrons (holes), carriers under high E-field can

remain energetic. This provides another reason for disordered materials to become highly efficient for carrier multiplication. It is to be noted that carrier multiplication rate depends on carrier energy, not momentum. Therefore, an energetic electron with its momentum relaxed by phonon scattering can have a greater probability of producing impact ionization within a thin layer than a fast travelling electron of the same energy since the latter spends little time in the material. Therefore, from this consideration, the low mobility of disordered material can be more favorable than high mobility crystalline semiconductor in producing carrier multiplication.

In calculating the carrier multiplication process for a-Si, we focus on the most dominant process of having an energetic conduction (valence) band electron (hole) interacts with a DAP via Coulomb potential and excites the DAP into a DAP exciton. Figure 1 sketches the schematic diagram of the process. Due to energy conservation, the hot carrier loses its energy to become a carrier of lower energy in the mobile band, and the lost energy is used to excite a DAP exciton.

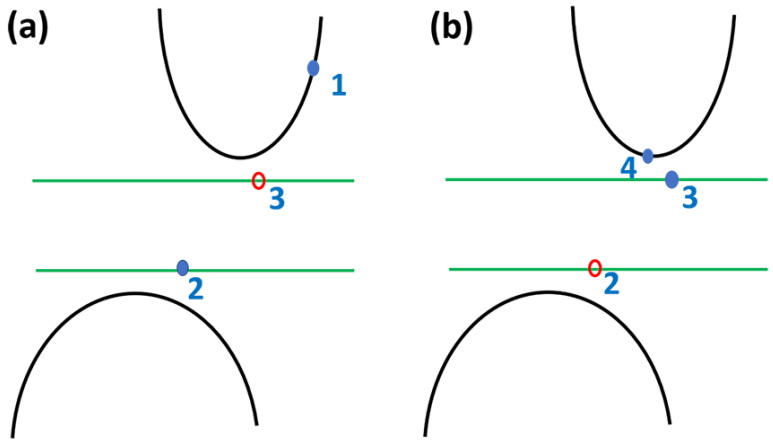

Figure 2.1: Schematic diagram of DAP pair assisted electron multiplication process in a-Si. (a) Before the multiplication process, there are a high energy electron (state 1) and an occupied acceptor (state 2), (b) Electron from state 1 loses its energy to excite a DAP pair (state 2 and 3) and becomes a low energy electron (state 4) after the multiplication process. At room temperature and under high field, we have assumed the exciton is rapidly ionized to become an e-h pair in mobile bands

We consider a perturbation Hamiltonian H' from the Coulomb interaction between the hot carrier with its position represented by $\boldsymbol{r_1}$ and a localized electron in the occupied acceptor state with a position vector $\boldsymbol{r_2}$ as

$$H' = \frac{q^2}{4\pi\epsilon|\boldsymbol{r_1} - \boldsymbol{r_2}|} \qquad (1)$$

where q is elementary electron charge and ϵ is dielectric constant of amorphous silicon.

Although the band diagram between a-Si and crystalline Si is very different near the band edge, the wavefunctions for high kinetic energy carriers are quite similar. Hence, we use the calculated wavefunction of crystalline Si for the carriers in the mobile band. We denote $\psi_{1,\boldsymbol{k_1}}(n_1, \boldsymbol{r})$ as the wavefunction of hot electron with wavevector $\boldsymbol{k_1}$, energy E_1 and band index n_1, and $\psi_{4,\boldsymbol{k_4}}(n_4, \boldsymbol{r})$ as the wavefunction of the electron post DAP exciton excitation with wavevector $\boldsymbol{k_4}$, energy E_4 and band index n_4. Both $\psi_{1,\boldsymbol{k_1}}(n_1, \boldsymbol{r})$ and $\psi_{4,\boldsymbol{k_4}}(n_4, \boldsymbol{r})$ were calculated by DFT [8] .

On the other hand, the wavefunctions of the trapped states are modeled as 1s Hydrogen orbital. $\psi_2(\boldsymbol{r})$ and $\psi_3(\boldsymbol{r})$ are the wavefunctions of the localized acceptor and localized donor states respectively and are represented as:

$$\psi_2(\boldsymbol{r}) = \frac{e^{-\frac{|\boldsymbol{r_A}|}{a_A}}}{\sqrt{\pi a_A^3}} \qquad (2a)$$

$$\psi_3(\boldsymbol{r_2}) = \frac{e^{-\frac{|\boldsymbol{r_D}|}{a_D}}}{\sqrt{\pi a_D^3}} \qquad (2b)$$

where $\boldsymbol{r_A}$ and $\boldsymbol{r_D}$ are the distances from the position of the acceptor ($\boldsymbol{r_{acc}}$) and donor states ($\boldsymbol{r_{don}}$), respectively, i.e. $|\boldsymbol{r_A}| = |\boldsymbol{r_{acc}} - \boldsymbol{r}|$ and $|\boldsymbol{r_D}| = |\boldsymbol{r_{don}} - \boldsymbol{r}|$. a_A and a_D are Bohr radius for the donor and acceptor states. For our calculation, we put the acceptor at origin, i.e. $\boldsymbol{r_A} = |\boldsymbol{r}|$

For simplicity, we assume that all the acceptor states are at a single energy level E_2 and all donor states are at E_3, and the total number of shallow donor and acceptor states modeling the band tail states has a concentration N_T. From the first order perturbation theory [9]–[13], the excitation rate of a DAP exciton with electron-hole energy E_2 and E_3, R_{E_2,E_3} can be represented as,

$$R_{E_2,E_3}(E_1, r_{acc}, r_{don}) = 2\frac{2\pi}{\hbar}\frac{V}{(2\pi)^3}\sum_{n_1,\boldsymbol{k_1}}\sum_{n_4}\int_{k_4}|M|^2\delta\left(E_{n1}(\boldsymbol{k_1}) + E_2 - E_3 - E_{n_4}(\boldsymbol{k_4})\right)d^3k_4 \quad (3)$$

Where E_1 is the energy of the energetic carrier that initiates the process and E_4 is the energy the carrier decays to afterwards. V is the volume of amorphous silicon, and M is the matrix element. The summation over $n_1, \boldsymbol{k_1}$ includes those states in all the mobile conduction bands with wave vector $\boldsymbol{k_1}$ that have their energy eigen value E_1.

The above discussion has treated electrons as if they are distinguishable. The anti-symmetry property of electron is considered in the expression of the matrix element M of the interaction [11], [14]

$$|M|^2 = \frac{1}{2}(|M_D|^2 + |M_E|^2 + |M_D - M_E|^2) \quad (4)$$

Here M_D is the direct process, i.e. the first electron is transitioned from state 1 to state 4 and the second electron is transitioned from an acceptor state (state 2) to a donor state (state 3). Exchange interaction element, M_E is the same as M_D except those electrons are exchanged. Since M_D and M_E have very similar values [14], we can ignore the last term in (4).

We can then express M for electron-initiated carrier multiplication process involving a donor-acceptor pair as

$$M = \int_{\boldsymbol{r_1}}\int_{\boldsymbol{r_2}}\psi^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1})\psi^*_3(\boldsymbol{r_2})H'\psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1})\psi_2(\boldsymbol{r_2})d^3r_1d^3r_2 \quad (5)$$

From equation (1), (2) and (5) we can write,

$$M = \int_{\boldsymbol{r_1}} \int_{\boldsymbol{r_2}} \psi^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1}) \psi^*_3(\boldsymbol{r_2}) \frac{q^2}{4\pi\epsilon |\boldsymbol{r_1} - \boldsymbol{r_2}|} \psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1}) \psi_2(\boldsymbol{r_2}) d^3 r_1 d^3 r_2 \quad (6)$$

$$\psi_2(\boldsymbol{r_2}) = \frac{e^{-\frac{r_A}{a_A}}}{\sqrt{\pi a_A^3}} = \left(\frac{1}{2\pi}\right)^3 \frac{1}{\sqrt{\pi a_A^3}} \int_{\boldsymbol{k_2}} A(\boldsymbol{k_2}) e^{i\boldsymbol{k_2}.\boldsymbol{r_A}} \, d^3 k_2 \qquad (7.A)$$

$$\psi_3(\boldsymbol{r_2}) = \frac{e^{-\frac{r_D}{a_D}}}{\sqrt{\pi a_D^3}} = \left(\frac{1}{2\pi}\right)^3 \frac{1}{\sqrt{\pi a_D^3}} \int_{\boldsymbol{k_3}} B(\boldsymbol{k_3}) e^{i\boldsymbol{k_3}.\boldsymbol{r_D}} \, d^3 k_3 \qquad (7.B)$$

where, $A(\boldsymbol{k_2}) = \frac{8\pi a_A^3}{\left(1+a_A^2 k_2^2\right)^2}$ and $B(k_3) = \frac{8\pi a_D^3}{\left(1+a_D^2 k_3^2\right)^2}$ are fourier coefficients.

Using (7.A) and (7.B), equation (6) can be rewritten as,

$$M = \left(\frac{1}{2\pi}\right)^6 \frac{1}{\pi\sqrt{a_A^3 a_D^3}} \frac{q^2}{4\pi\epsilon} \int_{\boldsymbol{k_2}} e^{i\boldsymbol{k_2}.\boldsymbol{r_{acc}} - i\boldsymbol{k_3}.\boldsymbol{r_{don}}} A(\boldsymbol{k_2}) d^3 k_2$$

$$\int_{\boldsymbol{k_3}} B(\boldsymbol{k_3}) \, d^3 k_3 \int_{r_1} \int_{r_2} \frac{\psi^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1}) \psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1}) e^{i\boldsymbol{k_3}.\boldsymbol{r_2} - i\boldsymbol{k_2}.\boldsymbol{r_2}}}{|\boldsymbol{r_1} - \boldsymbol{r_2}|} d^3 r_1 d^3 r_2 \quad (8)$$

Now, choosing $\boldsymbol{r_{acc}}$ as origin, and $\boldsymbol{\rho} = \boldsymbol{r_2} - \boldsymbol{r_1}$, we can write equation (8) as,

$$M = \left(\frac{1}{2\pi}\right)^6 \frac{1}{\pi\sqrt{a_A^3 a_D^3}} \frac{q^2}{4\pi\epsilon} \int_{\boldsymbol{k_2}} e^{-i\boldsymbol{k_3}.\boldsymbol{r_{don}}} A(\boldsymbol{k_2}) d^3 k_2 \int_{\boldsymbol{k_3}} B(\boldsymbol{k_3}) \, d^3 k_3$$

$$\int_{r_1} \int_{\rho} \frac{\psi^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1}) \psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1}) e^{i(\boldsymbol{k_3} - \boldsymbol{k_2}).\boldsymbol{\rho}} e^{i(\boldsymbol{k_3} - \boldsymbol{k_2}).\boldsymbol{r_1}}}{|\boldsymbol{\rho}|} d^3 r_1 d^3 \rho \qquad (9)$$

Since, ψ_{n1} and ψ_{n4} are bloch waves, they can be expressed as,

$$\psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1}) = e^{i\boldsymbol{k_1}.\boldsymbol{r_1}} u_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1}) \quad (10.A)$$

$$\psi_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1}) = e^{i\boldsymbol{k_4}.\boldsymbol{r_1}} u_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1}) \quad (10.B)$$

Then,

$$\int_{r_1} \psi^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1})\psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1})\, e^{i(\boldsymbol{k_3}-\boldsymbol{k_2}).\boldsymbol{r_1}} d^3r_1$$

$$= \int_{r_1} u^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1})u_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1})\, e^{i(\boldsymbol{k_1}+\boldsymbol{k_3}-\boldsymbol{k_2}-\boldsymbol{k_4}).\boldsymbol{r_1}} d^3r_1$$

$$= \left[\frac{(2\pi)^3}{V}\delta(\boldsymbol{k_3}-\boldsymbol{k_2}+\boldsymbol{k_1}-\boldsymbol{k_4})\right]\int_{r_1} u^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1})u_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1})\, d^3r_1$$

$$= \left[\frac{(2\pi)^3}{V}\delta(\boldsymbol{k_3}-\boldsymbol{k_2}+\boldsymbol{k_1}-\boldsymbol{k_4})\right] C(\boldsymbol{k_1}, n_1 : \boldsymbol{k_4}, n_4) \qquad (11.A)$$

$$\int_{\rho} \frac{e^{i(\boldsymbol{k_4}-\boldsymbol{k_1}).\boldsymbol{\rho}}}{|\boldsymbol{\rho}|} d^3\rho = \frac{4\pi}{(|\boldsymbol{k_4}-\boldsymbol{k_1}|)^2} \quad (11.B)$$

and,

$$\int_{\boldsymbol{k_3}} e^{-i\boldsymbol{k_3}.\boldsymbol{r_{donor}}} B(\boldsymbol{k_3})\, \delta(\boldsymbol{k_1}+\boldsymbol{k_3}-\boldsymbol{k_2}-\boldsymbol{k_4}) d^3k_3$$

$$= e^{-i(\boldsymbol{k_4}-\boldsymbol{k_1}+\boldsymbol{k_2}).\boldsymbol{r_{donor}}} \frac{8\pi a_D^3}{(1+a_D^2|\boldsymbol{k_4}-\boldsymbol{k_1}+\boldsymbol{k_2}|^2)^2} \qquad (11.C)$$

Using (10) and (11), equation (9) can be found as,

$$M = \frac{8q^2\sqrt{a_D^3 a_A^3}}{V\epsilon\pi^2} C(k_1, n_1; k_4, n_4) D\left(a_{A,} a_D, \boldsymbol{r_{don}}, \boldsymbol{k_1}, \boldsymbol{k_4}\right) \qquad (12)$$

Here C is the overlap integral between state 1 and 4 and expressed as

$$C(\boldsymbol{k_1}, n_1; \boldsymbol{k_4}, n_4) = \int_{\boldsymbol{r_1}} \frac{\psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1})}{e^{i\boldsymbol{k_1}.\boldsymbol{r_1}}} \frac{\psi^*_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1})}{e^{-i\boldsymbol{k_4}.\boldsymbol{r_1}}} d^3r_1 \quad (13.1)$$

Here $\psi_{n1}(\boldsymbol{k_1}, \boldsymbol{r_1})$ and $\psi_{n4}(\boldsymbol{k_4}, \boldsymbol{r_1})$ are Bloch functions directly solved from the DFT calculation. Dividing them by the plane wave term $e^{i\boldsymbol{k}.\boldsymbol{r}}$ gives the periodic part of the wavefunction.

D is defined as,

$$D\left(a_{A,}a_D,\boldsymbol{r_{don}},\boldsymbol{k_1},\boldsymbol{k_4}\right)=\frac{e^{-i(\boldsymbol{k_4}-\boldsymbol{k_1}).\boldsymbol{r_{don}}}}{(|\boldsymbol{k_4}-\boldsymbol{k_1}|)^2}\int_{\boldsymbol{k_2}}\frac{e^{-i\boldsymbol{k_2}.\boldsymbol{r_{don}}}d^3\boldsymbol{k_2}}{(1+a_A^2k_2^2)^2(1+a_D^2|\boldsymbol{k_4}-\boldsymbol{k_1}+\boldsymbol{k_2}|^2)^2} \quad (13.2)$$

Similar equations can also be derived for the hole-initiated carrier multiplication process.

Substituting (12) into (3), the impact ionization rate produced by an energetic electron of energy E_1 can be calculated. The length of the donor position vector $\mathbf{r_{don}}$ represents the distance between the acceptor (assumed to be at the origin) and the nearest donor, so it is also the distance of a donor-acceptor pair (i.e. $\boldsymbol{r_{DAP}}$). Since we assume equal concentration for both donor and acceptor states in the band tails of conduction and valence band, we have $N_{DAP}=N_A=N_D$. The net rate of impact ionization via excitation of a DAP exciton by a hot electron of energy E_1 can be represented as,

$$R(E_1)\sim R_{E_2.E_3}(E_1,\boldsymbol{r_{don}})VN_{DAP} \qquad (14)$$

2.3. Results

Experimental observations of high gain in highly doped, heavily compensated silicon p/n junction [1], [15] and amorphous silicon [2] lead us to postulate the origin of gain attributed to the high density of localized states in the band tails.

To investigate further, we calculated DAP assisted carrier multiplication initiated by energetic electrons and holes. DFT calculation was performed for bulk Silicon using SIESTA package [16] to extract wavefunctions and dispersion relations of mobile bands. Generalized gradient approximation (GGA) functional [17] was used as the exchange-correlation potential. In the calculation, mesh cutoff is 100 Rydberg. We used 28×28×28 k point grid for the DFT calculation [18]. Figure 2 shows the calculated electron-initiated carrier multiplication rate as a function of electron energy. Similar analysis also produces the hole-initiated carrier multiplicate

rate (Fig. 3). For both calculations, we have used donor-acceptor trap density of $5 \times 10^{19} cm^{-3}$ and chosen the energy level of traps to be 0.25eV from the edge of the mobile bands. Compared with crystalline Si [14], [19], the carrier multiplication rate for a-Si rises sharply with the carrier energy due to the relaxed k selection rule by the localized donor and acceptor states. We also introduced a trend line in Fig. 2 and 3 to carry out the calculation of multiplication coefficient and gain of the device under different amorphous Si thickness. Data points that deviate significantly from the trend line are unreliable and ignored due to the limited k-points within a supercell in the DFT band structure calculation. That is the main reason we used crystalline Si instead of a-Si to simulate the mobile bands. For a-Si, the supercell needs to be much greater than crystalline Si, thus the effective number of k-points in the simulation is reduced, leading to large fluctuations in the density of states and the multiplication rate. At higher energy, multiplication rate plateaus as a direct consequence of density of states at higher energy. Since k selection rule is relaxed for defect assisted multiplication rate, the availability of possible final states primarily depends on energy conservation and follows the density of states.

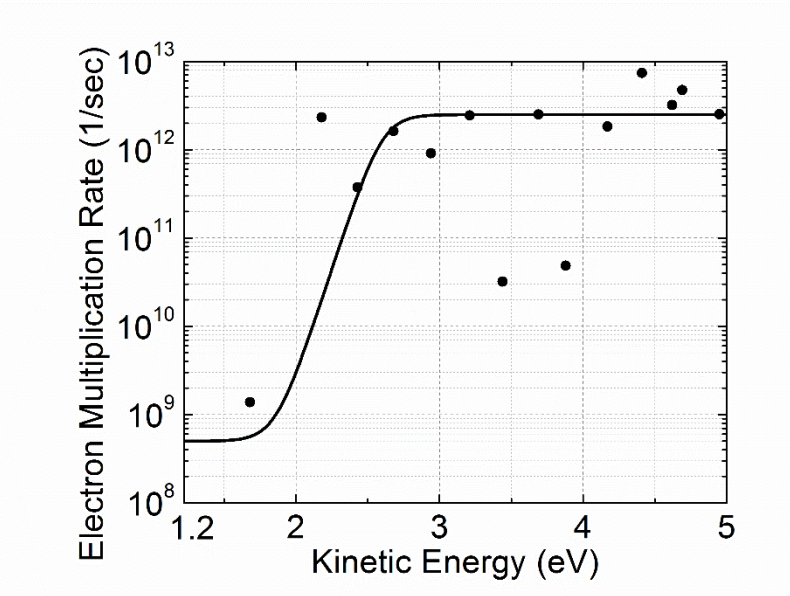

Figure 2.2: DAP assisted multiplication rate for electrons at different kinetic energy. Solid curve is the fitted curve, which is later used for distribution function and gain calculations.

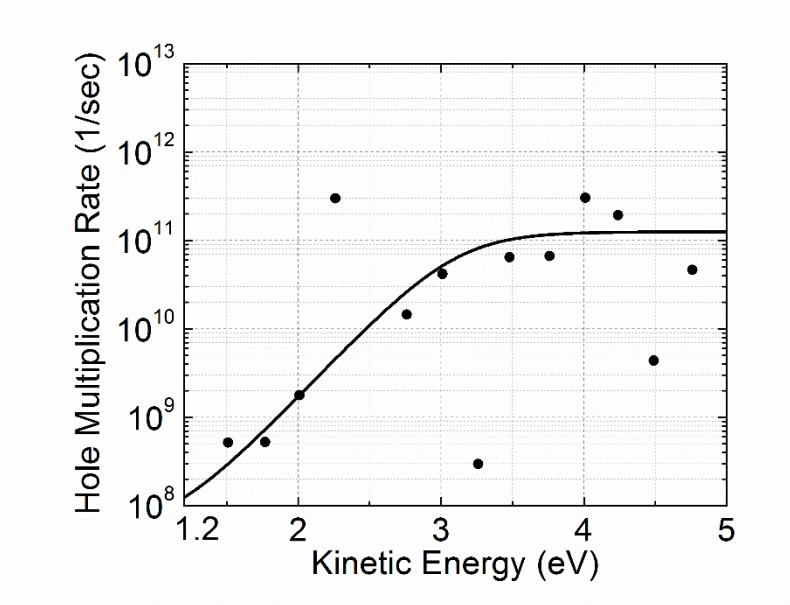

Figure 2.3: DAP assisted multiplication rate for holes at different kinetic energy. Solid curve is the fitted curve, which is later used for distribution function and gain calculations.

2.4. Conclusion

To summarize, we have developed a theoretical model for internal carrier multiplication gain in amorphous silicon. The model can be applied to other disordered materials as potential gain medium for signal amplification. We have focused on the DAP assisted carrier multiplication process where the donor-acceptor pairs are the bandtail states next to the mobile bands. With some approximations, we have combined the analytical model for the DAP pair and the DFT calculation for the mobile states including all bands and states of relevant energy. The calculation shows rapid increase in rate of carrier multiplication process involving excitation of DAP states, proving their effect of relaxation of the k-selection rule that limits the efficiency of conventional impact ionization process.

This chapter, in part, is a reprint of material as it appears in the following publications:

M.A.R. Miah*, I.A. Niaz*, and Y.H. Lo, “Defect assisted carrier multiplication in amorphous silicon”, IEEE Journal of Quantum Electronics 56 (3), 1-11 (2020).

The dissertation author was the primary author of this paper.

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CHAPTER 3: ROOM-TEMPERATURE LWIR DETECTION

Chapter 3 discusses the fabrication and characterization of a room-temperature Long Wave Infra-Red (LWIR) detector using thin layers of 25nm amorphous silicon (a-Si) and 100nm amorphous germanium (a-Ge). The detector couples the CEP gain of the a-Si with the photoconductive gain in a-Ge to produce a record responsivity, detectivity and noise equivalent power (NEP).

3.1. Motivation

Long-wave Infrared (LWIR) detection has been widely used in a large number of systems including night vision, thermal sensing, remote sensing, autonomous driving, robotics vision, machine vision, disease detection, and scientific research [1]. Over the past few decades, a large number of LWIR detectors have been demonstrated, including microbolometer [2,3], HgCdTe (MCT) [4], multi-quantum well (MQWIP) or quantum dots (QDIP) [5,6], Type-II superlattice structure (T2SL) [7,8], blocked impurity band (BIB) trap detectors [9,10], and graphene detectors [11]. According to the operation environment, LWIR detectors can be divided into two groups, uncooled detectors and cooled detectors. The former are mostly bolometers that detect IR induced temperature change and the output signal can be represented via different transduction mechanisms [12,13]. Even though microbolometers have demonstrated room temperature detectivity of 10^9 Jones, they generally have limited bandwidth less than 100 Hz [2,3]. As a quantum detector, Type-II superlattice (T2SL) structure has shown uncooled, broad IR spectrum detection ranging from short-wave infrared (SWIR) to very-long wavelength infrared (VLWIR) light [14,15]. The highest reported TIIS LWIR detectivity is about 6×10^8 Jones with an optical immersion design [7].

In contrast with uncooled LWIR detectors, almost all cooled LWIR detectors are quantum detectors with their photoresponse generated by photoexcited electrons or electron-hole pairs and having photocurrent as the output signal. At cryogenic temperature, cooled LWIR detectors show higher performance than uncooled detectors in general. For example, HgCdTe detectors have shown detectivity of 10^{11} Jones at lower than 100K [4]. Multi-quantum well (MQWIP) or quantum dots infrared photodetectors (QDIP) also achieved detectivity of 10^{11} Jones under ~77K [6,16,17]. Lastly, BIB trap LWIR detectors using shallow impurity states in highly doped Si or Ge have achieved detectivity as high as 10^{14} Jones, but the devices have to be operated at extremely low temperature (~10K) or the impurity states would be thermally excited to produce unacceptably high dark current [10]. For most applications, it is highly desirable to have room temperature LWIR detectors that are easy to fabricate at low cost, and can produce high detectivity, low noise equivalent power (NEP), and high frequency response much greater than 100Hz. However, few LWIR detectors reported to date can meet all these requirements. Most micro bolometers have limited frequency response, and most quantum detectors require cooling and complicated materials or processing. HgCdTe, being one of the prevailing choices for LWIR detectors, is expensive and difficult to grow and scale. Similar concerns also apply to MQWIP, quantum dots, T2SL, and BIB detectors.

In this chapter, a unique design for uncooled LWIR detectors using a combined structure of amorphous Ge (a-Ge) and amorphous silicon (a-Si), both intentionally undoped is presented. The a-Ge layer absorbs LWIR light and the a-Si layer produces carrier multiplication via cycling excitation process (CEP) as discussed in Chapter 2.

3.2. Device Processing

A 25nm thick a-Si layer is deposited at 270°C by plasma-enhanced chemical vapor deposition (PECVD) on a highly n-doped silicon substrate, followed by room temperature sputtering of a 100nm thick a-Ge layer as the absorption medium. After the a-Si and a-Ge deposition, 30µm diameter device mesas are photolithographically defined and dry etched with SF_6:C_4F_8. To passivate the mesa sidewall, Al_2O_3 (40 nm) and SiO_2 (200nm) are deposited by atomic layer deposition at 200°C and by PECVD at 270°C, respectively. Finally, a 18nm Cr/Au layer is deposited to form the top electrode with 10% transmission at 10.6µm wavelength light, and a 220nm Ti/Au layer is further deposited to form the top and ground contact pads. The cross-section and top view of the device structure are shown in Fig. 3.1.

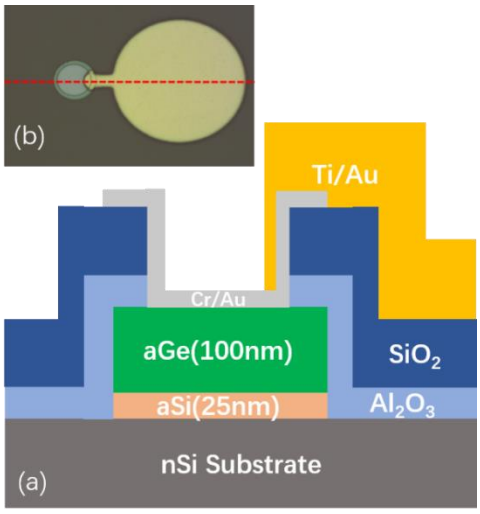

Figure 3.1: (a) Cross-sectional (not to scale) and (b) Top view of the device

3.3. Device Characterization

3.3.1. Characterization Methods

Dark current is measured with a Keysight B2900 source meter from 0V to -5V. Bias dependent photocurrent is measured by an RF spectrum analyzer, after being amplified by a

transimpedance amplifier (TIA). The RF spectrum analyzer also gives rise to the noise spectrum for noise equivalent power (NEP) measurement. To measure the device response between 2 Hz and 6 kHz, we use a chopper to modulate a CO_2 laser (10.6μm wavelength) operated at 100% duty cycle. To characterize the detector response at higher frequency than 6 kHz, we modulate the CO_2 laser output at 5 kHz and characterize the output power at higher (up to the 4th) harmonic frequencies as the input optical power. Using this approach, we are able to extend the range of measurement to 20 kHz. The laser spot on the device surface is 5×5 mm^2, producing an optical power density of 4mW/cm^2. The incident light power is calibrated with a commercial detector (Thorlabs: S401C). All measurements are performed at room temperature.

From the measured photocurrent at 1Hz resolution bandwidth from an RF spectrum analyzer, we calculate frequency-dependent responsivity ($R=I_{photo}/P_{optical}$), shot noise limited specific detectivity ($D^*=R/\sqrt{(2eJ_{dark})}$), and noise equivalent power ($NEP=\sqrt{A}/D^*$) under different bias voltage. In these expressions, A is the device area, e is magnitude of electron charge, $P_{optical}$ is the CO_2 laser power incident on the device area, and J_{dark} is the device dark current.

3.3.2. Results

We measure the device photo-response under 27nW CO_2 laser power modulated at different frequencies (DC to 20 kHz) and under different bias voltage. The bias dependent DC dark current and responsivity at 5kHz are shown in Fig. 3.2. We plot the responsivity between 2.5V and 5V bias here because, lower than 2.5V bias, the responsivity is too low to be measured reliably. Both the dark current and photo responsivity increase with the bias voltage. The detailed analysis of the device behaviors will be presented in section 3.4.

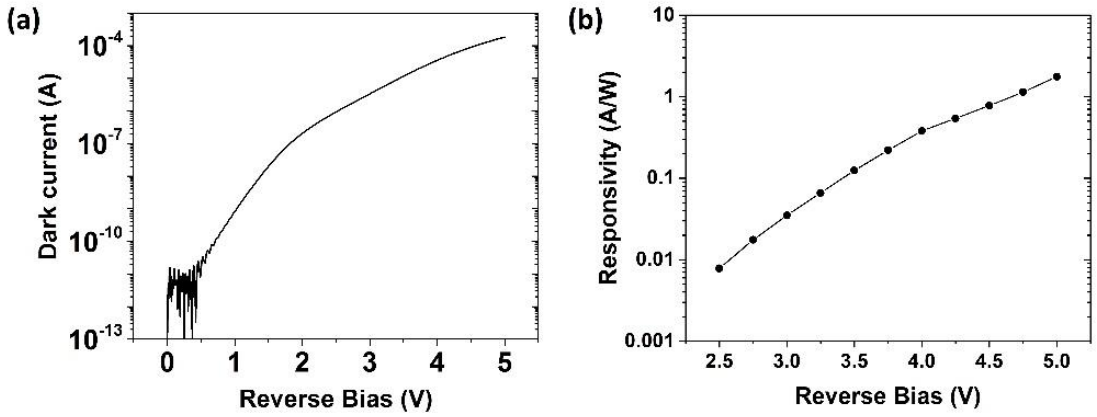

Figure 3.2: Bias dependent (a) DC dark current and (b) Responsivity at 5kHz under 27nW CO_2 laser illumination

Using the measured responsivity, we can calculate the specific detectivity (D^*) because above 2.5V, the dark current and the RF spectrum of the device show the dominant noise of the device is shot noise. The results are shown in Fig. 3.3. We observe the highest specific detectivity of 6×10^8 Jones and the lowest noise equivalent power (NEP) of 5pW/√Hz at 5V reverse bias with a 30μm diameter device at 10.6 μm wavelength. Unlike bolometers or thermopiles that measure thermal effects and have limited (usually <100 Hz) frequency response, our device can produce high detectivity and low NEP at 20 kHz frequency, limited by the CO_2 laser response.

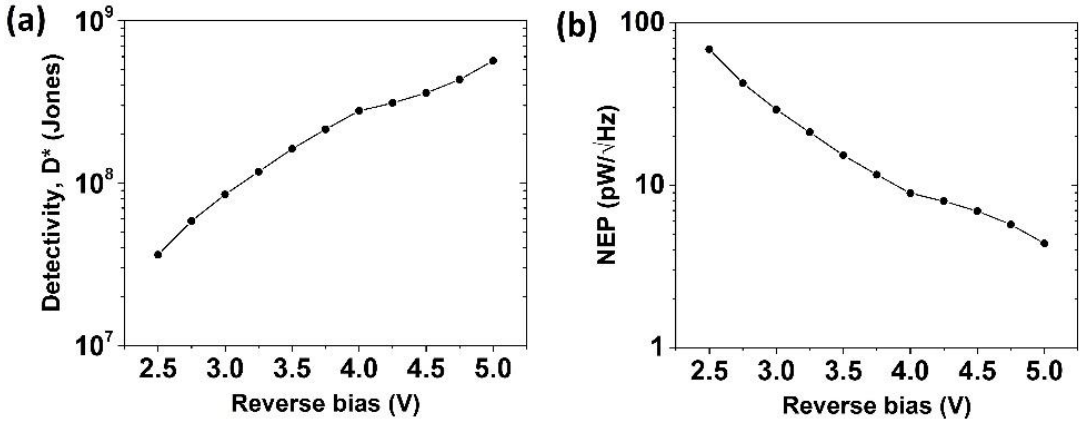

Figure 3.3: Bias dependent (a) Detectivity and (b) NEP of the device at 5kHz

Figure 3.4 shows the frequency dependence of device characteristics from 2 Hz to 20 kHz. We clearly observe that the device characteristics are divided into two regimes according to frequency. At 10 Hz or lower frequency, the device responsivity and detectivity reach 10 A/W and 7×10^9 Jones, which by themselves set a record value for uncooled LWIR detector, but the numbers drop rapidly above 10 Hz, showing the general property of thermal detectors. As a thermal detector, different materials of the device absorb the CO_2 laser power, causing temperature rise which subsequently increase dark current that is revealed as "photoresponse". However, what is more interesting and important is the higher frequency response of the detector. At higher than 100 Hz and up to 20 kHz, the maximum frequency we have measured, the device shows a photo responsivity of around 1.7A/W and detectivity of 6×10^8 Jones, and the values are nearly independent of frequency within measurement errors. The results indicate that above 100Hz, thermal effects vanish because of their slow response.

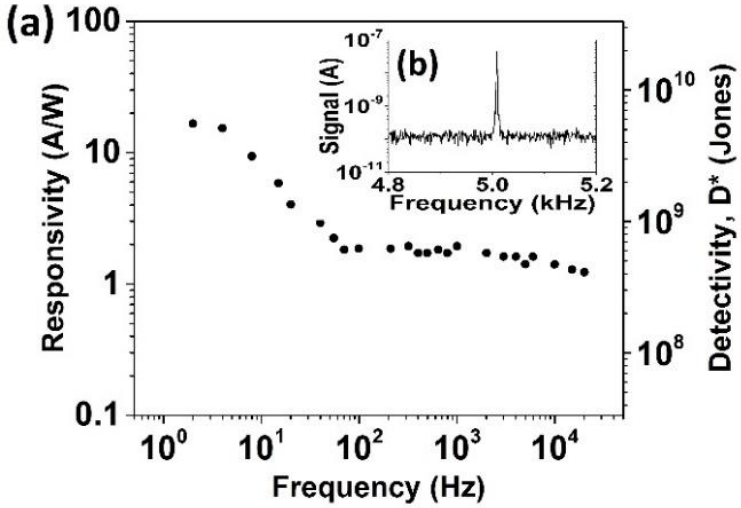

Figure 3.4: (a) Frequency dependent responsivity and detectivity of the device under 5V reverse bias (b) Photocurrent trace from RF Spectrum Analyzer at 5kHz laser modulation

Table 3.1 shows a comparison of our detector with other LWIR detectors that operate under room temperature. In spite of its simple structure and fabrication process, our device has shown

highly favorable performance in many key metrics. Compared with thermal detectors, our device has demonstrated much higher speed. Compared with quantum detectors, our detectors offer the best room temperature performance and are easiest to fabricate with low cost materials such as a-Ge and a-Si.

Table 3.1: Comparison of NEP (pW/√Hz) and specific detectivity, D^* ($\times 10^8$ Jones) for different uncooled LWIR detectors

Technology	λ(μm)	NEP	D^*
Quantum Detectors			
aGe/CEP (This work)	10.6	5	6
InAs QDIP [5]	9	N/A	6
MCT PC optically immersed [4]	9 – 10.6	>50[a]	5 – 1
MCT PVM optically immersed [4]	8 – 10.6	>167[a]	6 – 2
InAsSb PV [24]	8 – 11	1600 – 16000	0.6 – 0.06
T2SLs InAs/InAsSb on GaAs [7]	10.6	161	5
Type-II PC on GaAs [8]	8 – 12	1500[a]	1.3
Thermal Detectors (Frequency limited to 100Hz)			
VO_2 based Micro Bolometer [2]	8 – 12	N/A	1.9
$Si_xGe_yO_{1-x-y}$ Micro Bolometer [3]	8 – 12	N/A	11.9
Ni nano bolometer [25]	>10	8.7	0.15[a]
Thermopile Sensor [26]	8 – 13	N/A	2.9

[a]Calculated using reported detectivity or NEP and active device area

The frequency dependent characteristics suggest that our detector operates as a quantum detector (i.e. signal produced by photoexcited electrons or electron-hole pairs by absorption of LWIR photons) rather than a thermal detector at higher than 100Hz. One key question to answer is what quantum transition(s) is responsible for the device behaviors at this wavelength. Another important question is what signal amplification mechanism(s) take place to give the device its superior performance. In the following we propose a physical model and use carrier transport equations to analyze the optical excitation pathway and signal amplification mechanism for the LWIR detector.

To obtain information to help develop the physical model, we have measured the photoresponse of two test structures on n-Si substrate, one with a 100nm a-Ge layer and another with a 25nm a-Si layer. The test structure with 100nm a-Ge film produced responsivity of 0.01 A/W at 5kHz under 0.5V bias. On the other hand, the test structure with a 25nm a-Si layer showed very low LWIR responsivity (in the order of 10^{-4} A/W). This result indicates that it is the a-Ge layer that contributes to the primary photocurrent. The purpose of a-Si layer is to amplify the primary photocurrent via the CEP mechanism.

3.4. Device Model

Based on the above observation, we hypothesize that the main operation mechanism under high (>100Hz) frequency is due to photoexcitation of electrons from the bandtail states to the mobile states of the conduction band of a-Ge. The excited electrons in the mobile states have much greater mobility than those in the bandtail states and can cross the a-Ge/a-Si heterointerface to enter the a-Si layer where a high electric field exists under voltage bias. The a-Si layer provides efficient carrier multiplication via the cycling excitation process (CEP) reported in our earlier publications [19,22,23] producing high responsivity.

Assuming that photoexcited electrons are generated from electron transition between the bandtail states and the mobile states of conduction band of a-Ge, we can write continuity Eqs. (1) and (2) for electron concentrations in the mobile states of conduction band (n) and in the conduction bandtail (n_t).

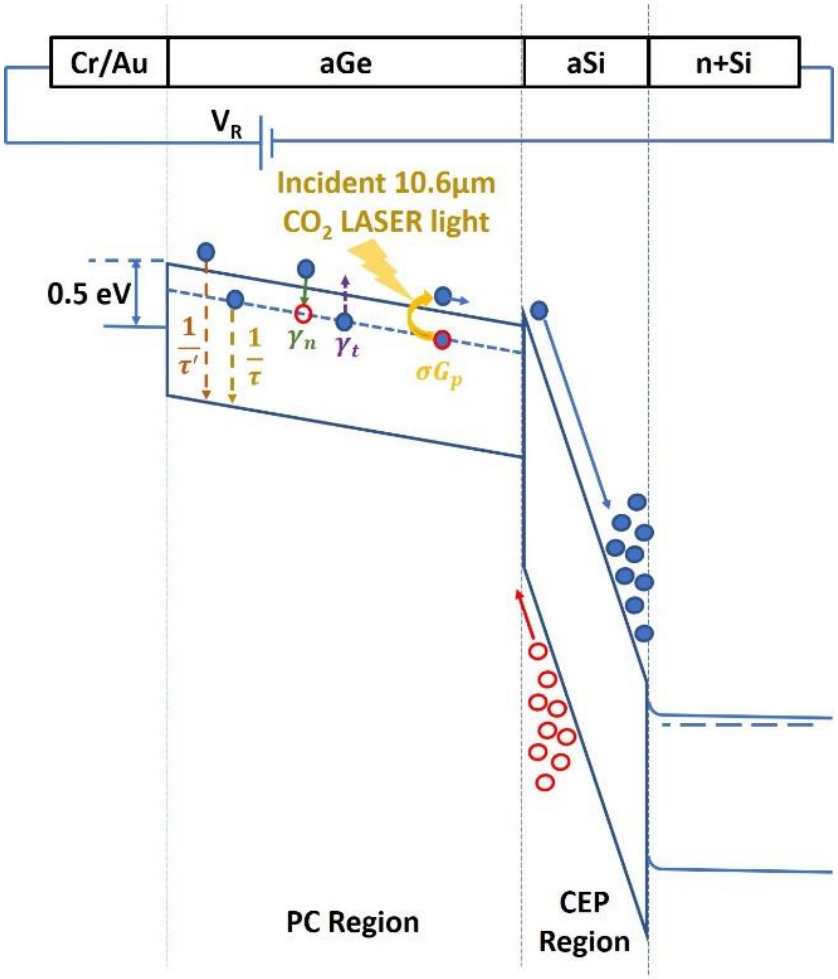

Figure 3.5: Band diagram of the device under reverse bias. Here, $\tau'^{-1}(\tau^{-1})$ represent generation recombination rate from conduction band (bandtail) to valence band, $\gamma_n(\gamma_t)$ are electron capture (emission) rate to (from) bandtail state, σG_p is electron generation rate via photoexcitation of bandtail states by incident LWIR photon flux

$$\frac{dn}{dt} = -n\gamma_n - \frac{n - n_o}{\tau'} + n_t\gamma_t + n_t\sigma G_p \qquad (1)$$

$$\frac{dn_t}{dt} = -n_t\gamma_t - n_t\sigma G_p - \frac{n_t - n_{to}}{\tau} + n\gamma_n \qquad (2)$$

where γ_t (γ_n) is the electron emission (capture) rate from (to) bandtail states to (from) the conduction band, $1/\tau$ ($1/\tau'$) is the thermal generation-recombination rate between bandtail states (conduction band) to the valence band, σ is the interaction cross section of a bandtail state electron and LWIR photon, and G_p represents the LWIR photon flux. In addition, n_o and n_{to} represent the

equilibrium electron concentration in the mobile states of conduction band and in the conduction bandtail of a-Ge, respectively. Hence the relation $n_o\gamma_n = n_{to}\gamma_t$ holds.

To write Eqs. (1) and (2), we have assumed $\frac{d}{dx}J_n \approx \frac{d}{dx}(env_d) \approx ev_d\frac{dn}{dx} \approx 0$ where J_n represents the electron current density in a-Ge and v_d is the drift velocity of electrons in the mobile states. Here we have ignored the current contribution by electron hopping over the localized states. We can express v_d in terms of electron transit time t_{tr} and a-Ge thickness d_{aGe} as $t_{tr} = d_{aGe}/v_d$.

After crossing the a-Ge/a-Si interface, electrons will experience bias-dependent CEP gain in a-Si. Since the energy barrier for a-Ge/a-Si interface is small for electrons, we assume 100% electron injection efficiency from the mobile states of conduction band of a-Ge to a-Si. Ignoring the drift velocity difference between electrons and holes in the mobile states of conduction and valence band for simplicity, we can represent the total particle current density, J, as

$$J = J_n G_{CEP} = env_d G_{CEP} \qquad (3)$$

where J is the sum of the electron current density and the CEP generated hole current density, as illustrated in Fig. 3.5.

By setting the *d/dt* terms to be zero for DC analysis and using the relation $n_o\gamma_n = n_{to}\gamma_t$, , n can be derived from Eqs. (1) and (2) as

$$n = n_o\left(1 + \sigma G_p \frac{n_{to}}{n_o} t_{life}\right) \qquad (4)$$

$$t_{life} = \frac{1}{\left(\gamma_n + \frac{1}{\tau'}\right) + \left(\gamma_t + \sigma G_p\right)\frac{\tau}{\tau'}} \qquad (5)$$

where t_{life} is the effective electron lifetime (i.e. the amount of time for an electron to stay in the mobile states of conduction band).

From Eqs. (3) - (5), we can find the dark current density (J_{dark}), photocurrent density (J_{photo}), and responsivity (R) as

$$J_{dark} = en_o v_d G_{CEP} \qquad (6)$$

$$J_{photo} = J - J_{dark} = e\sigma G_p n_{to} t_{life} v_d G_{CEP} \qquad (7)$$

$$R = \frac{J_{photo}}{h\nu G_p} = \frac{e}{h\nu}(\sigma n_{to} d_{aGe})\left(\frac{t_{life}}{t_{tr}}\right) G_{CEP} = \frac{e}{h\nu}\eta G_{PC} G_{CEP} \qquad (8)$$

To obtain Eq. (8), we have used the relations $t_{tr} = d_{aGe}/v_d$ and quantum efficiency $\eta = \sigma n_{to} d_{aGe} \sim \alpha d_{aGe}$ with α being the LWIR light absorption coefficient for a-Ge. The measured absorption coefficient at 10.6 μm for undoped aGe is ~50 cm^{-1} [27]. For a thin (100nm) layer of a-Ge, η is estimated to be in the order of 10^{-3}. This value may be overestimated since part of the measured light absorption is caused by photo excitation of holes from the valence bandtail states to the mobile states of valence band and those mobile holes enter the cathode directly without experiencing CEP gain.

In Eq. (8), the responsivity contains two signal amplification terms, the CEP gain produced in a-Si and the photoconductive gain in a-Ge defined by $G_{PC} = t_{life}/t_{tr}$ with t_{life} being the effective electron lifetime represented by Eq. (5) and t_{tr} the electron transit time across the a-Ge layer.

The above model shows that our device can operate as a "quantum detector" in which LWIR light excite electrons from the bandtail states to the mobile states of conduction band. Such excited electrons experience two gain mechanisms in series, the conventional photoconductive gain in a-Ge and the CEP gain in the high field a-Si region. The CEP gain is critical because the photoconductive gain is modest or in some case, negligible in our device. Due to the high density of bandtail states in a-Ge and high phonon emission rate for electrons to fall into the bandtail states from the mobile states, the effective lifetime for electrons to stay in the mobile states is in

picoseconds. On the other hand, the low mobility and low E-field in a-Ge (most E-field drops in a-Si layer) produces a transit time of the order of 10ps. As a result, the photoconductive gain $G_{PC} = t_{life}/t_{tr}$ in our device is modest. The device largely relies on the CEP gain to increase its photo responsivity and detectivity.

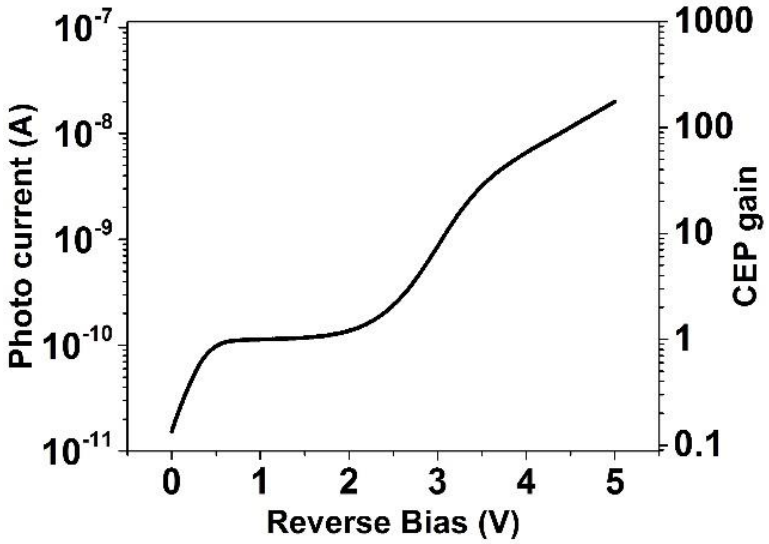

Figure 3.6: Photoresponse (at 639nm wavelength) of a device consisted of an a-Si layer on an n-Si substrate (same structure but without the a-Ge LWIR absorption layer) for characterization of CEP gain

Figure 3.6 shows the bias-dependent CEP gain under visible (639nm) light excitation from the same device structure without the a-Ge layer. Multiplying the responsivity of ~10^{-2} A/W for the a-Ge test structure by the CEP gain of over 100 from Fig. 6, we achieve the net responsivity of > 1A/W for the a-Si/a-Ge heterostructure device under 5V bias. This value agrees well with the measured responsivity (1.7 A/W) in Fig. 2(b). The result further confirms that CEP gain plays a key role in achieving high responsivity, high detectivity, and low NEP for our device.

3.5. Conclusion

A novel design for room temperature LWIR detector is demonstrated in this chapter. The device uses a-Ge for light absorption and a thin a-Si layer to produce CEP gain for photocurrent amplification. At 20kHz optical modulation, a 30μm diameter device has shown a detectivity value of 6×10^8 Jones, which is among the highest detectivity for room temperature LWIR detectors. The device shows a NEP value of 5pW/√Hz, the lowest value for all uncooled LWIR detectors. Frequency dependent measurements show the detector operates as a quantum detector above 100 Hz, and the CEP gain is key to its superior performance. The fast response, room temperature operation, high detectivity, low NEP, and simple and low-cost fabrication process make the device attractive to night vision, machine vision, autonomous driving and many other applications.

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J. Zhou*, **M.A.R. Miah***, Y. Yu, A.C. Zhang, Z. Zeng, S. Damle, I.A. Niaz, Y. Zhang, and Y.H. Lo, "Room-temperature long-wave infrared detector with thin double layers of amorphous germanium and amorphous silicon", Optics Express 27 (25), 37056-37064 (2019). ***-co-first author**

The dissertation author was a coauthor/ primary author of these papers.

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CHAPTER 4: PHYSICS BASED UNIFIED CIRCUIT MODEL FOR SINGLE PHOTON AND ANALOG DETECTOR

In this chapter, a unified circuit model for analog and single photon detector is presented. The applicability of the model is demonstrated with an optical amplifier for a sub-geiger mode detector operation. Additionally, the model is verified for passive quenching and integrated active passive quenching circuit design. The gain-bandwidth product of the gain medium from different materials are also predicted and experimentally verified with the model.

4.1. Motivation

In most prevalent equivalent circuit models for Geiger-mode detectors, a single-photon avalanche detector (SPAD) is modelled as an on-off switch with additional resistors, voltage sources and capacitors [11]–[14]. All parameters in the equivalent circuit are assigned from measured I-V response without relating them to the physical characteristics of the devices. For detectors made of different gain media (e.g. Si and InP) or having different designs, one cannot choose the equivalent circuit parameters to reflect such differences. On the other hand, there are a number of device models for SPADs that describe the device behaviors [15]–[18], but these device physics models, analytical or semi-empirical, cannot be directly converted into an equivalent circuit model and used for circuit simulations. In some cases, statistical behaviors including dark count rate and afterpulsing probability of SPADs were analytically modelled and added to the equivalent circuit model in hardware description language [19], [11], [12]. However, the parameters of the model are inconvenient to use for circuit designers as they are not attainable from the basic material properties or device geometries. In addition, almost all circuit models for SPADs are limited to Geiger mode operation or for some specific quenching circuit design [20]. On the other hand, when designers need to make tradeoffs between sensitivity and dynamic range

for different system requirements, the design can involve detectors that operate between Geiger mode, sub-Geiger mode, and analog mode. Therefore, it is most desirable to create a unified circuit model for detectors with avalanche or CEP gain that work for all modes of operations, i.e. analog mode, sub-Geiger mode, and Geiger mode. This is equivalent to a transistor circuit model that works for the transistor to be in linear, saturation, or subthreshold conditions. Additionally, we wish to have all the parameters of the equivalent circuit related to and obtained from the device geometries and material properties. In this manner, as the designer chooses detectors made of different materials or having different geometries, an equivalent circuit model for the chosen detector types becomes readily available to show how different detectors can affect the system performance.

In this chapter, we present a unified equivalent circuit model for photodetectors with built-in carrier multiplication gain such as avalanche photodetectors (APDs) and cycling excitation process (CEP) detectors. The equivalent circuit model has two salient features: (i) all the parameters in the equivalent circuit model can be obtained from the material parameters and rooted in device physics, and (ii) the circuit model works for all modes of operation (analog, sub-Geiger-mode, and Geiger-mode) and the transition between different modes is smooth without artificial separation of the circuit models between different modes of operation. When the device bias is switched between above-breakdown and below-breakdown voltage, the changes in device behaviors occur naturally, according to device physics. For example, below breakdown, the detector characteristics are subject to the gain-bandwidth limit while above breakdown (i.e. in Geiger mode), the device properties are no longer related to the gain-bandwidth product. Another unique feature is that the model treats dark current and photon current as individual electrical pulses, each of which contains a single photon or carrier, thus enables simulations of quenching

and recovery times, bias-dependence and frequency dependence of single-photon detection efficiency, and many statistic characteristics of the device. For instance, the model can show how increased dark current reduces the single-photon detection efficiency and shows circuit designers the limit of device dark current above which the detector can no longer detect single photons under Geiger-mode. In Geiger-mode operation, detectors require passive or active quenching when operating continuously. The dynamic switching of the detectors between above breakdown and below breakdown bias prefer a unified circuit model applicable to all bias voltage and showing the dynamics of carrier multiplication. All parameters in our circuit model are related to fundamental material and design parameters: impact ionization coefficients for electrons and holes based on the local-field model [25], [26], and the carrier transit time across the multiplication region.

4.2. Derivation of the Model

The current of a photodetector is composed of particle current and displacement current. Particle current is due to the flow of electrons and holes generated by photon absorption, dark current, and carrier multiplication such as impact ionization or CEP effect [1], [21]. Displacement current is due to charging/discharging of the device capacitance (C_j). We describe the model for the particle current next.

For illustration purpose, here we assume that the photoexcited carriers are produced in a p-doped layer next to the carrier multiplication region. As a result, being minority carriers in p type semiconductors, photoexcited electrons are injected into the gain medium to initiate the multiplication process. We also assume that only one photo- or thermally excited carrier is injected into the gain region within the carrier transit time (t_r) across the high-field gain region, typically 1 to 10ps depending on the device structure. For example, if the device has a primary dark current of 1.6pA, there is one thermal electron in the gain region every 100 ns, which is much longer than

the transit time. This satisfies the condition that at most one electron is injected into the gain region to initiate carrier multiplication within a transit time, which is regarded as the smallest time unit in our model. In case the incident light is strong, and the above condition is not satisfied, we can divide a single detector into units of small detectors in parallel such that each detector unit meets the above criterion. In most cases of single photon detector, however, the light intensity is low enough that it is not necessary to divide the detector into multiple units for circuit simulations.

Figure 4.1 (a) depicts a series of carrier generation events triggered by the injection of a single electron produced by photon absorption or thermal generation. It is assumed that the first electron is injected into the gain region at t=0 and it generates M_n second generation e-h pairs within a duration of t_r. Subsequently, these generated holes at t_r excite the 3rd generation e-h pairs with a multiplication factor M_p when time reaches $2t_r$, while the original electrons produced in the first t_r period leave the cathode as particle (electron) current. At $3t_r$, the 3rd generation electrons excite new e-h pairs with a multiplication factor M_n while the holes produced in the previous cycle leave the anode as particle (hole) current. To summarize the above process, we have electrons experience gain during the time intervals from $2Kt_r$ to $(2K+1)t_r$ and holes experience gain from $(2K+1)t_r$ to $(2K+2)t_r$, where $K = 0, 1, 2, 3$ .... Notably, as the above cycling process, initiated by a single electron injection at t=0, goes on, new photo- or thermally excited carriers can be injected into the gain region to start their own carrier multiplication cycles at different times, and the net particle current is the summation of all these events. Here we have simplified the carrier multiplication process by setting the smallest time increment to be carrier transit time and assuming that under high E-field, electrons and holes have the same transit time or saturation velocity. The first approximation can be improved by choosing a smaller time interval (e.g. a fraction of transit time), and the second approximation can be easily changed by replacing t_r with

$t_{r,n}$ and t_{rp} (i.e. transit time for electrons and holes). The mathematical expressions will be more complicated, but the SPICE implementation is essentially the same.

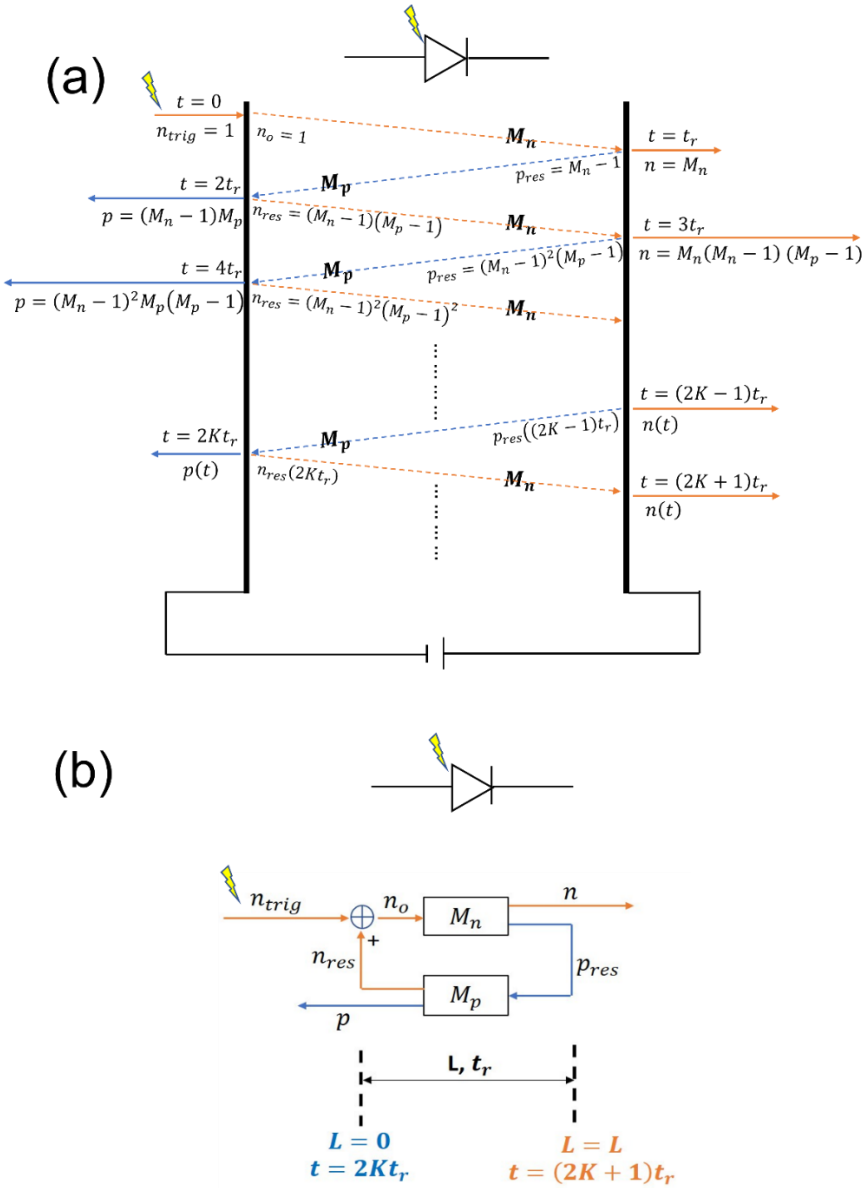

Figure 4.1: Carrier multiplication processes in the multiplication region of the device. (a) time evolution of a single triggering event and (b) block diagram. Here, t_r is the carrier transit time, L is the length of multiplication (gain) region, n_{trig} represents the triggering event (i.e. primary photoexcited or dark carrier injected into the gain region only at the even multiples of t_r (n_{trig} is 0 or 1 for a single electron), n_o is the total number of electrons experiencing the gain, $M_{n(p)}$ is multiplication factor for electrons(holes), $n(p)_{res}$ is the number of electrons(holes) remaining in the gain region, and n(p) is the number of electrons(holes) leaving the device within $2t_r$ to produce the particle current, K (K=0, 1, 2…) is a measure of time in the unit of $2t_r$.

The above process can be represented by a block diagram in Fig. 4.1(b), in which M_n and M_p are single-path carrier multiplication factor for electrons and holes, and their value depends on the voltage drop in the gain region. Next, we will derive the expressions for gain, particle current, and gain-bandwidth product.

Prior to the first triggering event at t=0, we set the initial state of the device as follows:

$$n_{res}(0) = 0, p_{res}(0) = 0, n(0) = 0, p(0) = 0 \qquad (1)$$

Here, n_{res} (p_{res}) is the number of electrons (holes) remaining in the gain region, and n(p) is the number of electrons(holes) leaving the device to produce electron (hole) particle current within a duration of $2t_r$. The results in Figure 4.1(a) can be summarized by the following equations:

$$n_o(t = 2Kt_r) = n_{trig}(t = 2Kt_r) + n_{res}(t = 2Kt_r) \qquad (2)$$

$$n(t = (2K + 1)t_r) = n_o\,(t = 2Kt_r)M_n \qquad (3)$$

$$p_{res}(t = (2K + 1)t_r) = n_0(t = 2Kt_r)(M_n - 1) \qquad (4)$$

$$p(t = 2(K + 1)t_r) = n_o(t = 2Kt_r)(M_n - 1)M_p \qquad (5)$$

$$n_{res}(t = 2(K + 1)t_r) = n_o(t = 2Kt_r)(M_n - 1)\big(M_p - 1\big) \qquad (6)$$

Here we divide time into discrete intervals by the unit of carrier transit time t_r. For an electron injected into the gain medium at t=0, the electron current is produced at each $(2K + 1)t_r$ (K =0, 1,2,3..) when electrons leave the cathode (Eq. 3) and the hole current is produced at each $2Kt_r$ (K =1,2,3..) when holes leave the anode (Eq.5). Equation (2) describes the number of electrons inside the gain region, being equal to the sum of the electrons excited by the on-going amplification process, n_{res} and new injected electron, n_{trig}, that will initiate new cycles of amplification ($n_{trig} = 0\ or\ 1$). Equations (4,6) describe the number of holes and electrons inside the gain medium. Using Fig. 1, the values of n, p, n_o, n_{res} and p_{res} at any given time can be calculated.

In (2)- (6), we choose the smallest time unit to be t_r. Within this time interval, the number of carriers inside the device should be at least 1 under Geiger mode (i.e. do not allow fractional photoexcited electrons). We enforce this condition by assuming that if at any moment the number of electrons entering into the gain region, n(t), falls below 1, we consider that no electrons are left inside the gain region and the carrier multiplication process stops, i.e.

$$n_o(t) = \begin{cases} 0;\ n_o(t) < 1 \\ n_0(t) \text{ from (2)};\ n_o(t) \geq 1 \end{cases} \qquad (7)$$

We enforce the condition in Eq. (7) only in Geiger mode. In other modes where we are dealing with ensemble average, we accept the condition that the electron(hole) number can be lower than one as the carrier multiplication process continues.

We calculate the particle current (I_{part}) by multiplying a factor of $e/2t_r$ to the number of electrons and holes leaving the device within each duration of $2t_r$. Then,

$$I_{part}(2(K+1)t_r) = \frac{\mathrm{e}}{2\mathrm{t_r}\left[n\big((2K+1)t_r\big) + p(2(K+1)t_r)\right]} \qquad (8)$$

From Eqs. (2-6) and the schematic in Fig. 1, we can find the bias (U) dependent DC gain since M_n and M_p are both bias dependent.

$$Gain_{DC}(U) = \frac{\sum_{K=0}^{\infty} \left[n\big((2K+1)t_r\big) + p(2(K+1)t_r)\right]}{\sum_{K=0}^{\infty} n_{trig}(2Kt_r)} \qquad (9.A)$$

For a single triggering event,

$$Gain_{DC}(U) = M_n + M_p(M_n - 1) + M_n(M_n - 1)\big(M_p - 1\big) + M_p(M_n - 1)^2\big(M_p - 1\big)$$
$$+ M_n(M_n - 1)^2\big(M_p - 1\big)^2 + M_p(M_n - 1)^3\big(M_p - 1\big)^2 + \cdots$$

$$\Rightarrow Gain_{DC}(U) = \left[M_n + \frac{M_p}{M_p - 1}\right]\left[1 + (M_n - 1)\left(M_p - 1\right) + (M_n - 1)^2\left(M_p - 1\right)^2 + \cdots\right]$$

$$- \frac{M_p}{M_p - 1}$$

$$\Rightarrow Gain_{DC}(U) = \left[M_n + \frac{M_p}{M_p - 1}\right]\left[\frac{1}{1 - (M_n - 1)\left(M_p - 1\right)}\right] - \frac{M_p}{M_p - 1}$$

$$\Rightarrow Gain_{DC}(U) = \frac{M_n + M_p(M_n - 1)}{1 - (M_n - 1)\left(M_p - 1\right)} \qquad (9.B)$$

From (9), gain approaches infinity when $(M_n - 1)\left(M_p - 1\right) = 1$, which determines the breakdown voltage, (V_{BD}). We can also infer that, above the breakdown voltage, $(M_n - 1)\left(M_p - 1\right) > 1$.

Next, we calculate the gain decay time (τ_{decay}) in analog or sub-Geiger mode when the voltage is below V_{BD} and gain build-up time (τ_b) when the voltage is greater than the breakdown voltage and the device is in Geiger mode. From Fig. 1(a), we find that under a single triggering event, the total number of electrons and holes at the end of K^{th} round trip (i.e. $t=2Kt_r$) is

$$N(2Kt_r) = n_{res}(2Kt_r) + p(2Kt_r) \qquad (10.A)$$

For a single triggering event at t=0 and using (2)-(6) we can write,

$$n_{res}(2t_r) = (M_n - 1)\left(M_p - 1\right); p(2t_r) = M_p(M_n - 1)$$

$$n_{res}(4t_r) = (M_n - 1)^2\left(M_p - 1\right)^2; p(4t_r) = M_p(M_n - 1)^2\left(M_p - 1\right);$$

In general,

$$n_{res}(2Kt_r) = (M_n - 1)^K\left(M_p - 1\right)^K \qquad (10.\mathrm{B})$$

$$p(2Kt_r) = M_p(M_n - 1)^K\left(M_p - 1\right)^{K-1} \qquad (10.C)$$

Using (10.2) and (10.3), N can be written as,

$$N(t = 2Kt_r) = (M_n - 1)^K \left(M_p - 1\right)^K \left[1 + \frac{M_p}{M_p - 1}\right]$$

$$\Rightarrow N(t = 2Kt_r) = \frac{2M_p - 1}{M_p - 1} e^{K \ln\left[(M_n - 1)(M_p - 1)\right]}$$

$$\Rightarrow N(t = 2Kt_r) = \frac{2M_p - 1}{M_p - 1} e^{\frac{t}{2t_r} \ln\left[(M_n - 1)(M_p - 1)\right]} \qquad (10.D)$$

In Eq. (10), we define τ_{decay} and τ_b as

$$\tau_{decay} = -\frac{2t_r}{\ln\left[(M_n - 1)\left(M_p - 1\right)\right]}; U < V_{BD} \qquad (11.A)$$

$$\tau_b = \frac{2t_r}{\ln\left[(M_n - 1)\left(M_p - 1\right)\right]}; U \geq V_{BD} \qquad (11.B)$$

From (9) and (11-A), the gain-bandwidth product of the detector under the condition $U < V_{BD}$ (i.e. in analog mode or sub-Geiger mode) can be approximated as

$$GB \cong -\left[\frac{M_n + M_p(M_n - 1)}{1 - (M_n - 1)\left(M_p - 1\right)}\right] \frac{\ln\left[(M_n - 1)\left(M_p - 1\right)\right]}{4\pi t_r} \approx \frac{M_n + M_p(M_n - 1)}{4\pi t_r} \qquad (12)$$

If the detectors are triggered by photoexcited holes, a similar expression for Eqs. (9,11,12) can be obtained by switching the subscript n and p in all terms in the equations.

The dependence of $M_{n(p)}$ on the voltage drop in the device can be represented as

$$M_n = e^{\alpha(U)L}; M_p = e^{\beta(U)L} \qquad (13)$$

where α and β are the multiplication coefficients for electrons and holes, and L is the thickness of the gain medium. We use empirical formulas for the electron and hole multiplication coefficients based on the local-field model that is widely used by device simulation programs such as Silvaco [27].

$$\alpha = A_n e^{-\left(\frac{B_n L}{U}\right)^{c_n}} ; \beta = A_p e^{-\left(\frac{B_p L}{U}\right)^{c_p}} \qquad (14)$$

A_n, A_p, B_n, B_p, c_n and c_p are material specific parameters that can be found in numerous publications (Table 4.1). Multiplication coefficient models can be expanded to incorporate non-local effects using Eq. 15 in [25]. Transit time (t_r) is the time required for the carrier to cross the gain region and can be approximated from the length of the gain region and carrier velocity. For example, in Si, the saturation velocity of both electron and hole is $\sim 10^7$ cm/sec, producing a transit time of 1ps for a gain region of 100nm. Impact ionization coefficient parameters of Si, L = 100nm and t_r = 1ps are used as default parameters for the circuit model.

Finally, to calculate the total detector current, we need to include displacement current through the device capacitance (Cj) in parallel with the particle current. It is to be noted that under Geiger mode, when the device is quenched by an external quenching circuit, particle current decreases rapidly and the device current is primarily produced by the displacement current through C_j. 1pF is used as the default value of the device capacitance C_j in our simulations.

Table 4.1: Empirical impact ionization coefficients of different materials

Material	Field (kV/cm)	A_n ($x10^5$ cm^{-1})	Bn ($x10^5$ cm^{-1})	c_n	A_p ($x10^5$ cm^{-1})	B_p ($x10^5$ cm^{-1})	c_p
Si [26]	400 – 800	7.03	12.3	1	6.71	16.9	1
InP [25], [28]	560 - 1250	2.32	8.46	2	2.48	7.89	2
$In_{0.52}Al_{0.48}As$ [29]	220 – 980	2.2	8.9	1.71	2.95	11.5	1.71
GaAs [25]	1100 - 1400	6.39	16	0.9	5.92	15.5	0.95
4H-SiC [30]	900 – 4000	27.8	105	1.37	35.1	103	1.09

Fig. 4.2(a) shows the device gain using Eqs. (9,13,14) with the default values of the model. The breakdown voltage is found to be 6.3V. The gain decay time below breakdown and gain buildup time above breakdown are plotted in Fig. 4.2(b) using the relations in Eq. 11. As expected, the gain decay time increases when the device approaches breakdown, limited by the gain-

bandwidth product. This can limit device sensitivity for photon counting in sub-Geiger mode. Also note that from Fig. 4.2(b), the gain buildup time decreases as the excess voltage (i.e. overbias above the breakdown voltage) increases. The model suggests that in Geiger-mode operation, detectors are not limited by the gain-bandwidth product and faster response can be achieved by increasing the overbias, which reduces the gain buildup time according to Eq. 11(b).

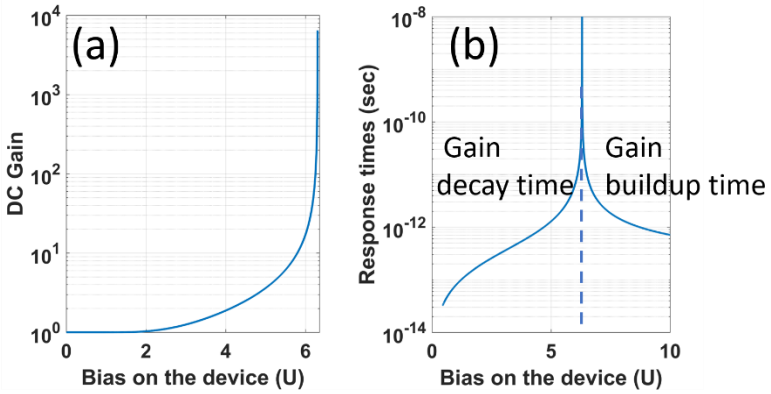

Figure 4.2: (a) DC gain dependence on device bias according to Equation (9) for a Si APD with a 100nm multiplication layer. (b) Gain decay time and gain build up time dependence on device bias according to equation (11). Below the breakdown voltage of 6.3V, the plot represents decay time (τ_{decay}) and above breakdown voltage the plot represents gain build up time (τ_b).

4.3. PSpice Implementation

We implement the device model using behavioral and circuit components in Orcad PSpice [31] as an example. This model can also be implemented in Cadence Spectre [32] by importing this PSpice model. Figure 4.3(a) illustrates the implemented model using different behavioral PSpice components. V_trigger denotes the incoming triggering pulse and V_Anode and V_cathode represent the device anode and cathode voltage, respectively. At every instant, the model calculates bias (V_bias_on_dev) dependent ionization coefficients, i.e. α ,and β from Eq. (14) and multiplication factors, M_n, M_p from Eq. (13). The particle current I_part is set to be 0 before the first triggering event. Once a single triggering event is registered by ntrig =1 at $t=t_1$, the multiplication process starts and values of n, p and I_part at $t=t_1+2t_r$ are calculated. Note that,

V_bias_on_dev($t=t_1+2t_r$) is also computed from the anode voltage at $t=t_1$ for numerical stability. Laplace blocks are used to realize the delay functions, and expressions from Eqs. (2)-(8), (13), (14) are implemented by 1 input and general purpose ABM blocks. For a note, ABM delay block can also be used in lieu of Laplace blocks for recent versions of PSpice. Even though PSpice simulates circuits under arbitrarily chosen time steps, the output current is only valid at the multiple of $2t_r$. Therefore, it is recommended to use 3-5 times of $2t_r$ as the "Maximum Step Size" in the "transient" options of PSpice such that PSpice arbitrary time steps are smaller than $2t_r$ and Laplace block does not show any non-causal warning. Finally, device capacitance is placed in parallel with the calculated particle current, I_part, to get the total current of the device. Fig. 4.3(b) shows the derived sub-circuit symbol from the model components. Device is triggered by the input pulse applied at terminal 1 (Trigger) of the symbol. Terminal 2 and terminal 3 represent the cathode and anode connection of the device. Since the particle current is calculated every $2t_r$, the input pulses have a width of $2t_r$ and subsequent inputs are separated by a time interval greater than $2t_r$. The amplitude of the pulse represents the number of photon/dark carrier per pulse. Moreover, if the DC primary dark/photo current, Ip, is known, then triggering pulses by primary dark/photo current need to be separated by a time interval of e/Ip. In cases that e/Ip becomes smaller than $2t_r$ due to a very high dark/photo current, the detector can be divided into identical subunits connected in parallel. Model shown in Fig. 4.3 along with the default parameters are used for simulations in this chapter.

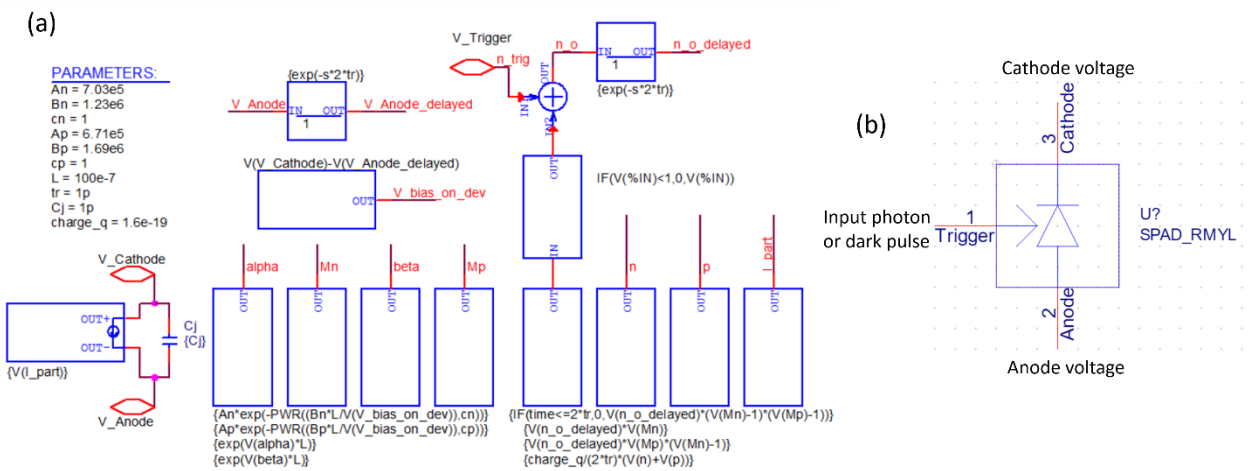

Figure 4.3: (a) Orcad PSPICE implementation of the model using Eqs. (2) – (14). (b) Modelled sub-circuit symbol used for different applications.

Library file .LIB of the model is shown below:

```
* source DEVICE_MODEL
*$
.SUBCKT SPAD_RMYL Trigger V_anode V_cathode +PARAMS: charge_q=1.6e-19 an=7.03e5
bn=1.23e6 cn=1 +ap=6.71e5 bp=1.69e6 cp=1 l=100e-7 cj=1p tr=1p
E_LAPLACE1      V_ANODE_DELAYED 0 LAPLACE +{V(V_ANODE)} {({exp(-s*2*tr)})/(1)}
E_ABM21         V_BIAS_ON_DEV 0 VALUE
+{ V(V_CATHODE)-V(V_ANODE_DELAYED)    }
E_ABM24         MN 0 VALUE { {exp(V(ALPHA)*L)}    }
E_ABM23         BETA 0 VALUE
+{{Ap*exp(-PWR((Bp*L/V(V_BIAS_ON_DEV)),cp))}}
E_ABM25         MP 0 VALUE { {exp(V(BETA)*L)}}
E_ABM22         ALPHA 0 VALUE
+{{An*exp(-PWR((Bn*L/V(V_BIAS_ON_DEV)),cn))}}
E_ABM11         I_PART 0 VALUE
+{{charge_q/(2*tr)*(V(N)+V(P))}}
E_ABM31 P 0 VALUE
+{{V(N_O_DELAYED)*V(MP)*(V(MN)-1)}}
E_ABM30  N 0 VALUE { {V(N_O_DELAYED)*V(MN)}}
E_SUM1  N_O 0 VALUE {V(TRIGGER)+V(N83646)}
E_ABM26   N83642 0 VALUE
+{{IF(time<=2*tr,0,V(N_O_DELAYED)*(V(MN)1)*(V(M+P)-1))}}
E_LAPLACE6     N_O_DELAYED  0
+LAPLACE {V(N_O)} {({exp(-s*2*tr)})/(1)}
E_ABM33 N83646 0 VALUE +{IF(V(N83642)<1,0,V(N83642))}
G_ABMI1 V_CATHODE V_ANODE VALUE +{{V(I_PART)}}
C_Cj  V_ANODE V_CATHODE  {Cj}  TC=0,0
.ENDS
*$
```

4.4. Application of the Model

We demonstrate the universal applicability of our model by simulating devices operating in different modes (sub-Geiger mode and Geiger-mode) with different circuits. We also show how material properties of the gain medium can affect the device performance.

4.4.1. Impulse Response of the Device

We simulated the impulse response of the device in different modes of operation. Figure 4.4a shows the device response under low DC gain of around 17 (at 6V bias) when the device is triggered by a single electron. As the bias voltage is close to 6.3V to achieve a DC gain of 1895, the device response in sub-Geiger mode is slowed down significantly from 25ps to 2.5ns, as shown in Fig. 4.4(b). Due to the slow response time, even though the DC gain is high, the peak amplitude of the device response does not increase substantially compared to the peak amplitude in linear mode. Figure 4.4(c) shows the Geiger mode response at 0.7V excess bias. The output current rises exponentially within a very short time, thus requiring a quenching circuit to bring the bias below breakdown to prevent device damage.

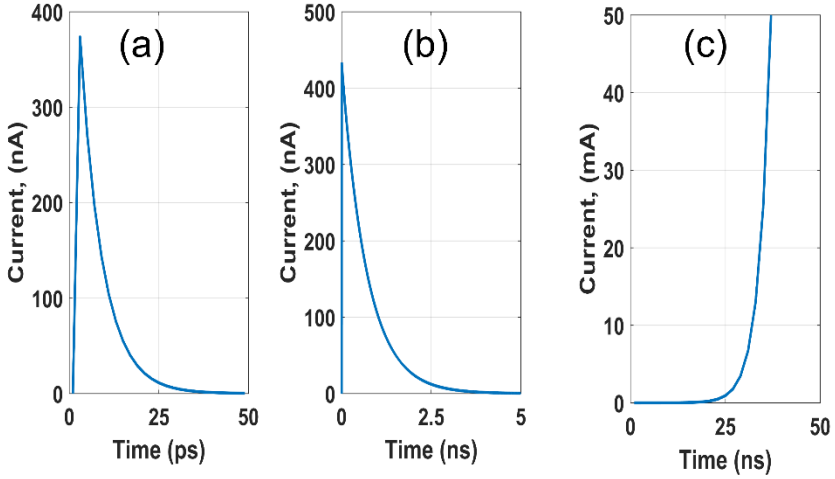

Figure 4.4: Impulse response of the device in (a) Linear mode (6V) with a gain of ~17, (b) Sub-Geiger mode with a DC gain of ~1895, and (c) Geiger mode (0.7V excess bias). The Geiger mode current response rises exponentially with time, thus requiring quenching.

4.4.2. Sub-Geiger Mode

Sub-Geiger mode operation can be used for detection of a few photons although with very low noise amplifiers, the device can achieve single photon sensitivity and even photon number resolving capabilities [33]. By integrating a charge sensitive amplifier (CSA) with the detector in sub-Geiger mode and using the equivalent circuit in Fig. 4.3 and parameter values of Si in Table 4.1, we show the circuit response in Fig. 4.5(b). For a DC gain of 1895, the peak amplitude of the output is around 142μV when triggered by a pulse containing 3 photons. As shown in Fig. 4.5(c), the output amplitude rises exponentially with the bias voltage in sub-Geiger mode, which stresses the importance of bias stability. Figure 4.5(d) shows the simulated circuit response to different number of photons. The device output increases with the photon number, thus providing a wider dynamic range than Geiger-mode operation. Using this example, we show that our detector circuit model can be used with an external circuit to simulate sub-Geiger mode characteristics.

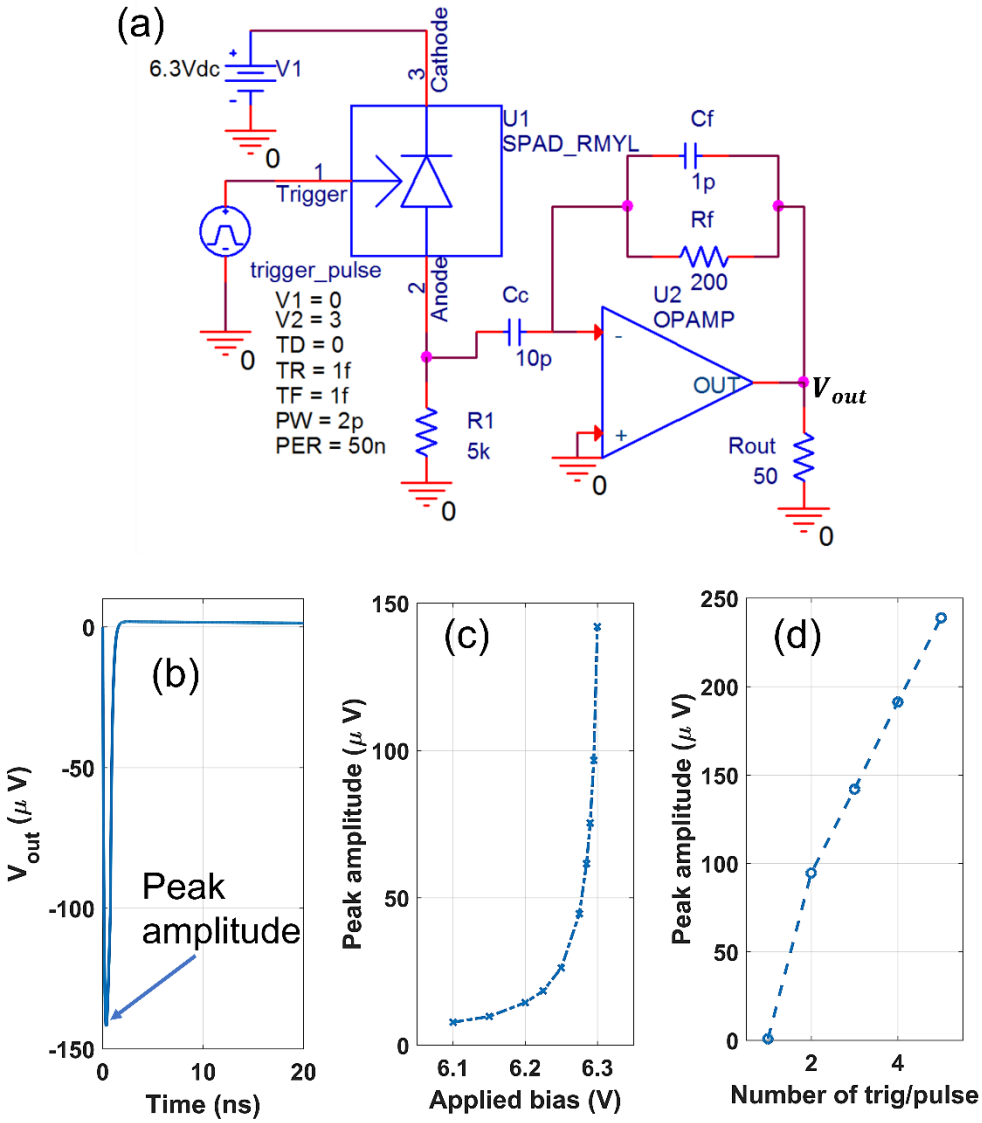

Figure 4.5: Simulation of sub-Geiger mode operation with the detector biased for a DC gain of 1895. (a) Simulated circuit diagram in PSpice. (b) Response at the output of a TIA. The TIA integration time is around 1.25ns. (c) Peak amplitude of the output voltage under different applied bias. (d) Dependence of the peak output amplitude on the number of photoexcited carriers per pulse.

4.4.3. Passive Quenching Circuit

For single photon detection in Geiger mode, a quenching circuit is needed to avoid device damage and to reset the device after detection of each triggering event. Next, we apply our detector model in a passive quenching circuit (PQC).

The passive quenching circuit in Fig. 4.6(a) uses a 100 kΩ resistor. The device is originally biased at 7V (0.7V excess bias) and the output signal is obtained from the 50Ω sensing resistor. We vary the rate of incoming photons to show the effect of recovery time and the performance limits for passive quenching circuits. Figure 4.6(b) shows the device response to a series of single photon events separated by 40ns. The red arrows indicate the photon arrival times. The device responds strongly to the first triggering event, but the output responses to the subsequent events become much less pronounced because an interval of 40ns is too short for the detector to be fully recovered after quenching. The simulation shows that after 200ns or from the 6^{th} triggering event on, the voltage swing across the device, $V_{Cathode}$-V_{Anode}, is only between 6.2V and 6.4V, about $\pm 0.1V$ around the breakdown voltage, and never reaches the original value of 7V across the detector. The recovery time of a passive quenching circuit is determined by the time constant $(R_{passive}+R_{sense})Cj$ (≈500ns for the simulated circuit), which explains why the circuit cannot support single photon triggering events separated by 40ns. If we increase the time interval between single photon pulses to 1.2μs, the detector has time to be fully recovered and the output signal can reach the full level, as shown in Fig. 4.6(c).

We also simulated a Si APD reported in [50] with a passive quenching circuit. The default Si parameters for impact ionization coefficients, $L = 1.5\mu m, t_r = 15ps$ and $C_j = 37.44fF$ [50] were used as the model parameter. C_j was extracted from the single photon gain curve of reported in [50]. The computed breakdown voltage was found to be 42.9V which was almost same as 43V, reported in [50]. Fig. 4.7(a) shows the amplified output voltage of the passive quenching circuit in Fig. 4.7(b) with R_q=250k and $V_{EX} = 1.6V$. The simulation result matches with the experiment very well.

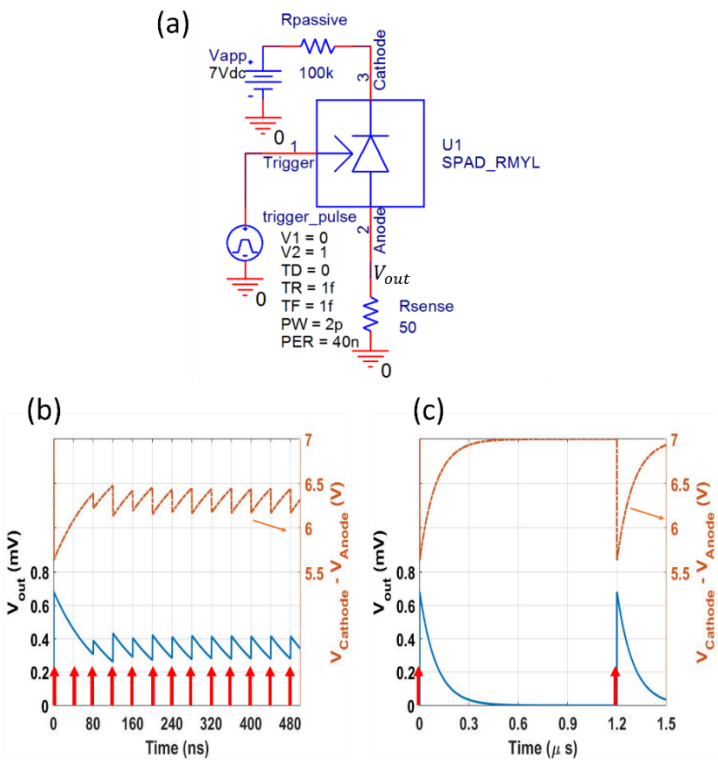

Figure 4.6: Simulation of a Geiger-mode detector with passive quenching circuit (PQC) using our model. (a) Simulated circuit in PSpice at 0.7V excess bias. (b) V_{out} and actual voltage drop ($V_{cathode}$ - V_{anode}) on the device with 40ns periodic triggering events. Device quenches after the first triggering event and cannot fully recover due to the slow recovery time. (c) Device response to triggering events separated by 1.2µs. The detector can fully recover in this case. Red arrows mark the incidence of the triggering events for (b) and (c).

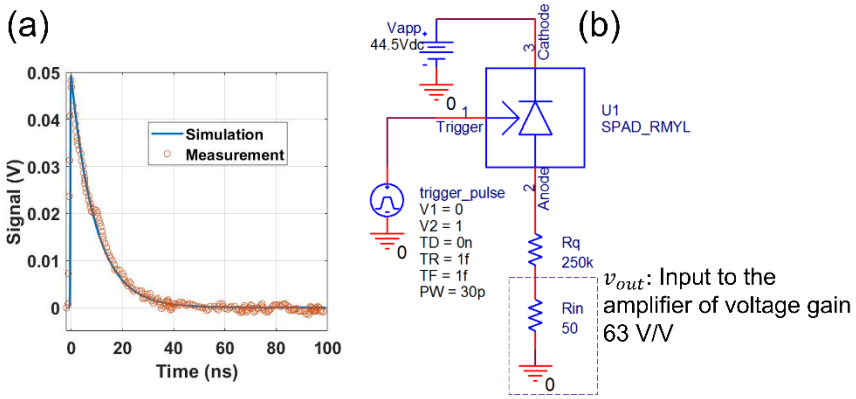

Figure 4.7: (a) Measured and simulated output signal of the circuit. (b) Schematic of the simulated circuit.

4.4.4. Mixed Active-Passive Quenching Circuit

To overcome the problem of slow recovery time for passive quenching circuits, active quenching circuits (AQC) with a fast recovery time can be integrated with Geiger-mode detectors [34], [35]. A high performance AQC requires elaborated design and optimization of circuit configuration and components, which is outside the scope of this paper. Instead we simulate an ideal mixed active-passive quenching circuit [12] with our detector model to demonstrate the viability of the detector model in Geiger mode operation with an active quenching circuit.

Figure 4.8(a) shows the circuit configuration in PSpice. When a photon or dark pulse triggers the detector, the carrier multiplication process is initiated and the detector is at first passively quenched by the resistors R_L and R_s. When the voltage V_{out} across R_s rises above the comparator threshold (1.5mV), the control logic block is activated and in 3ns, the delay block in the control logic closes the S_quench switch, reducing the voltage drop in the detector to 3V, which is about 3.3V lower than the breakdown voltage. After holding the detector at the quenched state for 3ns, the detector is reset to its initial state via the S_reset switch and the delay blocks in the control logic. In this design, in 6.5ns after detecting a single photon, the detector is fully recovered and able to respond to the next triggering event. In our simulation, we set four triggering events at 0ns, 10ns, 20ns, and 40ns, respectively. Figure 4.8(b) and 4.8(c) show the actual voltage drop in the device ($V_{Cathode}$-V_{Anode}) and output voltage across the sensing resistor R_s. We can clearly observe three actions upon each triggering pulse: (i) fast response upon photon arrival due to the short gain buildup time, (ii) passive quenching through R_L followed by active quenching at 3ns, and (iii) bias reset at 6.5 ns. In this design, the detector is fully recovered after 6.5ns. Moreover, the device produces no output in the absence of photon or dark pulses, as shown in the output between 28ns and 40ns in Figs. 4.8(b) and 4.8(c).

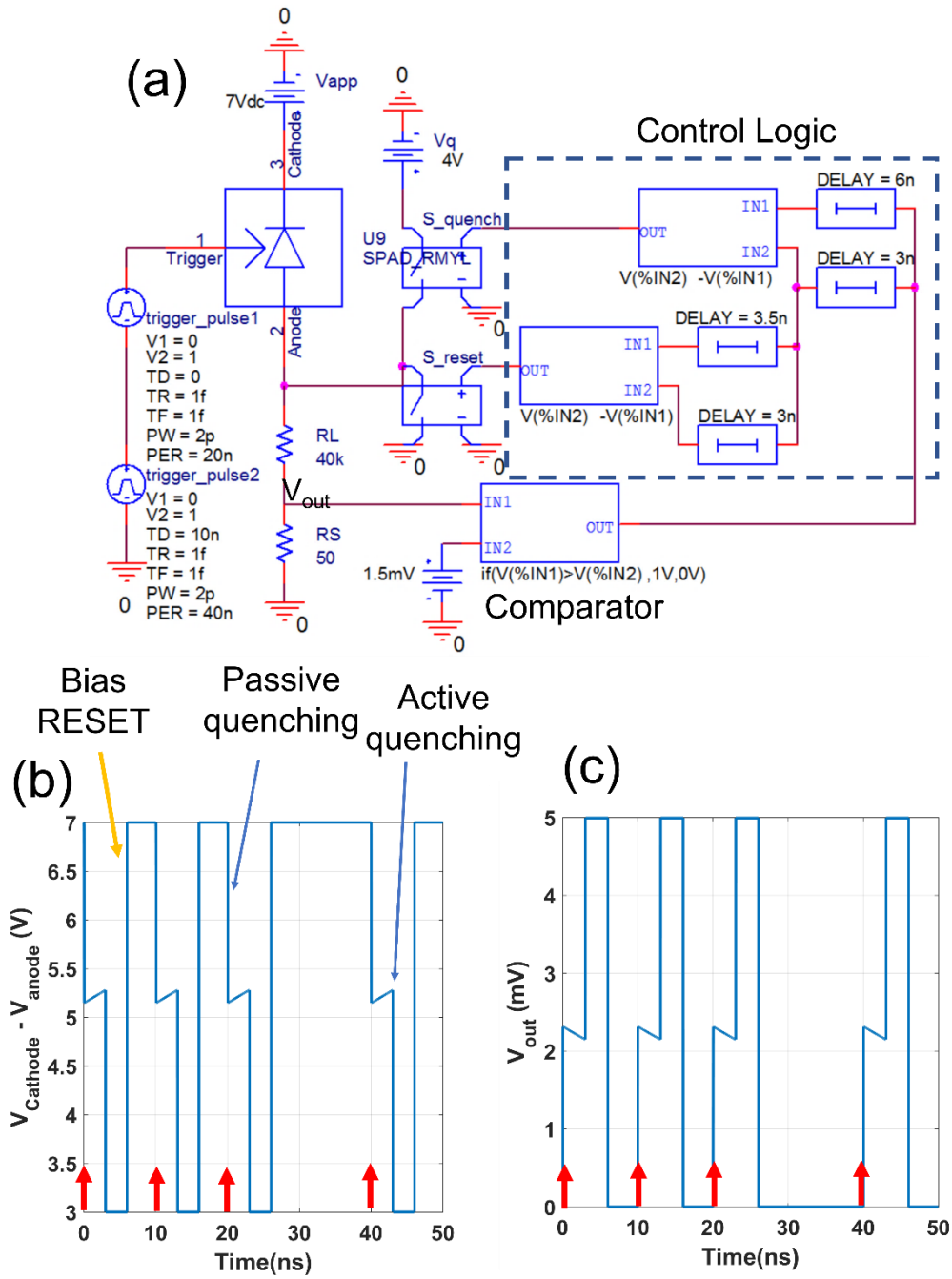

Figure 4.8: (a) Implementation of the model in PSpice for a mixed active-passive quenching circuit with a 7V applied bias on the cathode. (b) Voltage drop in the device with time and (c) Output signal, V_{out}, with time. Red arrows in (b) and (c) indicate the incoming triggering pulses. Device is actively quenched 3ns after being triggered. After 6.5ns since the detection of photon, the device is reset to have 7V drop across it and is able to detect the next triggering pulse.

The circuit model is also used for designing an integrated active-quenching circuit for a negative feedback aSi/pSi/nSi single photon detector. The basic design of the Active Quenching

Circuit (AQC) is shown in Figure 4.9. In the figure, V_anode is connected to the device anode, V_SS is connected to the ground, V_DD_18 is connected to 1.8V supply, V_R is the reset signal and V_o is the output of the active quenching circuit which can be used to control the reset signal after introducing a circuit delay.

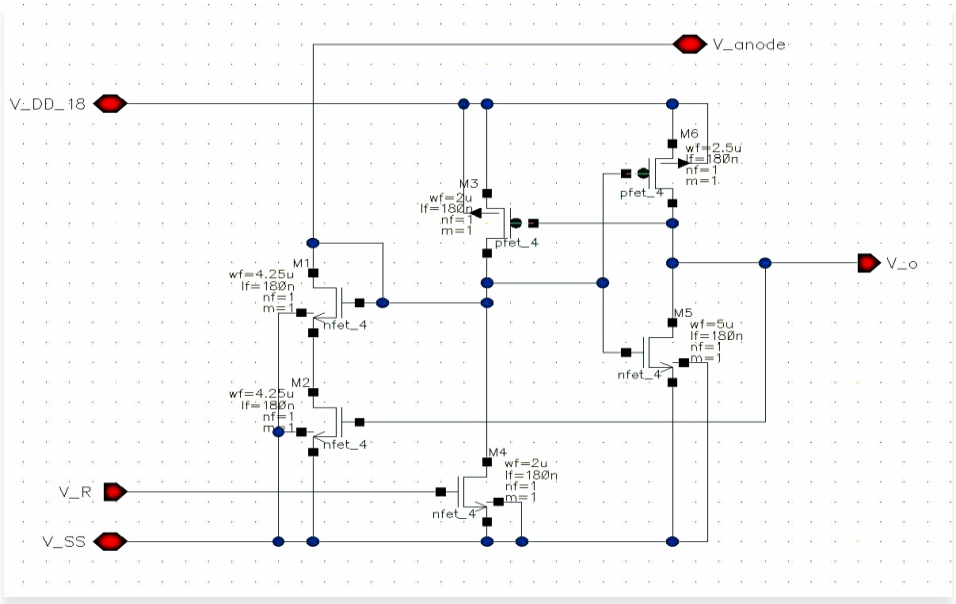

Figure 4.9: Transistor level integrated active quenching circuit of the SPAD detector

At the beginning of the photon detection cycle, V_R is set at 1.8V, which turns on M4 and M6 to effectively set V_anode = 0V. In other words, V_DUT = V_cathode – V_anode = V_cathode. Since M6 is turned ON, V_o becomes 1.8V which will turn on M2 and effectively connect the source of M1 to ground. After this setting cycle, V_R returns to 0 but the states at V_o and V_anode stays same as charges cannot be discharged.

Next, when an avalanche pulse is detected, a high current will start to flow through M1. Since M1 is in saturation region, the effective V_{GS} starts to increase and since source of the M1 is grounded, V_G of M1 starts to rise and at some point, it will turn ON M5. Then V_o will become 0V and in turn, M2 will be OFF blocking the path of the avalanche current. At this point, effective

voltage across the device will become V_DUT = V_cathode – V_anode = V_cathode – 1.8V, i.e. device is actively quenched.

After a finite delay, the reset signal V_R can be initiated again to set the V_DUT to be V_Cathode again so that device can be ready for the next pulse detection.

To simulate the designed device behavior with the AQC of figure 4.9, L=500nm and Si impact ionization coefficients were chosen for the circuit model. L=500nm gives us a breakdown votlage 18.4V from (9). Additionally, two back-to-back inverters are introduced in between the V_out and V_R of the AQC to introduce the required delay from the circuit. Additionally, an external reset signal is also applied to test out the circuit performance. Figure 4.10 (a) shows the schematic of the simulated circuit in HSpice. Figure 4.10 (b) shows the resultants Vout, VDUT and device current for a 100MHz photon pulse and a 200MHz reset signal. Device is biased at 0.7V excess bias for this simulation. It can be observed that the device quenches within 1ns and it resets in 6ns after the photo pulse is detected. The resultant characteristics are similar to what we observed with the switch blocks in Figure 4.8 (c). The simulate circuit is used for the tape-out of the chip presented in chapter 5.

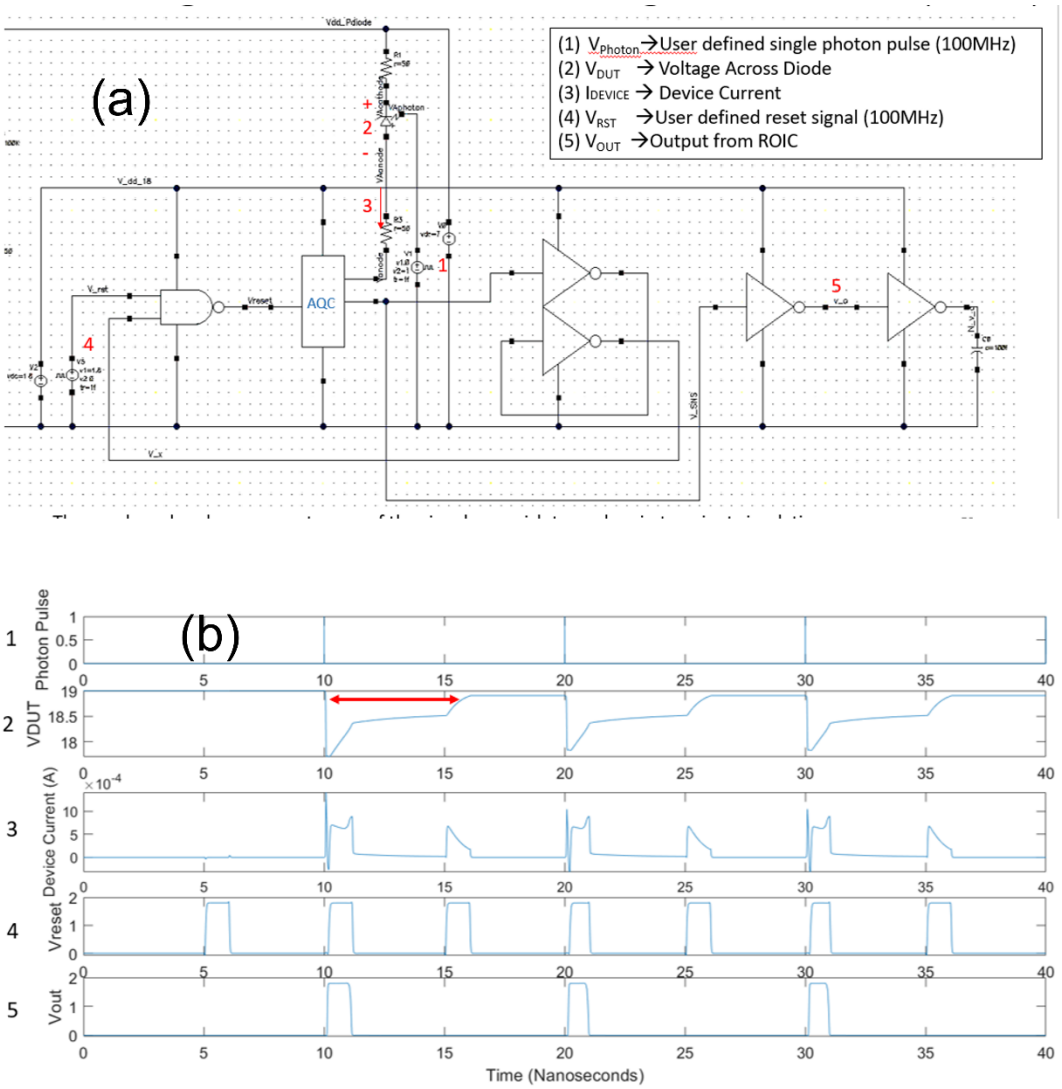

Figure 4.10: (a) Simulated active quenching circuit for a 19V biased device with L=500nm and impact ionization coefficients of Si. (b) The resultant VDUT, Vout, device current and Vreset signal from the simulation.

4.4.5. Material Dependence of Device Response

Different materials can be used for gain medium in single photon detectors to achieve the desired operational wavelength. Si is used for visible photons [36]–[38], 4H-SiC for UV photons [39], and InP, InAlAs and GaAs for telecommunication wavelengths for near infrared photons [40]–[43]. All parameters in our circuit model are obtained directly from material parameters related to the carrier multiplication process. Therefore, our circuit model can predict the

performance of detectors made of different materials by virtue of material specific impact ionization coefficients. We list the published impact ionization coefficients under high electric field for different materials in Table 4.1. Moreover, for new materials, these coefficients can be obtained from well-established experimental techniques [29], [44]–[46].

We use our circuit model to simulate the intrinsic gain bandwidth (GBW) product for detectors with Si and InAlAs gain medium. Gain is calculated from the integrated impulse response, and bandwidth is calculated from the fall time of the device when it is triggered by a single carrier. The above procedure is equivalent to taking a Fourier transform of the impulse response. APDs with Si gain medium has a breakdown voltage of 6.302V and APDs with InAlAs gain medium has a breakdown voltage of 8.782V. Figure 4.11 shows the variation in GBW product from 6V to 6.3V for Si and from 8V to 8.78V for InAlAs devices. The intrinsic GBW product of APDs using Si and InAlAs gain medium is ~433GHz and ~355GHz, respectively. These results are consistent with the reported GBW product for Si and InAlAs APDs [47]–[49].

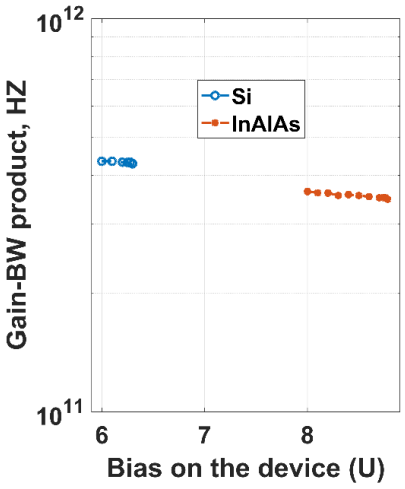

Figure 4.11: Simulated bias-dependent gain-bandwidth (GBW) product for detectors with 100nm Si and InAlAs gain medium. The intrinsic GBW of APDs is ~433GHz for Si gain medium and ~355GHz for InAlAs gain medium.

4.5. Conclusion

We have developed a universal circuit model in SPICE for photodetectors with carrier multiplication gain. Our model can simulate and predict both static and transient characteristics of the devices in analog, sub-Geiger and Geiger mode with charge sensitive amplifiers and passive/active quenching circuits. Moreover, using material dependent ionization coefficients as input parameters, designers can use our model to simulate circuit performance for detectors made of different materials. It offers a versatile and effective design and simulation tool for circuits including APDs or CEP detectors to serve the rapidly increasing applications that require high sensitivity photon detection.

This chapter, in part, is a reprint of material as it appears in the following publications: **M.A.R. Miah**, Y. Jiang, and Y.H. Lo, "A Physics Based Unified Circuit Model for Single Photon and Analog Detector", IEEE Access 9, 129571-129581 (2021).

The dissertation author was the primary author of this paper.

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CHAPTER 5: A NEGATIVE FEEDBACK SINGLE PHOTON DETECTOR IN 180NM CMOS PROCESS

In this chapter, a negative feedback single photon detector fabricated in a hybrid 180nm CMOS process is presented. The device design steps, experimental results and a tentative physical picture of the device will be discussed in this chapter.

5.1. Motivation

Single photon detectors are a valuable tool for medical imaging, diffuse optical tomograph, LiDAR, autonomous driving, optical communication, quantum key distribution and many other applications [1] . On a broad range, there are two different types of single photon detectors (SPDs); Superconducting Nanowire Single Photon Detector (SSPD) and Single photon Avalanche Detectors (SPAD). Even though SSPDs offer a wide spectral range of operation with high detection efficiency, low timing jitter and negligible dark count rate, cryo-cooling at 1K-4K is required for the device operation which limits the usage of the devices in many applications [1]. On the other hand, SPADs are semiconductor devices that are usually biased above the breakdown voltage, in geiger mode, and operated at the room temperature or moderately cooled temperature. Moreover, the scalability, low cost and robust operational conditions make the SPADs more attractive for those applications. However, for a conventional Geiger mode APD, the total number of charges is very high and also it needs external circuitry to quench the devices. These external quenching circuits will create additional parasitic capacitances and inherently create a slow response for the detectors. Therefore, a Negative Feedback Avalanche Diode (NFAD) has generally been used for fast quenching and reduction of the carrier numbers within the device [2]–[8]. A NFAD introduces a monolithic resistor or an energy barrier for the carriers to dynamically change the voltage drops in different parts of the devices to quench the APDs. Most of the previous

work was done for the Infra-red-light detection with InGaAs system. In the first ever reported NFAD devices was reported in our earlier work with a pn junction and aSi layer [9]. The devices showed promising results but with a high dark count rate which wouldn't allow it to be used for LIDAR or other applications. SPADs created from CMOS process nodes are reported have low dark count rate, high photon detection probability (PDP) and short timing jitter by means of guard rings and design modifications [10]–[15]. Additionally, a CMOS compatible process is preferable for integrating amplifiers or quenching circuits in commercial application. Considering these, a CMOS compatible negative feedback single photon avalanche detector is designed and characterized in this chapter.

5.2. Device Design

5.2.1. aSi Characterization from the Foundry

At first, we want to characterize the quality of the deposited amorphous Silicon (aSi) from the foundry process so that the designed device will behave uniformly throughout the samples.

A deposited 35nm aSi on top of n++Si wafer sample was sent from the foundry. At first solvent clean with 5-minute acetone, 5-minute methanol, 5-minute IPA and 2-min DI water is performed on the sample. A 120nm thick SiO_2 layer is deposited at 270°C by plasma-enhanced chemical vapor deposition (PECVD) on a-Si. After that 15µm diameter device mesas are photolithographically defined and dry etched with SF_6:C_4F_8 and SiO_2 etch mask layer is removed with BOE. To passivate the mesa sidewall, Al_2O_3 (40 nm) and SiO_2 (200nm) are deposited by atomic layer deposition at 200°C and by PECVD at 270°C, respectively. Finally, a 130nm ITO layer is deposited to form the top electrode, and a 220nm Ti/Au layer is further deposited to form the top and ground contact pads. The process flow of the fabrication steps and the top view of the device are shown in Figure 5.1.

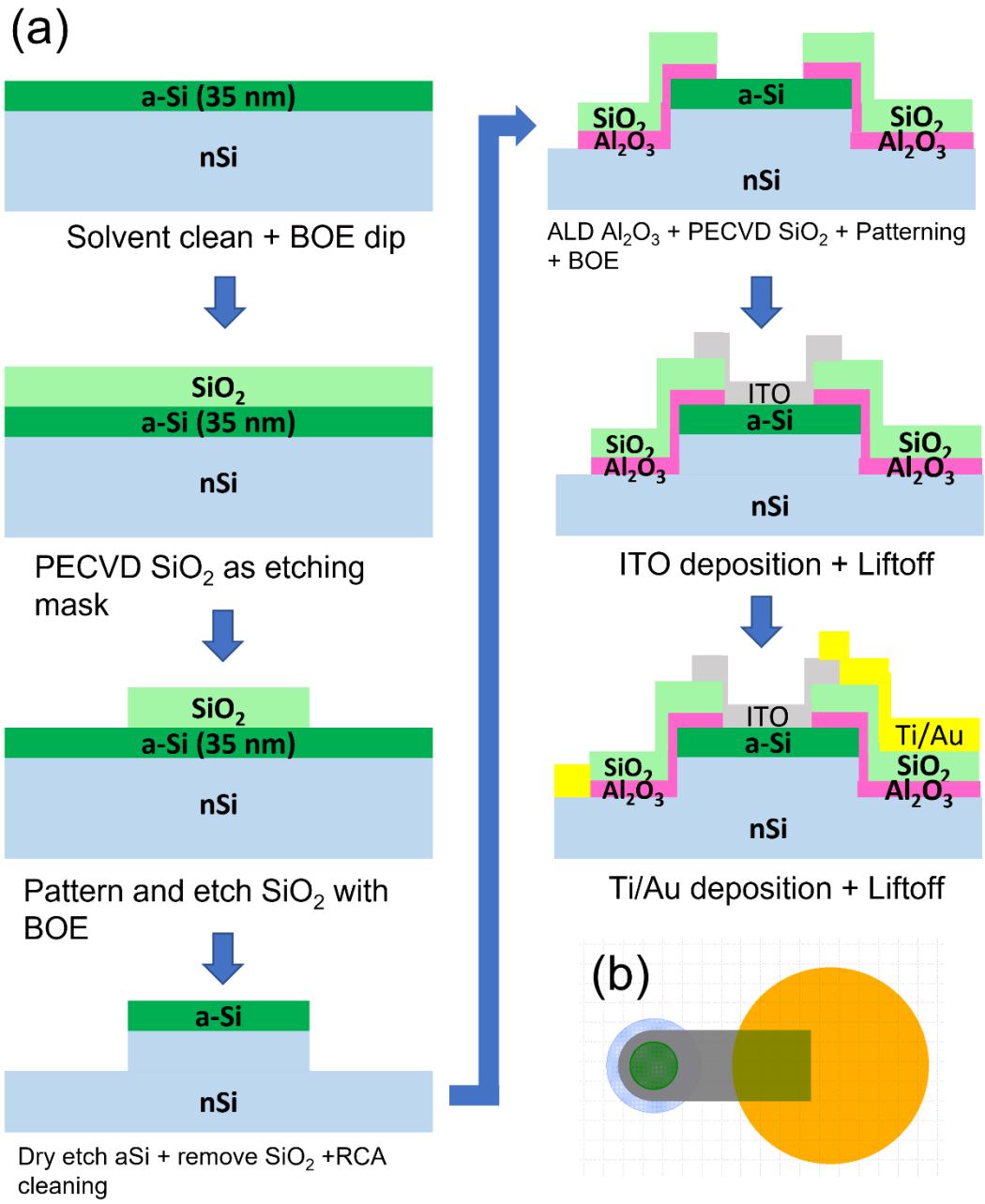
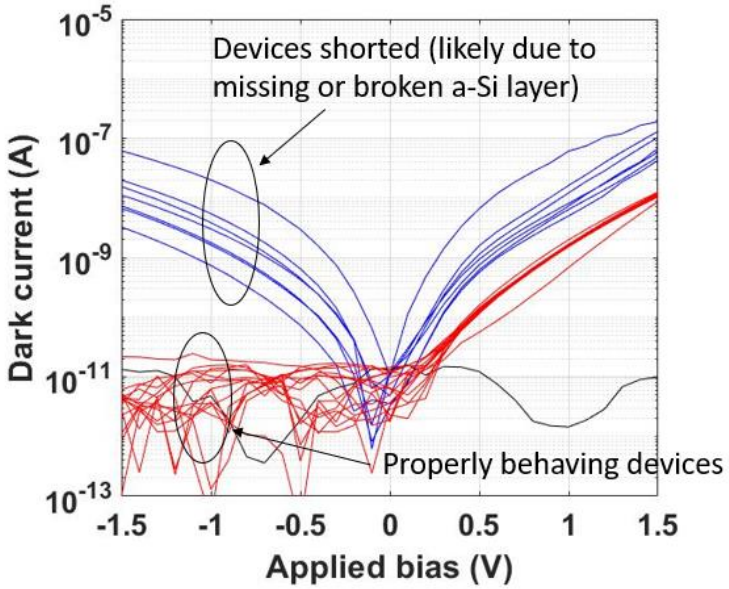


Figure 5.1: (a) Process flow of the device fabrication of aSi/nSi devices (b) Top view of the device

Diode characteristics of the device is measured using a DC source meter under the dark condition. Figure 5.2 shows that there are three types of the devices. Type 1 is the correctly behaving devices as the reverse biased dark current is ~4 order lower than forward biased dark current. However, almost 35% of the devices show a short circuit behavior which is due to the

non-uniform nature of the aSi film. We also observe a delamination of the aSi think film in some parts of the sample. Due to this delamination, ITO is directly connected to highly conductive n++Si substrate; hence the devices behave like there is a short circuit between them. In other words, due to the quality of the foundry amorphous Si, the device yield is lower.



Type 1	Type 2	Open
62%	35%	3%

Figure 5.2: Diode IV characteristics of the fabricated aSi/nSi devices.

After identifying the good behaving devices, a full DC characterization is performed on those Type 1 devices under both dark and light conditions. Figure 5.3 shows the DC dark and photo current at 639 nm wavelength light. We define the plateau photocurrent at 0.5-1V as the primary photocurrent for the gain and primary EQE determination. The initial rise of the photocurrent can be attributed to the required bias for photogenerated holes in nSi to tunnel to aSi and initiate the gain. The primary EQE of the device is around 5% and gain of the foundry amorphous Si is ~100 at 4.5V.

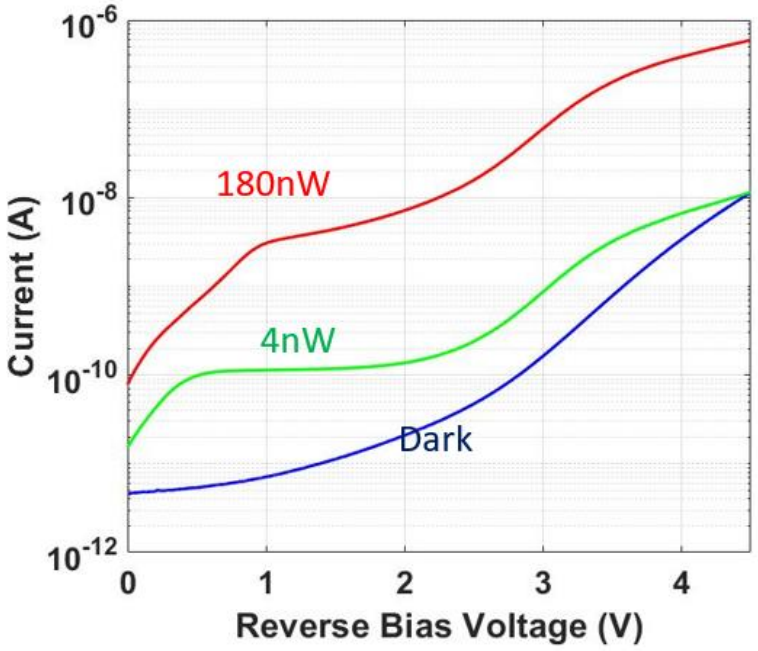


Figure 5.3: Dark and photo current of the aSi/nSi devices at 639nm incident light

The device gain is similar to what was observed before in CEP devices. However, the non-uniformity of the aSi thin film leads to the low yield of the devices. As a result, we decide to grow amorphous Silicon in the UCSD user facility instead at the foundry and design the negative feedback SPAD with a hybrid CMOS process flow where pn junction is formed in a CMOS process and amorphous Silicon is deposited in the post processing steps.

5.2.2. Layout Design for Hybrid CMOS Process Flow

Since we are using amorphous Silicon from UCSD fabrication facility, we use the device structure in Figure 5.4 for the final design. Area of the photosensitive region is around 45μm^2. The doping levels of the NWELL and PWELLs are shared by the foundry which results in ~18.5V breakdown voltage from the Silvaco TCAD simulation. As the breakdown voltage is lower than 20V, we stick with the NWELL and PWELL doping for the pn junction formation. We also introduce a guard ring, N- doping layer, to block the lateral transport between PWELL and NWELL. Moreover, guard rings also prevent premature edge breakdowns of the pn junction

devices. We design devices for two different guard ring thicknesses; 0.7µm and 3µm. The valence band discontinuity between the aSi and pSi will act as a barrier for the holes in the pSi leading to the negative feedback SPAD.

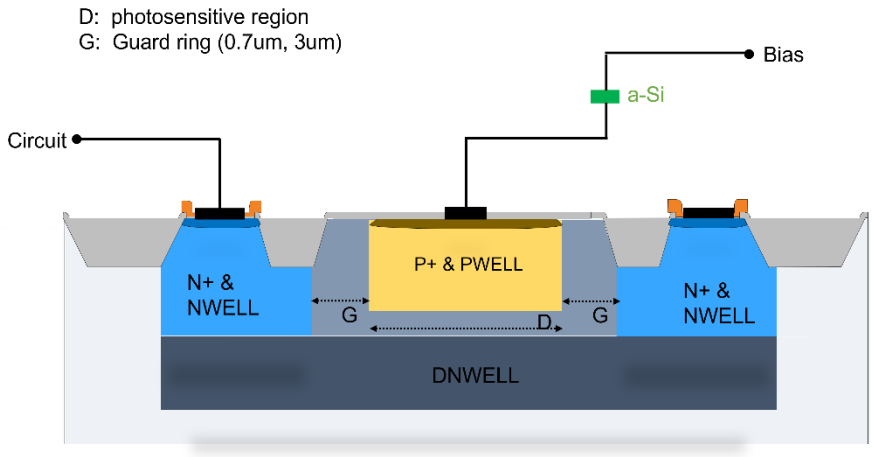


Figure 5.4: Cross-section of the device in the hybrid 180nm CMOS process flow

The full chip is designed using 19 mask sets. The actual device cross-section is created using the following 7 masks.

1. DNWELL: DNWELL is used for isolating PWELL from the p substrate wafer. In other words, DNWELL acts as an isolation layer which in turn will reduce dark currents and latch ups.
2. ACTIVE: ACTIVE mask is used to define the active area of the devices. In any places where active mask isn't defined a Shallow Trench Isolation (STI) is created using an oxide layer.
3. NWELL, NWELL2 and PWELL: In our design NWELL is the contact layer mainly as the pn junction is created in between PWELL and DNWELL. NWELL2 serves as the gurard ring and block any lateral transport and ensures all the photo generated carries in the PWELL will go through the PWELL/DNWELL junction. It is also reported that

the guard ring reduces the edge breakdown effects. For this reason, in our layout design there are three variations of the structure. We have devices without any NWELL2, a 0.7μm NWELL2 and a 3μm NWELL2.

4. NI (N++): NI mask is used on top of the NWELL layer for creating a ohmic contact between NWELL and the metals.
5. PI (P++): PI mask is used on top of the PWELL layer for creating a ohmic contact between PWELL and the metals.
6. SBLK (Block Silicide Formation): This mask is used to block silicide formation on top of the N++ and P++ layers. Since we connect aSi on the p side so we block silicide formation on the p++ layer due to the uncertainty on the transmission and conductivity. Silicide is formed as it is on top of the N++ layer
7. CONTACT: Contact mask is used to contact between the N++ and P++ layer to the M1, first metal layer. This is the gateway from the device to the interconnects.

Interconnects are used to connect the top of the device to the circuits. They are created using the following 11 mask sets

1. M1: First metal layer for routing
2. Via1: Connection from M1 to M2.
3. M2: Second metal layer for routing
4. Via2: Connection from M2 to M3.
5. M3: Third metal layer for routing
6. Via3: Connection from M3 to M4.
7. M4: Fourth metal layer for routing
8. Via4: Connection from M4 to M5.

9. M5: Fifth metal layer for routing

10. Via5: Connection from M5 to M6.

11. M6: Sixth metal layer

At the end a SILOX mask is used to create an opening on the M6 layer so that amorphous Silicon can be deposited at the user facility on top of the M6 layer later. Diameter of the SILOX opening octagon is 4.5µm which corresponds to 30.18µm^2 active aSi area.

The process flow of the 19 mask sets in the CMOS foundry is shown in Figure 5.5. Top view of the device is show in Figure 5.6. Device contact pads are designed to match 175um pitch size of the GSG probe. Before the post processing there is no connection from the Silox opening to the signal pads as shown in Figure 5.6.

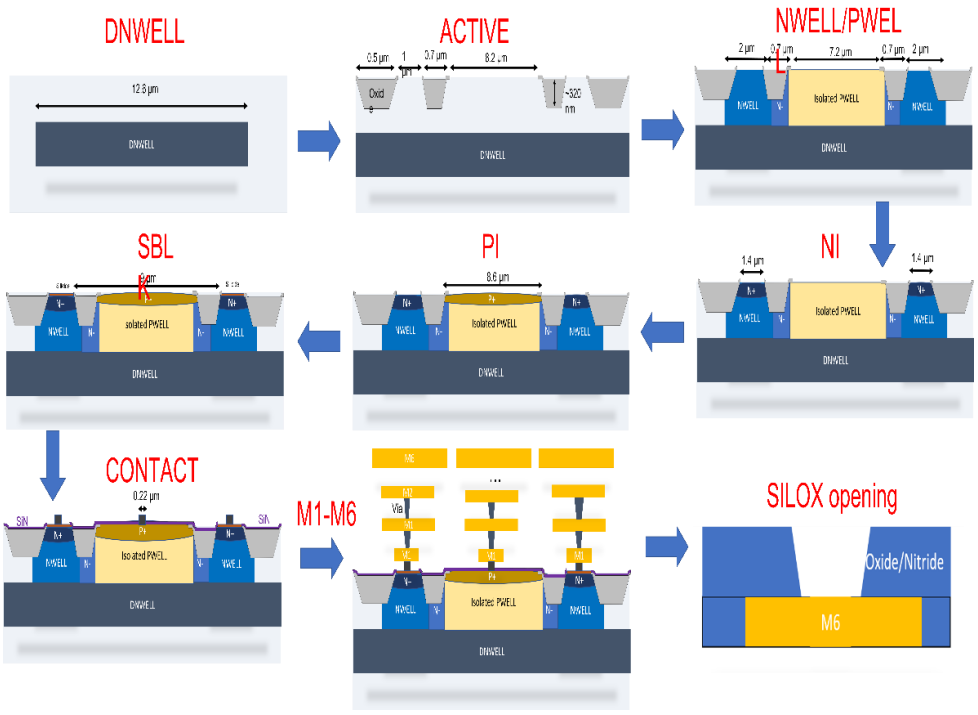


Figure 5.5: Process flow of the CMOS processes in the foundry

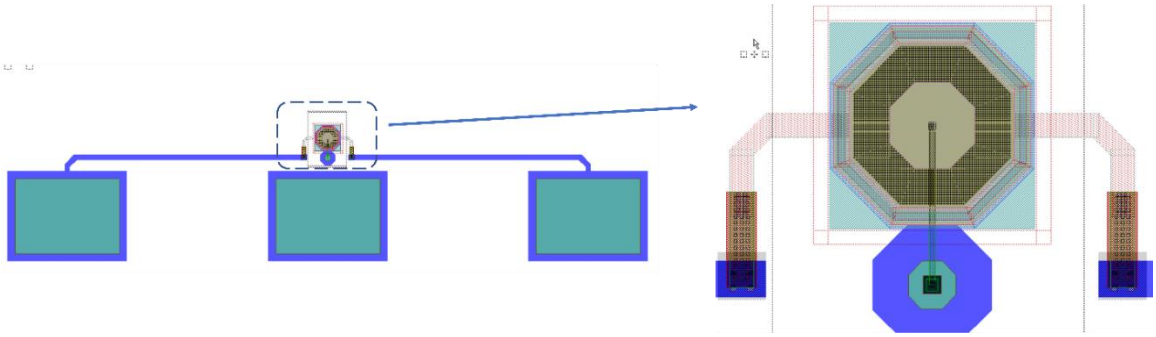


Figure 5.6: Top view of the device before the post-processing

Once we get the die back from the foundry, post-processing steps are performed on the devices. For the post-processing steps, at first, we clean the surface of the M6 layer and remove any residual Al_2O_3 with a 10sec Buffered Oxide Etching (BOE). After that, a 103nm thick carbon doped a-Si layer is deposited at 270°C by plasma-enhanced chemical vapor deposition (PECVD). The thickness of the aSi is calculated using both surface profilometer and ellipsometer measurement. The bandgap of the deposited aSi thin film is 2.25eV and the Urbach tail of the that is 106meV as shown in Figure 5.7. Bandgap of the amorphous Si is a little high compared to the reported ones due to the introduction of the carbon doping.

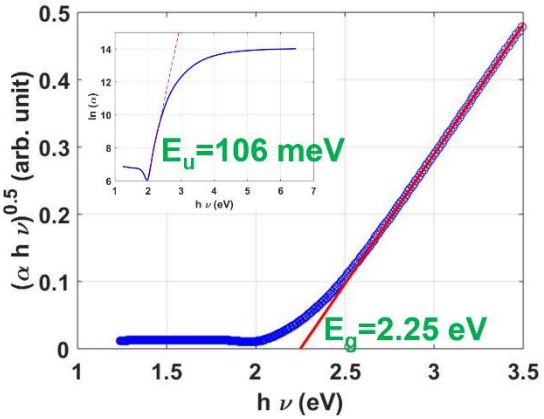


Figure 5.7: Bandgap and Urbach tail energy of the deposited a-Si

After the aSi deposition, aSi are photolithographically defined and dry etched with SF_6:C_4F_8. Next, SiO_2 is deposited with RF sputtering and patterned lithographically to create a

insulation at the sidewall of the aSi. Finally, a 120nm ITO layer is deposited to connect aSi with the signal contact pads. Figure 5.8 shows the process flow and the top view of the device after the post processing.

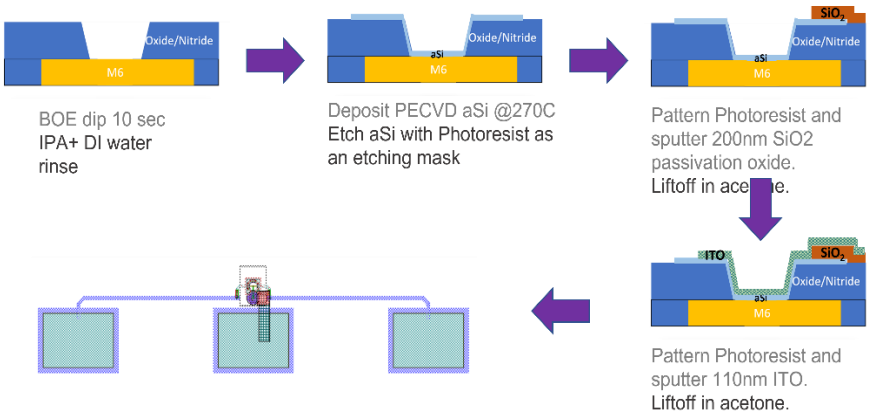


Figure 5.8: Process flow of the post processing and top view of the device after the post processing

5.3. Device Characterization

We use the 3um guard ring devices for the detailed characterization of the device.

5.3.1. DC Characterization

Figure 5.9 (a) shows the dark and photo current of the device under the DC bias @518nm wavelength light. The first breakdown of the device is at around 18.5V. Device current increases slowly from 20V compared to the current increase after the 1st breakdown. In other words, there is a mechanism which limits the device current or quenches the device. A pn junction only device will shoot to an infinite current after the breakdown and it won't allow us to measure the dark current or photo current without any external resistor above the breakdown. The primary photocurrent at 9.8pW 518nm green light corresponds to 40% of primary QE which is also a decent number among the conventional pn junction devices. Figure 5.9(b) illustrates the power dependent on the DC gain of the device. We observe a high gain of around 4×10^5 at 26V operating power

and lowest optical power. Gain role off at high optical power indicates a gain saturation behavior for the device. A high optical power means photons are impinging on the device at a faster rate not allowing the device to fully recover to exert the same gain as the low optical power.

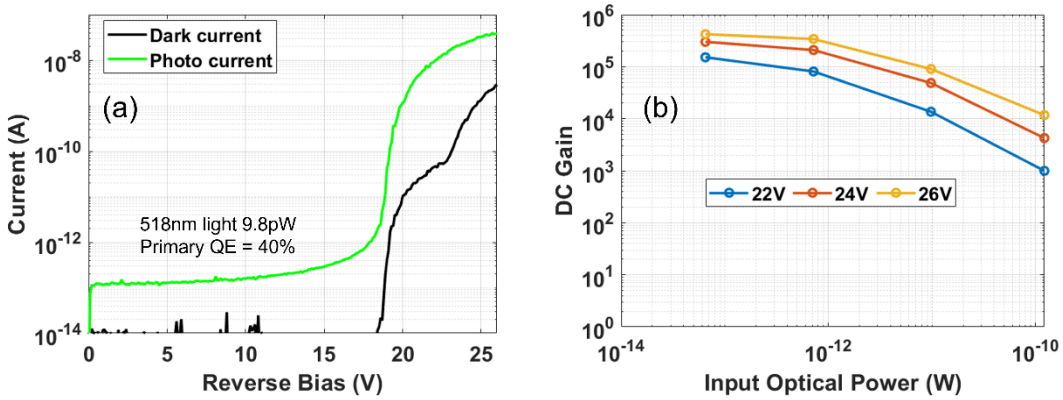


Figure 5.9: (a) Bias dependent DC dark and photo current at 518nm light (b) DC gain dependence of the device at different optical power and different applied bias

5.3.2. Photon Counting

For photon counting, we introduce a 518nm CW DC light to the device. When the power of the CW light is increased, effective arrival rate of the incoming photon is increased. From the observed DC primary photocurrent at a specific optical power, we calculate the photon arrival rate to the device. For a note, this photon rate actually represents the photo-electron rate as we estimate the arrival rate from the DC primary current. Now, if DC photocurrent is $I_{ph,DC}$, then the photon arrival rate can be calculated as,

$$Photon\ Arrival\ Rate\ (I_{ph}) = \frac{I_{ph,DC}}{1.6 \times 10^{-19}} \qquad (5.1)$$

Figure 5.10 shows the measurement setup of the photon counting experiment. A variable Neutral Density (ND) filter is used to attenuate the light power to vary the photon arrival rate. We use a bias Tee to isolate the DC and AC part of the device current. AC part of the current is then converted to a voltage using the 50Ω oscilloscope resistance.

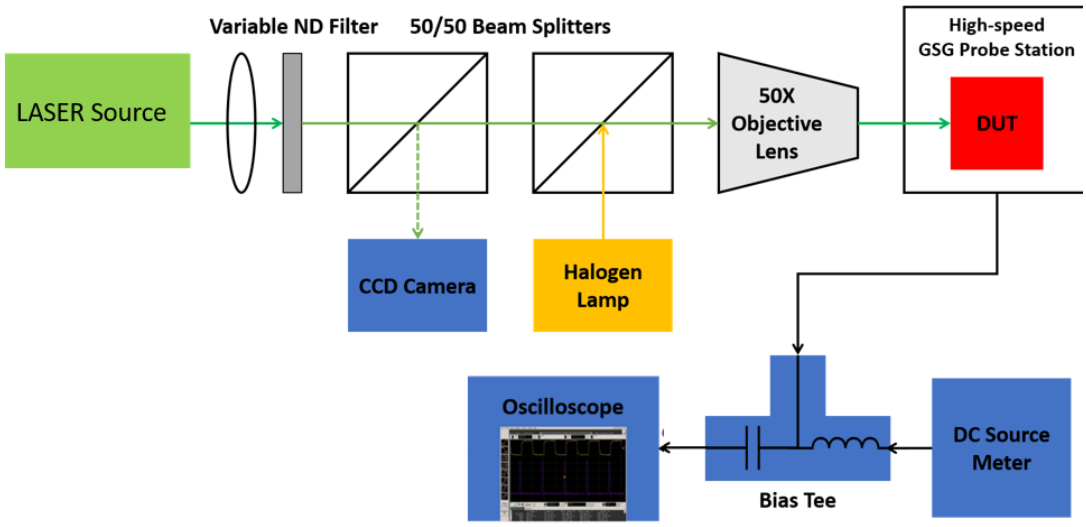


Figure 5.10: Measurement setup of the photon counting

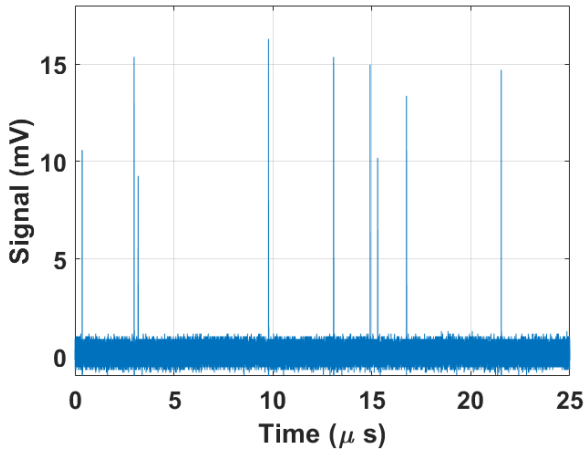


Figure 5.11: Sample raw data from the oscilloscope collected at 26V bias with 220fA of primary photocurrent

Figure 5.11 shows the sample raw data saved from the oscilloscope at 26V with 220fA of primary photocurrent. Data were saved using 20GHz sampling frequency, i.e. each data point is saved with 50ps sampling time. A total of 1ms of data is save for each bias and each optical power. A suitable threshold, above the noise floor, is chosen to count the number of detected pulses within that 1ms. Detection rate for a particular primary photocurrent can be found as,

$$Detection\ rate\ (I_{ph}) = \frac{Number\ of\ detected\ pulses}{Total\ time} \qquad (5.2)$$

Figure 5.12 (a) shows the bias dependent detection rate at different primary photo current levels and at the dark. Dark Count Rate (DCR) at 26V is found to be 20kHz (444Hz/μm^2). DCR is comparable to other CMOS SPADs [14], [16].

Photon Detection Efficiency (PDE) at any primary photo current level can be calculated from the detection rate and photon arrival rate as,

$$PDE = \frac{Detection\ rate\ (I_{ph}) - Detection\ rate\ (dark)}{Photon\ Arrival\ Rate\ (I_{ph})} \qquad (5.3)$$

Figure 5.12 (b) shows the PDE of the detector under different photon arrival rate and different operating voltages. Photon detection efficiency is around 25% irrespective of the photon arrival rate.

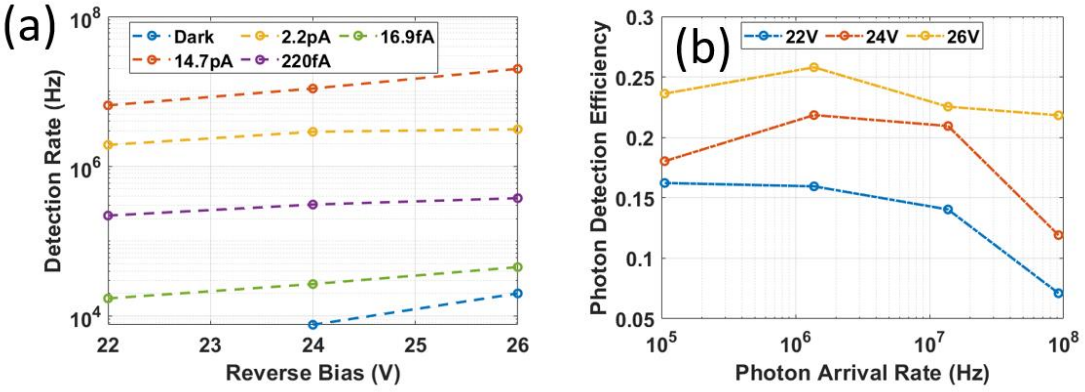


Figure 5.12: (a) Photon detection rate at different primary photocurrent (input optical power) (b) Photon Detection Efficiency (PDE) different photon arrival rate and bias voltage

At higher rate, photons are arriving at a faster rate which won't allow the device to recover and as a result, the peak height of the pulses may fall below the noise floor. Therefore, detection efficiency isn't totally accurate at the low bias voltages for 100MHz photon arrival rate. We also determine the mean peak height of the pulses at different photon arrival rate and different bias to show the dependence of the device recovery rate to the mean peak height of the device.

Figure 5.13 (a) shows the typical pulse shape @26V for the lowest photon arrival rate. The FWHM of the pulse is around 200ps. Fig. 5.13(a) also illustrates the definition of the peak height in the diagram. Figure 5.13 (b) shows the variation in the mean peak height for different optical power and device bias. As expected, when the bias voltage is higher, gain is high; hence the pulse height is higher. However, with an increase in the photon arrival rate the device gets shorter time to recover. When the device can't recover, i.e. pn junction bias isn't reached to the steady state, the pulse height is lower as the device gain is lower. Also, at around 100MHz photon arrival rate, the pulse height is almost close to the noise floor of the system. Therefore, we can't detect all the possible counts at this high arrival rate which accounts for the low detection efficiency at 22V and 24V at 100MHz arrival rate as shown in Figure 5.12 (b). Mean peak height is calculated from the average of the heights of all detected pulses. The error bar in the plot represents the standard error around the mean peak height.

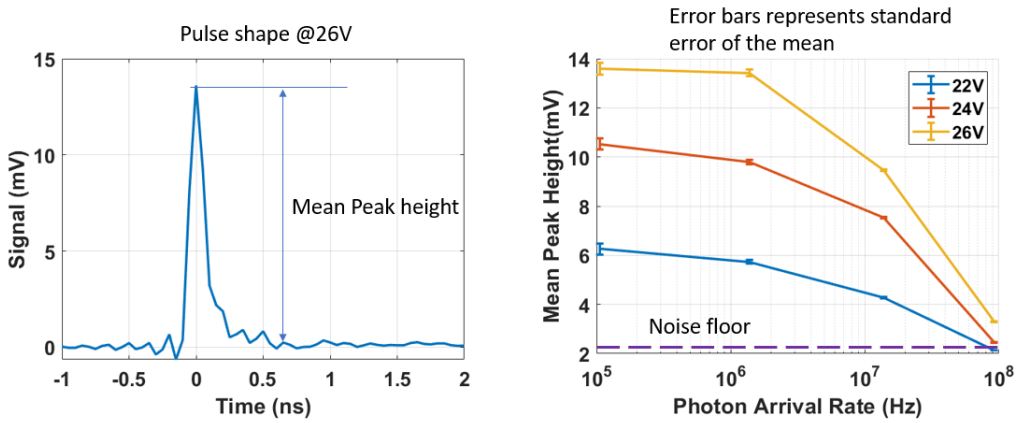


Figure 5.13: (a) Typical pulse shape @26V (b) Mean peak height of the device at different photon arrival rate and at different bias

Now, the area underneath the pulse shape represents the total number of carriers generated from a primary carrier, i.e. the device gain. Performing the integration of the pulses within this 200ps-300ps time and then plotting it with the photon arrival rate we can the gain vs. frequency

plot in the Figure 5.14. Gain at the 100kHz photon arrival rate is 2.4×10^5, 1.85×10^5, and 1.1×10^5 at 26V, 24V and 22V respectively. Gain drops to half of its value at around 37MHz for 26V, 41MHz for 24V and 90MHz for 22V. Therefore, gain-bandwidth product can be estimated as 8.88THz, 7.58THz and 9.9THz respectively. Also from the mean and standard deviation of the peak heights we find that excess noise factor (1 + (deviation/mean)^2) is in between 1.03 and 1.06.

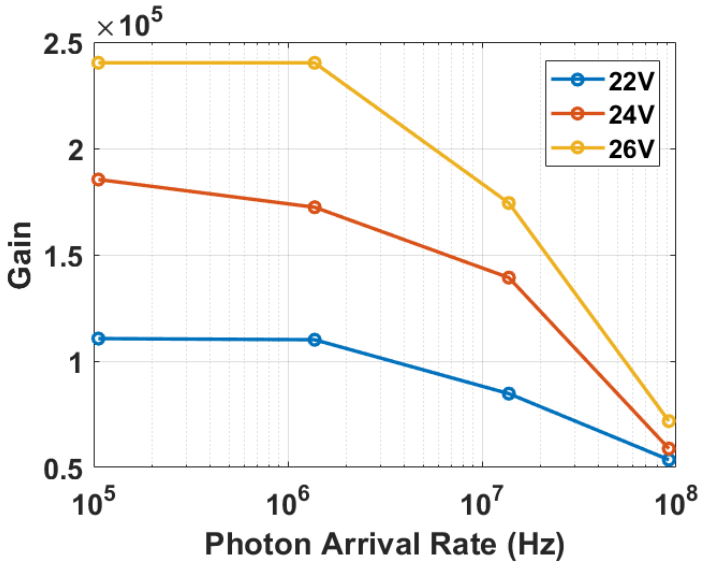


Figure 5.14: Gain of the device with the photon arrival rate. GBW is ~8.8THz at 26V and ~7.5THz at 24V

5.4. Tentative Physical Picture

As a negative feedback avalanche detector device, there is a dynamic voltage division between the aSi and pn junction. In this section, we will qualitatively discuss our thoughts on the device physics associated with the observed quick recovery time of the device. For example, let's assume at 25V, pn junction voltage is at 16V (close to the breakdown voltage) and other 9V drops across the aSi. Figure 5.15 (a) illustrates the condition when a photon is absorbed in the pn junction generating one electron-hole pair. Figure 5.15(d) shows the relative time in the pulse for the physical picture in 5.15(a).

Now, electrons will experience the avalanche gain and more and more holes will be coming to the p side of the pn junction. Electrons in the n side are free to flow to the electrode whereas holes on the p side will be stuck at the aSi barrier unless it gets a sufficient field to overcome the 100nm aSi. Figure 5.15(b) shows the accumulated holes and corresponding electrons after the avalanche gain in pn junction. Since current is continuous throughout the device, there needs to be a displacement current in aSi. A 100nm aSi will create a 0.8V voltage drop for a 12.5mV pulse height (250uA peak current) within 100ps of the gain build up time. In other words, at extreme cases, pn junction voltage will drop to 15.2V and aSi voltage will be 9.8V. Here, ~12.5V is the average pulse height at 26V as shown in figure 5.13. Gain-build up time is the period when the pulse is rising. Figure 5.15(e) shows the relative time in the pulse for the physical picture in 5.15(b).

After this point, holes will start to leave the aSi/pSi surface as the electric field inside aSi is sufficient enough to initiate carrier tunneling. Since the voltage in the pn junction is already below the breakdown, there is no more incoming holes to the interface. Now particle current is flowing through the aSi and a displacement current through the depletion capacitance of the pn junction. Figur 5.15 (c) and (f) illustrate this physical picture. From our previous experience, we know that at 9V aSi can only sustain around 1nA of current. If that's the case, then it will take 8us for the accumulated carriers to leave the interface. In other words, the device can't respond to any frequency higher that 125KHz. However, from our gain-bandwidth data, we know that the device can recover at ~30ns. Or for the extreme case we know for sure that within 100ns device is fully recovered as the height of the pulse are almost flat upto that point as shown in figure 5.14. In that case, we can qualitatively say that aSi has a gain of 80 and this gain in aSi only peaks up when pn junction in not in the breakdown region or there is no carriers in the pn junction gain to experience

the avalanche gain. This high gain in amorphous silicon allows the device to recover at a faster rate than the conventional NFAD detectors.

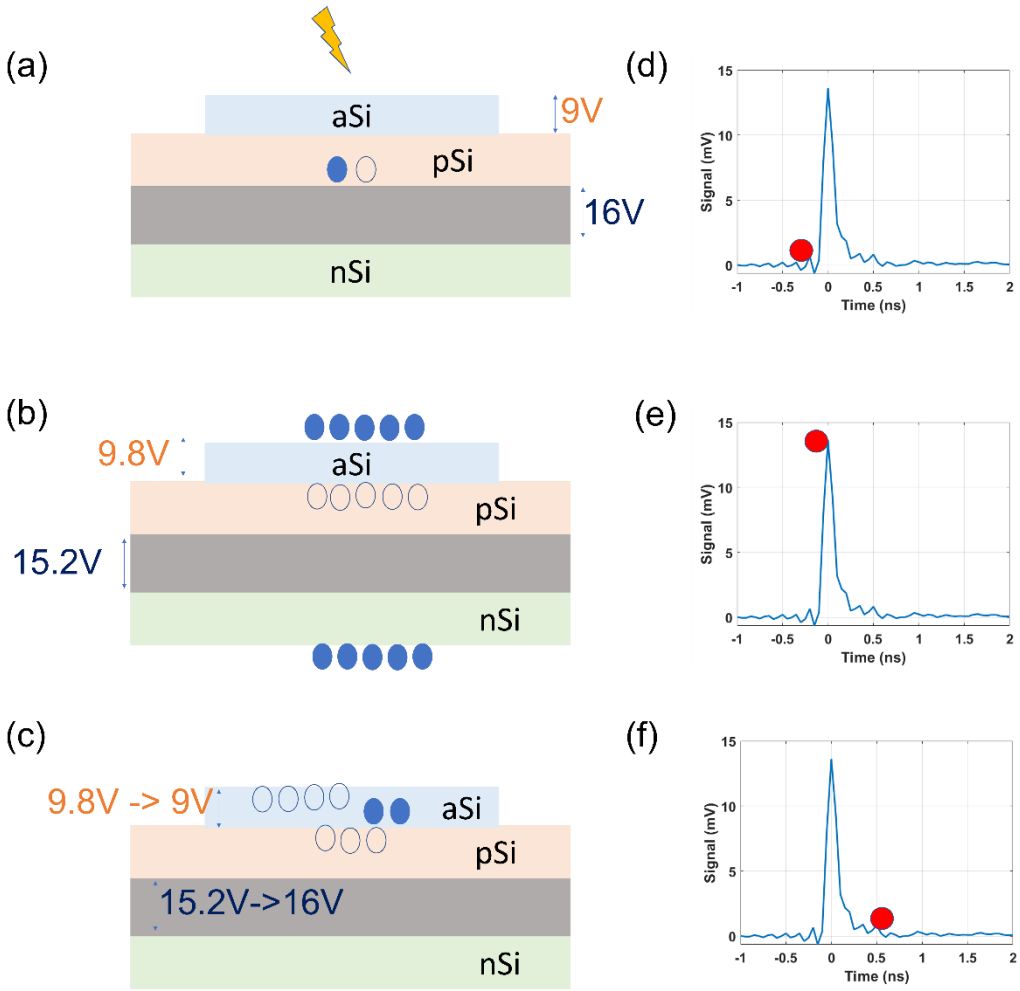


Figure 5.15: (a) An absorbed photon creates a electron-hole pair near the depletion region of the pn junction. (b) Photogenerated electrons experience avalanche gain while crossing the depletion regions. The generated electrons will reach the electrodes whereas the generated holes will be accumulated at the aSi/pSi interface creating a displacement current. (c) After a sufficient voltage drop in aSi, the accumulated holes can tunnel into the aSi gain medium and can create additional electrons allowing the device to recover faster. (d, e, f) The red circle shows the relative time within the pulse corresponds to the physical picture of (a), (b) and (c) respectively.

5.5. Conclusion

We demonstrate the CMOS implementation of a NFAD detector combining pn avalanche junction and amorphous Silicon. DCR of the device is 20kHz (444Hz/μm^2) and it quenches within

200ps due to the barrier discontinuity between pSi and aSi. Photon detection efficiency of the device is found to be 25% with a recovery time of around 30ns. The gain dynamics between pn junction and amorphous Si allows the device to operate at a faster rate which yields to ~7.5-8.8THz gain bandwidth product and 1.06 of excess noise factor.

This chapter, in part, is a reprint of material as it will appear in the following publications: **M.A.R. Miah,** B. Schuster, J. Zhou, H. Peng, Y. Jiang, A. Davis, and Y.H. Lo, "Negative Feedback Single Photon Detector in 180nm CMOS Technology", to be submitted.

The dissertation author was the primary author of this work.

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CHAPTER 6: CONCLUSION

6.1. Thesis Summary

This thesis presented a theoretical foundation of the Cycling Excitation Process (CEP) using 2nd order perturbation theory for amorphous Silicon and demonstrate the utilization of the gain in amorphous Si for two highly sensitive optical detection application.

Multiplication rate of the electron and hole-initiated CEP process is calculated using both the bloch wavefunction from the bulk Si and localized wavefunction of the defect states in the expression of the Fermi's Golden Rule. The theoretical method is applicable to any other amorphous material. This microscopic material property can be transformed into measurable electrical quantities by means of calculating multiplication coefficient using Monte Carlo simulation or distribution function. Any TCAD device simulator can use these multiplication coefficients to predict the device performance. This is the first time a defect assisted multiplication rate in amorphous material is computed from the quantum mechanical calculation.

The first application of the CEP gain in amorphous Si was demonstrated in the novel design for room temperature LWIR detector coupling it with the a-Ge for LWIR light absorption. At 20kHz optical modulation, a 30μm diameter device has shown a record highest room temperature LWIR detectivity value of 6×10^8 Jones and a decent NEP value of 5pW/√Hz, the lowest value for all uncooled LWIR detectors. The fast response, room temperature operation, high detectivity, low NEP, and simple and low-cost fabrication process make the device attractive to night vision, machine vision, autonomous driving and many other applications.

A universal circuit model in SPICE was presented for solid state photodetectors with carrier multiplication gain. The model can simulate and predict both static and transient characteristics of the devices in analog, sub-Geiger and Geiger mode with any external circuits making it an ideal

candidate for designing the integrated quenching circuits and amplifier for the SPADs. Additionally, using material dependent ionization coefficients as input parameters, the model can handle detectors made of different materials. It offers a versatile and effective design and simulation tool for circuits including APDs or CEP detectors to serve the rapidly increasing applications that require high sensitivity photon detection.

For the second application, CEP gain medium, amorphous Silicon, was used to demonstrate a negative feedback single photon avalanche diode with high ~8THz gain bandwidth product, 1.06 of excess noise factor, ~30ns recovery time, 20kHz (444 Hz/μm^2) dark count rate and 25% single photon detection efficiency. CEP gain in amorphous Silicon allows the device to recover faster and make it suitable for any high-speed photon-counting applications like LiDAR, autonomous vehicle and satellite communications.

6.2. Outlook

One of the major contributions of this thesis is the CMOS implementation of the negative feedback single photon detector implementation using both Si pn junction and amorphous silicon. Similarly, the thesis also presented a LWIR detector using amorphous Germanium and amorphous Silicon. Since aGe absorption can be coupled with the aSi as demonstrated in this thesis, a broadband single photon detector can be implemented in CMOS by coupling aSi and aGe in the post-processing phase of the CMOS implementation. Moreover, the commercial application requires an array structure to realize large fill factor and so on. The devices presented in this thesis can be extended to an array structure for LiDAR, autonomous driving, night vision, biological imaging and quantum information processing applications. Additionally high DC gain of the

CMOS NFAD devices at low optical power can allow us to realize a high speed single photo imager for photon starved imaging applications.