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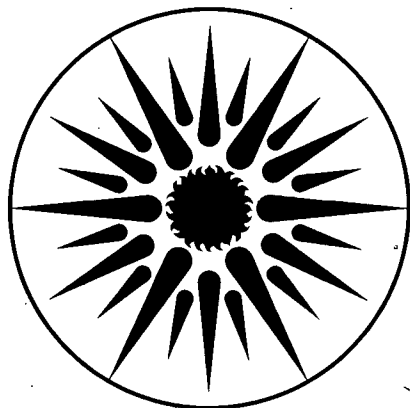
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Abstract

A simple and economical phase-sensitive detector circuit is described. The circuit, which was developed for use with large-area heat-flow sensors that employ resistance temperature detection, uses a synchronous rectifier driven by a square wave. It is shown that the circuit has linearity, resolution, and noise immunity.

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Introduction

Numerous laboratory measurement situations require sensing small resistance changes in a balanced wheatstone bridge. Strain gauges, RTDs, and pressure transducers are frequently used in a bridge configuration. The bridge is most commonly excited with a dc voltage that allows one to readily measure bridge output changes on a voltmeter or through a dc amplifier. When the signal levels are small, such measurements are subject to significant thermoelectric potentials from connections, and the output voltage drifts with the temperature of the amplifiers used. Such test situations are also vulnerable to interference from noisy environments.

While these problems may be reduced by increasing the drive voltage, this is frequently limited by the adverse effect of self-heating of bridge resistance elements, which changes their resistance.

Exciting the bridge with ac voltage and synchronous detection eliminates or reduces these problems, but typically requires expensive, complex apparatus to develop the drive signal with a synchronized amplification detection system. Such systems typically require a medium-impedance bridge load of hundreds of ohms for operation. Commercial lock-in amplifier systems frequently have phase-angle detection capabilities and other features not necessary for many resistance bridge measurement configurations.

We report here an economical phase-sensitive detector circuit that was developed for use with large-area heat-flow sensors that rely on resistance-wire temperature detection.¹ Instead of a true phase-sensitive detector, a square-wave driving signal is used with a synchronous rectifier. This allows use of inexpensive CMOS integrated circuits at the cost of a very slight increase in noise susceptibility. If a bridge is driven with only 270 mV peak-to-peak, a change in bridge balance of 1 part in 10^5 can be detected reliably. The bridge may have an

impedance as low as 30 Ω .

Circuit Description

The outline of the circuit is shown in Fig. 1(a), with details of the driving and the detection circuits in Figs. 1(b) and 1(c), respectively. Component costs for the circuit are about \$75.00.

The bridge is driven by a complementary square wave at 400 Hz, with an amplitude of ± 135 mV. This waveform is generated by I.C. 1, a dual, monostable CMOS multivibrator (C04528B)². R_T is adjusted for a symmetrical waveform over time (i.e., 50% duty cycle). Q_1 and Q_2 buffer the oscillator's output and I.C. 5 (LM313)³ is a two-terminal band-gap reference device that stabilizes the amplitude of the drive. R_u , R_v , and R_w define the amplitude of the output voltage to the wheatstone bridge, while I.C. 2 (OP-05)³ and I.C. 3 (OP-05) are the output buffers to supply sufficient current to a low-impedance bridge.

The complementary square-wave bridge drive is actively balanced to minimize common-mode output voltage from the bridge by I.C. 4 (OP-05). This open loop op amp maintains the reference side of the bridge at virtual ground by shifting the amplitude (with respect to ground) of the drive voltage seen by the R_u , R_v , R_w voltage divider network. The amplitude across this network is maintained at 1.2 V by I.C. 5. R_v is adjusted to minimize I.C. 4 output when the reference resistances in the bridge are equal.

The output of the bridge is amplified by an ac-coupled monolithic instrument amp, I.C. 6 (AD521).⁴ Diode input protection prevents high-voltage noise from overloading the amplifier input (and thereby overcoming its high common-mode rejection). The amplifier gain is set at 1000x and the output ac-coupled to a CMOS dual, 4-channel analog multiplexer, I.C. 7 (CD4052B). It is used as a DPDT switch synchronized to the drive oscillator (i.e., it is a synchronous rectifier). Input to the rectifier is voltage-limited to prevent overload of the CMOS gates. R_2 is adjusted so that any dc voltage applied to the rectifier input causes no output voltage (i.e., the rectifier is balanced). Two stages of

integration are shown at the rectifier's output, but a single stage is frequently sufficient if there is not too much pulse noise in the environment.

It was found that transitions in the square-wave drive caused transients in the amplifier's output. These are prevented from getting through the rectifier by the CMOS gate inhibit function, controlled by I.C. 8 (CD4528B). I.C. 8 defeats the inhibit function shortly after the square-wave transition, and activates it shortly before the transition repeats. R_y controls the period of the inhibit function.

Phase-Sensitive Detector Performance and Calibration

The ideal output voltage of the detector when the reference resistors are equal is given by:

$$V_{out} = V_c \frac{R_A - R_B}{R_A + R_B}$$

where V_c is the detector's characteristic voltage, defined as:

$$V_c = K G V_D.$$

Here V_D is the bridge-drive voltage, G is the gain of the amplifier, and K is an efficiency factor (< 1) primarily related to the rectification process.

A calibration wheatstone bridge was wired using two 38.3-ohm precision resistors to simulate a sensor source and two 3.20 \times -ohm precision resistors with a 20-ohm trimmer as the reference elements. The bridge was balanced for zero output voltage. Precision resistors were placed in parallel with each of the 38.3-ohm resistors in turn to simulate small resistance changes in a sensor source. The detector output voltage was recorded for bridge imbalances until the output became non-linear (due to clipping), which occurred at an output of 3.5 V.

Figure 2 shows the detector calibration for a sensor source impedance of 76.6 ohms. The detector is linear for a signal imbalance $(\frac{R_A - R_B}{R_A + R_B})$ up to 5×10^{-2} . The characteristic voltage is 41.6 V.

This calibration was repeated for sensor sources having impedances from 30 ohms to 674 ohms. For this range of impedances, the characteristic voltage varied $\pm 1.02\%$, increasing with impedance.

To determine the detector's temperature drift, its ambient temperature was varied from 18° to 25°C , while that of the calibration bridge was maintained at a constant temperature. The voltage output drift was less than $0.1 \text{ mV}/\text{C}^\circ$. A sine wave signal, in phase with the detector's drive/rectification frequency of 400 Hz, was applied to the detector input. The detector response to integral harmonics of the fundamental, up to the tenth, was determined.

Table 1 shows the response of the detector. There is somewhat greater response to the odd multiples, which is expected since the fundamental is a modified square wave. The maximum response was to the third multiple of the fundamental frequency: the gain was 9.3% of that for the fundamental. For the highest harmonics the response was less than 2% of that for the first harmonic. The detector showed no response to signals significantly different from these integral harmonics.

Discussion

The circuit we have described combines economy and relative simplicity with high sensitivity, good noise immunity, and long-term stability. The measured temperature coefficient of the circuit implies that thermal fluctuations in the circuit's environment (assumed stable to about 4°C) will produce voltage fluctuations of about 0.4 mV at the circuit output. We take this (which corresponds to a $1.3\text{-}\mu\text{V}$ signal at the input) to be the factor limiting reliable signal detection over the long term. Using the characteristic voltage of 41.6 V (derived from the slope of the line in Fig. 2), this implies a resolvable value of 10^{-5} for $(R_A - R_B)/(R_A + R_B)$. For the application described in Ref. 1, this

corresponds to a temperature difference of $5 \times 10^{-3} \text{ }^\circ\text{C}$.

While use of the square-wave drive and synchronous rectifier rather than a sinusoidal drive and mixer in principle degrades the noise immunity of the circuit by admitting higher harmonics, in practice this is unimportant. If we compare the minimum detectable signal in the presence of a white-noise spectrum with that of an ideal phase-sensitive detector,⁵ we find that the admitted noise is increased by the factor $\frac{\sqrt{\sum G_i^2}}{G_1}$, where G_i is the effective gain for the i^{th} multiple of the fundamental frequency, and the summation is for $i \geq 1$. From the measurements of G_i in Table 1, we find that the minimum detectable signal is increased by only 1.5%. (Negative gain in the table means that the circuit inverts the polarity of the sensor signal at that frequency).

Because the circuit is immune to dc thermoelectric potentials, it is possible to use switches and connectors in the input circuit without degrading accuracy. We have successfully employed a multiplexing scheme where several resistance bridges are alternately switched into the same detector. The switching rate is, of course, quite slow because of the detector's long settling time.

Acknowledgement

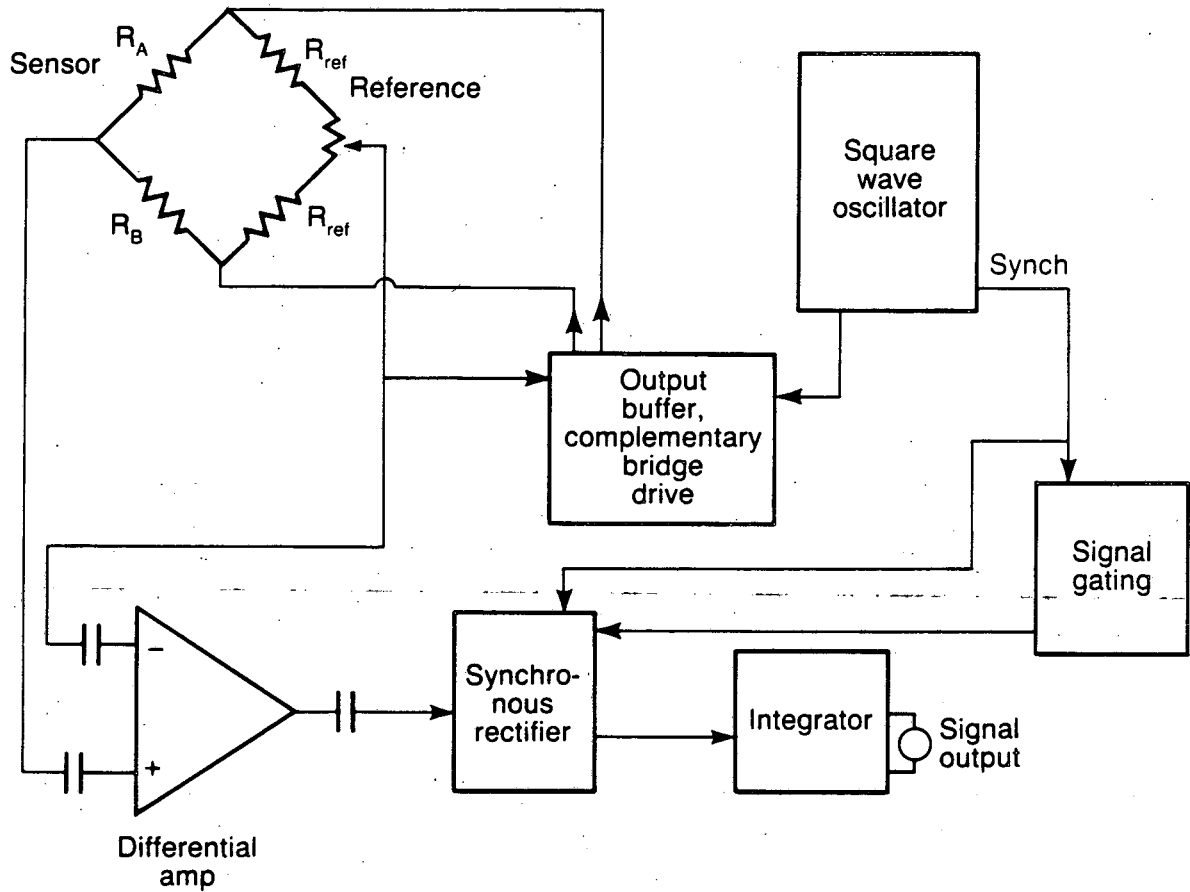
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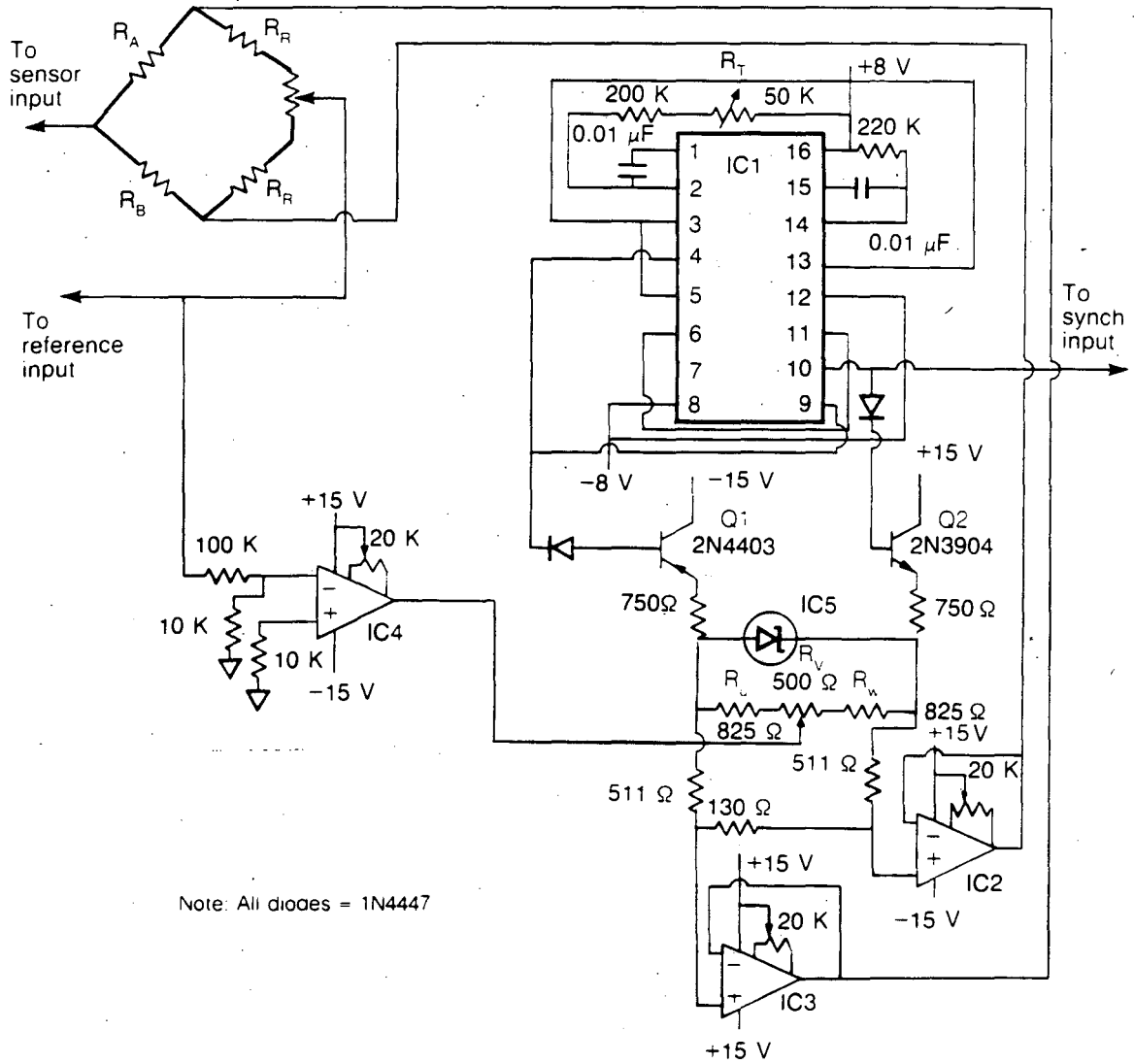
- (2) Motorola, CMOS Integrated Circuits, Motorola Semiconductor Products, Inc., 1978.
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- (5) A. VanDer Ziel, Noise in Measurements, John Wiley and Sons, New York, 1976, p. 91.

Table 1. Measured Harmonic Response of the Phase-Sensitive Detector Rectifier Circuit			
Multiple of Fundamental	Gain (units of 10^3)	Multiple of Fundamental	Gain $\times 10^{-3}$ (units of 10^3)
x1	0.6894	x6	0.0243
x2	0.0360	x7	0.0430
x3	0.0639	x8	-0.00737
x4	0.0466	x9	+0.0105
x5	0.0620	x10	-0.0140



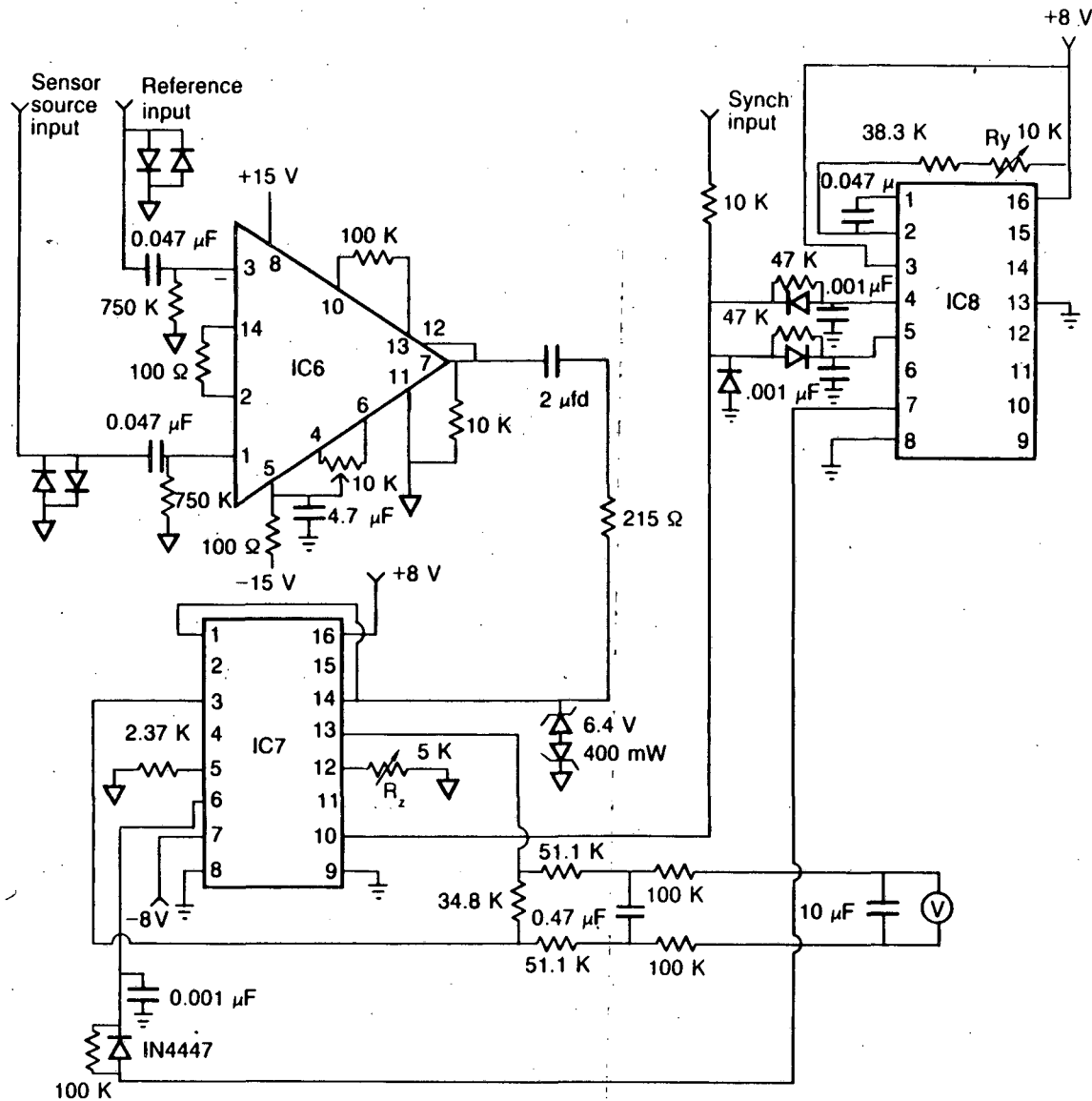
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Figure 1. The phase-sensitive detector circuit. (a) Block diagram.



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Figure 1. The phase-sensitive detector circuit. (b) Oscillator and bridge drive circuit.



Note: All diodes = 1N4447.

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Figure 1. The phase-sensitive detector circuit. (c) Amplifier and rectifier.

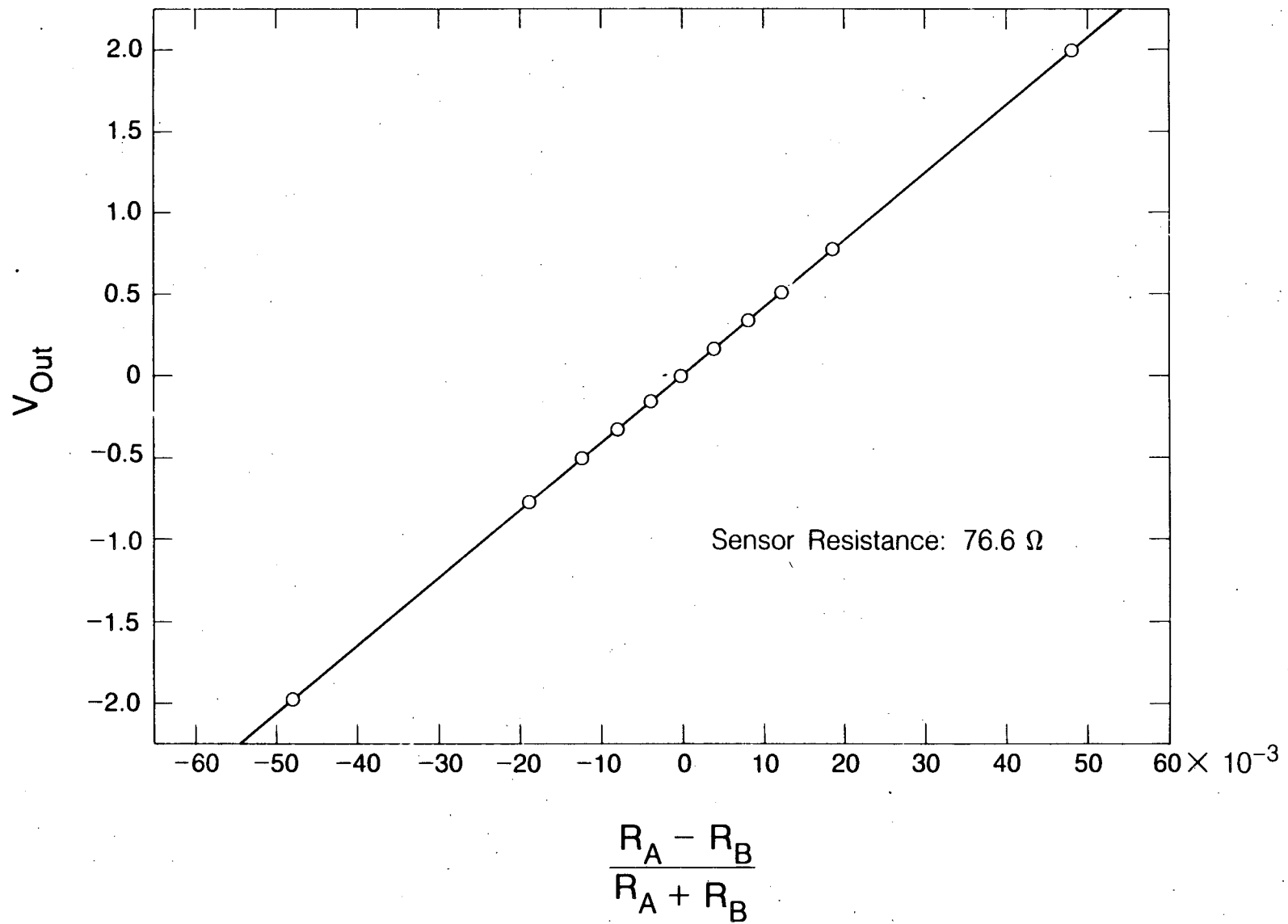


Figure 2. Detector calibration.

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