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Accurate Modeling of Nonideal Low-Power PWM DC-DC Converters Operating in CCM and DCM using Enhanced Circuit-Averaging Techniques

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The development of enhanced modeling techniques for the simulation of switched-mode Pulse Width Modulated (PWM) DC-DC power converters using circuit averaging is the main focus of this article. The circuit-averaging technique has traditionally been used to model the behavior of PWM DC-DC converters without considering important nonideal characteristics of the switching devices. As a result, most of these existing approaches present simplified models that are ideal or linearized, and do not accurately account for the performance characteristics of the converter. This is especially problematic for low-power applications. In this article, we present an enhanced nonideal behavioral circuit-averaged model that makes the simulation of DC-DC converters both computationally efficient and accurate, thereby presenting an important tool for circuit designers. Experimentally, we show that our Verilog-A-based new model allows for accurate simulation of both Buck- and Boost-type PWM converters operating in either CCM or DCM modes while providing more than one order of magnitude speedup over the transistor-level simulation.

CCS Concepts: • **Computing methodologies** → *Model development and analysis*; • **Hardware** → *Electronic design automation*

Additional Key Words and Phrases: Integrated circuit modeling, circuit averaging, switched-mode power supplies, DC-DC converters

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1. INTRODUCTION

For the Electronic Design-Automation (EDA) of integrated circuits and systems, it is of particular importance that circuit designers have access to component and system models of varying complexity for use across a wide range of applications. Typically, the trade-off in model complexity is that of computation time versus accuracy. Complex detailed models are designed to accurately represent the physical behavior of devices. However, simulations that use such models typically have high CPU cost due to the size of the model and fine time resolution that is required. For certain types of circuits,

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such as switching power converter circuits, the designer might be interested in the overall performance of the circuit rather than in obtaining a detailed time-domain waveform. In this case, if the switching interval is considered to be small, the basic operation of a switching converter can be accurately predicted using compact circuit macromodels. In particular, time-domain switching converter models may capture key design characteristics such as switching ripples, responses to load or input transients, and small-signal frequency responses [Vorperian 1990a]. With these compact circuit models, and by ignoring the nonessential details of the switching transitions, simulations over many switching periods can be completed efficiently using general-purpose Computer-Aided-Design (CAD) tools.

Circuit-averaged models have long been used for the prediction of the dynamic and steady-state responses of power electronic converters [Vorperian 1990a, 1990b; Maksimovic et al. 2001]. Averaging is a systematic way to obtain a simplified model that focuses on the cycle-to-cycle behavior without worrying about the details of the switching cycles. Averaging methods include averaged state-space models [Davoudi et al. 2006], which are equation based, or circuit-averaging techniques, which rely on developing equivalent averaged circuit models [Maksimovic et al. 2001]. These techniques provide physical insight and are helpful in developing analytical relations that can be used in the design process to select component and controller parameter values for a given set of desired specifications and performance figures of merit [Maksimovic et al. 2001; Sanders and Verghese 1991]. Most of these models, however, have been developed for modeling the performance of off-chip converters that are typically used to control the power flow to larger devices and appliances. Moreover, most of the models presented in the literature rely on ideal or linearized components to model the losses and nonidealities that are present in the circuit [Kovar et al. 2009; Nirguade et al. 2001]. This is a significant limitation, particularly in the case of low-power electronic converters, as these models will not account for many of the performance characteristics of microelectronic circuits.

In this article, we present for the first time an enhanced circuit-averaged model that is optimized to capture the dynamic behavior of Pulse Width Modulated (PWM) DC-DC converters, particularly in low-power Integrated Circuit (IC) applications. The enhanced model utilizes nonlinear controlled sources and elements to capture the nonideal characteristics of the semiconductor devices present in the converter. More specifically, our enhanced model will account for the nonideal behavior of the diodes and MOS transistors during converter operation, thereby significantly improving the accuracy of the analysis results when compared to traditional PWM circuit-averaged models present in the literature. We will show that our proposed model works well for both large-signal and small-signal dynamic simulations under varying operating conditions. We will also show how the model can be further improved by capturing the effects of subthreshold leakage currents. Furthermore, we present a technique to automate the extraction of the device parameters of our proposed model from industry-standard device models such as BSIM4 [Dunga et al. 2006] using simulation-based device characterization for additional accuracy. Finally, our new modeling technique is rather general and can be applied to both Buck- and Boost-type converters operating in both Continuous-Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) in addition to standard and synchronous configurations, which are of particular importance for low-power applications. The new approach has the ability to capture both large- and small-signal dynamic behavior, thereby making it simple to apply in general EDA tools. It is important to note that the improved accuracy of the enhanced model is achieved without adding significant computation cost overhead to simulations that utilize it, thereby preserving the low CPU cost advantage of using circuit-averaged techniques. When coded in a standard behavioral modeling language, that is, Verilog-A,

Fig. 1. Standard Buck PWM DC-DC converter.

our model provides more than one order of magnitude runtime speedup over the time-consuming transistor-level simulation. As a result, circuit averaging, as employed in this work, becomes an efficient practical tool for circuit designers studying the dynamics of switch-mode DC-DC converters for low-power applications.

2. ACCURATE MODELING OF PWM DC-DC CONVERTERS

Circuit-averaged models have long been used for the prediction of the dynamic and steady-state responses of power electronic converters. Most of the models presented in the literature, however, have been developed using ideal or linearized components to model the nonideal devices that are present in the circuit in an effort to preserve the simplicity and efficiency of the model.

In this article, we present an enhanced circuit-averaged model that uses nonlinear expressions of averaged quantities to model the nonideal devices in the circuit, thereby producing more accurate results. In this section, we present an overview of how we model the nonlinear diode and transistor expressions, followed by the proposed enhanced circuit-averaged models and equations. The detailed derivations of the models are best described with the aid of an example converter circuit. In this section, we will use the standard Buck converter of Figure 1(b) operating in CCM with the switching waveform $q(t)$ as given in Figure 1(a), unless otherwise specified. The detailed derivation will then be followed with a presentation of generalized models that are applicable to PWM converters operating in CCM as well as DCM in addition to synchronous topologies. The proposed accurate models are developed to be used in conjunction with a variety of analysis types, including large-signal simulations (for the computation of the operating-point and steady-state ripple), small-signal simulations, and simulation of dynamic behavior.

2.1. Modeling the Nonideal Devices

The proposed enhanced circuit model is applicable to general circuit nonidealities. Here, we focus on the two nonlinear semiconductor devices that are typically present in ICs, the pn-junction diode and the MOS transistor. These devices have the greatest effect on the accuracy of the model.

2.1.1. Diodes. The semiconductor pn-junction diode is one of the fundamental elements typically present in switching power converter circuits. The relation between the diode current I_D and diode voltage V_D is

$$I_D = I_s(e^{V_D/nV_T} - 1) \approx I_s e^{V_D/V_T}. \quad (1)$$

In this relation, I_s is the saturation current and V_T is the thermal voltage. For micro-electronic circuits, I_s is typically in the 10^{-15} amp range, which results in a considerable forward voltage drop under normal operating conditions. Typical averaged models for

this relation include the ideal diode model (with zero voltage drop), the constant drop model (with a fixed voltage drop) and the small-signal model (with a linear current–voltage relation) [Sedra and Smith 2009]. For low-power applications, the accuracy provided by these traditional models is not sufficient. Higher accuracy is achieved when the nonlinear current–voltage relation is included in the model, which is the main objective of our approach. For our model, it is more convenient to express the average diode voltage, $\bar{V}_D$, as a function of the average current, $\bar{I}_D$, as follows:

$$\bar{V}_D \approx V_T \ln \left(\frac{\bar{I}_D}{I_s} \right). \quad (2)$$

In this relation, we have assumed that the average of the logarithm is approximately the same as the logarithm of the average. This is a valid assumption in this case since $I_D(t)$ does not deviate too much from its average value.

2.1.2. MOS Transistors. In PWM converters, the active power switch is typically implemented using a MOS transistor driven by a PWM signal with a specified duty cycle and is biased to operate in the triode region when conducting. Traditional averaged models either assume no voltage drop (ideal switch case) or linearize the current–voltage relation. To achieve a more accurate averaged model, we include the current–voltage relation of the MOS device as a nonlinear resistor relating the average voltage drop to the average drain current as follows:

$$I_d = f(V_{DS}) = k' \left(\frac{W}{L} \right) V_{OV} \left(V_{DS} - \frac{1}{2} V_{DS}^2 \right) \quad (3)$$

$$\bar{V}_{DS} = f(\bar{I}_d) \approx \frac{\bar{I}_d}{k' \left(\frac{W}{L} \right) V_{OV}}, \quad (4)$$

with k' and (W/L) being transistor parameters, while $V_{OV} = V_{GS} - V_{th}$ and V_{DS} are the overdrive and drain-to-source voltages, respectively, and I_d is the transistor drain current [Sedra and Smith 2009]. It is important to note that, although we have only focused on the effect of one nonideality for each of the diodes and the MOS transistor to be included in our model (as given by Equations (2) and (4)), the effect of other nonidealities can also be included in our model using similar techniques to further refine its accuracy. One example is the effect of subthreshold leakage current, which we will show in Section 4.

2.2. Nonideal Large-Signal PWM Switch Model

2.2.1. Standard Converters. Consider the Buck converter shown in Figure 1(b). When the MOS switch is driven by the waveform $q(t)$, as shown in Figure 1(a), the converter essentially operates in one of two configurations. We apply circuit averaging to derive a dynamical model that can capture large-signal variations at the output load. In this case, we assume that the switching frequency of the converter is faster than the time scales of other signals in the converter such that the transient effects of these signals can be averaged out within each switching cycle. We will also neglect the small voltage drop across the inductance resistor r_L for simplicity.

The first configuration occurs when the transistor is on with the diode reverse-biased, while the second occurs when the transistor is off with the diode conducting.

Fig. 2. Proposed accurate average circuit model for the Buck PWM converter operating in CCM.

(a) Standard PWM converter

(b) Synchronous PWM converter

Fig. 3. Proposed accurate hybrid average circuit model for the PWM switch in CCM and DCM.

The governing circuit equations averaged over one switching period will be:

$$L \frac{d\bar{I}_L}{dt} = d_1(\bar{V}_S - \bar{V}_{DS}) - (1 - d_1)\bar{V}_D - \bar{V}_{out} \quad (5)$$

$$C \frac{d\bar{V}_{out}}{dt} = \bar{I}_L - \frac{\bar{V}_{out}}{R_L} \quad (6)$$

$$\bar{I}_D = (1 - d_1)\bar{I}_L \quad (7)$$

$$\bar{I}_S = d_1\bar{I}_L, \quad (8)$$

where d_1 is the duty ratio of the switching waveform $q(t)$ for fixed duty cycle converters. Additional equations for the additional variables $\bar{V}_D$ and $\bar{V}_{DS}$ are obtained from the nonlinear relations given in Equations (2) and in (4), respectively. We also note that the average voltage drop across the inductor and the average current through the capacitor will be zero in steady-state. The relations in Equations (5) to (8) can be combined into one equivalent enhanced averaged circuit model, as shown in Figure 2. As can be seen, the simplicity of circuit-averaged models is preserved while having a better representation of the nonideal behavior of the semiconductor devices over linearized or ideal models.

The derivation in this section is based on the standard Buck converter shown in Figure 1(b) operating in CCM. Similar derivations can be made for DCM operation in addition to other PWM converter types. To facilitate the application of this model in a standard behavioral modeling language such as Verilog-A, the proposed hybrid general accurate model of the PWM switch for CCM and DCM operation is shown in Figure 3(a). The expressions for d_2 vary depending on the mode of operation, as follows:

$$d_2 = 1 - d_1 \text{ (for CCM)} \quad (9)$$

$$d_2 = D_{con} - d_1 \text{ (for DCM)}, \quad (10)$$

where

$$D_{con} = \frac{2L}{T} \frac{|\bar{I}_C|}{\bar{V}_{AC}d_1}. \quad (11)$$

When $D_{con} \leq 1$, the converter operates in CCM. When $D_{con} > 1$, the converter operates in DCM. In these relations, L is the inductor value and T is the switching frequency [Ben-Yaakov and Adar 1994].

2.2.2. Synchronous Converters. It is important to note that an enhanced circuit-averaged model can also be developed for use in conjunction with synchronous converters, which are especially popular in low-power applications. Synchronous converter structures utilize two switches instead of one switch and one diode. A fundamentally similar modeling approach to that of standard converters can be developed by considering the device-level nonideal effects of the additional MOS device instead of those of the diode under the assumption that the transition “dead” time between switches is negligible and in the presence of zero-current detection circuitry [Chen et al. 2008; Yousefzadeh and Maksimovic 2006]. In this case, V_{DS} is replaced with V_{DS1} and V_D is replaced with V_{DS2} in the derivations of Equations (5) to (8) to represent the voltage drops associated with the two MOS device switches. Finally, the hybrid model of Figure 3(a) will have an additional nonlinear resistor in the place of the dependent source $\bar{V}_D$, which results in the hybrid model shown in Figure 3(b).

2.3. Nonideal Large-Signal Output Ripple Expression

Most DC-DC converters experience a large-signal DC ripple at the output due to large-signal variations of the input voltage and output load [Hart 2011]. Therefore, it is important that the accurate model that we are proposing also factors in the effect of $\bar{V}_D$ and $\bar{V}_{DS}$ in the expression for the ripple waveform. Again, we base our detailed derivation on the Buck converter of Figure 1(b).

When the MOS transistor switch is on and the diode is reverse biased, we can develop an expression for the variation in inductor current, ΔI_L , during one switching cycle. Assuming a linear rate of change of current, the change in inductor current during the on and off cycles of the transistor can be expressed as:

$$(\Delta I_L)_{ON} = \left(\frac{V_S - V_{DS} - V_{out}}{L} \right) d_1 T \quad (12)$$

$$(\Delta I_L)_{OFF} = \left(\frac{-V_D - V_{out}}{L} \right) (1 - d_1) T, \quad (13)$$

where d_1 is the duty ratio as before, and T is the switching period.

The expressions for the ripple voltage at the output are obtained from two relations for the charge, Q , across the capacitor. The first is the capacitor charge–voltage relation arising from the definition of capacitance as $\Delta Q = C \Delta V_{out}$. The second arises from the relation between the charge and the capacitor current. Since the steady-state average current through the capacitor is zero, the waveform of the capacitor current in the Buck converter will vary proportionally with the current through the inductor [Hart 2011]. Combining these two relations with that of Equation (13) results in

$$\Delta V_{out} = \frac{T \Delta I_L}{8C} = \frac{T}{8LC} (-V_D - V_{out})(1 - d_1) T. \quad (14)$$

Fig. 4. Accurate small-signal model for the Buck converter in CCM.

The averaged value of the output ripple voltage can now be obtained by averaging the expression in Equation (14), which gives the following:

$$\Delta \bar{V}_{out} = \frac{(1-d_1)(\bar{V}_D + \bar{V}_{out})}{8LCf^2}. \quad (15)$$

The expression in Equation (15) can be used to determine an enhanced estimate of the steady-state large-signal ripple waveform at the output of the converter once the large-signal operating point is determined using the proposed averaged models presented in Sections 2.2 and 4. Similar expressions can be developed for other standard PWM converter topologies.

2.4. Nonideal Small-Signal Dynamic PWM Switch Model

In contrast to the large-signal models derived previously, the small-signal assumption needs to be made in order to characterize the variation of duty cycle, since the converter operation intrinsically depends on it. Once the steady-state operating point has been determined, small-signal dynamic models can be developed to track small changes in duty cycle or supply voltage [Maksimovic et al. 2001]. In this case, if $\hat{v}_s(t)$ and $\hat{d}(t)$ represent small deviations from the steady-state supply voltage and duty ratio, respectively, then we have that

$$V_S(t) = V_S + \hat{v}_s(t) \quad (16)$$

$$d_1(t) = d_1 + \hat{d}(t). \quad (17)$$

Once all the transients have subsided, converter-dependent voltages and currents will also consist of the average large-signal operating point values plus small ac variations. By substituting the compound relations for voltages and currents into Equation (5) and neglecting the dc terms (which add to zero since the inductor voltage in steady-state is zero), in addition to neglecting the second-order ac terms due to the small-signal assumption, the resulting expressions become

$$L \frac{d\hat{i}_l(t)}{dt} = d_1 \hat{v}_s(t) + \hat{d}(t)V_S - \hat{v}_o(t) - (1-d_1)\hat{v}_d(t) + \hat{d}(t)\bar{V}_D \quad (18)$$

$$C \frac{d\hat{v}_o(t)}{dt} = \hat{i}_l(t) - \frac{\hat{v}_o(t)}{R_L} \quad (19)$$

$$\hat{i}_s(t) = \hat{d}(t)\bar{I}_L + d_1 \hat{i}_l(t). \quad (20)$$

These equations can be modeled using an equivalent small-signal circuit model, which is shown in Figure 4.

3. SIMULATION-BASED DEVICE CHARACTERIZATION

In Section 2.1, we modeled the time-averaged behavior of diodes and transistors through the use of nonlinear expressions given in Equations (2) and (4). While such

Fig. 5. Real-time evaluation of $V_{ds(ON)}$ for transistor Q_1 .

Fig. 6. PWM switch circuit and its equivalent circuits when switch S is ON and OFF.

an approach is accurate and simple, it does have some limitations. First, it is a device-specific approach, which means that the diode and transistor parameters required to evaluate the nonlinear expressions of Equations (2) and (4) need to be recomputed for different technologies and different devices. This makes the calculation of the device model parameters difficult to automate for arbitrary circuits and devices. Furthermore, the relations in Equations (2) and (4) capture only the most fundamental behavioral characteristics of the nonideal devices, thereby limiting the accuracy of the simulations that utilize this model.

To address these issues, a new method for simulation-based device characterization is proposed. This method allows for the accurate and automated computation of the diode forward voltage drop V_d and the transistor voltage drop $V_{ds(ON)}$ during the simulation of averaged circuits, in addition to the computation of other parameters such as the subthreshold leakage current i_{leak} (introduced in Section 4). This method is best illustrated with an example. Consider the case of calculating $V_{ds(ON)}$ for a MOS transistor device. Figure 5(a) shows a Boost converter with transistor Q_1 on. The gate-to-source voltage is V_s and the drain-to-source current is $I_{ds(ON)}$. Figure 5(b) shows the circuit that is used to evaluate $V_{ds(ON)}$ during the simulation of the averaged circuit. The circuit is designed such that Q_2 has the same size, gate-to-source voltage and drain-to-source current as that in Figure 5(a) in order to ensure that $V_{DS(ON)}$ measured in Figure 5(b) is the same as $V_{ds(ON)}$ of Q_1 in Figure 5(a). Both $I_{ds(ON)}$ and V_s are easy to compute using averaged circuit models. V_s is simply the amplitude of the switching signal, whereas $I_{ds(ON)}$ can be determined from Figure 7 using

$$I_{ds(ON)} = \frac{\bar{I}_{ds}}{d_1 + d_2} = \frac{\bar{I}_A}{d_1 + d_2}.$$

Fundamentally similar procedures can be performed to calculate i_{leak} and V_d .

The proposed approach for simulation-based device characterization accounts for all nonideal characteristics included in the original transistor and diode device models. Therefore, the accuracy of the averaged model becomes potentially as good as the device model itself. This is one of the main advantages that the proposed model presents over

Fig. 7. The currents i_A , i_C , and i_P of the PWM switch circuit when accounting for subthreshold leakage current i_{leak} .

conventional linear averaged models of the switching circuit. In this article, we utilize the BSIM4 model [Dunga et al. 2006] for all transistors. As a result, many nonideal characteristics, including short-channel effects and sub-threshold effects, become accounted for when simulation-based device characterization is performed. However, it is important to note that this technique captures only the DC characteristics of devices, meaning that any higher-order responses caused by fast switching activities are neglected. This is consistent with the nature of average circuit models, which essentially capture the DC (average) component of the real circuit response.

4. FURTHER ENHANCEMENTS: ACCOUNTING FOR SUBTHRESHOLD CURRENT EFFECTS

When testing the hybrid model of Figure 3(a) on a standard Buck converter operating in both CCM and DCM, the results obtained were found to be accurate while significantly reducing the computation time when compared to simulating the full converter circuit, as will be shown in Section 5. However, when the model was tested on some other PWM converter topologies and designs, some results were found to be less accurate due to limitations in the circuit-averaged models of the nonideal devices. One of the fundamental contributors to discrepancies in the results was not accounting for the effects of the subthreshold leakage current during the OFF-cycle of the transistor switch [Rabaey et al. 2003], especially when it was not insignificant when compared to the load current.

The circuit averaged hybrid model of the PWM switch shown in Figure 3(a) can be modified to account for the effects of subthreshold conduction. For the derivation of the modified model in this section, we will assume the converter is operating in DCM, since CCM is a special case of DCM with $d_1 + d_2 = 1$. Figures 6(b) and 6(c) show the equivalent circuits of the PWM switch of Figure 6(a) during the transistor ON and OFF cycles, respectively, where $R_{ds(ON)}$ is the equivalent resistance of the transistor under subthreshold conduction. The waveforms of the terminal currents i_C , i_A , and i_P of Figure 6 over one switching cycle are shown in Figure 7.

When the transistor switch S is on, as shown in Figure 6(b), the average voltage between terminals C and A is given by the relation

$$\bar{V}_{CA} = \bar{V}_{CA(ON)} = L \frac{\Delta i_L}{d_1 T_s} + R_{ds(ON)} \cdot i_{c(ON)}, \quad (21)$$

where Δi_L is the amplitude of the inductor current ripple, as shown in Figure 7, and $i_{c(ON)}$ is the current of terminal C when the transistor is on. We will consider the relation in Equation (21) to be the average voltage over the entire switching period under the assumption that the circuit time constant is much bigger than the switching period [Amran et al. 1991]. The same assumption also holds for the average voltage across

Fig. 8. The modified PWM switch model that accounts for subthreshold conduction.

Fig. 9. The proposed unified PWM switch model, consisting of a new averaged model and simulation-based device characterization. The three subcircuits on the right evaluate $V_{DS(ON)}$, i_{leak} , and V_d , respectively.

terminals P and C , denoted $\bar{V}_{PC}$. When the transistor is OFF, as shown in Figure 6(c), we have that

$$\bar{V}_{PC} = \bar{V}_{PC(OFF)} = L \frac{\Delta i_L}{d_2 T_s} + V_d, \quad (22)$$

where V_d is the forward voltage drop of the diode. By combining Equations (21) and (22), we obtain the voltage relation of our new PWM switch model:

$$\bar{V}_{PC} = \mu \cdot \bar{V}_{ca} - \mu R_{ds(ON)} \cdot i_{c(ON)} + V_d. \quad (23)$$

Note that the voltage relation given in Equation (23) is independent of the value $R_{ds(OFF)}$ due to the approximation made when deriving Equation (21). In practice, the effects of $R_{ds(OFF)}$ on voltage relations are negligible. As for the current relations, the average values of i_C , i_A , and i_P in Figure 7 are found to be

$$\bar{I}_C = \left(i_{pk} - \frac{\Delta i_L}{2} \right) (d_1 + d_2) \quad (24)$$

$$\bar{I}_A = \left(i_{pk} - \frac{\Delta i_L}{2} \right) d_1 + i_{leak} \cdot d_2 \quad (25)$$

$$\bar{I}_P = \left(i_{pk} - \frac{\Delta i_L}{2} \right) d_2 + i_{leak} \cdot d_2, \quad (26)$$

where i_{pk} is the peak value of the inductor current i_L , and i_{leak} is the subthreshold current flowing through $R_{DS(OFF)}$. Finally, $\bar{I}_A$ can be rewritten as

$$\bar{I}_A = \frac{d_1}{d_2} \bar{I}_P + (d_1 + d_2) i_{leak}. \quad (27)$$

Figure 8 shows the modified PWM switch model that accounts for the effects of leakage current, whereas Figure 9 shows a unified model for the circuit-averaged PWM switch, which consists of a combination of Figure 8 and the simulation-based device characterization circuits. This model can be used for several DC-DC converters that

Fig. 10. Circuit Diagrams of the Boost PWM DC-DC converters tested.

Table I. Component Values for the Example Circuits

Component	Boost Converter	Buck Converter	Synchronous Boost
L	$300\mu H$	$100\mu H$	$300\mu H$
C	$1\mu F$	$500nF$	$10\mu F$
r_L	$50m\Omega$	$50m\Omega$	$50m\Omega$
r_C (ESR)	$50m\Omega$	$50m\Omega$	$5m\Omega$

share the same structure, for example, Buck, Boost, and Buck-Boost. It also accommodates operation in both CCM and DCM, as explained in Section 2.2. Furthermore, the evaluation of the voltage drops associated with diodes and transistors is performed in real time. Finally, it is important to note that the efficiency of simulating the unified PWM switch model is not affected by including the simulation-based device characterization circuits despite the presence of diodes and transistors since no switching activities appear in any of those devices.

5. NUMERICAL EXAMPLES

The enhanced averaged model proposed in this article is implemented in Cadence Virtuoso and simulated using Spectre with 90nm technology. The original converters are described by transistor-level netlists with interfaces to industry standard BSIM4 models. The average models are coded using Verilog-A. Testing of the proposed model is performed on a combination of Boost and Buck converters using a mix of open-loop and closed-loop simulations. We compare the accuracy and speedup of our proposed models with the simulations of the transistor-level circuits and comment on the improvements obtained over existing averaged models found in the literature. Note that all simulations are performed on a Linux workstation with 4GB of memory and a quad-core 3.2GHz Intel Core i5 processor, although only one core was utilized.

5.1. Boost Converter Open-Loop Simulation

The Boost converter shown in Figure 10(a) is tested with the component values given in Table I. The switching frequency of the converter is 50kHz for a load resistor of 5Ω. The original transistor-level converter circuit and the averaged circuit are simulated with a startup transient of varying duty ratios. The duty ratio of the converter is controlled by a step signal such that the circuit starts with an initial duty ratio of 30% that is then stepped up to 60%. After 40μs, the duty ratio is stepped down to 40%.

Figure 11 shows a comparison of the output voltage and the inductor current obtained using three different averaged models. The first model is a naïve (ideal) averaged model with zero voltage drops across the diode and MOS switch. The second model is a

Fig. 11. Transient analysis of the Boost converter using three different averaged models.

Table II. Simulation Results for the Various Example Circuits

Converter	Parameter	Transistor-Level	Conventional Averaged Model	Proposed Enhanced Model
Open-Loop Boost	Simulation Time	652s	32s	48s
	Speedup	-	20X	13X
	Error/Discrepancy	-	30.60%	0.60%
Closed-Loop Buck	Simulation Time	1654s	47s	55s
	Speedup	-	35X	30X
	Error/Discrepancy	-	5.00%	0.03%
Synchronous Open-Loop Boost	Simulation Time	667s	-	48s
	Speedup	-	-	14X
	Error/Discrepancy	-	-	0.20%

traditional linear averaged model which assumes a constant voltage drop across the diode and a linear voltage drop across the MOS switch [Erickson and Maksimovic 2001]. The final model is our proposed averaged model. The waveforms of the original converter circuit are also provided in Figure 11 for reference. As can be seen, our model presents a significant improvement in accuracy over other averaged models. This improvement comes at the expense of some additional computation cost overhead, although the simulation time remains significantly faster than transistor-level simulations. This is clearly illustrated in the numerical comparison given in Table II. It is also important to note that, although both the linear model and our proposed model account for the effect of device nonidealities and parasitics, they do so in fundamentally different ways. As an example, the value of V_{DS} is accounted for in the linear model using a resistor, which is measured in steady-state simulation and fixed during the average model simulation. On the other hand, our proposed model measures the value of V_{DS} continuously during the average model simulation based on the circuit states. One can immediately see that the linear model can get a good estimation only in steady state, but not in the transient state in which the circuit states are dynamically changing. Furthermore, using the BSIM4 model to evaluate the values of $I_{DS(ON)}$ and $I_{DS(OFF)}$ provides improved accuracy over using device equations for the evaluations. Figure 12 shows a close-up comparison of the waveforms for the three models for additional clarity. The speedup obtained using the proposed model was $13\times$ over the original converter.

Fig. 12. Close-up comparison of the proposed averaged model with the other models.

Fig. 13. Closed-loop Buck converter simulation showing the variation of the load resistance (top) and the output voltage waveforms (bottom).

5.2. Buck Converter Closed-Loop Simulation

The Buck converter shown in Figure 1(b) is tested with the component values given in Table I, operating in a closed-loop configuration with variations of the load resistance used to mimic time-varying changes of the load. Its corresponding averaged model is shown in Figure 2. The input voltage is set to 2V while the switching frequency is set to 20kHz. The load resistance is initially set to 5 Ω , followed by a sinusoidal variation. The output voltage is regulated at 0.6V by the PWM-controlled feedback loop. Figure 13 shows the variation of the load resistance and output voltage for both circuits; the numerical simulation data is summarized in Table II. When compared with the actual Buck converter, a speedup of 30 $\times$ is obtained using our proposed averaged model.

To assess the robustness of the hybrid averaged model, the load resistance is controlled in such a way that the Buck converter transitions between operation in DCM and CCM. The top graph of Figure 14 shows D_{con} evaluated according to Equation (11), which indicates the operation mode of the converter. At 53 μ s after the simulation starts, the model switches from DCM to CCM, and D_{con} reaches 1. As shown in the

Fig. 14. How the averaged model determines the converter conduction mode (top) and the resulting inductor currents (bottom).

Fig. 15. Open-loop synchronous Boost converter simulation showing the variation of the load resistance (top) and the output voltage waveforms (bottom).

bottom waveform of Figure 14, our averaged model precisely captures this transition. It is also important to emphasize how closely the inductor current of the proposed averaged model follows that of the original circuit.

Finally, a comparison of the large-signal ripple voltage at the output of the converter is performed. The actual large-signal ripple voltage is 16.69mV. The large-signal ripple voltage computed using a linear expression, as shown in [Hart 2011], is 14.9mV. Using the expression derived from our model in Equation (15) gives 16.8mV, which again verifies the improved accuracy of our proposed model.

5.3. Synchronous Boost Converter Open-Loop Simulation

Finally, to demonstrate the effectiveness of the proposed model on synchronous converters, the synchronous Boost converter of Figure 10(b) is simulated using the components given in Table I. The comparison of the results obtained using the proposed model with those of the transistor level simulation are shown in Figure 15 and summarized in Table II. As can be seen, the accuracy of the results is quite high, with a simulation time that is significantly reduced.

6. CONCLUSION

We have presented an enhanced circuit-averaging technique for the modeling of PWM DC-DC converters. The enhanced model accurately accounts for the nonideal characteristics present in the circuit, thereby providing improved numerical accuracy while preserving the computation cost advantage of circuit averaging. Enhanced equivalent circuit models have been presented for determining large-signal and small-signal characteristics in CCM and DCM. Simulation results obtained verified the efficiency and accuracy of the proposed model.

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