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A Resonant Cockcroft-Walton Switched-Capacitor Converter Achieving Full ZCS and >10kW/inch³ Power Density

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Abstract—Hybrid LC switched-capacitor converter architectures have demonstrated high power density while retaining efficiency at high conversion ratios. This work presents a resonant Cockcroft-Walton (CW) converter that achieves full zero-current switching (ZCS) on all switches using a single inductor and requiring only one current sensor. To do so, an N-phase clocking scheme is employed, eliminating the parallel paths that typically introduce transient shorting losses in a conventional 2-phase CW converter. The reduced voltage stress on the CW’s fly capacitors results in a dramatic reduction in volume when using common MLCC capacitors. A discrete 1:5 CW prototype using silicon FETs and a spiral trace inductor was assembled on two commonly available PCB processes: 0.8 mm FR4 with 2 oz. Cu, and 0.127 mm polyimide film with 0.75 oz. Cu. The latter achieved a peak efficiency of 95% and a maximum power density of 0.686 W/mm³ (11.2 kW/inch³) in a volume of 44.5 mm³ (0.00271 inch³), excluding level-shifting and clock generation circuits.

I. INTRODUCTION

Switched-capacitor (SC) DC-DC converters are often highly inefficient during heavy load conditions due to the voltage mismatch and transient current pulses that occur when initiating a subsequent switching phase: this is the cause of reduced efficiency ‘slow-switching-limit’ (SSL) operation discussed in [1] and results from this rapid charge distribution loss. To surmount this, several hybrid converter techniques have been proposed [2-12] that utilize an inductor in conjunction with a switched-capacitor stage to yield efficient energy transfer at lower switching frequencies (see Fig. 1 and Fig. 2). Lei [7] offered an insight into which SC topologies most easily lend themselves to hybrid resonant and soft-charging techniques. This work was further developed in [8] and [9], which demonstrated that increased control complexity using both zero-current switching (ZCS) and zero-voltage switching (ZVS) as part of a ‘split-phase’ switching regime could facilitate a Dickson SC topology that benefits from a hybrid LC architecture. The same multi-mode technique had earlier been demonstrated using the Cockcroft-Walton (CW) converter in [10] and [11] but achieved split-phase functionality using passive diode switching which performs inherent near-ZVS. At lower voltage levels where diode forward voltage drop generates significant losses, the [11] approach requires the same added design complexity as in [8] to effect ZVS using active switches for low loss. Reference [11] also relied on the fly

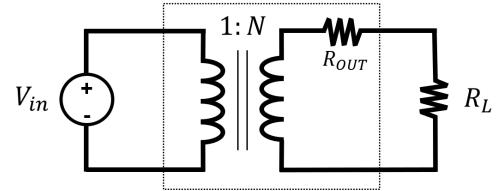


Fig. 1. Simplified model of a SC converter representing all conduction loss elements as a lumped output impedance R_{OUT} .

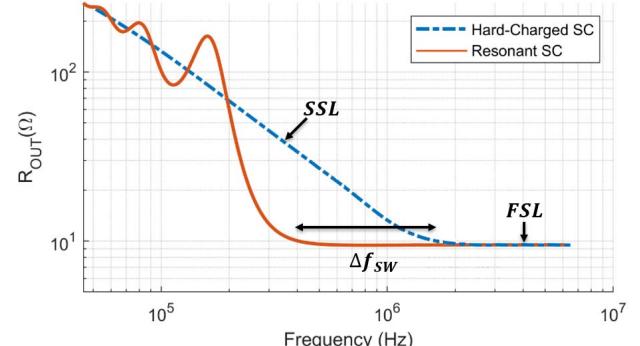


Fig. 2. Typical hard-charged and resonant switched-capacitor (SC) converter output impedance as a function of switching frequency.

capacitors to double as output filtering capacitors, thereby reducing their energy density utilization, although adjustable ripple control was implemented.

A Cockcroft-Walton variation with simplified gate driving and an added inductor for multiple inputs was presented in [12], also using diodes in its multiplier stage. This design utilized a dedicated output decoupling capacitor to offer a single-ended output with a common ground return path and allows for larger internal voltage ripple and more effective energy density utilization within the fly capacitors. However, the decoupling capacitor must be rated at the full output voltage and is used only for mitigating ripple and subsequently diminishes energy density utilization. For low-frequency high-density applications, the problematic introduction of a large output capacitor may potentially be mitigated using active energy buffering techniques such as those demonstrated in [13] and [14].

The Cockcroft-Walton topology offers a significant reduction in voltage stress on fly capacitors when compared with the Dickson topology, particularly at high conversion ratios. For

the 1:5 converters depicted in Fig. 3, fly capacitors C1, C2, C3, and C4 for a Dickson converter (Fig. 3 (a)) must tolerate V_{IN} , $2V_{IN}$, $3V_{IN}$, and $4V_{IN}$ respectively, whereas a CW converter (Fig. 3 (b)) need only tolerate V_{IN} , $2V_{IN}$, $2V_{IN}$ and $2V_{IN}$ respectively. This reduced voltage stress is significant for multilayer ceramic chip (MLCC) capacitors where a reduction in effective capacitance by more than 90% across the allowable voltage range is often observed in many commercial parts.

This work demonstrates a technique by which a single-phase Cockcroft-Walton DC-DC converter can be operated under complete resonant ZCS action, across all switches and across all phase transitions, using active switching (no diodes) and reduced sensing hardware complexity when compared with split-phase ZVS techniques. To do so, an N-phase switching scheme is employed which requires N switching configurations for a 1:N voltage ratio converter. Additionally, since N resonant cycles are required within a full period, this technique's inherent reduction in overall switching frequency make it attractive when combining multiple switching schemes for improved light-load efficiency.

The result is a high efficiency converter with a large conversion ratio and significant reduction in volume and/or weight making this technique attractive for several commercial applications, including mobile devices (e.g., backlight), biomedical devices (e.g., High Intensity Focused Ultrasound (HIFU)), and distributed power systems (e.g., solar, server racks, aviation).

II. CONVENTIONAL 2-PHASE COCKCROFT-WALTON

A conventional two-phase 1:5 CW converter is shown in Fig. 4. Due to the inherent parallelization of multiple capacitors and voltage sources across both phases (Phase 1: $V_{IN}||V_{C1}, V_{C2}||V_{C3}, (V_{IN}+V_{C2}+V_{C4})||V_{OUT}$, Phase 2: $(V_{IN}+V_{C1})||V_{C2}, V_{C3}||V_{C4}$), transient current pulses are inevitable due to rapid charge sharing, resulting in undesirable SSL operation. The optimization methodology described in [1] can be used in this case to minimize SSL losses but does not eliminate them.

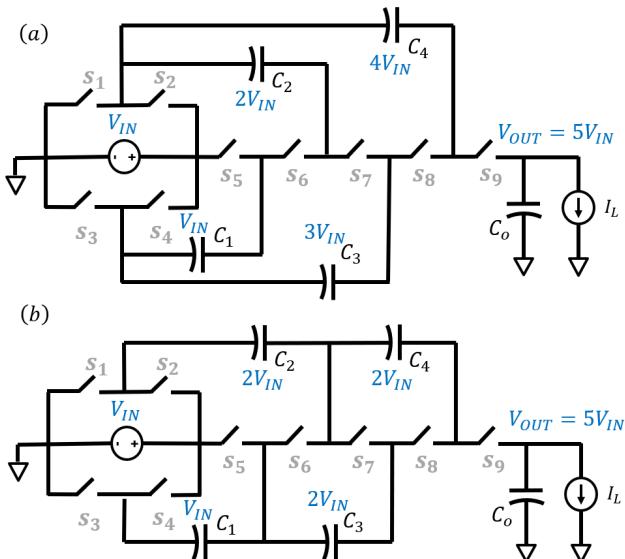


Fig. 3. (a) A 1:5 Dickson, (b) a 1:5 Cockcroft-Walton with reduced fly capacitor voltage stress.

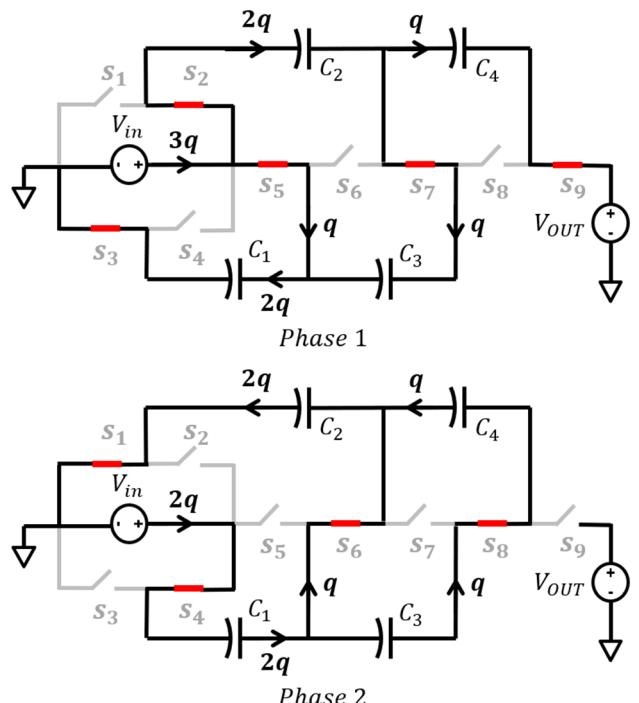


Fig. 4. A 1:5 Cockcroft-Walton operating under a typical 2-phase switching regime. Several parallel paths lead to SSL losses when no inductors are added. Charge flow is indicated as per the methodology presented in [1], verifying its operation as a 1:5 converter.

Placing an inductor at the input to effect ZCS or soft-charging does improve efficiency but cannot lead to full ZCS across all switches in a 2-phase switching regime without applying split-phase switching techniques at time sensitive points throughout both phases. Alternatively, an inductor could be placed between every parallel capacitor or voltage source connection during both phases, leading to a physically large converter solution. For a 1:N CW topology this would lead to $N/2$ inductors, where N is even, and $(N+1)/2$ inductors where N is odd.

III. N-PHASE RESONANT COCKCROFT-WALTON

To obtain full ZCS across all switches, we propose the N-phase switching regime depicted in Fig. 5. Due to its innate switching configurations, there is only ever one voltage loop that universally includes the input source. As a result, all transient current pulses can be mitigated by placing a single inductor immediately after the input source.

To achieve ZCS resonant mode, each phase's duration can be approximated by

$$T_{n0} \cong \pi\sqrt{LC_n} \quad (1)$$

Where C_n is the total effective capacitance seen by the input during phase n. This represents a 180° oscillation cycle, allowing inductor current to resonate from and to 0A (Fig. 6(a)). If the actual phase duration, T_n , were to increase beyond T_{n0} (Fig. 6 (b)), the converter would suffer a reversal of inductor current flow, with energy being returned ineffectively to the input source. If the phase duration is much greater than T_{n0} (Fig. 6 (c)), then the switch operation corresponds to a hard-charging event where $\frac{1}{2}C\Delta V^2$ of energy is dissipated in series resistances

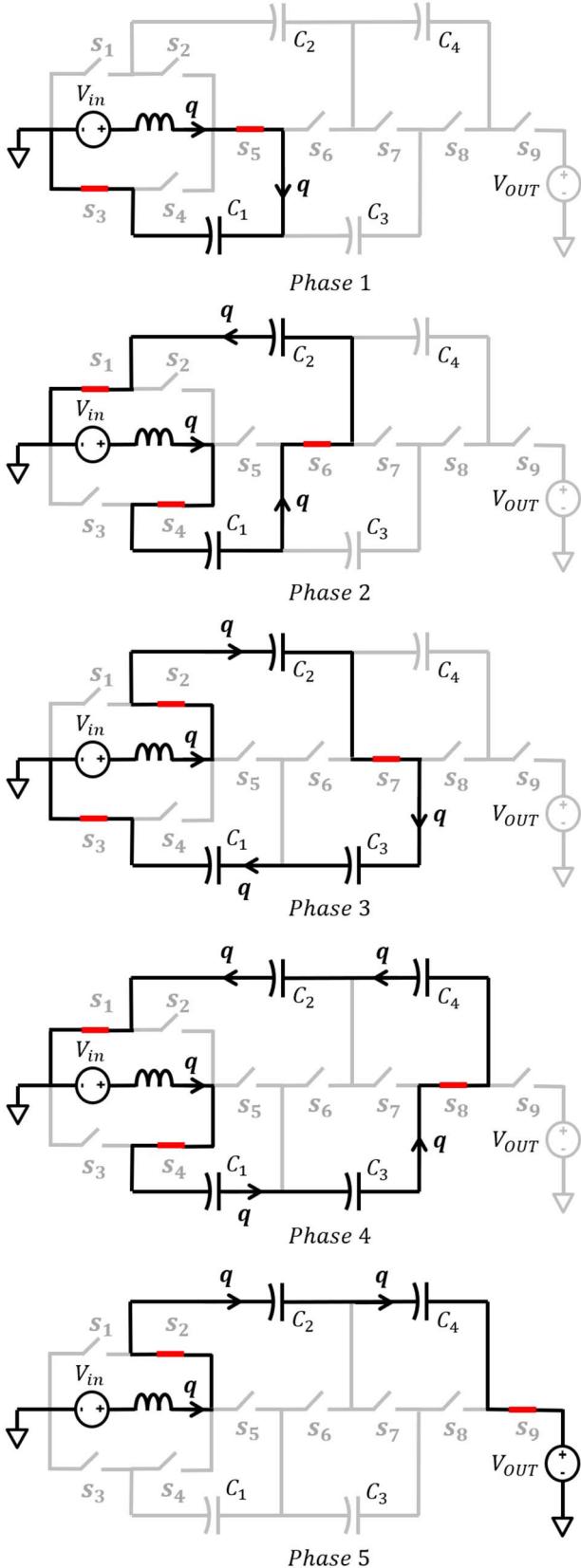


Fig. 5. The proposed N-phase switching regime for a N=5 Cockcroft-Walton converter.

defining the damped decay of the current waveform. Neither cases (b) nor (c) are desirable and result in the increasing output impedance variations with frequency seen in Fig. 2.

Integrating inductor current over a specified phase duration yields the net charge delivered by the inductor during that phase. Maximum charge is delivered by the inductor when the phase duration equals T_{n0} , with all phase durations greater than that delivering less net charge. As a result, if the phase duration must be longer than T_{n0} , it is more efficient for the converter to enter a discontinuous conduction mode (DCM) at $T_n=T_{n0}$, and pause in this state for the rest of the specified phase duration, than for it to allow any negative charge flow to occur (Fig. 6 (d)). Implementing a DCM allows the converter to retain a low output impedance while operating at low frequencies that would typically be deep into the SSL region [15].

Fig. 7 depicts simulated current and voltage waveforms illustrating complete ZCS between phases and smooth sinusoidal voltage transitions on fly capacitors, implying no SSL

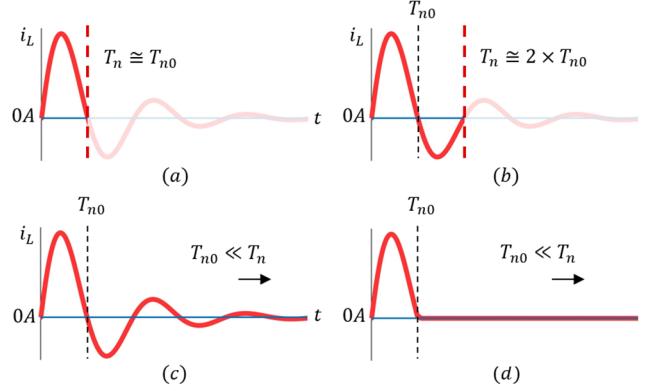


Fig. 6. Inductor current versus time for a phase duration, T_n , equaling; (a) T_{n0} , or half an underdamped oscillation; results in maximum charge transfer, (b) a full oscillation period; minimum charge transferred, (c) a duration much longer than the underdamped decay period, i.e. a hard-charging event, and (d) a duration longer than T_{n0} , but with a high impedance state maintained for $T_n > T_{n0}$, i.e. DCM.

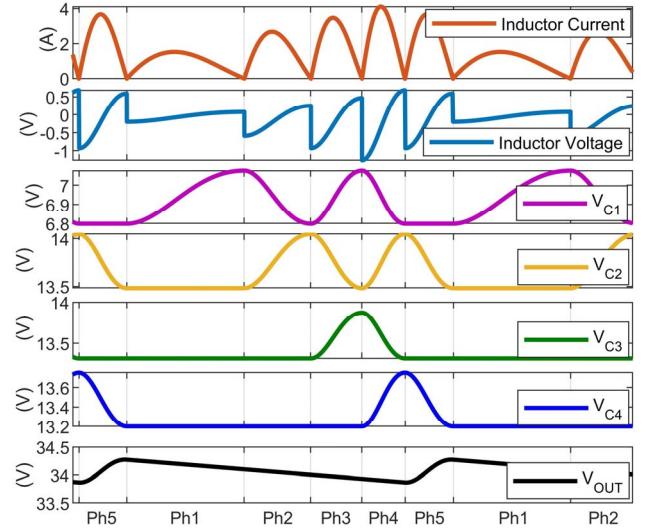


Fig. 7. Simulated results of the proposed technique, with N=5, $V_{in}=7V$, and $R_L=100\Omega$.

losses under N-phase operation: the inductor's ability to instantaneously change its voltage allows KVL to be satisfied around each phase's single loop while also inhibiting rapid charge sharing.

Unlike several topologies discussed in [7], there are no constraints placed on relative capacitor sizes in order to effect resonant or soft-charging operation and since SSL losses have largely been eliminated, the optimization method described in [1] for choosing capacitor sizes no longer applies. Instead, capacitors are chosen such that voltage ripple is maximized to fully avail of capacitor energy density, subject to the constraint that voltage tolerances not be exceeded.

IV. PROTOTYPE DESIGN AND RESULTS

Two 1:5 CW converters were constructed to demonstrate the described N-phase technique on common commercial PCB processes. The converters differ only in PCB substrate and metallization used, with otherwise identical parts and trace patterns (Fig. 8 and Table I). The first used 0.8 mm FR4 with 2 oz. copper and the second used 0.127 mm polyimide film with 0.75 oz. copper. The design goal was maximum power density in minimum size using discrete parts; to that end a 30 nH spiral trace inductor was patterned on the PCB reverse to save volume (Fig. 8 (b)). Auxiliary pads were also designed to allow for discrete inductor substitution and for comparative 0 nH hard-charged testing. The clock signals were generated externally using a Tektronix HFS9003 with phase durations automatically adjusted using a MATLAB control script until near-ZCS was achieved for all phases. The ADUM5210 level shifters were housed on a supporting motherboard which was designed for modular testability as opposed to size.

It is worth noting that for $V_{IN}=8V$ and a fixed effective fly capacitance requirement, a Dickson implementation would require a $1.48\times$ greater total volume of fly capacitance when accounting for capacitance degradation with applied voltage

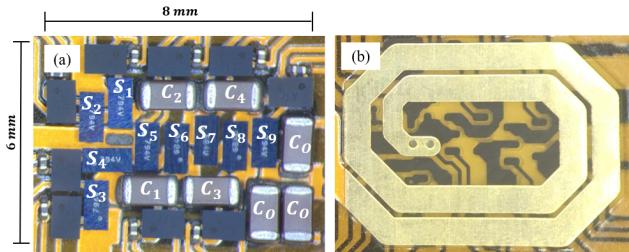


Fig. 8. (a) Constructed 1:5 CW prototype, (b) 30nH spiral trace inductor on PCB reverse.

TABLE I. COMPONENT LISTING FOR 1:5 COCKCROFT-WALTON

Component	Description	Part Number
S1-S5, S9	NMOS, 12V, 15mΩ, 4.3A	CSD13385F5T
S6-S8	NMOS, 30V, 26mΩ, 3.6A	CSD17585F5
C1-C4	10μF, 16V, X6S, 1608M	GRM188C81C106MA73
C _{OUT}	3×10μF, 35V, X5R, 1608M	GRM188R6YA106MA73
L	30nH Spiral Trace Inductor 150nH Powder Core	N/A SRP3012TA-R15Y
Gate Drivers	7A/5A, 0.8mm×1.2mm	LMG1020
Driver Caps	0.47μF, 6.3V, X5R, 0402M	GRM022R60J474ME15
Level-Shift	Dual-Channel Isolators	ADUM5210

bias, with this relative volume increase worsening at larger conversion ratios.

Fig. 9 and Fig. 10 show measured voltage waveforms for 0 nH hard-charged and 150 nH discrete inductor resonant-charged N-phase converters respectively. Abrupt voltage changes and damped settling behavior in Fig. 9 indicate distinct SSL losses in the hard-charged case. In contrast, the 150 nH resonant design exhibits smooth sinusoidal changes in capacitor voltages, with the inductor's near instantaneous voltage change allowing KVL to be satisfied across all phase transitions without significant transient current pulses. Fig. 11 depicts several additional voltage waveforms for the 150 nH resonant design.

To demonstrate the improvement in the resonant N-phase switching regime relative to a resonant 2-phase, measured efficiency curves are shown in Fig. 12 for the exact same 1:5 CW converter subject to both clocking schemes. Care was taken

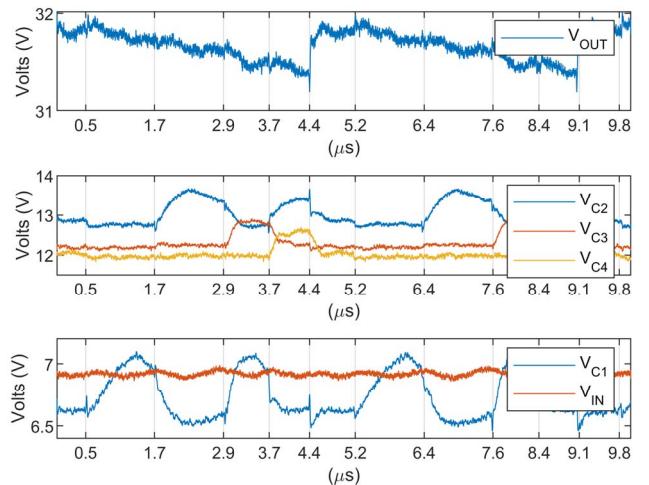


Fig. 9. Measured voltage waveforms for hard-charged 1:5 CW using 0.8mm FR4 with 2oz copper, $V_{IN}=7V$ and $R_L=160\Omega$. Damped voltage transitions indicate SSL losses.

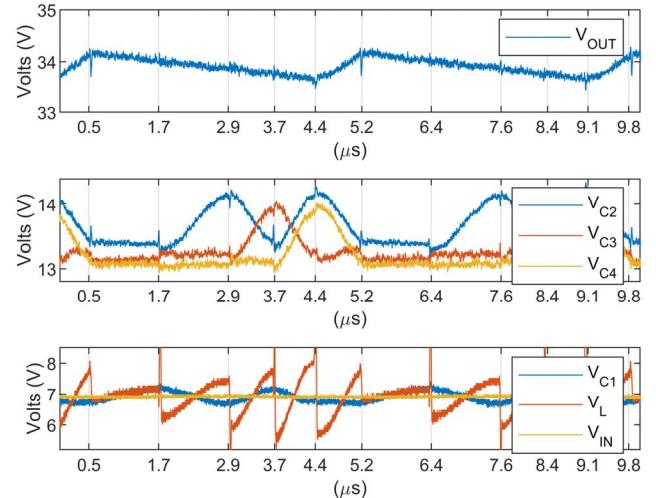


Fig. 10. Measured voltage waveforms for 150nH resonant 1:5 CW using 0.8mm FR4 with 2oz copper, $V_{IN}=7V$ and $R_L=160\Omega$. Smooth underdamped voltage transitions indicate extensive mitigation of SSL losses. V_L is voltage on inductor terminal opposed to the input voltage terminal.

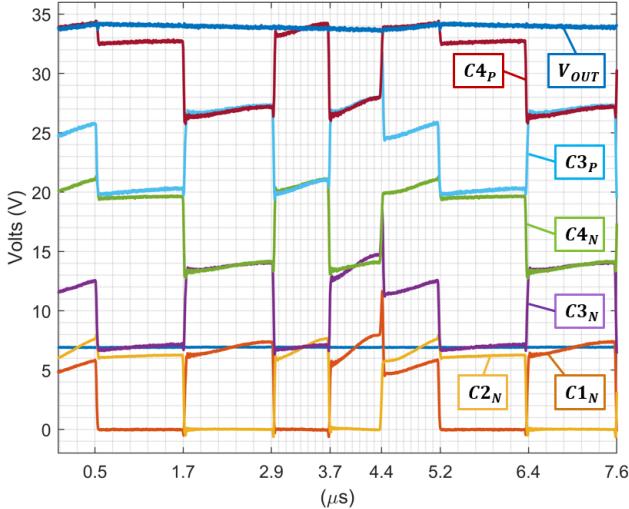


Fig. 11. Additional measured voltage waveforms for 150nH resonant 1:5 CW using 0.8mm FR4 with 2oz copper, $V_{in}=7V$ and $R_L=160\Omega$. ‘P’ and ‘N’ denote positive and negative capacitor terminals respectively.

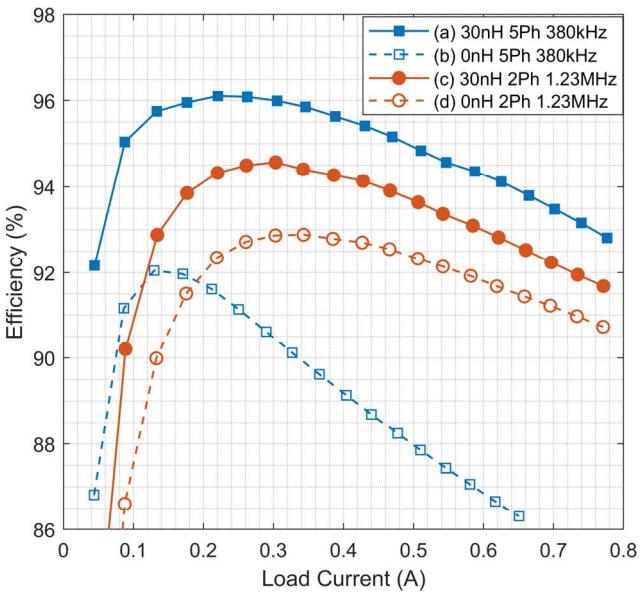


Fig. 12. Measured efficiency curves for (a) 5-phase 30nH resonant, (b) 5-phase 0nH hard-charged, (c) 2-phase 30nH resonant, and (d) 2-phase 0nH hard-charged modes. All measurements were taken using the same 1:5 CW 0.8mm FR4 2oz-Cu prototype, with $V_{in}=7V$ and the inductor being the only element changed between (a) & (c) and (b) & (d).

for both (a) and (c) to obtain near-perfect ZCS between phases to ensure a fair comparison. Both (b) and (d) are hard-charging configurations (no inductor) that use identical clocking to (a) and (c) respectively to illustrate the improvement due to resonant action. Despite worse hard-charging performance, when resonant ZCS is used the 5-phase scheme outperforms the conventional 2-phase approach due to its ability to fully mitigate the SSL losses.

At peak efficiency the 5-phase scheme offers a 31% reduction in total losses when compared with the 2-phase at the same load point. Additionally, the 5-phase’s lower overall switching frequency make it inherently more light-load efficient, with a 52.5% reduction in dynamic gate drive losses

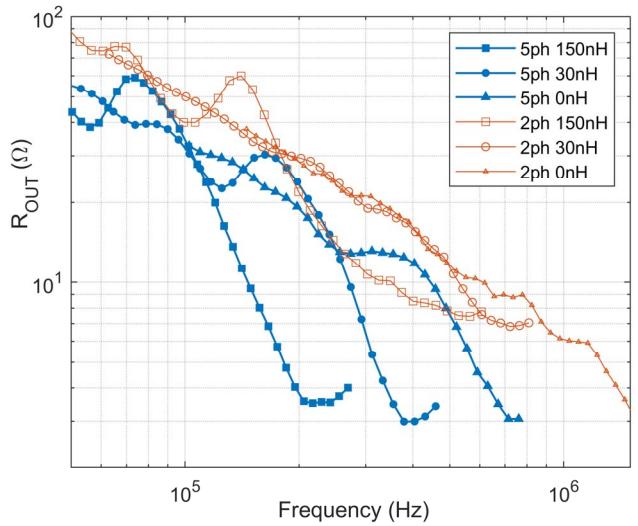


Fig. 13. Measured output impedance (R_{out}) for prototype using 0.8mm FR4 with 2oz copper.

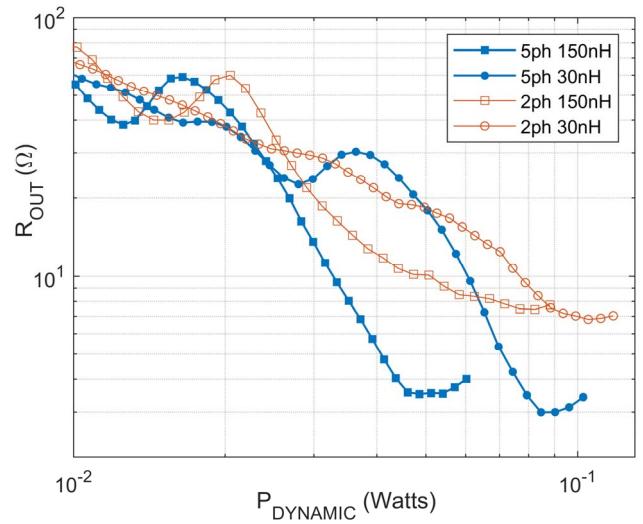


Fig. 14. Measured dynamic power consumption versus output impedance (R_{out}) for prototype using 0.8mm FR4 with 2oz copper.

across the entire load range. At a light load of 44 mA the 5-phase scheme sees 92.2% efficiency whereas the 2-phase scheme attains 82.4%.

Fig. 13 presents measured results of the FR4 converter’s output impedance as a function of switching frequency for several permutations of inductance and clocking scheme. The 5-phase schemes exhibit lowest output impedance with frequency due to near complete mitigation of transient inrush currents. It is worth noting that the 5-phase regime consumes $1.53\times$ more dynamic power in its gate drivers than the 2-phase scheme for the same switching frequency; therefore, it is helpful to plot output impedance versus dynamic power consumption, as in Fig. 14. Here we see that for a fixed dynamic power consumption and identical hardware, the 5-phase scheme yields a $\sim 65\%$ reduction in conduction losses at resonance when compared with the 2-phase scheme at the same dynamic power levels.

Measured efficiency curves for both PCB prototypes using the 30 nH trace inductors are plotted in Fig. 15 and offers a direct comparison between PCB substrate choices: while the 2oz copper of the FR4 revision offers a peak efficiency over 96% and increased output power before thermal failure, it's 6.3× larger board volume results in an overall decreased power density relative to the polyimide film version which achieves a peak efficiency of 94.9%. With the widespread adoption of CSP and BGA packaging, this directly incentivizes improved PCB fabrication techniques such that lower ohmic losses can be achieved on thinner board substrates.

The converters discussed herein are fixed ratio without voltage regulation and so experience a conversion ratio degradation with increased load that is a function of output impedance (R_{OUT}). Measured output power versus conversion ratio for four different input voltages for the 0.127 mm polyimide film version are plotted in Fig. 16. This implementation achieved a maximum measured output power of 30.56 W for $V_{IN}=8$ V before thermal protection inhibited operation. Up to 40.5 W was extracted when using a 12 V 0.5 A CPU fan for forced air cooling.

Solution volume was calculated by a best-fit cuboid encompassing both the power stage PCB and all components except the level shifting circuitry and HFS9003 clock generator (Table II). This resulted in a measured power density of 0.686 W/mm³ (11.2 kW/inch³) with no active cooling. While level shifting circuit volume was not included in these calculations, the volume estimate is still a reasonable projection given the recent release of commercial parts such as Peregrine Semiconductor's PE29102 which offers fully integrated level shifters alongside two isolated gate drivers in a 2 mm×1.6 mm flip-chip package. Coupled with bootstrapping techniques and a

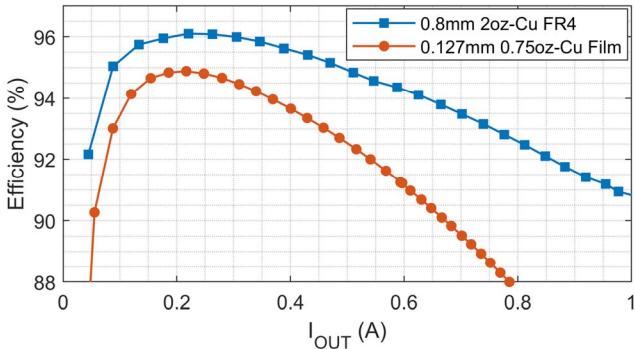


Fig. 15. Measured load current versus efficiency for 0.8mm FR4 prototype and 0.127mm polyimide film prototype with $V_{IN}=7$ V.

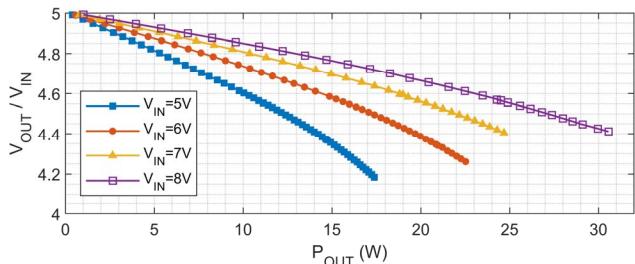


Fig. 16. Measured output power versus voltage conversion ratio for 0.127mm polyimide film prototype at four input voltages.

TABLE II. VOLUME BREAKDOWN OF 1:5 COCKCROFT-WALTON

Component	Volume (mm ³)
S1-S9	3.71
C1-C4, & C _{OUT}	7.17
Gate Drivers	5.4
Driver By-Pass Capacitors	0.14
Power Stage PCB	6.1
Power Stage Spacing	22
Supporting Motherboard & Level Shifters	6,375

dedicated timing microcontroller or ASIC, a commercial implementation near this density level is plausible.

V. CONCLUSION

High efficiency at high conversion ratios has been the motivation behind recent research into hybrid LC converter architectures. Commercial examples of the conventional boost topology can achieve high power densities but with limited voltage conversion ratio (e.g. the LTM8042 achieves 1,100W/inch³, but only with a 66% boost in output voltage and 90.8% efficiency). In this work, an N-phase switching regime allowing a 1:N Cockcroft-Walton converter to achieve complete ZCS using a single inductor has been demonstrated. Only one current sensing element is required at the input to enable the full ZCS scheme, potentially allowing for simpler design.

Experimental results were collected for two instances of a 1:5 CW converter using a PCB trace inductor for reduced size. Resonant operation was chosen to keep dynamic gate driver losses low and reduce switching losses, but this forsakes the ability to actively regulate the output and would require an increase in switching frequency or inductance to do so. The design objective was maximum power density using minimum size discrete components and silicon-based switches: as such, restrictions on device sizing were tolerated with the understanding that an ASIC implementation on an appropriate power process would likely yield improved performance.

Table III compares this work to other related SC converters. Both [11] and [12] leverage the reduced capacitor stress of the Cockcroft-Walton topology, but operate at lower switching frequencies with inductors >1000x larger than in this work. The increased inductance allows for near linear current ripple and subsequently the output voltage can be regulated. However, passive diode switching dictates the use of higher voltages for efficiency. Reference [9] demonstrates complete active switching at relatively high frequencies using GaN devices; this enables the use of a 100 nH inductor and dramatically increases power density, but its Dickson topology results in increased voltage stress on fly capacitors, increasing required volume. Active split-phase clocking adds to this approach's complexity and sensing requirements but eliminates diode forward voltage losses and allows for lower voltage applications.

Similarly, this work utilizes smaller passives to increase power density and adopts complete active switching to eliminate diode losses. While clocking complexity is similar to [9], no ZVS conditions must actively be sensed, and so hardware requirements and associated power draw is reduced, particularly at light load. Lower switching frequency and the distributed manner in which energy is admitted into the converter across N phases result in this switching technique achieving inherent

TABLE III. COMPARISON WITH EXISTING WORK

	[11] Young 2012	[12] Müller 2015	[9] Macy 2015	This Work
Conversion Ratio:	1-to-6 & Regulation	1-to-11 & Regulation	1-to-4 Fixed Ratio	1-to-5 Fixed Ratio
Topology:	Cockcroft-Walton	Cockcroft-Walton	Dickson	Cockcroft-Walton
Clocking Scheme:	2-Phase (Split-Phase)	2-Phase (Split-Phase)	Resonant 2-Phase (Split-Phase)	Resonant N-Phase
Switch Type:	Diode & MOSFET	Diode & MOSFET	GaN FET Only	MOSFET Only
# of sensors:	2 (1×Voltage, 1×Current)	3 (1×Voltage, 2×Current)	3 (2×Voltage, 1×Current)	1 (Current)
fsw:	60kHz	100kHz	1.2MHz	380kHz
Inductor:	1.5mH	100μH	100nH	30nH PCB-Trace
Peak Efficiency:	93%	95.8%	92%	95% @V_{IN}=8V
P _{OUT-MAX} :	200W	212W	263W	30.6W
V _{IN} @ P _{OUT-MAX} :	54V	25V	33V	8V
Eff. @ P _{OUT-MAX} :	91%	94.4%	<90%	87.5%
V _{OUT} @ P _{OUT-MAX} :	450V	-	117V @ 2.25A	34.83V
Power Density:	<17W/inch ³	6.85W/inch ³	1,011W/inch ³	11,248W/inch³

light-load efficiency. Future work will evaluate constraints on L and C values to prohibit reverse body diode turn-on in switches allowing for optimization and maximum energy density utilization.

VI. ACKNOWLEDGMENTS

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