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Electronic transport and quantum oscillations in thin bismuth crystals grown inside van der Waals materials

DISSERTATION

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ABSTRACT OF THE DISSERTATION

Exceptional electronic transport and quantum oscillations in thin bismuth crystals grown inside van der Waals materials

By

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Doctor of Philosophy in Physics

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Confining materials to two-dimensional forms changes the behavior of the electrons and enables the creation of new devices. In this thesis, I present a synthesis approach where thin crystals are grown in a nanoscale mold defined by atomically flat van der Waals (vdW) materials. By heating and compressing bismuth in a vdW mold made of hexagonal boron nitride (hBN), we grow high quality ultraflat bismuth crystals of various thicknesses. The vdW-molded bismuth shows exceptional electronic transport from the (111) surface states due to quantum confinement, enabling the observation of Shubnikov–de Haas quantum oscillations. The gate-dependent magnetoresistance is also presented, which provides evidence for multi-carrier quantum oscillations and Landau level splitting, with features originating from both the top and bottom surfaces. The vdW mold growth technique establishes a platform for electronic studies and control of bismuth's Rashba surface states and topological boundary modes. Beyond bismuth, the vdW-molding approach provides a low-cost way to synthesize ultrathin crystals and directly integrate them into a vdW heterostructure.

Chapter 1

Introduction

1.1 Thesis outline

This thesis starts with the introduction and background on various topics, that motivate the transport study of bismuth boundary states and inspires the development of new growth method for high quality thin crystals.

It is followed by Chapter 2, which describes in detail the vdW mold growth method that we developed, including various growth stage designs, sample preparation, growth process, discussions about implementing with other materials, and the improved techniques we developed based on the vdW mold growth method.

In Chapter 3, I present data from various structural characterizations on the bismuth crystals grown with this method, a model of the growth limits and molecular dynamics simulations.

Chapter 4 includes the description of the device design and fabrication from the vdW-molded bismuth crystals, and the discussion of the fabrication goals and challenges.

In the final chapter, I present the electronic transport data from the vdW-molded bismuth devices and the corresponding data analyses for their electronic properties.

1.2 Introduction and background

The boundary states of a crystal can behave drastically differently from its bulk. There can be many reasons leading to that, such as surface reconstruction from the dangling bonds, and the broken symmetry at the surfaces. The differences between boundary and bulk can lead to different potential applications, ranging from spintronics to quantum computing, motivating researchers to gain deeper understanding of various boundary states.

1.2.1 Bismuth structure and physics properties

Bismuth is a group V semimetal with a low melting point of 271 degrees Celsius. It has a large atomic number of 83, making it the element with the largest spin-orbit interactions among all non-radioactive materials. It has a rhombohedral crystal structure (space group R-3m), a layered buckled honeycomb structure perpendicular to its trigonal axis[1]. Within each buckled honeycomb layer (also called a “bilayer”), each atom covalently bonds to its three nearest neighbors with its outer shell electrons 6p3. What is holding each bilayer together is the van der Waals force, therefore the interlayer bonding strength is much smaller than the intralayer bonds. However, the interlayer bonding strength is not weak enough for bismuth to be exfoliable like the more common vdW materials graphite and hBN.

As a semimetal, the conduction band and valence band of bismuth both cross the Fermi level, resulting in a small carrier density of 1.41×10^{23} cm^{-3} in the bulk, with almost compensated electron and hole carriers. Due to its electronic structure, bulk bismuth exhibits a low effective mass of roughly 10^{-3} m_e, and a long Fermi wavelength of 10 to 50 nm, and a mobility that can be as high as 107 $cm^2V^{-1}s^{-1}$ [2–4]. de Haas-van Alphen effect and Shubnikov-de Haas oscillations were first observed in elemental bulk bismuth in 1930[5].

On top of its exceptional transport properties, what makes bismuth interesting in the quantum science aspect is its large spin-orbit coupling. The larger atomic mass creates a bigger nucleus electric field, causing a stronger relativistic effect in the carriers as they feel a stronger magnetic field in their reference frame, and therefore a strong spin-orbit coupling. Spin-orbit coupling can break the band structure's spin degeneracy, opening up band gaps, causing band inversions[6–13]. It is the core of topological properties in matter, and as a result, bismuth is intrinsic to many topological materials, such as bismuth telluride and bismuth selenide, both of which are well-studied prominent examples of topological insulators[14].

1.2.2 Bulk bismuth, thin bismuth and bismuth boundary states

Elemental bismuth bulk crystal is proposed to be a higher order topological insulator[15]. In a Z2 topological insulator[16], the band topology of which is protected by time reversal symmetry. In comparison, bismuth is protected by three-fold rotational symmetry on top of that. As a result of the additional symmetry, it is expected to exhibit helical states along the crystal hinges instead of topological surface states. In a helical state, the electron spin is locked with its momentum to be perpendicular to each other.

Due to its large spin-orbit coupling and the broken inversion symmetry at its surface, elemental bismuth holds metallic Rashba surface states[1,10,11]. The spin degeneracy is broken on the surfaces, leaving spin textures on the surface state pockets, which could be utilized for inducing spin currents and other potential spintronics applications[17,18].

2D bismuth in (111) orientation, which only consists of a single bilayer of the buckled honeycomb layer, is theoretically predicted to be a 2D topological insulator, also known as quantum spin Hall insulator[12,19–23]. Quantum spin Hall systems can be naively thought of as two quantum Hall systems with opposite magnetic fields and electron spins adding together. The magnetic field cancels out, and the system has two counter-propagating helical edge modes. The rest of the system remains insulating. The helical edge modes are protected by time reversal symmetry[24–26] and cannot be scattered and cause dissipation by non-magnetic impurities, because to scatter into the other counter-propagating mode, the carrier's spin has to be flipped, which breaks the time reversal symmetry. Helical edge modes of 2D TIs are ideal for transmitting quantum information with high fidelity. When placed next to a p-wave superconductor, due to proximity effect, the helical edge state turns into a topological superconductor, which holds non-Abelian Majorana zero mode on its two ends[27–29]. Majorana fermion is a charge neutral fermionic quasiparticle which is its own antiparticle. It obeys non-abelian statistics when exchanged location (in a more common term: braiding) with another Majorana fermion, therefore is a strong candidate for realizing quantum computing gate operations[30].

These potential applications draw a lot of interest in realizing 2D TIs. So far, there have been numerous materials that have been experimentally probed to be 2D TIs, such as HgTe quantum wells, InAs-based heterostructures, 1T' WTe_2, monolayer Bi_4Br_4, germanene [31–36]. However, these already probed 2D TI systems are only measurable under cryogenic temperatures, due to

the size of their band gaps. What makes 2D bismuth (111) a desirable material, is that it is predicted to have a 0.6 eV band gap, making it a 2D TI that is robust at room temperature[19,37]. This could greatly reduce the complication and energy consumption for the applications. According to theoretical calculations, Bi (111) remains a 2D TI up until 4 bilayers (1.6 nm thick when standalone), when the indirect bandgap of the surface states are still positive[19]. This lifts the restrictions in growth to some degree, as it is not necessary to strictly grow single bilayer Bi (111) to observe such an effect.

Moreover, 2D bismuth (110) in black phosphorous-like structure is theoretically predicted and experimentally probed to be a 2D TI[38,39] and a 2D Weyl semimetal[40]. This would offer a playground for studying a plethora of unconventional quantum properties[41–44].

1.2.3 Bismuth boundary states spectroscopy and transport studies

There have been numerous attempts in studying the boundary states of bismuth through spectroscopic probes and electronic transport experiments. Most are done through STM and ARPES, and they demonstrated the existence of the spin-split Rashba surface states and helical edge states. The conductive hinge states along the bisectrix axis were observed as expected in STM differential conductance maps[15,45]. The surface Landau levels and spin states were also studied by STM, where the exchange-induced nematicity in the Landau level were discovere[46,47]. Spin-resolved ARPES measurements confirms the Rashba metallic surface states of bulk bismuth (111)[48–50]. The metal-insulator transition of bismuth thin films and nontrivial topology was also reported by ARPES studies[51,52]. While these above studies were mostly on bismuth

(111) surface states, bismuth (110) surface states were also probed by ARPES studies to exhibit evidence for 2D weyl semimetal[40].

There have been many attempts in studying the transport behavior in bismuth boundary states, however, there is still limited transport studies on the electronic structure of the Rashba surface states and helical hinge states. The existence of the surface states was observed in several transport studies of bismuth thin films, through the co-existence of the metallic surface states and semiconducting bulk states[53], and the AB and AAS oscillations in bismuth nanowires[54]. The thickness dependence of the transport properties was also reported[53,55,56], along with the magnetoresistance studies including the analysis of weak antilocalization[55,57]. Jiang et al was able to observe dynamic nuclear spin polarization by inducing hyperfine interactions in bismuth surface nucleus via the spin currents generated in the Rashba surface states[18]. Apart from surface state transport studies, evidence for the hinge state transport was observed in Josephson-interference measurements from loops formed by single crystal bismuth nanowires[15].

Considering bismuth surface is a good 2D metal, certain transport properties should be expected to show up, especially quantum oscillations or quantum Hall effect in magneto transport when the surface band pockets are quantized into Landau levels under out-of-plane magnetic field. However, apart from the quantum oscillations from the bulk crystal[58–60] and AB and AAS oscillations from the surface state transport interference in bismuth nanowires[54], no other oscillations, especially quantum oscillations from the surface states were reported in previous bismuth transport studies. In bulk bismuth transport, this could be due to that the surface transport features are overshadowed by the bulk transport, since the bulk volume is high in this case. In bismuth thin film transport, where the bulk semimetallic or semiconducting contribution should be reduced, the fact that no surface state quantum oscillations were observed indicates

that the carriers' mean free path is smaller than the quantum coherence length, and that the scattering events are quite frequent within the surfaces of the bismuth thin film samples. This is contrary to the advantage of bismuth bulk transport, that the carriers have an extraordinary long mean free path which reaches millimeter scale at cryogenic temperatures[1], because high quality bismuth bulk crystal is easy to grow. The source of the scattering events could be the impurity/defects in the grown thin film samples, the domain walls formed due to the lattice mismatch between the growth substrate, and the uneven surfaces. I will give a summary of the existing methods in growing nanoscale bismuth below.

1.2.4 Existing methods in growing thin bismuth

The most common way to grow bismuth thin films is through deposition, and more specifically, molecular beam epitaxy (MBE), through which higher quality ultrathin film could be achieved. One of the most common growth substrates is the Si(111)-7 x 7 substrate (a silicon surface with a specific atomic arrangement known as the "7 x 7 reconstruction", where the repeating unit on the surface is 7 times larger in both directions compared to the underlying bulk lattice). This will give a substantial 18% lattice mismatch with bismuth (111) triangular lattice structure[61]. Other substrates include BaF_2, SiC(0001), Mica, Bi_2Te_3 (111), Ge (111), SnS(Se) and more[40,62–67]. Take Si(111)-7 x 7 substrate as an example, upon growth, a disordered bismuth wetting layer would form to accommodate the large lattice mismatch, on which black-phosphorous-like bismuth (110) islands would grow up to 4 monolayers, before transforming into rhombohedral bismuth (111) structured thin films[61]. Other substrates will have different process, for example, bismuth will grow as rhombohedral (111) structure from the start on Bi_2Te_3 substrate[66]. As the film

thickness increases, the bismuth films always tend to stabilize into a (111) orientation, as the cohesive energy of the Bi (111) becomes larger than the Bi (110) when the film thickness exceeds 4 monolayers of black phosphorous-like Bi (110)[62].

Other growth methods include solvothermal methods, where bismuth nanoribbons are grown. The reported thicknesses are on the scale of tens of nanometers[60]. For bismuth nanowires, methods combining deposition and nanofabrication are used[68,69]. Considering bismuth is a van der Waals material, there have been attempts to exfoliate bismuth thin films from the bulk crystal, however, the interlayer bonding force is too strong for it to be exfoliated similar to graphene and many other van der Waals materials. Cleaving along the (111) crystal plane is relatively easy, and that facilitates the scanning probe study of the boundary states of bulk bismuth.

1.2.5 Challenges in growing thin bismuth with conventional methods

These growth methods were able to produce bismuth thin films of various thicknesses. While many STM, ARPES studies on the electronic structure of bismuth thin films were based on the deposited samples, the transport studies from them were still yet to produce evidence of clean surface state transport across a micrometer-scale region, which poses a higher requirement on crystal quality.

Upon deposition growth, bismuth forms small islands, before joining together into (111)-oriented film. The crystal orientation from each island can be different, therefore when they join, domain walls will form between them. The domain wall is one of the potential unwanted scattering sources in deposited bismuth thin films. Therefore, a common procedure after deposition is

annealing the film for one or more hours. This would greatly increase the quality of the grown bismuth thin films, by reducing the number of domains to even achieve single-crystal films within a large distance[58], and by flattening the surface and increasing the size of the surface terraces to sub-micrometer scale[70,71]. The uneven surface is another source of unwanted scattering, but it should provide less resistive scattering to transverse transport when the crystal orientation is preserved across the terrace.

Apart from these potential scattering sources, bismuth's band structure can be altered by the stress induced by lattice mismatch with the substrate. When bismuth is immiscible to the substrate, the substrate interaction can alter its crystal structure and band structure as well. For example, the single bilayer Bi (111) grown on SiC substrate is no longer a buckled honeycomb structure. Instead, it becomes a flat honeycomb structure similar to graphene, which enlarges its band gap[64]. Bi (111) single bilayer grown on Bi2Te3 also shows a slightly altered band structure[66]. On top of that, the Dirac cone from the Bi2Te3 surface remains unaffected, therefore will provide parallel conductance in electronic transport[66]. Other conductive substrates have the same disadvantage when it comes to transport studies.

Bismuth forms a self-limiting insulating oxide layer of 1~2 nm[72] when exposed to air, similar to aluminum and indium. Theoretical calculations suggest that the formation of the oxide layer does not affect the metallic Rashba surface states[73], however, the oxidation can cause the actual thickness of the bismuth thin film to change, or even disappear if it is thin enough. Therefore, some researchers choose to add termination layer on top of the bismuth thin films when there is a need to take them out of the growth chamber for additional characterizations[74], and that would induce the risk of altering the surface state properties, considering it is not protected by topology.

1.2.6 Mechanical methods for thin crystal growth

Considering the previous transport studies of bismuth thin films grown by conventional methods gave limited information about the electronic structure, it is worth considering alternative methods for growing low-dimensional materials.

Here are some of the existing methods for growing nanowires or thin films involving pressurizing or spatial confinement. Pressurizing molten or solid phase materials at an elevated temperature into nanowire mold arrays have seen success in producing crystalline nanowires of various elemental metals or alloys[75–77]. Stacking sheets of target material with other soft metals like Al/Ag, then by repeated folding then compressing, or by applying pressure via rolling, people have been able to reduce the thickness of the material and obtain thin films after dissolving the spacing layer materials [ref]. A more straightforward way to apply pressure is to squeeze the target material, in this case bismuth, between two flat surfaces and apply heat below its melting point at the same time[78]. Bismuth is softened by the elevated temperature and is compressed into ultrathin films. Similarly, black phosphorus thin film was grown on sapphire substrate by being compressed in a heated pressure cell under a layer of hBN[79]. The addition of hBN helps in achieving an atomically flat surface. Another class of material that garnered a lot of interest in its thin film synthesis is metal halide perovskites. Different from metals, it is usually grown from a solution form. By confining its growth direction and applying optional out-of-plane pressure, perovskite films are grown from the solution with controllable thicknesses[80].

These alternative growth methods involving space confinement and mechanical compressing gave us inspiration in developing a new method in growing higher quality ultrathin bismuth films.

1.2.7 van der Waals materials and hBN

Van der Waals (vdW) materials are a unique class of materials composed of layers held together by weak van der Waals forces, allowing them to be easily exfoliated into atomically thin sheets. These materials exhibit fascinating properties due to their reduced dimensionality and tunable electronic and optical characteristics. The discovery of graphene in 2004 sparked widespread interest in vdW materials, leading to the exploration of other layered compounds such as transition metal dichalcogenides (TMDs) and hexagonal boron nitride (hBN)[81–83].

Apart from the exciting application possibilities enabled by tailoring the electronic and optical characteristics of various vdW materials, this work only focuses on their most basic structural property – the exfoliable layered structure. The original and the most widespread utility of graphite is to be used as a lubricant, because the friction between each layer of graphite is extremely small, so that it can be easily smeared[84]. The low interlayer friction is a result of not only the weak interlayer van der Waals bonding force, but also the flatness of each layer. Each of the layers is atomically flat, which is what allows the easy gliding between the layers, and that also makes it very easy to achieve atomically flat surfaces through exfoliation.

The specific van der Waals materials that is used in this work is hBN. It is composed of boron and nitrogen atoms arranged in a flat hexagonal lattice similar to graphite. Contrary to graphite, hBN is a band insulator with a 6 eV band gap, therefore it is able to provide high electrical insulation and is an important material for optoelectronics and other nanomaterial technologies[83]. It has excellent chemical stability, which makes it suitable for interfacing target materials while preserving their chemical properties.

Chapter 2

vdW mold growth method

2.1 Motivation and overview of the vdW mold growth method

In deposition method, bismuth thin films grow from the bottom, and the whole film gain thickness simultaneously. For bismuth, it relies on post-growth annealing to improve the crystallinity and surface smoothness. While in the space confined growth method, the thin films or nanowires grow from the edge, and their crystallinity is largely affected by the space confinement geometry. The traditional space confined growth method is the cast molding method, where the target material is melted into liquid form and poured into a mold, before solidifying into the shape of the mold. The result reflects the shape and the surface of the mold. It is widely used in the manufacturing industry for producing macro scale products. It is therefore tempting to apply this idea to nanoscale materials by creating nanoscale molds.

In order to achieve improved surface geometry and large domain size compared to bismuth thin films grown through deposition, the mold surface should be as smooth as possible. This is where the extreme flatness of vdW materials becomes useful. Exfoliation and nanofabrication techniques can produce nanoscale molds using vdW materials with ease and flexibility. For the subsequent transport characterizations, hBN is a better choice than graphite since it is a large bandgap insulator.

Bismuth in its liquid form has a high surface tension[85]. Without any external pressure, on a surface that it does not wet like hBN, liquid bismuth tends to ball up. In this case, to obtain thin films from liquid phase bismuth, compressing pressure needs to be applied by the mold. Choosing other vdW materials that liquid bismuth wets can reduce the requirement on pressure and eventually produce thinner result, but that comes with a cost of stronger interaction between bismuth and the mold material. For the purpose of studying the intrinsic boundary state of bismuth, hBN is the better choice as it provides almost no influence on bismuth surface band structure due to the big difference in lattice constants.

These requirements can be fulfilled by an easy-to-make experimental setup. The mold can be made of two pieces of exfoliated hBN crystals, and for simplicity, the seed bismuth crystal can be placed between them before the actual melt-grow process. The out-of-plane pressure can be realized by placing the hBN/bismuth/hBN stack on a rigid flat surface such as SiO_2/Si wafer chip, and compressing it with another rigid flat surface. We name this growth method vdW-molding.

Since bismuth has a low melting point of 271°C, a simple heating stage with a power of tens of watts would be enough to heat up the system to melt the seed bismuth crystal.

2.2 Growth setup designs

Implementing such an idea has a bit more complications than it suggests. The major challenges and requirements are listed below:

1. The top and bottom compressing surfaces need to be parallel with each other.
2. During heating, there will be lateral displacement between the top and bottom compressing surfaces that causes unwanted tearing motion between the two hBN crystals.
3. The ability of monitoring the growth process in real time can enable pressure adjustment, and can be greatly beneficial for holistic understanding and improvement of the growth process.
4. The whole growth setup should be stable and be isolated from external vibrations.
5. The growth setup should ideally make the growth process fast and easy to repeat.

I built a total of 3 versions of the growth setups in total, each version is designed aiming to solve the previous version's biggest issue. The previous 2 versions all have their own drawbacks that prevent them from meeting all the above requirements. Below are brief descriptions for each of the versions.

2.2.1 vdW-molding stage design v1

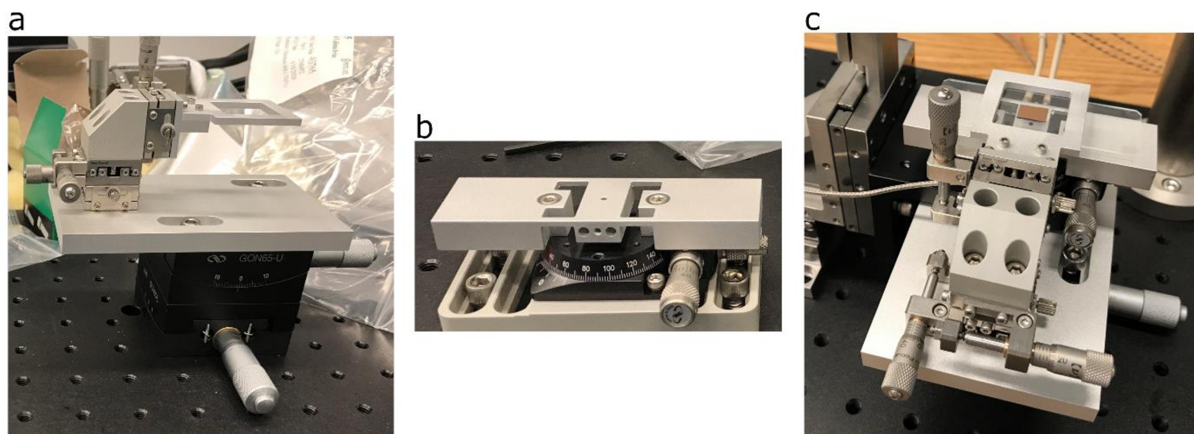

Figure 2.2.1 vdW-molding stage design v1. a, the pressing arm. b, the heating stage. c, the whole stage after being put together.

vdW-molding stage design v1 has two major components, the pressing arm (Figure 2.2.1a) and the heating stage (Figure 2.2.1b). The pressing arm consists of two goniometers, an XYZ translation stage and a glass slide holder. The top squeezing substrate while using this setup is a glass slide. When a piece of glass slide is mounted, the rotation center of the two goniometers is at the middle of the square-shaped opening of the glass slide holder, on the bottom surface of the glass slide. The heating stage is made of a block of aluminum, of which the middle part is isolated from the two larger pieces of aluminum on the side, only connected with four thin arms. The purpose of this design is to isolate the heat in the middle part, dissipate the heat to the air through the large side pieces, reduce the heat flow to the parts holding the stage and therefore reduce the thermal drift of the stage. There are two insertion heaters and a thermocouple attached to the stage, all of which are connected to a PID temperature controller to regulate the stage heating. The stage is bolted down to a rotation stage, which is secured on an L bracket secured on an XYZ translation stage. There is a microscope connected to a camera on top of the whole setup for real time display of the vdW-molding process.

The ideal vdW-molding procedure on this setup is: 1. A sample chip with the hBN/Bi/hBN stack is placed on the heating stage and secured with the vacuum hole. 2. Heat up the sample stage to 150°C to soften the bismuth and reduce the thermal drift later. 3. Lift up the sample stage closer to the top glass slide until an interference pattern appears between them. 4. Adjust the goniometers to widen the interference pattern until the stripes disappear. 5. Further lift the heating stage until the sample chip engages with the glass slide. 6. Heat up the sample further to melt the bismuth, then turn off the heater to let the whole setup cool down naturally to room temperature.

As an initial test design, no actual thermodynamics simulation was performed to support the design purpose of isolating the high temperature middle stage, and as a result, when the middle stage is heated up, the temperature of the two side pieces increases quickly too. When they reach an equilibrium in temperature, there is a minimal temperature difference between the center stage and the side stage. The rotation stage and the L bracket under the heating stage also experience a substantial increase in temperature, resulting in obvious lateral thermal drift on the order of a few microns in the position of the sample, and that can shear the hBN/Bi/hBN sample stack apart when we apply a large pressure.

Another discrepancy between reality and expectation is that a regular 1 cm x 1 cm sample chip is too big for us to align the top and bottom squeezing surfaces by tuning the interference pattern through the microscope field of view. Usually, one corner of the SiO2/Si chip gets much closer to the top substrate than the others, and the interference pattern only appears in its close vicinity. The chip is much larger than the area viewable through the microscope objectives, so to locate the interference pattern, the microscope needs to be moved around to show the corners of the chip. This is a lengthy process for the XYZ translation stage attached to the microscope, and it is

very common that after adjusting the goniometers, another corner becomes the closest and the same procedure needs to be repeated. The solution is to reduce the size of the chip's top surface so that it can fit within the microscope's view, for example, using Dremel to grind away the chip surface except for the region surrounding the sample stack, or using KOH solution with polymethyl methacrylate (PMMA) mask to dissolve the chip surface around the sample region.

This vdW-molding stage not only requires an hour on average to mold each sample stack, but also quite frequently induce lateral displacement between the top and bottom hBN, sometimes even shear and smear the hBN, destroying the stack. Therefore, the goal of the next stage design is to eliminate the thermal displacement between the top and bottom substrate.

2.2.2 vdW-molding stage design v2

vdW-molding stage design v2 took inspiration from diamond anvil cell (DAC), a device to apply extreme pressure to the sample inside, which consists of a top and a bottom diamond seat connected by three screws, that apply pressure and provide parallel alignment to the diamond anvils held between the seats. The sample is placed between the diamond anvils within a pressure medium, secured by a metal gasket. Diamonds, pressure medium and metal gasket are not needed for the vdW-molding process, because it does not require extreme pressure condition. The pictures of the vdW-molding stage design v2 is shown below.

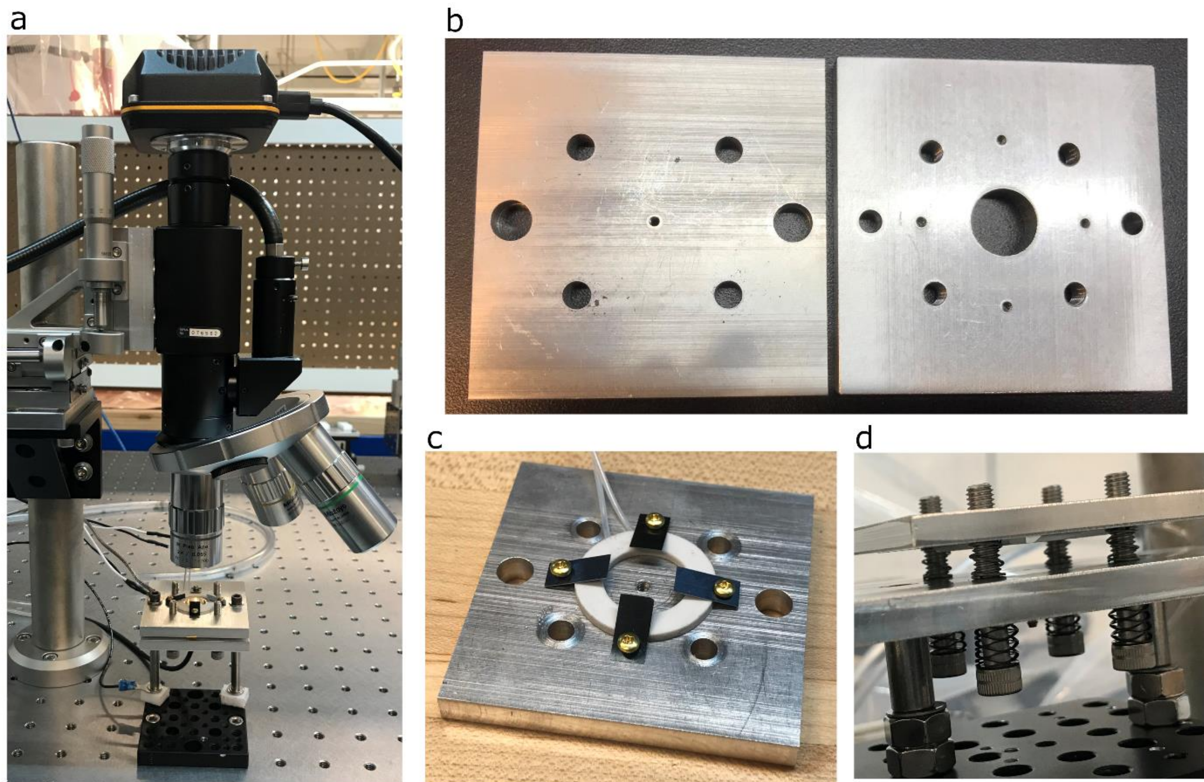

Figure 2.2.2 vdW-molding stage design v2. a, the whole vdW-molding stage in use. b, the top and bottom plate. c, the bottom plate with a ring heater attached. d, springs and spring washers for sample protection and tilt angle fine tuning.

This design consists of a top plate and a bottom plate that holds the transparent top squeezing substrate and the bismuth sample chip, respectively (Figure 2.2.2). They are held together by a set of four screws, which are used to align the top and bottom substrates to be parallel, and to apply pressure. The screw holes on the top plate are threaded, and the screws go from the bottom through the bottom plate into the top plate. The whole structure is hung from the top plate. To prevent the top and bottom squeezing surfaces from collapsing together under gravity and accidentally crashing the sample before the actual vdW-molding growth, I put springs around the screws between the top and the bottom plates. A small turn on the screws results in a relatively large displacement of the bottom plane on the z axis compared to the size of the sample stack. To

scale this displacement smaller, I put spring washers around the screws between the bottom plate and the screw heads. Ring heaters are secured around the center on the top plate and the bottom plate to ensure symmetric heating. The sample chip is held down by a vacuum opening on the bottom plate.

The advantage of this version is the overall symmetric design, and the fact that the top and bottom plates are held together. As a result, the lateral displacement between the top and bottom substrates is negligible throughout the vdW-molding growth process. The whole growth setup is simple and inexpensive to make.

The disadvantages are plenty. vdW-molding one sample with this stage involves a lot of turning screws, as the parallel adjustment and pressure application are both done with the screws. This results in every molding process taking over one hour. Since the top and bottom substrate parallel alignment is still done through the interference pattern, we still need to prepare the sample chip with recessed edge area. The mistake of choosing a four-screw design for better symmetry instead of three screws makes this process more complex. A plane is defined by three points -- in this case three screws, therefore the addition of the fourth screw adds uneven strain on the threads of every screw. Inappropriate adjustment of the screws can easily strip the threads. The high temperature causes the spring washers to degrade over repeated use.

After experimenting with vdW-molding stage design v1 and v2, we gain better understanding of the necessary stage functionalities to perform vdW-molding. For substrate parallel alignment, the interference pattern method takes a long time, and preparing the shape of the sample chip adds to the total effort. For reducing thermal drift, it either requires lots of modifications to the structure of the transfer arm-heating stage design, or keeping the DAC-inspired symmetric design while improving the ease of tilt angle and pressure adjustment.

However, after discussing with my PI and teammates on this project, we come up with new solutions to simplify the top and bottom substrate alignment and pressure application process and solve the thermal drift problem at the same time. A diagram describing the schematics is shown below[86].

2.2.3 vdW-molding stage design v3

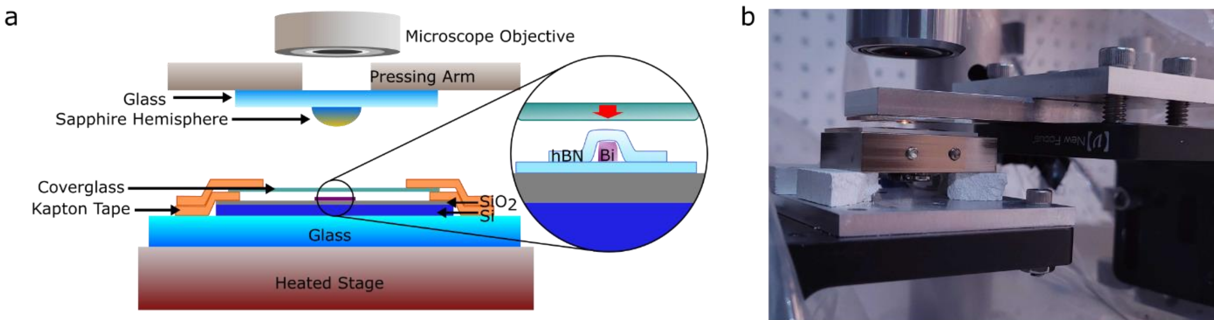

Figure 2.2.3 vdW-molding stage design v3. a, schematics of the whole setup. b, picture of the actual setup.

The solution to aligning the squeezing substrates is to use a hemisphere as the top substrate. We use a sapphire hemisphere of 1 mm diameter that can apply pressure in a ~500 μm^2 region. Compared to the size of the sample stack, the curvature of the hemisphere is negligible and will be counteracted by substrate deformation around the stack. The sapphire hemisphere is secured face-down on a glass slide mounted to an XYZ translation stage. By aligning the center of the sapphire hemisphere with the sample stack and lowering it to press onto the sample structure, only the bottom of the hemisphere will be in touch with the sample structure and there is no need for substrate tilt adjustment. The pressure is therefore localized and only a small amount of force is in need to be applied by the pressing arm.

The solution to avoiding thermal drift is to place an additional flexible top substrate on top of the sample, fixed on the sample chip. We use either a glass or a sapphire coverslip with thickness ranging from 0.19 to 0.23 mm as the flexible piece, and secure it on the sample's SiO_2/Si chip with 2.5 mils thick Kapton tape to prevent lateral motion with respect to the chip. With this design, the glass or sapphire coverslip is prevented from touching the chip by the Kapton tape spacers when no pressure is applied. When pressure is applied, the sapphire hemisphere will bend the coverslip and the pressure is conducted via the coverslip bottom surface to the sample. When the stage is heated and with the pressure applied, the temperature in the pressing arm will increase majorly through the contacted sapphire hemisphere, and the lateral position of the hemisphere will shift due to thermal expansion. In this situation, the sample stack is protected from the shifting top substrate by the protection of the coverslip since it is fixed to the sample chip. The lateral displacement will only happen at the interface between the hemisphere and the coverslip. To further reduce the risk of shearing, we can pre-heat the stage to a moderate temperature (I choose 150°C in the case of bismuth). Unlike normal 2D materials transfer process, the sample chip is not fixed on the heating stage with vacuum because it is not needed, and it would require high temperature resistance material for the vacuum tube attached.

Other aspects of the setup remain the same to the previous designs. This includes the camera and the microscope on top of the setup, which is able to image and record the real-time vdW-molding process through the transfer arm glass slide, the sapphire hemisphere and the coverslip. The whole setup is mounted on an optical breadboard, sitting on top of a vibration stage (RS Kinetic Systems VibraPlane BenchMate 2212), which isolates the setup from external vibrations.

The vdW-molding process with the version 3 stage as a result is much simpler and faster. The steps are as follows: 1. Place the sample on the stage and center it on the microscope with the

lowest magnification. 2. Move the sapphire hemisphere so that its center aligns with the sample. 3. Change to a bigger magnification in the microscope, lower the hemisphere and tune the height of the microscope at the same time, until an image of the sample is in focus through the microscope camera. 4. Raise the stage temperature for pre-heating. 5. Lower the pressing arm until the sample is squeezed, and the color of the chip region next to the sample stack turns slightly gray. 6. Keep raising the sample temperature to above its melting point. 7. Turn off the stage heater and let the sample cool down. 8. Lift up the pressing arm to release pressure. The whole process usually takes around half an hour to complete.

2.2.4 Home-made glove bags

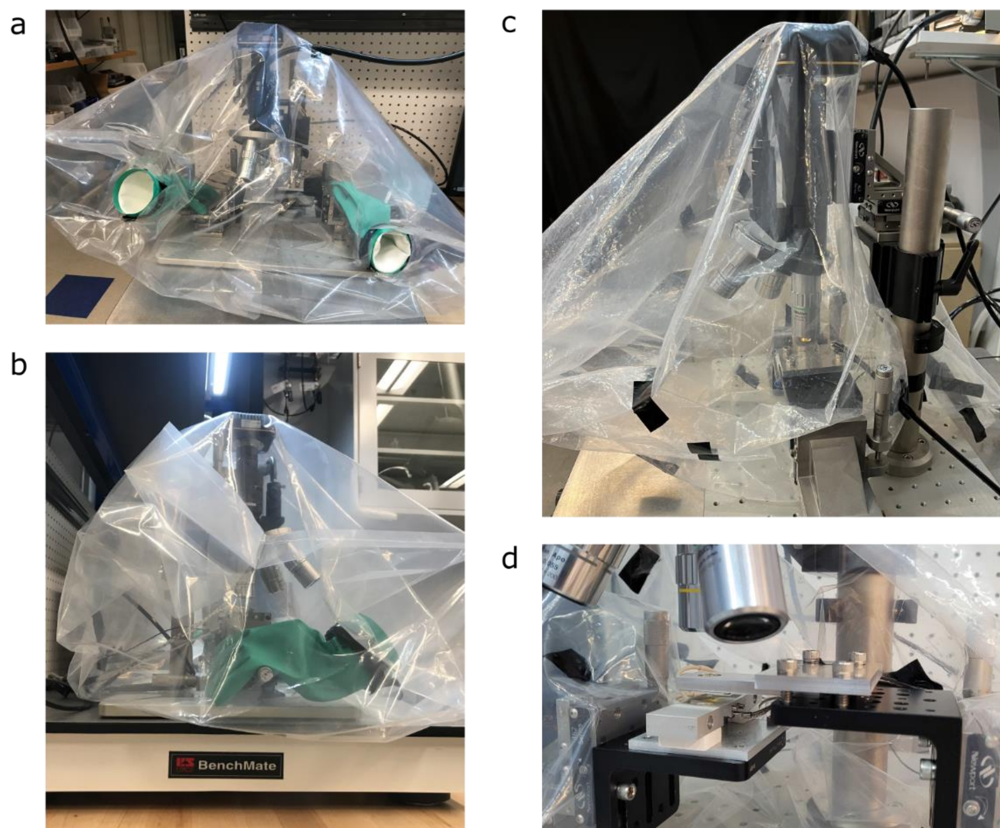

Figure 2.2.4 Pictures of the home-made glove bags. a, front view of the first glove bag. b, side view of the first glove bag. c, side view of the second glove bag. d, inner view of the second glove bag.

Since some of our bismuth samples are not fully encapsulated in hBN, therefore prone to oxidation especially in the melt phase, I added a home-made glove bag enclosing the vdW-molding setup to provide a more inert environment. The glove bags are made of thick plastic bags, and a tube connected to a nitrogen cylinder is inserted to the bags.

The first glove bag (Figure 2.2.4a&b) encloses everything on top of the optical breadboard. A pair of nitrile gloves are attached to the bag and are sealed on the rims using tapes. All the tubes and wires exit the bag from the back and these bag openings are sealed with tapes too. For every

vdW-molding experiment, after placing the sample inside, we seal the bag with tapes, then try to deflate the bag to some extent and flow N_2 for a few minutes to increase the N_2 concentration.

The second bag (Figure 2.2.4c&d) only encloses the vdW-molding region and the microscope. This is because when using the first bag, to modify the applied pressure on the pressing arm, we have to wear the gloves in order to reach inside the bag. This will inevitably tug on the bag and introduce vibrations to the setup. With the second bag, all the micrometer knobs are outside the bag, so the bag and the setup remains unperturbed throughout the vdW-molding process. To seal this bag after placing the sample inside, we fold the opening and clip the folded region.

2.3 Sample stack preparation

The preparation of an hBN/Bi/hBN stack involves material preparation and stacking.

Preparation of hBN: hBN crystals grown by our collaborators are exfoliated using tapes (Ultron Systems' Silicone-Free Adhesive Plastic Films). With a small piece of hBN bulk crystal on a piece of tape, I fold and unfold it a few times to spread the material out, and stick the tape to other pieces of tapes to further reduce the thickness of the crystals and to save for future use. I further fold and unfold the tape to spread the hBN crystals to empty regions of the tape, while avoid the already-used regions on the tape. Then, I prepare freshly diced SiO_2/Si chips, and gently press the tape onto them and avoid creating bubbles. hBN crystals already separated by the tape with the clean surfaces exposed, will be exfoliated again by the clean SiO_2 surface due to the van der Waals force. To improve the adhesion between the hBN crystals and the SiO_2 surface, I place the chips with the tape on an 80°C hot plate for 1 min. After that, I peel off the tape, leaving hBN crystals with clean top and bottom surfaces transferred on to the chip. Because

the tape was heated, there is always a substantial amount of tape residue left on the chip. I then anneal the exfoliated chips in a vacuum tube furnace at 350°C for half an hour or more to remove the tape residue and flatten the hBN crystals.

Preparation of seed bismuth crystals: First, a bismuth powder solution is made by adding bismuth powders (Sigma-Aldrich, ~100 mesh, ≥99.99%, 140-μm-diameter) in isopropyl alcohol or ethanol. After shaking the solution, a few drops are drop-casted on a clean Si/SiO_2 chip and let dry. The chip is then covered by another Si/SiO_2 chip, and the stacked chips are heated to 204 °C while being compressed in a hydraulic press to a pressure of ~6 MPa. The elevated temperature is intended to make bismuth softer while being pressed. During the pressing process, the bismuth powders are compressed to pancake forms, and the majority of the bismuth inside the powder is squeezed out of the original oxide shell. The resulting hydraulically pressed bismuth flakes are typically around 300 nm to 400 nm thick and are used as the starting material in the hBN/Bi/hBN stacks.

Figure 2.3.1 An example of flattened bismuth powder after being heated and compressed in a hydraulic press.

Stacking the hBN/Bi/hBN stack: From the exfoliated and annealed hBN exfoliation chips, hBN crystals with clean and large surfaces between 10 to 100 nm thick are selected. They are then picked up using separate polycarbonate (PC) stamps. Similarly, small pieces of flat bismuth crystals on the hydraulic-pressed bismuth chips can be picked up by PC stamps as well. These tend to be one or a few adjacent single crystal domains of bismuth formed while being heated and compressed in the hydraulic press.

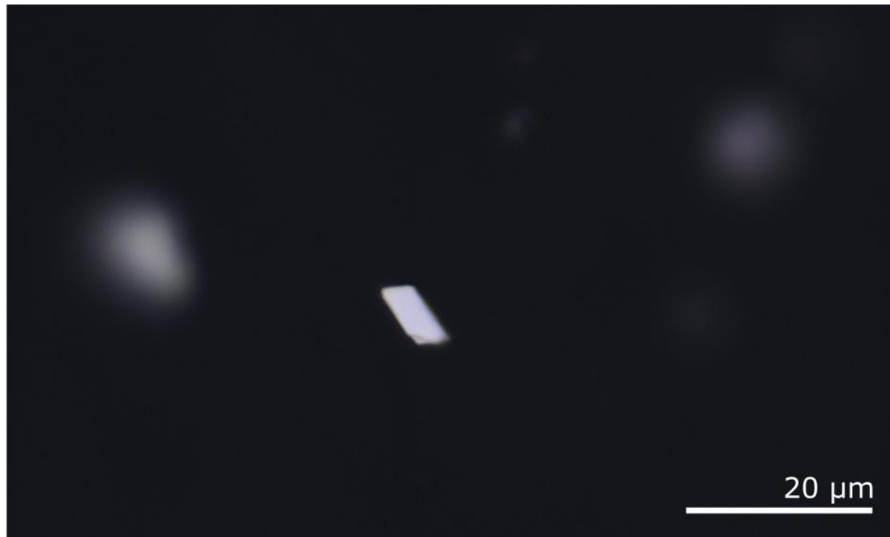

Figure 2.3.2 Optical microscope image of small bismuth crystals picked up on a PC stamp.

With these crystals picked up by separate PC stamps, we then transfer the crystals onto SiO_2/Si chips following the hBN-Bi-hBN stacking sequence. The sample stack is then complete. Because the stack is made in three separate transfer steps, a finite amount of organic residue is encapsulated between the top and bottom hBN as well. Annealing the bottom hBN before transferring the bismuth on top, and transferring the top hBN in a N_2 or Ar environment can help significantly reduce the amount of trapped organic residue.

The fabrication of PC stamps is as follows: PC films are prepared by drying a thin smooth layer of 10% PC in chloroform solution on glass slides in a fume hood. The PC films are then cut and mounted onto mm-size polydimethylsiloxane (PDMS) rectangular pieces using double-sided tapes on the side. The soft PC film surface can then be used to pick up and release micrometer-scale thin and flat crystals.

The process of PC pick up that was used in the project is as follows: 1. Lower the PC stamp to be in contact with the target crystal. 2. Raise the temperature to 120°C, so that the PC softens and

conforms better to the target crystal. 3. Cool down to room temperature, so that PC returns to the original rigidness. 4. Slowly peel off the PC stamp. The process of PC transfer is similar, with the main differences to be that the temperature needs to be raised to above 160°C, and at that temperature lift up the PDMS, leaving the PC with the crystal on the chip, before cooling down to room temperature.

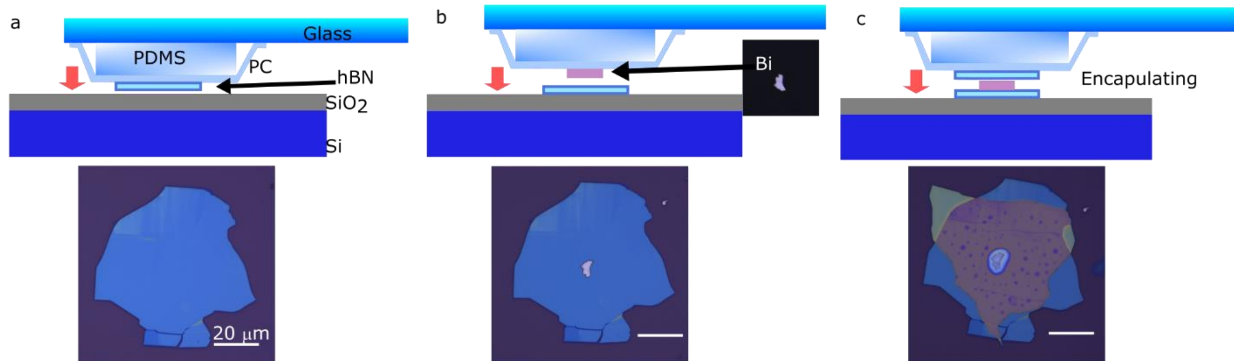

Figure 2.3.3 Diagram and optical sample image of each step to make an hBN/Bi/hBN stack. a, transfer of bottom hBN flake onto substrate, b, transfer of starting bismuth flake on the bottom hBN, c, encapsulating bismuth with top hBN flake.

2.4 The vdW-molding process

The schematics and optical image of the three stages of the vdW-molding process is shown below in Figure 2.4.1.

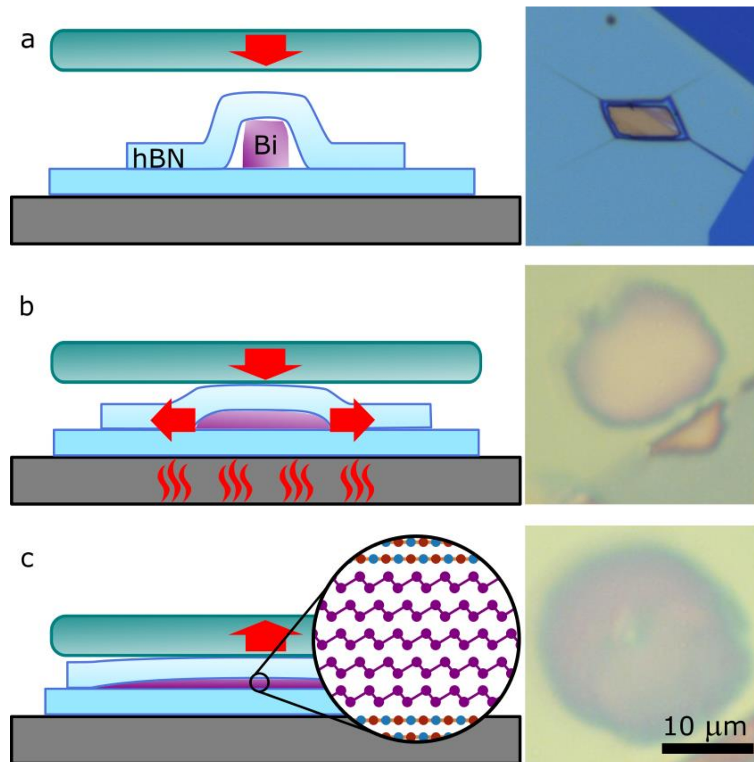

Figure 2.4.1 Growth of ultrathin bismuth crystals inside a vdW mold. a–c, Cross-sectional schematics of the vdW-mold process with corresponding optical images of the bismuth. a, Bismuth flake encapsulated in hBN on a bottom substrate of Si/SiO2 before squeezing. b, Uniaxial compression (vertical red arrow) is applied to the stack by a rigid top substrate (glass or sapphire) while the stage is heated. When the bismuth reaches its melting point, it rapidly compresses and expands laterally. c, Bismuth is cooled below its melting point and then pressure is removed, resulting in an ultrathin bismuth crystal. The inset shows the atomic structure.

First, a flake of bismuth is encapsulated in thin hBN layers using the PC stamp transfer methods described in the previous section. Next, the hBN/Bi/hBN stack is compressed between two substrates and then sequentially heated and cooled to melt and resolidify the bismuth (Figure 2.4.1b). On melting, the bismuth rapidly spreads between the hBN layers and decreases in thickness due to the applied pressure. The squeezed form is retained when it is cooled into the

solid phase and the pressure is released, resulting in a thin bismuth crystal encapsulated in hBN (Figure 2.4.1c).

2.5 Compatibility with other growth materials

The vdW-molding method in principle can be applied to many other materials. Since hBN is chemically inactive, the major limitation of this technique is the degradation temperature of the components in the growth setup, like the Kapton tape spacers and the microscope objectives. If these components can be replaced with high temperature resistant materials or be distanced away from the high temperature region, the real limitation would be the degradation temperature of hBN.

hBN can also be substituted by other vdW materials, such as Mica or transition metal dichalcogenides, which opens pathways to more interfaces and interactions.

The most applicable candidate material would be tin, indium, tellurium, and selenium. They are similar to bismuth in that they are all elemental materials with a low melting point, therefore could be easy to be implemented in vdW-molding method. They are interesting because they either have topological phases or will exhibit topological properties under certain conditions. The drop casting - hydraulic press method to prepare seed material might not be suitable in these cases, but other preparation methods can be developed specifically for them. For example, depositing thin films on hBN for vdW-molding would be an easy approach.

Other materials that can be applicable are binary compounds such as Bi_4Br_4 and Bi_4I_4, both are topological materials with melting points below 350°C. The as-grown crystals can be used as

seed materials so that the ratio of each element is already optimized, and the vdW-molding can be used as a way to achieve high surface quality and passivation. Encapsulating each of the component elements in the mold could work too, if they both are in solid form. However, how the elements interact in the mold is dependent on their specific properties and are so far all unknown to us.

2.6 vdW-molding with interlayer hBN molds

The thickness of the molded bismuth crystal in the vdW-molding technique is dependent mostly on the volume of the seed crystal, the pressure applied and the rigidness of the squeezing substrate. These can provide some tuning knobs for thickness control. However, the thickness range achieved using this method turn out to be quite limited. To be able to control the thickness in a more straightforward way would be very beneficial for thickness dependent analysis.

One way to achieve this is to add a structural supporting layer between the top and bottom hBN crystals. This layer should have a hollow structure so that the melt phase bismuth can flow inside. The thickness of the grown bismuth is determined mostly by the thickness of the supporting layer.

I start by making lithographically defined hBN channel structures and stack them between the hBN heterostructures and place the seed bismuth crystals at the entrance of the channels. During the vdW-molding process, the bismuth melts and flow into the channel structures. However, the pressure gradient within the stack during the growth process also affects the hBN channel pieces. Since the friction between vdW materials with large lattice mismatch are usually small[87], these hBN channel pieces are easily pushed around by the melt phase bismuth. As a result, the shape

of the channels is destroyed by these lateral movements (Figure 2.6.1). Aligning the lattice orientations of the hBN layers so that they are commensurate to increase the friction does not stop the hBN channel pieces from moving. Furthermore, hBN-Bi-hBN stacks with additional open hBN channels are much more difficult to make than normal vdW-molding stacks.

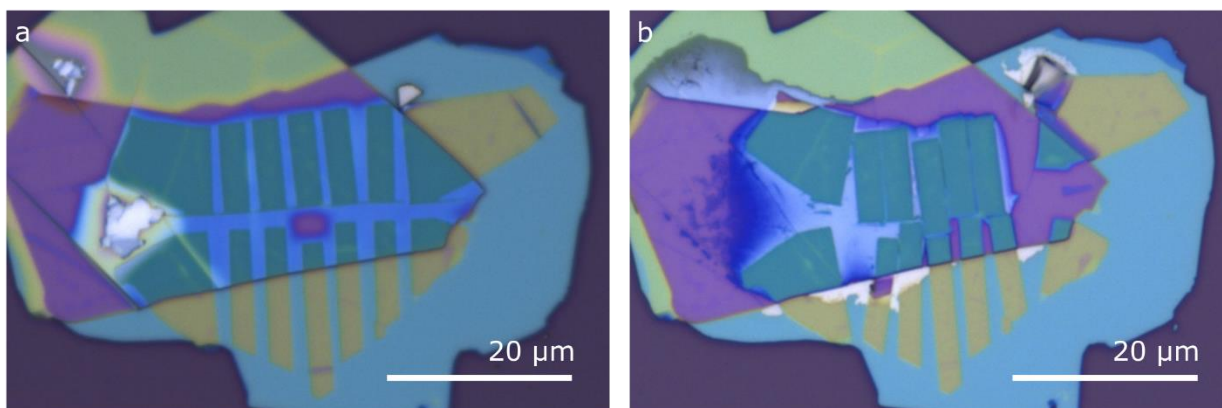

Figure 2.6.1 vdW-molding with interlayer hBN channel structures. a&b, optical images of the bismuth sample stack before and after the vdW-molding process.

To improve this idea, I consider making closed shape mold within hBN instead. This way, the shape cannot be easily broken by the pressure gradient in the melt phase bismuth, and this would give us much better control of the overall shape. To ensure the majority of the mold is filled by bismuth and reduce the amount of seed crystal oxide shell entering the mold, I place the seed bismuth next to the hBN mold, between two flat surfaces of hBN layers. There are versions of hBN molds with entrance regions for bismuth seed crystals, but that usually results in trapped gas in the mold after vdW-molding.

This method turns out to be a success (Figure 2.6.2). Bismuth grown this way is already in the designated shape and encapsulated in hBN, which makes device fabrication much simpler, and the crystal quality better maintained throughout the device fabrication process.

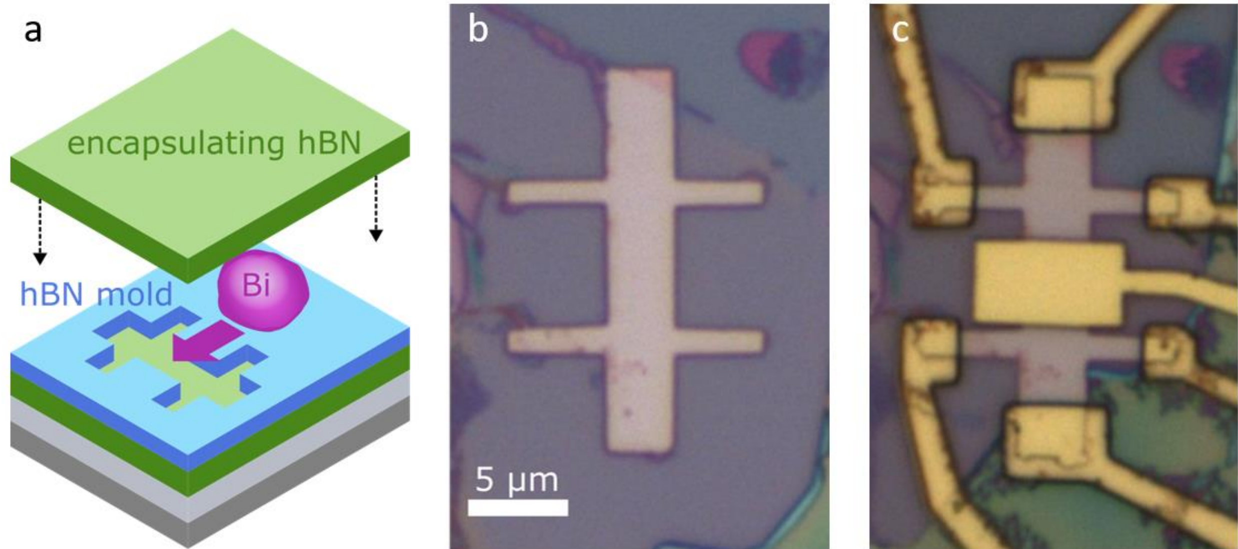

Figure 2.6.2 vdW-molding with a closed shape interlayer hBN mold. a, schematics showing the molding process. b, optical image showing the molded bismuth sample. c, optical image showing the transport device fabricated from the same sample.

The bismuth samples thicker than 40 nm presented in this thesis are all made with the interlayer hBN mold method. While they produced high quality data, there is still room for improvement in this growth method described in the following three issues:

1. The dangling bonds on the edge of the interlayer hBN molds can affect the crystal orientation of the grown bismuth crystal and increase the number of domains in it.
2. Each of the sample stack uses one lithographically defined hBN mold, which cannot be reused. There is always need for new large flat hBN crystals and lithography at these specific locations.
3. The top hBN is flexible, so the top surface of the molded bismuth can be concave or convex depending on the volume of the seed crystal and the pressure applied; the mold can even collapse if its width is too wide or the top hBN is too thin.

2.7 The vdW injection molding method

Based on the idea of vdW-molding within specific shaped mold, my team members of this project came up with a new growth technique improved upon the existing interlayer hBN mold method. In this technique, the first two out of the three issues listed above is solved, while the third problem can be solved by increasing the rigidity of the top squeezing substrates or changing the way pressure is applied, etc.

This method is named the “vdW injection molding” method. Instead of using patterned hBN molds within the sample stack, the shape defining mold is outside the stack (Figure 2.7.1). The mold is made from SiO_2/Si chips, by defining the shape using photoresist PMMA and e-beam lithography, and etching away the SiO_2 using Armour Etch, we can create trenches of the desired shape on the chip surfaces. Then, by transferring the hBN-Bi-hBN stack on top the trench, we are effectively using hBN as the liner material of the trench-mold. This way, there are no dangling bonds inside the mold, and by sonicating and rinsing, the mold can be reused multiple times. Bismuth samples grown in this mold show great structural and electronic transport properties.

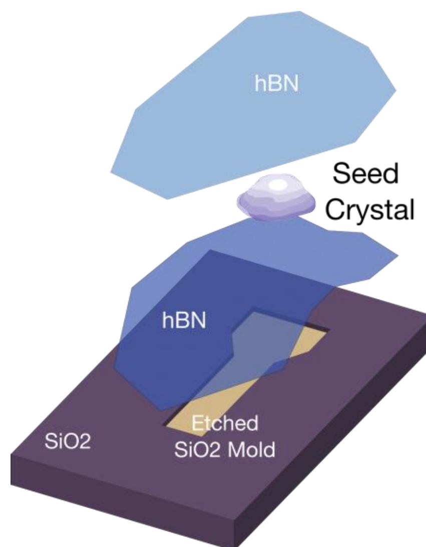

Figure 2.7.1 Schematics of the vdW injection molding method.

2.8 Removing the top hBN

To characterize the surfaces of our bismuth sample, we used a polyvinyl chloride (PVC) pillar stamp to remove the top hBN flake[88]. The PVC pillar is made by securing a PVC film (Riken Wrap from Riken Fabro) onto a micromolded PDMS pillar that is 10 µm × 10 µm × 20 µm. Then, we approach the top hBN flake slowly with the PVC–PDMS pillar as we heat the stage to 55–70 °C[89]. Once in contact, we slowly lift the PVC–PDMS pillar stamp with piezo-motors, which peels the top hBN flake away from the bismuth.

Chapter 3

Structural analyses of vdW-molded bismuth

3.1 Thickness and surface geometry study via AFM characterizations

Through vdW-molded growth method, we reduced seed bismuth crystals that were 250–500 nm thick to ultrathin crystals ranging from 5 to 30 nm thick. Optically, the crystals exhibit large smooth areas with step-like contrast changes (Figure 3.1.1 and Figure 3.1.2). These smooth areas emerge from a rougher material composed of both small voids in the crystal, likely due to trapped gas, and oxide that surrounded the original bismuth flake. After removing the top hBN layer, we characterize the bismuth surface by AFM (Figure 3.1.1b and Figure 3.1.3). The optically smooth regions correspond to flat terraces 0.5 to 5 μm wide separated by uniform steps. The average step height in Figure 3.1.1b is 3.9 ± 0.4 Å, which matches the thickness of a buckled hexagonal layer of bismuth[1].

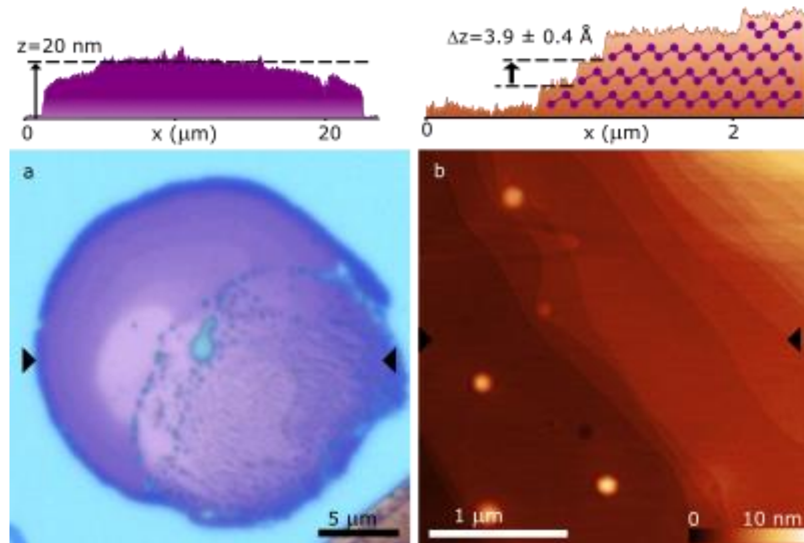

Figure 3.1.1 Optical image and AFM characterizations of the vdW-molded bismuth crystals. a, Optical image of the encapsulated vdW-molded bismuth (sample M30); black triangles indicate location of the AFM line trace (top) of the bismuth taken after removing the top hBN flake. This bismuth varies from 10 to 20 nm thick. b, AFM topography of the vdW-molded bismuth after removing the top hBN, showing wide flat terraces. Black triangles show location of the line trace (top). The average step height is 3.9 ± 0.4 Å. The diagram inset in the shaded region shows the crystal structure.

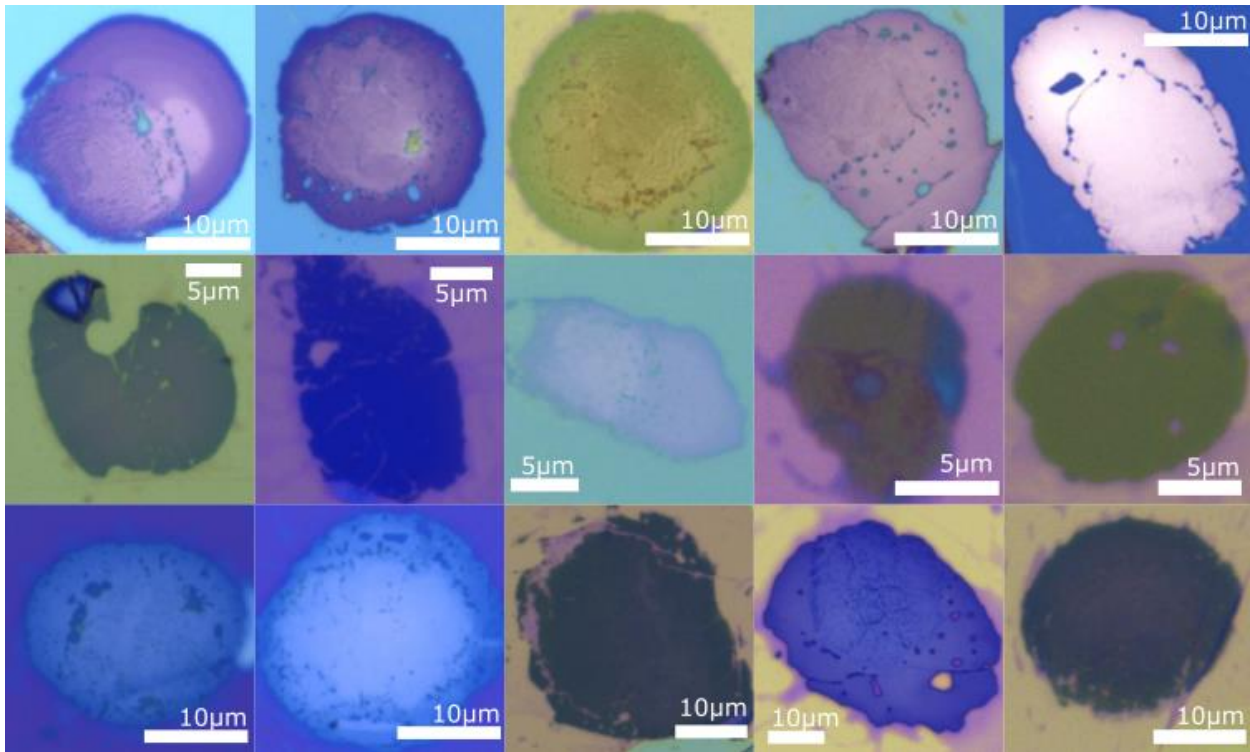

Figure 3.1.2 Optical images of vdW-molded bismuth samples. For samples M60 and M87 the top hBN flakes have been removed. Scale bar is the same for all the images 10 µm.

To characterize the flatness of the vdW-molded bismuth, we plot the distribution of height deviations across a wide terrace (Figure 3.1.4a&b). Within the terrace of the vdW-molded bismuth, the surface is ultraflat with an average root mean square deviation $\delta_{Bi-BN} = 0.11$ nm (Figure 3.1.4b). By comparison, bismuth molded by thermally grown SiO_2 exhibits a roughness of $\delta Bi-SiO_2=0.27$ nm. We ascribe this difference to the intrinsically flat structure of the vdW-layered hBN ($\delta_{BN} = 0.05$ nm) as compared to the amorphous SiO_2 ($\delta SiO_2=0.25$ nm). We have tested other mold substrates, such as graphite, sapphire and mica, and observed that the mold surface roughness is imprinted on the squeezed bismuth (Figure 3.1.5), with hBN producing the overall best results.

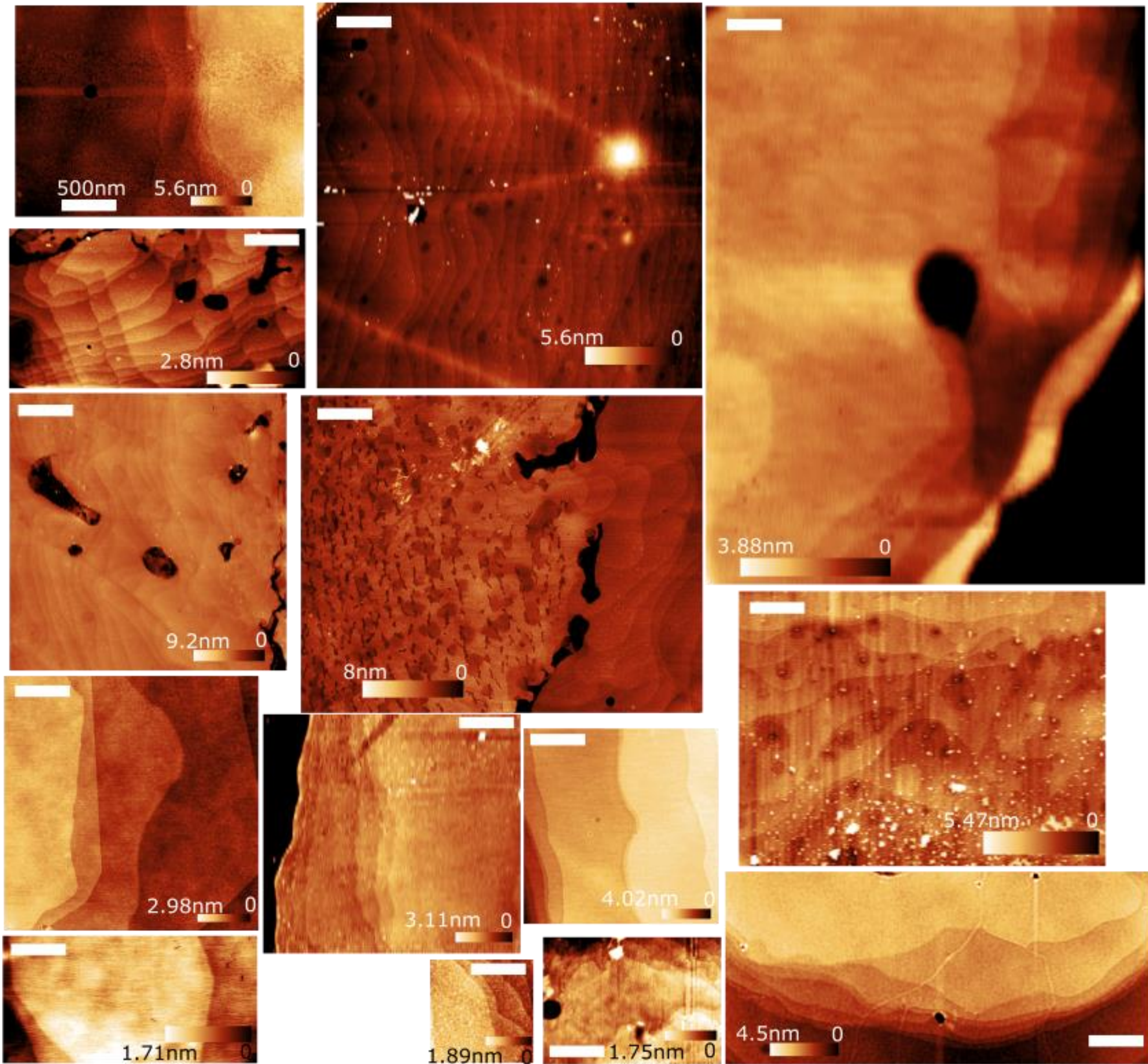

Figure 3.1.3 AFM scans of the vdW-molded bismuth surfaces showing various flat terrace structures. All samples have the top hBN removed, except for M92. Clear layered terraces are visible in M92 through the thin hBN layer.

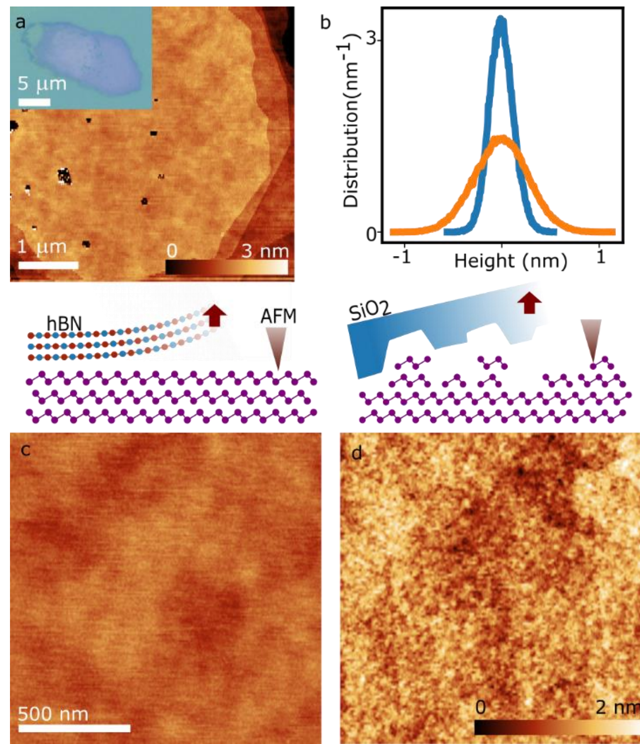

Figure 3.1.4 a, AFM topography of vdW-molded bismuth showing large flat terraces (sample M60). The inset shows an optical image of the sample. b, Height distribution of vdW-molded bismuth (blue) and SiO2-molded bismuth (orange). c,d, AFM images of the surfaces of vdW-molded bismuth (c) and SiO2-molded bismuth (d). Top substrates are removed before AFM. Scale bar is the same for both images, and the color bar shows the height. The diagrams above depict the imprinting effect of the mold substrate on the bismuth.

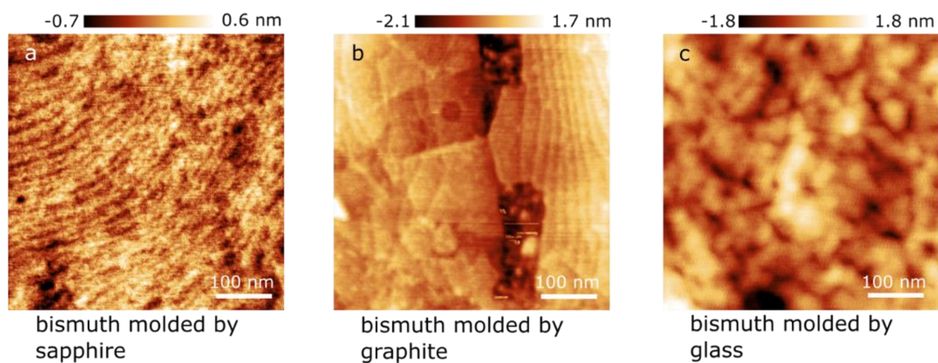

Figure 3.1.5 AFM topography of bismuth molded under pressure between different substrates.

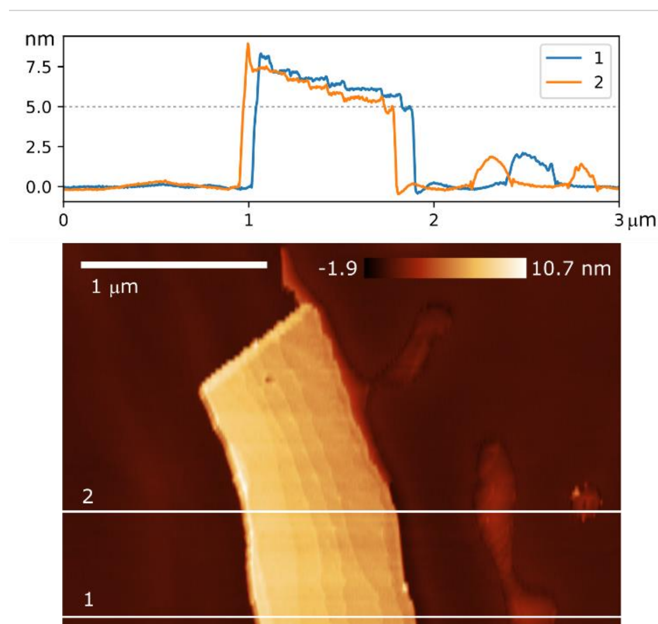

Figure 3.1.6 AFM topography and line profile of a vdW-molded bismuth showing a 5 nm thick terrace.

Table 3.1-1 Thickness and terrace sizes for vdW-molded bismuth samples.

Note: This table only shows thin samples molded between two hBN layers.

Sample Name	Max thickness (nm)	Min thickness (nm)	Diameter (μm)	Substrate	Max Terrace width (μm)
M60	15	12	18	Glass	2.1
M69	16	12	11	Glass	0.4
M65	17	12	13	Glass	1.0
M48	17	12	20	Glass	
M42	19	9	21	Glass	
M77	21	12	26	Glass	0.9
M30	21	6	21	Glass	2.2
M91	22	13	32	Glass	
M66	22	9	27	Glass	0.7
M79	25	13	17	Glass	1.0
M75	26	16	24	Glass	0.3
M87	26	20	27	Glass	1.2
M76	27	13	23	Glass	0.4
M59	33	18	9	Glass	0.6
M49	39	13	24	Glass	1.0
M58	10	7	17	Sapphire	1.8
M88	11	9	18	Sapphire	2.4
M80	11	11	26	Sapphire	1.3
M92	15	11	14	Sapphire	3.8
M61	20	12	9	Sapphire	1.2

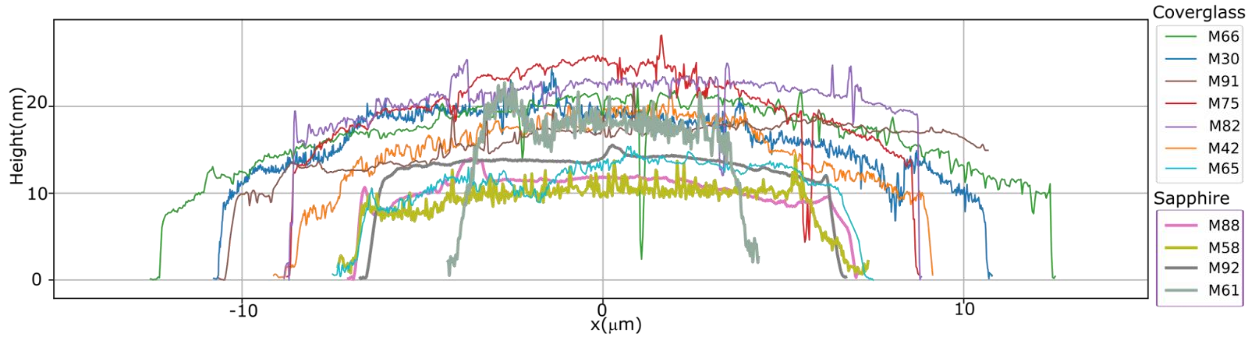

Figure 3.1.7 AFM line profiles of vdW-molded bismuth samples squeezed by glass or sapphire top substrates showing a dome shape. Squeezing with sapphire as the top substrate leads to overall thinner bismuth with a flatter profile.

By analyzing 20 different growths, we find that vdW-molded bismuth forms a dome shape with a typical thickness of 8 to 20 nm; terraces as thin as 5 nm can be observed near the crystal edge (Figure 3.1.6). The compression squeezes the bismuth until the top and bottom substrates elastically deform and contact around the hBN/Bi/hBN stack, which we estimate to occur at 300 MPa pressure. Without compression, vdW molding results in thicker bismuth crystals (thickness $t > 100$ nm). This behavior is consistent with a continuum model, which predicts that thinner crystals are achievable by using more rigid substrates (see section 3.4). Using sapphire top substrates instead of glass shows 40% thinner bismuth on average (Figure 3.1.7).

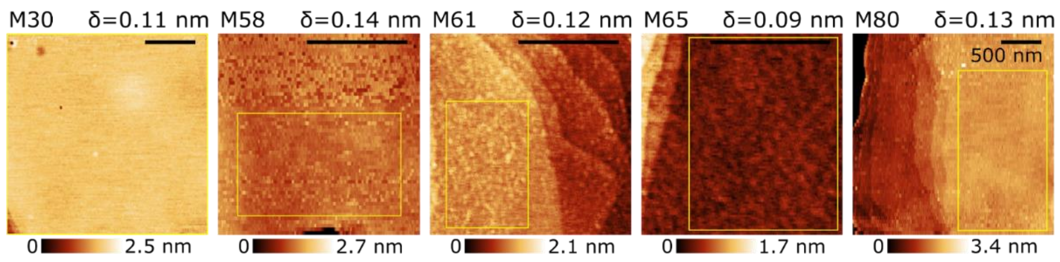

Figure 3.1.8 Additional AFM roughness data from 5 different vdW-molded bismuth samples. The roughness shown on top of each AFM image is measured in the region inside the yellow box. Scale bar is 500 nm. All samples show low roughness comparable to the sample in Figure 3.1.4c.

Table 3.1-2 RMS roughness of different molding substrates and the corresponding molded bismuth

Substrate	RMS roughness of the substrate	RMS roughness of the molded bismuth
Sapphire	0.63 Å	2.1 Å
Graphite[90]	0.23 Å	1.0 Å
Glass	1.3 Å	5.3 Å

3.2 Crystallinity study via TEM, EBSD and Raman characterizations

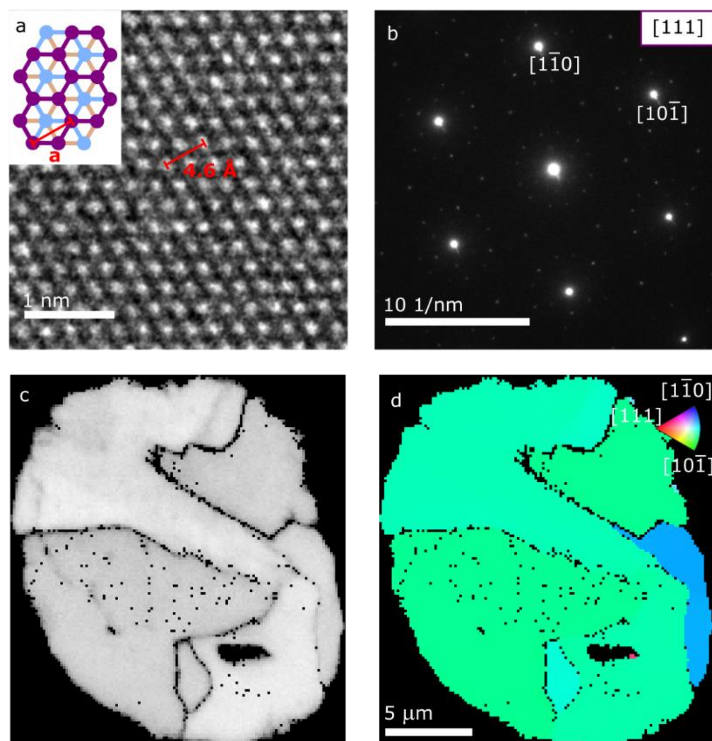

Figure 3.2.1 Crystallinity of vdW-molded bismuth. a, TEM real-space image of vdW-molded bismuth. The inset shows the bismuth (111) lattice structure. b, TEM selected area electron diffraction (SAED) of vdW-molded bismuth. c, EBSD band contrast of the vdW-molded bismuth showing internal domain boundaries (dark lines). d, EBSD Y-axis inverse pole figure of (111)-orientated vdW-molded bismuth showing domains with different in-plane rotations. Colors indicate the crystal orientation parallel to the in-plane Y-axis.

To determine the structure and crystallinity of the vdW-molded bismuth, we performed transmission electron microscopy (TEM), electron backscatter diffraction (EBSD) and Raman spectroscopy. All three measurements are consistent with the rhombohedral structure of bismuth. The TEM and EBSD diffraction measurements, performed on seven different samples, reveal that the bismuth is highly crystalline and oriented along the (111) axis, corresponding to buckled hexagonal layers stacked parallel to the substrate (Figure 3.2.1a,b&d). The in-plane lattice constant measured from the real-space TEM image is 4.59 Å, which is within 1% of the bulk

bismuth value 4.54 Å[1]. Diffraction measurements show (111) domains many micrometers in width that are differentiated by relative in-plane rotations (Figure 3.2.1d). Domain boundaries are also visible in AFM images (Figure 3.3.1). In some samples, the entire 20-µm-diameter flake is single crystal (Figure 3.2.4). The in-plane orientation of the bismuth shows no alignment with the encapsulating hBN (Figure 3.2.2).

TEM sample preparation: We transfer the vdW-molded ultrathin bismuth onto a TEM grid (200 nm silicon nitride membrane TEM grid with 2.5 µm holes from Ted Pella) via the PVC transfer method explained previously[88]. Samples are measured in a JEOL-2100F TEM instrument with a Schottky-type field emission electron source with 80–200 kV acceleration voltage.

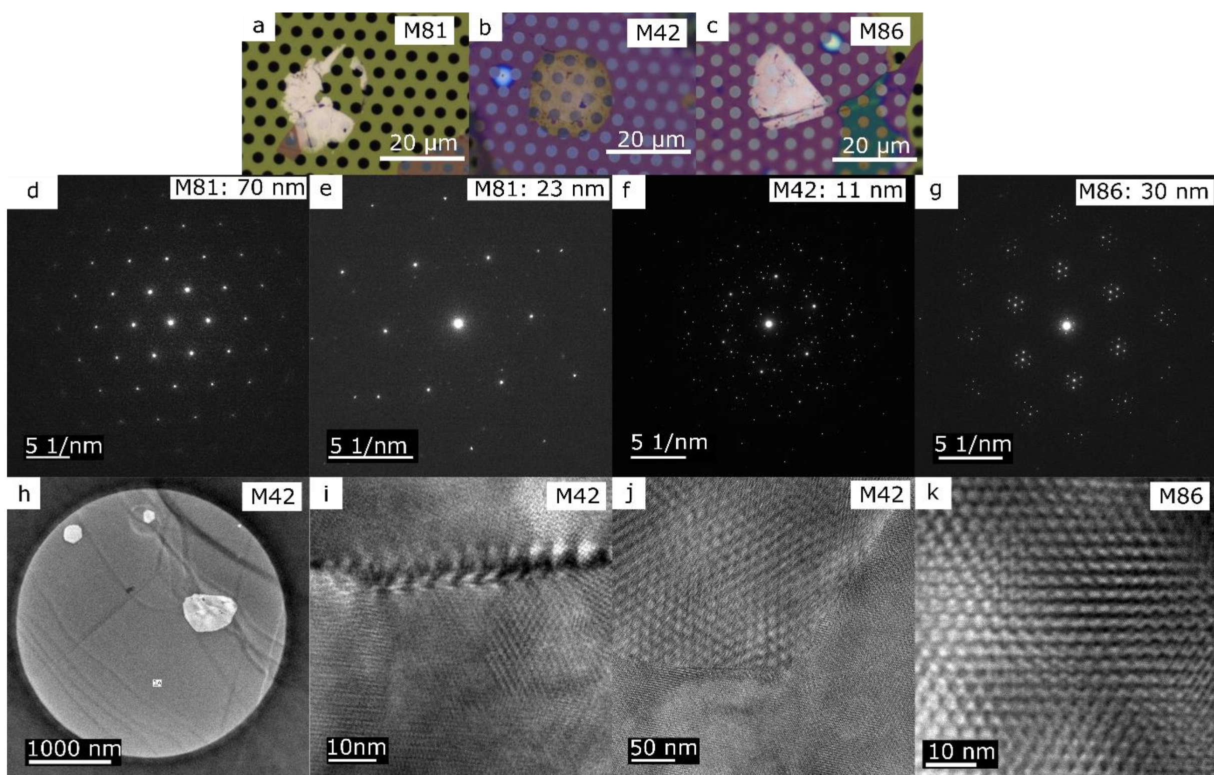

Figure 3.2.2 3 samples measured in TEM all exhibited rhombohedral lattice structure with the (111) axis oriented out of plane. a-c, Optical image of vdW-molded bismuth samples on TEM grids. a, vdW-molded bismuth with hBN flakes removed, b, vdW-molded bismuth encapsulated between hBN flakes and c, vdW-molded bismuth with bottom hBN flake. d-g, Selected area diffraction images for the samples shown in a,b,c. Bismuth thickness at site of diffraction measurement is indicated in top right corners. h-k, Real space TEM images showing terraces (h), grain boundaries (i&j),and bismuth-hBN moire patterns (j&k).

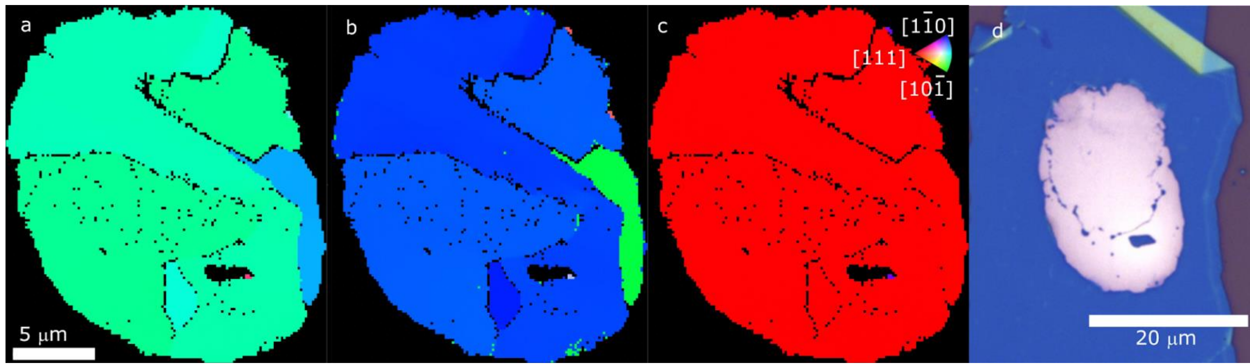

Figure 3.2.3 a-c, Electron beam backscattering (EBSD) inverse pole figures (IPF) of vdW-molded bismuth sample shown in Figure 2 g&h. a, Y-axis IPF, b, X-axis IPF, c, Z-axis IPF, d, Optical image of vdW-molded bismuth used for EBSD (top hBN removed). Note that due to stage drift, the EBSD image appears distorted in size compared to the optical image.

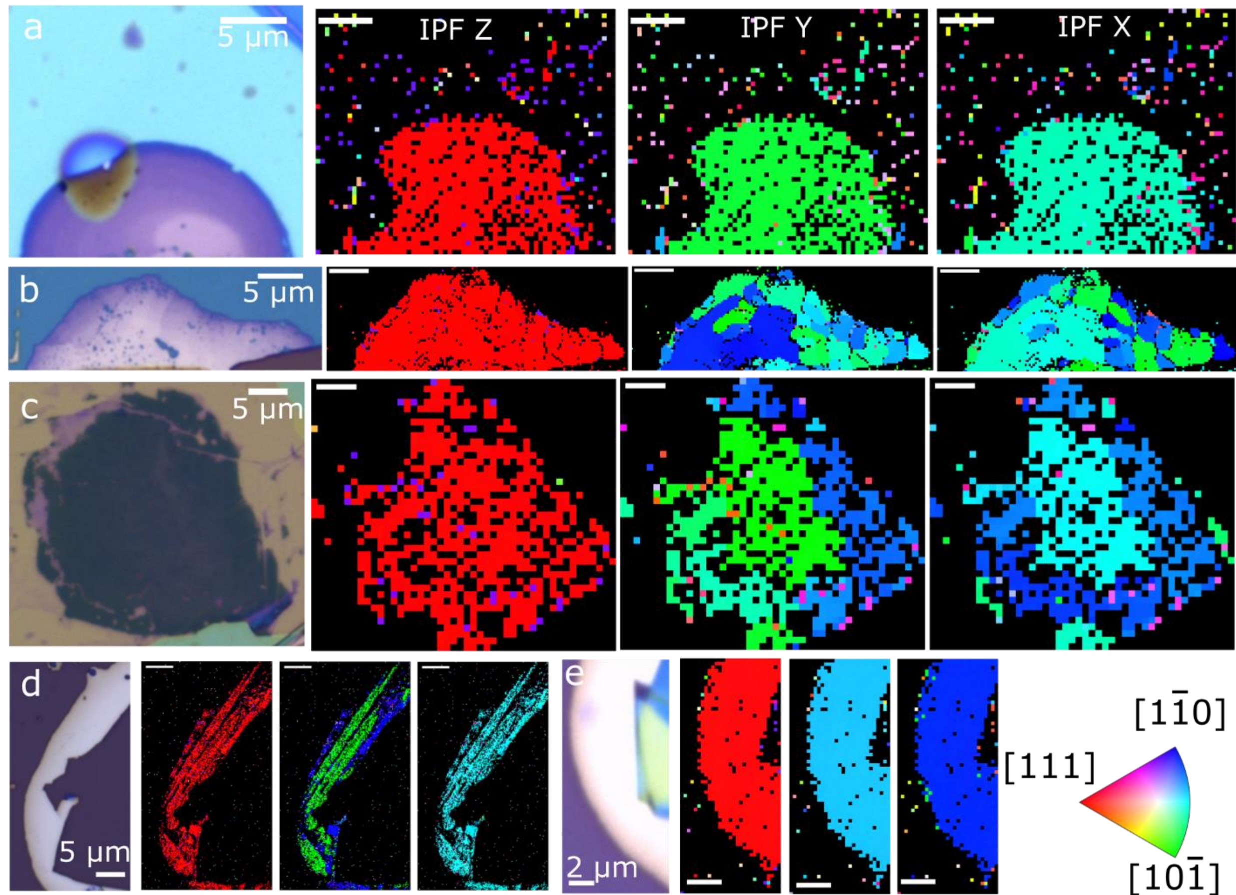

Figure 3.2.4 Optical image and X,Y,Z inverse pole figures are in respective order from left to right for each sample. a&c, vdW-molded bismuth encapsulated between hBN. b, vdW-molded bismuth without top hBN. d-e, SiO_2-molded bismuth on the edge of a hBN flake. Bismuth thickness for panels a-e are 21 nm, 23 nm, 17 nm, 20 nm − 61 nm, and 30 nm, respectively.

3.3 Correlating domain structure in AFM and EBSD data of vdW-molded bismuth

Domain walls observed in EBSD can also be observed in AFM. Figure 3.3.1 shows a comparison of EBSD and AFM data from different regions on two samples. In AFM, we observe that domain

boundaries typically appear along terrace edges, internal voids, valleys, or as raised ridges. Domain walls can even be identified that cross the interior of a terrace, where they appear as a 2 nm raised ridge in an otherwise flat surface (Figure 3.3.1f&g). Within regions composed of clear terraces that are not obscured by irregular features, we found only one domain wall that is not clearly visible in AFM, as compared to the > 30 domain walls observed in both AFM and EBSD. In this way, we can use AFM images to avoid domain walls within a device.

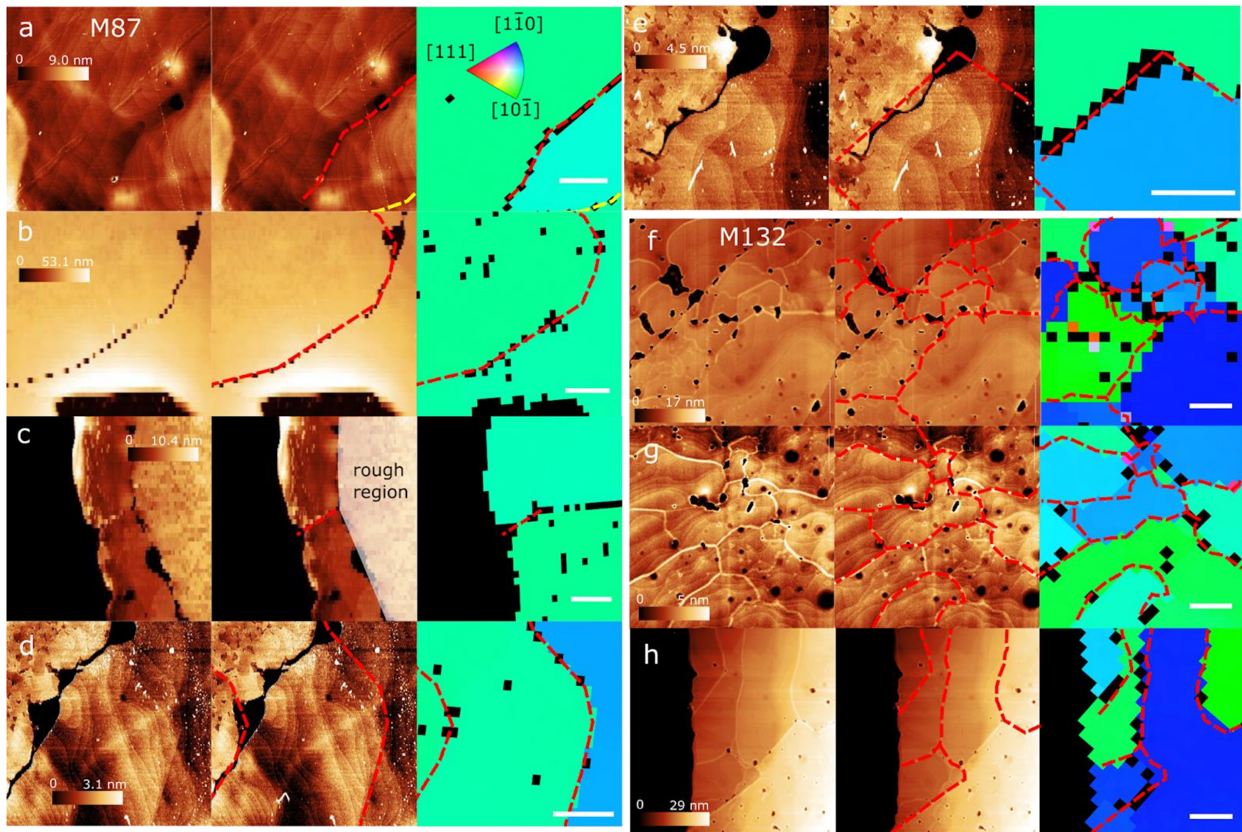

Figure 3.3.1 Visibility of domain boundaries in AFM images. a-h, Each set of 3 adjacent images correspond to an AFM topography map (left), the same AFM map with domain wall overlay (center), and an EBSD map of the same sample region with the same overlay (right). Dashed overlay lines indicate the grain boundaries identified from EBSD. Red dotted lines indicate a domain wall observed in both EBSD and AFM. Yellow dashed line indicates a domain wall not observed in AFM (a). White shaded area is a rough surface region that we exclude. Data is taken from two samples: M87 (a-e) and M132 (f-h). The scale bar is 1 µm.

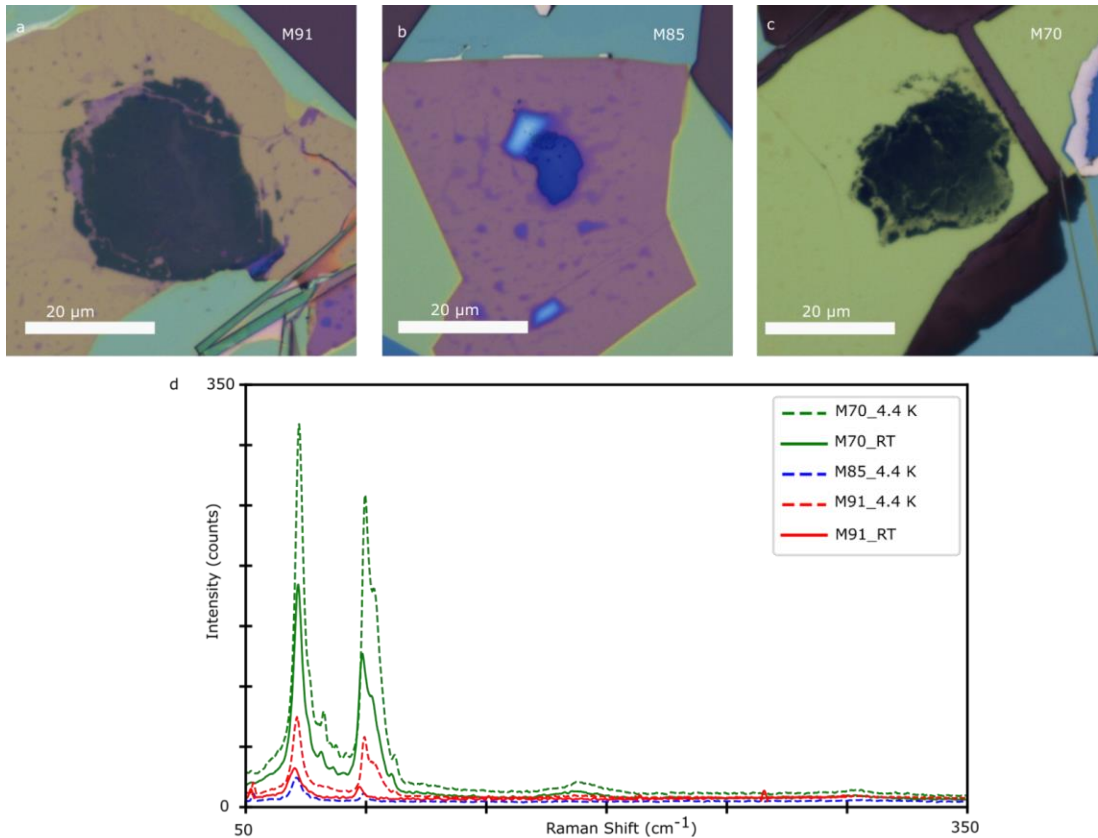

Figure 3.3.2 a-c, Optical image of bismuth hBN-encapsulated samples. d, Raman data of M70, M91 at room temperature (solid lines) and M70, M85, M91 at 4.4 K (dash lines).

Raman data (Figure 3.3.2d) are taken in a Horiba LabRAM HR Evolution with an ultra-low frequency module (532 nm laser). The vdW-molded bismuth samples are on Si chips with 300 nm SiO_2. M91 and M85 are encapsulated stacks of vdW-molded bismuth.

At room temperature, we observed two peaks in M70 at 71.9 cm^{-1} and 98.6 cm^{-1} (M91 at 70.3 cm^{-1} and 97.3 cm^{-1}). These values closely match the frequencies of the normal modes observed in bulk rhombohedral bismuth at 71 cm^{-1} (E_g) and 98 cm^{-1} (A_{1g})[91]. In M91 and M85, we do not observe any bismuth oxide related Raman modes. In M70, we observe a faint peak at 185.9 cm^{-1} which matches the Bi-O stretching mode at 185 cm^{-1} [92]. During the molding process of M70, most of the melted bismuth flowed out of the bottom hBN flake, leaving a higher concentration

of the bismuth oxide from the source flake (Figure 3.3.2c). We conclude that our samples are rhombohedral bismuth encapsulated between hBN flakes with minimal oxidation.

3.4 Simple continuum model of squeezing limits

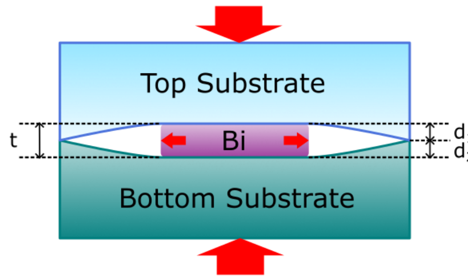

Figure 3.4.1 Depiction of substrate deformation during the squeezing process.

The squeezing limit model considers a balance of the pressure to squeeze the liquid bismuth due to its surface tension $P = 2S/t$ with the pressure to indent the substrate $P = 2rEd/\pi r^2 = 2Ed/\pi r$, where r is the droplet radius, E is the substrate's elastic modulus, d is the depth of indentation, and S is the the difference in surface energy per unit area between the bismuth-hBN and hBN-hBN interfaces (i.e. the relative surface tension). Assuming identical top and bottom substrates, the limiting condition occurs when $t = 2d$, i.e. the bismuth is fully indented symmetrically into both substrates. From this condition we derive the thickness limit $t = \sqrt{2\pi S_T\, r/E}$. In the case where the substrates are different (ex: Silicon on the bottom, glass on top), then we can relate the depths of indentation into each substrate with the total thickness $t = d_1 + d_2$, where d_1 and d_2 are the depth of indent for the bottom and top substrates, respectively.

The resulting derived equations are ${d_1}^2 = \pi r S_T / E_1 (1 + E_1/E_2)$ and ${d_2}^2 = \pi r S_T / E_2 (1 + E_2/E_1)$.

Table 3.1-1 shows calculated values for the limiting thickness under various conditions. For these estimates, we use the bare bismuth surface tension value of S = 0.388 J/m^2 [85]. Note that this neglects the interaction between the bismuth and hBN, and also neglects that growing the surface area of the bismuth requires breaking hBN-hBN interlayer bonds at the periphery of the laterally expanding droplet. The hBN-hBN cohesion energy is measured to be 0.326 J/m^2 [93], potentially nearly doubling the true value for S.

The primary results in this paper are for Si:Glass and Si:Sapphire squeezing, with predicted limits of 15 nm and 10.6 nm, respectively, using the above equations. This matches well the range of thicknesses we observe in our actual squeezings. Switching to dual Sapphire substrates would reduce the predicted thickness to 9 nm, and reducing the droplet radius by 4x would give an additional 2x reduction in thickness. Thinner squeezing may be achievable by circumventing the substrate deformation trapping, for example, by concentrating pressure into smaller regions.

Table 3.4-1 Limiting thickness value at max pressure for r = 10 μm droplet following the simple deformation model

Squeezing substrates	thickness (nm)
Si:Si (E=170GPa)	12
Si:Glass (170GPa:70GPa)	15
Si:Sapphire (170GPa:300GPa)	10.6
Sapphire:Sapphire (300GPa)	9

3.5 Molecular Dynamics Simulations of Squeezing

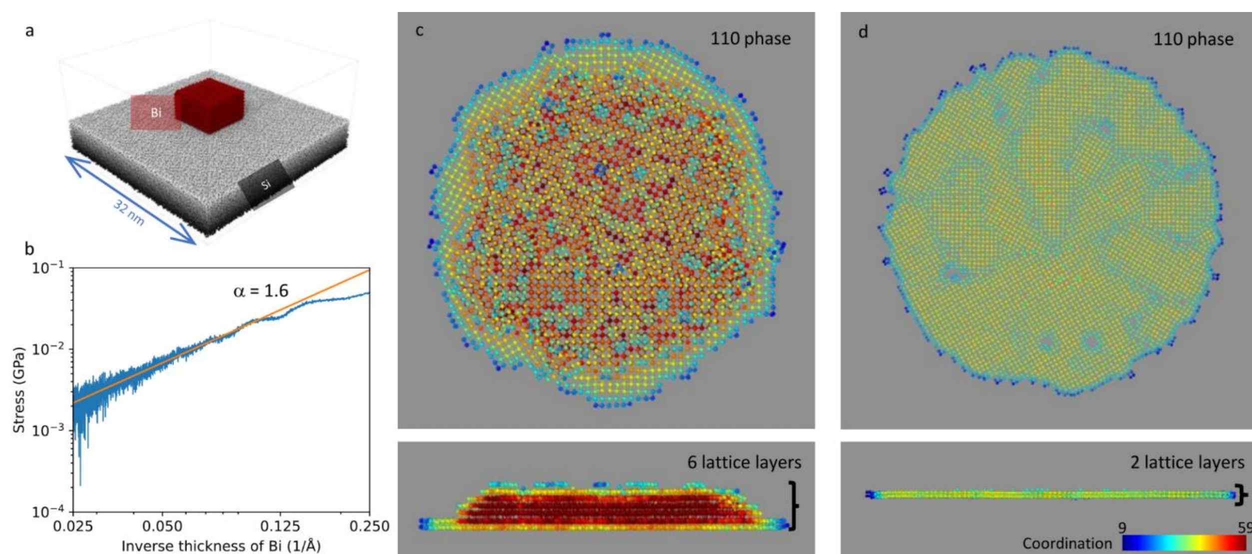

Figure 3.5.1 Molecular dynamics simulation of bismuth squeezed by silicon. a, 3D view of the simulation setup, consisting of a bismuth block on a silicon slab. b, Blue: Simulation data showing uniaxial compressive stress as a function of the inverse thickness of the squeezed bismuth in the liquid state (temperature 550 K). Orange: Power-law fitting to data with exponent alpha. c, Resulting bismuth crystal after melt-growth while squeezing with a 2 nm gap with a Si (111) substrate. Top view and side view (upper and lower panels, respectively). d, Same simulation as in (c) but with a 0.75 nm gap between squeezing substrates. The colors of the atoms represent the sum of coordination numbers from 1st to 5th nearest neighbors (c-d).

To further study the limits of the squeeze method of producing ultrathin crystals, we performed molecular dynamics (MD) simulations of a nanodroplet of bismuth squeezed between planer indenter and silicon substrates. In the simulations, we find that it is possible to achieve crystals thinner than 1 nm when using starting bismuth material that is 301 nm^3 in volume and at applied uniaxial compression of 21 MPa (Figure 3.5.1). At this ultrathin limit, the bismuth is sensitive to the substrate interaction, in this case showing a (110)-orientated crystal when squeezed by (111)-orientated silicon (Figure 3.5.1c&d) and an amorphous phase when squeezed by (100)-orientated

silicon (not shown). Note that silicon was chosen as the squeezing substrate to simplify the simulation as compared to the more complex dynamics of a hBN crystal.

Details of Molecular Dynamics Simulations: Molecular dynamics simulations were performed using the open-source code LAMMPS[94]. The simulation consisted of a bismuth block compressed by a silicon substrate. The dimensions of the bismuth are 77.16 Å, 78.62 Å and 49.68 Å along x, y and z cartesian coordinates, respectively. The (111) plane of bismuth is perpendicular to the vertical direction, i.e., along the z-axis. The dimensions of the silicon were 325 Å, 325 Å and 55 Å, respectively. Periodic boundary conditions were applied along all three dimensions. Modified embedded-atom method (MEAM) was used to compute non-bonded interactions of bismuth[95]. Interactions between silicon atoms were modeled with a 3-body Stillinger-Weber (SW) potential[96]. The interactions between bismuth atoms and silicon atoms on the interface were described by the Lennard-Jones (LJ) potential, in which the well depth ε and size-parameter σ are 0.019996 eV and 3.225 Å, respectively[97]. The temperature was maintained at 300 K by a Langevin thermostat with the damping parameter set to 1 ps. A planar indenter with a force constant equal to 10 eV/Å^3 was used to compress the model from above the bismuth block with a constant velocity 0.1 Å/ps. The bottom of the silicon substrate was fixed to prevent movement. After the compression, the model was heated to the melting point (550 K) of bismuth for 50 ps. The planer indenter was maintained above the bismuth droplet to avoid the escape of bismuth atoms. The bismuth droplet was then cooled down to 300 K at a constant cooling rate 1 K/ps. The atomic structures were visualized by the program OVITO[98].

Chapter 4

vdW-molded bismuth device design and fabrication

4.1 Device design and fabrication goals

The vdW-molded bismuth shows large domains, ultraflat surfaces and micrometer-wide terraces through structural characterization, which is promising in exhibiting improved electronic transport properties compared to bismuth grown via deposition. The molded bismuth crystal is encapsulated with band insulator hBN sitting on SiO_2/Si chips, which makes it convenient to fabricate on-chip electronic transport devices through nanofabrication techniques.

To obtain clean transport data from bismuth boundary states, we would like to avoid uneven surfaces, grain boundaries and terrace edges, and isolate regions for device fabrication. This is enabled by the AFM topography characterizations of the vdW-molded bismuth in combination with their optical images. By avoiding terrace edges and irregularities visible in AFM, we select

micron-scale ideal areas in clean bismuth crystal regions composed of wide and flat terraces to minimize domain boundaries for electronic transport.

To electrically characterize the vdW-molded bismuth, we fabricated devices in clean crystal regions composed of wide and flat terraces to minimize domain. We measured both uniform-thickness devices etched from a single flat terrace and variable-thickness devices featuring many terrace steps.

4.2 Challenges in device fabrication

We successfully grow bismuth crystals between hBN layers and aim to fabricate transport devices from them. As this approach is new, I need to develop a corresponding device fabrication sequence. Several challenges arose, for example, making electrical connections to the bismuth encapsulated under hBN is one of the obstacles. There can be two solutions: removing the capping hBN layer, as explained in section 2.8, or etching through the top hBN using SF_6 plasma etch. Devices were fabricated using both approaches, with the fabrication sequence using the first approach shown in Figure 4.3.1.

Another requirement was to fabricate the bismuth in a transport geometry, specifically in a Hall bar shape. For ultrathin bismuth grown with vdW-molding method, plasma etching is an optimal solution, with chloride gases being the most effective option. However, since our clean room facility does not provide chloride gases in reactive ion etchers, I choose to use argon plasma etch with a high DC field instead. As a result, I have to increase the thickness of the PMMA resist used as a mask can survive the etching process.

The final challenge is the self-limiting oxide layer that bismuth forms when exposure to air. Testing revealed that the oxide layer introduces contact resistance ranging from hundreds of kiloohms to megaohms. Fortunately, we are able to obtain access to an ion mill integrated with an e-beam evaporator through one of our collaborators. This allowed the oxide layer to be removed by argon ion beam, followed by the direct deposition of electrodes on the bismuth without air exposure. Resistance tests after device fabrication show a significant reduction in contact resistance to approximately 100 ohms. However, the contacts will still deteriorate over time, so we had to store the sample in a glove box.

4.3 The device fabrication sequence

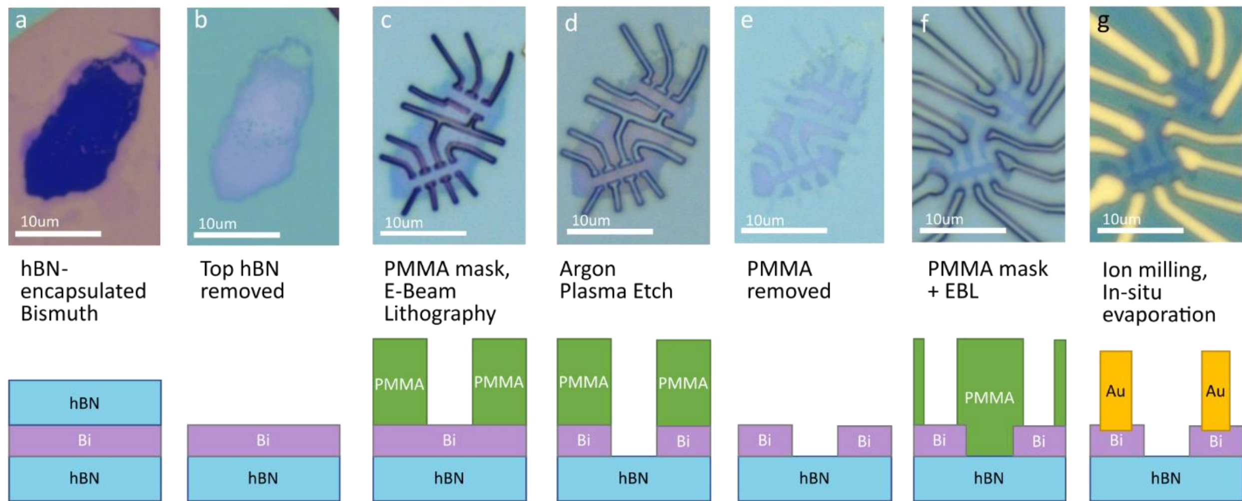

Figure 4.3.1 Process for fabricating open-face devices from vdW-molded bismuth crystals. a-g, Optical image and cross-sectional schematics of the fabrication of the bismuth transport devices.

The general device fabrication procedure is to isolate clean regions of vdW-molded bismuth via etching and then attach electrodes to the crystal. Here, ‘clean’ refers to regions with wide and flat

terraces where surface irregularities are minimized. This approach also minimizes internal domain walls, which appear as clear surface irregularities in the AFM images (Figure 3.3.1). The 8 nm and 13 nm devices are fabricated from vdW-molded bismuth samples with the top hBN removed, and the main transport channel between the voltage tabs is from one terrace of uniform thickness. The fabrication procedure for the open-face devices is shown in Figure 4.3.1.

First, the top hBN flake is removed via the PVC method[88]. The uniform regions are identified by AFM and are etched out from the bismuth using a PMMA mask (Microchem, 950 A7, 1 μm thick) made by electron-beam lithography. The bismuth is then etched into the designed shape via Ar plasma etch (Plasma-Therm reactive ion etcher model 790) with the following parameters: 300 W power, 401 V d.c. bias voltage, 30 sccm Ar flow rate and 115 mtorr process pressure for 45 s. This is followed by an O_2 plasma etch to remove cross-linked PMMA, using 70 W power, 227 V d.c. bias voltage, an O_2 flow rate of 9.9 sccm and a process pressure of 70 mtorr for 10 s. The remaining PMMA etch mask is removed in acetone. Next, electrodes are defined by a PMMA mask written via electron-beam lithography (1-um-thick piece of 950 A5 PMMA) and developed by a 3:1 (volume ratio) mixture of isopropyl alcohol and water. Since the bismuth is exposed to air, a thin oxide layer forms at its surface and results in a large contact resistance. We remove the oxide layer by Ar ion milling (Intlevac Nanoquest 1) with a 400 V beam voltage, 30 mA beam current, 80 deg beam angle and 80 V acceleration voltage for 5 s at 10 °C, and immediately deposit 5 nm Cr and 15 nm Au on top without exposing the bismuth to the atmosphere (Telemark 249). Finally, we evaporate additional metal onto the sample in a separate evaporator (Temescal CV-8; 5 nm Cr and 100 nm Au) and lift off the PMMA in acetone.

A similar fabrication process is also used to produce devices from encapsulated vdW-molded bismuth samples without removing the top hBN. Note, when the top hBN is thin, we are still able to observe the bismuth terraces through the hBN by AFM (as shown in Figure 3.1.3). In the bismuth geometry-defining etch (Figure 4.3.1d), we perform an extra step of an SF_6 plasma etch to etch away the top hBN before etching the bismuth with the Ar plasma. The hBN etching parameters are 30 W power, 15 V d.c. bias voltage, a SF_6 flow rate of 10 sccm and a process pressure of 100 mtorr for 15 s. In the step where we define the electrodes (Figure 4.3.1g), an SF_6 plasma etch is used to remove the top hBN in the unmasked region before ion milling the bismuth oxide.

Chapter 5

Cryogenic magneto transport characterizations

5.1 Brief introduction to cryogenic systems used in this work

Cryogenic measurement systems are specialized setups designed to perform precise measurements at extremely low temperatures. Their key components include cryostats to achieve and maintain at low temperatures, temperature sensors, and electronics for data acquisition.

Most of the transport data in this work is measured in Cryomagnetics C-Mag. It is a cryogenic measurement system with a superconducting magnet that can provide magnetic field along the vertical axis ranging from -12 T to 12 T, a variable temperature insert that can reach down to 1.6 K with a rotatable sample positioner, and a 49 mm diameter sample space. It is a dry system, meaning that there is no large volume of cryogens like liquid nitrogen or liquid helium stored in the cryostat to maintain the low temperature. The primary cooling from room temperature to 40 K in the 1st stage and 4 K in the 2nd stage is conducted through a cryocooler. The 4 K 2nd stage is

used to cool the magnet below its critical superconducting temperature, and to condense a small volume of helium for further sample cooling. The small volume of helium circulates in a closed loop through a scroll pump. Gas phase helium enters the cryostat, and is pre-cooled by the 1st and 2nd stage, before going through a needle valve into a helium pot where it expands, loses heat and condensed into liquid form. The liquid helium in the pot is continuously pumped by the scroll pump, and the evaporation of helium provides cooling power to maintain liquid helium at the 1.6 K. The liquid helium pot is attached to the wall of the variable temperature insert (VTI) chamber, where the variable temperature insert sits. The insert is cooled from the VTI chamber wall through a low pressure helium exchange gas (-10 inHg). Sample temperature adjustments are done through the sample heater on the insert next to the sample mount, in combination with a VTI heater attached to the wall of the VTI chamber.

A small portion of the transport data is obtained in Cell 9 of the National High Magnetic Field Laboratory, which is equipped with a 31 T, 50 mm bore magnet, and a top-loading liquid into sorbtion pumped He-3 system, which is able to bring the sample down to 320 mK. The cryostat is cooled and maintained at low temperatures via liquid nitrogen and liquid helium bath, which requires periodic refill but provides a low-noise measurement environment compared to dry systems because there is a lot less vibration. In this He-3 system, the sample insert and the He-3 gas/liquid share the same space, which is a long cylinder that goes from the top of the cryostat to the bottom of the magnet structure. A ring-shaped sorb is located on the middle of the cylinder chamber, on top of a 1 K helium pot. To activate the He-3 system to cool down the sample to the base temperature, first cool down the sorb to absorb the He-3 gas from the external He-3 tank and close off the cylinder chamber from the He-3 tank, then warm up the sorb to release the He-3 gas, so that they can be condensed into liquid form through the 1 K pot and drip down to the

bottom of the cylinder chamber. The sample sits at the bottom of the cylinder and is cooled by the liquid He-3. The liquid He-3 is then cooled further by evaporation cooling after lowering the sorb temperature again. The magnet in Cell 9 is a resistive bitter solenoid magnet. The temperature of resistive magnets can be controlled by water cooling, compared to superconducting magnets which requires cryo-cooling, which makes them more favorable in reaching high magnetic field. Resistive magnets can be quickly charged and reach high magnetic fields (in this case, 31T in a few minutes), as opposed to hour-long charging time of superconducting magnets. The disadvantage of resistive magnets is the high power consumption, and it is the reason why the magnet time is limited and we cannot keep the sample at high magnetic fields for an extended amount of time.

5.2 Temperature dependence and magnetic field dependence of bismuth thin crystal's resistance

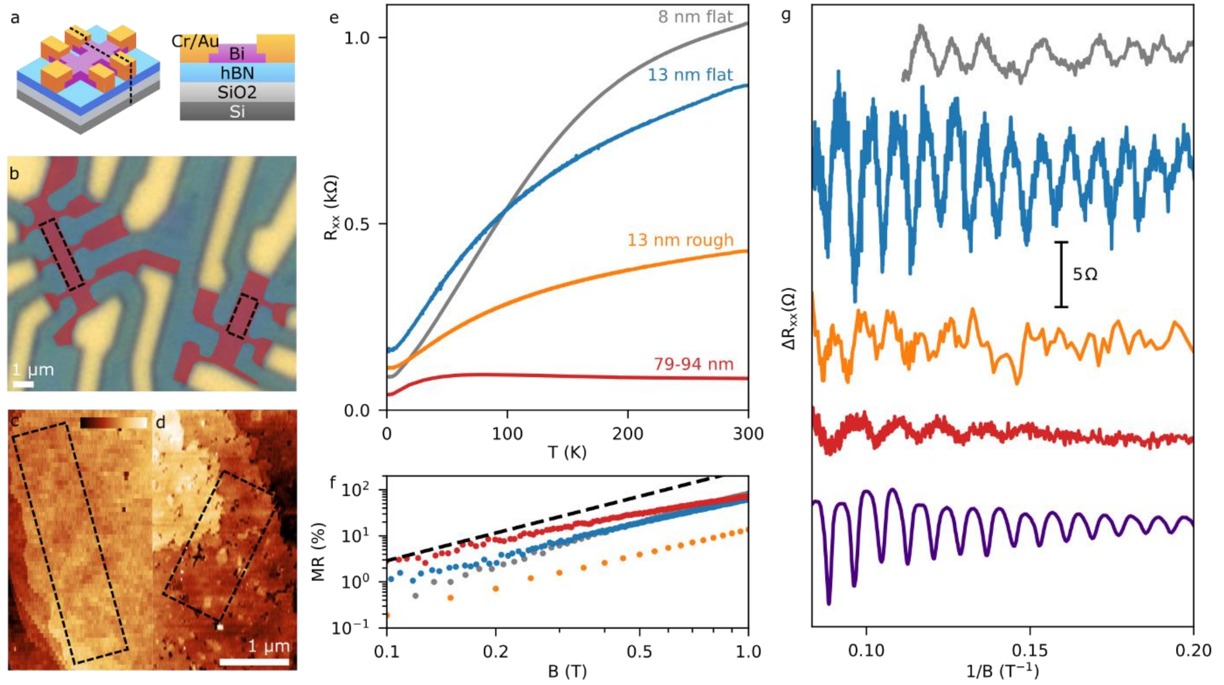

Figure 5.2.1 Electronic transport and quantum oscillations in vdW-molded bismuth devices. a, Isometric and cross-sectional schematics of the devices. b, False color optical image of the 13-nm-thick vdW-molded bismuth devices; top hBN layer is removed. Bismuth is red, while gold electrodes are yellow. c,d, Surface topography of the 13-nm-thick bismuth devices; one is ultraflat (c; 0.8 µm × 3.6 µm) and the other is rough (d; 1.1 µm × 2.1 µm). Color scale range is 0 to 2.5 nm and shows the height. Black dotted rectangles indicate the same regions on the bismuth devices in b. e, Longitudinal resistance (R_{xx}) as a function of temperature for different thickness devices. f, Logarithmic plot of magnetoresistance (MR) as a function of out-of-plane magnetic field ($T = 1.6$ K) for the same devices as in e. Black dashed line is quadratic dependence. g, Quantum oscillations in a plot of $\Delta R_{xx}(1/B)$, calculated by subtracting a smoothed background. Line colors correspond to the device labels in e. Additional data from a 92- to 106-nm-thick device is included (bottom-most purple line, scaled by ×0.05). Fermi surface areas from top to bottom are 2.75×10^{12}, 2.82×10^{12}, 2.99×10^{12}, 1.99×10^{12} and 2.60×10^{12} cm^{-2}.

We measured both uniform-thickness devices etched from a single flat terrace and variable-thickness devices featuring many terrace steps. In all vdW-molded bismuth devices, we observe metallic behavior at low temperatures with a positive slope of resistance versus temperature,

dR/dT (Figure 5.2.1e and Figure 5.3.1). The slope decreases with rising temperature, unlike the linear T dependence observed in bulk bismuth, and is a signature of confinement effects in the vdW-molded bismuth[4]. In thin devices, with thicknesses $t = 8$ nm and 13 nm, the metallic dependence persists to room temperature, but in thicker flakes, $t = 45$ nm to 106 nm, dR/dT can become zero or negative above ~50 K, indicating an activated dependence. This behavior, measured in eight devices, is well modelled by parallel conduction through a metallic channel and a semiconducting bulk that is gapped due to vertical confinement[51,53,99] (Figure 5.3.1). The metallic channel is identified with the (111) Rashba surface states, which are known from ARPES and STM studies to have electron and hole pockets[46,47,51]. This is consistent with our observation of a positive non-saturating magnetoresistance in all devices up to 12 T (Figure 5.2.1 and Figure 5.2.3), indicating nearly compensated electron-like and hole-like carriers.

The vdW-molded bismuth exhibits exceptional transport properties compared to MBE-grown thin films. Previously, thin bismuth studies have been characterized by weak temperature dependences with little metallic contribution and small residual resistance ratios of 0.5 to 1.6[53–56]. By contrast, our vdW-molded devices exhibit strong metallic dependencies, showing that surface-derived states can dominate the conduction at room temperature. This results in substantially larger residual resistance ratios, such as 12 and 5.4 for the flat 8 nm and 13 nm devices, respectively (additional devices in Figure 5.3.1). The substantially larger residual resistance ratio indicates reduced scattering times, which is also consistent with our observation of ×100 larger magnetoresistance signals than measured in MBE films (Figure 5.2.1f).

At high fields, quantum oscillations in the magnetoresistance emerge in the vdW-molded devices. The quantum oscillations are pervasive, occurring in 12 devices covering a wide range of thicknesses from 8 to 106 nm, with onset fields of 3 to 4 T (Figure 5.2.1g and Figure 5.2.3).

Even samples with non-uniform thicknesses and many terraces exhibit clean quantum oscillations (79 to 94 nm and 92 to 106 nm samples in Figure 5.2.1g). Additional discussion on the possible role of terrace steps and domains on transport behaviors can be found in section 5.6. The dominant oscillations correspond to a Fermi surface area of 2×10^{12} to 3×10^{12} cm^{-2}, which are ×13–20 larger than that of bulk bismuth[100] and are consistent with STM and ARPES studies of the surface state[46,47,51]. Such Shubnikov–de Haas oscillations in the magnetoresistance were first observed in bulk bismuth[5].

The presence of quantum oscillations in vdW-molded bismuth is striking, especially considering that the nanofabrication process exposes the bismuth to ambient air and polymers, which are avoided in MBE studies using in situ measurements[53,56]. A key difference is that MBE-grown bismuth has irregular surfaces with dense steps, typically 20 to 100 nm apart[62,70], which can scatter electrons and provide parallel conduction[45,101]. By contrast, the vdW-molded bismuth frequently exhibits 10 to 100 times wider terraces (Figure 3.1.3). The importance of surface flatness on transport properties is clear when we compare two devices from the same 13-nm-thick bismuth flake: one fabricated on an ultraflat terrace and the other on a rougher region (Figure 5.2.1c&d). The rough device shows features qualitatively similar to the flatter device, but with reduced values for the residual resistance ratio, magnetoresistance and amplitude of quantum oscillations (Figure 5.2.1e-g).

The quantum oscillations in the vdW-molded bismuth disperse with back-gate voltage, resulting in clear Landau fan features (Figure 5.2.2 and Figure 5.2.4). In the flat 13 nm device, two fans are observed with opposite slopes in the field-versus-gate space, indicating electron-like and hole-like carriers (Figure 5.2.2 c&e). At fields above 8 T, the hole fan changes to a different slope. At zero gate voltage, the $1/B$ frequencies of the oscillations, where B denotes the out-of-

plane magnetic field, correspond to Fermi surface areas n of 2.77×10^{12} cm^{-2}, 0.73×10^{12} cm^{-2} and 1.94×10^{12} cm^{-2} for the electron and two hole pockets, respectively. Interestingly, each Fermi surface changes similarly over the 140 V gate voltage range with $\Delta n = 0.78$, 0.93 and 1.13×10^{12} cm^{-2}. By fitting Landau fans to the datasets, we observe that the highest gate voltage depletes the low-density hole pocket to Landau index $N_h = 2$. Such a large gate modulation is important, as the different Fermi surfaces are expected to carry different spin textures due to Rashba spin–orbit coupling[1].

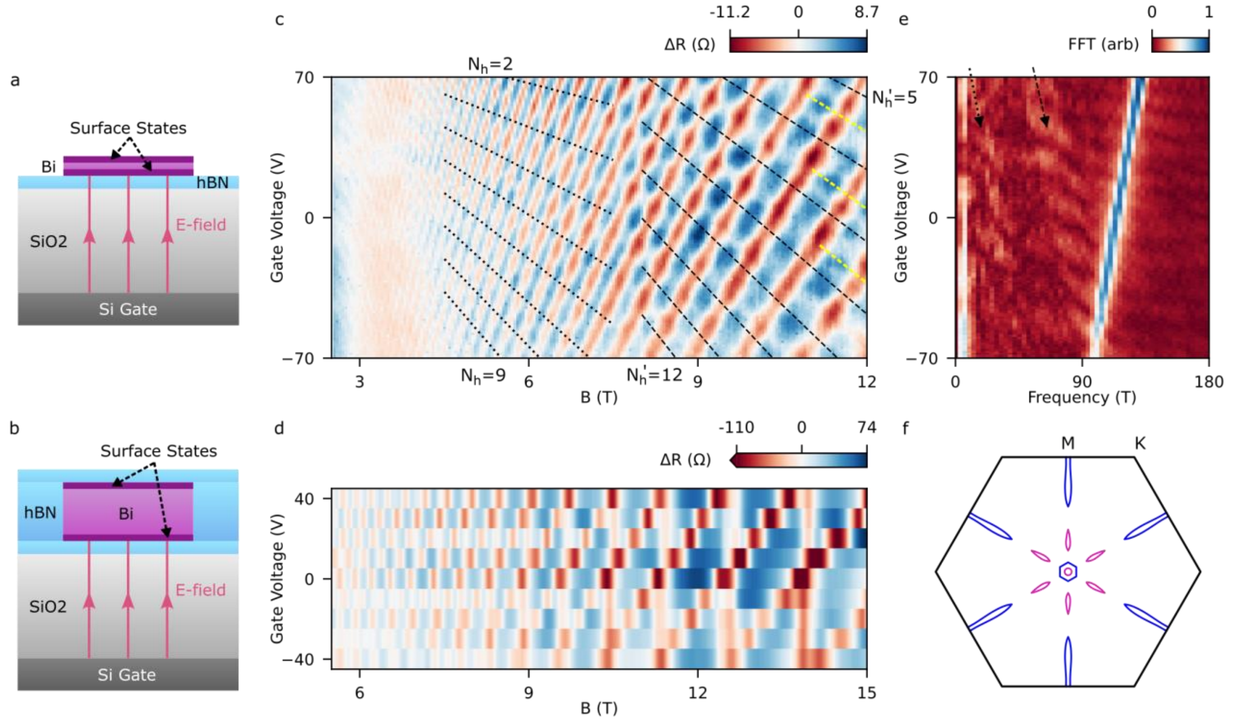

Figure 5.2.2 Gate-dependence and surface state coupling in thin and thick vdW-molded bismuth. a, Cross-sectional schematics of a 13-nm-thick bismuth device showing similar gate capacitive coupling to the top and bottom surfaces. b, Cross-sectional schematics of a 92- to 106-nm-thick bismuth device showing larger capacitive coupling of the gate to the bottom surface. c,d, Quantum oscillations measured as a function of gate voltage and magnetic field for the flat 13 nm device (c; T = 1.5 K) and the 92–106 nm device (d; T = 0.3 K). The ΔR is calculated by subtracting a smooth background from magnetoresistance measurements. Landau fan fit is indicated by dashed lines based on e. Devices are the same as in Fig. 3. e, The fast Fourier transform (FFT) of the quantum oscillations shown in c, showing one electron-like oscillation (blue streak feature) and two sets of hole-like oscillations indicated by the dashed arrows (same as in c). f, Fermi surface diagram of bismuth (111) surface states based on density functional theory (DFT) calculations of 4.7-nm-thick bismuth (Figure 5.2.5). Blue, electron pockets; purple, hole pockets.

Previous theoretical and ARPES studies of the bismuth (111) surface states have identified three types of Fermi surface: a gamma-point electron pocket, a six-fold degenerate hole pocket and a

set of electron pockets near the M point (Figure 5.2.2f)[51,99]. Landau level features have been observed only by STM and were ascribed to the gamma electron pocket and the oblong hole valleys[46,47]. The pocket sizes we observe are comparable to these previous studies, but it is surprising that all the pockets exhibit similar gate couplings despite large expected differences in their degeneracies. The origin of the change in the hole pocket size at fields above 8 T is also unknown (Figure 5.2.2c).

Transport is differentiated by measuring contributions from the top and bottom surfaces, while STM and ARPES probe only the top. Generically, asymmetries between the surfaces are expected due to both the device structure and the applied electric fields. In the 13 nm device, we do not observe any splitting induced by the back-gate, suggesting that the surfaces are coupled due to proximity. Instead, we observe magnetic-field-induced splittings of the Landau levels at 11 T (Figure 5.2.2c, yellow lines), which can arise from exchange-induced nematicity[47]. By contrast, in the 92–106 nm device (Figure 5.2.2d), we observe clear gate-induced splitting of the electron-pocket Landau fan, resulting in two sets of oscillations with applied gate voltage, one strongly gate dependent and the other independent of gate. We ascribe these oscillations to the decoupled top and bottom surface states, where the bottom surface couples more strongly to the back-gate and screens the electric field from reaching the top surface. This demonstrates how the surfaces of thin bismuth crystals intrinsically support independently controllable 2D systems.

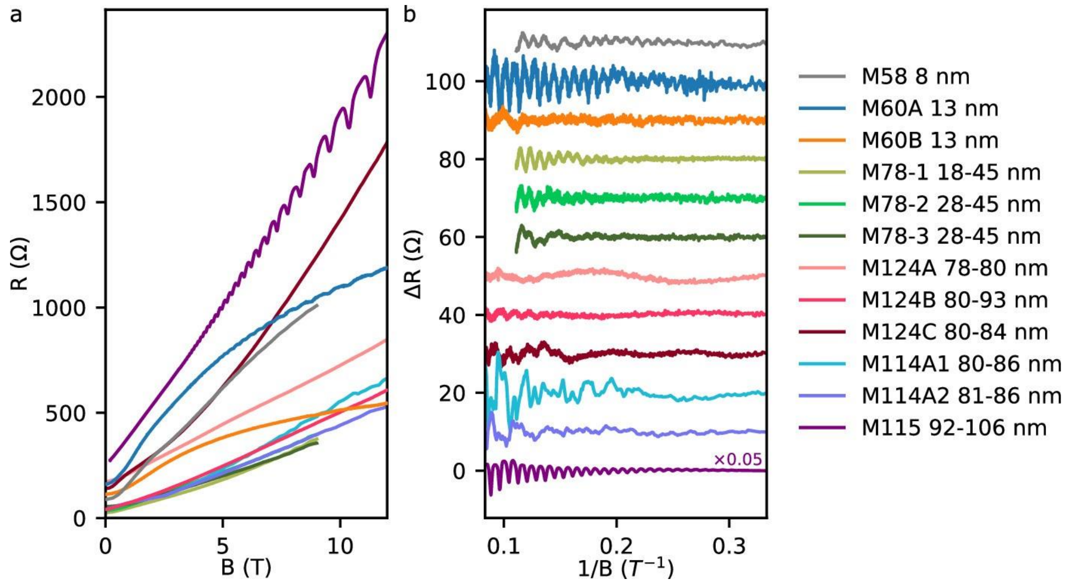

Figure 5.2.3 Field-dependent transport measurements from various devices. a, Resistance as a function of magnetic field. b, Quantum oscillations in R(1/B) under 12 T, calculated by subtracting a smoothed background. Sample with a nonuniform thickness is labeled with a range.

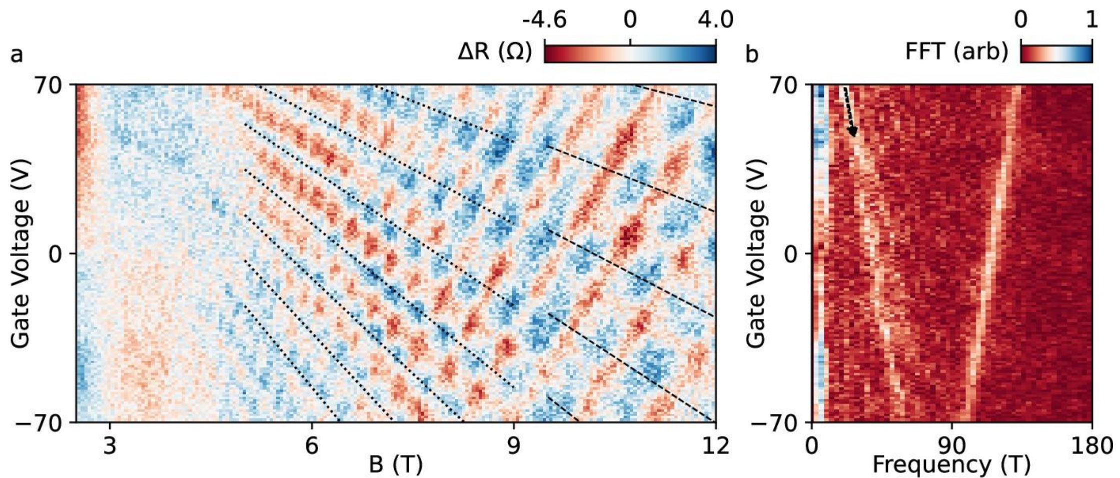

Figure 5.2.4 Quantum oscillations measured in the rough 13 nm device. a, Quantum oscillations measured as a function of gate voltage and magnetic field for the rough 13 nm sample (1.1 µm x 2.1 µm) at 1.5 K. Same device as appears in Figure 5.2.1. The amplitude of the quantum oscillation is much smaller in comparison to the flatter sample. b, FFT calculation of the quantum oscillation of the sample. Unlike the flat sample, we observe only one dominant hole oscillation.

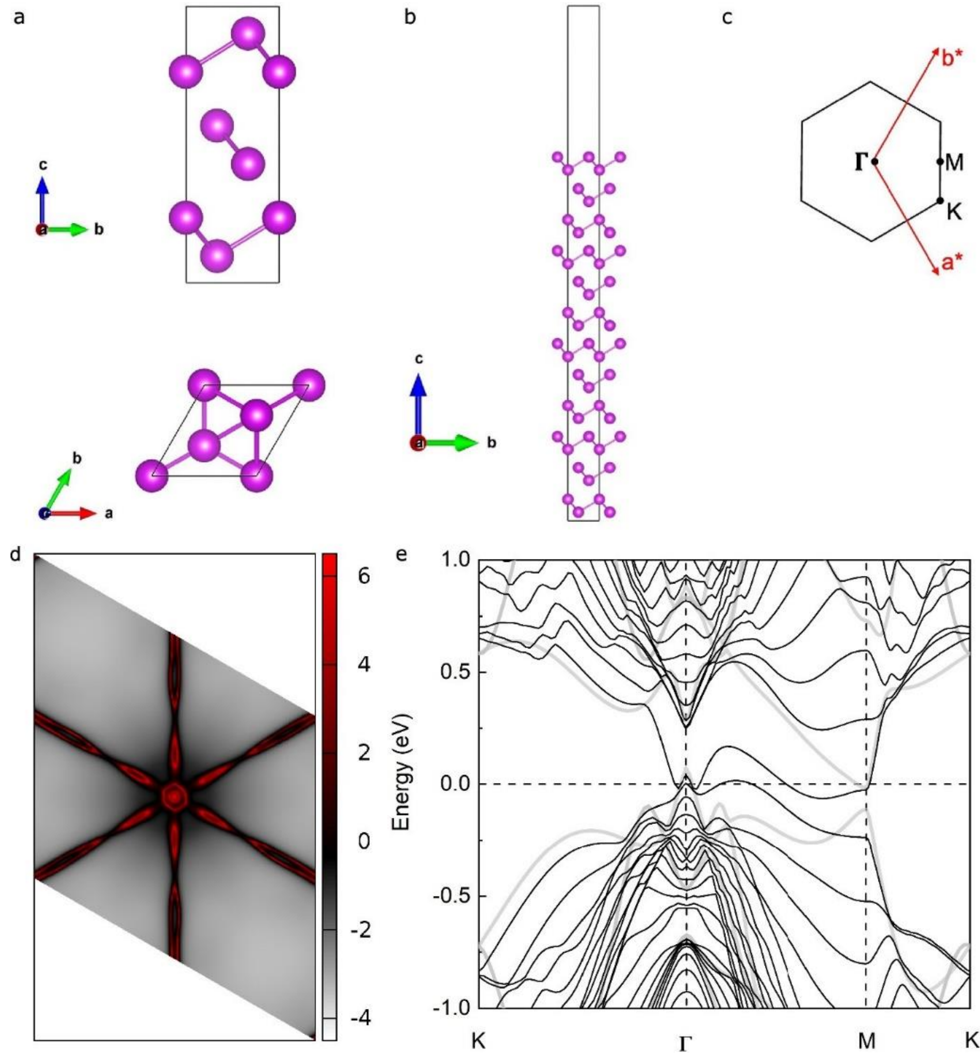

Figure 5.2.5 DFT calculations of the lattice structure, Fermi surfaces, and band structure for 12-bilayer bismuth. a, Lattice structure of the bulk bismuth (111) for orientation aligned with the c-axis. The lattice constants are a = 4.57 Å, c = 11.75 Å and the Bi bond length is 3.10 Å. The intra-bilayer height is 1.63 Å and inter-bilayer spacing is 2.29 Å. b, Lattice structure of 12 bilayer bismuth with two (111) surfaces. After relaxation, the average of the intra bilayer height is 1.50 Å and inter bilayer spacing is 2.13 Å. c, The 2D first Brillouin zone of bismuth (111). d, Fermi surface at kz = 0, calculated using WannierTools[102] with a dense 201 × 201 × 1 k mesh, based on the tight-binding Hamiltonian obtained by employing maximally localized Wannier functions (MLWFs) method using WANNIER90[103] with initial projections to Bi-p orbitals. e, Band structure with Fermi surfaces at 0 eV. This plot is used as the basis of the Fermi surface schematic in Figure 5.2.2f.

5.3 Metal-semiconductor parallel conduction model fit to the temperature dependent resistance

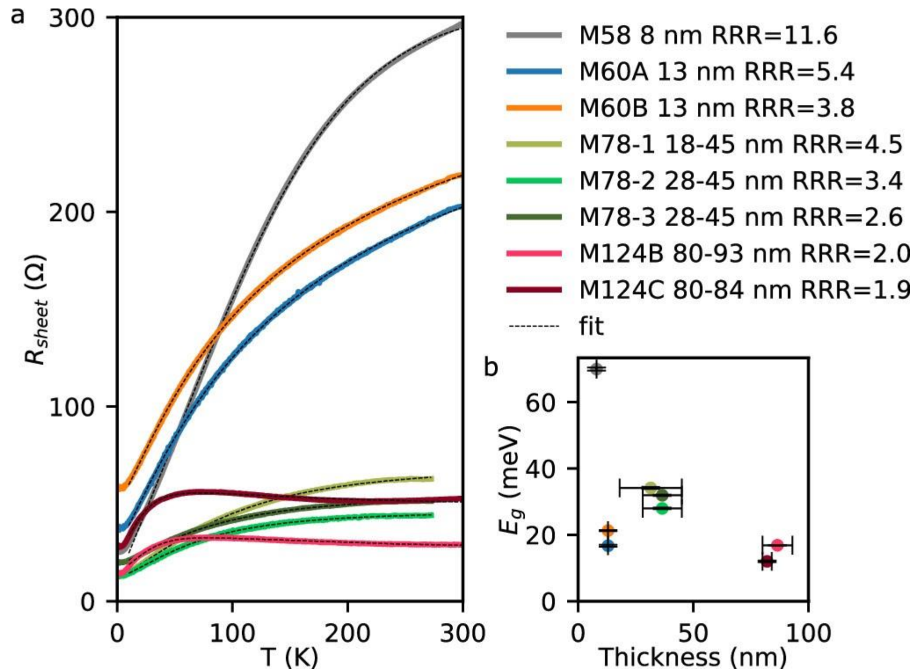

Figure 5.3.1 Temperature-dependent transport measurements of various devices, plotted in designated colors. a, Sheet resistance as a function of temperature. b, Fitted bulk gap as a function of device thickness, averaged from the minimum and maximum thicknesses of each device. Vertical error bar denotes the standard deviation of the fitted bulk gap. Horizontal error bar denotes the range of the thickness of each device.

Figure 5.3.1 shows the temperature dependence resistance measurements on various devices. We fit these data to a resistance model which consists of metallic conduction and activated conduction in parallel, where R_0 is the residual resistance, a is the metallic dependence prefactor, G_1 is the semiconducting dependence prefactor k, E_g is the bulk gap, k_B is the boltzmann constant[19].

$$R = [(R_0 + aT)^{-1} + G_1 exp(-\frac{E_g}{2k_B T})]^{-1}$$

The fitted curves are plotted as dashed lines on top of the sheet resistance in Figure 5.3.1a. The fitted parameter E_g is plotted as a function of device thickness in Figure 5.3.1b.

5.4 Two-carrier model fit to the magnetoresistance

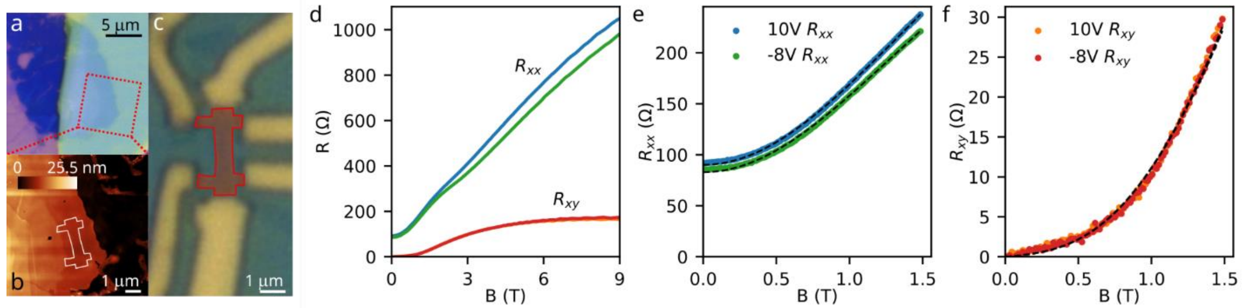

Figure 5.4.1 Magnetic field-dependent measurement of the longitudinal resistance (R_{xx}) and the transverse resistance (R_{xy}) of a 8nm flat device at two different back gate voltages. a, Optical image of the bismuth where this device is fabricated. b, AFM image of the area marked out in a. c, Optical image of the fabricated device. d, R_{xx} and R_{xy} plotted as a function of magnetic field up to 12 T. e, Two-carrier model fit result under 1.5 T plotted on top of R_{xx}. f, Two-carrier model fit result under 1.5 T plotted on top of R_{xy}.

We are able to apply the semimetal two-carrier model[104] on the longitudinal (R_{xx}) and transverse resistance (R_{xy}) (Figure 5.4.1d) of M58, a flat 8 nm device (Figure 5.4.1a-c). We corrected the R_{xy} data by subtracting the 0-field resistance, because we did not obtain resistance in the negative field to symmetrize the data.

$$\rho_{xx} = \frac{1}{e}\frac{n\mu_n + p\mu_p + \left(n\mu_p + p\mu_n\right)\mu_n\mu_p B^2}{\left(n\mu_n + p\mu_p\right)^2 + (p-n)^2\mu_n^2\mu_p^2 B^2}, \qquad \rho_{xy} = \frac{1}{e}\frac{\left(p\mu_p^2 - n\mu_n^2\right)B + (p-n)\mu_n^2\mu_p^2 B^3}{\left(n\mu_n + p\mu_p\right)^2 + (p-n)^2\mu_n^2\mu_p^2 B^2}$$

Where n and p are the carrier density of electrons and holes, μ_n and μ_p are the corresponding mobility. We fit the R_{xx} and R_{xy} data under 1.5 T to the model, and the fit result is plotted on top of the data in Figure S11e and f, and the fitted parameters are listed below.

Table 5.4-1 Carrier densities and mobilities from the two-carrier model fit.

Gate Voltage (V)	n (cm^{-2})	p (cm^{-2})	μ_n (cm^2/Vs)	μ_p (cm^2/Vs)
10	7.63e+12	1.72e+13	1.22e+04	8.67e+03
-8	7.99e+12	1.84e+13	1.26e+04	8.84e+03

5.5 Effect of bismuth oxide on device transport measurements

The vdW-molded bismuth is protected from air during the growth process. However, the device nanofabrication process exposes the bismuth to some oxygen. Bismuth forms a self-limiting oxide layer about 1-3 nm in thickness as we discussed in Methods, and we can see signs of a crystalline oxide layer in our TEM measurements. As such, likely all of our electronic measurements of clean quantum oscillations in the bismuth surface states are coming from electrons near this oxide layer. Given the high quality of the resulting transport data and the agreement with STM and ARPES studies, we conclude that this oxide layer does not

significantly degrade transport. Instead, it seems that the surface roughness is the most important factor for thin bismuth transport. These observations are also supported by DFT calculations, which show that the bismuth surface state is barely affected by the presence of an oxide layer[99].

5.6 Effect of domains and terraces on device transport measurements

In this work, we measure 12 different devices that vary in crystal uniformity. Despite wide variations in thickness and terrace structure, we observe qualitative consistent features such as larger RRR values compared to MBE-grown films, as well as clear quantum oscillations that have been previously unrealized in bismuth thin film transport. Here, we discuss in more detail the role of crystal nonuniformity in our electrical device characterization, specifically focusing on the effects of crystal domains and surface irregularities such as terraces.

Due to concerns for beam-induced damage and contamination, we do not perform EBSD or TEM diffraction measurements on our devices. As such, we cannot completely exclude the possibility of a domain wall in the device channel. But, our nanofabrication procedure is effective at minimizing domain walls. The vdW-molding process produces thin bismuth flakes with large domain sizes, typically at least $(4\ \mu m)^2$ in size, and some flakes are single crystal over 20 μm dimensions. Therefore, even random placement of a 1 μm x 3 μm device will result in few to zero domain walls. To further minimize domains, we target regions that have flat and wide terraces. From our comparison of EBSD and AFM data, we observe that domain walls are

clearly visible in AFM as topographic features (Figure 3.3.1). In this way, we can produce devices that are single-crystal with very high certainty.

Of the 12 devices we present, 2 of the devices are made in a single flat terrace, and hence very likely to be single-crystal. These are the flat 8 nm and 13 nm devices that appear in Figure 5.2.1e,f,g and Figure 5.2.2c,e. We measure an additional 10 devices that are typically larger and with more non-uniform surfaces, primarily due to multiple terraces steps. Due to the surface non-uniformity, it is likely that some of these devices contain a few domain walls. As mentioned above, the non-uniform devices show the same qualitative features as the highly-uniform devices. Therefore, the presence of domain walls and terraces does not critically affect our conclusions.

These observations are consistent with the expected transport effects of a domain wall or terrace. A rotational domain wall in a (111) bismuth crystal is expected to behave as a 1-dimensional (1D) metallic wire[1,16,101]. A domain wall that runs parallel to the device channel will have little effect on the conductance as it is a small fraction of the channel width and is shunted by parallel conduction through the metallic surface. From STM studies, we estimate that the domain wall has a width of 10 nm as compared to the ~1 μm typical width of our devices[45]. When orientated perpendicular to the channel, the domain wall will act as a source of scattering as the domains have different in-plane orientations. This will impede electronic transport through the surface state and add extra resistance to the device. Terrace steps on the surface will behave similarly to domain walls, in that they should host 1D metallic modes[45], but should provide less resistive scattering to transverse transport when the crystal orientation is preserved across the terrace.

To summarize, the likely effect of sparse domain walls and terraces in our devices is to increase resistive scattering and, in this regard, behave similarly to other random sources of disorder, such

as impurities or rough crystal edges. Disorder is expected to decrease the measured RRR value by increasing the residual resistivity at base temperatures. This is clearly observed in the comparison of the flat and rough device in Figure 5.2.1. It is also consistent with the highly-uniform devices exhibiting a greater improvement in RRR values as compared to the non-uniform devices.

Likewise, resistive scattering from disorder, including domain walls and terraces, will reduce the amplitude of quantum oscillations[105], but will not change the frequency of the quantum oscillations themselves. Domain walls and terraces cannot produce quantum oscillations, as they are too narrow to support cyclotron motion. Furthermore, quantum oscillations are not sensitive to the in-plane rotations that differentiate the domains, as this simply causes an overall rotation of the electronic structure which preserves the size of the Fermi surface. Hence, a device that is made up of a few domains with different in-plane orientations will have a similar pattern of quantum oscillations as a single crystal device. We can estimate the length scale for scattering from the B = 3 T magnetic field where quantum oscillations typically onset, using the equations for the quantum scattering time $\tau = m_{eff}/eB$ and cyclotron diameter $d = 2m_{eff}v_F/eB$, where we use $m_{eff} = 0.16\, m_0$ and $v_F = 4.7e5\, m/s$[46]. This results in a 0.3 ps quantum scattering time that corresponds to a 280 nm cyclotron diameter. This is close enough to the ~1 μm width of most of our devices that scattering from the device edges is likely an important limiting factor.

Chapter 6

Conclusion

To summarize, we demonstrate a method to synthesize ultrathin and flat bismuth crystals within a nanoscale vdW mold. The confined bismuth exhibits gate-tunable quantum oscillations that originate from the (111) surface states. The bismuth surface bands are known to feature spin–momentum locking, which can be used to electrically generate spin polarizations[1,7,18,106]. Moreover, vdW-molded bismuth can shed light on the transport behavior of intrinsic helical edge modes that have been observed in STM[15].

Our mechanical modelling and atomistic simulations suggest that vdW molding offers a route to 2D bismuthene, which is predicted to be a large-gap 2D topological insulator[12,19]. Beyond bismuth, we anticipate that the vdW-mold technique will be applicable to other soft materials, enabling an approach combining ultrathin vdW and non-vdW materials.

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