UNIVERSTIY OF CALIFORNIA, SAN DIEGO

Ge and Si based nanowires/nanotubes synthesis and their applications in wearable device, biochemical sensor, and thermoelectronics

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy

in

Doctor of Philosophy in Materials Science and Engineering

by

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2015

The Dissertation of Soonshin Kwon is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Dedication

To my loving wife Sohyun and my family,

without whom this dissertation would not be possible.

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Publications

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(6) Soonshin Kwon‡, Zack C. Y. Chen‡, Hyunwoo Noh‡, Ju Hun Lee, Hang Liu, Jennifer N. Cha, and Jie Xiang, “Selective Functionalization and Loading of Biomolecules in Crystalline Silicon Nanotube Field-Effect-Transistors”, Nanoscale, 2014,6, 7847-7852 (‡ equal contribution)

(5) Ji-Hun Kim, Zack C. Y. Chen, Soonshin Kwon, and Jie Xiang, "Three-Terminal nanoelectromechanical Field Effect Transistor with Abrupt Subthreshold Slope", Nano Letters, 14, 1687–1691 (2014).

(4) Ji-Hun Kim, Zack C. Y. Chen, Soonshin Kwon, and Jie Xiang, "Steep Subthreshold Slope Nanoelectromechanical Field-Effect Transistors with Nanowire Channel and Back Gate Geometry", 2013 Device Research Conference (DRC), Notre Dame, IN, June 23-26, 2013.

(3) Ji-Hun Kim, Zack C. Y. Chen, Soonshin Kwon, and Jie Xiang, “Steep Subthreshold Slope Nanowire Nanoelectromechanical Field-Effect Transistors (NW-NEMFETs)”, 3rd Berkeley Symposium on Energy Efficient Electronics Systems, Berkeley, CA, Oct 28-29, 2013.

(2) Soonshin Kwon, Zack C. Y. Chen, Ji-Hun Kim, and Jie Xiang, "Misfit-guided self-organization of anticorrelated Ge quantum dot arrays on Si nanowires", Nano Letters, 12, 4757–4762 (2012)

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ABSTRACT OF THE DISSERTATION

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by

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Doctor of Philosophy in Materials Science and Engineering

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Si and Ge nanowires and their heterostructure have been received widespread attention in various research fields because of the inherent advantages and the major historical roles played by these materials in contemporary microelectronics. From decades of research on two materials, integrated in-depth knowledge on the nature of material properties and manufacture process provide useful guidelines to design nanostructures and related devices with increased structural and functional complexity.

In this dissertation, synthesis and applications of Ge and Si based nanowires and nanotubes in electronics, photonics, biochemical sensor, and thermoelectrics are discussed.

In chapter 2, self-organizing characteristics of misfit-guided Ge quantum dots growth on Si core nanowires are systematically demonstrated. Unique Ge quantum dots growth mode caused by strain supperlattice along the Si nanowire backbone can be controlled by the choice of core diameter. Such strain-guided growth opens up a new avenue towards growth of self-organized nanoscale heterostructures.

In chapter 3, fundamental study of crystalline Si nanotubes properties as a platform for electrically and biochemically functional devices is demonstrated. Four-probe current-voltage characterization of precisely probe the inherent electrical properties of crystalline Si nanotubes. Selective functionalization and loading of fluorescence dye and biomolecule inside the core of nanotubes are demonstrated lighting the potential as in-vivo drug carrier.

In chapter 4, characterization of thermal transport behavior of crystalline and amorphous Si nanotubes are presented. Ultra-low thermal conductivity of crystalline nanotube below the amorphous counterpart is observed. Study on elastic properties of those nanotubes reveals new possible control mechanism of phonon transport behavior.

In chapter 5, fabrication of optical polarizer by printing Ge or Ge/Si core/shell nanowires into highly compacted and ordered fashion is presented. Transmission measurement under various mechanically stressed circumstances reveals potential of nanowire polarizer as high flexible and stretchable optical filter.

Chapter 1: Introduction

1.1. Introduction

Si and Ge nanowires and their heterostructure have been received widespread attention in various research fields because of the inherent advantages and the major historical roles played by these materials in contemporary microelectronics.[1-4] From decades of research on two materials, integrated in-depth knowledge on the nature of material properties and manufacture process provide useful guidelines to design nanostructures and related devices with increased structural and functional complexity. For example, 4.2% of lattice mismatch between Ge and Si provides stain engineered feature which allow tailoring morphology and electrical band structure.[5, 6] In addition, relatively low eutectic points of Si and Ge with several metal catalyst c.g. gold or aluminum, allows robust synthesis method based on vapor-liquid-solid mechanism leading to single crystalline structure and flexibility in controlled growth of complex nanostructure. Moving further, physical properties stem from quasi-one dimensional nanostructure draws interest in numerous applications as biological and chemical sensors, thermoelectrics, photonics, and nanoelectronics. Such features include: (1) Large surface area with nanoscale volume comparable to the sizes of targeted biological and chemical species for detection provides high signal transduction. (2) High absorption and tunable emission properties of nanowires leads to high sensitive photodetector, solar cell, and laser applications. (3) Electrical confinement along the axial direction enables high electrical conductance. (4) Enhanced phonon scattering thanks to the size of the nanowire introduces new era of thermal material management

and thermoelectrics. (5) Mechanical softness from small size in radial direction allows the material easily adopted into flexible/stretchable devices. The scope of this dissertation covers following topics: (1) p-n zigzag Si nanowires, (2) assembly of Ge nanodomes on Si nanowire backbone. Before delving into the details, it is prudent to briefly review the basics of nanowire synthesis and their applications in conjunction with the topics of this thesis.

1.2. Synthesis of Si, Ge, and Si/Ge heterostructure nanowires

The first observation of anisotropic one-dimensional structure of Si was discovered by Holonyak et al. and Greiner et al. dates back to 1961.[7] A few years later, Wagner et al. proposed whisker growth method in more systematic way named as 'vapor-liquid-solid (VLS)' by using gold nanoparticles decorated on Si substrate to catalyze Si whiskers growth.[8] From VLS method, Wagner was able to successfully grow 100~500 nm size of free standing Si whiskers out from Si(100) substrate by flowing Silicon tetrachloride precursor at 950 C into the reactor. Although several research on Si and Ge whiskers where published[9], the major blooming in this research field was triggered by C. M. Lieber at late 1990's. Also, the terminology 'nanowire' was widely used from this moment. Series of methods to grow nanowires from Si and Ge were developed c.g. chemical vapor deposition (CVD)[3], laser ablation[10], supercritical fluid[11], molecular beam epitaxy (MBE)[12], top-down etching.[13] Among them CVD is the most widely used method because of its simple preparation of growth sample, high crystalline structure of material, and opportunity to change composition and structure in in-situ steps. Focusing on CVD method, there are in

general five major elements which affect critically on the growth of nanowires: growth substrate, temperature, reactant gas phase precursor, carrier gas, and seeding material. Depending on the choices of such conditions various types of nanowires with different size, length, orientation, cross-section, doping profile, and heterostructure are possible.

Vapor-liquid-solid and vapor-solid-solid (VSS) are the two most famous mechanisms known for Si and Ge nanowires growth. In general, for both mechanisms, catalytic materials such as Au or Al metal nanoparticles are used to lower the surface energy on localized sites, serving as nucleation of nanowire growth. For VLS mode, when vapor phase precursors are introduced to catalytic materials into the reactor chamber, metal-semiconductor (Si, Ge) alloy of liquid droplets are formed on the substrate at much lower temperature above the eutectic point of 360 C compare to individual materials which have melting points at near 1000 C. This fact indicates that such method is very promising tool to create high crystalline semiconductor materials with much less energy which is favorable for many electrical and optical applications. Widely used precursors for Si are silane, disilane, silicon chloride and for Ge are germane and digermane.[14, 15]

The more supply of source material, the higher concentration of source atoms can be accumulated in the metal alloy. Continuous supply of source molecules near to the alloyed droplets can push them to reach supersaturation which leads to precipitation and crystallization of Si or Ge atoms on the lowest energy site at liquid solid interface. This process lift the liquid droplet displaced from the substrate shaping source material into free-standing one-dimensional structure. During the growth, the catalytic droplet floating on top of the nanowire defines the shape and diameter of the

nanowire as it grows. In here choice of substrates are not necessarily have to be crystal although the control of growth direction heavily depends on the crystallinity and surface state of the substrate.

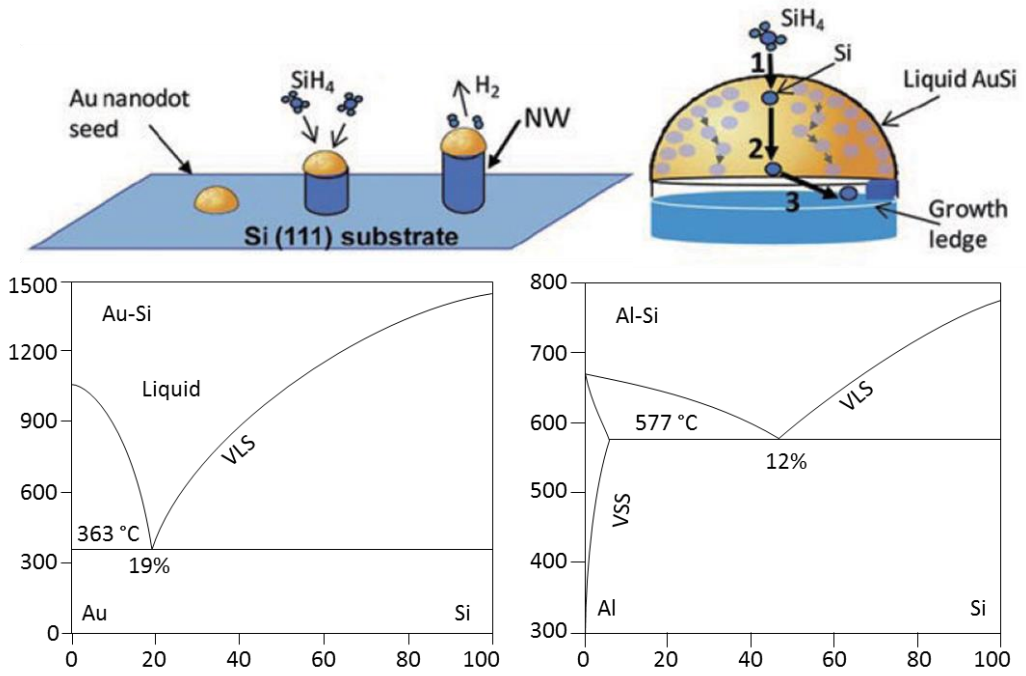

Figure 1.1. Schematics of VLS growth mechanism for Si nanowire synthesis from a liquid Au-Si particle. Enlarged view on the left shows three kinetic steps; 1) silane decomposition, 2) diffusion of Si atom through liquid droplet, and 3) crystallization of Si atom at liquid-solid interface. Below two are representative phase diagrams of Au-Si and Al-Si presenting possible VLS and VSS growth modes and minimum growth temperature.[16, 17]

Because nanowire growth is heavily depend on the role of the catalyst, careful selection of its material is very important for producing high quality nanowires as intended way. Numerous research efforts have focused on identifying the thermodynamic and kinetic role of catalyst as well as search new material as alternatives. To work as catalyst, non-horizontal phase boundary between liquid alloy and solid Si or Ge phase is required to activate VLS process. The eutectic temperature

which is the lowest melting temperature of a mixture of components is considered as minimum growth temperature. Au is the most widely used material for catalyst because of several following reasons: (1) relatively high Si concentration of 19% and Ge of 26% compare to other metal candidates. This indicates Si or Ge is easier to dissolve in metal alloy costing with less energetic cost thus requires less precursor pressure to grow nanowires. (2) Low vapor pressure (7.5×10^{-9} torr at 800 ℃ for Si) even at high temperatures along with decent amount of surface tension allows stable droplet-nanowire system during the long period of growth. Unfortunately, regardless of bundles of advantages, the fact that Au is a source of deep level defects in Si and as impurity of nanowires, it is considered incompatible with industrial standard for electronics and photonics. Such situation has motivated researchers to find new non-Au alternatives for catalyzing nanowire growth. Wide range of non-Au catalysts were demonstrated in case of Si (Ag[8], Al[18], Bi[19], Cd[20], Cu[21], Fe[22], Ga[23], In[24], Ni[25], Pd[26], Pt[27], Ti[28], Zn[29]) and also for Ge (Mn[84], Ni[85], Ti[86], Cu[87]). From various choices of catalyst with different phase diagram with Si and Ge, the way to design the nanowire depending on the purpose has diverse in wide range, for example, by using Al as catalyst one can expect both VLS and VSS growth. Especially, low Si solubility of 2% for VSS growth provides opportunity to design sharp interface when designing heterostructure of Si and Ge.

Studies to understand growth kinetics and thermodynamics to achieve better control of nanowire synthesis have been made extensively. Diameter, tapering, kinking, and growth rate are the fundamental aspects to understand such nanowire growth properties. Growth rate of nanowire depends on several growth parameters:

temperature, pressure, diameter, precursor, and dopant. It is well known that increasing temperature enhances the reaction process and several reports show mm long Si nanowires grown at near 1000 C.[30] Kinetics studies of Si nanowire growth show that effect of pressure and temperature are linearly proportional to the growth rate,[31] while, diameter shows more complex relation with growth rate depending on the other growth parameters.[32] Also, the effect of precursor choice on the growth rate has been demonstrated that at temperature around 400 ℃, disilane can achieve much higher growth rate of 31 um/min compare to silane of 1~2 um/min.[33] Considering doping of nanowire, adding diborane can affect the growth rate when silane is used as precursor by enhancing dissociation rate of silane induced by diborane.[34]

The distinctive merits of Si and Ge rise when two materials are integrated into heterostructure systems. During the VLS or VSS growth either axial or radial heterostructures can be easily realized by simply changing precursor and proper adjustments of growth parameters such as temperature and pressure. Depending on the choice of core material, two types of radial heterostructures are available resulting in totally different morphology and electrical property. Because of larger lattice constant (4.2% of mismatch) of Ge against Si, when two materials create interface, Ge layer is subjected to compressive strain while Si layer experience tensile strain. This result in core/shell structure with smooth surface when Ge serves the core material while the opposite case appears as rough shell with Ge nanodomes arranged along the Si core. Derivative from Ge/Si core/shell structure is also possible by utilizing weakness of Ge compare to Si under certain chemical reaction such as hydrogen peroxide reduction and solubility in water which offers synthesis of Si nanotube by selectively removing

Ge core.[4] Besides radial structure, heterostructure formed along the axial direction of nanowire can provide another root to integrate multiple functions in a single nanowire.[35] The following sessions will briefly overview applications of Si and Ge based nanowire systems.

1.3. Applications of Si and Ge related nanowire system

1.3.1. Nanowire electronics

The relentless scaling in CMOS technology leads to searching new materials and structures to continue successful progress in semiconductor device development and Si nanowire as a bottom-up solution has been considered as a promising candidate. During the past decades, Si and Ge nanowire FETs in either lateral or vertical fashion have been successfully demonstrated showing high performance for both n- and p-type by properly doping the nanowires during the synthesis. More fascinating properties can be illuminated when Ge and Si are combined into heterostructure. In case of Ge/Si core/shell nanowires, due to the large band offset on valence band between Si and Ge, resultant Fermi level pinning creates a highly concentrated valley of holes along the Ge core. Besides core region, energy band leveling at Si shell effectively prevent the surface pinning and creates negative Schottky contacts with metal contact junction. Such unique characteristics lead to ultrahigh-performance as p-type transistor devices demonstrating high operation speed indicated by intrinsic gate delay of 2 THz[36]. Such one-dimensional hole gas system has been used to demonstrate various electrical phenomena including ballistic transport, coulomb blockage, and tunable quantum dots.[37-39] Furthermore, combining with their high mechanical flexibility, electronics on non-conventional flexible substrates such as plastic sheets are demonstrated as well as nanoelectromechanical field effect transistors which utilize the elastic movement of nanowire channel to operate the device with very steep subthreshold slop.[40, 41]

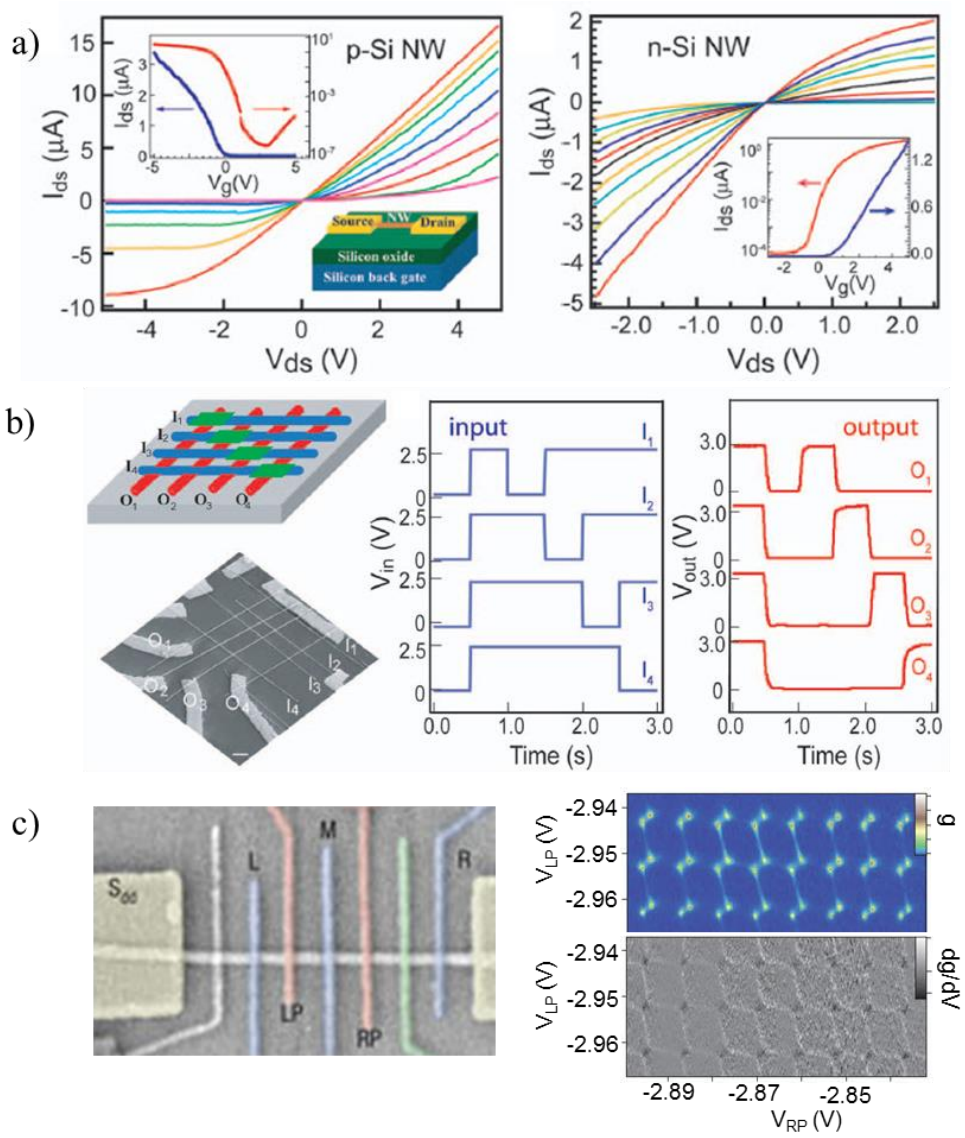

Figure 1.2. Electrical application of Si nanowires. a) High performance p- and n-type single Si nanowire transistors.[42, 43] b) Si nanowire cross array integrated into decoder and regarding input and output performance.[44] c) Ge/Si core/shell nanowire double quantum dots with multiple gate electrodes designed for charge detection sensor from Coulomb blockage transport.[38]

1.3.2. Nanowire photonics

Favor of group IV photonics is traditionally driven by the low-cost and high quality of Si wafers, and mostly compatibility with the mature Si IC manufacturing. As a photonic material, despite the low quantum efficiency due to indirect band gap, merit such as large index contrast between waveguide and its surroundings, c.g. Si (n=3.45) and SiO2 (n=1.45), allows scaling of photonic devices down to sub-100 nm size with high optical intensity which also can contribute to nonlinear optical interactions likely Raman effect[45], Kerr effect[46], two-photon absorption[47], and free-carrier dispersion[48] at chip-scale level. Moreover, guided by ongoing advance in the synthesis and fabrication methodologies, Si and Ge in nanowire platforms are realized as promising optical materials enriched with compositional and structural diversity. High interest as optical material is also triggered by several following factors: (1) large surface to volume ratio causing higher light sensitivity than their bulk counterparts, (2) elongated one dimensional anisotropic shape as waveguide of light propagation, (3) Tuning optical guiding modes by control of cross-sectional dimension, (4) ease to synthesis radial heterostructures creating p-n or Si/Ge junctions. Driven by such fascinating features, series of studies on Si and Ge nanowires as optical materials have been demonstrated such as phototransistor, photovoltaic, tunable waveguide, antireflection coating, and optical switch.[49-52]

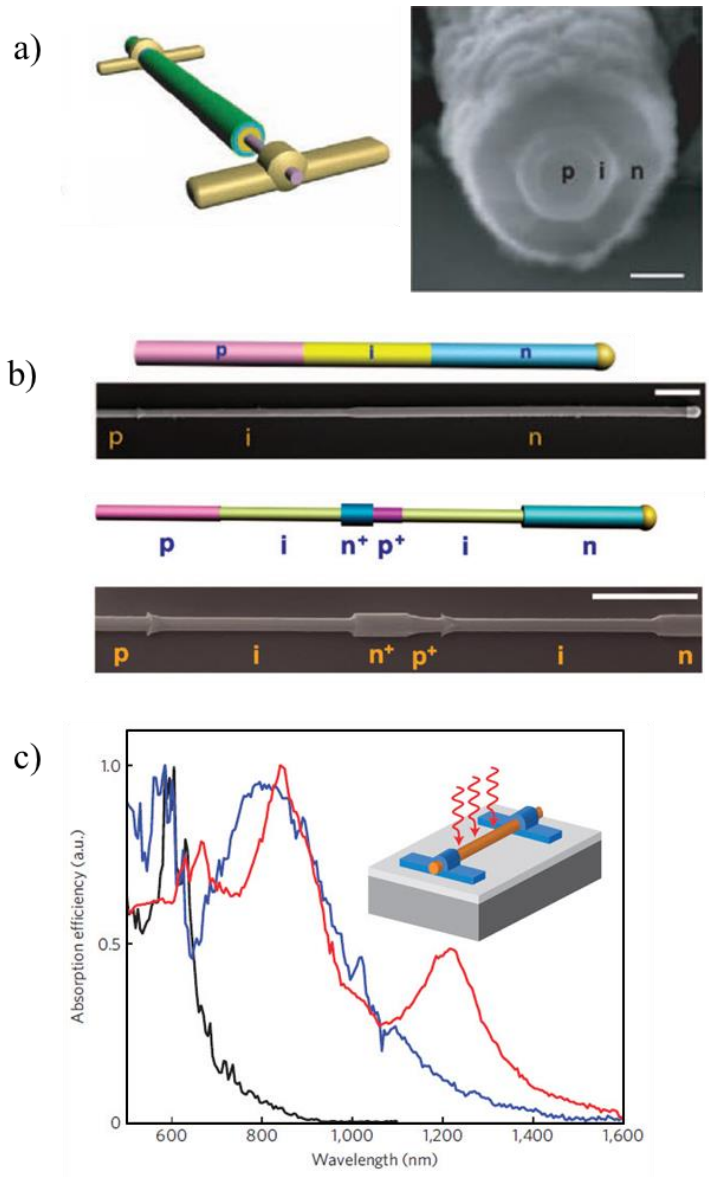

Figure 1.3. Applications of Si and Ge nanowires in photonics. a) and b) show that single nanowire Si nanowire solar cell with either radial and axial p-n doping.[49, 53] c) Size dependent light absorption of Ge nanowire indicating multicolor phtodetection.[54]

1.3.3. Application in biochemical sensors

Si nanowires have proven their potential as ultrasensitive, direct, label-free detection of biological and chemical species.[55-59] Such high sensitivity comes from large surface to volume aspect ratio and high performance of NW-FETs enables the detection of single biochemical molecules such as virus. Generally, biochemical detection system using nanowire as active material is designed from field effect transistors with surface functionalized nanowire used as the electrical conduction channel. Based on this scheme, NW-FET sensors can also be miniaturized and integrated into electrically addressable array of sensors for real-time detection of multiple disease marker proteins at the femtomolar level. To work as biochemical sensors, decorating nanowire surface with probe molecules is required to recognize specific target molecule. Three approaches, electrostatic adsorption, covalent binding, and joule heating are used to attach probing molecules on the surface of Si nanowires. Electrostatic adsorption method uses attractive force between oppositely charged adsorbing ionic solute and adsorbent. For example, DNA strand can be electrostatically adsorbed onto the Si nanowire surface passivated by amine-terminated organic monolayer.[60] The covalent binding method, in general, utilizes silane chemistry on the native oxide of Si nanowires. Popular choices of linker molecules are 3-aminopropyltriethoxysilane (APTES) which expose amino groups on the nanowire surface[61] and 3-mercaptopropyltrimethoxysilane (MPTMS) to yield thiol (SH)-termination.[62] Other reported alternatives are 3-(Trimethoxysilyl)propyl aldehyde (APTMS) resulting in an aldehyde-terminated Si nanowire[63] and phosphonate derivatives are known to functionalize Si nanowire surface with hydroxyl

groups.[64] Such decorations can be used to immobilize peptide nucleic acid (PNA), DNA, and antibodies attached to the nanowire channel causing electrical conductance change.[65] Such works offers potential for powerful sensors that could significantly improve healthcare in the future.

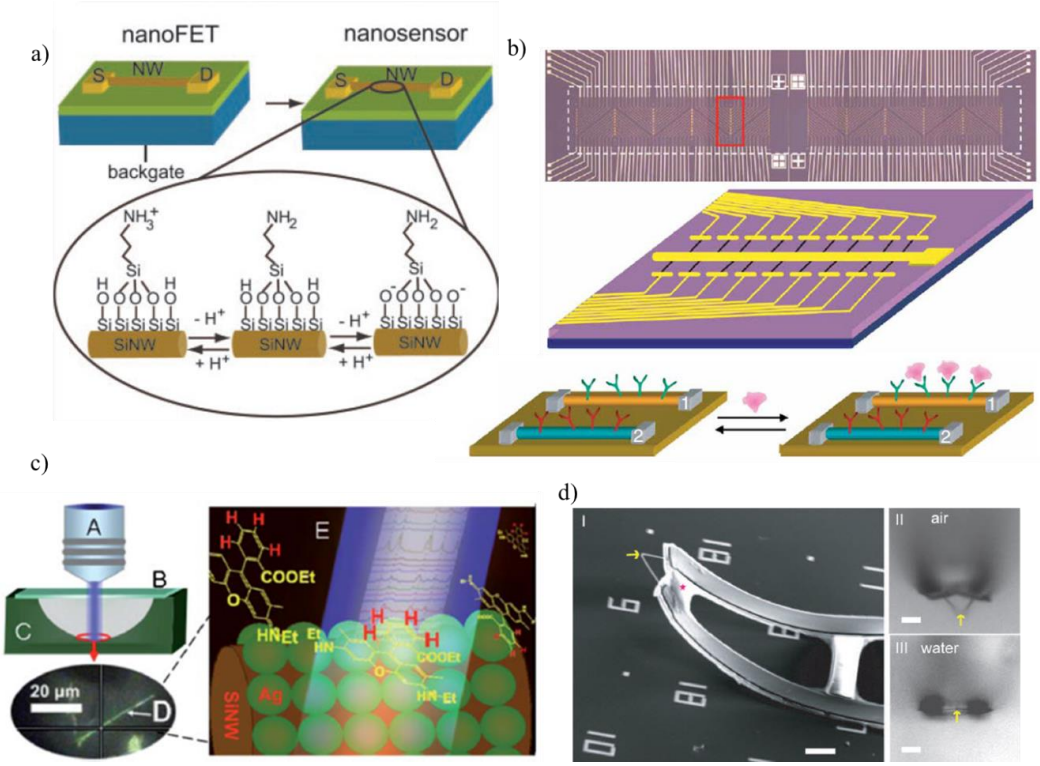

Figure 1.4. Applications of Si nanowire in biochemical sensors. a) Surface functionalized single Si nanowire field-effect transistor as high sensitivity biochemical sensor.[63] b) Multiplexed senor using Si nanowires with difference bio-markers.[66] c) Optically induced detection of biochemical sensor.[56] d) Si kinked nanowire as intracellular bio-probe.[67]

1.3.4. Nanowire for thermal management and thermoelectrics

Understanding and control of thermal transport in nanoscale become increasingly important in electronics and photonics because the continuous integration and downscaling of devices and circuitries inevitably result in dramatic increase in power consumption per unit area and associated heat density of the system.[68, 69] Such circumstance leads to the demands for more efficient heat managements in electronics packaging, cooling, and heat dissipation of materials to improve the reliability and prevent premature failure. For example, excessive power consumption by supercomputer, which gain more popularity due to the growing needs of data processing in larger scale such as cloud computing[70], needs exotic cooling cost to maintain heat dissipation.[71] Reducing interface/junction thermal resistance, increasing the heat convection through the system are the paramount issues that confront the development of electronics and photonics into more integrated fashion.

Another major interest in thermal transport research is recycling heat to electricity mediated by "Seebeck effect" of semiconductor.[72] From the fact that one third of generated energy is wasted as thermal losses[73] accompany with the rapid increase of world-wide energy consumption, building a strategy to recycle waste heat is highly demanding. Such need draw a significant attention to thermoelectric generator (TEG) because of its high reliability and compactness as a solid-state energy converter and carbon-free energy source. Despite of its attractiveness, key challenge that hinders TEG to be widely used in series of applications, e.g, solar energy converters, heat pumps or engines, automobiles,

power plants etc, is due to its low energy conversion efficiency and high module cost. Such circumstances lead to an effort to develop cost-effective thermoelectric materials with higher figure of merit (ZT). Improvement of ZT is directly related to finding optimized leverage of thermoelectric parameters--Seebeck coefficient, electrical conductivity, lattice, and electric thermal conductivity. Since these values are often interdependent in case of conventional bulk materials, decoupling of those parameters to enhance thermoelectric performance was extremely challenging[72, 74] and researches were mostly focused on finding better thermoelectric materials.

Blooming of nanotechnology raises new opportunity by introducing new physical properties and additional engineering capability of materials, for example, thermal conductivity of carbon nanotube[75] or graphene[76] appears 10~20 times larger compare to copper and Ge/Si core/shell nanowires[77, 78] show large reduction in thermal conductivity without sacrifice of power factor thanks to electric and phononic confinement effects. Such merits rely on the modification of charge/phonon transport characteristics by changing dispersion relation of carriers apart from their bulk properties. For example, density of states of one- or two-dimensional systems of electrons reveal totally difference profile introducing new energy occupation of carriers during transport.[79] For thermal transport, phonon spectrum experiences large modification when the structure size of material shrinks down much smaller than the phonon mean free path and become similar to the scale of dominant phonon wavelength. Such phenomena provide new controllability on thermal management and

energy conversion applications using the same material, which was impossible in macroscopic scale.

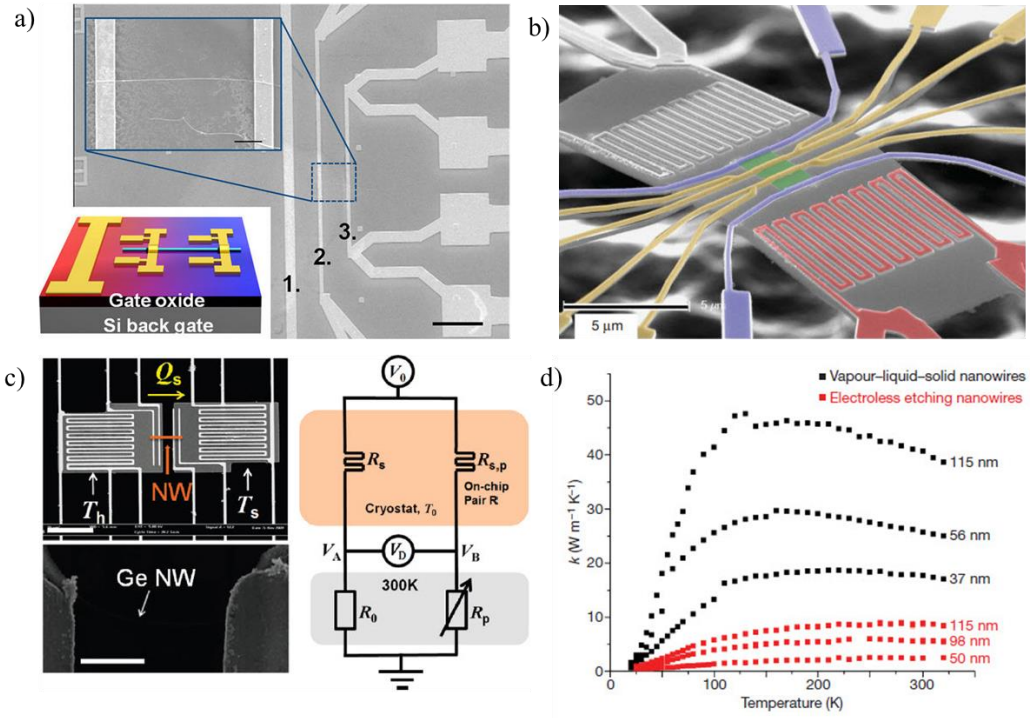

Figure 1.5. Applications of Si and Ge nanowires in heat management and thermoelectrics. a) Thermopower measurement on a) Ge/Si core/shell nanowires with four probes method designed on SiO2/Si substrate[80] and b) Si nanowire using suspended structure.[81] c) Heat transport measurement on Ge nanowire using bridge method.[82] d) Representative results of Si nanowire thermal conductivity displaying the effect of surface phonon scattering.[83]

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Chapter 2: Self-organized and self-limited growth of Ge quantum dot arrays on Si nanowires

Misfit-strain guided growth of periodic quantum dot (QD) arrays in planar thin film epitaxy has been a popular nanostructure fabrication method. Engineering misfit-guided QD growth on a nanoscale substrate such as the small curvature surface of a nanowire represents a new approach to self-organized nanostructure preparation. Perhaps more profoundly, the periodic stress underlying each QD and the resulting modulation of electro-optical properties inside the nanowire backbone promise to provide a new platform for novel mechano-electronic, thermoelectronic, and optoelectronic devices. Herein, we report a first experimental demonstration of self-organized and self-limited growth of coherent, periodic Ge QDs on a one dimensional Si nanowire substrate. Systematic characterizations reveal several distinctively different modes of Ge QD ordering on the Si nanowire substrate depending on the core diameter. In particular, Ge QD arrays on Si nanowires of around 20 nm diameter predominantly exhibit an anti-correlated pattern whose wavelength agrees with theoretical predictions. The correlated pattern can be attributed to propagation and correlation of misfit strain across the diameter of the thin nanowire substrate. The QD array growth is self-limited as the wavelength of the QDs remains unchanged even after prolonged Ge deposition. Furthermore, we demonstrate a direct kinetic transformation from a uniform Ge shell layer to discrete QD arrays by a post-growth annealing process.

2.1. Introduction

In growth of pseudomorphic semiconductor thin film heterostructures, when the top layer grows beyond a critical thickness, large misfit-strain due to lattice mismatch will unavoidably lead to rough surfaces, formation of QDs and as thickness increases, the introduction of dislocations and faults due to strain relaxation[1,2]. These defects are undesirable in electrical and optical device applications as they act as scattering sites, recombination centers, and leakage path. Considerable efforts have been spent minimizing strain relaxation in heterostructure growth.[3-5] In recent years core/shell nanowire (NW) heterostructures have attracted increasing attention as they are more accommodating to high misfit strain than planar thin films without relaxation. The radius of curvature of the small diameter core surface is expected to alleviate the strain in the shell layer, allowing thicker critical thickness for a wide range of coherent shell material growth without formation of dislocation and other defects.[6,7] Indeed, epitaxial core/shell and core/multishell heterostructure NWs of IV, III-V, II-VI and transition metal oxide materials have been successfully synthesized[8-13]. The advent of nanoscale heterostructure semiconductors, such as quantum dots[14,15] and core/shell nanowires[8-10] has provided an unprecedented opportunity towards engineering accurate and scalable devices at an atomistic scale for applications in photonics[11,16], electronics[12,17], and biosensors[18,19].

Still, even with a small diameter nanowire, for very large misfit strain between two materials such as Ge on Si (4.2%), the critical thickness for epitaxial shell growth is no more than a few nanometers[6], beyond which a change in shell morphology is commonly observed. Multiple grain boundaries and roughened surfaces may form due

to strain relaxation, similar to the case on a bulk substrate.[4,20] Interestingly, recent studies on thick Ge shell deposition on ~ 50 nm diameter Si NWs have discovered an instability from uniform shells and formation of individual Ge QDs[21]. Compared with earlier reports of uniform Ge shell growth on small, 10-15 nm diameter Si NW cores, these results suggest a strong influence from the core diameter on the morphologies of the shell layer. The transition of shell layer growth mode into QD arrays is a result of interplay of surface and strain energies that is unique in a thin and flexible nanowire substrate. Unlike in a traditional planar growth substrate, a small diameter nanowire core is thin enough to allow the strain distribution on one side to influence the strain on the opposite side of the cylindrical substrate. Recent theoretical studies by Schmidt et.al.[22] and Wang et.al.[21] have shown that at certain diameters, misfit strain in core/shell nanowires can propagate along the length of the wire and self-organize into a periodic pattern to minimize total strain energy.[10,21-23] They used a surface perturbation model to describe a series of morphological instability growth modes after deposition of Ge on a Si NW backbone.[21,22] The model predicts that initial instability of the shell layer deposition would lead to formation of periodic QD arrays in one of several unique growth modes, with the core size being the key determining factor of the QD morphology. Such misfit strain-guided epitaxial islands not only present a new type of periodic nanostructure, but also serve as periodic nanostressors to the core nanowire backbone thus providing a unique opportunity towards strain-engineered materials with novel mecahno-electronic properties for applications in, for example, thermoelectronic, and optoelectronic devices.

Experimentally, while periodic Ge QD array structures have been reported on both surfaces of thin Si nanomembranes[24], most studies of Ge deposition on Si NWs have focused on homogeneous shell growth[8,9,11,12,17,25-27] with few reports on observation of the predicted periodic surface instability.[18,20,24] Herein we report the first systematic study of misfit-guided QD growth based on CVD growth of Si/Ge core/shell nanowires with a variety of core diameters. Regular periodic arrays of coherent Ge QDs are formed and interestingly, anti-correlated QDs growth is observed for ~20 nm core diameter, consistent with theory. The wavelength of QD array is inversely proportional to core diameter while insensitive to growth time due to pinning of QDs with the periodic strain field. Lastly, a surface kinetics-driven transformation of uniform Ge shells to QD arrays is demonstrated ex-situ by thermal annealing at higher temperatures. Such strain-guided growth opens up a new avenue towards growth of self-organized nanoscale heterostructures.

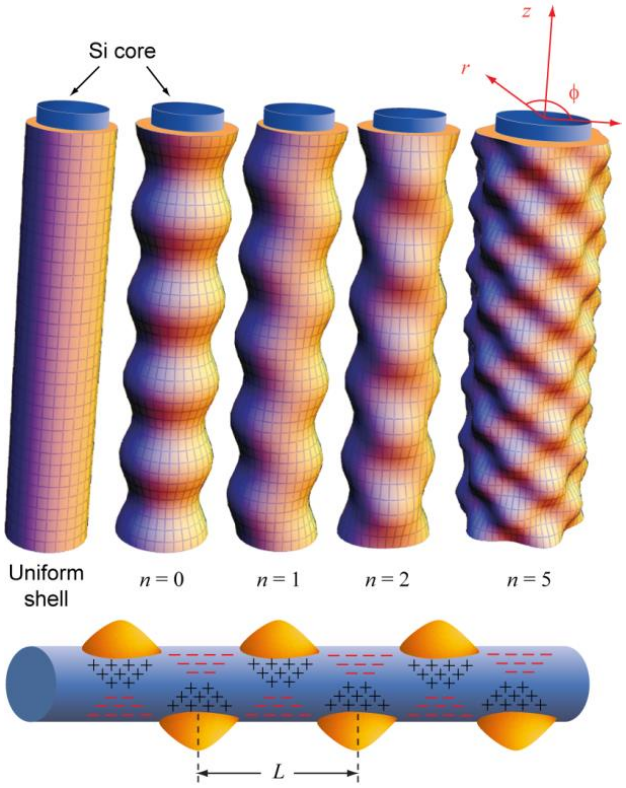

Figure 2.1. (Top) Schematic of possible surface instability modes of Ge shell on Si core nanowires. Homogeneous Ge shell and four different types of inhomogeneous growth modes are shown: n = 0, 1, 2, and 5. (Bottom) Alternating coherent strain distribution inside the core is shown as + (tensile) and – (compressive) signs for an n = 1 mode growth. The QD wavelength L is defined as the periodic distance between QDs on the same side of the wire.

2.2. Synthesis of Ge quantum dots decorated Si nanowires

In our experiment Si/Ge core/shell nanowires were grown on Si (100) substrate using silane (SiH_4, 2%) and germane (GeH_4, 2%) diluted in hydrogen as precursor gas sources in an LPCVD system (ET2000, Firstnano). Gold colloids (Ted Pella) with diameters ranging from 10 to 80 nm were dispersed on the Si substrate as catalyst seeds. The Si nanowire core was grown at 470 ℃ for 25 min with total pressure of 100 Torr (P_{silane} = 2 Torr) followed by Ge shell/QDs growth with total pressure of 40 Torr under a selection of growth temperatures and durations. During the transition from Si to Ge growth, small amount of silane (P_{silane} = 0.45 Torr) was flowed to prevent gold diffusion from the catalyst to the nanowire sidewall. Temperature, pressure, Si core diameter, and Ge shell/QDs growth time were varied extensively to explore Ge shell/dots morphology.

TEM analysis of the as-grown Si/Ge nanowires heterostructures shows prominently uniform Si NWs with Ge islands on their surface (Fig. 2.2a, b). The Ge islands or QDs appear darker in contrast compared to the Si backbone due to its higher elemental weight. In Fig. 2.2c, high-resolution TEM image shows that each QD consists of dislocation-free heteroepitaxial growth of single crystal Ge on Si. The corresponding fast Fourier transform (FFT) pattern (Fig. 2.2d) shows that the Si NW grows along the <110> direction and exhibits two clearly distinguishable peaks at the $[1\bar{1}0]$ direction, normal to the Ge/Si interface (inset of Fig. 2.2d). The twin diffraction peaks indicate a clean expitaxy between the Ge and Si lattices similar to those reported previously in Ge/Si core/shell NWs[12,31].

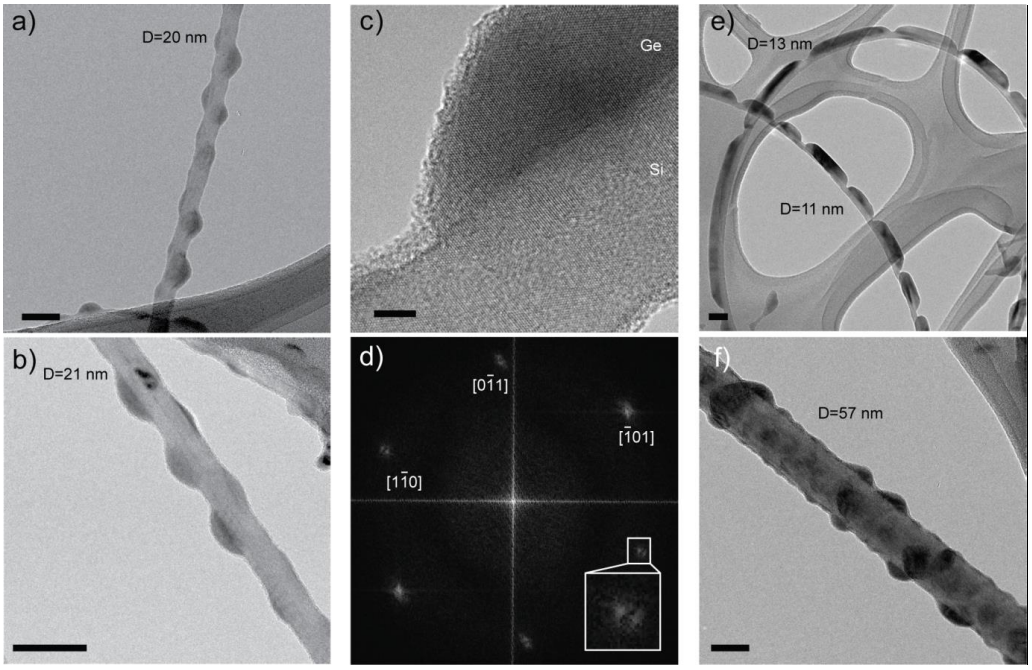

Figure 2.2. TEM images of Ge QDs on Si nanowires. Both Si core and Ge QDs were grown at 470 ℃. a) and b) Representative TEM images of anti-correlated quantum dots with 20±2 nm core diameters. c) High resolution TEM showing the defect-free single crystal Si core and Ge island. d) FFT of the TEM image in c). Note that the [0$\bar{1}$1] and [1$\bar{1}$0] FFT spots are composed of twin peak signals (lower inset). e) and f), morphology of Ge dots on small (11~13 nm) and large (> 50 nm) Si cores. Scale bar, 50 nm for a) - d), 5 nm for e).

2.3. Effect of Si core diameter on Ge quantum dots growth modes

Significantly, we find that the choice of core diameters has a strong influence on morphology of Ge QDs on Si NW substrate. Fig. 2.2a and b show TEM images of Si/Ge core/shell NWs grown with 20 nm gold colloids as catalysts. The measured core diameter of each nanowire is 20 and 21 nm respectively and both nanowires have periodic arrays of anti-correlated Ge islands or QDs decorated along the circumference in an alternating fashion corresponding to the n = 1 mode in Fig. 2.1b. The average wavelengths of Ge QD arrays (as defined in Fig. 2.1) are L = 56.6 and 53.3 nm respectively. These results are strongly indicative of the previously proposed anti-correlated organization of Ge dots on nanoscale Si NW substrates due to the periodic correlation of strain field in the nanowires.

In the case of nanowires grown with smaller, 10 nm diameter catalysts, however, the morphology of the Ge deposition is distinctively different. Fig. 2.2e shows two thin nanowires with 13 nm and 11 nm diameter backbone on which instead of discrete Ge QDs covering both sides, wider Ge islands are formed and they are found on a single side of Si surface only. In addition, the nanowires exhibit a bending curvature with the Ge on the convex surfaces (Fig. 2.2e). Such bending can be attributed to the high flexibility of these thin nanowire cores.[32] At such small diameter, the core substrate itself is close to or even less in thickness than the thickness of the Ge shell deposition, hence most of the strain energy is accommodated by bending stress within the core.

At the other end of the spectrum, as we focus on much larger diameter Si NW cores (Fig. 2.2d), the arrangement and density of Ge dots resemble island growth on planar substrates, covering all exposed surfaces around the circumference of the core and without clear angular or axial correlation among island location distributions. These represent higher order growth modes ($n \geq 2$) in Fig. 2.1d. This is because with large core diameter the correlating effect of strain field across the core NW diameter is no longer significant enough to produce the coherent pattern of Ge dots.

To gain quantitative insight into the self-organization of QDs on the Si nanowire substrates we collected and analyzed images from a variety of diameter-dependent morphologies of QD arrays. For this purpose, two key growth parameters, core diameter and Ge deposition time were extensively varied and TEM analysis was used to perform a statistical study on the wavelength of QD arrays.

Table 2.1. Statistical summary of Ge shell morphology versus core diameter *D*.

Core diameter		$D < 15$ nm	$15 \leq D \leq 30$ nm	$D > 30$ nm
Morphology	Single-side	90%	12%	-
	$n = 0$	5%	-	-
	$n = 1$	5%	84%	-
	$n \geq 2$	-	4%	100%
Number of samples		20	25	14

Table 2.1 summarizes the core diameter dependence of Ge shell growth morphologies. In all, three groups of nanowires were included based on initial growth of Si NW with catalyst Au colloids of 10, 20 and 40 nm. For samples with the smallest diameter (D < 15 nm), single-side Ge growth mode with Ge deposition on only one side of the Si NW is found on a majority (90%) of the nanowires. Among these single-side growth samples most (80%) exhibit bending curvature similar to that in Fig. 2.2e. Only one small diameter sample was found with Ge QDs on opposite side of the circumference in either n = 0 or n = 1 geometry. For medium range diameter samples ($15 \leq D \leq 30$ nm), however, we find a predominant distribution (84%) of n = 1 mode growth, while none shows n = 0 behavior. Lastly, the largest diameter nanowires in this study (D > 30 nm) uniformly exhibit higher index mode ($n \geq 2$) growth with the core surrounded by Ge dots on all sides. The fact that surface morphologies or growth modes of the Ge QDs are sensitively defined by the core diameter is strong indication of the role of growth substrate diameter in directing the correlation of misfit-strain across the circumference and is directly supportive of previous theoretical calculations[21,22,28]. The diameter dependence can be qualitatively understood by considering that the ability to form regular arrays of correlated QDs on the nanowire surface closely relies on the strain field correlation across the nanowire backbone (Fig. 2.1 bottom panel), therefore the larger the core diameter, the weaker the effect of strain on one side of the nanowire will propagate to affect the opposite side. At 84%, 90% and 100% for each diameter groups, such large, near-uniform distribution of certain growth modes suggests a novel route towards self-organization of QD nanostructures driven by minimization of strain energy in nanoscale heterostructures.

2.4. Analytical modeling on self-organizing of Ge quantum dot arrays

Following the model by Schmidt et.al.[22], Fig. 2.1 illustrates several predicted growth modes of Ge shell on a Si NW core when uniform shell growth becomes instable followed by preferential growth towards island/QDs. Ge growth on Si surface is prone to form islands rather than a thin film under the Stranski-Krastanow (S-K) growth mechanism. This is because of a large 4.2% lattice mismatch between Ge and Si and the need to minimize surface and edge energy.[7,28,29] The morphology of the shell instability in Fig. 2.1 is defined by perturbation of the outer shell layer thickness $R = R_s + \delta\, cos(qz)\, cos(n\phi)$ where R_s is the unperturbed outer radius of a uniform core-shell nanowire, δ is the amplitude of the perturbation, and q and n are the wave numbers in axial (z) and azimuthal (ϕ) direction.

Fig. 2.1 bottom shows schematically the nonuniform strain distribution inside the Si NW backbone at mode n=1. In this example, a Ge island pseudomorphically formed on the top side creates tensile strain within the Si substrate immediately underneath it due to the larger lattice of Ge compare to Si (+ signs). This in turn leads to compressive strain in Si at the bottom side (– signs), much in the same way as the convex and concave surfaces of a bent pipe. As a consequence further Ge deposition and QD formation at the bottom side will tend to avoid the compressively strained (–) surfaces while preferentially grow at the tensilely strained (+) region, resulting in an anti-correlated zig-zag organization of Ge dots on Si in order to reduce the total elastic energy of the system [30].

Among each of the different growth modes, we investigated the effect of core diameter on the wavelength of Ge QDs. In particular, Fig. 2.3a shows in the case of anti-correlated (n=1) nanowires the wavelength L is nearly insensitive to core diameter at 20~50 nm but increases rapidly with smaller D. These observations are also in good agreement with theoretical calculation (solid line, Fig. 2.3a) of the shell instability using first order perturbation[22]. Therefore with careful control of the nanowire core diameter, one can rationally tune the QD wavelength as a new route toward nanomaterial design.

Calculation of the wavelength of Ge QD arrays as a function of core diameter is carried out from considering perturbation of radius takes the form of $R = R_s + \delta\, cos(qz)\, cos(n\phi)$ where R_s is the outer radius of the unperturbed core-shell nanowire, δ is the amplitude of the perturbation, q and n is the wavenumber in the axial and circumferential direction. The time dependent perturbation can be expressed as[22]

$$\dot{\delta} = \frac{D_s \Gamma\, \Omega^2\, \gamma}{kT}\left(\frac{n^2}{R_s^2} + q^2\right)\left(\frac{1-n^2}{R_s^2} - q^2 - \frac{\Delta\omega}{\gamma}\right)\delta \qquad (1)$$

where D_s is the surface diffusion constant, Γ is the area density of lattice sites, Ω is the volume per atom, γ is the surface energy density and $\Delta\omega$ is the change of the strain energy on the nanowire surface caused by sinusoidal perturbation. $\Delta\omega$ is a function of shear modulus G, Possion ratio ν, surface free energy γ, surface stress τ and misfit m as defined in Ref. 1. At the fastest growth mode, the wavelength of QD array λ_{fg} as a function of core diameter R can be expressed as follow:

$$\lambda_{fg} = 2\pi \sqrt{\frac{2}{-\frac{\Delta\omega}{\gamma} - \frac{1}{(R+t)^2}}} \quad \text{for mode } n=1 \tag{2}$$

where R and t are core diameter and shell thickness respectively.

Besides simple n = 1 mode, we collected a large set of data of Ge QD wavelength versus core diameter from all observed growth modes (n = 0 and above) including varying Ge growth time from 3.5 to 20 minutes. Here the Si core nanowires were grown with 10~40 nm gold catalyst. The resulting L vs. D trend is plotted in Fig. 2.3b and reveals interestingly an inverse relationship between L and D. The trend is consistent with that from previous theoretical calculations[21,22,28] and strongly reinforces the picture of the controllability of self-organized QDs by strain engineering within specific core diameters.

Another striking finding from the statistical analysis of Ge QD wavelength L is the lack of dependence with increased Ge deposition time. As can be seen in Fig. 2.3b, despite Ge deposition time being varied nearly 6 times from 3.5 minutes to 20 minutes, there is no significant difference in L vs. D. That is, with longer growth time each individual QDs may grow in size but maintain spaced according to the strain field distribution and will not converge into each other.

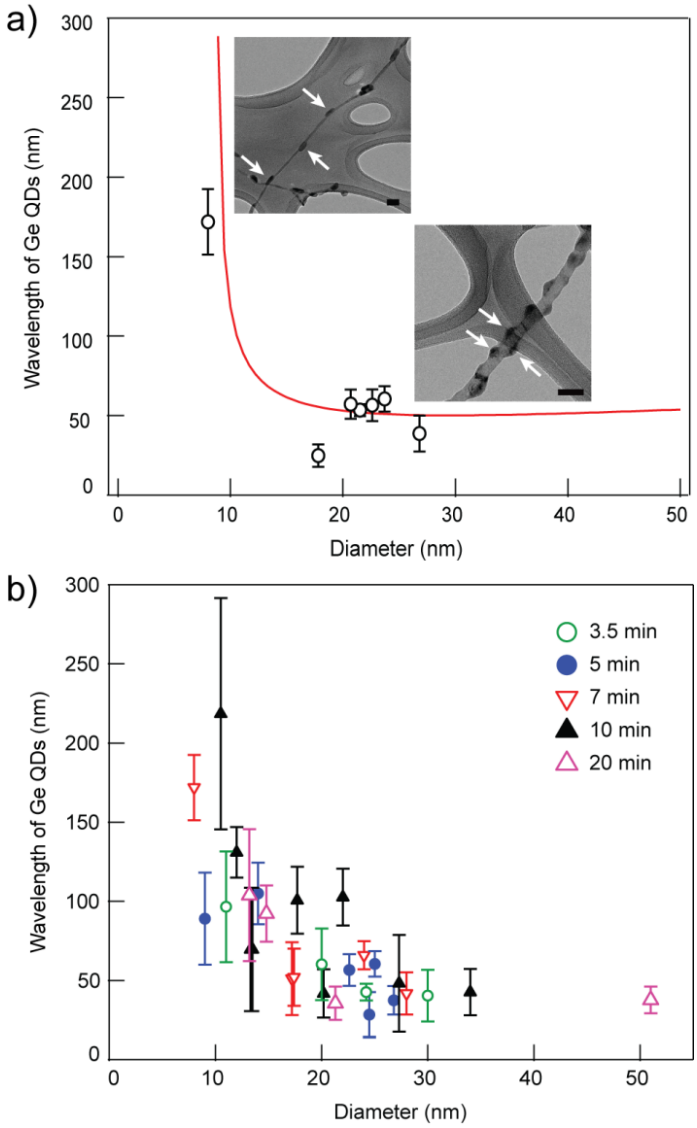

Figure 2.3. Wavelength of Ge QD array as a function of Si core diameter. Each point indicates the average distance between two Ge dots on the same side of one particular nanowire obtained from TEM images. Error bars represent the standard deviation obtained from measurements along the length of each nanowire. a) Statistic analysis and fitting result at the anti-correlated mode n=1. Arrows in the inset indicate selected QDs and their relative positions. Scale bar, 50 nm. Solid line corresponds to the calculation result of perturbation theory with the following parameters: Shear modulus[22] (G = 80 GPa), Possion ratio[22] (υ = 0.3), surface free energy[21] (γ = 1.5 Jm^{-2}), surface stress[21] (τ = 1.5 Nm^{-1}) and misfit (m = 0.042). See supporting information for details. b) Statistical summary of the general trend of core diameter dependent QDs wavelength for five batch of nanowire samples with different Ge growth time. The growth modes include all the modes observed and is not limited to n = 1.

2.5. Self-limiting growth of Ge quantum dots

This echoes previous observations in planar S-K growth of Ge on Si, where it is found that during extended growth, smaller islands tend to disappear while larger island continue to ripen, leading to a low island density rather than the islands merging into each other forming a continuous film.[29,33] To put this into our perspective on nanowire substrates, we focused on one specific group of 20±2 nm core diameter nanowires to characterize the size evolution of standalone Ge QDs as a function growth time and to see whether they will merge with each other to form a continuous Ge layer upon a long Ge deposition. Fig. 2.4a–c show the time evolution of Ge QDs on Si NW for a series of growth batches each with a different Ge deposition time (3.5, 5 and 10 minutes). These images show clearly that QDs grow larger in both width and height direction upon a longer Ge deposition: from Fig. 2.4a to c, the average QD heights increase from 2.6±0.6, 6.3±2.3, to 8.5±2.4 nm while the average QD widths increase from 18±1.4, 27±3.4, to 30.5±8.3 nm respectively (Fig. 2.4d). High resolution TEM images show that individual Ge QD shapes evolve from a small dome shape to a much taller and wider nanocrystal island with a large number of high-index facets as the Ge grows thicker (Fig. 2.5). Yet, as the size of each QD grows larger, the wavelength *L* (indicated between two black arrows) remains unchanged (Fig. 2.4e) regardless of growth duration (Fig. 2.4a to c: 50.3, 51.7, and 48.8 nm respectively). The QD formation remains discrete and is limited by the periodic strain distribution even after up to 40 minutes of Ge deposition. The self-limited growth of the QD array via the alternating tensile and compressive stress suggests that inner-nanowire strain engineering has the potential as a robust and reliable assembly driving force.

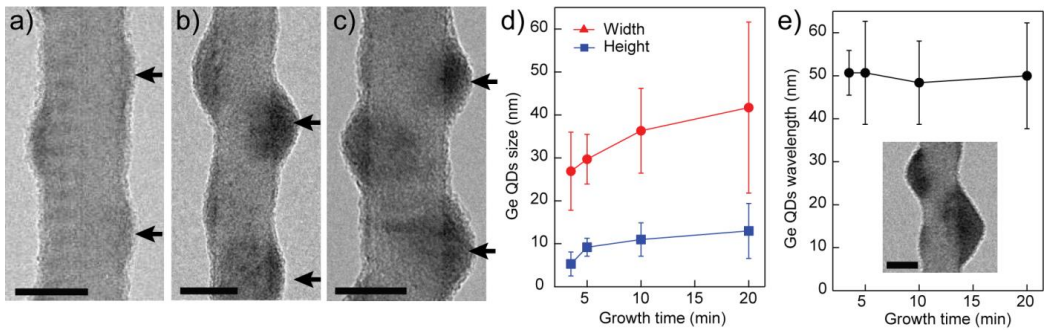

Figure 2.4. Evolution of Ge QDs as a function of growth time. a) – c) TEM images showing anti-correlated array of Ge QDs at different Ge growth time; 3.5, 5, and 10 min from left to right. d) and e) Summary of width, height and wavelength of Ge QDs as a function of growth time. Inset of e) TEM image of 20 min growth of Ge QDs. Error bars indicate the standard deviation from mean size of QDs on each nanowire. Sale bars, 20 nm.

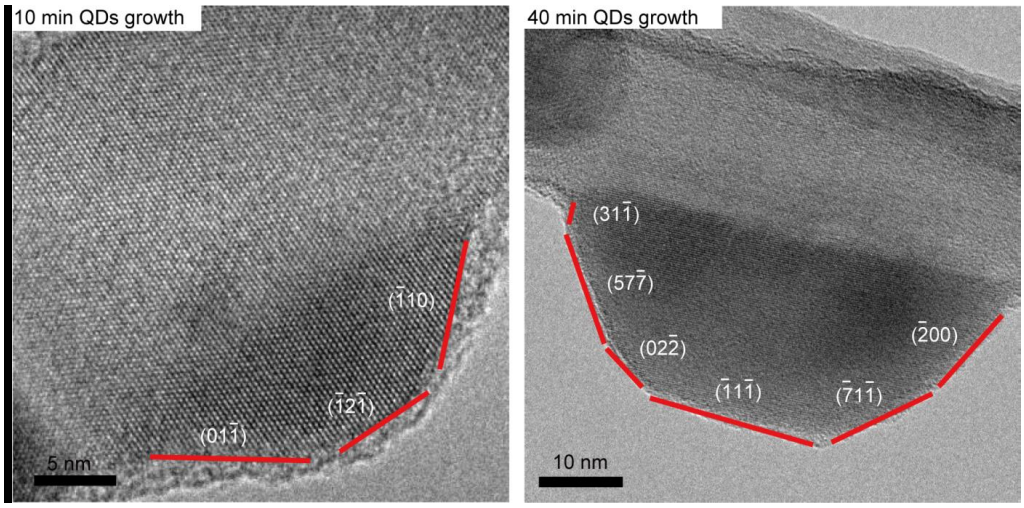

Figure 2.5. TEM images at two different Ge deposit time showing time evolution behavior of Ge QDs. As Ge deposition increases, Ge QDs grow taller and wider with increased number of facets.

2.6. Kinetic evolution of Ge quantum dot array

While our observation is consistent with the instability growth models from the perturbation method which considers thermodynamic energy minimization within the context of deposition influx of Ge atoms[20,21], we can further extend our experiment to explore the possibility of kinetic surface evolution to create misfit strain-driven QD arrays directly from an existing nanowire with uniformly coated Ge shells. For this purpose, we first grew 20 nm diameter Si NWs followed by Ge shell deposition at a lower temperature of 290 ℃ compare to previous growth conditions. TEM reveals no formation of QDs. Instead, an amorphous Ge shell with a relatively uniform surface is grown throughout the entire length of the Si nanowires as shown in Fig. 2.7 and Fig. 2.8a. In all, 2-3 nm of Ge shell was grown with 20 minutes deposition time at such a low temperature (Fig. 2.8a). Subsequently, post-growth anneal at a higher temperature have transformed these smooth Ge shell into n = 1 QD arrays (Fig.2.6, Fig. 2.8b). The results suggest that at high anneal temperatures, Ge adatoms on the surface of the amorphous shell will diffuse kinetically on Si surface forming a regular QD array to minimize total free energy. To quantitatively analyze the effect of temperature on morphological evolution of the Ge shell, we focus on the normalized shell roughness amplitude $\delta/R = (R_{max} - R_{min})/(R_{max} + R_{min})$ where δ and R are the amplitude of shell thickness perturbation and the outer radius of the unperturbed core/shell nanowire respectively. The minimum and maximum nanowires radius R_{min} and R_{max} along the entire length of the wire is used to calculate δ and R as a function of annealing temperature (Fig. 2.6). In Fig. 2.8b and its inset, (δ/R) increases from 0.15 to 0.25 as temperature is raised from 440 ℃ to 500 ℃, with the Ge islands thickness

increasing and the remaining amount of inter-island Ge material decreasing. Overall, as temperature T increases (1000/T decreases), the roughness δ /R is seen to increase sharply and the morphology transitions from a smooth Ge shell, to a rippled, semi-roughened surface, to eventually discrete QDs. This is summarized in Fig. 2.6. Characteristic of morphological evolution of Ge shell is quantitatively analyzed by calculating the thermodynamic activation energy of Ge adatoms for surface diffusion. The temperature dependence of the perturbation amplitude δ from equation (1) is used to extract the activation energy of Ge adatoms diffusion. (1) can be reduced to:

$$ln\delta \propto \frac{1}{kT}\exp\left(\frac{E_A}{kT}\right) \tag{3}$$

where E_A represents the effective activation energy. From fitting equation (3) on kinetic growth we deduced the activation energy to be 0.67 eV which is in agreement with previous study on Ge adatom diffusion on Si surface.[34]

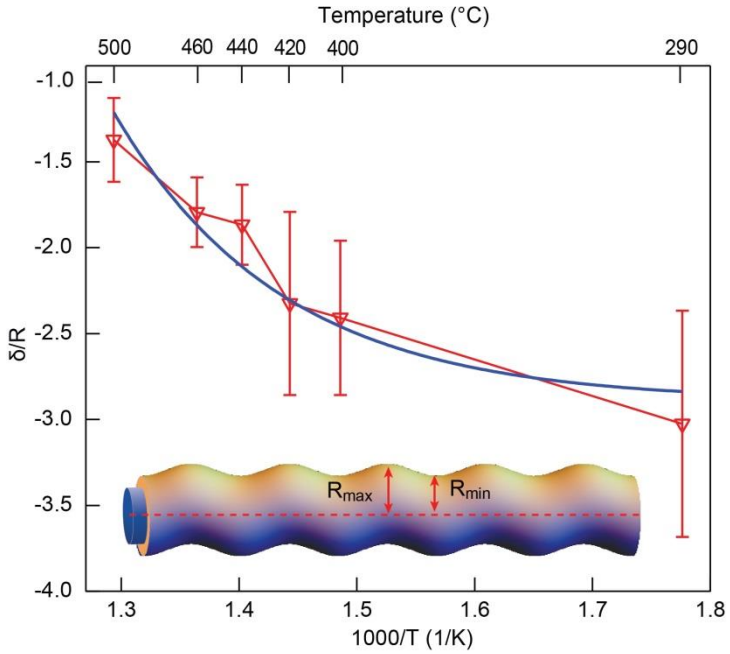

Figure 2.6. Transition of Ge morphology as a function of inverse temperature 1000/*T*. Experimental result (red line) and a theoretical fit (blue line). Scale bars, 20 nm.

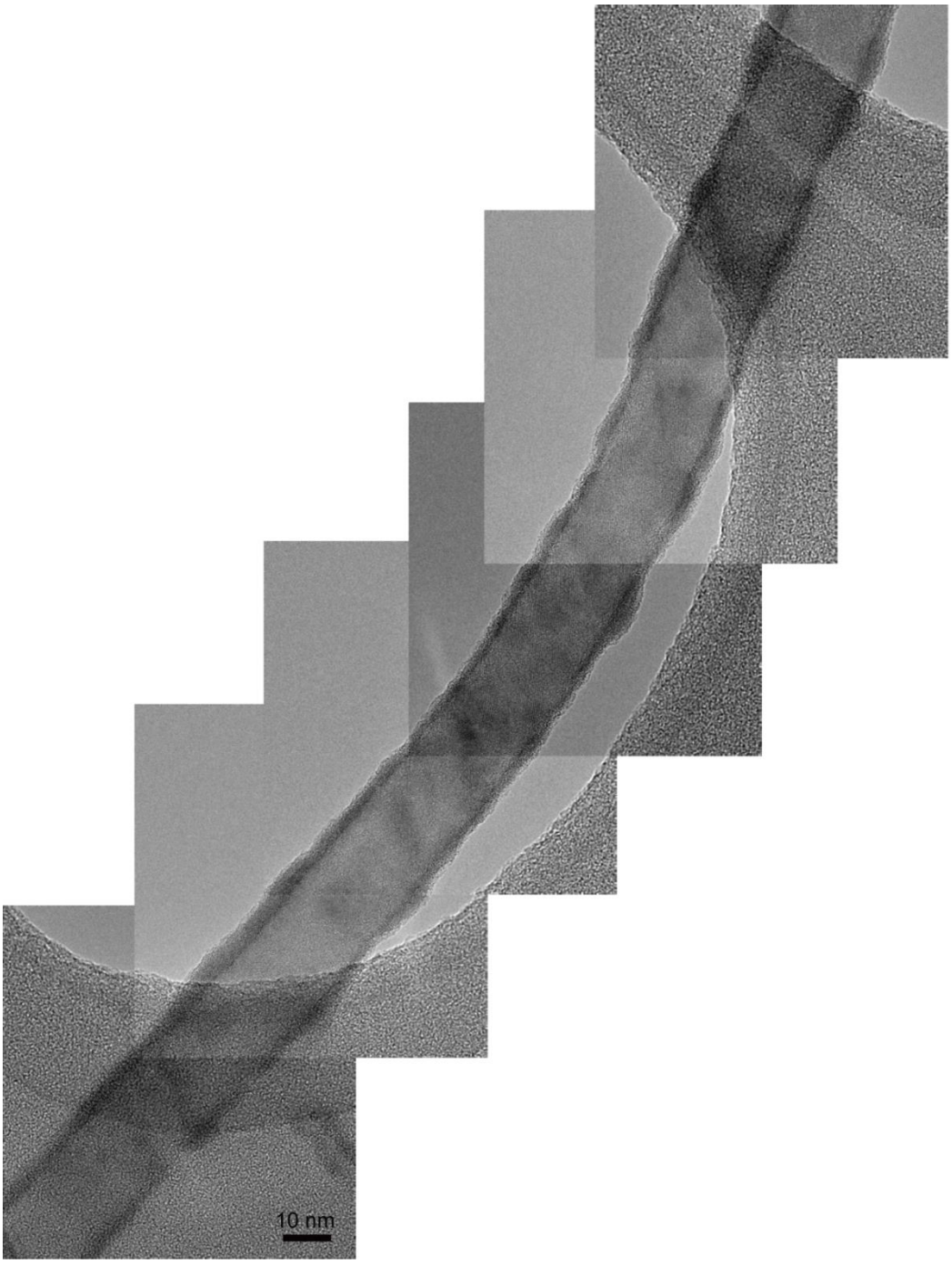

Figure 2.7. A series of TEM images of uniform Ge shell deposition along the 320 nm long Si core. The measured shell thickness is 2±0.6 nm.

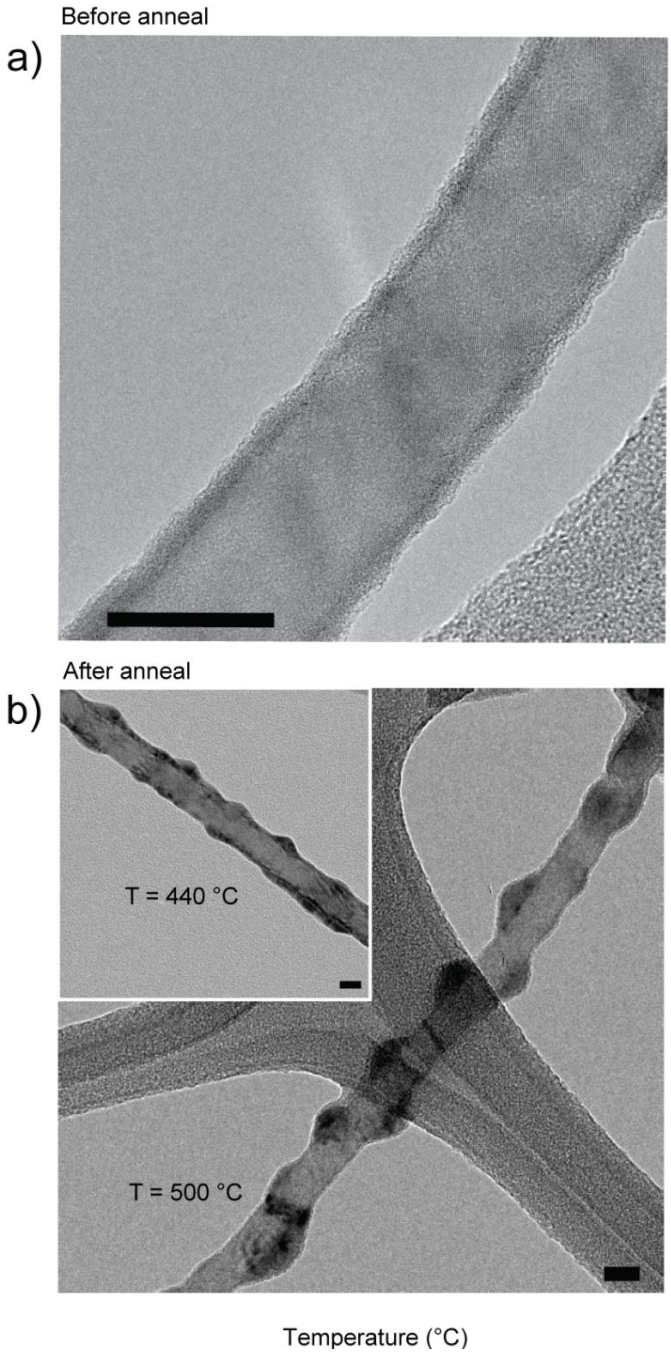

Figure 2.8. Effect of post growth anneal on morphological transition of Ge shell. a) Uniform Ge shell growth on Si core at 290 ℃ for 20 minutes. b) Effect of different annealing temperature. Main panel: sample annealed at 500 ℃ after Ge shell growth at 290 ℃ for 20 minutes. Inset, 440 ℃ for 20 minutes.

2.7. Conclusion

In summary, we report the first systematic experimental study of coherent QD array on nanowires and their diameter dependence. By varying growth parameters, we provided a comprehensive picture on self-organized and self-limited growth behavior of misfit-driven QDs on the nanowire substrate. First, the core diameter of nanowire plays an important role in determining the morphology mode shape and wavelength of Ge QD arrays. Secondly, growth-time dependent comparison on the Ge shell morphology reveals that the QD wavelength exhibits self-limiting characteristics. Furthermore, we have demonstrated ex-situ Ge QD array transformation from existing uniform shells by a post-growth annealing process. Compare to other self-organization or template techniques for nanostructure growth, we found that strain in nanostructure substrates presents another thermodynamic and kinetic driving force towards self-limited formation of periodic nanostructures without the need for lithography. Depending on the magnitude of misfit strain, it can naturally be extended to a wide range of heterostructure material systems.

Acknowledgments

This, in full, is a reprint of the material as it appears in Nano Letters, Volume 12, 2012. S. Kwon, Z. C. Chen, J.-H. Kim and J. Xiang. The dissertation author was the primary investigator and author of this paper.

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Chapter 3: Four-probe electrical characterization and selective functionalization of Si nanotubes

Crystalline silicon nanotubes Si-NTs) provide distinctive advantages as electrical and biochemical analysis scaffolds through their unique morphology and electrical tunability compared to solid nanowires or amorphous/non-conductive nanotubes. Such potentials are investigated in this report. Gate-dependent four probe current-voltage analysis reveals electrical properties such as resistivity to differ by nearly 3 orders between crystalline and amorphous Si-NTs. Analysis of transistor transfer characteristics yields field effect mobility of 40.0 $cm^2/V \cdot s$ in crystalline Si-NTs. The hollow morphology also allows selective inner/outer surface functionalization and loading capability either as a carrier for molecular targets or as nanofluidic channel for biomolecular assays. We present for the first time a demonstration of internalization of fluorescent dyes Rhodamine) and biomolecules BSA) in Si NTs as long as 22 μm in length.

3.1. Introduction

In depth understanding of biomolecular interactions has led to more sophisticate diagnostics and therapeutic systems in the field of bioanalysis and biomedicine[1] and prompted the development of biosensors with ever improving specimen selectivity, signal-to-noise sensitivity, and variety of detectible biomaterials[2-5]. Silicon nanowires have shown their potential as an advanced biosensor platform[6-10] with real-time electrical readouts thanks to their reduced dimensionality, large surface-to-volume ratio, amplification of signal as an active field-effect device, selective surface modification for detecting specific targets, and abundant material processing knowledge derived from semiconductor manufacturing techniques.

Considerable efforts have been devoted to improve the performance of nanowire NW) field-effect transistor FET) biosensors. Point-like localized detection area along the NW axis via either dopant modulation[11] or p-n heterostructures[12] can enable finer spatial resolution and faster response. Multiplexing from nanowires array networks[13,14] have paved the way toward extreme sensitivity in the range of femtomolar precision since multiple sensor arrays on a single chip correlate effectively to discriminate electrical false-positive signals. Meanwhile, series of techniques involving modification of NW structure[15,16], device geometry[17] and functionalization of NW surfaces[18] have been demonstrated to further enhance the detection performance of NW FET biosensors. Beyond solid NWs, crystalline silicon nanotube[19] c-Si NT) provides two distinctive inner and outer surfaces for analyte detection thus offering a new platform for novel applications as a biosenor. Unique

morphology and non-cytotoxicity[20,21] of Si NTs endow them with potential functionality for intravascular drug delivery/imaging by using their inner cavity to load biomolecular species[21,22] Previously Shi et al. has examined the mechanism of one-dimensional nanostructure-cell interaction[23] while Ben-Ishai et al. has shown selective binding of metal nanoparticle either on inner or outer surfaces of Si NTs[24]. Meanwhile, electrically active high-quality c-Si NT themselves possess additional functionality as an FET channel sensitive to potential and charge modulations from environments both inside and outside. A combination of these traits makes c-Si NTs an attractive material for novel biosensor FET devices as recently demonstrated by Gao, R et al.[25]. In this report, we present a fundamental study of c-Si NT properties as a platform for electrically and biochemically functional devices.

3.2. Synthesis and functionalization process of Si nanotubes

Synthesis of Si NTs shows well-controlled inner diameter 6~90 nm) and wall thickness 4~40 nm) by selectively etching core/shell Ge/Si nanowires NWs). Ge/Si core/shell NWs were used as sacrificial templates to synthesize crystalline and amorphous Si NTs, as depicted in Figure 3.1a. Ge/Si core/shell NWs were grown using a two-step process[1,2]. The Si shell can be controlled to be epitaxially grown or amorphous by the process temperature. The detail process of Ge/Si core/shell NWs growth and Si NTs synthesis by selective wet etching is as follow: Ge/Si core/shell NWs were grown on Si 100) wafers by the well-known vapor-liquid-solid VLS) process using low-pressure chemical-vapor-deposition ET-2000, CVD Corporation) .

Colloidal Au nanoparticles of 5-80 nm were dispersed on Si substrates as catalyst for Ge core growth using 1.8% GeH_4 in H_2 300 Torr total pressure, 290℃). Subsequently, in-situ deposition of epitaxial, crystalline Si shells was carried out using 2% SiH_4 30 Torr, 600℃) with varying growth duration depending on the desired shell thickness. During Si shell growth diborane B_2H_6) was used as in-situ doping source at a flow rate of 20 sccm and a B:Si atomic ratio of 1:560. As a comparison, amorphous Si shells were grown using a lower temperature at 490 ℃. Following growth of core/shell NWs, Si NTs were made by selective wet etching of Ge cores using 30% hydrogen peroxide with an etch rate of ~760 nm/min at 60℃. A series of centrifugal filtration Nanosep 30K MWCO, Pall Co.) in isopropyl alcohol IPA) were used to purify the resulting NTs.

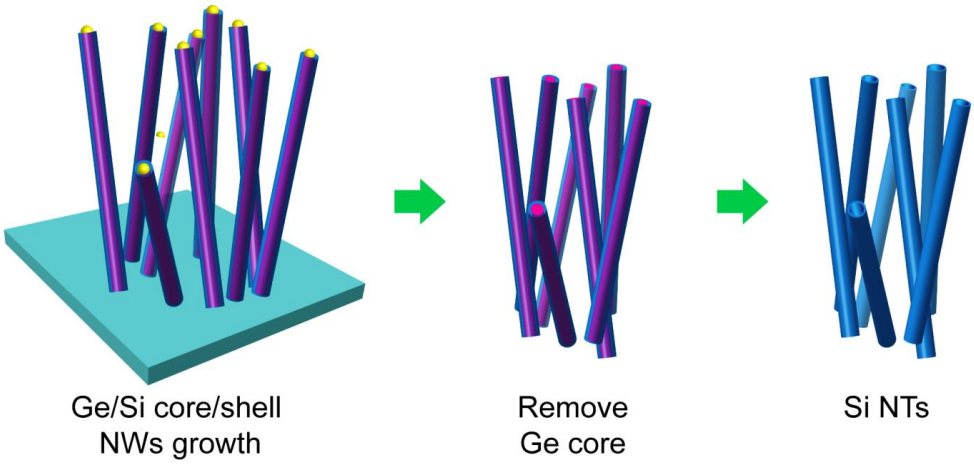

Figure 3.1. Schematics of Si NT synthesis steps showing transformation from Ge/Si core/shell NWs to Si NT structures by etching away the Ge core.

Previously extensively studies have shown decoration of Si NWs with a wide selection of biomolecules with help from covalently bonded silane chemistry[6,35]. To explore the potential integration and compatibility of our c-Si NTs with bio-specimens,

in particular the capability of introducing analytes on the inner surface and cavity of the NT, we have further studied selective surface functionalization on the NT's inner and outer surfaces Figure 3.2). The outer silicon surface was first selectively functionalized with polyethylene glycol PEGylation) as a stealth moiety. We begin with outer surface PEGylation of the as-grown core/shell NWs using trimethoxysilane PEG 2 kDa, ProChimia) upon immediate cool-down and removal from the growth chamber see Supporting materials). PEGylated NWs are cleaved and suspended in solvent using an ultrasonicator to expose the fresh Ge on the ends. This is followed by etch removal of the Ge core to form hollow SiNTs with the inner surface being fresh Si while outer surface protected by PEG Fig. 3.2a). Here we demonstrate loading of two different molecules, Rhodamine Figure 3.2b) and bovine serum albumin BSA)-fluorescein isothiocyanate FITC) conjugates Figure 3.2c) into Si NTs. The Rhodamine and FITC are red and green fluorescent respectively and are used to help visualize the loading results. The average ID size of NTs used is 30 nm.

PEGylation of Si NT surface was performed as follow: the surface of as-grown Ge/Si core/shell NWs was first cleaned and activated by a UV cleaner Jelight, model 42) for 20 min. The growth wafer then reacted in trimethoxysilane PEG solution 2 mg in 200 μl toluene) for 30 minutes, followed by rinsing with toluene and acetonitrile for three times. It is worth noting that both the growth substrate and the NWs outer surface were covered in this step during PEGylation. The entire growth substrate was then sonicated in isopropyl alcohol IPA) to break off the PEG-encapsulated NWs from the substrates and to expose clean, naked terminals of the Ge core to allow for the

subsequent Ge core etching. The etching step was performed in the solution of IPA mixed hydrogen peroxide (30%) 3:1 v/v at 60 ℃ for 3 hours.

After successful PEGylation process, Si nanotubes were further functionalized selectively at inner surface with Rhodamine dye. First, Si NTs with PEG on the outer surface were centrifuged to exchange buffer solution with DI water using a 30K MWCO centrifuge filter. Subsequently, inner surfaces of Si NTs were hydraoxylated with 2M nitric acid, then coated with 3-aminopropyltriethoxysilane APTES) as a self-assembled monolayer to enable the covalent bonding to the carboxylic group on Rhodamine. 2 % v/v) APTES was added to the Si NTs solution and reacted for 4 hours. Excessive APTES was removed by a 100K MWCO centrifuge filter. The purified solution was mixed with 5 mM Rhodamine dye Sigma-Aldrich) in methanol and kept reacting overnight. After reaction, excess Rhodamine dye was removed by using 30K MWCO centrifuge filter and the functionalized Si NTs were dispersed in DI water.

Besides functionalization of Si nanotube with small fluorescence molecules, more large and practical loading of biomolecules, BSA-FITC, is carried out. Synthesize BSA-FITC conjugates, thiol-maleimide coupling chemistry was used. BSA was dissolved at 20 mg/mL in pH 7.0 10 mM phosphate buffer. Disulfide bonds in BSA were reduced by 100 fold excess of dithiothreitol DTT) for 20 min. Excessive DTT was removed by desalt column Thermo Scientific). DTT treated thiol-BSA was then reacted with maleimide-FITC for overnight, and the resulting BSA-FITC was purified by 30K MWCO centrifuge filtration.

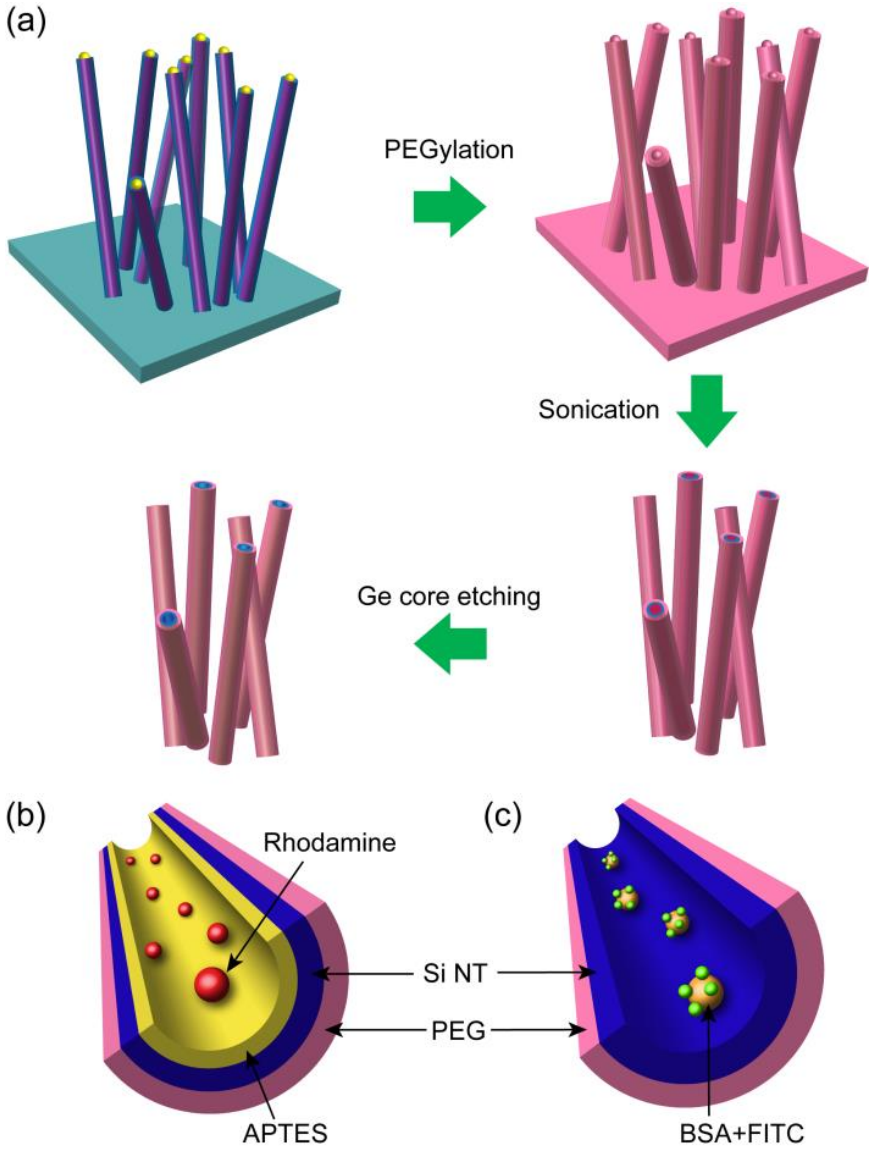

Figure 3.2. Schematic illustration of selective biomolecule functionalization. a) PEGylation process on the outer wall of Si NTs followed by Ge core removal for inner wall functionalization. b) Two types of biomolecules, Rhodamine and BSA-FITC, loading inside the cavity of Si NTs.

3.3. Characterization of inherent electrical properties Si nanotube

Figure 3.3a shows transmission electron microscope TEM) image of as-synthesized c-Si NTs with inner diameter ID) of 88±16 nm and 10 nm shell thickness. The ID is solely determined by the Ge core diameter during synthesis based on choice of the Au catalyst diameters. Using this method, NT with ID from 50 nm figure 3.3b) and, by using 5 nm diameter catalysts, to as small as 6.5 nm surrounded by 4 nm thick Si shell can be synthesized inset to Figure 3.3b). The NT shells have relatively uniform thickness with 1~2 nm fluctuations. High-resolution TEM figure 3.3c) and fast Fourier transform FFT) images inset of Figure 3.3c) further reveal the highly crystalline nature of the c-Si NTs. The FFT shows the NT's <112> growth orientation with the measured 0.11 nm interatomic distance matching that of Si {224} planes[28]. The 6 sharp diffraction spots around the centre indicate epitaxial deposition of Si layer following the Ge core. As shown in figure 3.3d, we found these crystalline NTs to preserve their crystallinity even after been exposed in air at room temperature for 28 days. There is also little discernable change in their oxide layer thickness shown as the light contrast layers on the outer surface of the TEM images)[29]. Such stability is ideal for nanoelectronic and biomedical applications.

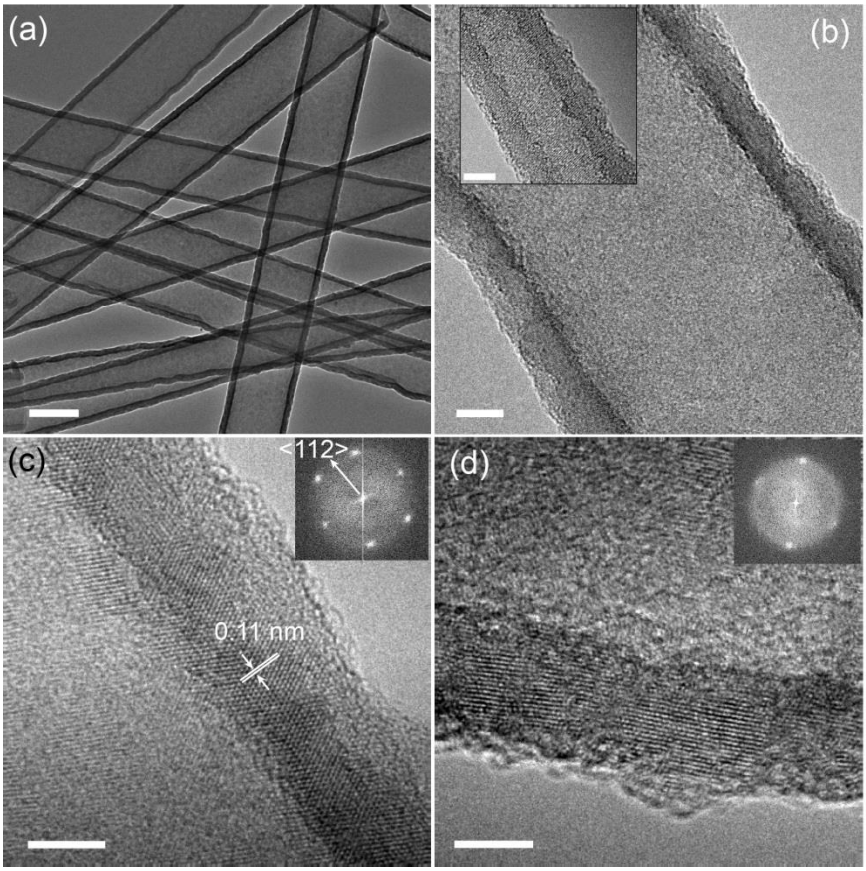

Figure 3.3. TEM analysis on crystalline Si NTs a) Bundle of Si NTs shown in low-resolution TEM image and b) Higher resolution image of individual NT with 50 nm ID and 9 nm shell thickness. Inset shows a NT with 6.5 nm ID with 4 nm shell. c) High-resolution TEM shows the crystal lattice on the shell of representative Si NT. Fast Fourier transform FFT) images in the inset indicates a <112> growth direction. d) TEM from crystalline Si NT after 28 days exposed in air and its FFT pattern on the inset. Scale bars: 100 nm for panel a) and 5 nm for b), c), and d).

To establish the fundamental electrical properties of c-Si NTs, we performed four point probe measurement on c-Si FETs with 100 nm thick thermal oxide layer as the back-gate dielectrics Figure 3.4a). The devices were fabricated using standard e-beam lithography, metallization, and lift-off techniques. Four metal contacts of 1 μm width were deposited on each NT FET with 150/30 nm thick Ni/Au bilayer followed by rapid thermal annealing at 400℃ for 30 seconds to improve electrical contacts

between Si and Ni. Four-probe measurements were carried out using HP 4155A semiconductor parameter analyser and SR560 voltage pre-amplifier to monitor the inner voltage drop V_{D23} while capturing I_D-V_{D14}. First, gated two-probe I-V measurement across electrodes 1 and 4 top inset, figure 3.4b) shows typical p-type FET behaviour, where the drain current increases with more negative gate voltages and begins to saturate at negative bias voltage. Meanwhile the four probe I_D-V_{D23} measurement result figure 3.4b) shows clear linear *I-V* curves indicating contact barriers are effectively eliminated. At V_G = -20 V, the two-probe resistance of the NT is 180 M while only 4.4 M when measured using the four-probe method, suggesting an average contact resistance of 88 M which dominates the two-probe measurement results. Therefore, four-probe current-voltage *I-V*) measurements are necessary in order to eliminate the effects from Schottky contact barriers at the Ni-Si contact interfaces and to represent intrinsic *I-V* characteristics of the NT material.

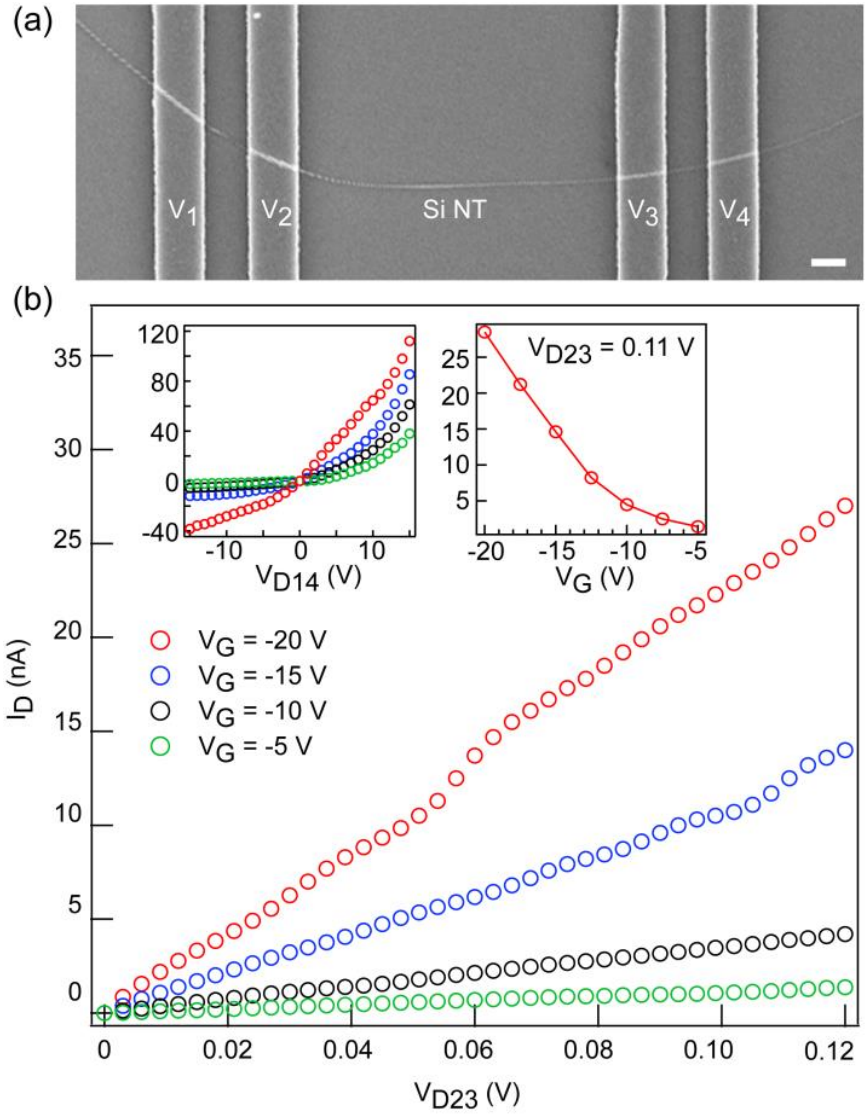

Figure 3.4. a) Device SEM picture and b) I_D-V characteristics under four different sets of gate biases from a representative c-Si NT FET with ID of 30 nm, shell thickness of 5 nm and length of 7.3 μm between the two inner contacts. The voltages on the four electrodes are indicated in the device SEM. Top left inset: two-probe I-V_{D23} characteristics across the two outer contacts. Top right inset: four-probe current versus gate bias V_G measured at an inner probe voltage of V_{D23} = 0.11 V. Scale bar in a): 1 μm.

From the dimension of the NT and slopes of the linear I_D-V_{D23}, we can obtain the resistivity of crystalline Si NT to be 0.032, 0.069, 0.22, and 0.68 Ω·cm from gate voltage of -20 red) to -5 V green) with 5 V steps. With decreasing gate bias, the four-probe NT conductance rises, representative of the linear-region transfer characteristics of a p-type FET[30] top right inset, figure 3.4b), with transconductance $g_m = dI/dV_G$) of 2.78 nS at V_{D23} = 0.11 V and an extrapolated threshold voltage of V_T = -9.9 V. From these values we can extract the low-field mobility μ based on a long channel transistor model using $\boldsymbol{\mu = g_m L^2 / C_G V_{DS}}$. For estimation of the gate capacitance C_G we used finite-element modelling similar to a previous study on the dielectric screening effect from low carrier density Si NWs[31] and found that back gate capacitance coupling to NTs is near identical to NWs across a wide range of carrier concentrations.

To determine gate capacitance of Si NT FETs we used finite element electrostatic simulation coupled with the equation:

$$\varepsilon_r \varepsilon_0 \nabla^2 V(x,y) = q\left[p(V) - n(V) + N_a\right]$$

to evaluate the potential V and hole carrier distribution in the cross-section of the NT or NW at different back-gate voltages in order to extract the gate capacitance. Here p, n and N_A represent hole density, electron density and unintentional doping/impurity doping density in the Si shell, respectively.

A cross-sectional view of the equipotential and hole carrier distribution is presented in Fig. 3.5b and c, for the cases of a nanowire and a nanotube, respectively. Both cases have the same outer diameter 40 nm), with the difference being the NT is hollow inside its 30 nm ID. If we assume a doping level N_A at 1×10^{17} cm^{-3}, Fig. 3.5b,c show that the hole carriers are mostly concentrated at the bottom surface and the outer

circumference for both cases, regardless whether there is a void inside the NT. Indeed, as we experimented through a wide range of N_A levels, the resulting gate capacitance C_G is identical between NT and NW Fig. 3.5a inset) and does not depend on N_A at on state V_G = -20 V). This is a result of the screening effect from large amount of hole carriers distributed on the outer surface of the NW or NT, making both materials behave similar to a metallic cylindrical conductor. As Fig. 3.5a shows, C_G also remains relatively constant with V_G throughout most of the on-state and only decreases significantly at V_G > -3 V when the hole carriers are beginning to be depleted. Although in our experiments, the exact activated dopant level N_A is yet to be determined due to the c-Si FETs exhibiting enhancement mode normally-off) FET behavior, since C_G is insensitive to N_A as our simulation shows, we can use C_G = 3.37 fF to extract the on-state field effect mobility of the device in Fig. 3.4.

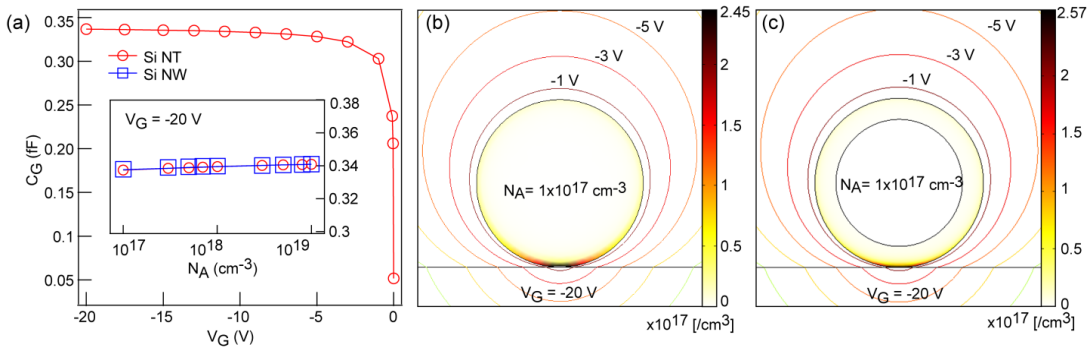

Figure 3.5. Two-dimensional finite element electrostatic analysis of gate capacitance for NT and NW structure using COMSOL Multiphysics. a) Calculated gate capacitance of a NT on 100 nm thick gate oxide with 30 nm ID, 5 nm shell thickness and 7.3 μm in length as a function of applied gate bias. The inset represents gate capacitance versus doping level at V_G= -20 V. b, c) Comparison of calculated gate capacitance between Si NT and NW from FEM modeling. Space charge distribution colored scale) and equipotential profile lines) of b) Si NW and c) Si NT at carrier concentration of 1×10^{17} cm^{-3} and gate bias of -20 V.

Field-effect mobility for the c-Si NT in Fig. 3.4 is 40.0 $cm^2/V \cdot s$, which is comparable to values reported in bulk polycrystalline Si with large grain sizes[32-34]. One can also obtain mobility from the Ohm's law using the Drude model: $\sigma = ne\mu = V_G - V_T)C_G\mu/L^2$ which yields μ = 40.6 $cm^2/V \cdot s$. These robust performances attest to the highly crystalline nature of the electronically active Si nanotube channels.

The high conductivity of our c-Si NTs is also evident when compared with *I-V* measurement of amorphous Si NT a-Si NT) FETs. We intentionally synthesized a-Si NTs using a modified growth recipe with Si shell growth at a lower temperature for 2 hrs which produced 40 nm thick amorphous shells as confirmed by TEM and the lack of distinctive spots from selected area electron diffraction SAED) patterns figure 3.6b). Compared to the thin, 4~5 nm thick c-Si NTs, here a thick a-Si shell thickness was necessary to achieve measureable conductance above the noise level of our measurement system. a-Si NTFET device was fabricated with four 2 μm wide Ni/Au contacts and an inner channel length of 2 μm Figure 3.6a). Two probe I_D-V_{D14} measurement top inset of Figure 3.6) shows non-linear, Schottky contact behaviour and p-type characteristics with a maximum on current of less than 50 pA under 30 V bias with V_G as small as -40 V. Four-probe conductance in Figure 3.6b shows an intrinsic resistivity of 28.8, 24.8, and 22.7 Ω·cm for -20, -30, and -40 V gate bias respectively with more apparent noise in the *I-V* curves due to the low current level. These values in a-Si NT are nearly 3 orders more resistive than the on-state resistivity from c-Si NTs. Such difference is a direct result of their respective morphologies.

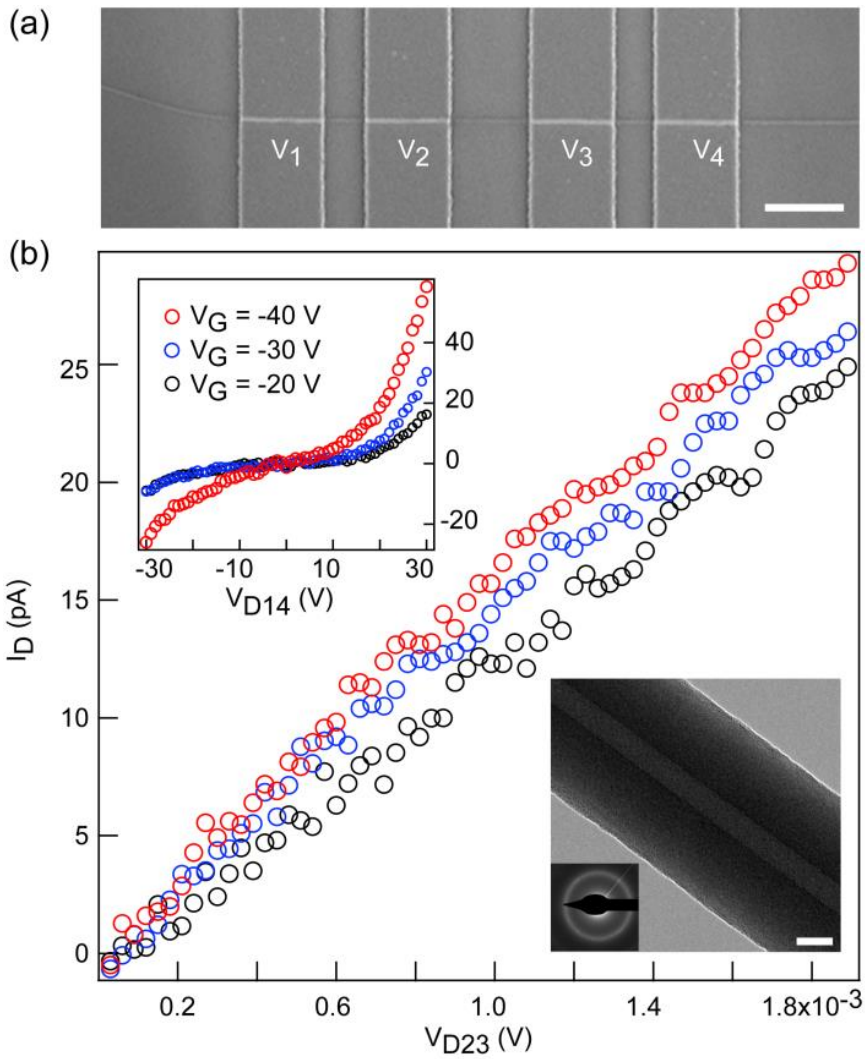

Figure 3.6. a) Device SEM picture and b) *I-V* characteristics under four different sets of gate biases from a representative a-Si NT FET with ID of 20 nm, shell thickness 40 nm and length of 2 μm between the two inner contacts. Top inset depicts corresponding two-probe *I-V* measurement and bottom inset shows TEM image of 40 nm thick amorphous Si NT with 20 nm core along with its SAED pattern in the inset. Scale bar, a) 2 μm and bottom inset of b) 20 nm.

3.4. Molecule infiltration fluorescent analysis

First, for loading of Rhodamine molecules, 3-aminopropyltriethoxysilane APTES) was used as a self-assembled monolayer on the inner surface of the SiNT to enable covalent bonding to the carboxylic group on Rhodamine see Supporting materials for details). Far-field fluorescent optical images Figure 3.7a and b right panels) along with corresponding bright-field images Figure 3.7a and b left panels) of functionalized Si NTs show a fluorescent rod-shaped structure 5 µm in length suggesting the successful functionalization of Rhodamine in the Si NTs. As a control experiment and to verify that Rhodamine is not attached to the outer surfaces, we performed the same functionalization procedures on solid core Ge/Si core/shell NWs. The solid NW surfaces are identical to the outer surface of hollow NTs and are PEGlyated via the same procedure. Absence of fluorescence Figure 3.7c right panel) compared to the NW in the corresponding bright-field image Figure 3.7c left panel) confirms the high selectivity of functionalization on the nanotube inner surface only and demonstrates the high quality PEGylation on the outer Si surface preventing any side reaction with APTES or fluorescent molecules which could be attached directly onto Si. Therefore we have shown that with protective PEGylation of the outer surface, the inner surface of the Si NT can be selectively functionalized and loaded with small molecules.

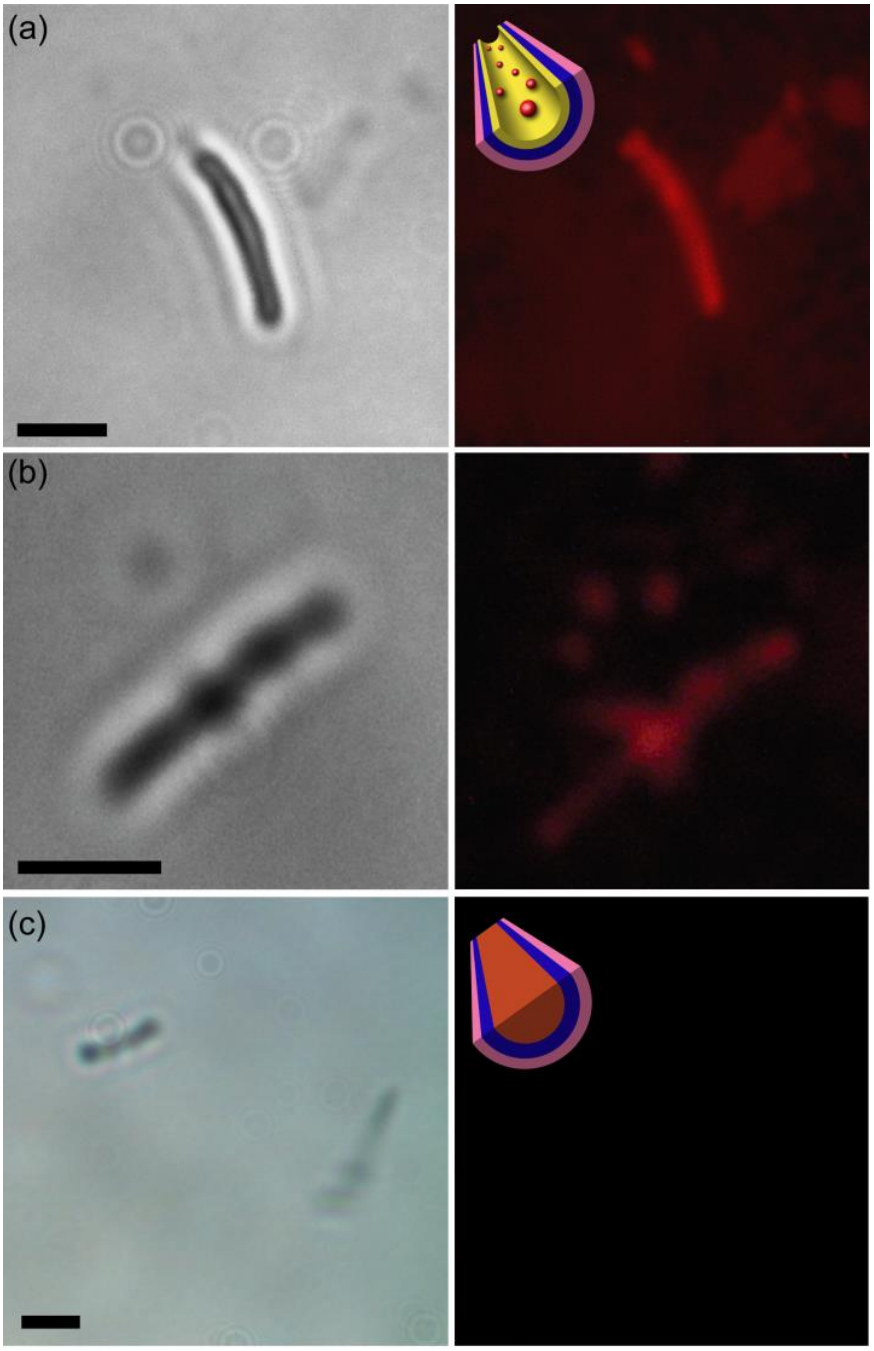

Figure 3.7. Demonstration of Rhodamine loading. a) and b) Bright field left) and fluorescent right) images showing red fluorescent signals in Rhodamine-loaded Si NTs. c) Control sample after APTES functionalization and incubation with Rhodamine using a solid core Ge/Si nanowire, showing no fluorescent signals. Scale bars, 3 μm.

Beyond fluorescent dyes, we further experimented with a larger, FITC decorated BSA molecule loaded inside Si NTs Figure 3.8). BSA is a single polypeptide chain with 580 amino acid residues, and contains 17 intrachain dissulfie bridges and 1 sulfhydryl group[36]. A BSA protein is approximately 14 nm x 4 nm x 4 nm in size. From the right panel of Figure 3.8a, rod-shaped green fluorescence signals are clearly observed in NTs shown in the bright field image Figure 3.8a, left), indicating fluorescently functionalized proteins BSA) are successfully loaded within Si NTs. Significantly, Figure 3.8a shows loading of BSA in an NT as long as 22 m. Similar to the case with Rhodamine, a control experiment loading BSA-FITC into solid core/shell Ge/Si NWs shows no fluorescence from its outer surface Figure 3.8b, right) of the corresponding NWs in the bright-field image Figure 3.8b, left), which again demonstrates the lack of leakage path or side reaction through the encapsulated PEG layers on the outer surface of Si NTs or NWs and most importantly, the successful selective functionalization of the inner walls of Si NTs by relatively large protein molecules.

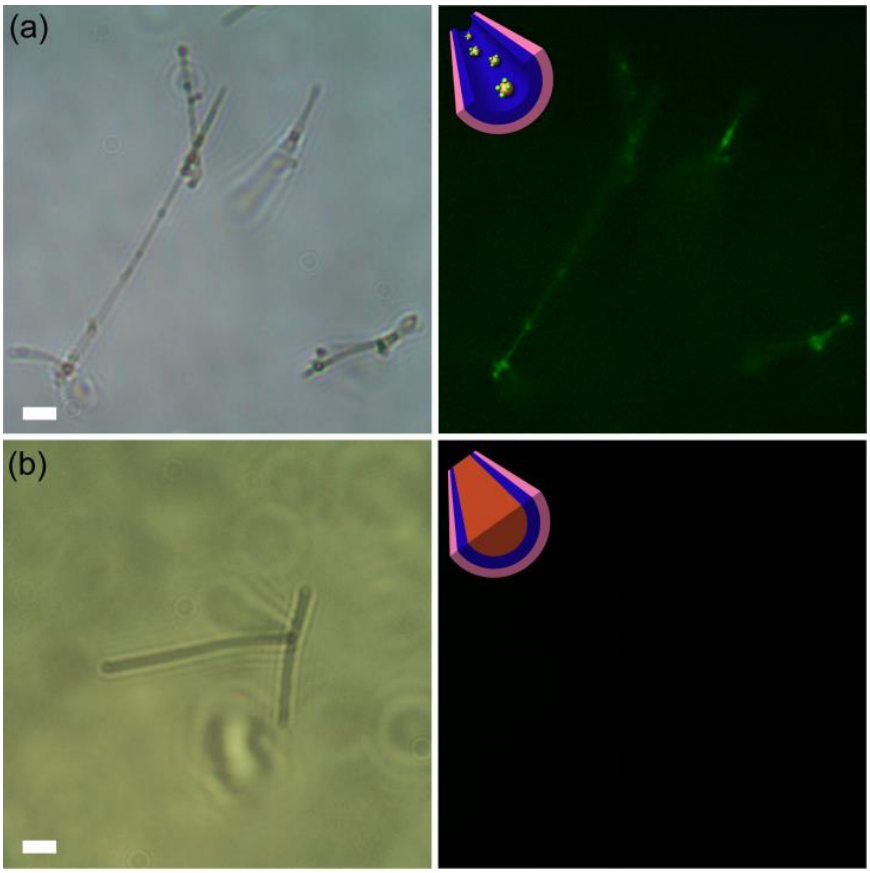

Figure 3.8. Demonstration of BSA-FITC functionalization. a) BSA-FITC-loaded Si NTs from bright field left) shows green fluorescent right) signals while b) control sample of a solid Ge/Si nanowire functionalized in the same condition presents no fluorescent signal. Scale bars, 5 μm

3.5. Conclusions

In summary, we have explored the potential of crystalline Si NTs as an electrically active and biochemically compatible material in ways that distinguish them from solid NWs. TEM analysis reveals the crystalline nature of the as-synthesized NTs. Four probe transport analysis yields field effect mobility of 40 $cm^2/V \cdot sec$ for the c-Si NT and a resistivity as small as 0.032 $\Omega \cdot cm$, nearly 3 orders more conductive than that of amorphous Si NTs. Such demonstrated electrical property in c-Si NTs may extend to much broader applications such as high efficiency thermoelectric modules due to phonon confinement effects in Si NTs[37,38]. Moreover, by selectively functionalizing the inner/outer surfaces, we demonstrated uptake of molecules from small dye molecules to proteins bonded on the NT inner surface, which when combined with the electrically active NT channel have the potential to lead to a range of novel therapeutic drug delivery or diagnostic detection applications[39-41].

Acknowledgments

This, in full, is a reprint of the material as it appears in Nanoscale, Volume 6, 2014. S. Kwon, Z. C. Y. Chen, H. Noh, J. H. Lee, H. Liu, J. N. Cha and J. Xiang.. The dissertation author was the primary investigator and author of this paper.

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Chapter 4: Ultra-low thermal conductivity in crystalline Si nanotubes approaching amorphous limit

Thermal transport behavior in nanostructures has become increasingly important for understanding and designing next generation electronic and energy devices. This has fueled vibrant research targeting both the causes and ability to induce extraordinary reductions of thermal conductivity in crystalline materials, which has predominantly been achieved by understanding that the phonon mean free path MFP) is limited by the characteristic size of crystalline nanostructures, known as the boundary scattering or Casimir limit. Herein, by using a highly sensitive measurement system, we show that crystalline Si c-Si) nanotubes NTs) with shell thickness as thin as ∼5 nm exhibit a low thermal conductivity of ∼1.1 W m^{-1} K^{-1}. Importantly, this value is lower than the apparent boundary scattering limit and is even about 30% lower than the measured value for amorphous Si a-Si) NTs with similar geometries. This finding diverges from the prevailing general notion that amorphous materials represent the lower limit of thermal transport but can be explained by the strong elastic softening effect observed in the c-Si NTs, measured as a 6-fold reduction in Young's modulus compared to bulk Si and nearly half that of the a-Si NTs. These results illustrate the potent prospect of employing the elastic softening effect to engineer lower than amorphous, or subamorphous, thermal conductivity in ultrathin crystalline nanostructures.

4.1. Introduction

Understanding and controlling extraordinary thermal transport behavior in nanostructures has been widely pursued[1-5] because of its broad implications for a diverse range of applications, such as nanoscale transistors,[6] phase change memory,[7] and advanced thermoelectrics.[8,9] In particular, nanostructuring has proven to be an effective approach to reduce the thermal conductivity[9-12] of crystalline semiconductors. This approach shortens the phonon MFP, which is limited by the characteristic size of crystalline nanostructures due to scattering at surfaces and interfaces. Crystalline thermal conductivity has been measured for nanowires as thin as ~15–20 nm[10,13] and ~10–100 nm thick films.[12,14] However, it is believed that the lower limit of the thermal conductivity of a material is that of its amorphous form,[15] thereby representing the minimum one could achieve through nanostructuring. Here, we experimentally probed thermal transport in Si nanotube NT) structures at unprecedentedly small length scales of ~5 nm. We showed that the thermal conductivity of the crystalline Si c-Si) NTs at this scale is even lower than that of amorphous Si a-Si) NTs of similar geometries. These striking results were further supported by a drastic reduction in elastic moduli of the 5 nm c-Si NTs, measured as a 6-fold reduction compared to bulk Si and nearly half that of the a-Si NTs. A convincing explanation of this sub-amorphous thermal conductivity in the 5 nm c-Si NTs is presented based on the phonon softening effect due to the drastically reduced mechanical stiffness.

Thermal characterization of nanostructures with an ultra-small size down to 5 nm has not been realized in the past due to the experimental challenges in both sample

manipulation and accurate thermal measurements. We employed crystalline NTs of sp^3 Si with ultrathin shells as a novel platform for probing thermal transport in this previously inaccessible regime. These NTs have thin crystalline shells ranging from 5 to 10 nm and, at the same time, large outer diameters ODs) greater than 40 nm, facilitating sample manipulation.

4.2. Nanotube synthesis, structural characterization, and device fabrication for thermal conductivity measurement

4.2.1. Si nanotubes synthesis and TEM characterization

The Si NTs were prepared from Ge–Si core–shell nanowires NWs) synthesized using a chemical vapor deposition CVD) process,[16] during which crystalline and amorphous Si shells were grown on Ge cores at 520 and 490 °C, respectively. The Ge core was then etched away using a H_2O_2 solution to obtain hollow Si NTs.[17] In detail, Ge/Si core/shell NWs were synthesized using gold nanocluster catalysts Ted Pella, Inc.) dispersed on Si 100) wafers using a vapor-liquid-solid VLS) mediated low pressure chemical-vapor-deposition process ET-2000, CVD Corporation). On the Ge core backbone grown at 290 °C, 300 Torr, and 100 sccm flow of GeH4 1.8% in H_2) for 2 hours, different types of Si shell were grown using 520 °C, 40 Torr, and 40 sccm of SiH4 2% in H_2) for crystalline shell and 490 °C, 70 Torr, and 100 sccm of SiH_4 for their amorphous counterpart. During the transition period between Ge core and Si shell growth, a small amount of SiH4 0.7 Torr, 15 sccm) was added to prevent gold diffusion from the AuGe eutectic droplets at the end of the Ge cores.[55] The shell

thickness was controlled by the growth time ranging from 5~25 min to deposit 5~10 nm of crystalline growth rate 1.3 nm/min) or amorphous shell growth rate 0.4 nm/min). Subsequent Ge core wet etching was performed in 30% hydrogen peroxide at 60 ℃ for 5 hours followed by purification process using multiple centrifugal filtration Nanosep 30K MWCO, Pall Co.) in isopropyl alcohol IPA). For the thermal conductance study, NTs were further transferred onto 19 by 19 um holey TEM grids Ted Pella, G1000HS) to investigate their inner-/outer- diameters, Si/oxide thicknesses and select clean and long NTs. Final FIB process was carried out to suspend selected NTs across two membranes of microfabricated devices. Figure 4.1a and b shows TEM characterization of ~5 nm shell crystalline and amorphous NTs, respectively, and Figure 4.1c shows a representative hollow NT at low magnification in TEM. The crystallinity of the c-Si NTs is clearly demonstrated in the TEM images and their associated electron diffraction patterns. Additionally, electrical conductivity[17] and fracture strength Figure 4.7) measurements indicate that although the c-Si NTs are polycrystalline, they are of high growth quality with grain sizes larger than 300 nm, much larger than the NT shell thickness, similar to NTs in previous studies.[18]

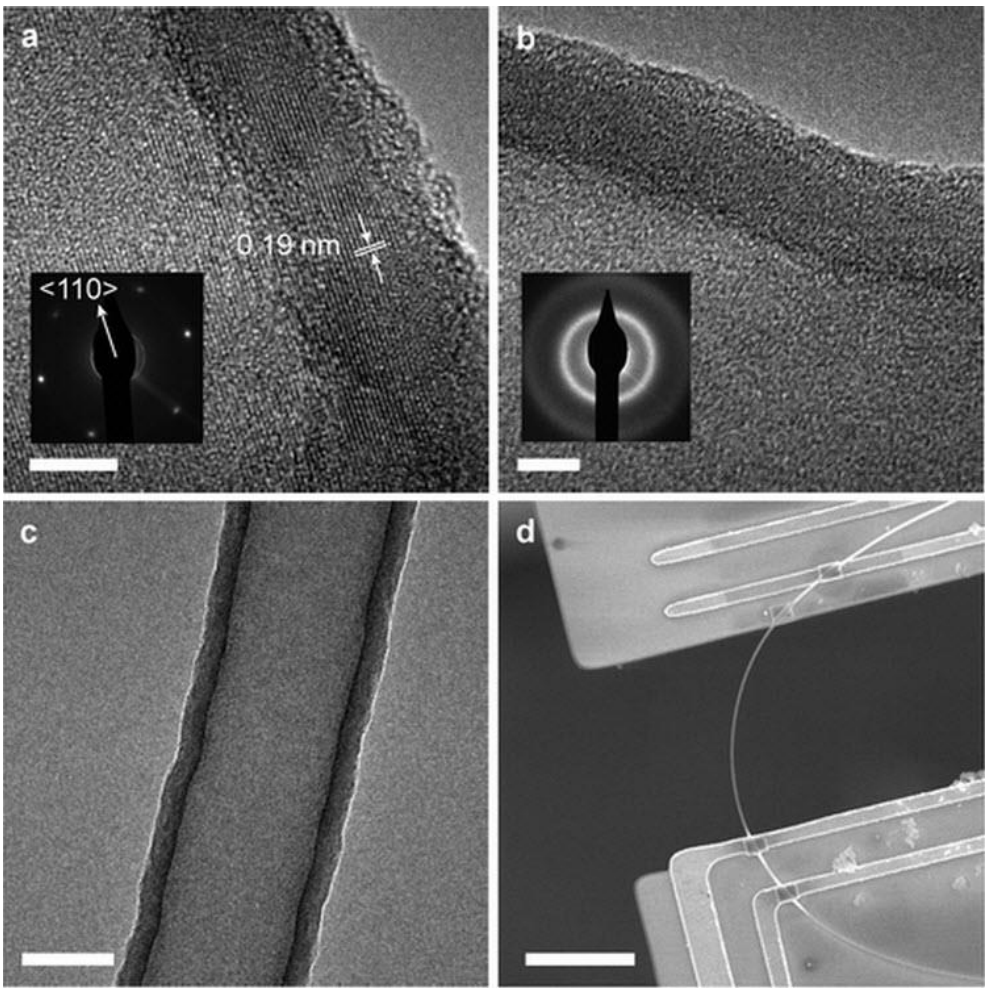

Figure 4.1. TEM images of silicon NTs: Crystalline 5 nm Si shell thickness a) and diffraction pattern inset a)) as well as amorphous 5 nm Si shell thickness b) and diffraction pattern inset b)). c) Low-resolution TEM image of hollow NT. d) Suspended nanotube sample used in the thermal conductivity measurement setup. TEM was performed to characterize all samples prior to thermal and tensile measurements to ensure crystalline or amorphous structure as well as geometry. Scale bars are 5 nm, 5 nm, 50 nm, and 5 μm for a), b), c), and d) respectively.

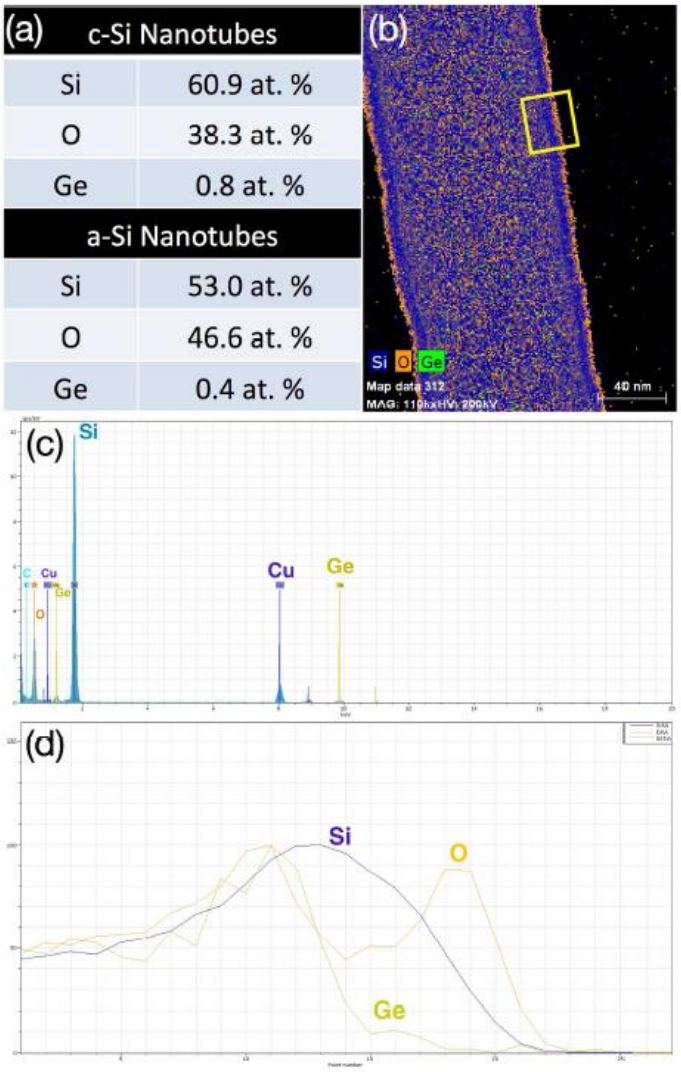

Figure 4.2. TEM EDX on Si NTs. a) Elemental concentrations in c-Si and a-Si NTs. The Si shell ~5 nm thick) and outer/inner oxide coatings each ~1 nm thick) account for the majority of atomic constituents while Ge impurities in the NT account for less than 1%. The higher Ge impurity concentrations observed in the c-Si versus a-Si NTs is most likely caused by larger amounts of Ge diffusion during the growth at higher temperature c-Si is grown at 520 ℃ while a-Si is grown at 490 ℃). b) EDX elemental mapping of c-Si NT in TEM. c) Element counts from EDX mapping b). The peaks for Cu and C come from the lacy C support structure on the Cu TEM grid. d) Cross-sectional element mapping from yellow box in b), starting from the inner tube surface left) to outside the NT right). The Si shell blue curve) has inner and outer oxide coatings orange peaks), while the majority of Ge impurities green curve) are close to or within the inner oxide surface. The vertical scale is a.u. and the Ge curve was scaled vertically to emphasize the spatial distribution.

4.2.2. Device fabrication

After the nanotubes were etched in solution, they were drop-cast onto TEM grids Gilder 1000 Mesh) for sample characterization. Using TEM FEI Tecnai Sphera), nanotube samples with the desired shell thickness and usable lengths ~15-20 µm fully suspended) were identified. These nanotubes were then checked using both electron diffraction and lattice pattern images to identify whether tubes were crystalline or amorphous as well as accurate shell dimensions.

The positions of the chosen nanotubes were carefully documented and then the TEM grids were transported to a dual-beam FIB FEI Quanta 3D) for further processing. Using SEM, the documented positions from TEM were identified and checked to make sure identified nanotubes were undamaged. The nanotube was then attached to a tungsten probe by electron-deposited Pt-C and lifted off the TEM grid with a nano-manipulator Omniprobe 200) after waiting for the Pt-C gas to dissipate. The nanotube was subsequently moved to a suspended membrane thermal measurement device, maneuvered into the preferred orientation, and placed into contact with the heating and sensing membranes, with ~10 µm distance between the edge of the gap between the two membranes and the end of the nanotube attached to tungsten probe to eliminate exposure of the suspended nanotube section to the ion beam if used to cut the probe free and reduce exposure to re-deposition effects. The nanotube was then bonded to the membranes using the electron-deposited Pt-C, with care taken to not expose the suspended portion to the electron beam. The probe was then either cut free using the ion beam or broken free after moving the probe. This process is shown in Figure 4.3. Later, the outer diameter and suspended nanotube

length were measured using a UHR SEM FEI XL30) to calculate the thermal conductivity from the measured conductance. Several samples were checked in TEM after the fabrication and measurement procedure to ensure that the nanotubes were not amorphized during device fabrication Figure 4.4).

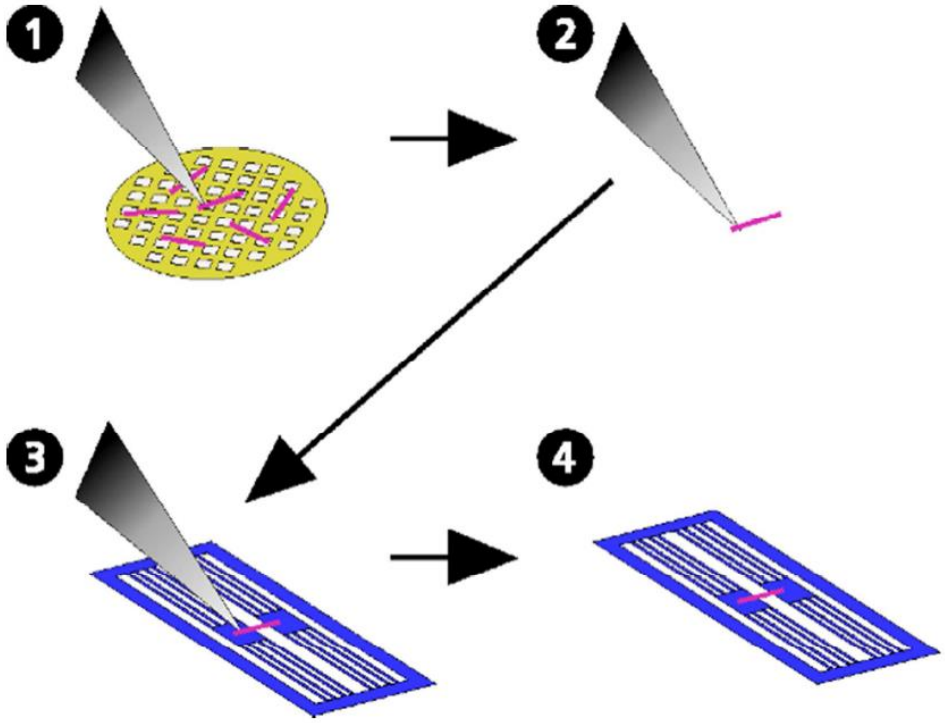

Figure 4.3. Nanotube thermal device fabrication procedure. The nanotube thermal conductivity samples are fabricated via a pick-and-place procedure. 1) Nanotubes are characterized in TEM to identify crystallinity and geometry. Furthermore, samples are mapped and then re-located in a dual-beam FIB. 2) In the FIB, the nanotubes are picked up using a tungsten manipulator probe. 3) The samples are then moved to a suspended thermal characterization device and placed between the hot and cold reservoir membranes. 4) The manipulator is then removed, leaving the suspended nanotube ready for thermal conductivity measurements.

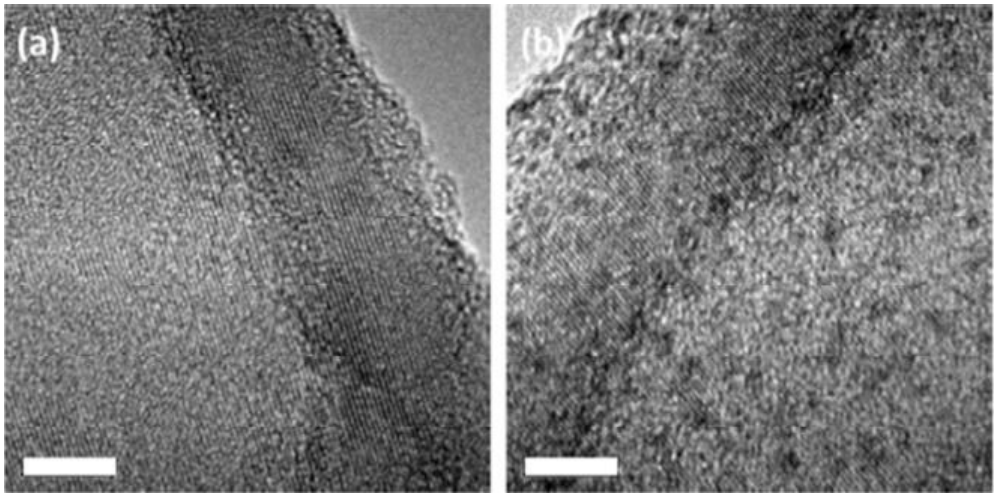

Figure 4.4. TEM of nanotube sample for thermal measurement a) before and b) after device fabrication. Nanotube samples were checked in TEM after device fabrication in FIB and compared to initial TEM images taken of samples. The measurement sample fabrication procedure does not damage the thin crystalline walls of the nanotubes as can be seen from the clear lattice images afterward. The small dark dots in b) are small Pt-C deposits on the surface from the FIB bonding procedure. Scale bars are 5 nm.

4.2.3. Elastic properties of Si nanotubes

AFM Cantilever Calibration was performed prior to the study on Si nanotubes. The elastic modulus tensile testing was done using an AFM cantilever as force transducer by measuring its deflection in SEM. For this reason, accurate knowledge of the cantilever spring constant is required to convert the deflection distance into an applied force. Before any tensile measurements were performed, we calibrated the AFM cantilever spring constant using the Sader method[61,62]. The spring constant of a rectangular cantilever is dependent on the cantilever geometry, material, and the fundamental radial resonant frequency in a vacuum. This can been calculated without knowledge of the density and thickness when the length 100 μm) is longer than the width 40 μm) which is longer than the thickness 1-2 μm), which is the case for our

cantilevers Bruker ORC8). The fundamental vacuum frequency shifts in the presence of a fluid, such as air, and can be calculated from the resonant frequency in the fluid with knowledge of the fluid properties, cantilever width, hydrodynamic function, and quality factor in the fluid which should be ≫1). Using an AFM Veeco Scanning Probe Microscope), we measured the resonance spectrum of the cantilever through a frequency sweep and narrowed the sweep band to capture both the fluid resonance frequency and the quality factor. The measured AFM cantilever resonant frequency and quality factor was 67.5 kHz and ~104, respectively. These parameters were used to calculate the static spring constant as opposed to the dynamic spring constant) necessary for the tensile tests, which was found to be 0.64 N m^{-1}. This proved very similar to the vibrometer test results supplied by Bruker resonant frequency: 67.9 kHz, spring constant: 0.66 N m^{-1}).

After calibration, elastic modulus of Si nanotubes and nanowires was measured. For such measurements, samples were first identified and characterized in a TEM, their positions were documented, and then they were moved to a FIB, similar to the sample fabrication process previously described. Then, in a process similar to previous tensile measurements on single nanowires,[36] the samples were picked up with a tungsten probe in a dual-beam FIB FEI Quanta 3D) and attached to the end of an AFM cantilever Bruker ORC8) using electron beam deposited Pt-C. The nanotube was then pulled using the probe while both the deflection of the cantilever and the length of the nanotube were measured schematic in Fig. 4.10a) and SEM measurement pictures in Figure 4.5, providing both the applied force stress) due to the cantilever deflection and strain from measurements of the nanotube length. Spring constants for

the AFM cantilevers were independently calculated using the Sader method[61,62] and were found to be approximately the same as the vibrometer calibrated spring constant values from manufacturer. The linear fit to the stress-strain slope is the Young's modulus of the nanostructure Figure 4.6). In addition to the calibration measurements on large diameter ~50 nm) c-Si NWs, for which we measured bulk-like elastic modulus similar to Zhu et al.[36], we measured the modulus of soft Nylon-11 polymer fibers. We measured two fibers of diameter approximately 615 and 713 nm with moduli of 706±92 and 614±92 MPa, respectively, within the range of values for bulk Nylon-11 612-860 MPa) [63-65]. Error in the measured elastic modulus came from uncertainty in the slope of the stress-strain curve do to errors in the measured nanotube lengths, uncertainties in the measured cantilever deflection and uncertainties in the calculated cantilever spring constant.

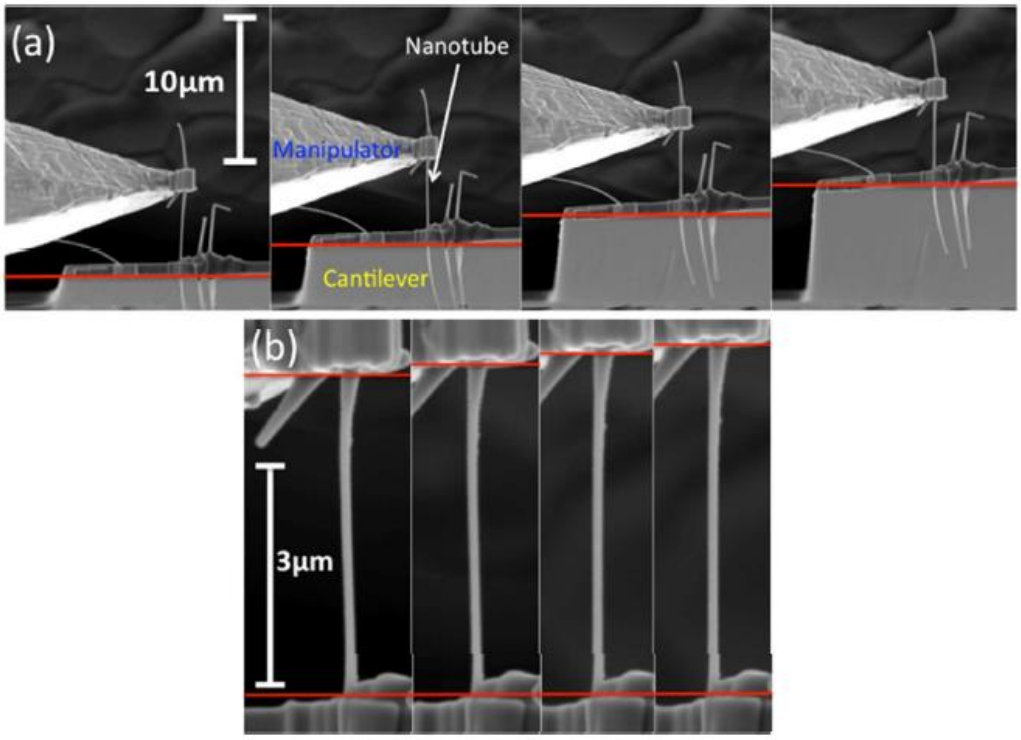

Figure 4.5. SEM of elastic tensile testing. a) AFM cantilever deflection measurements for applied stress. The nanotube sample being tested is bonded to a tungsten probe manipulator with electron beam deposited Pt-C and is then attached to the end of an AFM cantilever. Moving the tungsten manipulator perpendicular to the cantilever direction then stretches the nanotube. b) The nanotube strain is measured from increases in the nanotube length. At each cantilever deflection step, the length of the nanotube is measured.

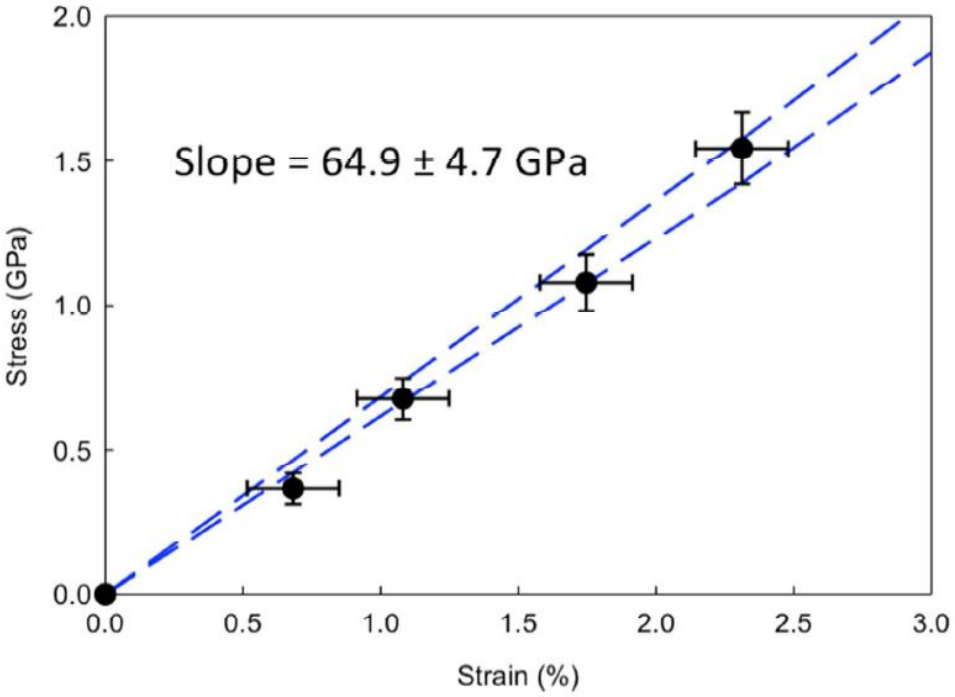

Figure 4.6. Stress-strain curve from nanotube tensile test. Applied stress to nanotubes during tensile tests is calculated from the nanotube geometry, as measured by TEM and SEM, and AFM cantilever force. The force is calculated from the cantilever deflection and spring constant. The nanotube strain is measured from increases in length during cantilever deflections. The dashed blue lines represent upper and lower bounds of the linear stress-strain slope fitting.

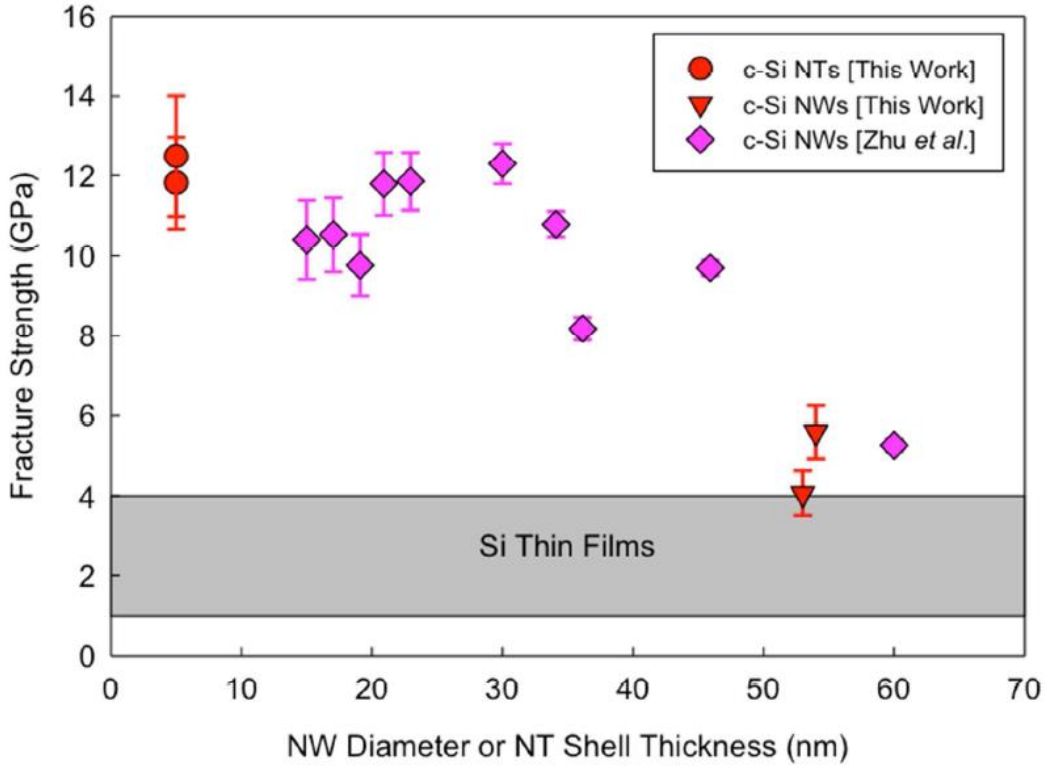

Figure 4.7. Fracture strength of crystalline silicon nanowires and nanotubes versus nanowire diameter or nanotube shell thickness. Following tensile testing of crystalline nanowires and nanotubes, the samples were stretched until breaking. The cantilever deflection is continuously measured until the nanotube/nanowire fracture point. This deflection leads to the maximum applicable stress, or fracture strength. This fracture strength is an indication of the concentration of defects in the sample, with low fracture strength indicating a higher amount of defects. From the measured data, as well as the previous electrical measurements[17] and TEM diffraction Figure 4.1a inset), it can be seen that the thin ~5 nm polycrystalline nanotubes are of high growth quality, with grain sizes longer than 300 nm, which are much larger than the NT shell thickness. Values of fracture strength of silicon nanowires and silicon thin films were taken from Zhu et al.[36] and Tsuchiya et al,[50] respectively.

After examining individual NTs in TEM, we then transferred the same NTs to suspended microdevices for thermal conductivity κ) measurements Figure 4.1d). The measurement was done in a differential bridge configuration we developed[19] that possesses a low noise floor of ~10 pW K^{-1} necessary for individual NT κ measurements. We also characterized and subtracted the parasitic background conductance of all measured devices. Figure 4.8a shows the measured thermal conductivity of Si NTs with nominal crystalline shell thicknesses of ~5, 7, and 10 nm over a temperature range of 35–300 K. The combined structural characterization by high-resolution HR) TEM carried out on each of the measured NTs allowed us to confirm crystallinity and precisely measure the dimensions of the samples

We used the full tubular thickness, as characterized by HRTEM for each measured NT ~5–10 nm c-Si or ~5 nm a-Si with ~1–1.5 nm inner/outer oxide coatings) to determine the thermal conductivity from the measured total thermal conductance. Although we could have estimated the oxide contribution to thermal conductance and subtracted it from the total measured conductance, we elected instead to use the full NT thickness including oxide) because there could be acoustic coupling at the interfaces between the oxide and Si. In addition, the thermal conductivity of the ~1 nm thick SiO_2 could deviate from the bulk value and is not known. We note that the native oxide thickness, which is formed during the H_2O_2 etching of the Ge cores, is usually ~1 nm, but sometimes is as thick as 1.5 nm, and did not grow over the period of study. We did not see oxide layer thickness greater than 1.5 nm. This is consistent with previous Si NT growth studies.[18] Measured dimensions and thermal conductivity for all NT samples are listed as following:

Table 4.1. List of measured Si nanotube samples. The measured geometries and thermal conductivities at 300 K. All samples were first characterized in TEM to check for crystallinity and shell thickness. After the samples were bonded to thermal measurement devices, suspended lengths and outer diameters were checked in UHR SEM.

Sample ID	Sample Type	Shell Thickness (nm)	Outer Diameter (nm)	Sample Length (μm)	κ @ 300 K (W m^{-1} K^{-1})
C5-1	Crystalline NT	5.6	138	7.66	1.18±0.08
C5-2	Crystalline NT	5.1	48	5.75	1.11±0.10
C5-3	Crystalline NT	5.7	101	4.76	1.21±0.09
C5-4	Crystalline NT	5.7	143	4.78	1.19±0.08
C5-5	Crystalline NT	5.3	111	4.20	1.21±0.09
C5-6	Crystalline NT	5.6	91	4.21	1.15±0.08
C5-7	Crystalline NT	5.6	108	3.72	1.21±0.08
C7-1	Crystalline NT	7.4	113	10.25	1.36±0.10
C7-2	Crystalline NT	7.2	100	5.16	1.36±0.09
C10-1	Crystalline NT	11.4	109	10.60	1.65±0.11
C10-2	Crystalline NT	11.0	89	10.02	1.66±0.11
C10-3	Crystalline NT	9.6	84	7.42	1.68±0.13
A5-1	Amorphous NT	5.6	81	10.50	1.78±0.13
A5-2	Amorphous NT	5.1	88	5.67	1.52±0.11
A5-3	Amorphous NT	5.2	46	6.23	1.60±0.12

4.3. Crystalline and amorphous Si nanotubes thermal conductivity measurement

Multiple samples of each type, including seven 5 nm c-Si NTs, have been measured, all with high repeatability, underpinning the accuracy and reliability of the measurement technique. Furthermore, the measured thermal conductivity shows no length dependence for lengths ranging from 4 to 8 μm, suggesting negligible thermal contact resistance.

The detail measurement of thermal conductivity of Si nanotubes is as follow. The thermal conductance of nanotube samples was measured using the suspended micro-device technique,[10, 56] where two SiNx membranes patterned with Pt resistive thermometer PRT) coils are each suspended by six SiNx beams. One of the membranes is used as a heater by passing DC current through the PRT, inducing a temperature rise by Joule heating, while the other is used solely as a sensor. Subsequently, the temperature rise is measured on both membranes, with knowledge of the temperature coefficient of resistance TCR), by passing small AC currents through both PRTs and measuring the change in resistance. The TCR is directly found by fitting the measured base resistance as a function of sample temperature to the Bloch-Gruneisen equation. Sample temperatures were measured using a K-type thermocouple directly attached to the micro-device being measured. The nanotube to be measured is placed bridging the two membranes and the applied Joule heating is varied. By measuring the resulting temperature rise on both heating and sensing membranes, the heat flux through the suspended nanowire sample can be found and

the thermal conductivity calculated. The measurement is conducted in a closed cycle He cryostat used to vary the global temperature of the sample from 35-300 K. The system is also held in vacuum pressure of less than ~10^{-5} Torr to reduce conductive and convective heat transfer by residual gas molecules in the chamber. Radiative heat losses along the suspending SiN_x beams are also negligible as it accounts for <1% of the systematic measurement error over the measurement temperature range.[57] Due to the low thermal conductance of the nanotubes <1 nW K^{-1}), a variation on the measurement employing a Wheatstone bridge based circuit to measure the resistance change of the sensing membrane was used to increase sensitivity, enabling measurements of thermal conductance as low as ~0.1 nW K^{-1}.[19, 58] At such sensitivities, however, there is an intrinsic background thermal conductance in addition to the nanotube thermal conductance, which has a value of ~0.2 nW K^{-1} at 300 K for device with a 5 μm gap between the membranes and decreasing with the system temperature. In order to eliminate this background conductance, a canceling scheme is used, with the sensing membrane of an identical blank pair device with no nanotube present as the other branch of the Wheatstone bridge.[59, 60] The heating membrane of this pair device is Joule heated with applied power equal to that of the heating power applied to the nanotube device. The bridge then measures the difference between the temperature rises of the nanotube and pair sensing devices, effectively subtracting the background conductance and leaving only the nanotube thermal conductance which is used to calculate the thermal conductivity. Error in the measured thermal conductivity comes from error in the measured TCR, standard deviations of

multiple measurements to account for random errors, and uncertainties in the geometry measurements from TEM and SEM.

The measured thermal conductance was then converted to the reported thermal conductivity values using cross sectional area based on the total shell thickness including the Si shell and 1-1.5 nm native oxide layers on both inner and outer surfaces. The thermal conductance of the native oxide layers was not subtracted from the total conductance because thermal conductivity of ~1 nm thick SiO_2 is unknown. Therefore, the reported thermal conductivity values can be viewed as the effective ones for the Si and SiO_2 composite nanotubes, which is also consistent with the values extracted from the MD simulations in this work. Nevertheless, it should be noted that since the thermal conductivity of the SiO_2 is on the order of 1 W m^{-1} K^{-1}, similar to the measured thermal conductivity value of the NT samples, the thermal conductivity of the 'pure' Si shells would only be altered slightly if the oxide layer contribution was subtracted.

As shown in Figure 4.8a, the average measured thermal conductivities were 1.18 ± 0.12, 1.36 ± 0.10, and 1.66 ± 0.13 W m^{-1} K^{-1} at 300 K for ~5, 7, and 10 nm shell c-Si NTs, respectively. The measured κ of the ~5 nm c-Si NTs approaches the theoretical minimum thermal conductivity κmin) for amorphous silicon 1 W m^{-1} K^{-1}),[15] which is extraordinary given that these are crystalline structures, whereas the κmin model is used to describe amorphous materials where phonon energy transport is limited to nearest atomic neighbors.[15] Furthermore, we compared κ of 5 nm crystalline NTs to that of the fully amorphous Si NTs with similar shell thickness Figure 4.8b). Surprisingly, the measured κ of the crystalline samples is even lower than that of the

a-Si NTs. The difference ~30%) is substantial and clearly exceeds the measurement uncertainty. Similar subamorphous behavior has been observed in layered WSe_2 crystals,[23] which was largely due to the interfacial thermal resistance between stacked crystal layers, whereas the low κ observed in the c-Si NTs here corresponds to heat conduction along the axial direction without interfacial resistance. Though the NTs contain a small concentration of Ge less than ~1% atomic ratio, see Supporting Information Figure S16), in line with previous NT studies,[18] it would not affect thermal conductivity in the ~5 nm c-Si NTs. The small amount of Ge could only affect thermal conductivity in much larger nanostructures (>100 nm) because of the coexistence of impurity and boundary scattering.[24,25] However, for very small nanostructures, such as the NTs studied here, boundary scattering overwhelmingly dominates impurity and even Umklapp scattering.[26] It has additionally been shown that thermal conductivity of a-Si is far below that of Si–Ge alloys with Ge concentrations ranging from 0.13% to 20%.[27] Therefore, impurity scattering introduced by the small amount of Ge would not be strong enough to induce the subamorphous thermal conductivity in the ~5 nm c-Si NTs.

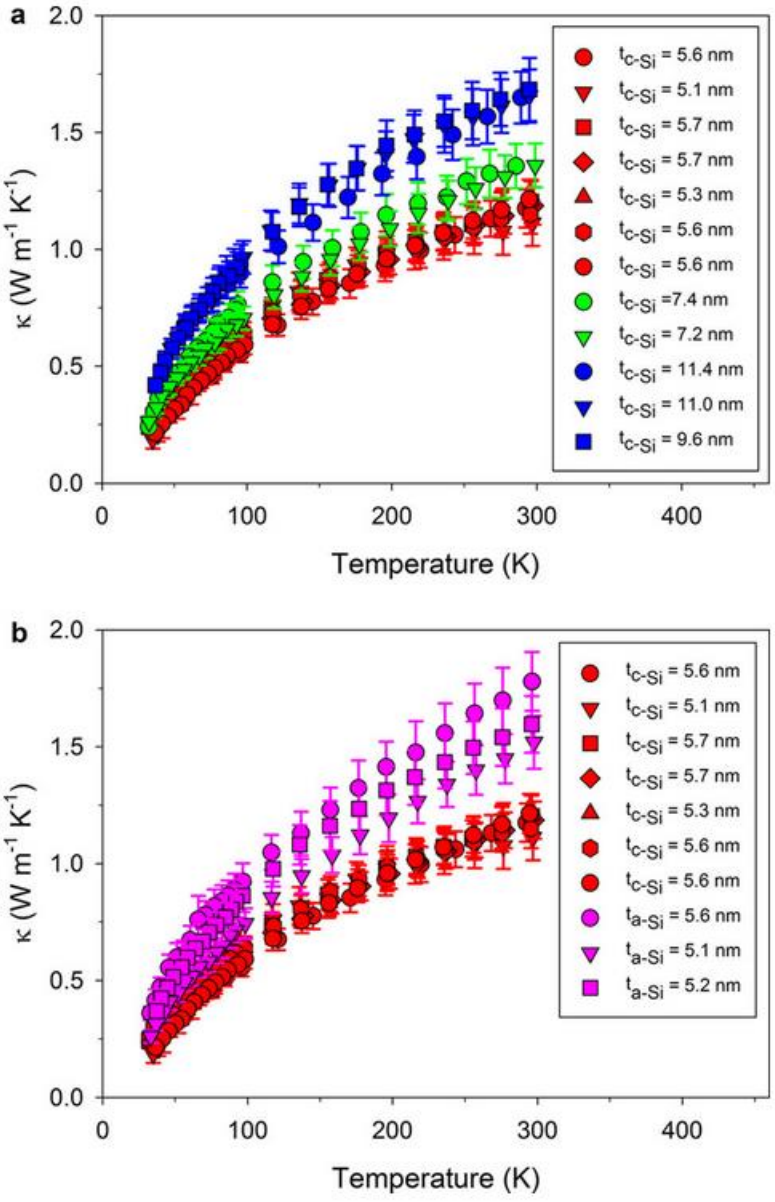

Figure 4.8. Thermal conductivity of silicon NTs: a) ~5, 7, and 10 nm c-Si NTs versus temperature and b) ~5 nm amorphous and crystalline NTs versus temperature. The dependence of thermal conductivity on shell thickness at room temperature is clearly visible in a), with a gradual decrease in thermal conductivity with decreasing thickness of the crystalline shell layer.

4.4. Contact resistance

To estimate the thermal contact resistance between the Si NTs and the suspended devices, we can use studies on similar systems, such as for Si NWs and multi-walled carbon nanotubes. Length dependent measurements 2-10 (μm) on VLS synthesized c-Si NWs with diameters ranging from 70-130 nm exhibited an average contact resistance for all samples of ~4.5×10^{6} K W^{-1}.[51] These NWs were Pt-C bonded onto suspended membranes similar to those used in this study, with NWs in contact with Pt electrodes and Pt-C bonding over ~1 μm long sections. Because of the similar OD and Pt-C contact bonding of the present Si NT samples, we can assume that the contact thermal resistance of our NT samples is of the same order of magnitude (1-10×10^{6} K W^{-1}), which is two to three orders of magnitude lower than the total measured thermal resistance of the NT samples (<1 nW K^{-1}). Therefore, we can conclude that the thermal contact resistance is negligible in the present Si NT samples. This is in agreement with the length dependent measurements seen in Supplementary Figure 4.9b). Another way to look at the relative role of the contact resistance is by examining the areal interfacial thermal resistance, which is typically on the order of 2×10-8 m^2 K W^{-1} or lower for common materials. For instance, MWCNTs with outer diameter OD) of 10 and 66 nm in contact with 2 μm wide Pt electrodes measured both with and without electron-deposited Au bonding.[52] The 66 nm OD MWCNT had a calculated contact width of ~4 nm and an areal contact resistance of 2.2×10^{-8} m^2 K W^{-1}. If we consider a 1 μm contact length for our Si NTs with similar values for contact width and areal contact resistance as the 66 nm MWCNT, then we have a contact resistance of ~5.5×10^{6} K W^{-1}, which is similar to that observed for the Si NWs previously mentioned.

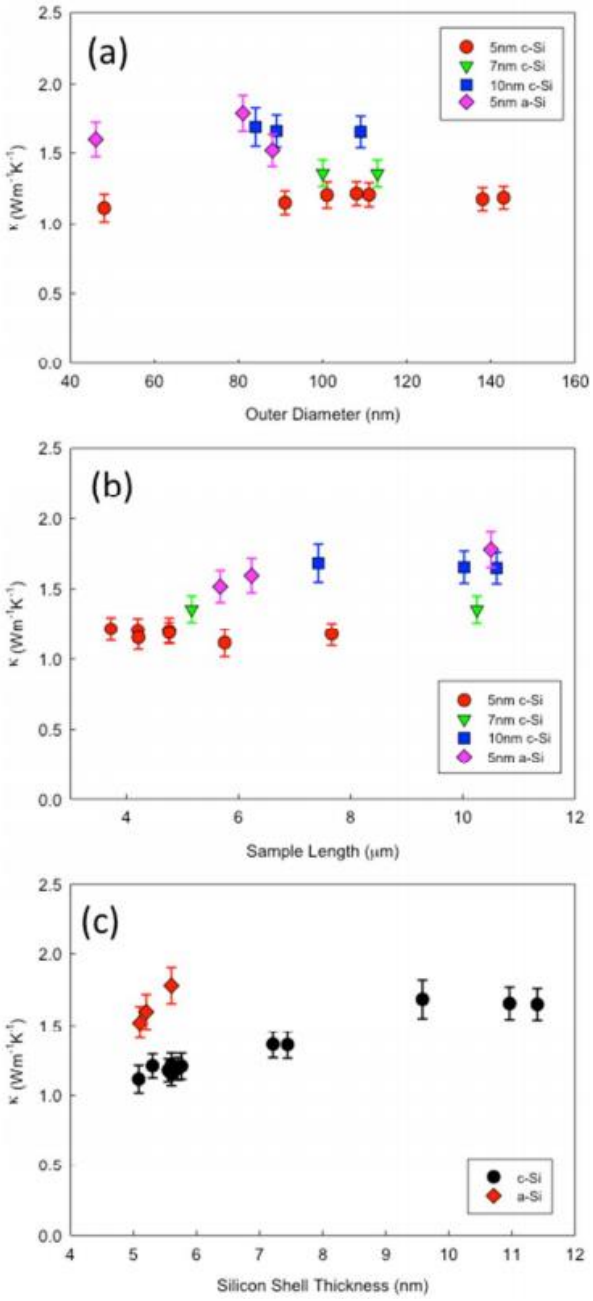

Figure 4.9. Thermal conductivity of crystalline and amorphous nanotubes versus a) outer diameter, b) suspended sample length, and c) shell thickness. There is no correlation between the measured nanotube thermal conductivity and the nanotube outer diameter for any of the crystalline or amorphous samples. This leaves the shell thickness as the sole dimension that strongly affects phonon scattering. Since thermal conductivity of the Si NTs is independent of the sample length, contact resistance between the nanotubes and the measurement devices is negligible. A clear size dependence on shell thickness can be seen in c) for c-Si NTs from 5 to 10 nm.

4.5. Phonon transport mechanism of ultra-thin crystalline Si nanotube

To develop an understanding of the extraordinarily low thermal conductivity in the crystalline Si NTs, it is necessary to first discuss the phonon transport mechanisms that occur in their amorphous counterparts. In amorphous Si, κ can be modeled as the sum of the contributions from two distinct vibrational modes, propagons and diffusons.[28] Propagons, as their name suggests, are propagating and delocalized modes and, in the case of a-Si, could possess a broad MFP possibly ranging from ~10 to ~40 or even 100s of nm.[1,29,30] Diffusons, on the other hand, are nonpropagating and delocalized modes, whose MFP is rather short (~0.5–10s of nm), albeit not well defined, and contribute to thermal conductivity by coupling with other modes through atomic disorder.[29,30] The diffuson contribution can be modeled using the Allen–Feldman theory[28] and is estimated to be ~1 W m^{-1} K^{-1} for a-Si, whereas the propagon contribution has been shown to exhibit a strong size dependence.[29] Therefore, our measurement results Figure 4.8b) suggest that the propagon contribution is about ~0.5 W m^{-1} K^{-1} for our 5 nm thick a-Si, indicating the important size effect for propagons even down to the 5 nm regime in the >5 μm long NTs, which has not previously been probed experimentally. Our results on a-Si NTs are also qualitatively in line with previous thermal conductivity measurements on thin films of a-Si, which show values ranging from 1.1 to 4.0 W m^{-1} K^{-1} over film thicknesses ranging from ~50 nm to tens of microns. The wide variation is presumably caused by the dependence of the thermal conductivity on a combination of factors including film fabrication method, film

thickness, growth temperature, and purity.[20,21] The thermal conductivity of the thinnest a-Si film at ~50 nm[22] was found to be 1.4 W m^{-1} K^{-1} while ion-amorphized ~17 nm thick films[31] were 1.7 W m^{-1} K^{-1}. The thermal conductivity values measured for a-Si NTs in this work are very similar to values measured for thin high-purity and fully dense a-Si films.

The MFP alone, however, cannot explain the subamorphous values of thermal conductivity in 5 nm c-Si NTs, as one would expect that phonons in the crystalline NTs would have MFP longer than that of propagons in disordered a-Si NTs with similar geometries. In addition to MFP, the thermal conductivity can also be influenced by the phonon group velocity v_g), which is characterized by the speed of sound in the low frequency limit, which has been proposed theoretically to decrease due to phonon confinement in NWs with diameter less than 20 nm.[32] The phonon specific heat could also increase due to excitation of low frequency phonon modes, leading to enhancement of the thermal conducitvity. However, these modes are only excited at very low temperatures. Consequently, specific heat is expected to be bulk-like even for 5 nm structures over the measured temperature range 35–300 K).[33-35] We hypothesize that phonon modes could have been altered in the ultrathin c-Si NTs, leading to a lower speed of sound and, consequently, contributing to the subamorphous thermal conductivity.

To experimentally verify this hypothesis, we indirectly measured the speed of sound *v*) in single Si NTs through tensile Young's modulus E) tests Figure 4.10a), as v is related to $E/\rho)^{1/2}$, where ρ is the mass density. Figure 4.10b shows the measured Young's moduli of a-Si and c-Si NTs, as well as literature data on Si NWs with larger

diameters 15–60 nm),[36] bulk c-Si,[36] and a-Si thin films.[37] Two c-Si NWs with diameters of 54 and 53 nm were used to calibrate the measurement and exhibited bulk-like elasticity, consistent with prior measurements on large-diameter Si NWs.[36] The averaged E of the three 5 nm crystalline NTs is 30.1 ± 2.7 GPa, or about six times lower than bulk Si. This drastically reduced E is consistent with previous studies on small diameter c-Si nanostructures including sub-25 nm NWs[36] and ~6 nm nanojunctions,[38] as well as the observed reduction of vg in InSb NWs.[39] Comparatively, three ~5 nm shell a-Si NTs were found to have an average modulus of 62.7 ± 6.5 GPa, within the range of measured elastic moduli of a-Si thin films[37] and nearly twice that of the crystalline NTs of the same size. This elastic softening in c-Si NTs stems from the growing importance of surface effects at reduced dimensions. Surface atoms have lower coordination numbers and electron densities than bulk atoms, requiring changes in bond spacing which leads to strain and surface stresses.[40,41] Meanwhile, simulations have shown that Si surface stresses are compressive in nature and require atomic reorganization and bond lengthening to reach an equilibrium state,[42,43] leading to elastic softening. Furthermore, other surface and interfacial effects may also play a role, such as the presence of native oxide layers.[40,44]

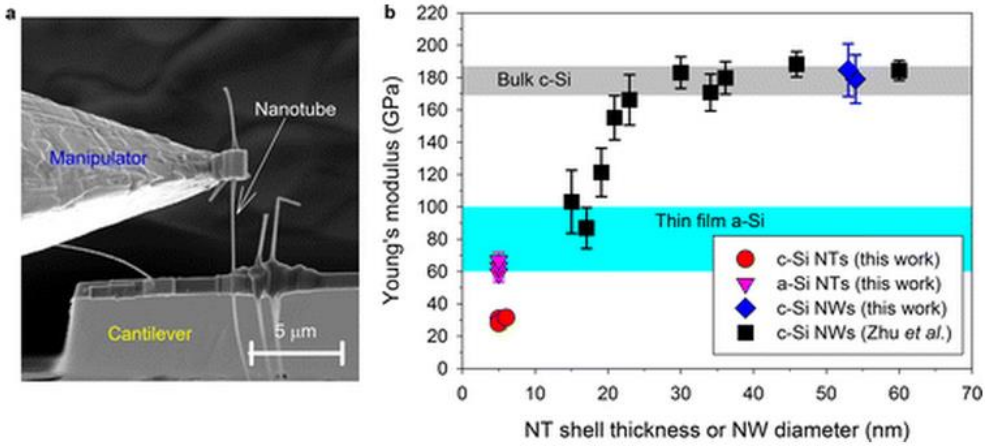

Figure 4.10. Elastic tensile tests: a) Elastic modulus tensile measurement using manipulator probe to pull NT attached to the end of an AFM cantilever. b) Elastic moduli of silicon NTs and NWs. ~5 nm amorphous NTs exhibit ~2× stiffer moduli than ~5 nm crystalline NTs. Values of elastic moduli of silicon NWs were taken from Zhu et al.[36] and expected ranges for bulk c-Si[36] and a-Si thin films[37] are shown.

The close correlation between thermal conductivity and elastic properties in Si NTs and NWs is clearly illustrated in Figure 4.11, which shows the κ^*/D^* ratio left axis) and $E^*)^{1/2}$ right axis), where κ^*, D^*, and E^* are κ, D, and E normalized with their respective values from ~60 nm Si NWs all values taken at 300 K), as a function of D, the shell thickness for NTs or the diameter for NWs, whichever is applicable. In the boundary scattering regime, the κ/D ratio scales with the phonon velocity $\kappa/D \sim C_v$, where C is the phonon heat capacity), whereas $\sqrt{E}$ is also a measure of the speed of sound $v = E/\rho)^{1/2}$). Figure 4.11 shows that there is an excellent match between the size effects on thermal and elastic properties within the size range considered here 5–60 nm). Above 25 nm, diffusive scattering at the NW surface dominates and κ^*/D^* and $E^*)^{1/2}$ are the same among NWs with different sizes, suggesting no change in v. This is also known as the boundary scattering or Casimir limit.[10] However, below 25 nm, κ^*/D^* markedly drops below unity, by as much as 50% in the 5 nm c-Si NTs. The

reduction in κ*/D* coincides exactly with the decline in E*)$^{1/2}$. Additionally, the previously measured 22 nm c-Si NW,[10] for which a theoretical explanation of the low κ has been elusive, matches very well with the observed trend of E*)$^{1/2}$. The close correlation between elastic and thermal properties suggests that the observed ultralow thermal conductivity in the 5 nm c-Si NTs is caused by elastic softening arising at these reduced dimensions. It is important to note that, because the NTs are softer compared to bulk Si, the actual theoretical κmin will be lower, by as much as ~50% or ~0.5 W m^{-1} K^{-1}) in our 5 nm c-Si NTs, due to its dependence on the speed of sound.[15] Therefore, the measured κ of 1.18 W m^{-1} K^{-1} is still substantially larger than what the theoretical κmin could be for such a soft material. Furthermore, even though the ~5 nm NTs are very small, approaching the phonon wavelength <6 nm at 300 K in bulk Si),[45] the transport is still largely three-dimensional, which warrants the applicability of the same "κ ~ Cvl" formula for all the NW and NT samples shown in Figure 4.11. One-dimensional 1-D) behavior is predicted to occur only at low-temperature <30 K) in structures approaching sizes comparable to half the dominant thermal wavelength.[33,46]

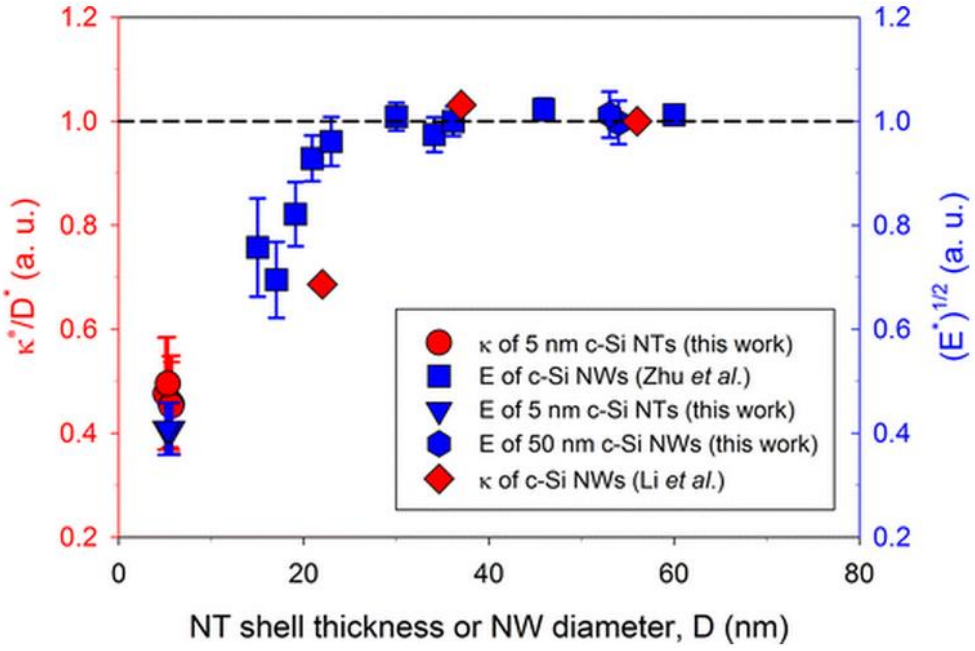

Figure 4.11. Correlation between thermal conductivity κ) and elastic modulus E) in crystalline NTs and NWs. κ, D, and E have been normalized with their respective values for ~60 nm Si NWs and plotted as a function of D, where D is the shell thickness for NTs or the diameter for NWs, whichever applicable. Normalized variables are labeled as κ*, D*, and E*, respectively, and the dashed line represents the maximum of both κ/D and √E. Above 25 nm, the nanostructure dimensions are smaller than the phonon MFPs, which limits the thermal conductivity due to diffuse phonon-boundary scattering. Below 25 nm, elastic softening in the nanostructure alters the phonon dispersion and causes a rapid decrease in thermal conductivity beyond the expected influence of boundary scattering. The κ/D and √E for ~5 nm thick c-Si NTs and c-Si NWs are from thermal and elastic measurements shown in Figures 2b and 3b, respectively, as well as literature values from Li et al.[10]

4.6. Equilibrium molecular dynamic analysis

In order to theoretically underpin and quantify the mechanisms leading to the measured ultralow thermal conductivity of c-Si NTs, we performed equilibrium molecular dynamics EMD) simulations of phonon transport in such structures. The employed molecular model system consists of a hollow c-Si NT with a-Si layers on both inner and outer shell surfaces. In order to directly compare simulations to experimental samples, the ID is chosen to be 20 nm and total thickness is about 5 nm. For all cases the thickness of the a-Si layer on both surfaces is about 2 nm. All molecular dynamics calculations were performed using the LAMMPS package,[53] and the original Stillinger-Weber SW) potential[54] was used to describe Si-Si interactions. A time-step of 0.25 fs was used throughout all simulations. The initial structure was cut from a perfect crystalline structure of bulk Si and the longitudinal direction of the NT was extended in the [110] direction. Next, the outer and inner surfaces with thickness pre-specified as 2 nm were heated to 5000 K and maintained at this temperature for 10 ps such that atoms in both regions melted. Subsequently, the regions were rapidly quenched down to 300 K in 0.5 ps such that the amorphous structure was formed. We then continued to relax the entire NT with an NPT constant particles, pressure, and temperature) ensemble for 100 ps. After relaxation, the thermal conductivity of the Si NTs was computed with an NVE constant particles and volume without thermostat) ensemble by integrating the heat flux autocorrelation function the Green-Kubo method)

$$\kappa = \frac{1}{Vk_BT^2}\int_0^{\tau_m}\langle Q_z(t)Q_z(t+t')\rangle dt' \,, \qquad (1)$$

where V is the volume of the NT which is considered a hollow cylinder, k_B is Boltzmann's constant, T is the absolute temperature, Q_z is the heat current along the longitudinal direction z) of the NT, τ_m is the autocorrelation length, and the angular brackets denote an average over time. In our EMD simulation, τ_m is chosen to be 50 ps and the total simulation time for a single run lasts over 2.5 ns. The final thermal conductivity results reported here were averaged over at least 5 independent runs by assigning different initial velocities in the NVE stage.

It is known that convergence can be a problem while running EMD simulations. To this end, we checked the length dependence of the thermal conductivity of Si NTs. For a selected case of total thickness 5nm, we simulated four different lengths 11.5, 15.4, 19.2, and 23.0 nm), but did not find any noticeable change in the calculated thermal conductivity for both amorphous coated crystalline NTs and fully amorphous NTs. Therefore, in order to save computational time, we chose a length of 15.4 nm for all EMD simulations. Figure 4.12a shows the calculated κ and E of an as-quenched c-Si NT. For all cases in Figure 4.12a, the inner diameter is 20 nm and the thickness of the amorphous layer on the inner and outer surfaces is 2 nm. The total thickness of the shell is varied from 5 to 10 nm. It is clear that, both the thermal conductivity and Young's modulus decrease with decreasing shell thickness, confirming the relationship between the thermal conductivity reduction and the softening of the elastic modulus, as revealed by the experiments Figures 3 and 4). In order to imitate realistic experimental conditions where roughness at the crystalline/amorphous interface is inevitable, for the case of inner diameter of 20 nm and total thickness of 5 nm, we also considered the presence of such roughness by

randomly removing up to 80% of the interface atoms on the crystalline sides and investigated its effects on κ and E. A total thickness of 5 nm, as opposed to the smallest total shell thickness measured experimentally ~7 nm, i.e., ~5 nm Si with ~1 nm oxide on each side), was used due to computational limitations. Nevertheless, it is clearly shown in Figure 4.12b that, upon interface roughening, both κ and E are reduced compared to the as-quenched interface, which again demonstrates the close correlation between κ and E, as we observed experimentally. Furthermore, the vibrational density of states VDOS) of the amorphous layer in the high frequency regime is significantly reduced compared to the crystalline layer and the entire VDOS shifts toward low frequencies Figure 4.13). This results in a large vibrational mismatch between the crystalline and amorphous layers thereby causing strong phonon scattering at the crystalline/amorphous interface, which leads to the ultralow thermal conductivity in amorphous coated c-Si NTs. We would like to note that it is more informative to view the MD simulations as a tool to illustrate possible mechanisms giving rise to the experimental observations, which in this case is the close correlation between thermal conductivity and elastic properties. It is difficult to quantitatively compare the MD and experimental results due to the various inherent differences, including but not limited to interatomic potential, surface roughness, native oxide, and defects.

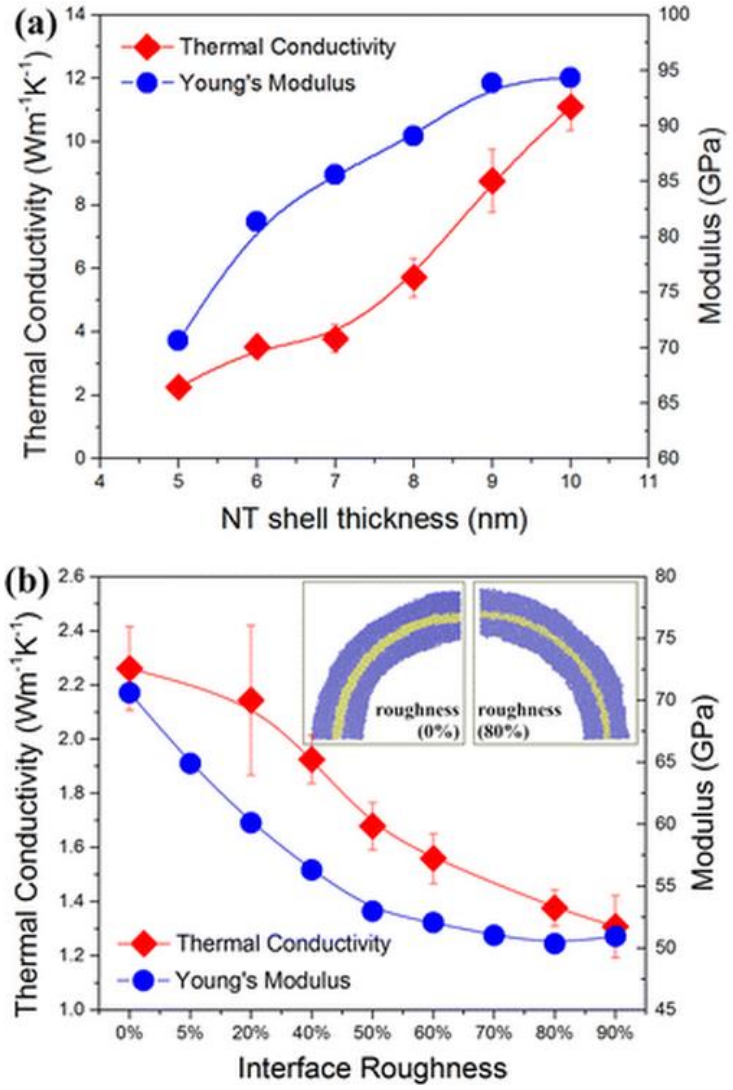

Figure 4.12. a) EMD simulation of thermal conductivity and elastic modulus with different NT thickness. The interface between amorphous layer and crystalline part is the as-grown condition, which is quenched from the high temperature liquid phase of the amorphous region see Supporting Information for details). b) EMD simulation of thermal conductivity and elastic modulus reduction with c-Si NT interface roughness. Interface roughness is achieved through random removal of atoms on the crystalline face of the crystalline shell-amorphous coating interface. The insets show two typical atomic structures of the Si NTs with different interface roughness. Color coding: yellow, c-Si; blue, amorphous layer.

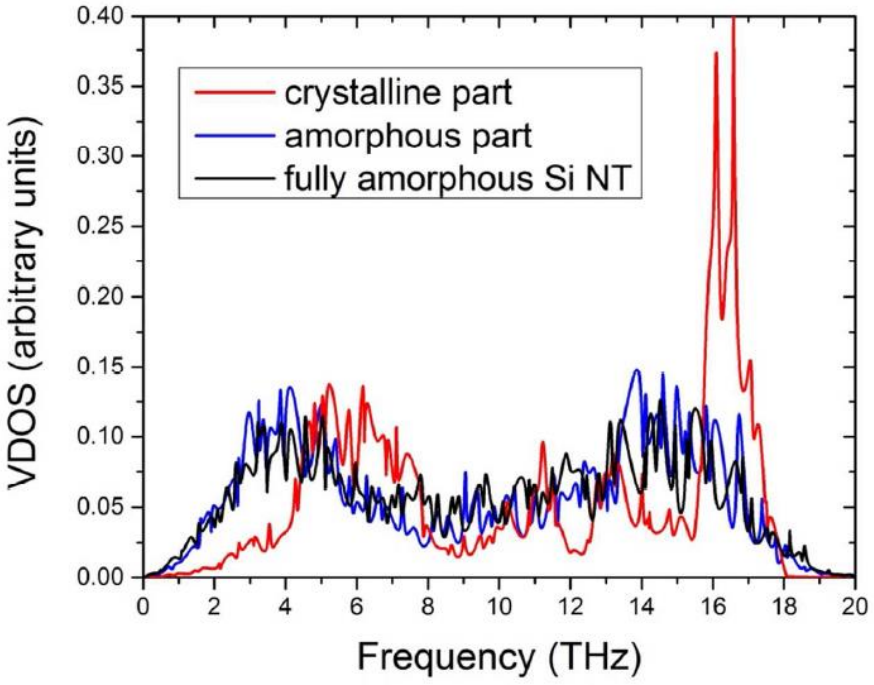

Figure 4.13. Comparison of vibrational density of states from EMD simulation in crystalline and amorphous layers in a thin Si nanotube with inner diameter of 20 nm and total thickness of 5 nm including 2 nm amorphous layer on inner and outer surfaces. The VDOS of a pure amorphous Si nanotube is also shown for comparison. The VDOS is calculated by a Fourier transform of the atomic velocity autocorrelation function.

4.7. Conclusion

The close link between thermal and elastic properties discovered from the ultrathin c-Si NTs reveals that one can engineer the thermal properties of crystalline nanostructures beyond the phonon boundary scattering limit via the phonon softening effect and consequently achieve thermal conductivities in crystalline structures below their amorphous analogues. This finding paves the way for new approaches to reduce thermal conductivity in nanostructures, which has been a key obstacle and the topic of voluminous research, such as in the field of thermoelectrics,[9] over the past decade. Moreover, understanding the thermal and mechanical behavior of materials with ultrasmall length scale is critical for the design and performance prediction of a diverse range of technologies including flexible nanowire electronics,[47] nanoelectrode materials for batteries,[48] and nanoelectromechanical systems.[49]

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Chapter 5: Bottom-up nanowire array optical polarizer for high stretchable and printable display

Designing optical components such as polarizers on substrates with high mechanical flexibility realizes new platforms in photonics, wearable electronics, and sensors. Conventional manufacture approaches which rely mostly on top-down lithography, deposition, and etching suffer from low process tolerance and therefore an alternative way of integration scheme is necessary. Here, we demonstrate wire grid polarizers WGPs) on flexible/stretchable substrates by printing as-grown Ge or Ge/Si core/shell nanowires NWs) on planar substrates creating highly dense and well-ordered fashion to impose polarization effect of high contrast for optical polarizer sheets. The maximum contrast ratio of 104 between transverse electric TE) and transverse magnetic TM) fields and 99.7% of light blocking efficiency across the visible spectrum range are achieved. Further systematic analyses are performed both in experiment and finite element model to reveal the correspondence between physical factors coverage ratio of NW arrays and diameter) and polarization efficiency. Moreover, we demonstrate distinctive merits of our approach: i) high flexibility in choice of substrate such as glass, plastic, or elastomer; ii) easily combined with novel functional group, for example, air permeable, flexible/stretchable, biocompatible, and skin-like low mechanical modulus; iii) localized printing on a designated area, which are greatly challenging from top-down approach.

5.1. Introduction

Polarizer is one of the most common techniques that enable control of electromagnetic waves in various optical instruments and display systems.. Wire grid polarizer WGP), since invented at mid-1920 by Land[1], has become a major components in modern liquid crystal displays LCDs) to modulate visual feedback in the realm of ubiquitous personal and mobile computing[2, 3] Moving further, innovations in consumer portable and wearable electronic products have demanded development of electronic and photonic components that are compatible with a variety of new solid-state substrates, for example in the form of glasses, clothing, adhesive patch etc. Such circumstance introduces new process requirements in device fabrication such as biocompatibility, versatile in substrate choices, flexibility/stretchability, mechanical softness and air permeability.[4,5] The traditional top-down semiconductor manufacturing approach, however, struggle to harmonize with these new standards due to the monolithic nature of the individual processing steps that render material choices limited by thermal budget constraints or material lattice mismatch constraints, and geometry choices limited to planar substrates.[6] Therefore, new design and fabrication strategies to satisfy these compatibility requirements are essential to fulfill the trends in future. Design of device components through nanostructure assembly via bottom-up approach such as from well-ordered nanowire or nanocolloids can provide alternative routes to overcome the drawbacks of traditional fabrication systems as well as introduce new novel functionalities such as ballistic transport[7], nanoscale energy converter[8], nanoelectromechanical system[9], phonon engineering[10], tunable light emission and absorption[11], and high detection sensitivity[12]. Intense efforts have been

focused on development of assembly methods to be more process efficient and fine control of these bottom-up building blocks into macroscale functional systems in the fields of nanoelectronics and photonics, for example, Langmuir-Blodgett[13], micro fluidic[14], ink-jet[15], dielectrophoresis[16], self-assembly[17], and contact printing[18].

Among the nano-building blocks, semiconductor NWs, by virtue of their high aspect ratio and a thickness less than a few tens of nanometers, have demonstrated themselves as an excellent flexible device component[19-21]. Moreover, intensive studies on optical properties of these nanowires reveal their unique characteristics as a light absorber and scattering source correlated to their shape and geometry[22, 23]. Barrelet et al. have shown low loss waveguide nature of CdS NWs from direct measurement of light guiding effect along the length direction of NWs[23]. Cao et al. demonstrated resonance behavior of Ge and Si NWs showing strong polarization sensitive spectra of incoming light absorption and scattering features in visible spectrum range[24]. Both high mechanical flexibility and optical cavity resonator effect allow the semiconductor NWs to function as excellent building blocks of optical devices well-fitted to the wearable optoelectronics framework. In addition, a wide range of selection in dimension, material composite, and heterostructure provides highly tunable optical behaviors such as transmission/absorption spectrum and resonance modes[25-27]. Several fundamental studies were made on polarization effect of semiconductor NWs[28-30], however, there was no direct integration of polarization property of NWs into macroscopic device system.

Here, we demonstrate a new design concept of WGPs using Ge or Ge/Si core/shell NWs and a simple and robust printing method creating arrays of aligned

NWs in subwavelength feature. Integration of these finely printed NW arrays with transparent substrates, polyethylene terephthalate PET) and polydimethylsiloxane) PDMS) elastomer, enables design of soft optical filters possessing multi-functional and human-friendly characteristics such as biocompatibility[31], air permeability[4], stretchability, and conformal lamination on complex shaped/curvy substrates. Assembled NW arrays show misalignment of ~5° to implement high quality optical polarizer with contrast difference exceeding 100 times between transverse electric TE) and transverse magnetic TM) mode and blocking efficiency of 99.7% of incident TE light across the visible spectrum range. We have further systematically studied the performance of our NW-WGPs as a function of NW coverage/diameter and further demonstrate their optical characteristics under circumstance of NW polarizers laminated on various wavy/folded substrates and stretchability. With such performance and noticeable features our new NW-WGPs offer a great potential in the development of human-device interface and communication system in the field of wearable electronics.

5.2. Printable nanowire polarizer from bottom-up

Inspired by aforementioned advantages of semiconductor NWs, we have successfully fabricated NW-PET/NW-PDMS WGPs as shown in Figure 5.1 where arrays of either Ge or Ge/Si core/shell NWs are used as light scatter or absorption sources. The overall fabrication process is depicted in Figure 5.1a. To begin with, either Ge or Ge/Si core/shell NWs were synthesized by chemical vapor deposition process. For Ge NWs, they were grown on Si substrates using 2% of GeH_4 in

hydrogen as precursor gas source at 290℃ and 300 torr for 2 hours. For Ge/Si core/shell NWs, on the top of same Ge core growth, ~2 nm of Si shell was deposited by 2% SiH_4 in hydrogen at 465℃, 100 torr for 10 min. The size of Ge NWs which affects the transmission spectra of NW-WGPs was controlled by the size of gold colloids Ted Pella) ranging from 15~40 nm. Si wafer with as-grown NWs of 60~80 μm length were further diced into 2~5 cm square pieces to be ready for the transfer on a transparent ~150 μm thick PET substrate. To transform randomly oriented NWs forest into compact and parallel fashion, we use mechanical contact transfer[32] where donor substrates NWs forest grown on Si substrates) are slide over the receiver substrate PET) by directional shear force. The van del Waals force between NWs and the receiver substrate plays a major role in alignment of NWs by anchoring portion of bent NWs on the surface of the receiver substrate while the whole donor substrate glide across the printing zone by directional sliding 1~2 mm/sec) result in highly ordered NW arrays in parallel manner.

It is important to note that we have suffered to enhance the maximum contrast ratio, defined as a ratio of TM over TE transmission, above ~10 regardless of increased number of repeated printing of NWs on the device substrate. This obstacle may cause by detachment of NWs by NW to NW friction[32] limiting the increase of density of NW array. Therefore, to keep the high transfer efficiency and achieve subwavelength pitch-to-pitch distance array of NWs for sufficient contrast ratio and light blocking efficiency as a polarizer, we introduce fresh layers of PMMA, spin coated 4000 rpm, 40 sec, ~120 nm thickness) on top of the predefined NW array, as new intermediate transfer layers to reduce the frictional loss as well as to enhance

stiction and transfer. After 5 to 7 times of repeated transfers, interim PMMA layers were gently removed by optimized low power oxygen plasma process minimizing the damage on the PET substrate and obtain overall endurable and close-packed layer of NW array. Figure 5.1b shows the result of dense and well-ordered Ge NW array with reddish brown color on a PET substrate. The SEM images from top view in Figure 5.1c shows alignment of NW array with fine distances among NWs.

Fabrication of NW-PDMS WGPs can be realized by continuous process from the NW-PET WGPs. Printing NWs directly on the PDMS fails to create alignment because of the adhesive surface of PDMS causing randomized dispersion of NWs which is useless for the polarizer application. Instead, we adopted more simple way, by pouring viscous PDMS-curing agent mixture with ratio of 10:1 on top of the NW-PET WGPs followed by spinning of substrate to control thickness of PDMS and final curing to have soft elastomer substrate. Sufficient amount of curing time ~3 hours) was applied in vacuum condition to achieve full infiltration of liquid PDMS into NW array followed by additional curing of PDMS at 50 ℃ to create robust NW-PDMS film. After PDMS is totally cured, it is ready to be gently peeled off from the original PET substrate to obtain NW-PDMS WGP. The result of NW incubation into PDMS substrate is displayed in Figure 5.1d showing that degree of alignment and compactness of NW array are still well maintained. The smooth surface from 45° tilted view in Figure 5.1e shows complete embedding of NW array into PDMS indicating liquid phase PDMS was fully infiltrated into the array of NWs to form a robust NW-PDMS film. The demonstration of fully functional NW-WGP is displayed in Figure 5.1f) and 1g) under TM incident light polarized parallel to the NW axial

direction) and TE incident light polarized perpendicular to the NW array) fields respectively. The obvious difference in visibility of the background image for TE and TM conditions demonstrates high blocking efficiency of NW optical filter across the visible wavelength range and further illuminates the potential of this fabrication technique to create high performance WGPs. Quantitative characterization of such high performance of NW-WGP is shown in Figure 5.1h) and 1i) with detail measurement set up depicted in Figure 5.2. In Figure 5.1h), transmission spectra under TM and TE incidence across the visible wavelength are displayed. The trend for TM transmission shows gradual increase from 12% to 64% across the visible range from 400 to 800 nm) while TE transmission shows a trench with its minimum presented near 600 nm wavelength. Trend of TE-polarized spectrum is more obvious in log sale where the blocking of incident light appears to be below 1% across 400 to 650 nm with the minimum of 0.3% at 595 nm wavelength proving its potential as a high quality optical filter. The contrast ratio is also depicted in Figure 5.1i) showing its maximum of 104 at 595 nm. This implies the bandwidth characteristic of NW polarizer is heavily dependent on the TE-polarization which is correlated to the dielectric dispersion response of Ge NW array. The inset of Figure 5.1i shows measured 360˚ polarization angle dependence of transmission red dotted line) in agreement with a calculated curve from Malus' law[33] blue solid line).

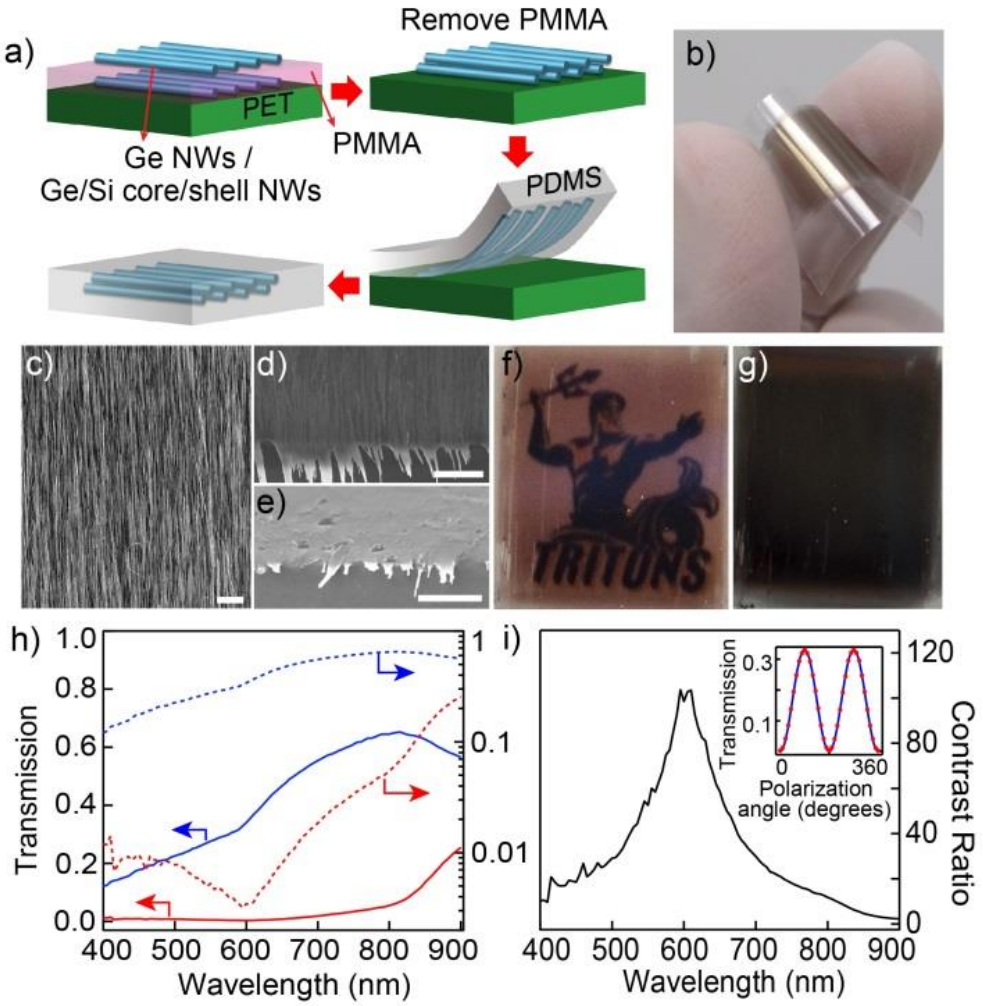

Figure 5.1. a) Schematics of fabrication process of printed NW WGP on a plastic PET) or elastomer PDMS). Multiple printing of randomly oriented NWs on the growth substrates mediated by PMMA sacrificial layers are transferred on a PET sheet and finally embedded in PDMS. b) Photography of NW WGP on a thin PET sheet. c) SEM images of NW WGP on PET and d,e) PDMS showing compact and highly ordered NW array. e) 45˚ tilted-view SEM image shows embedded NW array beneath PDMS surface. All scale bars are 10 μm. f,g) Demonstration of printed NW WGP for TM and TE-polarized incident wave with assist of commercial polarizer positioned on top of NW WGP. h) Linear solid lines) and log dashed lines) scale of TM blue lines) and TE red lines) transmission spectra of NW polarizer. i) Contrast ratio extracted from TM and TE transmission spectra. Inset shows measured polarization angle dependent transmission at a wavelength of 595 nm red dash line) in agreement with a calculated curve from Malus' law $I=I_0 \cos 2\theta$; blue solid line).

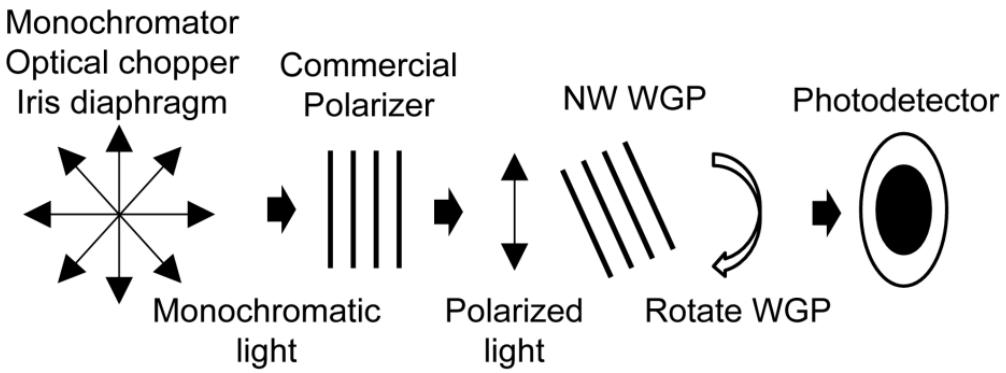

Figure 5.2. Diagram of optical transmission measurement set up.

The transmission data was collected using monochromator Horiba Jobin Yvon iHR550) equipped with 1200 groove/mm grating and 330 nm blaze combined with calibrated photodetector Newport), lock-in amplifier SR530), and 100 W halogen lamp Osram 64628) as an incident light source. As described in Figure 5.2, polarized monochromatic light source with 0.5×0.5 mm spot size is created by incoming light pass through series of monochromator, optical chopper, iris diaphragm, and commercial polarizer mounted on an optical table with all components aligned along the optical axis. Optical chopper is synchronized with the lock-in amplifier to provide an accurate and stable reference frequency. NW WGP is mounted on a rotatable stage and finally the light intensity is detected by the photodetector. Prior to the measurement on NW WGP, reference spectrums are obtained on a blank PET or PDMS sheet to extract substrate effect.

5.3. Working principle of semiconductor nanowire polarizer

The mechanism behind such high contrast ratio of semiconducting NW arrays differs from the metallic WGPs which relies on the plasmonic effect of electrons on the metal surface[34, 35]. These dielectric NWs achieve their polarization by absorption/scattering through the multiple internal reflections of photons along the length of NWs[36, 37] originate from high contrast of dielectric constant mismatch between NWs and their surroundings. To gain quantitative understanding on how the preparation of the NW WGPs affects the performance of polarizers, we first analyze the coverage effect of NWs on the polarization efficiency defined as ν=TM-TE)/TM+TE). In Figure 5.3a, 7 samples with varying fill factor ratio of covered area by NW arrays and whole region of investigation under SEM) are chosen to explore how does spatial distribution of NW arrays on a transparent substrate affects the polarization efficiency. Estimation of fill factor from each SEM image was done by using the threshold tool in imageJ image processing software. The degree of misalignments for all samples are controlled to be less than 7° analyzed by fast Fourier transform technique[38]. For the accuracy of the study, the incident beam spot on the samples were marked on each measured sample prior to the measurements and corresponding NW density and degree of alignment were captured by SEM afterward. As the portion of covered area increases from 6 to 78%, the polarization efficiency rise linearly from 0.08 to 0.84. Side by side SEM images corresponding to each data point visualize differences in NW coverage while maintaining similar degree of alignment.

In single Ge NW photocavity, there is a tendency of red shift in the absorption spectrum correlated to the increase in diameter of a single NW caused by photon

confinement effect[24]. Our interest, therefore, is to explore the polarization characteristics of these quasi-periodic and mono-layer dispersed arrays of Ge NWs linked to their size dispersion of Ge dielectrics Figure 5.3b). For such purpose, three NW WGPs having distinctive size distribution of 25±7 nm, 33±8 nm, and 47±9 nm were chosen to compare the spectrum of polarization efficiency accompany with two-dimensional finite element modeling FEM). NW arrays of three diameters, 25 nm, 33 nm, and 47 nm are controlled to have misalignment of 3.5°, 4.8°, and 5.8° and periods of 259±132 nm, 248±115 nm, and 255±93 nm respectively in order to highlight the size effect of NWs on polarization spectrum. The FEM model assumes infinitely long Ge NWs in parallel and size of NW and pitch to pitch distance are provided from the SEM study on each NW polarizer. In addition, we use bulk Ge dispersion spectrum for real and imaginary part[39] and calculates the zeroth-order transmission. In Figure 5.3b, efficiency spectra of experiment show broader and lower features compare to the simulated results probably due to the large standard deviation of periods from their mean values and defects on NW array created during the fabrication process. From both experiment and numerical calculation, a linear shift of efficiency maxima from 600 nm to 640 nm is observed as the diameter of NWs increase. From additional numerical studies visualizing the effect of NW pitch to pitch distance on TE spectra minima TE_{min}) and effective reflective indices of NW array see Figure 5.4a and b), we found that dielectric responses of NW arrays to the wavelength of incident light become weaker as the diameter of NWs shrinks down. This results in less sensitive changes of TE_{min} versus period of NWs which explains the diameter dependence of polarization spectrum shift. The study on the size effect of NW arrays provides an

insight into optimizing design of NW arrays as optical filters, for example, broadband application, such as polarizer, can benefit from combination of different diameters to broaden the spectrum profile, while on the other hand, examples like color filters require a narrow bandwidth. The results also specifically demonstrate that smaller size is preferable for Ge NW array in case of polarizer application because the polarization effect appears more dominant in visible light range.

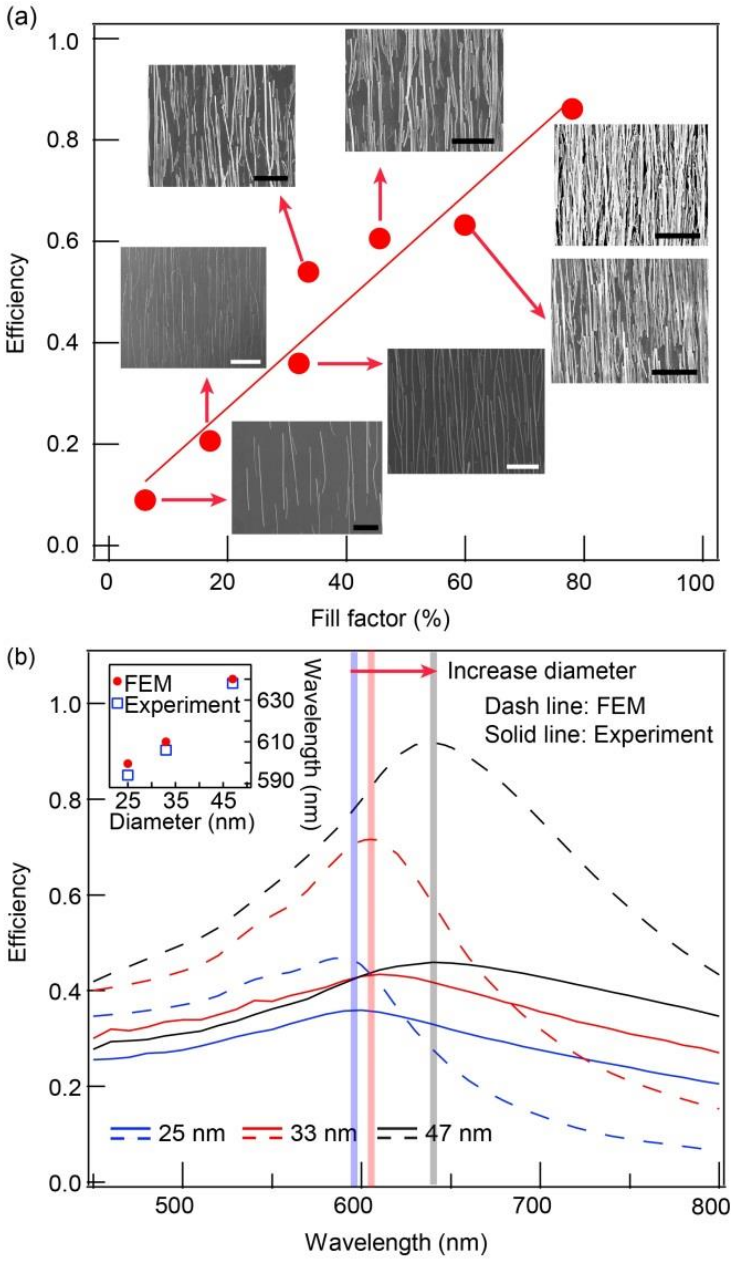

Figure 5.3. Effect of geometric factors NW filling density and size distribution) of Ge NW arrays on the polarization efficiency. a) NW fill factor versus efficiency where SEM images are presented next to the each corresponding data point. All scale bars, 2 μm. b) Polarizer efficiency as a function of NW diameter. Three samples with average size of 47 nm black), 33 nm red), and 25 nm blue) are studied both experimentally and numerically. Measurement and FEM simulation results are displayed in solid and dotted lines, respectively. Left top inset shows the shift of wavelength position at maxima of efficiency curves.

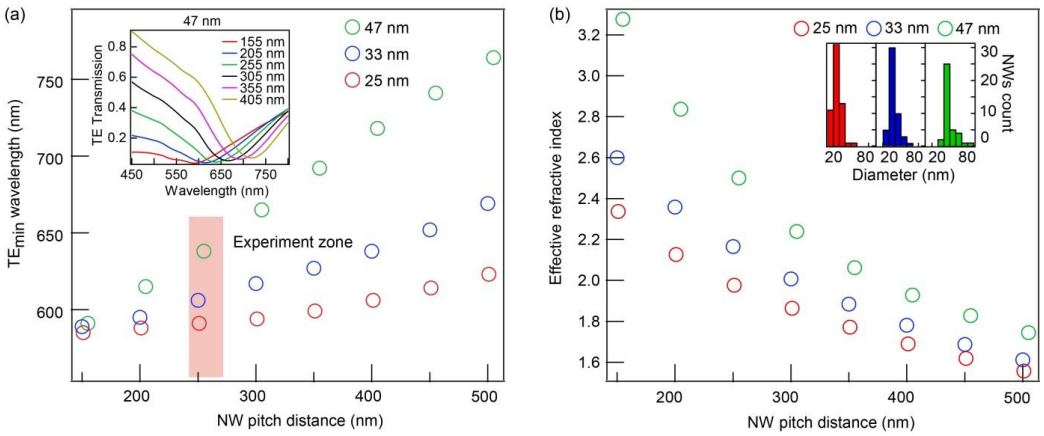

Figure 5.4. Effect of varying NW pitch distance on a) location of TE spectra minima and b) effective refractive indices, $n_{eff} = \sqrt{F n_{Ge}^2 + (1-F) n_{air}^2}$, for three different NW diameters where F is the fill factor of Ge array and n_{Ge} and n_{air} are the refractive index of Ge NWs and air, respectively. All three curves in figure a) show red shift while larger increment is observed with increasing of NW diameter. Three experiment samples are located within the highlighted red box. Inset of a) shows the trend of TE spectrum shift for 6 different periods of NW array in case of NW diameter of 47 nm in average. In figure b), changes of n_{eff} are more dramatic for larger NWs which may correspond to the slope of TE_{min} shift. Inset of b) shows the diameter distribution of three samples used for experiment where the mean values are located at 25 nm, 33 nm, and 47 nm respectively.

5.4. High mechanical tolerance of nanowire polarizer

One of the distinctive merit of NW-PDMS WGPs apart from the traditional design on the rigid substrates is a high degree of deformability that originates from the low mechanical modulus of PDMS and softness of NWs[40, 41] in conjunction with conformal contact on a curvy surface as the overall thickness of NW-PDMS films can be shrunk down to a few mm or even hundreds of m thin. In order to demonstrate this characteristic, as shown in Figure 5.5a and b, we overlay the NW-PDMS WGP on spherical glassware with 2 cm of radius of curvature or folded transparent plastic sheet and visualize the polarization effect by overlapping and rotating an additional commercial polarizer under fluorescent room-light. Noticeably, Figure 5.5a and b show that both WGPs are well adhered without any lift off from the high curvature surface caused by stretching/bending stress. Within such configurations the polarization performance is still highly retained as a background image for TM mode center) is clearly visible compared with near zero visibility for TE mode right). As a further example of feasible application, NW-PDMS WGPs, 90° off phase to each other, are attached on two curved glass lenses of 1 inch in diameter and aligned side by side to mimic smart contact lens for three-dimensional virtual imaging effect as shown in Figure 5.5c-e). In general, 3D display is achieved by creating illusion of depth with a slightly different image to each eye while in our case two different images are used to verify the operation of two WGPs respectively. Figure 5.5d and e clearly demonstrate the high performance of NW-PDMS WGP visualizing/blocking two different side-by-side background images while the reddish brown color originates from the dielectric dispersion spectrum of Ge NW array. To explore such

excellent mechanical adaptability of NW WGP in more quantitative way, we examine TM/TE transmission and polarization efficiency of NW-PDMS WGPs as a function of strain displayed in Figure 5.6. Stretching direction was chosen vertical to the length of NW array as shown in top right inset of Figure 5.6 which is expected to have more dramatic effect on polarization performance than pulling in parallel to NW lateral axis. To acquire reliable measurements, the two ends of NW-PDMS film are fastened on the stretching instrument and pre-examined that there is no loose after stretching and releasing of the film. Transmission spectrums are measured at each step of stretching among total 6 steps from 0 to 30% strain as shown in Figure 5.7 and finally measured when the film is released back to zero strain. During the stretching from 0 to 30% at 600 nm wavelength, both TM and TE show gradual linear increase (from 50.7% to 54.1% and 5.1% to 6.2%). After strain is released back to zero, transmission intensity of TM and TE match to the original values implying durable and reversible polarizer film containing high mechanical tolerance. Comparison between non-stretched and maximum of 30% stretched over visible spectrum range for TM, TE, and polarization efficiency are presented in Figure 5.6. The study reveals the slight decrease in efficiency starts to appear below 620 nm wavelength and from 400 to 560 nm the percentage of efficiency loss is around 7.0±1.2 after 30% strain while above 630 nm it is negligible. Since the period of NW grids should be less than $\lambda/2$ to be fully functional as polarizer[4], the measurement indicates that average period of NW array still maintains subwavelength feature even at 30% of elastic tensile strain.

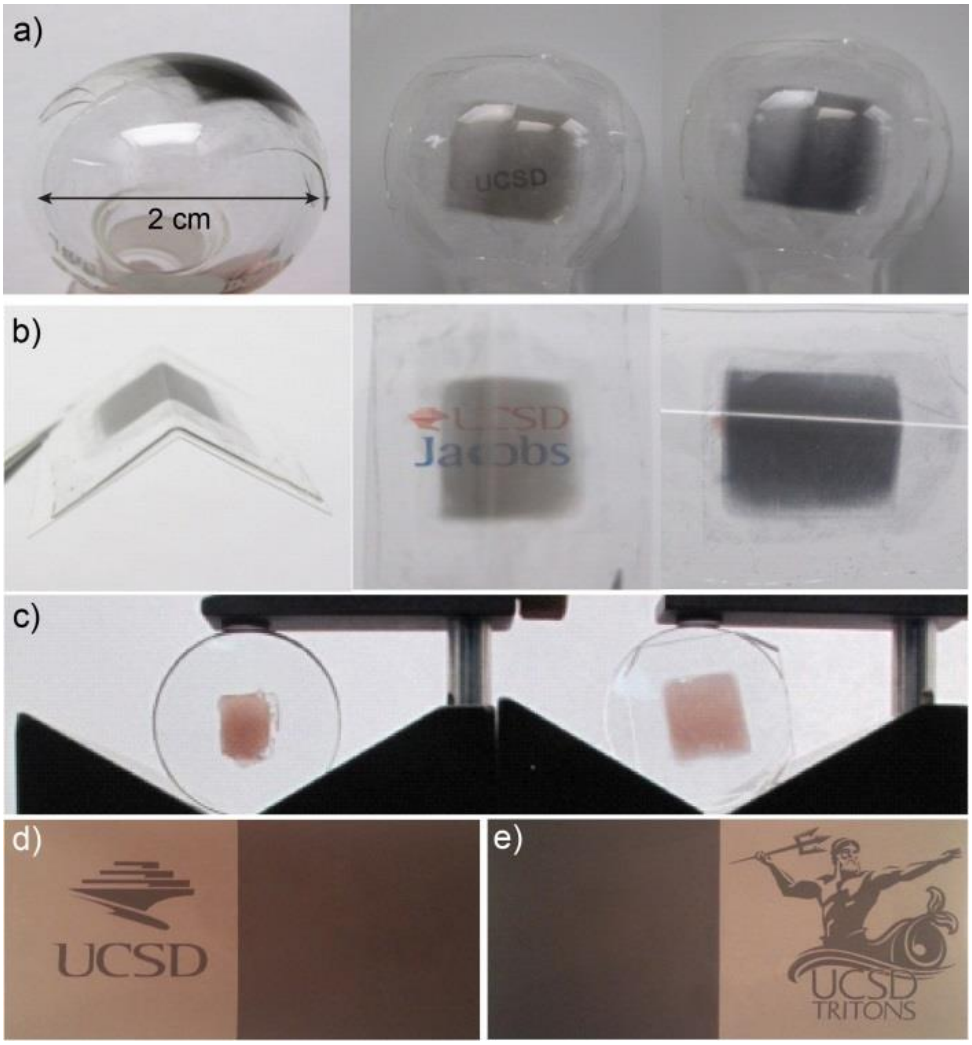

Figure 5.5. Performance and applications of NW-PDMS WGPs. a) NW-PDMS WGPs laminated on spherical glassware with 1 cm of radius of curvature and b) on a fold plastic sheet. Polarizer performance under TM center column) and TE right column) transmission are shown. c-e) Demonstration of NW-PDMS WGPs in three-dimensional imaging system. Two WGPs are adhered on the surface of curved lens. Photos are taken under TM and TE polarized conditions.

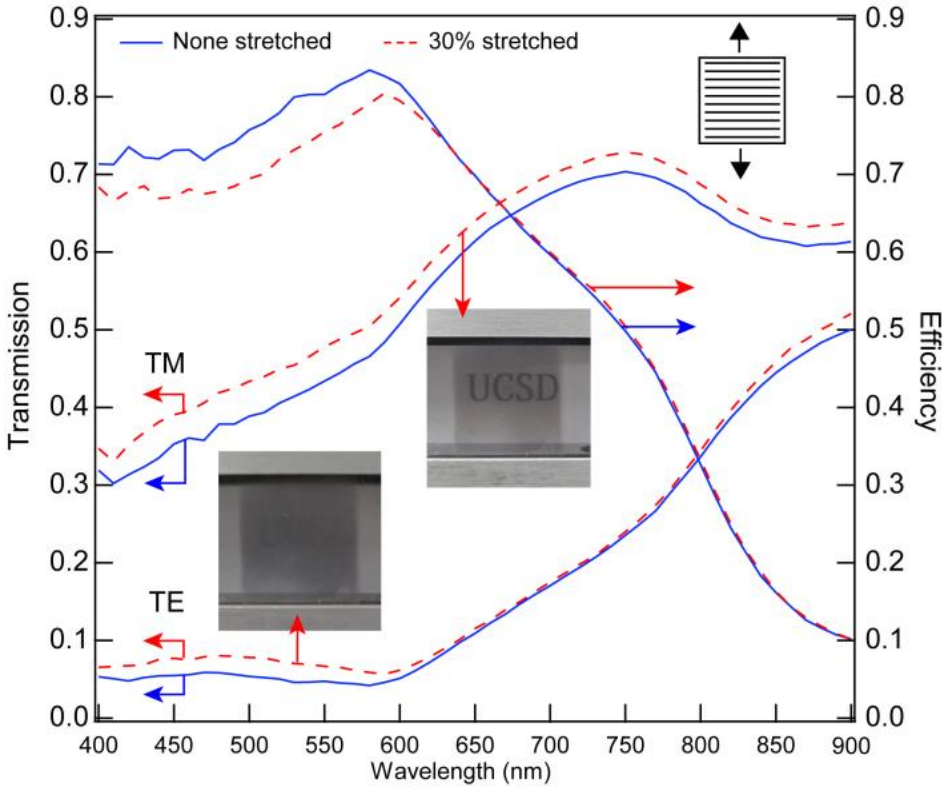

Figure 5.6. NW-PDMS WGP transmission and efficiency spectra before and after stretch. Strain orientation is vertical to NW alignment direction indicated in the top right inset. Solid and dash lines represent performances at non-stretched and 30% stretched cases, respectively. Two photographs visualize the performances of polarizer at stretched condition under TM and TE polarization.

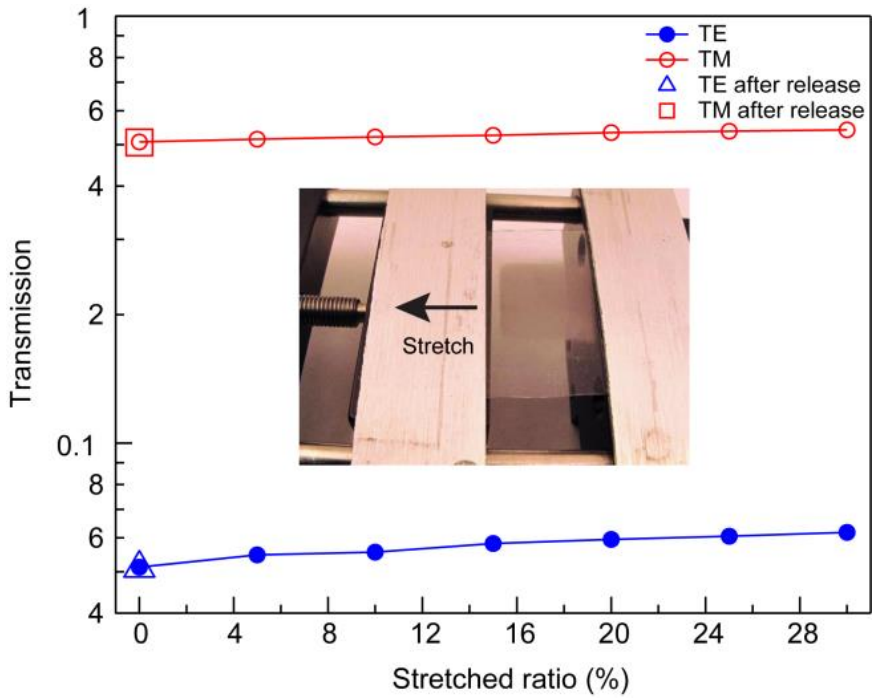

Figure 5.7. Stretching test on NW-PDMS WGP. Transmission of NW WGP is measured with 6 steps of stretching from 0 to 30% of strain. After 30% of stretching the sheet is released back to non-stretched state indicated as empty square and triangle markers.

5.5. Local printing of nanowire polarizer at selected area

In addition to soft conformal contact and stretchability, NW-PDMS WGPs are eligible for printing selectively on local area with preferable polarizing orientation similar to simple imprinting of mold on a substrate. This new concept provides micro-patterning of polarizer creating localized screening/visualization effect of information display with much simplified process detouring sophisticated lithography, etching, and deposition steps. As an example of this concept shown in Figure 5.8a, we designed, at first on a PET sheet, two adjacent areas printed with NW arrays to have 90˚ off phase to each other followed by transfer of whole NWs layer onto a PDMS sheet. Figure 5.8b shows the final result of double-phase NW-PDMS WGPs patterned on a single

PDMS sheet with clearly defined boundary between two parts along with a demonstration of localized polarizers at 0˚ and 90˚ phases where both top and bottom parts exhibit excellent TM and TE performances. Such feature verifies the promise of this technique that variety of substrates can be easily printed to have polarizing effect.

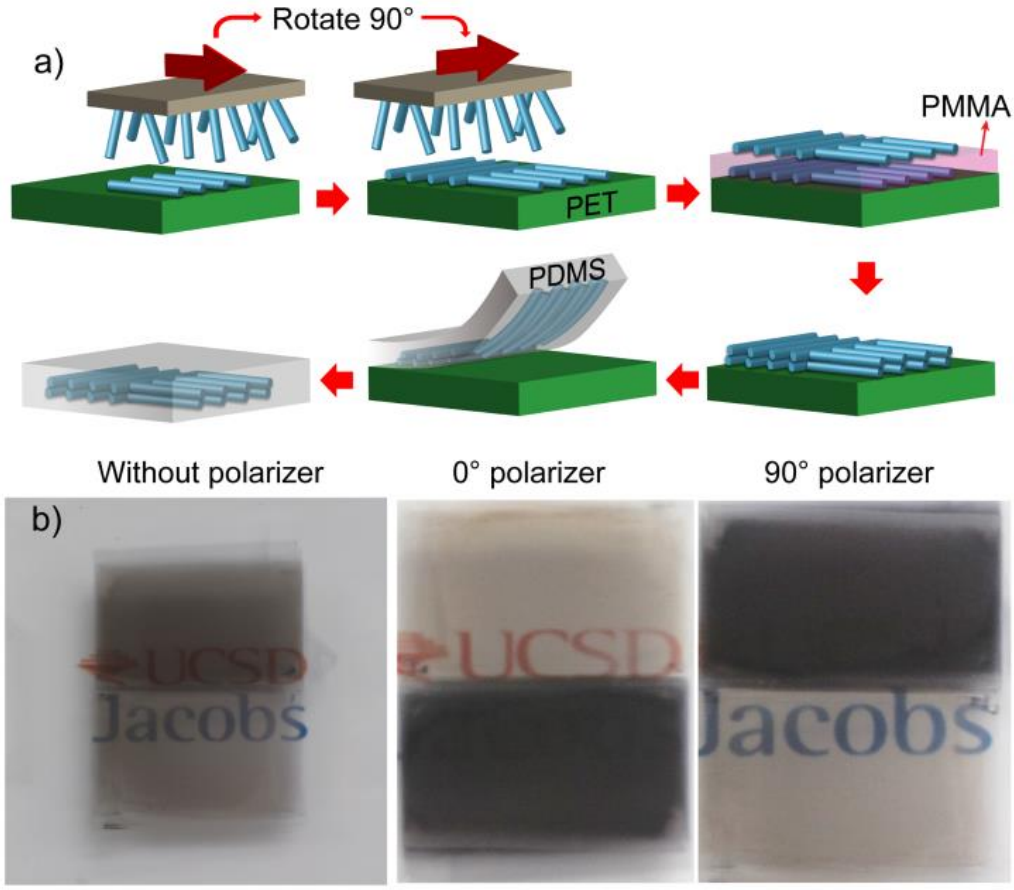

Figure 5.8. Dual phase printing of NW-PDMS WGPs. a) Schematics of fabrication process. Array of NWs are printed on two designated neighboring areas on a PET sheet followed by final transfer to PDMS and peeled off. b) Demonstration of dual phase NW polarizer designed on a PDMS sheet. From left to right photographs show the WGPs under unpolarized, 0°, and 90° phase polarized light.

5.6. Conclusion

In summary, we have successfully demonstrated printable NW WGPs from bottom-up assembly of NW building blocks into sub-visible wavelength periodicity and parallel array integrated with novel functionalities that aim toward human-friendly wearable optoelectronics. Systematic studies were conduct to expose behind physical nature of NW array as macroscale polarizer by addressing the dimensional effect on the polarization properties. Quantitative studies on the effect of size and density of NW arrays on the polarization efficiency provide some of the design rules which are useful in refining the fabrication process. By direct imaging and measurement of each NW WGP, ~1:1 ratio of linear increase in polarization efficiency is revealed. In addition, both experimental and numerical analyses on the size effect of NW arrays show that the shape and position of transmission spectrums can be tuned by controlling the mean diameter and their size distribution. Moving forward, we further present the potential applications as an extension toward smart optical filter by introducing low mechanical modulus and highly bendable/stretchable characteristic by easily switching the underlying substrates. Depending on the variety of material composite and substrate choices, the fabrication concept can further be extended to a wide range of applications, for example, electrically local active or wide-band filters and photodetectors.

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