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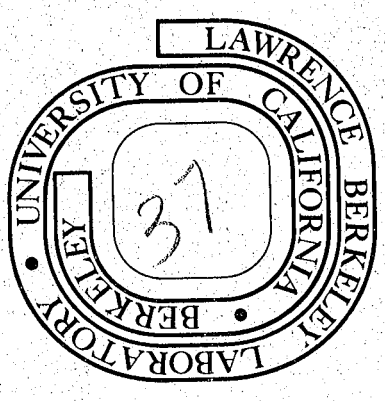
CHARGE-COUPLED DEVICE HIGH-FREQUENCY DRIVERS AND TESTING INSTRUMENTS

Branko Leskovar

January 1978

Prepared for the U. S. Department of Energy
under Contract W-7405-ENG-48



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Charge-Coupled Device High-Frequency Drivers and Testing Instruments

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Charge-Coupled Device Drivers and Testing Instruments

Branko Leskovar
Lawrence Berkeley Laboratory
University of California
Berkeley, California

January 24, 1978

In most applications, charge-coupled devices require a complex array of peripheral circuitry to support their operation; such as: input gates, multiple phase clock signal generators, output gates, propagation gate drivers, reset gates, photogates and various d.c. biasing circuits. For example, for a 128 cell CCD analog shift register, which is used for both delaying and expanding the time base of quantized analog data with a 62.5 Msample/second input rate and a 100K sample/second output rate, the supporting circuitry contains an input sample and hold propagation gate driver, a multiphase phase generator, amplifiers and output strobe circuits, (1)-(5). We will consider in some detail the four-phase generation circuitry and driver requirements for such a device. The four-phase clock signals required can be generated by using a pair of D-type Flip Flops connected as shown in Fig. 1. When a clock signal with a pulse rate four times the shift rate is applied to the generator, the four outputs will produce the signals shown in Fig. 2. Each pulse is shifted 1/4 a cycle in phase. The logic family used for such an operation has to be consistent with frequency of operation. For example, for a shift rate of 62.5 MHz the input clock frequency of 250 MHz is required. The Emitter Coupled Logic (ECL) is the only logic family capable of operating at these frequencies.* With this method of four-phase generation, the clock fre-

* Some new D-Flip-Flop devices eventually can operate at frequencies up to 700 MHz, but with a very distorted waveshape of the output signals.

quency can vary preserving at the same time the quadrature relationship of the generator output signals.

For an operating shift rate of 62.5 MHz, the period of the driver signal waveform is T_o = 16 ns as shown in Fig. 3. The transition times, Δt_r and Δt_f, have a maximum value which equals to $T_o/2$=8 ns. The manufacturer of this particular CCD recommends a minimum transition time of 5 ns, to preserve the device dynamic range and charge transfer efficiency. The minimum risetime value of the driving signal determines the driver current capability necessary for the capacitive load of the gate input.

The current requirements of the driver signal generator can be derived from the device manufacturer's recommended gate voltage and the gate capacitance. For the device under consideration the recommended peak-to-peak voltage, $\Delta V=V_H-V_L$ is in the range of 12 to 15V. Because of the high density gate structure of the device, the driver current capability will be based on the larger voltage value of 15V. For the gate capacitance of 25pF the required driver current is given by:

$$I=C\frac{\Delta V}{\Delta t} = 25.10^{-12}\ \frac{15}{6.10^{-9}} \approx 63\ \text{mA} \qquad (1)$$

where the transition time Δt=6 ns.

With an additional stray capacitance of 10-15pF, the driver current requirement is approximately equal to 100 mA per CCD gate.

The four-phase output signals of the driver should remain in quadrature over the entire frequency range of interest. Typically, for a set of four drivers the stability should be better than $\pm$ 1 ns.

Concerning the driver power capability, the power at 62.5 MHz can be approximately calculated from the equation:

$$P \approx \eta \, I \, V_{ps} \, \delta \qquad (2)$$

where η is driver efficiency, I is the required gate current, V_{ps} is the power supply voltage and δ is the duty cycle. This formula is not valid for frequencies higher than approximately 80 MHz. For η = 80%, I = 100 mA, V_{ps} = 17V and δ = 6/16 = 38% the P/driver output $\approx$ 800 mW. For four drivers the power required is approximately equal 3.2W. Because of capacitive character of the CCD gate, a very small amount of power is dissipated by the gate. Almost all power is dissipated in the four-phase driver circuitry. Fortunately, the overall power is significantly reduced because in the time expansion mode, the drivers operate at the 62.5 MHz rate for less than 10% of the time. However, drivers should be designed to withstand peak power of 3.2W for periods of up to 10 ms.

CCD development programs in the Lawrence Livermore Laboratory (3) have created a need for a versatile four-phase CCD testing instrument being capable of operating at clock frequencies of from 100 MHz to 250 MHz. A testing instrument has been designed to satisfy necessary requirements for testing CCD's intended for use in analog signal recorders for sampling and time expansion of transient signals. The testing instrument has the capability of switching the high clock driver frequency to a lower CCD readout frequency and supplying the required signals at appropriate levels for the input gate, the input diffusion clock, the input diffusion d.c. bias, and the reset gate. The low CCD readout frequency varies from 500 kHz to 10 MHz. All signals necessary to operate CCD have waveshapes with preserved phase

integrity over a wide range of frequencies. Both the high and low read-out frequency clock generators must supply four channel signals which are in quadrature. Furthermore, the switching from high-to-low frequency and from low-to-high frequency has to be reasonably smooth, that is without excessive ringing. This is especially important during the high-to-low clock frequency switch-over period. Hence, electronic switches with very short on and off time must be used to insure fast switching actions and they must be well matched over a wide frequency range to insure smooth transitions.

Concerning the four-phase signal generation, the MECL III logic family was considered initially for a possible application. Unfortunately, at frequencies above 80 MHz, output signals do not have rectangular waveshape. The output signal has a distorted trapezoidal waveshape. The distorted trapezoidal waveshapes approach the waveshape of a distorted sinusoidal as the frequency increases. Therefore, a completely new approach for the generation of four-phase signals over a wide range of frequency had to be taken and evaluated using microwave technology components. Hybrid junctions and quatrature hybrids were specifically evaluated for this particular application.

A hybrid junction is a four-part network capable of splitting input signals into equal amplitude, isolated outputs which are either in phase or 180° out of phase. The network is recognized in the microwave technology under various names; such as, magic tee, ring hybrids and hybrid tees. Their low-frequency counterpart is the hybrid transformer. When a signal is applied to the H, or symmetrical port, it will split equally and in-phase between the collinear output ports (1 and 2), Fig. 4. When a signal is

applied to the E, or antisymmetric port, it will split equally and out-of-phase between the Ports 1 and 2. This in-phase and out-of-phase output relationship results in isolation between the E and H ports, the extent of which is an important measure of hybrid balance. The simultaneous application of signals to both H and E ports results in their vector addition at one collinear port and vector subtraction at the other. Typically, a 50-ohm hybrid junction designed for frequency range from 5 MHz to 1000 MHz has an insertion loss of approximately 4 dB, an isolation of 25 dB, a maximum value of the phase balance of 3 degrees, and the amplitude balance of 0.5 dB.

A quadrature hybrid is a four-port 3 dB coupler capable of splitting an input signal into isolated quadrature phased outputs. This type of device is commonly known in microwave technology field as a 3 dB stripline coupler or a "short slot" waveguide coupler. The device can also be made from lumped components permitting applications at low frequencies. If a signal is applied to Port 1, as shown in Fig. 5, it splits equally between output Ports 2 and 3 with a 90° phase difference. If Ports 2 and 3 are properly terminated, the signal applied to Port 1 is absorbed in the loads. Therefore, Port 4 can be isolated and receive very little power from the incident signal. The extent of this isolation is an important measure of the coupler performance. Typically, a 50-ohm quadrature hybrid, designed for frequency range from 50 MHz to 500 MHz, has an insertion loss of 1 dB, isolation of 20 dB, an amplitude balance of 0.5 dB, and a maximum deviation from quadrature of 3 degrees. Generally, for low level signal application the device can handle input power levels of 1W. The hybrid junction and

quadrature hybrid specifications given above are typical of the available devices manufactured in this country as well as in Europe.

The four-phase clock signal generator was developed combining a number of hybrid junctions and quadrature hybrids. Because of the frequency bandwidth limitations of these devices, the four-phase generator was designed with two channels in an appropriate configuration. The channel for very high frequency signal generation uses components capable of operating in the frequency range of 50 MHz to 500 MHz. The channel for low CCD readout frequency generation uses components with operating characteristics from 2 MHz to 32 MHz. A block diagram of the high frequency channel is shown in Fig. 6. A combination of five hybrid junctions, used as broadband out-of-phase and in-phase power dividers, and two broadband 90° quadrature hybrids generates pairs of four-phase clock signals in the 50-500 MHz frequency range. A similar configuration, shown in Fig. 7, generates pairs of the four-phase clock signals in the 2-32 MHz range. Finally, combining the outputs from the high-frequency and the low-frequency channels by means of eight in-phase linear power combiners, as shown in Fig. 8, four-phase clock signals are obtained in pairs over a frequency range from 2 to 500 MHz. As a self-contained unit the four-phase generator is capable of operating at frequencies up to 1000 MHz. The front and top view of the four-phase generator are shown in Figs. 9 and 10, respectively.

Description of the Wide-Band Charge-Coupled Device Measuring System

Block diagram of the wide-band charge-coupled device measuring system is shown in Fig. 11. The system requires for its operation an external

high frequency clock signal generator capable of operating in a frequency region from 100 to 250 MHz and delivering an output signal of at least $1V_{rms}$ into 50 ohm load. The first stage of the sytem is a high-to-low frequency processor capable of operating at frequencies up to 300 MHz. A thumb-wheel switch selects the high-to-low frequency division ratio in the increments of 20, 40, 60, 100....up to 500. Therefore, with a 200 MHz clock signal and a division ratio of 100 the low readout frequency clock signal is 2.0 MHz. The output from the frequency processor unit consists of a high frequency clock signal, which is at the same frequency as the input signal and a low readout CCD frequency clock signal which frequency is determined by division ratio selected by the switch. Both the high frequency and low frequency signals are gated on and off by a dual radio-frequency high speed switch. The gating conditions depend entirely on the external logic signal which in turn is governed by the requirements of the CCDs under test. Only one channel is on at any given time. The output signals from the switch are amplified by wide-band amplifiers, with adjustable wide-band frequency gain controls, to approximately 1W output power level. After amplifications, the high and low frequency clock signals are processed by the four-phase signal generator which provides a pair of four high and low frequency output signals which are 90 degrees out of phase with respect to each other.

One set of four-phase high and low frequency clock signals is further amplified by four seperate wide-band RF power amplifiers having output power capabilies of 3W each. Each amplifier channel has at its input a 1 dB step and a 0.1 dB step wide-band low-phase error attenuator. These attenuators have phase errors of less than $\pm$ 3 degrees in the frequency band

1-250 MHz. The amplifiers used were phase matched so that the phase difference between any of the four amplifiers is less than ± 5 degrees in the 1-250 MHz frequency band. The nominal gain of each amplifier was 37 dB with a gain flatness of ± 1 dB over the same frequency range.

The second set of four-phase high and low frequency clock signals is applied to a four channel radio frequency to ECL level translator. The translator module supplies ECL level signals to other logic devices required for the CCD operation.

The output signals from the four-channel wide-band amplifier are applied to the test fixture where the CCD will be tested. The final driving signals are provided to the CCD thru four low-Q factor wide-band transformer circuits. A schematic diagram of the transformer driving stage is shown in Fig. 12. The primary-to-secondary turn ratio of each transformer is 4.1. The nomimal 50 ohm output impedance of the output amplifier is transformed to approximately 3 ohm for the source impedance. With this impedance the charging and discharging time constant is 120 ps for a 40 pF capacitive load. Transformers are designed in such a way that their stray and leakage inductances do not resonate with the load capacitance at any frequency within the frequency range of interest. The transformer core material was selected to be lossy at high frequencies to make the Q-factor of the circuit low. At very high frequencies additional loss is introduced by the eddy current loss of the enclosure walls. A small high-Q capacitor is connected in parallel across the primary of each transformer for final phase adjustment and tracking between channels. Each driving stage is enclosed in a separate chamber. Chambers are provided with ventilation holes. The CCD under test

is mounted on a small printed circuit board which is situated between the two main transformer circuit enclosures, as shown in Fig. 13.

The complete measuring system with the test fixture is shown in Fig. 14. The test fixture is in the right hand lower corner of the photograph. The phase difference between the four low frequency channels (90 degrees out of phase with respect to each other) as a function of frequency is shown in Fig. 15. The measurement was made with a 10V peak-to-peak signal across a 35 pF load. The phase difference was measured directly at the capacitive load with the 0 degree channel as a reference channel. The phase difference of the low frequency channels is within $\pm$ 5 degrees through the 1-10 MHz frequency band. The phase difference between the four high frequency channels as a function of frequency is shown in Fig. 16. The phase difference of high frequency channels is within $\pm$ 10 degrees through the 100-250 MHz frequency band. The available output voltage across capacitive load, in V peak-to-peak, as a function for frequency for high frequency channels is shown in Fig. 17. With a 100 pF load a voltage of 10V peak-to-peak can be obtained up to 170 MHz. For a 25 pF load, an available voltage of 10V peak-to-peak can be obtained up to 280 MHz. The upper frequency limits are determined by the power available from each driver for the various capacitive loads. A very important characteristic of the tester is its performance when switching from high-to-low frequency and from low-to-high frequency. The waveform of the high-to-low frequency switching is shown in Fig. 18.

The wide-band measuring system was designed to meet flexible requirements of the CCD testing. The system can be easily modified by increasing the power of the final amplifiers and changing the output transformer

stages to accommodate larger capacitive loads. Furthermore, the size and cost of the system can be significantly reduced using high Q-factor output circuitry once the optimum operating parameters of the CCDs have been chosen.

Acknowledgment

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Figure Captions

Fig. 1 Four-phase generator logic diagram.

Fig. 2 Four-phase generator output timing diagram.

Fig. 3 Typical drive signal waveform of a charge-coupled device.

Fig. 4 Functional schematic of a hybrid junction and its low-frequency equivalent.

Fig. 5 Functional schematic of a quadrature hybrid.

Fig. 6 Block diagram of the high-frequency channel of the four-phase clock signal generator.

Fig. 7 Block diagram of the low-frequency channel of the four-phase clock signal generator.

Fig. 8 Block diagram of the four-phase clock signal generator.

Fig. 9 Front view of the four-phase clock signal generator.

Fig. 10 Top view of the four-phase clock signal generator.

Fig. 11 Block diagram of the wide-band charge-coupled device measuring system.

Fig. 12 Schematic diagram of the transformer driving stage.

Fig. 13 Top view of the testing fixture.

Fig. 14 The wide-band charge-coupled device measuring system with the test fixture in the right hand lower corner.

Fig. 15 The phase difference between the four low-frequency channels.

Fig. 16 The phase difference between the four high-frequency channels.

Fig. 17 Available output voltage as a function of frequency for the high-frequency channels.

Fig. 18 The waveform of the high-to-low frequency clock switching.

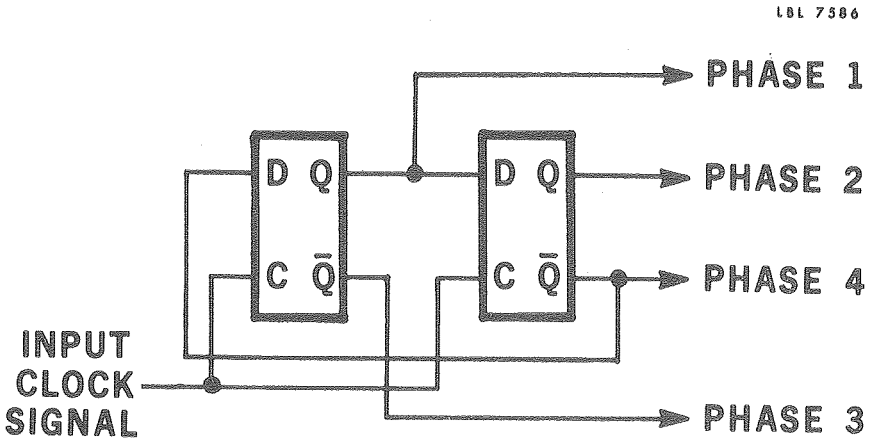
LBL 7586
PHASE 1
PHASE 2
PHASE 4
PHASE 3
D Q
C Q̄
D Q
C Q̄
INPUT
CLOCK
SIGNAL
XBL 789-11451

Fig. 1

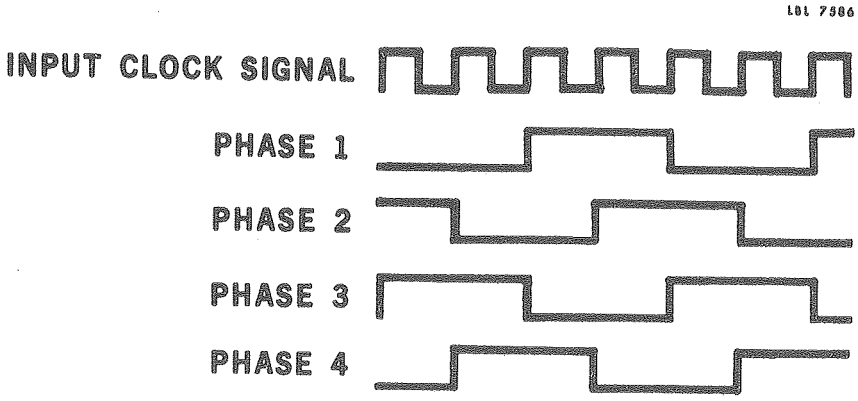
LBL 7586
INPUT CLOCK SIGNAL
PHASE 1
PHASE 2
PHASE 3
PHASE 4
XBL 789-11452

Fig. 2

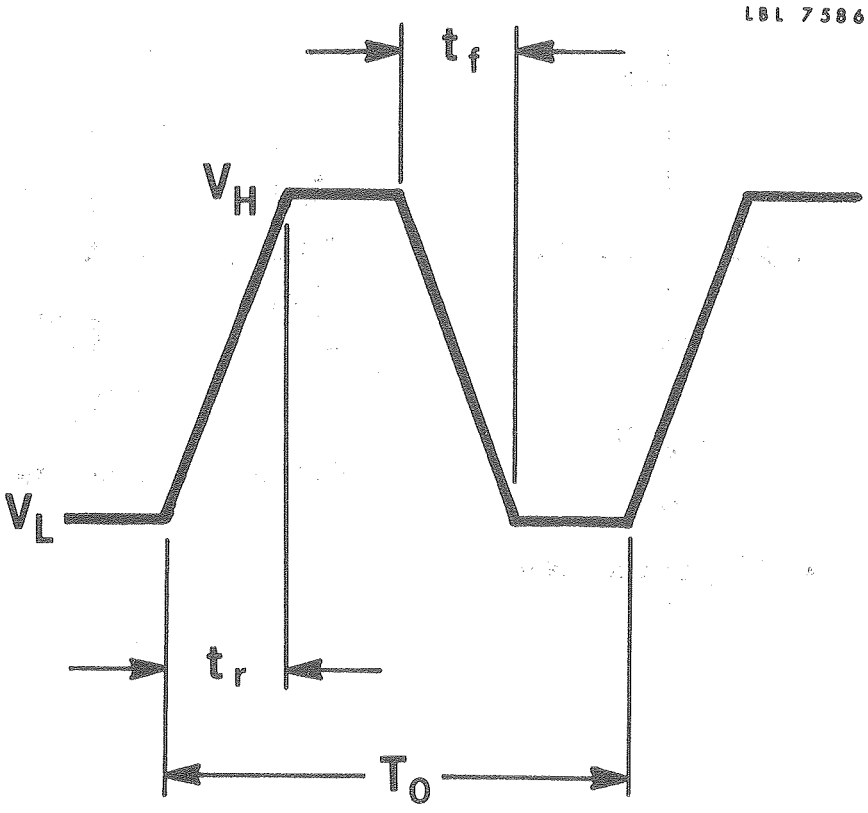

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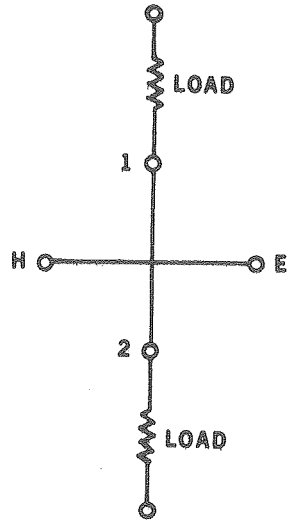
Fig. 3



MICROWAVE FUNCTIONAL SCHEMATIC

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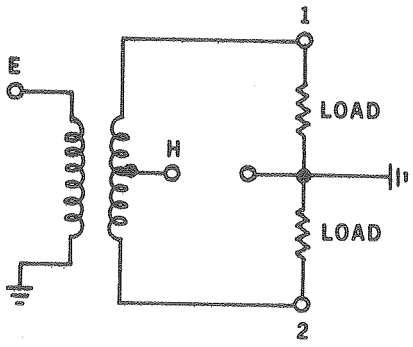
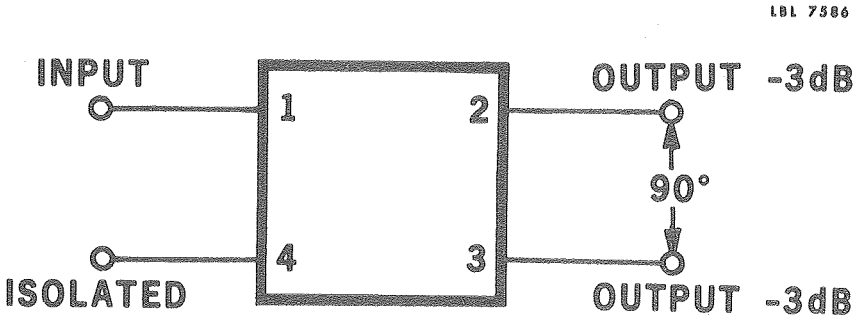


LOW FREQUENCY EQUIVALENT

XBL 789-11454

Fig. 4



XBL 789-11455

Fig. 5

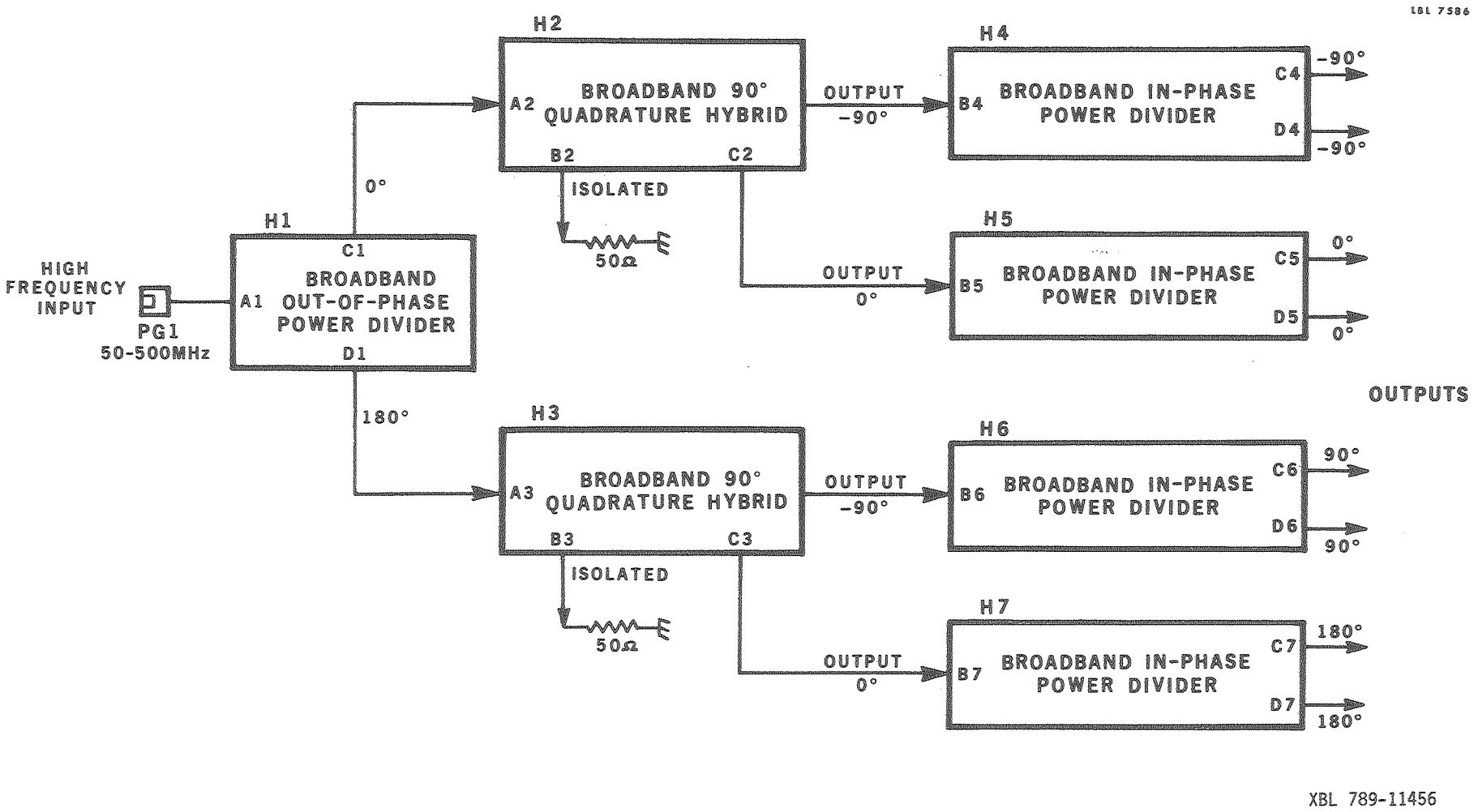


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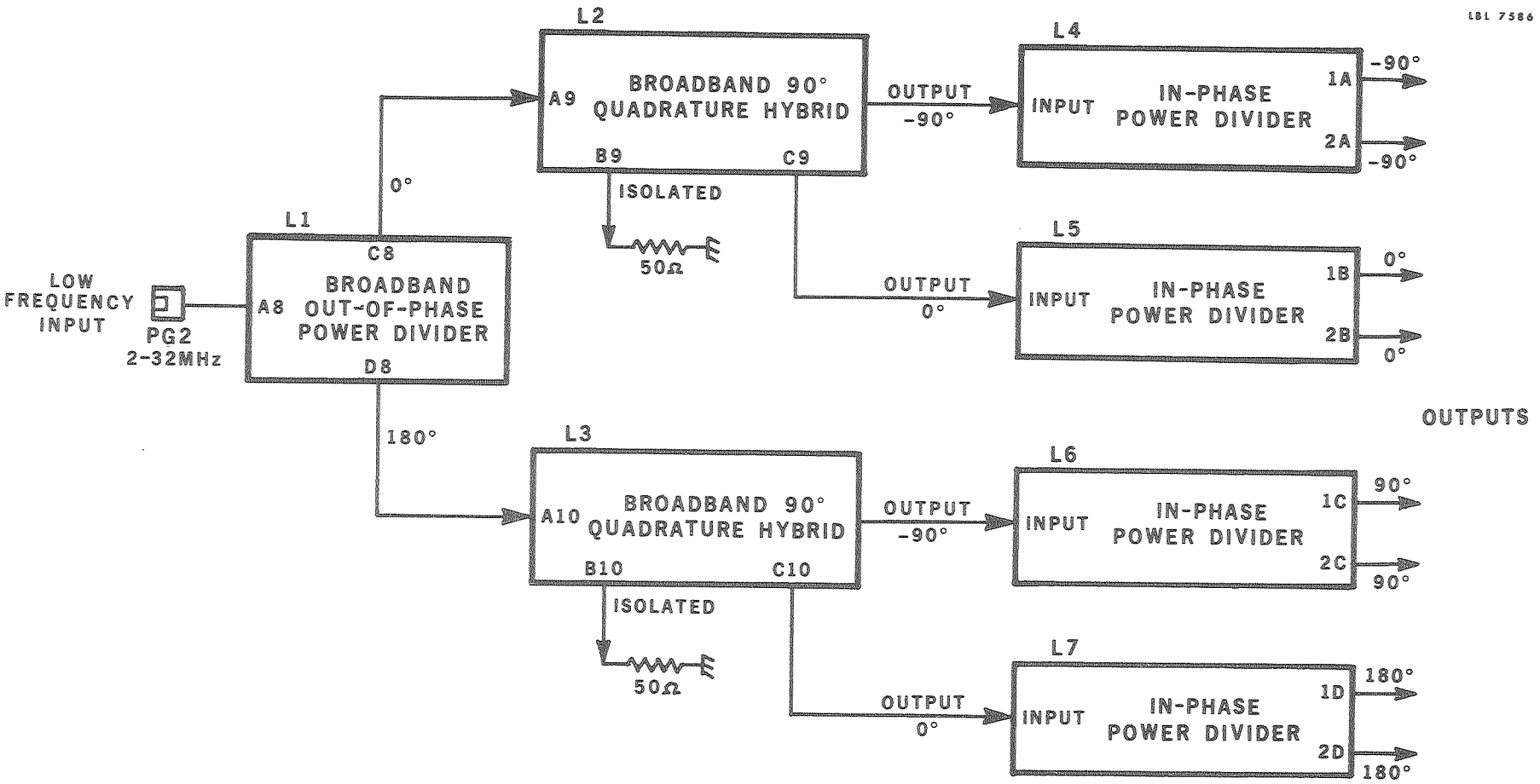
Fig. 6



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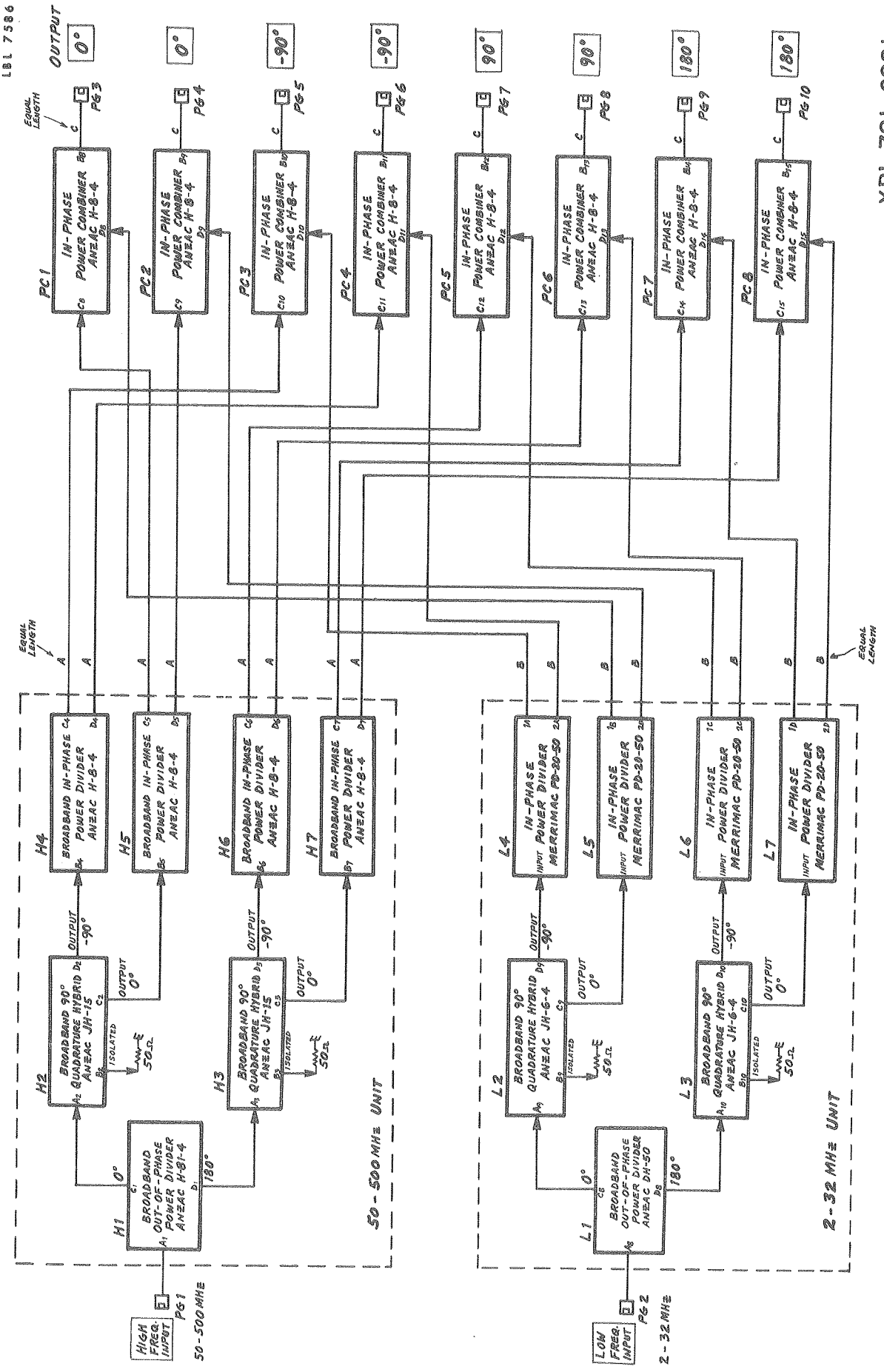

XBL 781-6921

Fig. 8

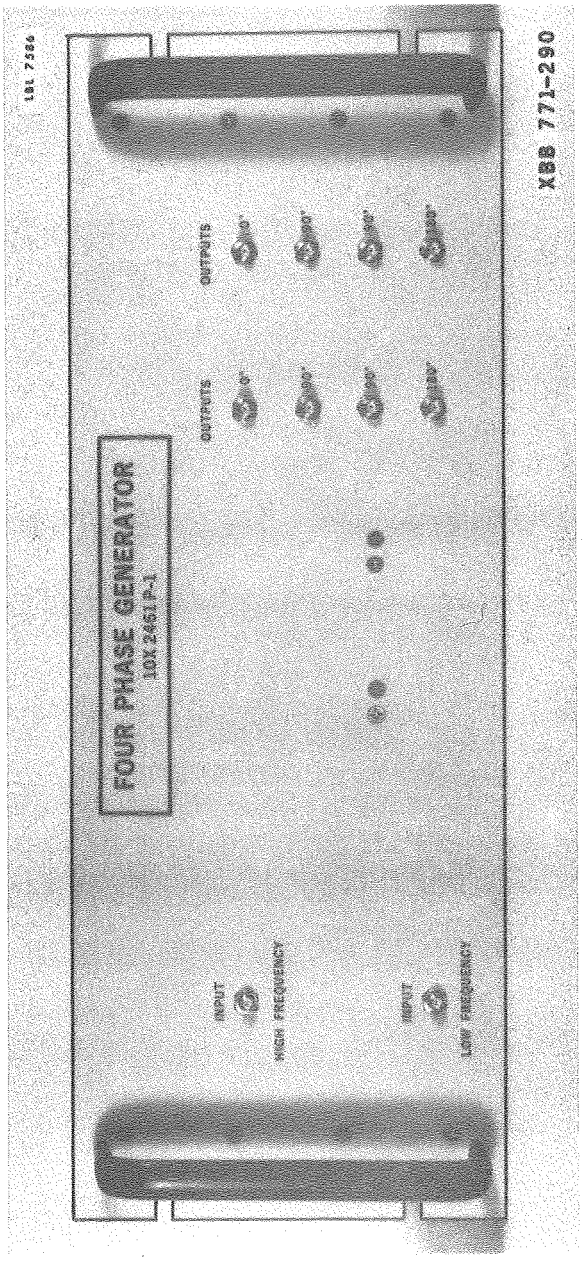
LBL 7586
FOUR PHASE GENERATOR
10X 2461 P-1
INPUT
HIGH FREQUENCY
INPUT
LOW FREQUENCY
OUTPUTS
OUTPUTS
XBB 771-290

Fig. 9

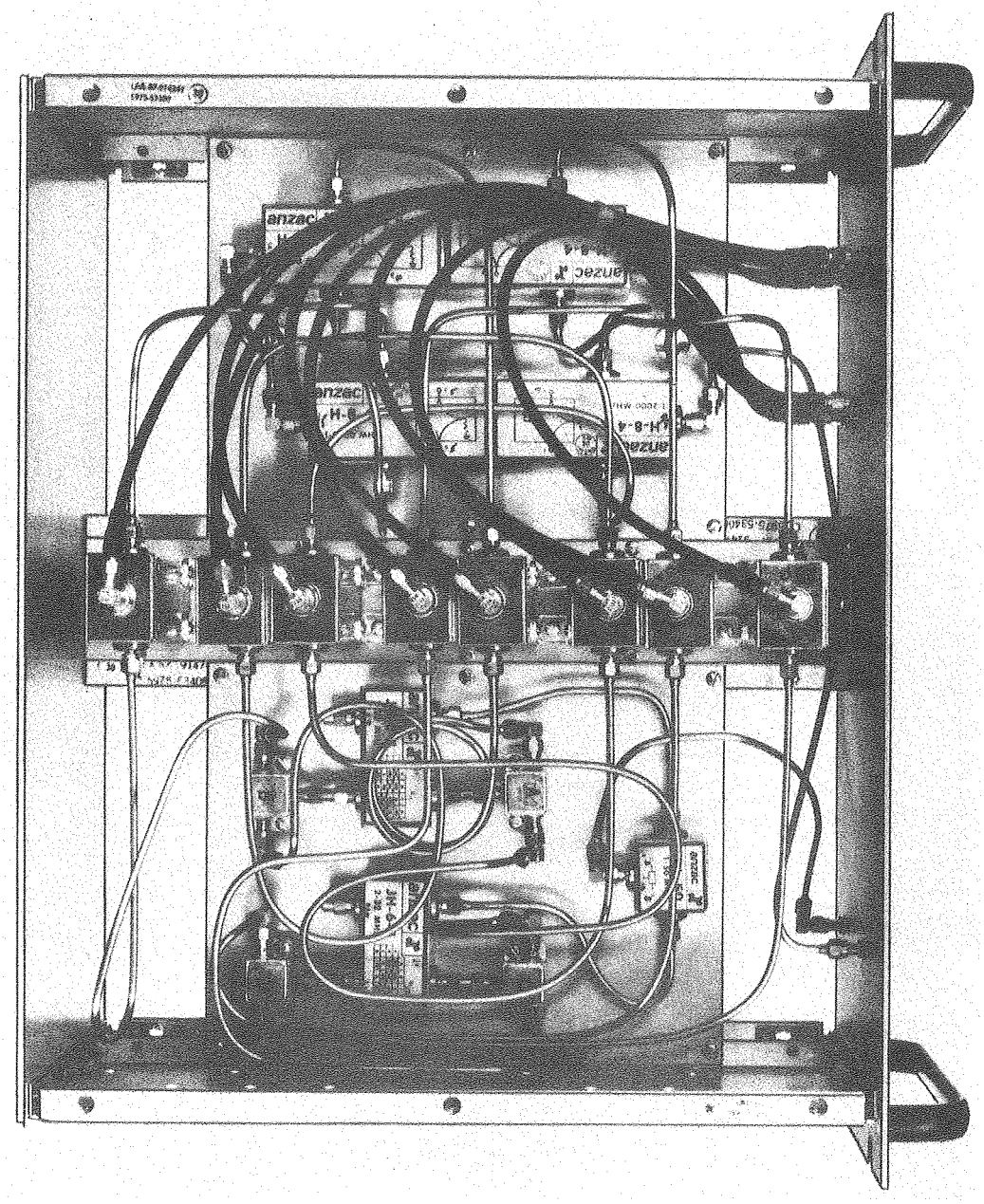

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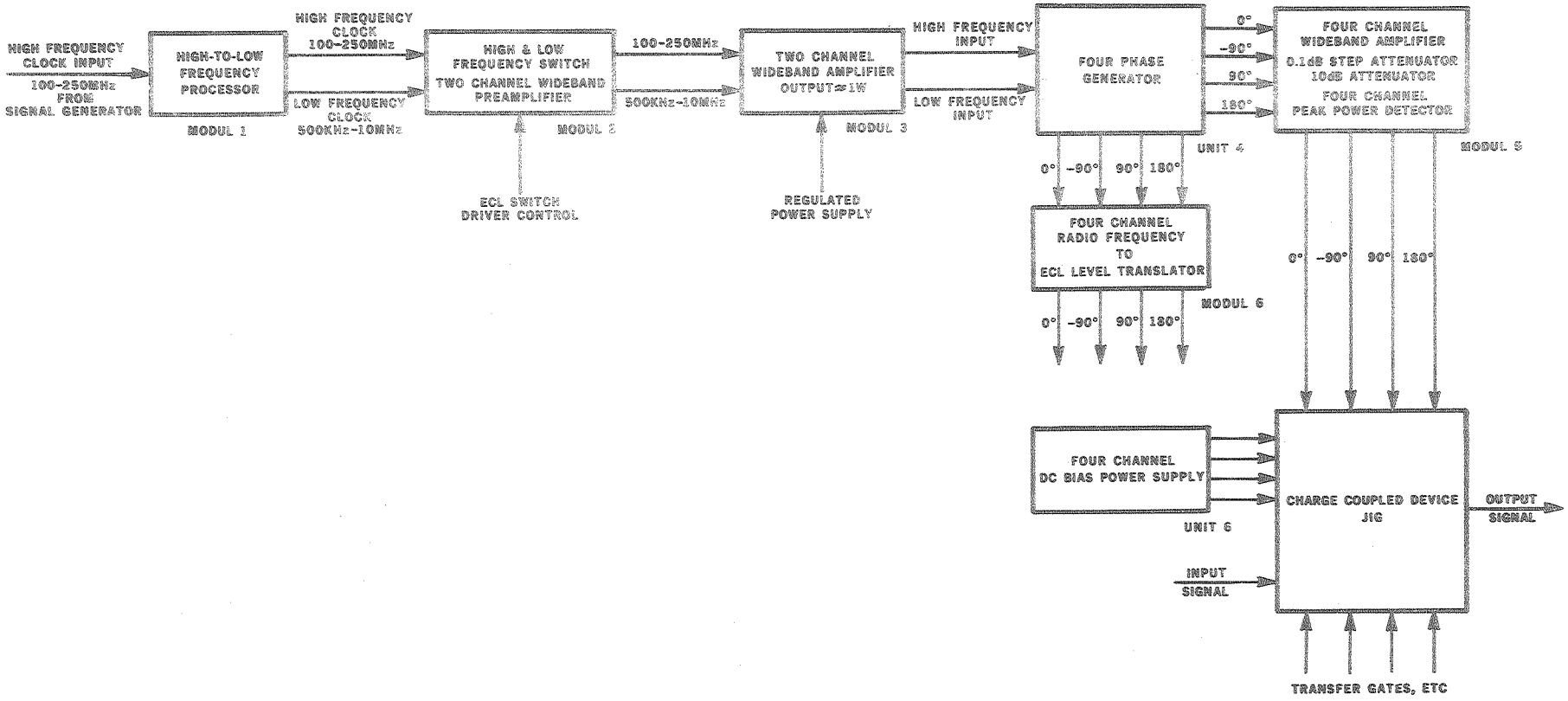
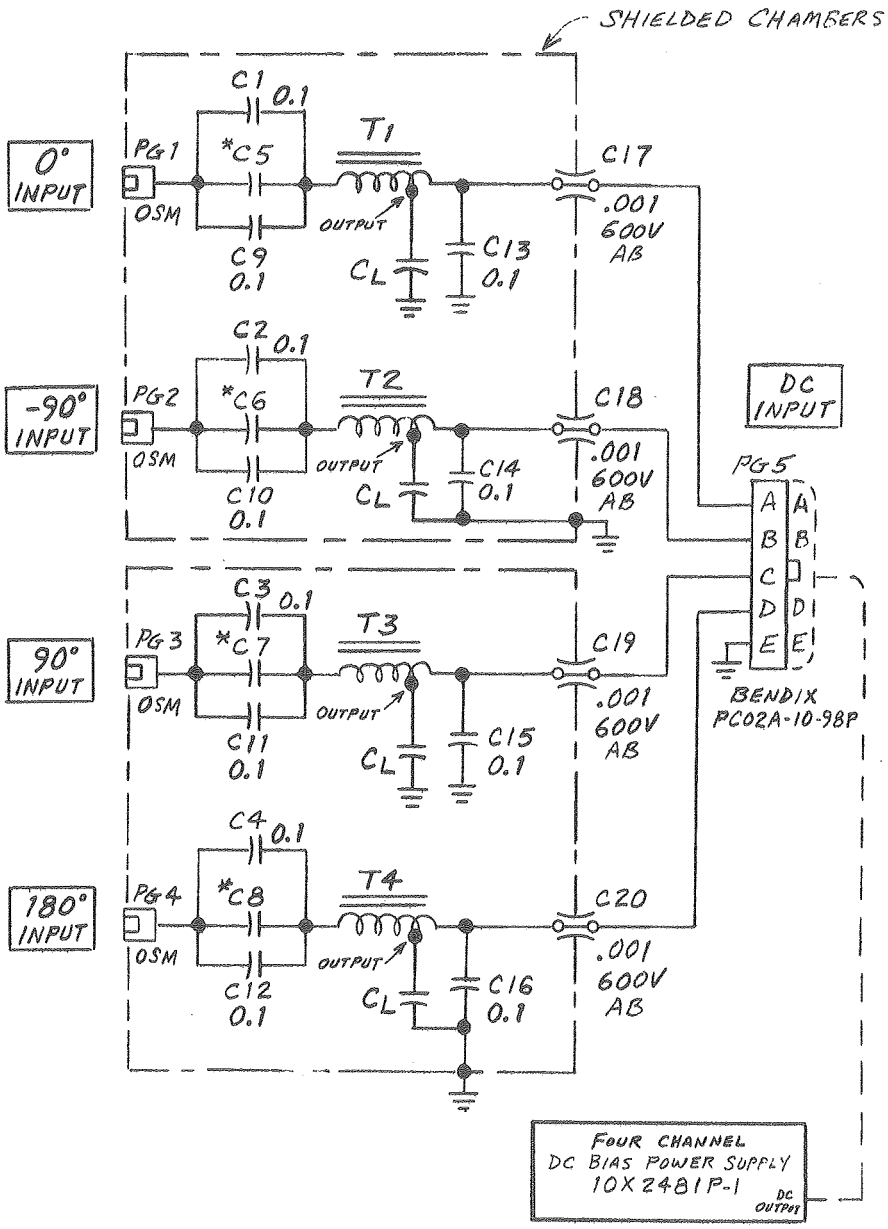
Fig. 10



XBL 785-8391

Fig. 11



NOTE:

1. CAPACITORS 0.1μF 50V CK05 CERAMIC.
*2. C5-C8 ARE 470pF CHIP CAPACITORS.
3. CAPACITIVE LOAD C_L = 50pF-100pF (CCD LOAD).
4. TRANSFORMER T1-T4 = 1 INDIANA GEN. H CF111 AND 1 INDIANA GEN. Q2 CF111 STACKED TOGETHER (EXPOXY) 3 TURNS COPPER STRIP WINDING TAPPED OFF AT 1 TURN.

XBL 781-6917

Fig. 12

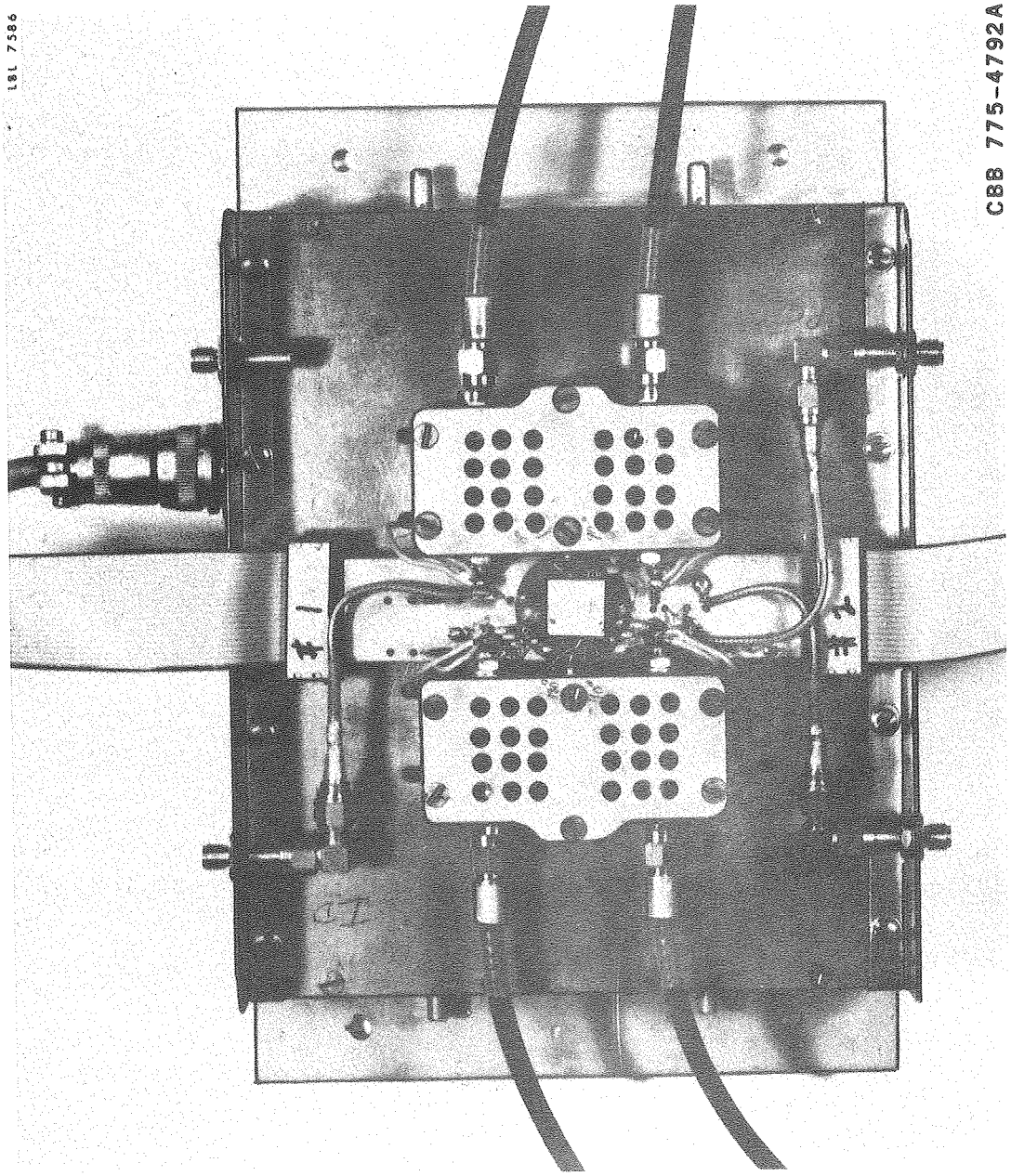


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Fig. 13

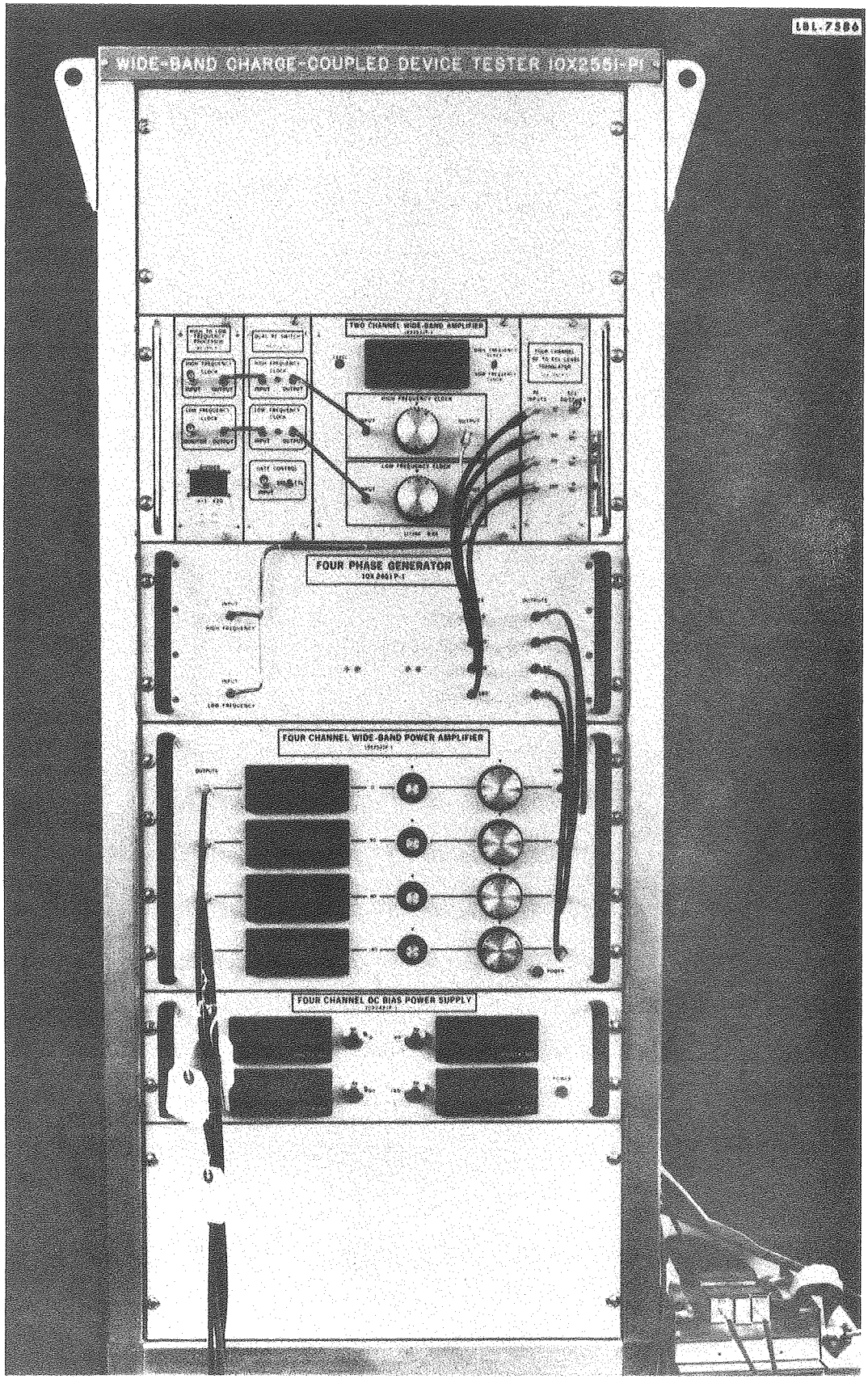

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Fig. 14

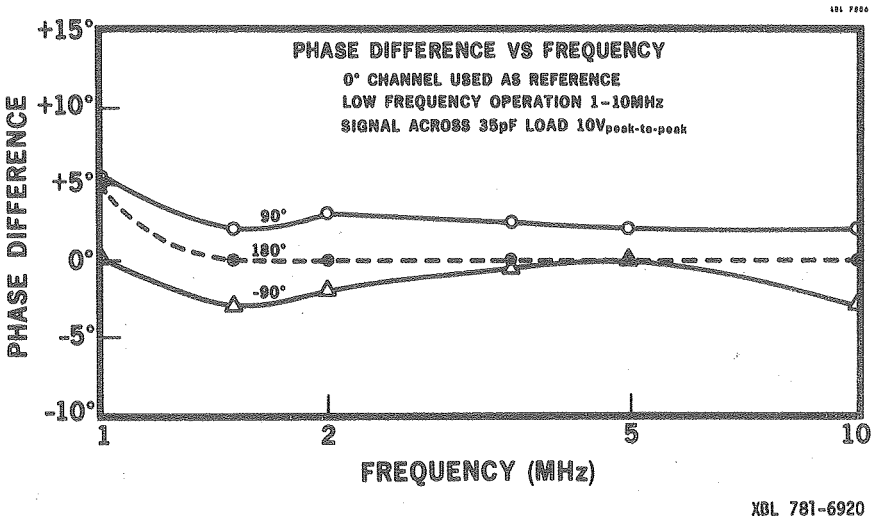

PHASE DIFFERENCE VS FREQUENCY
0° CHANNEL USED AS REFERENCE
LOW FREQUENCY OPERATION 1-10MHz
SIGNAL ACROSS 35pF LOAD 10Vpeak-to-peak
PHASE DIFFERENCE
+15°
+10°
+5°
0°
-5°
-10°
90°
180°
-90°
1
2
5
10
FREQUENCY (MHz)
XBL 781-6920

Fig. 15

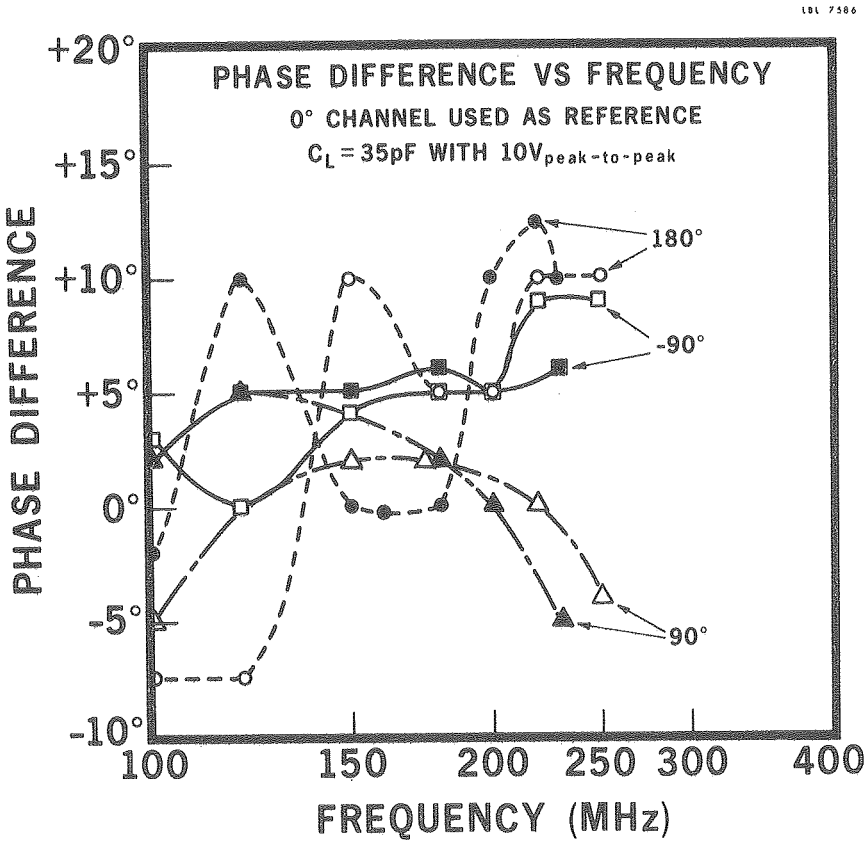

LBL 7586
PHASE DIFFERENCE VS FREQUENCY
0° CHANNEL USED AS REFERENCE
C_L = 35pF WITH 10V peak-to-peak
PHASE DIFFERENCE
+20°
+15°
+10°
+5°
0°
-5°
-10°
180°
-90°
90°
100
150
200
250
300
400
FREQUENCY (MHz)
XBL 781-6918

Fig. 16

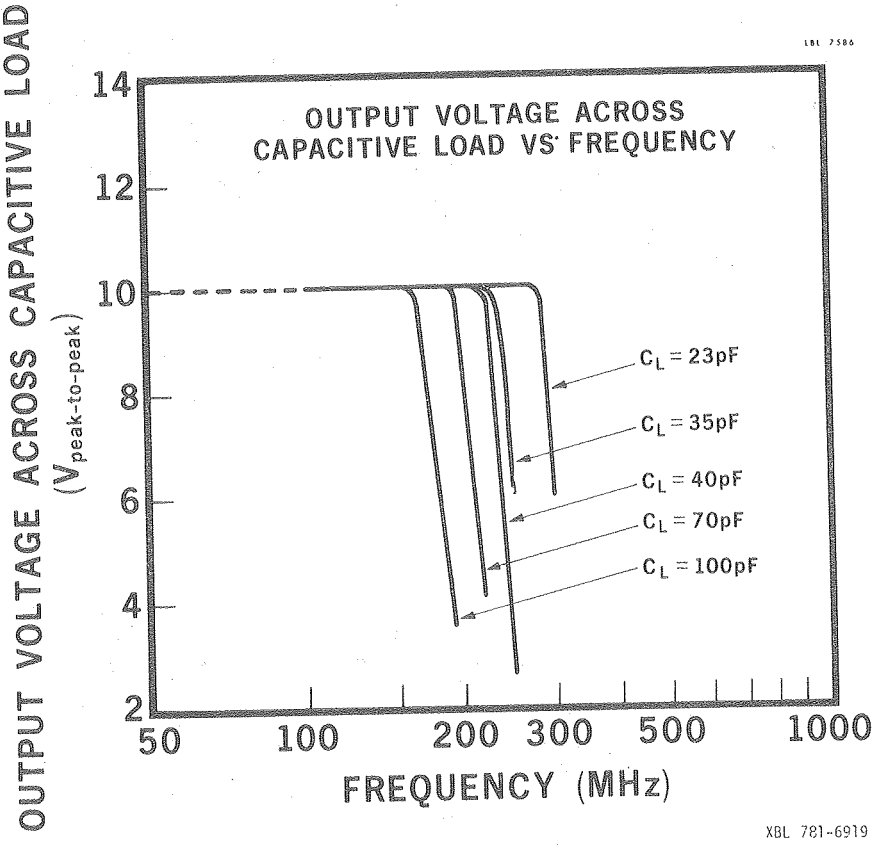
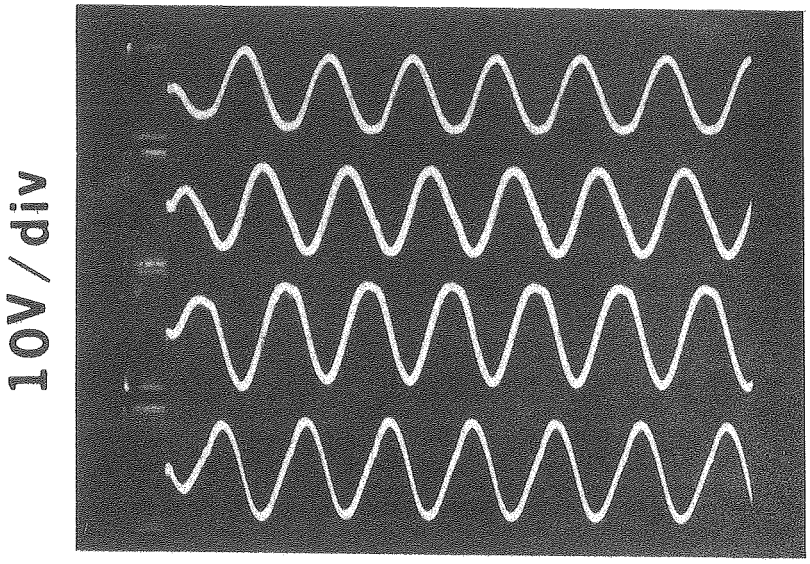

LBL 7586
OUTPUT VOLTAGE ACROSS CAPACITIVE LOAD VS FREQUENCY
OUTPUT VOLTAGE ACROSS CAPACITIVE LOAD
($V_{peak-to-peak}$)
14
12
10
8
6
4
2
50
100
200
300
500
1000
FREQUENCY (MHz)
C_L = 23pF
C_L = 35pF
C_L = 40pF
C_L = 70pF
C_L = 100pF
XBL 781-6919

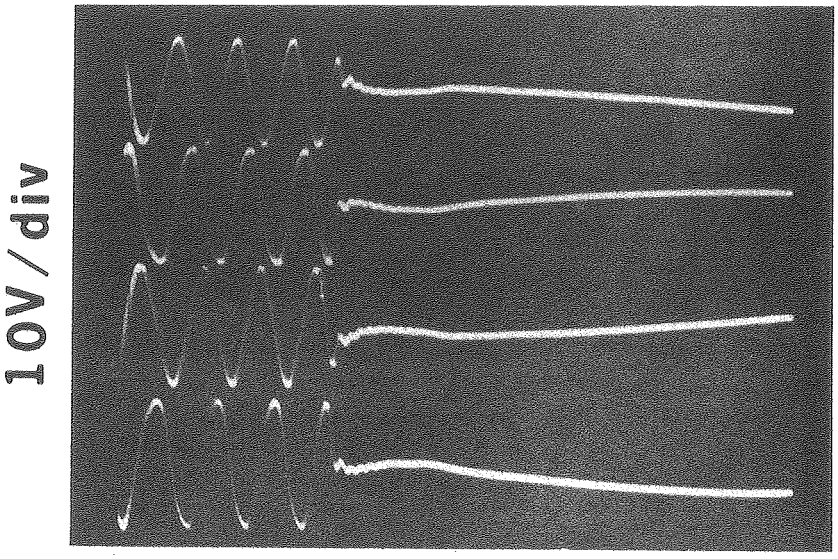
Fig. 17

LBL-7586



XBB 785-5157

LBL-7586



XBB 785-5157A

Fig. 18