A Resonant Gate Driver with Variable Gain and a Capacitively Decoupled High-Side GaN-FET

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***Abstract*— Here we describe a gate-driver with resonant action that minimizes gating loss at high switching frequencies (10-20 MHz) while facilitating variable voltage gain that can exceed the supply rails. The gate voltage swing can be controlled with minimal duty cycle constraints, making this driver capable of meeting the diverse drive requirements of different switch technologies and converter topologies. A prototype uses two small N-channel gallium nitride (GaN) transistors within the drive structure, significantly decreasing parasitics. To do so, a capacitive decoupling technique is used to allow the high-side N-channel device's 'flying' driver to receive power; a distinct challenge for flying drivers commuting between two variable voltages. The prototype was applied to several high frequency switching devices. Up to a 72% reduction in gating-loss is observed as compared to a conventional hard-charged gate-driver while maintaining rise and fall times <18 ns for the devices tested.**

I. Introduction

In the ongoing effort to improve power density, power converter designers have been pursuing higher and higher switching frequencies, allowing passive components to shrink. However, increased switching frequency results in increased switching loss and reduced volume requires improved efficiency as the heat generated per unit volume also increases. Several resonant and soft-charged topological methods have been proposed (e.g., [1-4]) that are designed to approach adiabatic (or "loss-less") energy transfer by recognizing high-efficiency soft-switching conditions, i.e. zero-current-switching (ZCS) and zero-voltage-switching (ZVS). These techniques can significantly improve efficiency, but typically do not address dynamic CV^2f gating-loss, which continues to rise with increased frequency.

To address switch-related losses, several gate driver designs have been discussed in the literature. For hard-switching applications, fast rise/fall times are critical and reverse conduction losses must often be addressed. In this vein, [5] proposed a three-level hard-charged gate driver where V_{GS} can be held high, low (0V), or at an intermediary voltage V_X which is just below the switching device's turn-on threshold. The latter state greatly reduced reverse conduction losses and eliminated the need for a parallel diode. To avoid a switch turning back on immediately after turn-off, a well-studied result of Miller feed-through and a large dv/dt on V_{DS}, [6] discussed a two-level driver with a negative low-level gate drive voltage. In this case, a Zener regulator was used to produce the required negative driver offset. This approach eliminated Miller turn-on losses, but introduced additional biasing losses as a result of the Zener reference. Furthering this work, both [7] and [8] presented three-level gate drivers with a negative low-level, allowing both Miller turn-on and reverse conduction losses to be minimized. Of these approaches, all but [8] are entirely hard-charged, dissipating considerable power in the form of CV^2f loss. In addition, the need for isolated power delivery complicates effective implementation.

For converters operating under soft-switching conditions, such as those mentioned earlier, rise/fall times can be relaxed considerably with reduced impact on overall converter efficiency. Additionally, reverse conduction losses may also be reduced if the converter is designed without intentional free-wheeling time-intervals. These points serve to increase the viability of two-level resonant or adiabatic gate-driver topologies which aim to reduce their intrinsic CV^2f hard-charged gating loss at the expense of increased switching time. Many techniques have been proposed to mitigate gating-loss, largely using the aforementioned adiabatic methods, but applied within the gate-driver itself. Operating from 10 kHz to 1.5 MHz, [9-11] effectively use an inductor, diodes and multiple synchronously-controlled active devices, but require precise timing constraints for good performance, ultimately limiting the frequency of operation. [12] and [13] employ tuned resonant methods with minimal active circuitry and can reach much higher frequencies efficiently (30-100 MHz) but require accurate tuning and have fixed duty cycle and frequency requirements, limiting their use to specific resonant converter topologies and modes of operation.

This work significantly extends an intermediary solution ([14]) by employing low-voltage level-shifted gate-drivers, GaN-FETs, and a capacitive decoupling technique to provide power to a 'flying' high-side driver. The result is a resonant gate-driver with an all N-channel output stage, controllable output swing, reduced parasitic losses, minimal active timing constraints, full flexibility of duty cycle and switching frequency, and no isolated power delivery requirements. These attributes make it broadly applicable to various power-FET technologies and diverse resonant and soft-charged topologies with complex clocking requirements (e.g., [3,4]).

Section II discusses the evolution towards the proposed topology, Section III describes the proposed capacitive decoupling technique which provides power to a high-side flying driver, and Section IV demonstrates a discrete driver prototype which achieves up to a 71.7% reduction in gating loss while operating over 20 MHz.

II. Topology Selection

Figure 1 depicts the evolutionary steps taken towards the proposed gate driver solution. Fig.1(a) depicts a conventional hard-charging gate driver: Switches S_1 and S_2 operate complementary to each other and drive the input capacitance, C_{ISS}, of the primary power-FET or device-under-test (DUT), high or low. Here we observe unmitigated $C_{ISS}V_{DD}{}^2 f$ gating-loss.

Fig.1(b) introduces an inductor which forms an LC resonant tank with C_{ISS} and performs efficient energy transfer into and out of C_{ISS}. Once the gate has fully transitioned from high to low, or vice versa, the active switch must be turned off immediately for C_{ISS} to retain its new voltage level. Due to the resonant action, the gate drive voltage experiences gain and can extend well beyond the 0V and V_{DD} rails. Any stray gate inductance is absorbed into the driver's deliberate inductance making this approach well suited to scaling to higher frequencies, as noted in [1].

Adding diodes, as in Fig.1(c) and proposed in [14], removes the turn-off timing constraint in Fig.1(b), automatically latching the gate voltage at its peak values. The diodes also allow the gate voltage to rest at voltages greater than V_{DD} and less than 0V without turning on intrinsic body diodes in S_1 and S_2. Here the gate voltage will oscillate about $V_{DD}/2$ with an amplitude dictated by the Q-factor, as determined by parasitic loss elements in the circuit. There is no control over gate voltage swing.

In Fig.1(d) V_{DD} is split into two unique source and sink voltages allowing for independent tuning of both maximum and minimum gate voltages. Energy flows out of V_{POS} during an upward swing and is recovered by V_{NEG} on a downward swing.

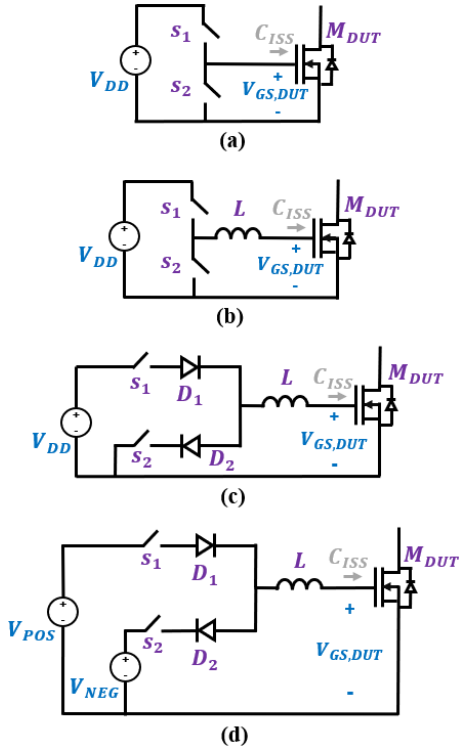

Fig. 1. Evolution towards proposed design.

A complete solution might feature a small DC-DC converter that returns energy captured at V_{NEG} back up to V_{POS} and which may also be used to adjust the gate swing by regulating V_{NEG}. Figure 2 depicts example waveforms of the proposed driver from Fig.1(d). Since the gate is high-impedance when held at its maximum or minimum, a negative gate bias may be desired in practice to compensate for Miller induced turn-on due to an increasing $V_{DS,DUT}$. In addition, clamping switches such as those used in [11] may be used, however these elements would increase the parasitic load to the driver, decreasing efficiency.

III. Practical Considerations for a High-Side N-FET

In the past, designers have been reluctant to use high-side "flying" N-channel devices due to difficulties in level-shifting and providing power, despite their significantly reduced size for the same conductivity relative to P-channel devices in CMOS processes. Fortunately, this has been largely solved through the simple use of a bootstrap diode and integrated level-shifting gate driver solutions (e.g., LMG1210) as shown in Fig. 3. Here, while switch M_2 is ON, the source of M_1, the negative supply of U_1, and the bottom-plate of C_{BP1} are shorted to ground and diode D_{BT} is used to charge C_{BP1} to near V_{DD}. Once charged, C_{BP1} can

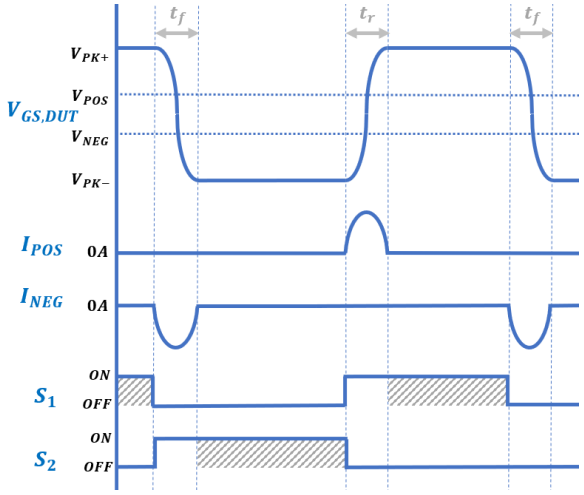

Fig. 2. Waveforms exemplifying the operation of the proposed driver shown in Fig.1(d). Diodes catch the gate voltage at its peak values and relax the turn-off times of S_1 and S_2 (turn-off window indicated in grey).

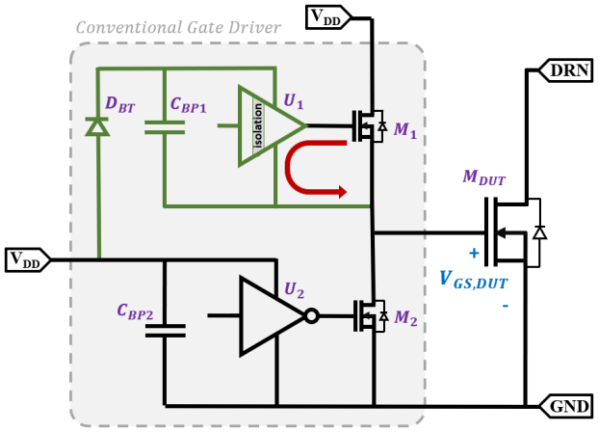

Fig. 3. Conventional half-bridge bootstrapping technique. Power is delivered to C_{BP1} and the high-side driver U_1 via bootstrap diode D_{BT} while switch M_2 is ON. The V_{GS} discharge path of M_1 is highlighted in red.

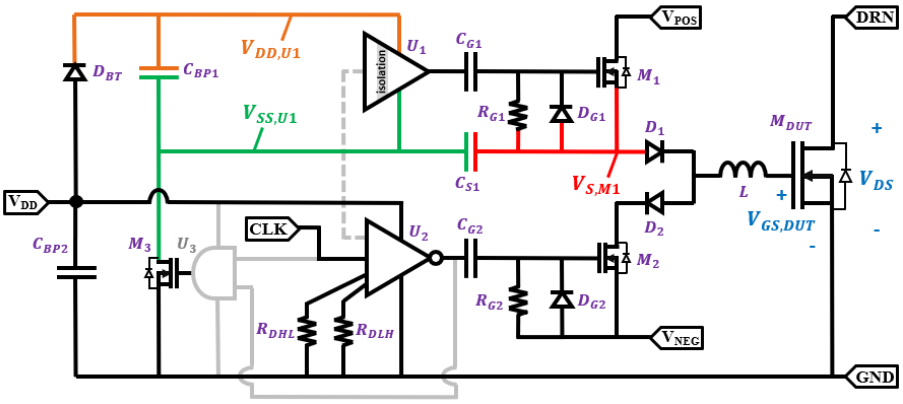

Fig. 4. Schematic of the constructed prototype. Color-coding of select nets correlates with high-lighted nets in Fig. 5.

continue to provide power to U_1 as M_1 is activated, forcing C_{BP1}, U_1 and M_1 to 'fly' to a higher potential. Note here that expended M_1 gate charge is released into the primary power path defined by M_1 and M_2 (highlighted in red).

However, in the case of Fig. 1 (d) this challenge is made significantly more difficult as the $V_{GS,DUT}$ swing of M_{DUT} is an arbitrary function of V_{POS}, V_{NEG}, L, C_{ISS}, and parasitics, and can easily extend beyond the power rails. For example, Fig. 2 shows $V_{GS,DUT}$ swinging between V_{PK+} and V_{PK-} where V_{PK-} need not equal 0V. As such, the high-side driver may not periodically return to a low impedance reference voltage as would ordinarily be the case in a conventional half-bridge (i.e. Fig. 3). Here, a simple bootstrap diode is inappropriate for power delivery and would lead to over/under-charging of C_{BP1} if the peak negative value (V_{PK-}) of $V_{GS,DUT}$ were to deviate from 0V. To resolve situations such as this, commercial solutions offer isolated power delivery for flying gate-drivers (e.g., ADUM5210), however these parts are often expensive with poor efficiency and have large volume due to the use of magnetics.

Instead, we propose the capacitive decoupling circuit depicted in Fig. 4, with several relevant waveforms depicted in Fig. 5. This solution removes the requirement for isolated power delivery and instead provides power to the high-side driver U_1 using a capacitive decoupling circuit comprised of D_{BT}, C_{BP1}, M_3, C_{G1} and C_{S1}. Here, C_{G1} and C_{S1} are significantly larger than the C_{ISS} of M_1 and allow the AC content of U_1's square-wave output to be applied to the V_{GS} of M_1 with near unity gain. As U_1 transitions to a logic low, it sinks charge through its negative supply onto the net $V_{SS,U1}$. Since C_{S1} represents a DC block, this charge cannot be dispersed into the drivers output stage as it was in the conventional gate driver (Fig. 3). Instead, M_3 is used to prevent charge accumulating on $V_{SS,U1}$.

As a result of the DC decoupling provided by C_{G1} and C_{S1}, U_1 and C_{BP1} can now 'fly' within an offset voltage range, albeit with the same AC magnitude. Turning M_3 ON during the negative peak of $V_{GS,DUT}$ (V_{PK-}) ensures that the lowest point of the voltage swing experienced by net $V_{SS,U1}$ is equal to 0V. This is illustrated in Fig. 5 where M_3 turning ON results in $V_{SS,U1}$ being shorted equal to 0V, effectively sweeping away the charge ejected by U_1 during its falling edge. This results in C_{S1} charging to (0V- V_{PK-}) and ensures that $V_{SS,U1}$ commutes definitively between 0V and ($V_{POS} - V_{PK-}$). Since the high-side driver now periodically returns to 0V, a bootstrap diode, D_{BT}, can be used to charge C_{BP1} near to V_{DD} as per conventional bootstrap operation (Fig. 3). If the steady-state minimum of net $V_{S,M1}$ or $V_{GS,DUT}$ were to change, (e.g. if V_{POS} or V_{NEG} were adjusted), the DC offset stored on C_{S1} will track appropriately since $V_{SS,U1}$ is forced to 0V every period. As such, power can always be delivered to U_1, irrespective of operating point. An appropriate gate signal for M_3 can be synthesized by leveraging the propagation delay of U_2.

In steady-state D_{G1} and R_{G1} act to ensure the correct offset is stored on C_{G1} irrespective of operating point: If $V_{GS,M1}$ goes significantly below 0V, D_{G1} turns on and increases C_{G1}'s offset. Conversely, R_{G1} continuously bleeds charge out of C_{G1} and the gate of M_1 ensuring $V_{GS,M1}$ does not operate with an excessively positive offset. An alternative solution to the $\{R_{G1}, D_{G1}\}$ pair is to replace them with a Zener diode that has a reverse voltage rating equal to the intended gate drive voltage of M_1. In this case the Zener will clamp $V_{GS,M1}$ within the intended range. Satisfying the level-shift requirement between U_2 and M_2 is much simpler as the source of M_2 has a fixed voltage offset relative to the negative rail of U_2; equal to V_{NEG}. Identical to the function of R_{G1} and D_{G1}, here R_{G2} and D_{G2} ensure an appropriate offset is stored across C_{G2}.

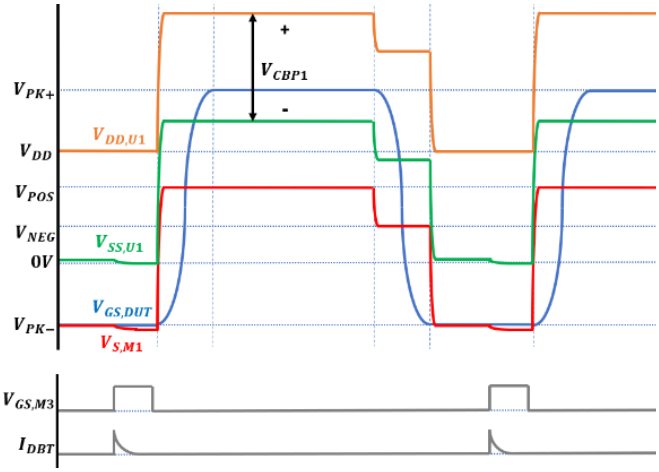

Fig. 5. Waveforms relevant to high-side capacitive decoupling. Note that $V_{SS,U1} \geq 0V$, allowing use of bootstrap diode D_{BT}.

IV. Discrete Prototype

Figure 6 depicts a discrete implementation of the proposed gate-driver alongside a silicon carbide DUT. The driver was used to control four different commercial FETs: one silicon (Si), one silicon carbide (SiC) (depicted), and two gallium nitride (GaN). The FETs were chosen for their low intrinsic gate resistance, R_{GATE}, with respect to C_{ISS}; a property critical in maximizing Q-factor and subsequent resonant gate driver efficiency. Manufacturers often deliberately increase R_{GATE} within a power device to increase reliability and immunity to ringing and/or ESD events in hard-charged driver applications. As such, a power FET with low R_{GATE} designed explicitly for resonant driving schemes would likely further improve gating loss.

The proposed gate-driver enables the use of two N-channel devices in the driver's output stage, significantly decreasing parasitic losses which ultimately limit the driver's frequency of operation. Furthermore, two small GaN devices are chosen for their greatly reduced parasitic capacitance relative to Si-based output stages, extending the efficacy of this design at high switching frequencies. One of two inductors was used for each device tested, 12.3 nH or 27 nH, providing an estimated Q-factor of ~5-12, where;

$$Q \cong \frac{1}{R_{GATE}} \sqrt{\frac{L}{C_{ISS}}} \quad (1)$$

and when discounting parasitic losses. This region was chosen to provide a moderate balance between gating-loss reduction and increased rise/fall times. Details of the components used are listed in Table I. The driver's total component volume is 17.4 mm^3 with 55% of that being the LMG1210 gate-driver, ~28% the inductor, and 8.5% the GaN-FETs.

Table II lists measured results for the proposed gate driver when applied to a selection of commercial power FETs. V_{DD}=5V for all cases. The maximum and minimum $V_{GS,DUT}$ gate voltages, V_{PK+} and V_{PK-}, were selected by manually adjusting V_{POS} and V_{NEG}. In the case of the Si and SiC devices, V_{POS} was

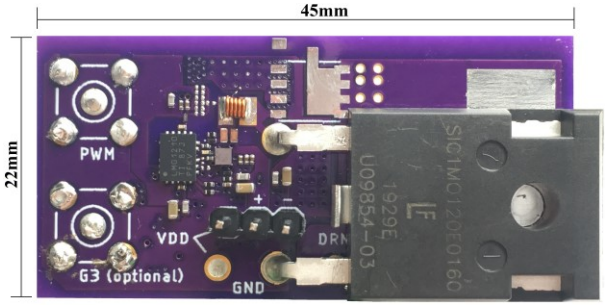

Fig. 6. Photograph of the prototype gate driver test board. The proposed gate driver solution occupies only 7 x 7 mm^2 despite its added complexity.

TABLE I. Component Details

Device	Details	Part Number
M_{DUT}	Si 150V	FDMS86252
	GaN 40V 53A	EPC2015C
	GaN 100V 90A	GS61008T
	SiC 1200 V 22A	LSIC1M0120E0180
L	12.3 nH 2.9A	0806SQ-12NJLB
	27 nH 3.5A	1812SMS-27NJLC
M_1	60V 1.7A (30pF)	EPC2108_Q1
M_2	60V 1.7A (40pF)	EPC2108_Q2
M_3	100V 0.5A (4pF)	EPC2108_Q3
U_1, U_2	50MHz Gate Driver	LMG1210
D_1, D_2	0.23V@100mA (28pF)	DB2G40800L1
D_{G1}, D_{G2}	0.24V@1mA (0.25pF)	JDH2S02SL
R_{G1}, R_{G2}	10Kohm 5%	RC0201JR-0710KL
C_{G1}, C_{G2}	910pF 25V C0G	TMK063CG911JT-F
C_{S1}, C_{BP1}	10nF 25V X5R	GRM033R61E103MA12J
C_{BP2}	0.1uF 25V X6S	GRM033C81E104KE14D
D_{BT}	0.37V@100mA (7pF)	PMEG4002AESF
R_{DHL}, R_{DLH}	82kohm	RC0201JR-0782KL
U_3	2-Input AND	SN74LVC1G08

TABLE II. Measured Gate Driver Results

Device	FDMS86252	LSIC1MO120E0160	EPC2015C	GS61008T
Technology	Si	SiC	GaN	GaN
Rating	150V, 16A	1200V, 14A	40V, 53A	100V, 90A
R_{GATE} (Ω) | C_{ISS} (pF)	0.4 | 678	0.95 | 870	0.3 | 980	0.64 | 590
L (nH)	12	27	12	12
f_{SW} (MHz)	17.5	10.29	17.5	20.5
t_r / t_f (ns)	8.6 | 9	17.9 | 16.4	10.1 | 9.6	7 | 6.7
V_{POS} / V_{NEG} (V)	5 | 2.3	5 | 0	3.4 | 1.5	3.8 | 1.4
V_{PK+} / V_{PK-} (V)	7.8 | -0.55	9.48 | -5.64	5.1 | -0.55	5.94 | -1.5
I_{POS} = I_{NEG} (A)	0.161	0.267	0.15	0.143
P_{POS} / P_{NEG} (W)	0.805 | -0.37	1.335 | 0	0.51 | -0.225	0.54 | -0.2
P_{DD} (W)	0.162	0.106	0.164	0.182
P_{Total} (W)[a]	0.597	1.441	0.449	0.526
$P_{Total\text{-}Hard\text{-}Charge}$ (W)	1.824	3.059	1.201	1.856
% Reduction in loss relative to Hard-Charged	-67.25%	-52.89%	-62.61%	-71.66%

[a] P_{TOTAL} is the sum of P_{POS}, P_{NEG}, and P_{DD}, where P_{NEG} can be negative due to energy recovery.

set equal to V_{DD} and, in the case of the SiC device, V_{NEG} was set equal to 0V, eliminating the need for any additional power supply circuitry to generate V_{POS} or V_{NEG}. Given this gate-drivers' high impedance holding state, in order to avoid the possibility of Miller turn-on, V_{PK-} was selected in all cases to be sufficiently negative to ensure that $V_{GS,DUT} < 0V$ for a $V_{DS,DUT}$ increase from 0V to 70% of its $V_{DS,MAX}$. The expected $V_{GS,DUT}$ increase due to Miller feed-through was estimated using the C_{RSS} and C_{ISS} capacitance listed in device datasheets. Since this driver type has intended use in resonant or ZCS/ZVS soft-switching converters where reduced rise/fall times are acceptable, $V_{DS,DUT}$ was shorted to ground with no bus voltage applied. Further data acquisition with a time-varying $V_{DS,DUT}$ would serve to empirically validate the driver's expected immunity to Miller turn-on.

To compare the gating loss of this resonant driver topology to that of a conventional hard-charged gate-driver, the inductor and diodes were shorted while V_{POS} and V_{NEG} were set equal to the previously measured resonant peaks, V_{PK+} and V_{PK-}. This effectively converts the driver into a conventional hard-charged half-bridge output stage (Fig. 3) with the same drive voltages being applied to the DUT. Since resonant action has been removed, CV^2f gating losses are reintroduced. Table II lists the relative improvement in losses seen by the proposed resonant topology versus the conventional half-bridge output stage. All devices tested saw at least a 52% reduction in total losses.

Figure 7 depicts a measured $V_{GS,DUT}$ waveform with expected symmetric oscillations about V_{POS} and V_{NEG}. Additionally, Fig. 8 depicts a measured gate signal with varying pulse width duration, illustrating this resonant driver's suitability for use in topologies with diverse duty-cycle requirements. A gradual $V_{GS,DUT}$ settling is also observed in Fig. 8 from t = 0.25 µs to 0.34 µs. This effect is due to leakage and the charging of parasitics throughout the driver stage. Since this driver is high-impedance while holding, leakage results in a lower bound being placed on switching frequency, further high-lighting the importance of non-ideal element considerations.

V. Conclusion

Operating at high frequencies (10-20 MHz), the proposed gate-driver achieves up to a 72% reduction in gating-loss when compared with conventional hard-charging gate-drivers. While generally used as primary switching elements, here GaN-FETs contribute to the driver's attainable switching frequency through their reduced parasitic capacitance. To facilitate this, a capacitive decoupling technique is described which allows use of a high-side N-channel device in the driver's output stage. Future work will include applying the proposed topology to a functional resonant converter, developing the system of equations defining the steady-state operating point, including parasitic contributions, and demonstrating a complete closed loop energy recovery system.

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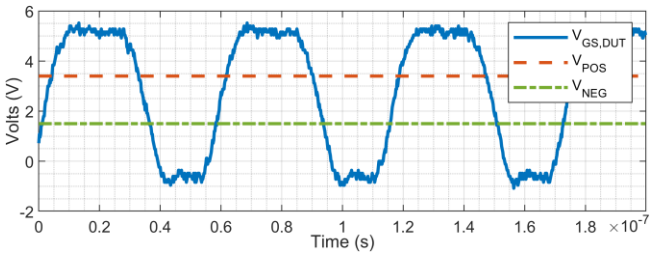

Fig. 7. Measured $V_{GS,DUT}$ waveform for the EPC2015C GaN-FET operating at 20.5 MHz. V_{POS}=3.8V, V_{NEG}=1.4V, and L=12 nH.

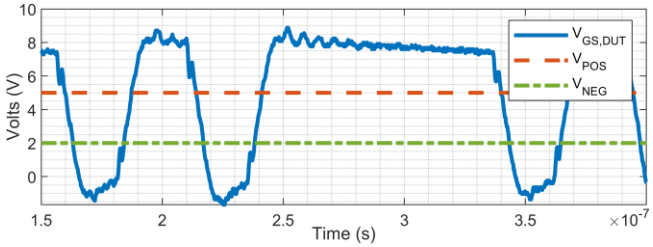

Fig. 8. Measured $V_{GS,DUT}$ waveform for the FDMS86252 Si-FET with a varying duty cycle. V_{POS}=V_{DD}=5V, V_{NEG}=2.3V and L=12 nH.

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