UNIVERSITY OF CALIFORNIA SAN DIEGO

Ka Band Transmit and Receive RF-Beamformers on 22nm FD-SOI Technology for Communication and Radar Systems

A Dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Sultan Awad Ali Alqarni

Committee in charge:

Professor Gabriel Rebeiz, Chair
Professor Kam Arnold
Professor Gert Cauwenberghs
Professor Drew Hall
Professor Tzu-Chien Hsueh

2024

The Dissertation of Sultan Awad Ali Alqarni is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

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EPIGRAPH

The last page from the “Nobel Quraan.”
[Source: https://quran.ksu.edu.sa and https://qurancomplex.gov.sa]

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In the name of Allah, the Entirely Merciful, the Especially Merciful. All Praises to Allah, Lord of the worlds. Oh Allah, you are the Sovereign, the Truth; there is no deity except you, The Lord of the Nobel Throne. Oh the Generous, your blessings are uncountable. Oh the Knowing, I am blessed by your generosity in completing the Ph.D. May you, the Creator of everything, accept this work as a good deed for my parents, my grandparents, my siblings, my wife, and me.

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VITA

2011 Bachelor of Science in Electrical Engineering (Communication and Electronics), King Saud University

2012 King Abdulaziz City for Since and Technology (Electronics, Communications, and Photonics National Center), Academic Researcher

2018 Master of Science in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego

2024 Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego

ABSTRACT OF THE DISSERTATION

Ka Band Transmit and Receive RF-Beamformers on 22nm FD-SOI Technology for Communication and Radar Systems

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Sultan Awad Ali Alqarni

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

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Professor Gabriel M. Rebeiz, Chair

This dissertation comes as an application of receive and transmit phased array beamformers on 22 nm fully depleted silicon-on-insulator technology. They both use the concept of passive vector modulation for higher linearity. The advantage of the smaller feature size switches was used to implement the design at the Ka-band with minimized losses.

The receiver IP-1dB is higher than -20 dBm with a power consumption of 60 mW at typical biasing. The biasing was varied for gain from 11 dB to 18 dB, 5 GHz bandwidth (24-29 GHz), and power consumed from 35 mW to 180 mW. The noise figure is optimized to be at 3 dB while minimizing the power consumption. The phase error standard deviation is less than 4.5 degrees for 6-bit phase shifters. The gain error standard deviation is less than 0.25 dB for the attenuators.

The Ka-band transmit channel, beamformer, has an OP-1dB is 15.5 dBm with 12.5 % efficiency of the entire channel. For the QAM-64-100 MHz modulated signal, the efficiency is 7.9 % at EVM of 3.7 % and output power of 13.1 dBm. The gain is 27 dB, and the 3 dB bandwidth extends from 22.5 GHz to 26.8 GHz. The channel 6-bit phase shifters have 5.5-degree phase error standard deviations at the center frequency and 2 degrees at 26.8 GHz. The attenuator's gain error standard deviation is less than 0.4 dB within the transmitter band.

Chapter 1 INTRODUCTION

Solid-state devices reached beyond 500 GHz of unity frequency in transistors fabricated from compound semiconductors at feature lengths of 100 nm. Bulk Complementary Metal-Oxide-Semiconductor (CMOS) devices' parasitics prevent them from further unity frequency increase beyond 400 GHz with technology nodes less than 20 nm. Silicon-On-Insulator (SOI) technology devices kept many CMOS advantages while reducing the devices' parasitics. This allows it to have higher unity frequencies compared to bulk CMOS devices [1].

Solid state circuits and systems are constantly searching for the new optimum set of performance parameters and for more circuits and systems integration. Electromagnetic sensing and communication systems achieve more maturity and flexibility in terms of already defined standards or adapting new standards with higher performance [1,2].

All leads to more data experiences for users, whether it is for a surgery or a game. And hopefully, that is beneficial and not harmful. It is a challenge and opportunity with respect to many life aspects, like health, educational, military, or economic aspects, for engineers to invest their efforts, ethically and nobly, in newly developed technologies.

Solid-state phased-array transceivers are being deployed more, relaxing many systems' specifications. Nothing is perfect; however, they provide electronic control of the antenna beam or simultaneous beams, space power combining, and high performance without the need for extreme circuits and devices' specifications [3].

Radio Frequency (RF) transceivers generally employ an amplifier, a frequency translation—sometimes more than once— and a data converter. In phased arrays' RF transceivers, a combining/splitting architecture has to exist, and the array's elements must include beam management blocks.

Combining an incoming received wavefront from any specially spaced antenna-receiver elements requires the availability of time delay units to align the receivers' output waves in the perfect sense, true time delay units may be replaced with phase shifters within Inter-Symbol Interference (ISI) limits of operation [4]. Therefore, a combing scheme with phase control per element is necessary to provide the phased array transceiver with a larger energy allocation in a specific direction.

In addition, for beam tapering or windowing, the elements must include an amplitude control function. Also, in contrast with phased array receivers, transmitters' input signal is split to reach the element using splitters; then, the elements apply the amplitude/phase control. And after the antennas radiate the elements' signals, the elements' powers are combined in space coherently. That leads to a decrease in the required power generation per element compared to non-array transmitters' power generation devices—solid-state power amplifiers are suitable for high Effective Isotopically Radiated Power (EIRP) phased array transmitters since they are medium-low power generators [6].

For example, in RF receivers, the front end usually uses an Low Noise Amplifier (LNA) followed by a frequency translation —mixer— and then a data converter. If the phased array receiver uses LNA followed by mixer per element, then the combining scheme would be at a low frequency whether the phase shifting is created at the mixer oscillator input or after the mixer output. However, if the combining was done after the LNA and before the mixer, then the combing would be at RF frequencies and the phase shifting elements must be in RF, perhaps after the LNA and before the power combiner. Therefore, a choice must be made for the combing and phase shifting frequencies. This selection extends even to the type of the signal since a "data converter" may be inserted per each element as in Digital Beam Forming (DBF), [4,5]. Digital beamformers provide

soft control of the beam and simultaneous beams. However, RF combining is usually preferred over DBF due to the following:

- Cancellation of an interference/jamming by nulling the angle of the source can be done in the RF combining network before any frequency translation.
- No global fast clocks, such as for sampling, or reference oscillators, as in mixers, need to be distributed.
- Power consumption.

In addition, "hybrid" combining techniques were developed to balance costs and advantages [3,4].

It should be noted regarding multiple beams in link budget management that, for the same hardware receive front ends with the ability of multiple beam conditioning, the received single beam energy—or received power (P_r) at the receiver output—with single port output is going to be reduced to multi-simultaneous receive beams energies with the multi-port outputs, according to the energy conservation principle. In another way to understand it, it is possible to make the receiver receive multiple beams from a single direction, leading to higher received energy. On the other hand, in transmitters, the EIRP would be reduced in multi-beam scenarios. That is compared to the maximum possible EIRP that can be created using a single beam scenario and by the same hardware. Therefore, multiple beam employment results in link or range reduction compared to the single beam for the same phased array transceiver.

It is of interest to use phased array transmit/receive systems efficiently, especially for the transmit array. For example, if a transmitter element of 5 % efficiency and 50 mW output power is used for a 1000-element array, that means 950 W would be dissipated on the array, which requires heat management. Therefore, efficient elements are essential as the elements' power and number of elements increase.

22 nm Fully Depleted Silicon-On-Insulator (FD-SOI) devices, by Global Foundry, have a high unity frequency compared to other CMOS devices [1,7]. This spec generally leads to better efficiency and less loss in switches. However, with lower device channel lengths, the device's maximum reliable voltage approaches the minimum saturation voltage. That leads to lower maximum linear output power compared to similar designs that have devices with larger lengths. Nevertheless, power amplifiers in this technology can provide up to 40 % Power Added Efficiency (PAE) [7,8] at the Ka-band with tens of milli-watt output power. The devices' noise performance in the Ka-band is demonstrated in an LNA with less than a 2 dB Noise Figure (NF) [9].

The thesis focuses on implementing phased array single receive and single transmit RF beamformers on Global Foundry's 22 nm FD-SOI technology. The optimum performance that was looked for in this work is to use the technology for Ka band RF combining phased array receiver and transmitter with sufficient gains, noise figure of 3 dB for the receiver, and transmitter's saturation power larger than 60 mW at the highest efficiency possible. For beam management, the phase and gain steps are designed for less than 6 degrees and 0.5 dB, which is targeted with high linearity.

The maximum linear input power in RF systems would constrain the minimum power consumption and vice versa. Therefore, receiver amplifiers' devices sizing is mainly defined by linearity and power consumption. The low noise figure in the receiver requires an LNA in front and a minimization of the NF of each stage. For the transmitter, the delivered output power requires a set of power amplifiers to achieve that in an efficient manner.

Thesis chapter two is for the Ka-band receiver beamformer. Chapter three is for the Ka-band transmitter beamformer. Both chapters include the designs and measurements while chapter four is the conclusion of the thesis.

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Chapter 2 Ka-Band Receive RF-Beamformer Using Passive Phase Shifters and Attenuators on 22FD-SOI Technology

The chapter sections are divided to explain the receiver architecture and components' design. Section two is for the receiver architecture. While sections three to six explain each block's design. Sections seven and eight show the beamformer integration and measurements. At last, the design is compared with other similar designs in conclusion.

2.1 Architecture

Analog combining architecture requires control over each element of the array to be phase shifted or time delayed. To implement tapering- minimization of the beam's side lobe level- gain control would be required. In addition, to have a higher Signal-to-Noise Ratio (SNR), the noise figure is minimized by inserting a low noise amplifier at the input. Also, the receiver's maximum linear input power must be optimized with the beamformer power consumption, which helps to have a higher dynamic range. The architecture was built to achieve the previously mentioned goals.

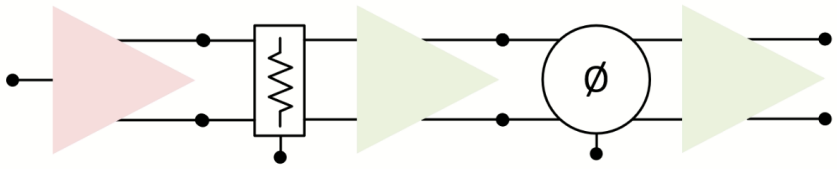

Figure 2.1: Channel block diagram.

In 22 nm transistors, the maximum voltage to be applied between its active terminals (gate, source, and drain) is 0.8 V. This limit on the transistors affects the maximum linear power to be provided by a single transistor. This is in comparison with transistors that have larger feature lengths, and both are at the same current density. However, that limit would also be a power consumption reduction. If the system was implemented on a specific impedance, then the maximum voltage

allowed limits the maximum power transfer between system nodes. Thus, by lowering the devices' feature length and keeping the system at fifty ohms, for example, the design would not be able to drive the same power while the circuits can operate at low power consumption at the same time. Also, this means that limiting the voltage would not affect the drain efficiency— ideally and neglecting Vdsat.

The device size determines the device's capacitances. That produces higher unity frequencies in smaller transistors, but that needs to be noise or power-matched for RF frequencies. In tuned designs, extra matching elements may be needed to meet overall performance. In passive phase shifters and attenuators, the low device size is helpful since the switches would provide fewer parasitics. That shows in lower loss across frequency. However, that results in less linearity compared to devices with larger voltage limits.

The architecture, Figure (2-1), is composed of a low noise amplifier at the input to shield the rest of the system from degrading the noise figure, as much as possible. Followed by five attenuators that attenuate the signal power from 0 dB to 15.5 dB prior to any further process. A gain amplifier is needed to compensate for the attenuators' loss and to provide matching and isolation between the attenuators and the phase shifters. Six phase shifters are added after that to shift the signal phase from 0 to 355 degrees. At last, the signal is amplified using a gain amplifier to compensate for phase shifters' loss and, again, to provide matching and isolation for the phase shifters and the output.

The system was implemented differentially with 50 Ω as a single-ended reference impedance. The input from the antenna is designed to be single-ended; hence, the low noise amplifier transforms the single-ended input signal to a differential at its output, using Balanced-to-Unbalanced (BALUN). The common mode is rejected as much as possible in each gain stage, effectively three times after the BALUN.

Matching is important for attenuators and phase shifters to apply a fixed intended state effect. Therefore, the gain amplifiers' ports' reflection minimization was preferred over the gain and noise performance. In addition, the phase shifter and attenuator, as blocks, must provide matching over their states.

Cascading amplifiers mean extra work on the bandwidth requirement. The targeted 1 dB bandwidth is approximately the system 3 dB bandwidth. That is without considering the attenuators' rate of loss over the frequency and phase shifters' many frequency responses over their states. Therefore, the blocks' bandwidths must be carefully widened- or flattened- during its design.

2.2 Low Noise Amplifier

The low noise amplifier enables the system to have other components with relatively higher noise figures. To achieve that, a low noise amplifier gain must be high enough so that the noise floor at each component's input is higher than the component's input-referred noise floor alone. That leads to the minimum noise contribution of other blocks to the total input-referred noise floor. This concept applies to the low noise amplifiers' stages as well. So, the first stage gain is important as its noise figure. The input-referred noise floor from the first stage alone is considered the starting point of the noise floor level throughout the system, and it should be as low and dominant as possible. The other low noise amplifier's stages must also provide low noise contribution so as not to overwhelm noise resulting from the preceding stages. The noise figure (F) of multiple linear time-invariant stages with gain (G) is:

$$F_{LNA} = F_{1st} + \frac{F_{2nd} - 1}{G_{1st}} + \frac{F_{3nd} - 1}{G_{1st}G_{2nd}} + \cdots \quad (1)$$

The single-stage noise figure is optimized using noise-matching. Fundamentally, the device operates at best regarding noise by finding the optimum current density versus noise-figure-minimum and then matched to its optimum noise impedance (Y_{sopt}). It should be remembered that the noise-figure-minimum is different than the noise figure. The noise figure is the result of imperfect noise-matching at the input. Hence, the noise figure can be minimized to the limit of noise-figure-minimum (NF_{min}). That is:

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|^2 \quad (2)$$

IEEE standard provides a conventional definition of the noise parameters in (2). Nevertheless, for a given transistor, at a frequency (f) and a current density (j_c), the noise-figure-minimum should not

be affected by its size (W), ideally. The effect of sizing shows up in other noise parameters — $R_n(j_c, f, W)$ and $Y_{sopt}(j_c, f, W)$, while keeping the noise-figure-minimum fixed [2].

$$NF = NF_{min} + \frac{R_{n,o}\frac{W_o}{W}}{G_s}\left|Y_s - \frac{W}{W_o}Y_{sopt,o}\right|^2$$

$$NF(j_c, f, W)$$

$$NF_{min}(j_c, f) \tag{3}$$

$$R_n(j_c, f, W) = \frac{W_o}{W}R_{n,o}(j_c, f)$$

$$Y_{sopt}(j_c, f, W) = \frac{W}{W_o}Y_{sopt,o}(j_c, f)$$

Power-matching, low S11, was considered. Hence, inductive degeneration was included to increase input real resistance. For perfect power-matching, a large gate inductance must be added to compensate for the small Cgs, especially if a power-constrained design was chosen with a small device width and length.

Adding source inductance will create a new noise-matching problem, unlike a single transistor with its source being grounded. An infinite quality of the reactive degeneration of an ideal transistor model, only Cgs and gm, will not change the minimum noise figure or the noise-figure-minimum but will change the other noise parameters. Real models need to be simulated for accuracy and to include the finite quality of all inductors, all transistors' small signal components, and the transistor's model of noise.

Differential stages differ in nothing important in terms of noise and gain analysis, differential input to differential output mode [3]. However, the common mode gain must be minimized.

Therefore, a common mode inductor was added. In the design process, the noise figure and differential gain are expected to change adversely.

Figures (2-2,3) show the schematic design of the LNA and its layout. The single-ended input low noise amplifier's first stage is an inductively degenerated cascode. The cascode is loaded with a BALUN to translate the signal to differential mode. The second stage is differential and inductively degenerated cascodes with an inductor used for common mode rejection.

A power-matching network is done at the output stage since it is the attenuators' source impedance. The network provides 100 Ω differential resistance, 25 Ω common mode, from the amplifier output. The output matching network provides the LNA with a wide bandwidth response, that is, with low output reflection in the band.

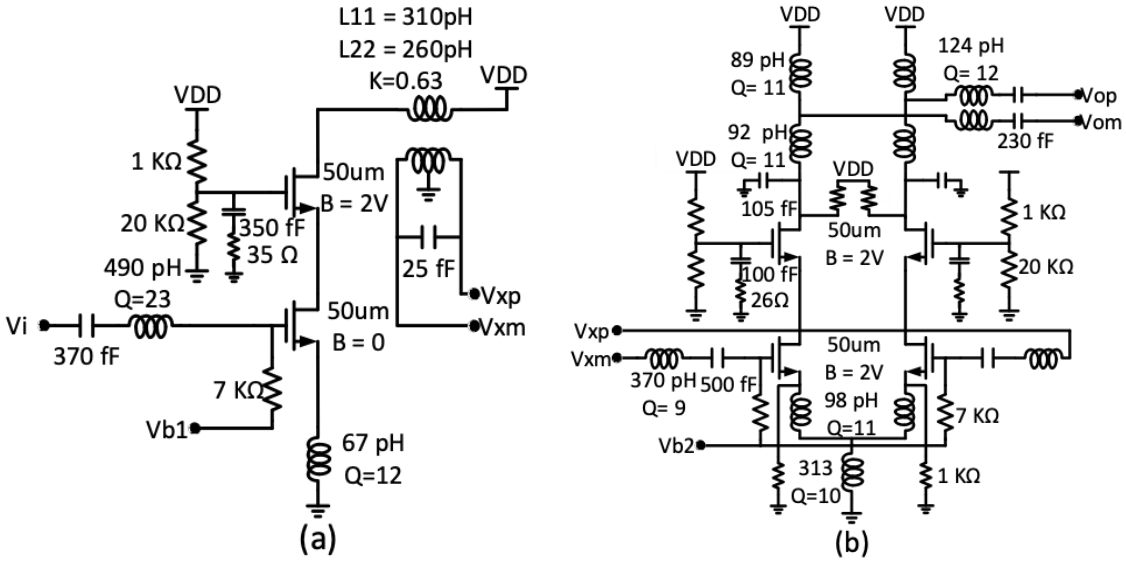

Figure 2.2: Schematic design of the single-to-differential ended LNA. (a) first stage of the LNA. (b) second stage of the LNA.

The device sizes are the same for all cascodes. However, the current density is not. For the first stage, the current density is set at the optimum current density for the noise figure to maximize the gain and linear power range and minimize the power consumption. The valley of noise-figure-

minimum versus the current density, as shown in [4], can be used by increasing the current density beyond the optimum for gain and linearity, which is the case for higher power consumption states. For the second stage, the density was selected to minimize power consumption rather than noise and gain, in typical biasing.

The design passives at the first stage were intended to have high quality. The gate inductor has no ground plane to increase the inductance and quality factor, though there is a ground wall. To avoid substrate loss, a high resistance layer beneath it was added.

Stabilizing resistances were added at the cascode gate in two ways, one to the ground through the capacitor and the other to the supply through the gate biasing. The analysis of required capacitance C_c were small for stable operation with small transistor widths, [5,6]. Differential and common mode stabilities were relaxed by adding the resistors, which also used in [16]. In the second stage, the passives were kept at a satisfactory level of quality factor. Almost every point was ensured to have a maximum quality limit not to be exceeded. Figure (2-4) shows the simulation results of the LNA.

Generally, for any block in this design, the following layout strategies were followed. First, Decoupling capacitors were added as close as possible to the circuit for each supply and as much as possible toward the supply's pad. Also, ground planes and walls thickness and density were maximized in RF and non-RF areas. For RF areas, distances from the grounds of the RF lines were ensured to be effective for the required operation. Also, RF grounds are preferred to be made from thick metals compared to thin metals which are highly resistive, lossy, and time-consuming for electromagnetic simulation. However, thin metals must be used in some layout situations, like transistor layout and general device modeling. In addition, Electrostatic Discharge (ESD) protection was included in every non-RF pad.

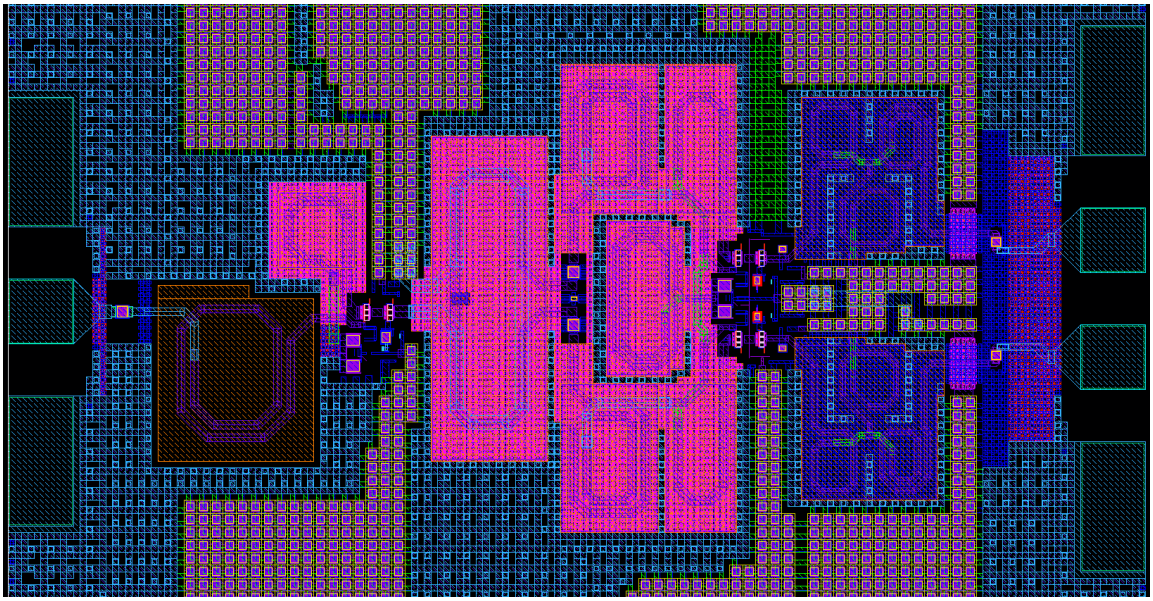

Figure 2.3: LNA layout.

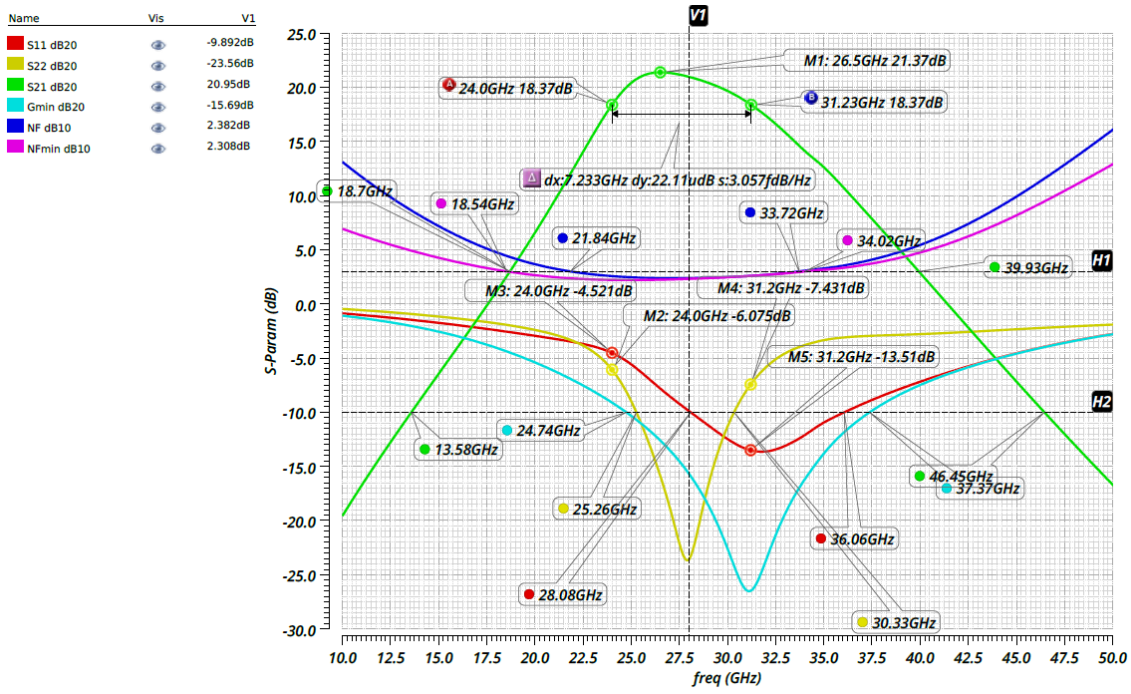

Figure 2.4: Simulation results of the LNA.

2.3 Gain Amplifier

The gain amplifier was designed to be like the second stage of the low noise amplifier. However, the input matching network in the low noise amplifier is matched with the inductive BALUN network. The gain amplifier input impedance is the output's resistive impedance of the attenuators or phase shifters. Therefore, the input matching of the gain amplifier was redesigned to satisfy that.

The input impedance of the second stage in the low noise amplifier gives a negative reactance. The required gate inductor is large, and further increasing its value would lower the resonance frequency of the inductor and raise stability and bandwidth issues. Hence, an increase in gate inductance was avoided in the gain amplifier.

A solution to this matching problem is to change the effective capacitance of the gate itself [3]. That is according to:

$$Z_{in} \approx sL_g + sL_s + \frac{1}{sC_{gs}} + f_t L_s \tag{4}$$

This can be done by increasing the size of the device or by adding a capacitor between the gate and the source to have:

$$Z_{in} \approx sL_g + sL_s + \frac{1}{s(C_{gs} + C_o)} + f_t L_s \tag{5}$$

The first method would require more power dissipation compared to the low noise amplifier second stage since the current density of the devices was kept as low as possible, and further decrease results in lower gain and noise figure. The second method is effective in matching, but it would degrade the gain and noise figure of the amplifier. They would be reduced due to less effective transconductance of the input transistors, or less unity frequency of the transistor.

Adding an extra capacitor is selected because the amplifier gain aims to overcome passive components' losses and provide isolation. While the extra power consumption of the third and fourth gain stages would improve the noise figure and linearity in general, the improved noise figure would be within 0.5 dB, and linearity improvements would require geometric increases in the power consumption per stage. However, the noise figure after applying the attenuators would increase. It would be minimized by assuring that the gain stages have high gain with low noise figures. To summarize, the effects of the amplifier's gain and noise figure on the system's noise figure and linearity:

$$F_t \approx F_{LNA} + \frac{\left\{ F_{GA} - \frac{\left(\frac{G_{GA}^2}{L_{att}} + G_{GA} + \frac{1}{G_{LNA}}\right)}{(G_{GA}^2 + G_{GA} + L_{PhS})} \right\}}{G_{LNA} \frac{G_{GA}^2}{L_{att}(G_{GA}^2 + G_{GA} + L_{PhS})}} \tag{6}$$

$$OP_{-1dB,BF} \approx \frac{G_{GA}G_{GA}}{L_{PhS}L_{Att}} OP_{-1dB,LNA} \parallel \frac{G_{GA}}{L_{PhS}} OP_{-1dB,GA} \parallel OP_{-1dB,GA} \tag{7}$$

Figure (2-5) shows the schematic design of the gain amplifier while its layout is like the LAN layout.

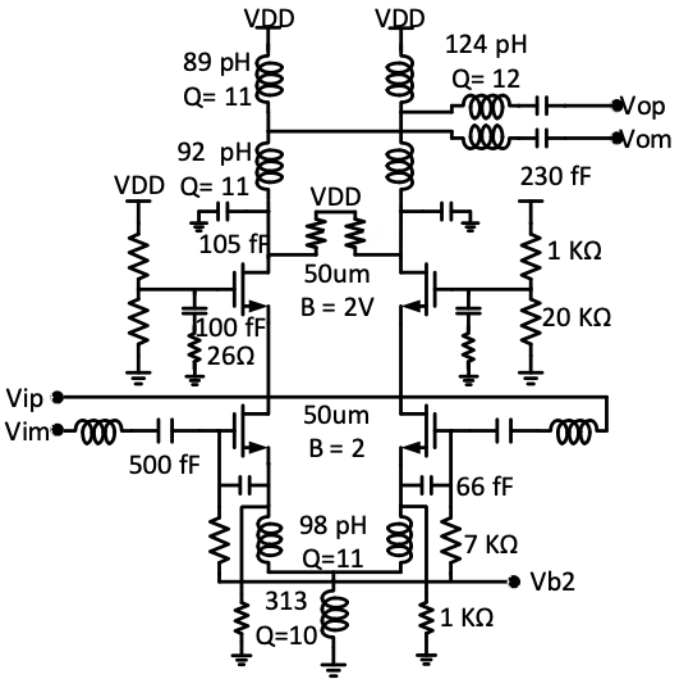

Figure 2.5: Gain amplifier schematic design.

For example, the noise figure and compression powers can be analyzed as:

$$for\ OP_{-1dB,LNA} \approx OP_{-1dB,GA} \approx 2\ mW = 3\ dBm$$

$$and\ L_{PhS} \approx L_{Att} \approx 4\ ;\ G_A = 2.5$$

$$and\ G_{LNA} \approx 80\ and\ F_{GA} \approx F_{LNA} \approx 1.8$$

$$\therefore F_{BF} \approx F_{LNA} + \frac{\{F_{GA} - 0.32\}}{9.8} \approx 1.95 = 2.9\ dB \tag{8}$$

$$and\ G_{BF} \approx 31.3\ \frac{mW}{mW} = 15\ dB$$

$$\therefore OP_{-1dB,BF} \approx 0.24\ mW = -6.2\ dBm$$

2.4 Phase Shifters

Ideally, a phase shifter should only apply a phase on the original transfer function where no phase is needed. That is:

$$\frac{G_{phased}}{G_{not\ phased}} = e^{-j\theta} \tag{9}$$

It should be noted that phase shifters may not be effective if the phased array has a large number of elements in any dimension. That is because applying phase shift on the received signal at an element is not necessarily equivalent to applying the physical time delay, which is the true time delay between elements. The two would be equivalent if the signal is a single-frequency signal. A received signal modulated with a message may receive a corrupted message, ISI. Therefore, the choice of phase shifters or true-time delay must be made according to the dimensions of the antenna and massage bandwidth [1]. In this design, the phase shifters were not implemented as true-time delay, even if they were.

Figure (2-6) shows the schematic design and the layout of the phase shifters. The design comprised six passive stages that create phase shifts from 180 degrees to 5.6 degrees. In [7-11], a detailed circuit analysis was presented. All switches have the smallest feature length. Each phase shifter requires matching in the band of the design. In addition, it is necessary to have the ON/OFF states of a single stage to be similar in loss. Sometimes, an improvement of the switch is not necessarily helpful if the opposite state has a limiting loss. The opposite is true when the metal stack is much better than what the device can offer. Matching the loss between ON/OFF states is usually based on knowing the effective parameters in both transfer functions. Therefore, systematic errors are expected in the phase shift and gain. Also, the phase and gain error in a single stage is not always

expected to be constant when cascaded with other phase shifters. They are expected to interact, resulting in different errors.

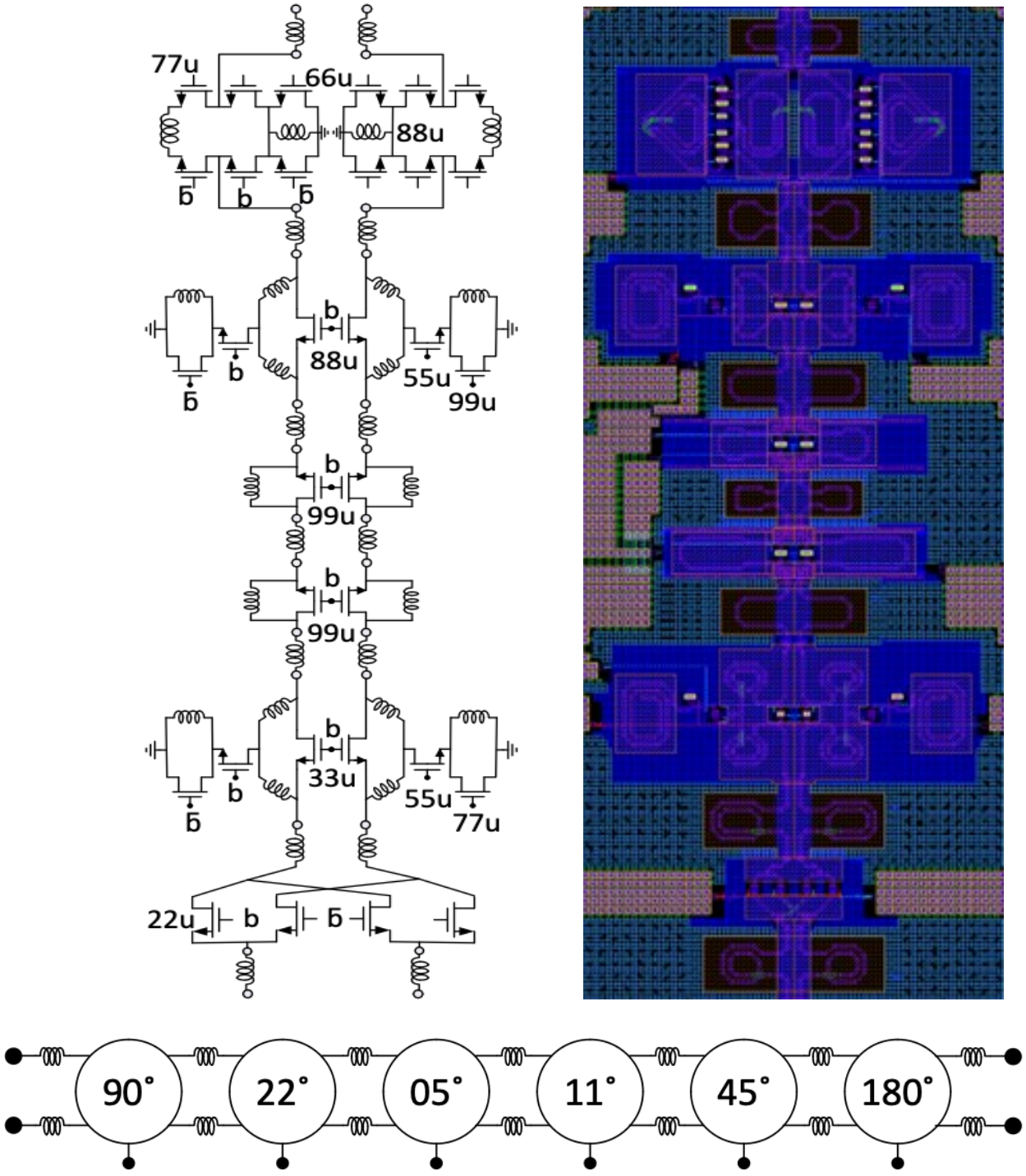

Figure 2.6: Phase shifters diagram, schematic, and layout.

The standard deviation of phase shift errors and standard deviation of loss errors are selected as the parameters to quantify errors across the 2^N states. The standard deviation of the errors should be kept minimal over the entire band of the design since it varies over frequency. Usually, the minimum standard deviation is at the frequency used in optimization.

The low phase shifts, 5/11 deg, were designed with large transistors for less loss. The phase shifters of 22/45/90 degrees were perfected in terms of the passives' values, quality factors, and switch sizes. The 180-degree phase shifter is a path switch. Also, inductors between stages were used for phase shifters intra-matching to 100 Ω differentially. The phase shifters simulation results are shown in Figure (2-7)

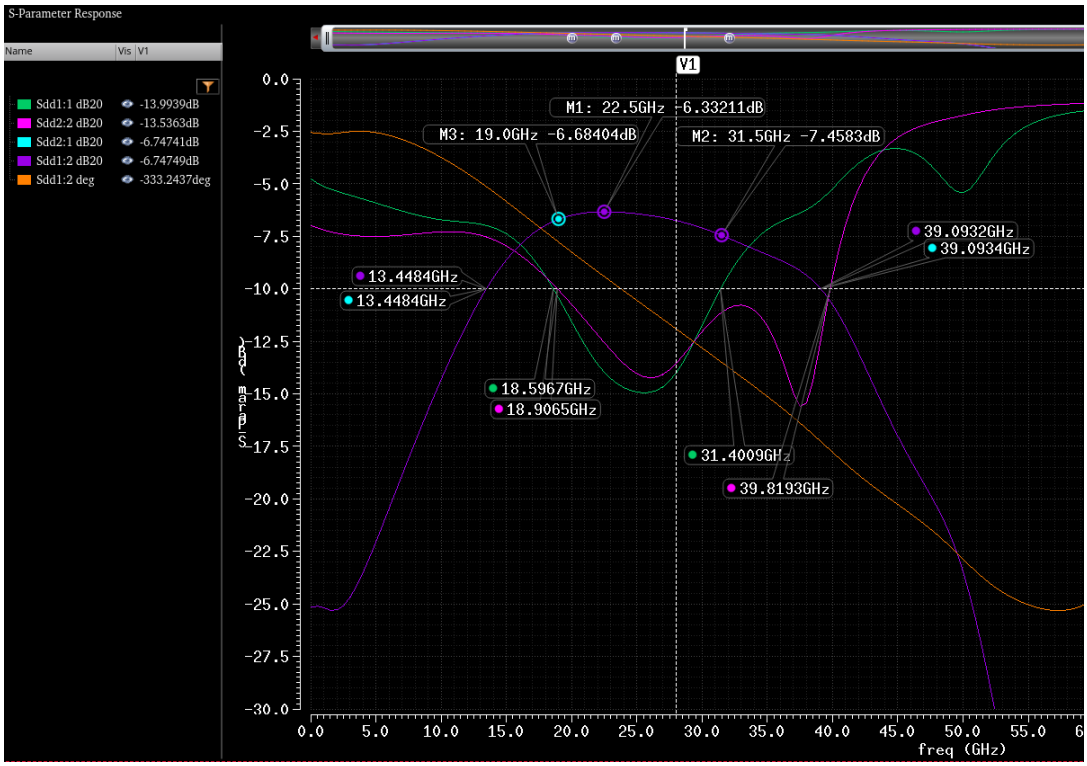

Figure 2.7: Simulation results of the phase shifters at its first state.

2.5 Attenuators

The attenuators were used for their good linearity impact on the beamformer. The five stages attenuate the incoming signal power from 0 to 15.5 dB, plus the fixed loss. It was inserted after the low noise amplifier to attenuate large inputs early. Figure (2-8) shows the schematic design and its layout.

The attenuators circuit is referred to as the "Pi" model [12,13]. It is symmetric, meaning its matching for input is the same as for the output. The attenuators have a low pass frequency response that starts from dc. The loss increases as the frequency increases by a fixed rate up to 40 GHz. It was optimized for a low standard deviation of errors at 28 GHz.

Each attenuator ground switches ware made as small as possible so that it does not influence the parallel resistances while it is at the attenuation state. Also, its small size would make the to-ground arm at higher impedance, in no attenuation state.

The pass switches were made as large as their on-state loss can be minimized. The pass switch off-state impedance must not affect the pass branch impedance, especially at high values of attenuation. Inductance was included in the pass arms to preserve the phase shifts and to keep matching during the ON and OFF states [13]. Another inductor was added to each stage to compensate for negative reactance input/output impedances. The stages were integrated by separation of large attenuation stages and combining intra-stage inductors resulting in less interaction between stages and higher resonance frequencies of the inductors.

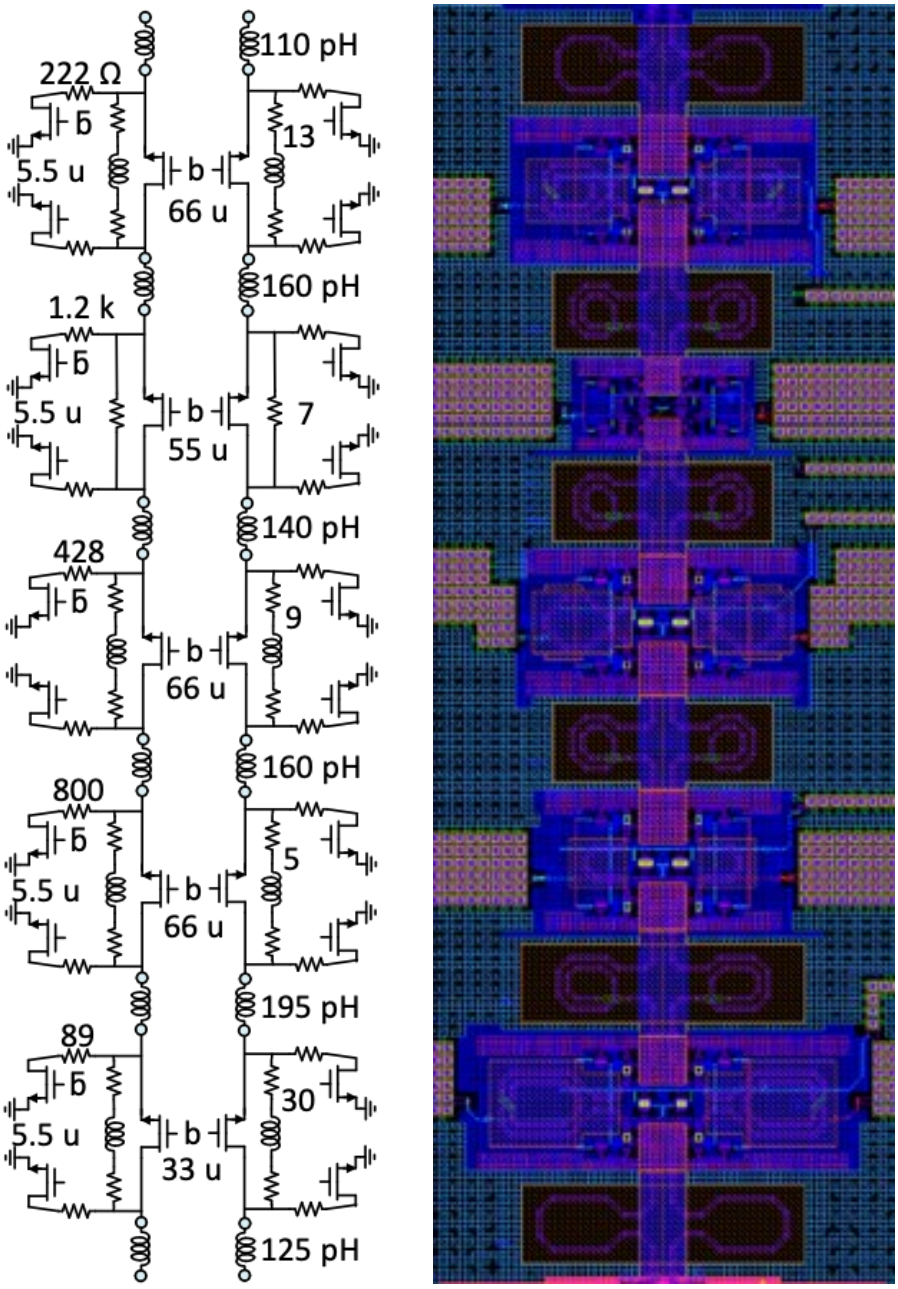

Figure 2.8: Attenuators diagram, schematic, and layout.

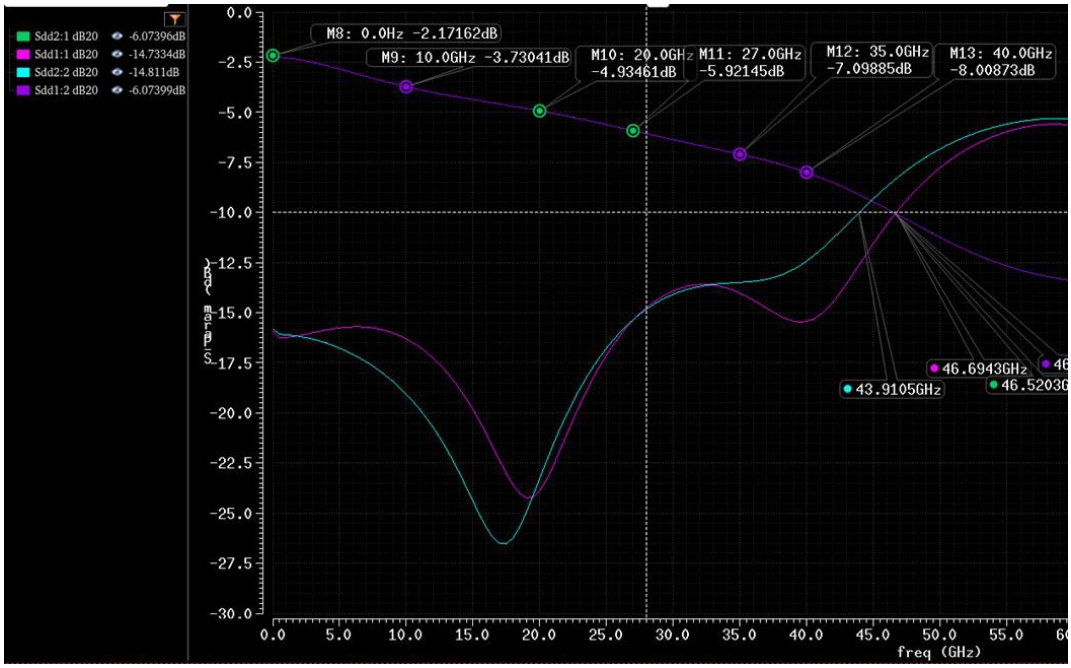

Figure 2.9: Simulation results of the attenuators.

It should be noted that applying attenuation increases the beamformer noise figure. This cost can be mitigated if the gain control is done by an active stage with gain. This is a tradeoff between linearity and noise figure. Based on equations in (6,7,8),

$$F_t \approx F_{LNA} + \frac{\{F_{GA} - 0.2\}}{0.28}$$

$$L_{att,15.5dB} \approx 4 * 35 \qquad (10)$$

$$F_t \approx 7.5 = 8.8\ dB$$

$$IP_{-1dB,BF} \approx IP_{-1dB,LNA}$$

2.6 Channel Integration

All previous blocks were integrated into a single channel, beamformer, as shown in the block diagram in Figure (2-1). Its overall simulation is shown in Figure (2-10). The chip and test board are shown in Figure (2-11). The non-RF pads are wire-bonded and have decoupling capacitors and ESD protection.

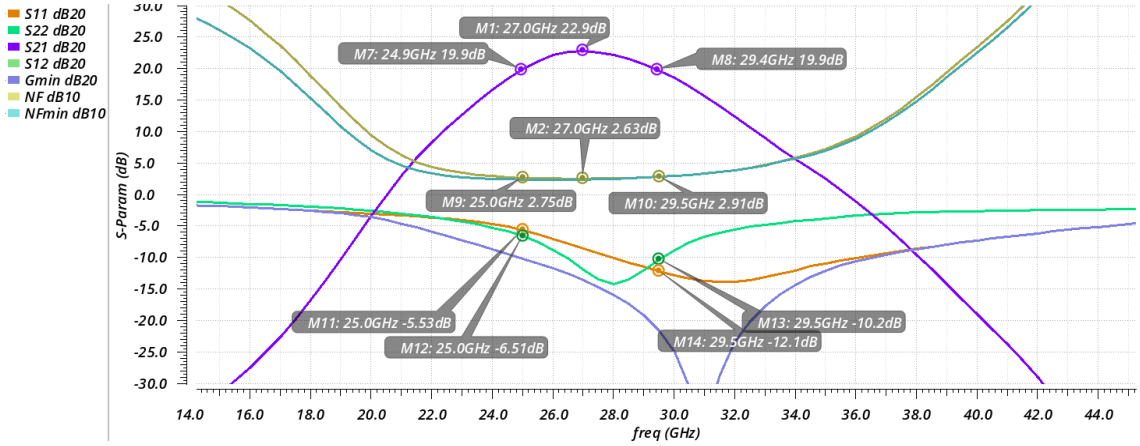

Figure 2.10: Simulation results of the receive beamformer for typical biasing (state 6), VDD = 1 V , Vsw = 0.8 V, and Pdc = 55 mW.

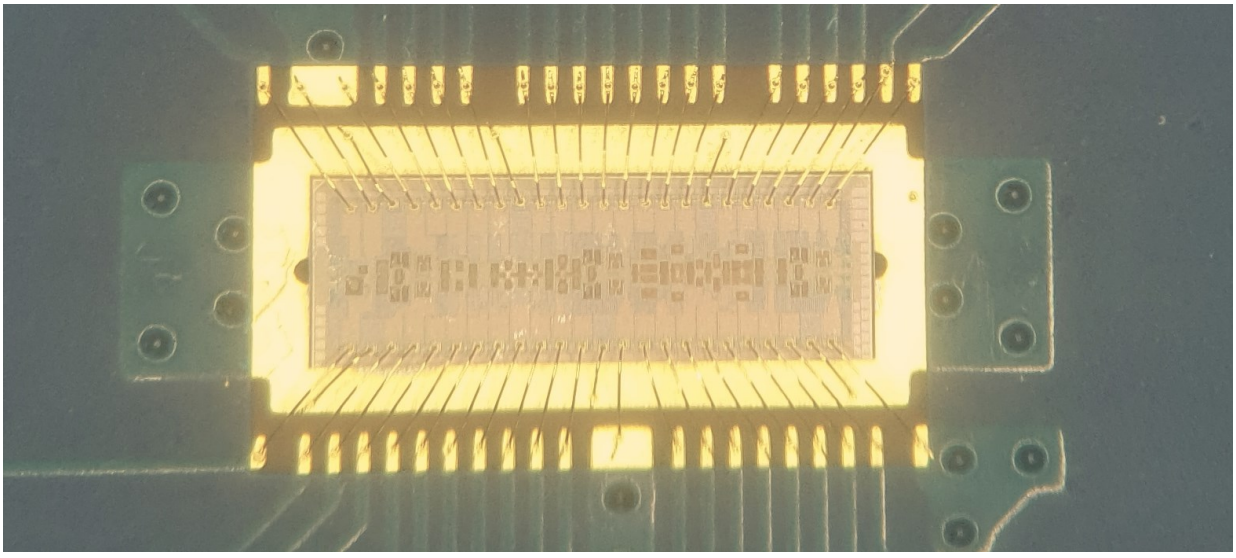

Figure 2.11: The beamformer chip and test board. Total receive beamformer area, which includes the decoupling capacitors and the pads, is 3750x1220 (µmxµm).

2.7 Architecture Measurements

The receive beamformer measurements are divided to test the biasing, attenuation, and phase shifting in separate tests. After that, all the 2048 states were measured. The tests were in the following subsections.

2.7.1 Receive Beamformer Specs Versus Different Biasing States, at First State of the Attenuation and Phase Shifting:

Each stage is supplied and biased, typically, by 1.05 V. The switches' ON-OFF voltages are 0.95-0 V. The biasing is controlled to change the power dissipation and gain of the beamformer as needed. Table (2-1) shows the selected biasing state that is tested. Figure (2-12) shows the S parameters of states 2, 6, 10, 15, and 19.

Table 2-1: Biasing states used for measurements. Note that the switch voltage is 0.95 V. I1 represents the first-stage current. Pt and It are the total power and current. The values of NF and IP-1dB are the values at 27 GHz.

#	Pt	Vdd	It	J	I1	Gmx	IP-1dB	NF
-	mW	V	mA	mA/μm	mA	dB	dBm	dB
1	35	0.85	39	0.2;0.1	10	10.5	-17.8	3.79
2	43	1.05	39	0.2;0.1	10	11.9	-17.9	3.25
3	51	1.25	39	0.2;0.1	10	12.2	-17.7	3.25
4	59	1.45	40	0.2;0.1	10	12.4	-17.7	2.96
5	49	0.85	53	0.26;0.14	13	12.6	-20.1	3.37
6	59	1.05	53	0.26;0.14	13	14.3	-17.6	3.27

Table 2-1: Biasing states used for measurements. Note that the switch voltage is 0.95 V. I1 represents the first-stage current. Pt and It are the total power and current. The values of NF and IP-1dB are the values at 27 GHz. (Continued)

#	Pt	Vdd	It	J	I1	Gmx	IP-1dB	NF
-	mW	V	mA	mA/μm	mA	dB	dBm	dB
7	71	1.25	54	0.26;0.14	13	14.8	-16.6	3.13
8	82	1.45	54	0.26;0.14	13	15.1	-16.2	3.22
9	64	0.95	63	0.3;0.16	15	14.0	-20.7	2.84
10	71	1.05	63	0.3;0.16	15	15.2	-19.3	2.64
11	83	1.25	63	0.3;0.16	15	16.1	-17.0	2.79
12	96	1.45	63	0.3;0.16	15	16.4	-16.3	2.58
13	103	1.20	80	0.4;0.2	20	16.2	-19.9	2.78
14	119	1.40	80	0.4;0.2	20	17.3	-17.2	3.04
15	135	1.60	80	0.4;0.2	20	17.7	-15.9	3.01
16	58	1.00	54	0.2;0.15	10	14.4	-18.6	2.99
17	81	1.40	55	0.2;0.15	10	15.4	-16.2	3.07
18	116	1.30	84	0.3;0.23	15	16.6	-20.7	2.53
19	144	1.60	86	0.3;0.23	15	18.1	-16.6	2.98
20	180	1.60	106	0.4;0.3	20	17.8	-20.4	2.66
21	170	1.60	100	0.3;0.3	15	17.6	-20.2	2.58

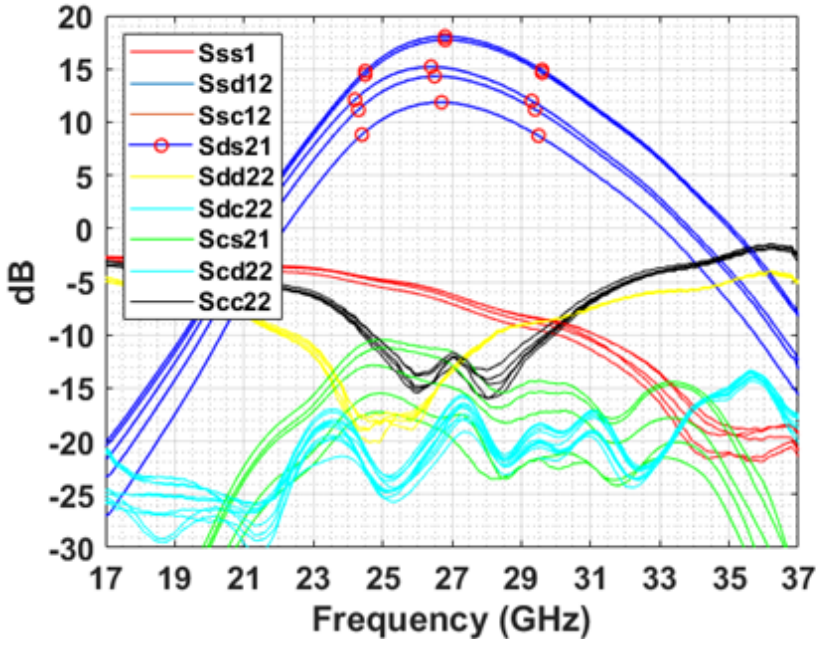

Figure 2.12: Measured single-differential S parameters for 2, 6, 10, 15, and 19 biasing state as in Table (2-1). Sds21: S parameter from differential port number 2 to single ended port number 1.

The sixth state is the typical state. The rest of the states can be used for different modes of operation. It can be used to have higher linearity or gain. Figure (2-12) shows that the highest gain is at state 19, where the current density increased. That current density approaches perfect utilization of the transistor's transconductance, as can be seen in [8].

The IP-1dB and NF are shown in Figure (2-13,14). They were measured in an uncalibrated setup and at single output port. Then, based on the measured "thrus" between the three ports of the PNA, the loss between the pads and the PNA was calculated, S21. Then, it was removed using:

$$F_t \approx S_{21,PNA-PAD} + F_{Chip(SE-SE)} + \frac{S_{21,PAD-PNA} - 1}{G_{chip(SE-SE)}} \tag{11}$$

$$IP_{-1dB,t} \approx IP_{-1dB,Chip(SE-SE)} + S_{21,PNA-PAD}$$

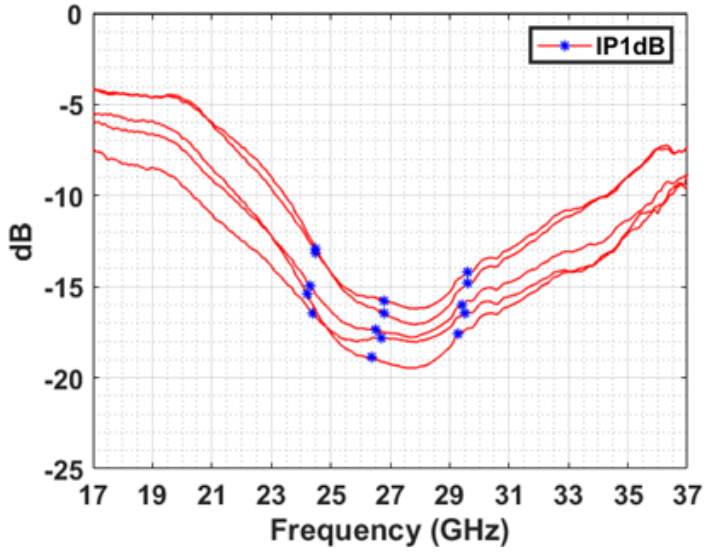

Figure 2.13: Measured IP-1dB for 2, 6, 10, 15, and 19 biasing states as in Table (2-1).

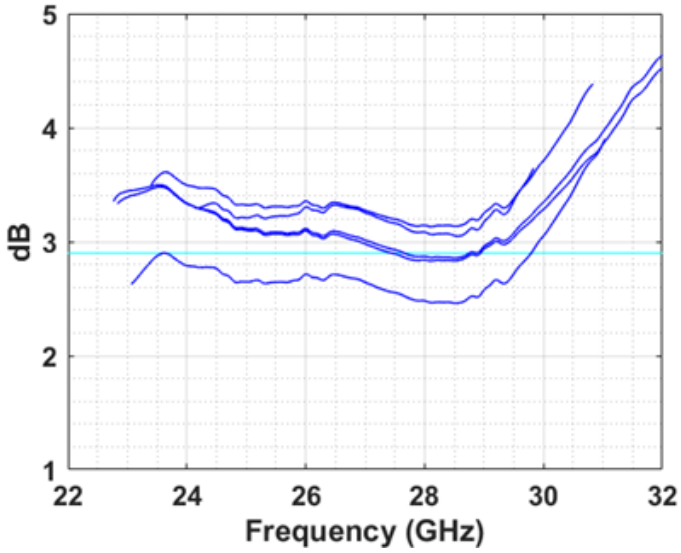

Figure 2.14: Measured SE-SE noise figure is for 2, 6, 10, 15, and 19 biasing states, as in Table (2-1). The mean values are more accurate as shown in phase states measurements.

As in Table (2-1), the typical power dissipation can be reduced to 40 mW. However, every other spec of the design is adversely affected since MOSFETs' current density dictates a design's specification. The voltage supplies can be used to reduce the total power, within the devices'

saturation/reliability range. For example, the high current density mode requires a larger supply voltage to ensure that all transistors are saturated. Figure (2-15,16) plots the gain, 1 dB power compression, and noise figure versus total power dissipation based on Table (2-1).

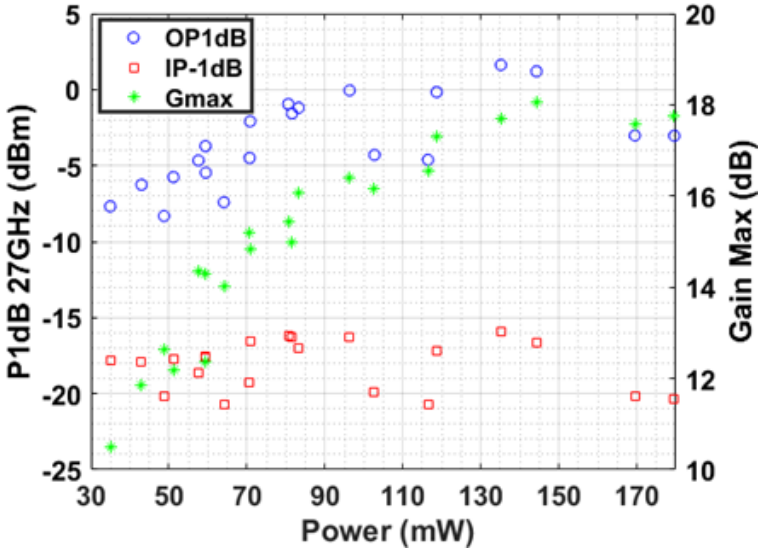

Figure 2.15: 1 dB power compression and gain versus power of all biasing states measurements.

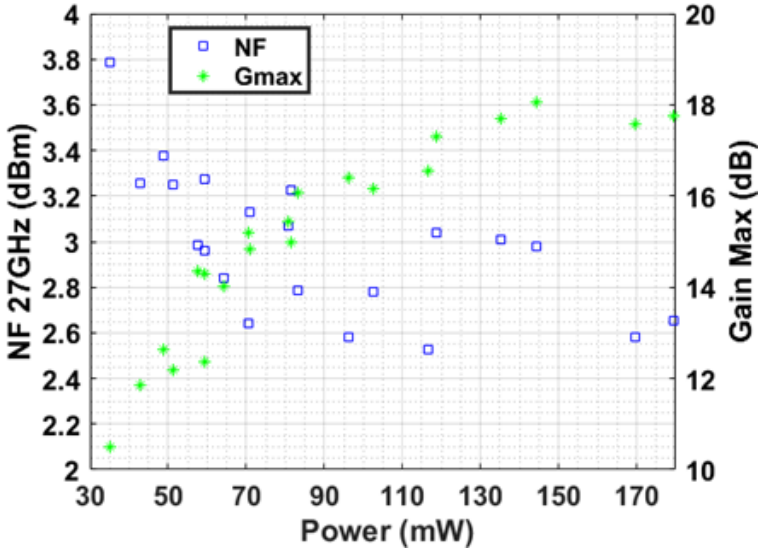

Figure 2.16: Noise figure versus power of all biasing states measurements. Accuracy is within 0.4 dB. More accurate measurements can be seen in phase shift states.

2.7.2 Beamformer Phase Shifts States at Typical Biasing State and no Attenuation:

Under state 6 in table (2-1), the phase shifts were applied. The switches 'voltages are 0.95 V or 0 V. Figure (2-17) shows the phase states polar distribution at 25, 27, and 29 GHz. Figure (2-18) shows the gain/phase errors as standard deviations across frequency for phase shifters without attenuation. Figure (2-19,20) shows the IP-1dB and NF.

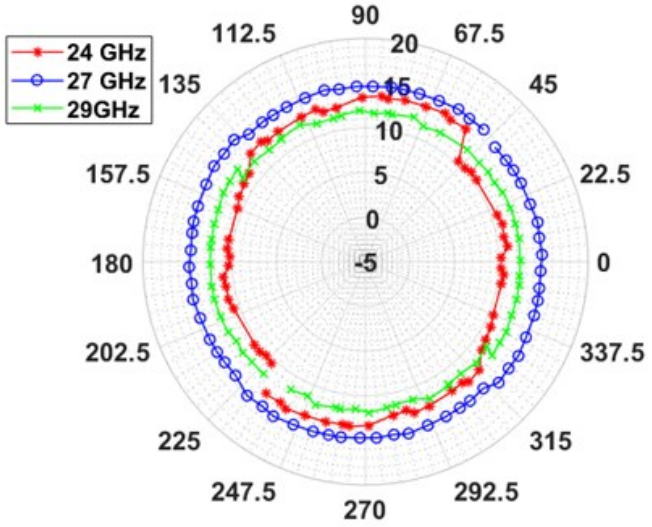

Figure 2.17: Polar plots of measured Sds21 (dB, Deg) for phase shifter states.

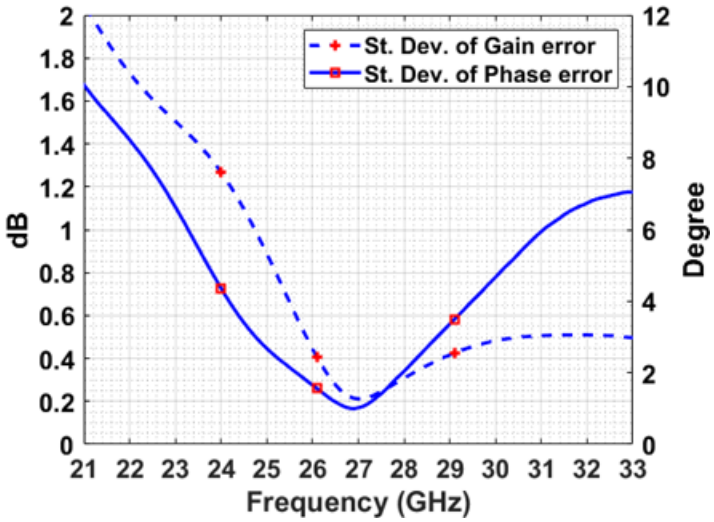

Figure 2.18: Standard deviation of measured gain/phase error for phase shifters states only.

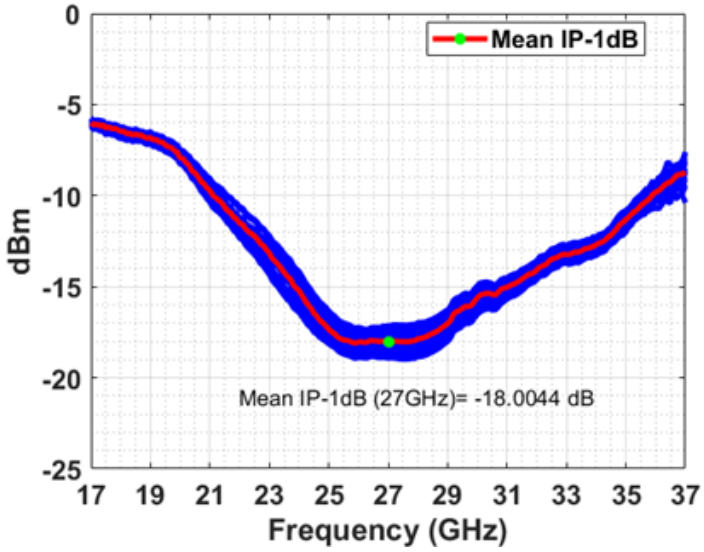

Figure 2.19: Measured IP -1dB for all phase shifters states.

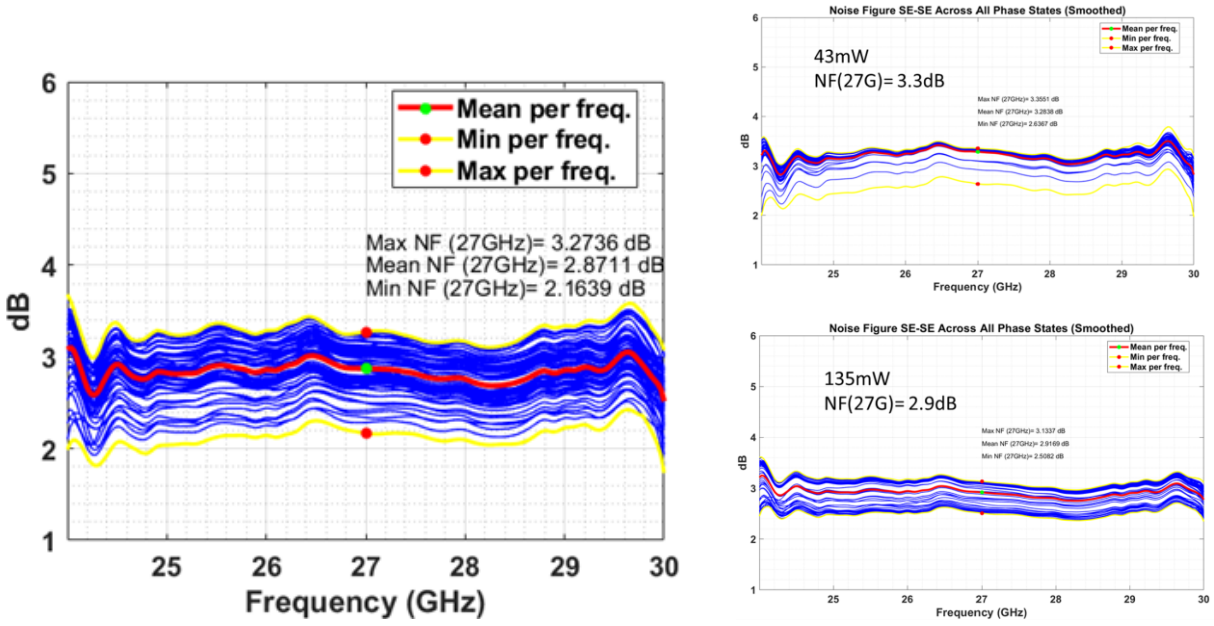

Figure 2.20: Measured noise figure SE-SE across all phase shifters states (smoothed). Right plots are for other biasing states.

2.7.3 Receive Beamformer Attenuation States at Typical Biasing State and First Phase Shifting State:

Under state 6 in Table (2-1), the attenuations were applied with switches' voltages of 0.95 V or 0 V. Figure (2-21) shows S21 of the channel across all states. In Figure (2-22), the phase/gain errors standard deviation for the attenuators, at first phase shift state, are plotted versus the frequency. The IP-1dB and NF are shown in Figure (2-23).

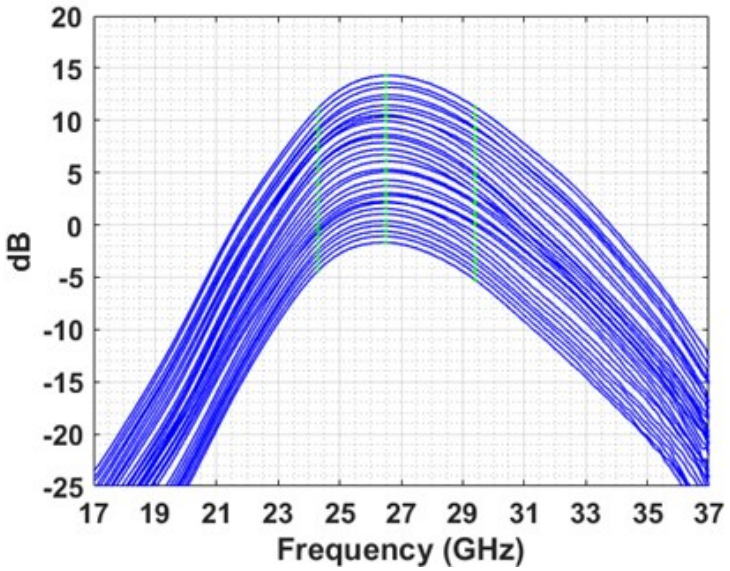

Figure 2.21: Measured gain of all attenuation states (Sds21).

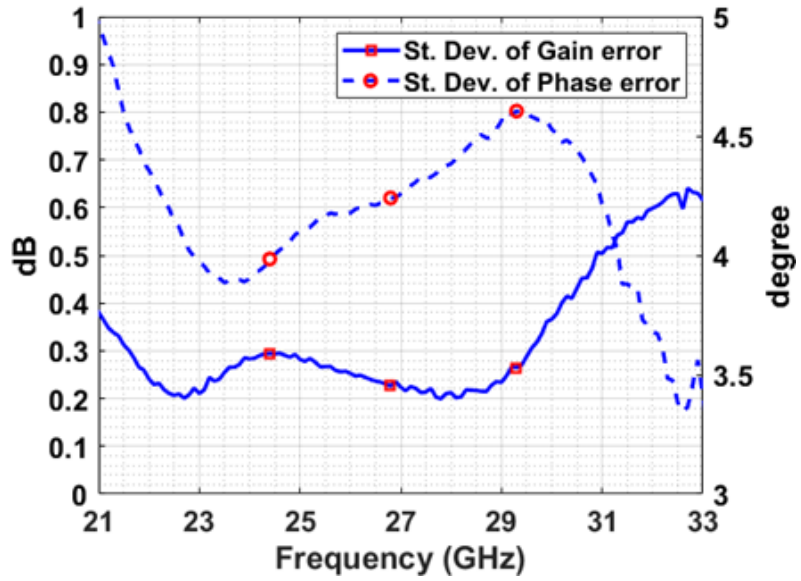

Figure 2.22: Standard deviation of measured gain/phase error for attenuation states only.

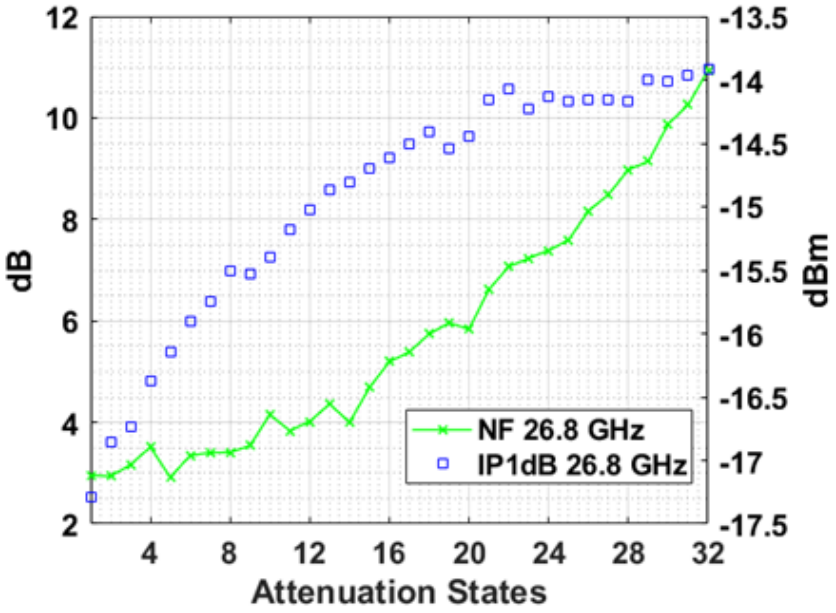

Figure 2.23: Standard deviation of measured gain/phase error for attenuation states only.

2.7.4 Measuring All States of the Receive Beamformer at High Power State of Biasing:

Under state 15 in Table (2-1), a small signal measurement for all states, 2048 states, was done with switches' voltages of either 0.95 or 0 V. The polar plots are shown in Figure (2-24,25). Figure (2-26,27) shows the standard deviation of phase/gain errors across all gain/phase states.

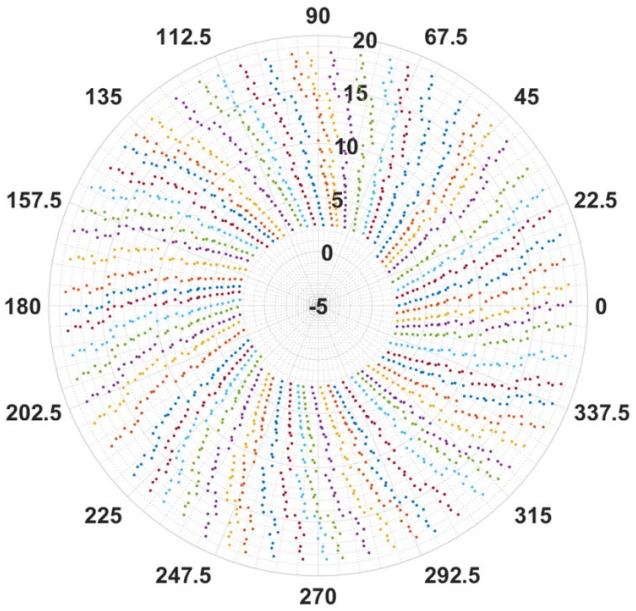

Figure 2.24: Polar plots of measured Sds21 (dB, Deg) at 27 GHz for all states.

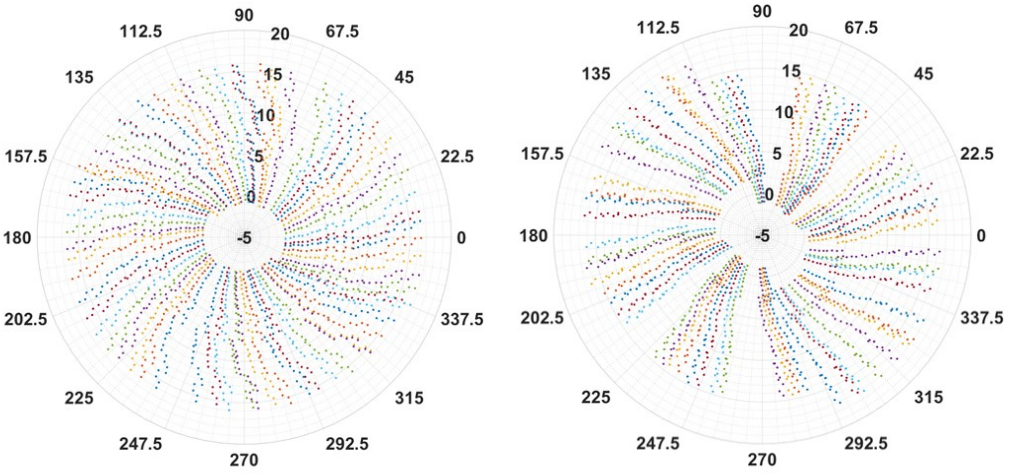

Figure 2.25: Polar plots of measured Sds21 (dB, Deg) at 29 GHz and 24.5 GHz for all states.

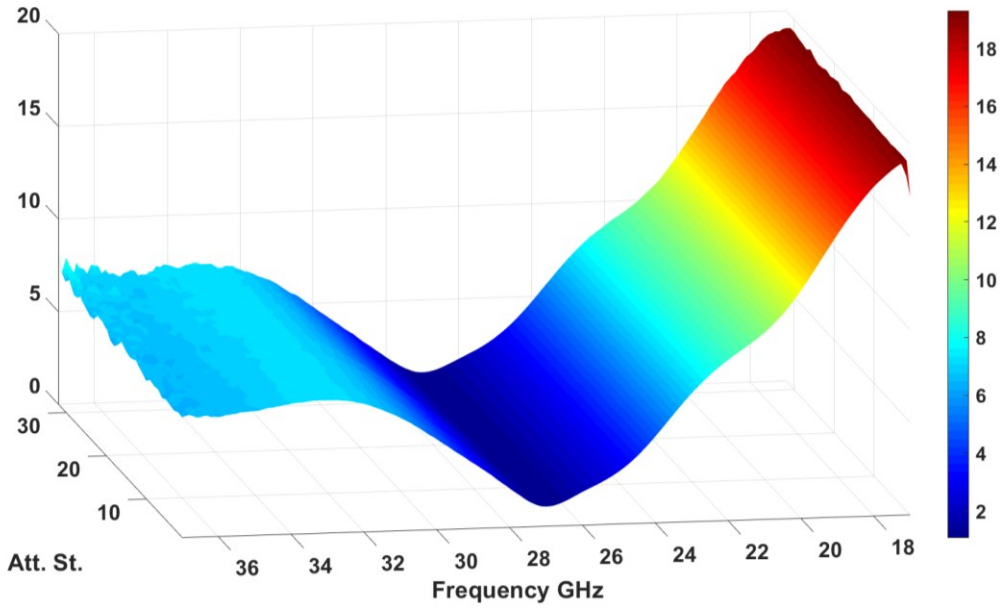

Figure 2.26: Standard deviation of measured phase error versus frequency and attenuation states.

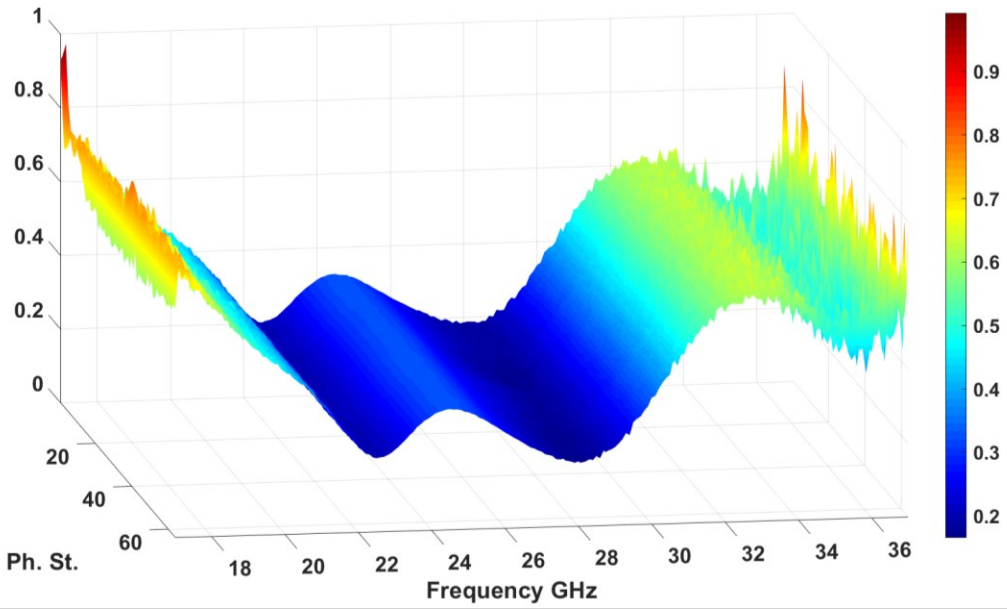

Figure 2.27: Standard deviation of measured gain error versus frequency and phase states.

2.8 Blocks Performance Estimation

Since the typical biasing state is state 6 in Table (2-1), the performance of each block was estimated based on the measured data of G, NF, and OP-1dB. Table (2-2) shows the estimation results (at 27 GHz) and compares them with simulation results, assuming equal specs of GA and minimum change of noise figure and gain from simulation. To check for the accuracy of the estimation, the attenuators were used to provide the NF/OP-1dB as close as possible to measurements. Note that the attenuation steps were preserved but not the absolute values, as shown in Figure (2-28).

In Figure (2-29), the OP-1dB and IP-1dB across attenuation states were plotted. Here, the IP-1dB was not actually solved in the estimation. The gain, calibrated small signal S_{ds21}, was used to find the IP-1dB. Therefore, it is apparent from IP-1dB that there is a mismatch between the gain in the calibrated and uncalibrated setups, for small signal S parameters and for P-1dB, respectively.

Table 2-2: Estimated components specifications.

	LNA	Att.	GA	Ph.S.	GA	Total
Gain Est. (dB)	18.9	-6.5	4.17	-6.5	4.17	14.2
Gain Sim. (dB)	21	-6	6.8	-6.5	6.8	22.1
NF Est. (dB)	2.3	6.5	2.4	6.5	2.4	2.9
NF Sim. (dB)	2.4	-	3.5	-	3.5	2.7
OP-1dB Est. (dBm)	4.7	~6	4.2	~5	4.2	-3.6
OP-1dB Sim. (dBm)	1.3	-	2.1	-	2.1	-2.5

Using the estimated specs in Table (2-2) and the preserved attenuation steps, Figure (2-23) shows the measured NF and estimated performance. Generally, noise measurements are averaged and smoothed, and they take longer time than other measurements. However, the measured NF/OP-1dB shapes and the mean NF from Figure (2-20) were used to predict all blocks.

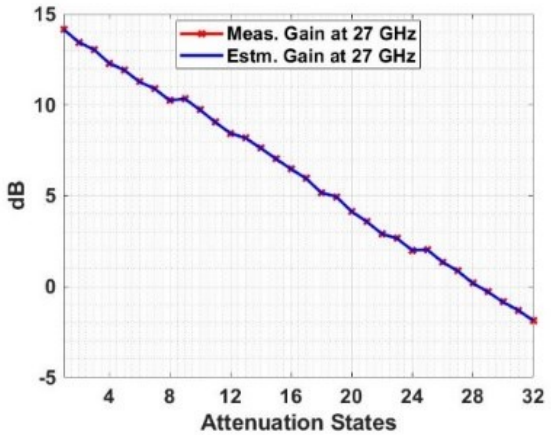

Figure 2.28: Measured and estimated gain with preserving attenuation steps at 27 GHz.

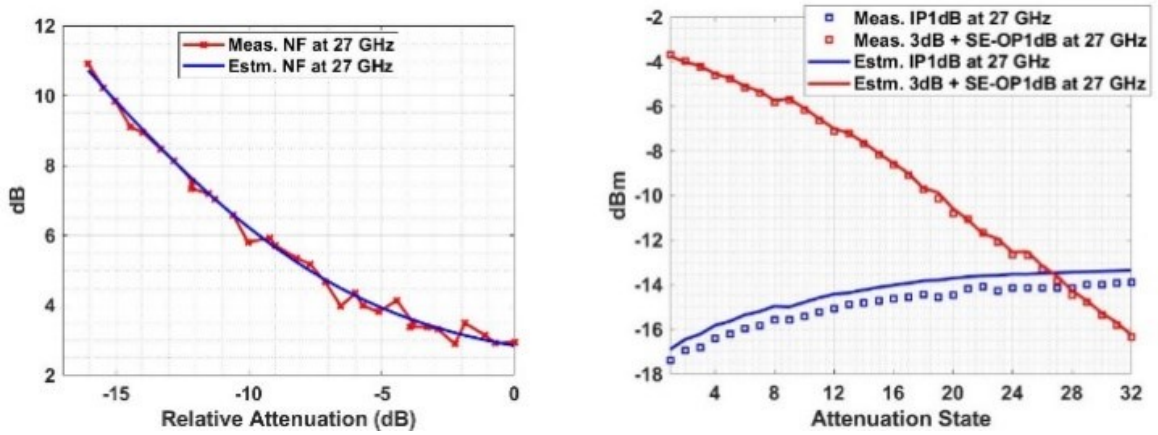

Figure 2.29: Measured and estimated 1dB compression powers at 27 GHz across attenuation states.

2.9 Acknowledgements

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Chapter 2, in full, is currently being prepared for submission for publication as it may appear as: Sultan A. Alqarni and Gabriel M. Rebeiz, " Ka-Band Receive RF-Beamformer Using Passive Phase Shifters and Attenuators on 22FD-SOI Technology" in IEEE. The dissertation author was the primary researcher and author of this material.

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Chapter 3 Ka Band Transmitter Channel on 22 nm Technology with Passive Phase Shifters and Attenuators

An implementation of Ka band transmit beamformer on Global Foundry's FD-SOI 22 nm technology is presented. The design architecture is in section 2. The power amplifiers are shown in section 3. The phase shifters and attenuators are the same as in chapter 2. Then, section 3 shows the channel measurements result.

3.1 Transmitter Channel Architecture

Figure (3-1) shows the diagram of the design along with its layout. The high output power requires the front-end power amplifiers' total gain to be high enough to reduce the power level at the phase shifters and the attenuators. Therefore, the power amplifier consists of three stages: a two-stage power amplifier and an extra-gain stage.

The gain amplifier, located before the attenuators and before the phase shifters, is used to overcome their losses, cancel the common mode signal, provide matching, and provide isolation. Also, its output power is high enough to minimally affect the compression and efficiency of the channel, or beamformer. The phase shifters' and attenuators' power levels at their inputs are less than -6 dBm at maximum linear output power. The values on the block diagram in Figure (3-1) are the simulation values at 28 GHz.

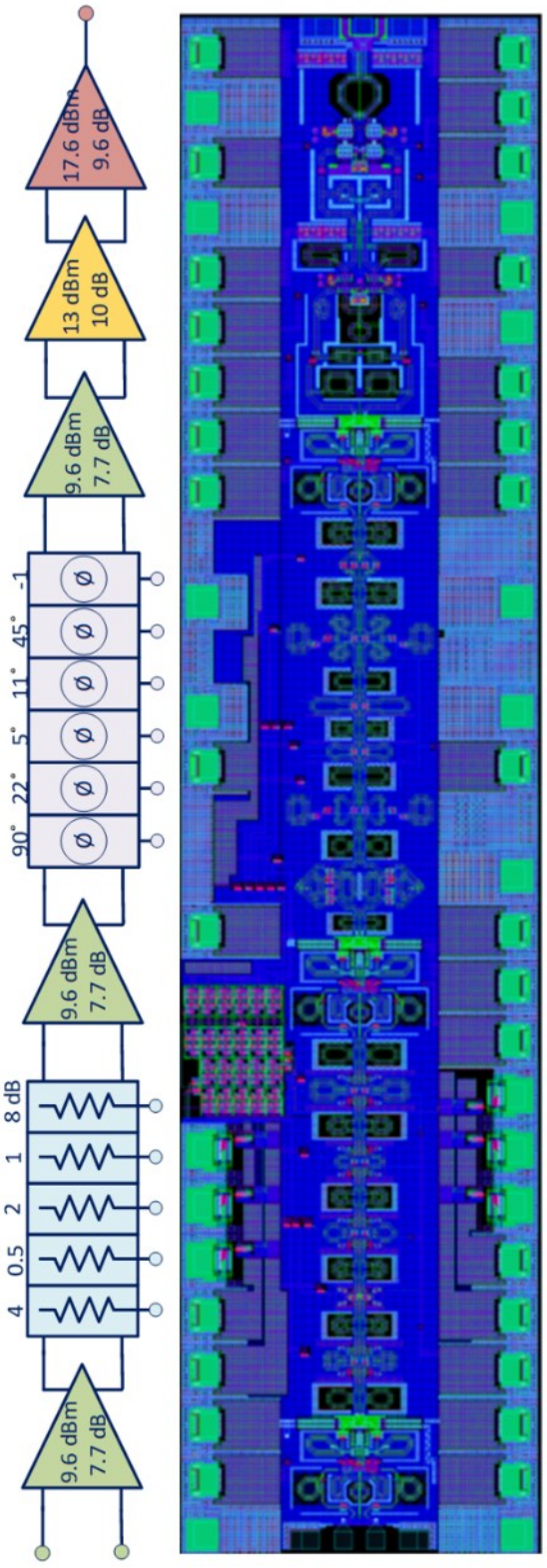

Figure 3.1: Block diagram of the transmit phased array and its layout.

3.2 Power Amplifiers

In Figure (3-1), the front-end power amplifier consists of three stages. The last two stages are shown in Figure (3-2), and the first is shown in Figure (3-3). The first stage is also the gain amplifier used before the attenuators and the phase shifters.

All stages are biased in class AB range. The last stage is closer to class B for efficiency. The first stage is closer to class A to provide more gain with its other specs. The 18 dBm, 13 dBm, and 10 dBm stages are biased at 0.04 mA/μm, 0.063 mA/μm, and 0.135 mA/μm, respectively. The transistors' widths are selected to provide the required current per stage while the maximum voltage is 0.8 V per transistor. The voltage dividers were used to implement the biasing. Their resistances are in the order of 1 kΩ to ensure fast response time.

The amplifier stages are matched to 50 Ω, single-ended, except for the last stage output. The matching networks are designed to provide the cascodes output/input with an optimized impedance after an iterative process of load-pull and source-pull. While the impedance scales down when the gates are scaled up, it is necessary to repeat the process after electromagnetic extraction or RCC extraction; the EMX tool was used in the last stage gates, and the Caliber tool was used for the other gates. For the last two stages, the common gate capacitance was optimized to provide high linearity specs along with the neutralizing capacitors around the differential pair; the optimization is within stable range of operation and under-neutralization range.

All the power amplifiers have source inductance at the differential pair's gates. For the last stage, it is a parasitic inductance. It is necessary for the 10 dBm stage since matching to 100 Ω, differentially, is required for the phase shifters and the attenuators.

The 10 dBm and 13 dBm power amplifiers contain common mode rejection inductors. It is useful in the 10 dBm since it is used three times in the channel. The 13 dBm matching network at the

input was modified for the common mode rejection function over frequency. The last stage has no common mode rejection since the common mode signal was already rejected by a significant amount, and it is loaded with balun. The layout is shown in Figure (3-4,5).

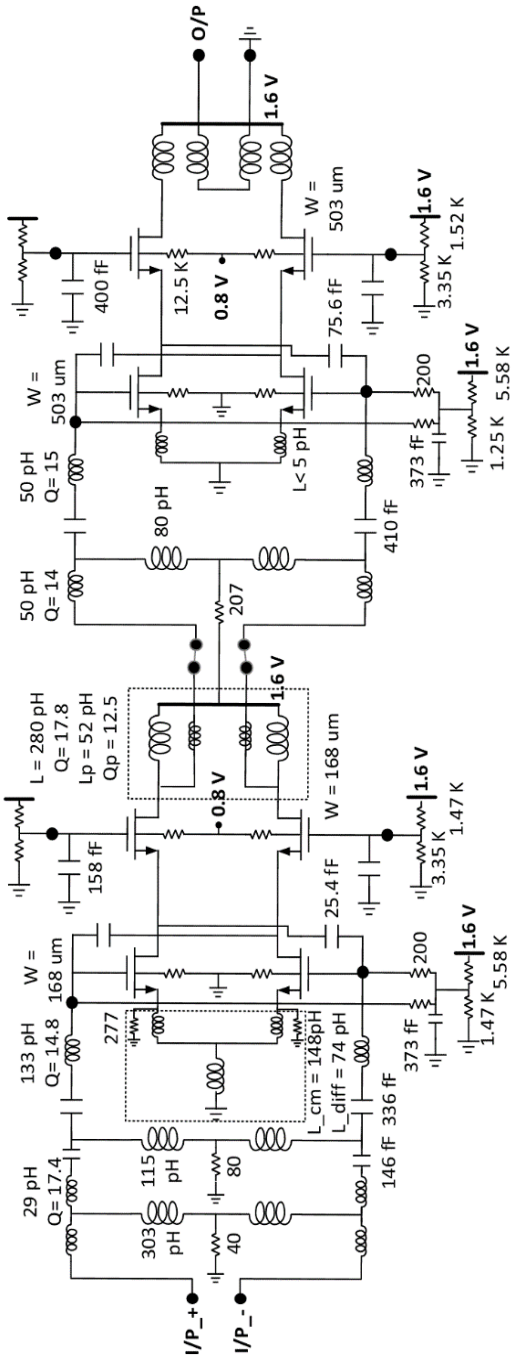

Figure 3.2: Schematic design of the last two stages of the power amplifier (18 dBm and 13 dBm).

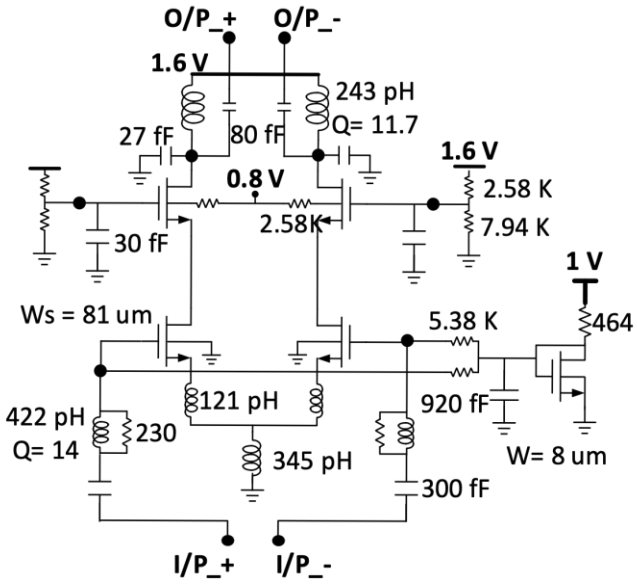

Figure 3.3: Gain stage amplifier schematic. It is the first stage of the power amplifier (10 dBm).

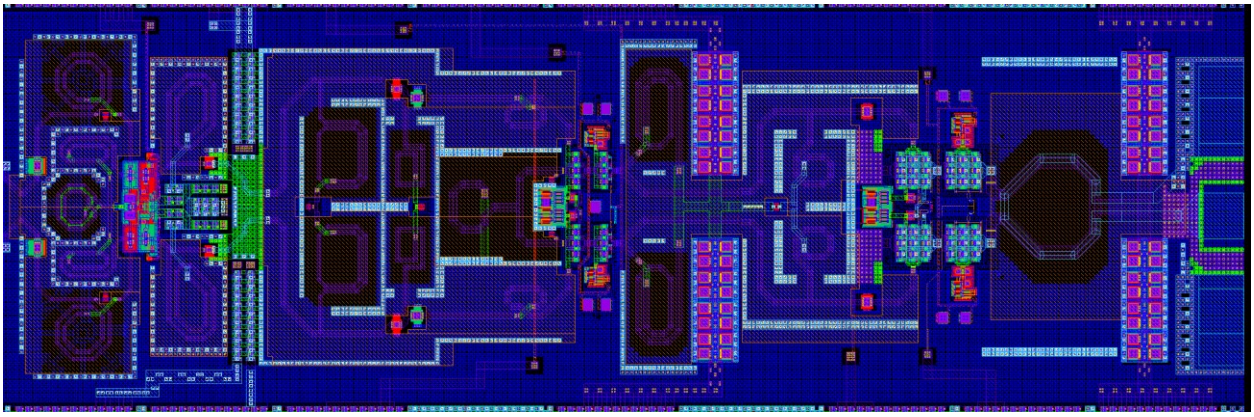

Figure 3.4: Layout of the last three stages of the transmitter.

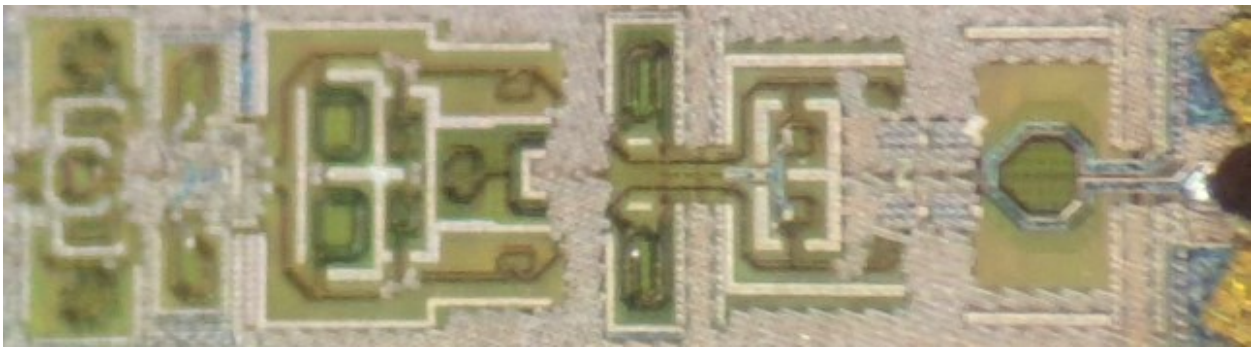

Figure 3.5: Picture of the fabricated power amplifiers in Figure (3-4).

Table 3-1: Simulated OP-1dB and OP-3dB of the last three stages of the transmitter channel.

Output Referred 1dB Compression ...

	fo	Output Referred 1dB Compression Points (dBm)	Output Referred 3dB Compression Points (dBm)
1	23.00E9	16.76	17.88
2	24.00E9	15.76	18.43
3	25.00E9	16.19	18.51
4	26.00E9	16.86	18.67
5	27.00E9	17.29	18.83
6	28.00E9	17.30	18.84
7	29.00E9	17.09	18.76
8	30.00E9	16.92	18.67

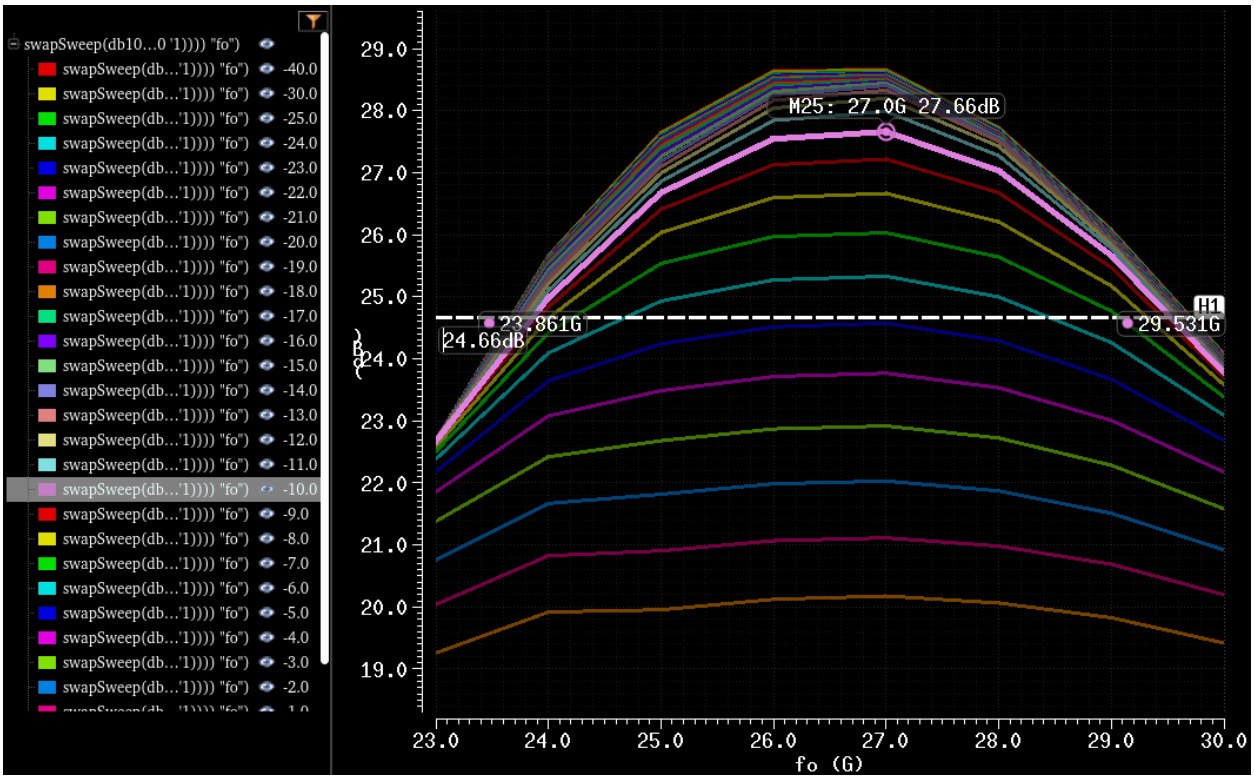

Figure 3.6: Large signal simulation results of the three stages power amplifier.

3.3 Channel Measurement

The channel components were integrated, as shown in Figure (3-1), with a control unit to control the phase shifters and attenuators. The simulation results are shown in Figure (3-7).

Decoupling capacitors were added at the dc pads along with ESD cells. Figure (3-8) shows the fabricated chip and test board.

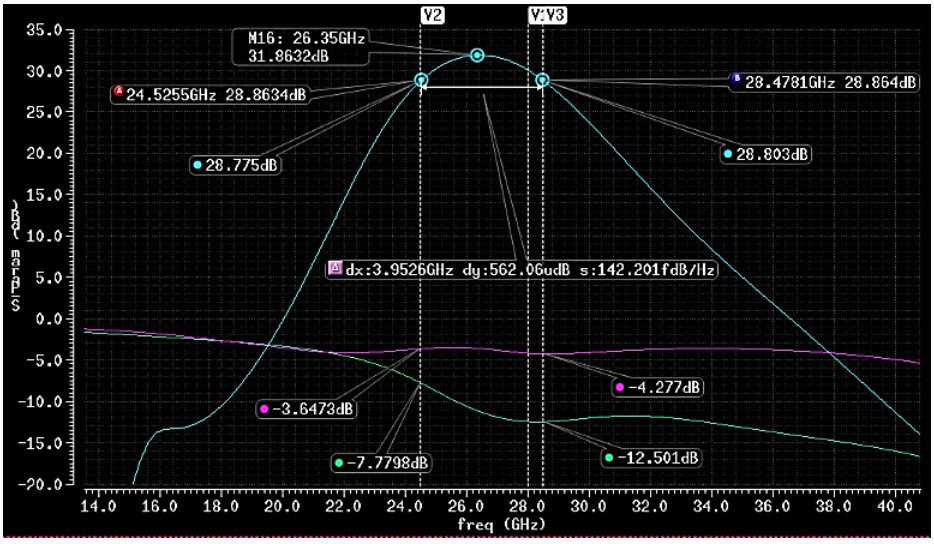

Figure 3.7: Simulation result of the transmitter channel.

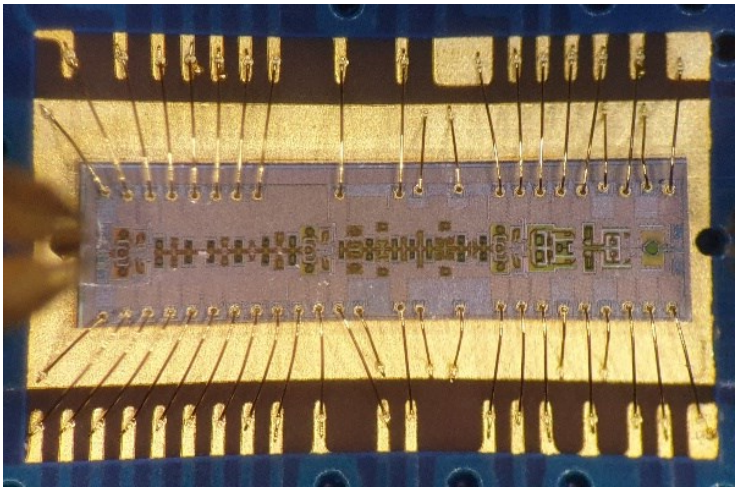

Figure 3.8: The used test board in measurements. Total transmit beamformer area, which includes the decoupling capacitors and the pads, is 4195x980 (µmxµm).

The test board connects all supplies with similar voltage, based on the schematic shown in Figures (3-2,3). The performed measurements are done to test the beamformer's gain/phase states and analyze its power compression and efficiency in the next two subsections.

3.3.1 Attenuation and Phase Shift States

The channel was biased in typical conditions. The digital supply and the switches' ON-state voltage are 0.95 V. The attenuators' states are tested first. Figure (3-9) shows the single-ended to differential-ended S parameters for all the attenuation steps with applying smoothing within 1 GHz. The maximum gain measured is 26.9 dB at 24.5 GHz, and the bandwidth is 4.3 GHz. The standard deviation of the gain and phase errors for the attenuation states are shown in Figure (3-10). The minimum gain errors standard deviation is 0.13 dB at 25.2 GHz.

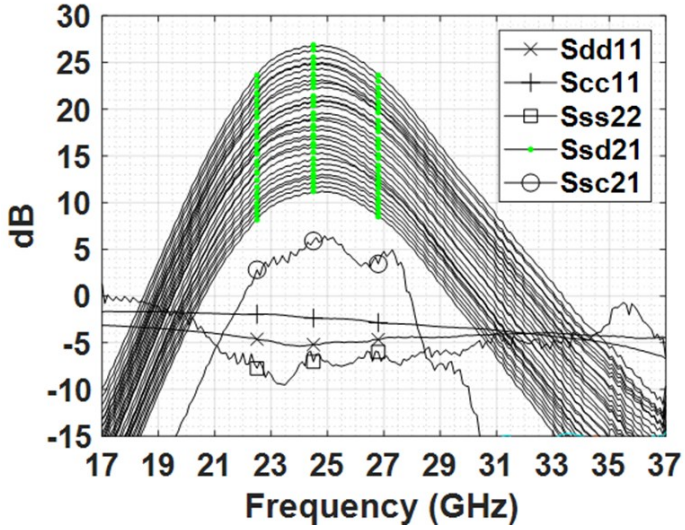

Figure 3.9: Measured single-differential ended S parameters. Only the gain, Ssd21, was plotted for all attenuation states.

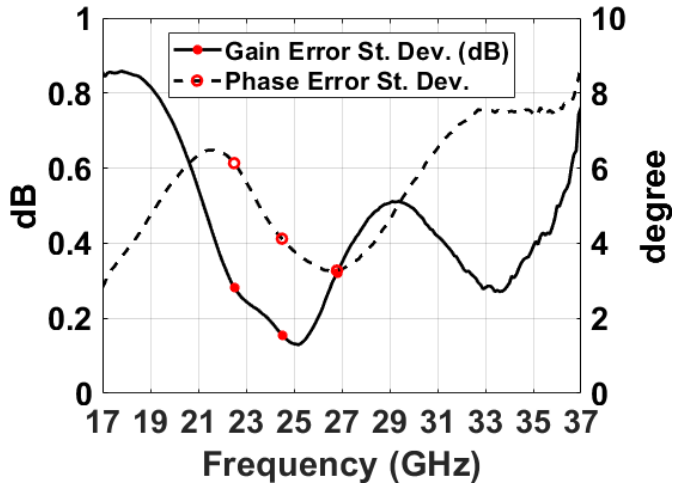

Figure 3.10: The standard deviation of measured gain/phase errors for the attenuation states.

Secondly, the passive phase shifters were tested. Figure (3-11) shows the phase error after removing the mean phase error at each frequency for all the phase shifting states. The standard deviation of the gain and phase errors for the phase shift states, at first attenuation state, are shown in Figure (3-12). The minimum phase errors standard deviation within the channel bandwidth is 2.1 degrees at 26.7 GHz.

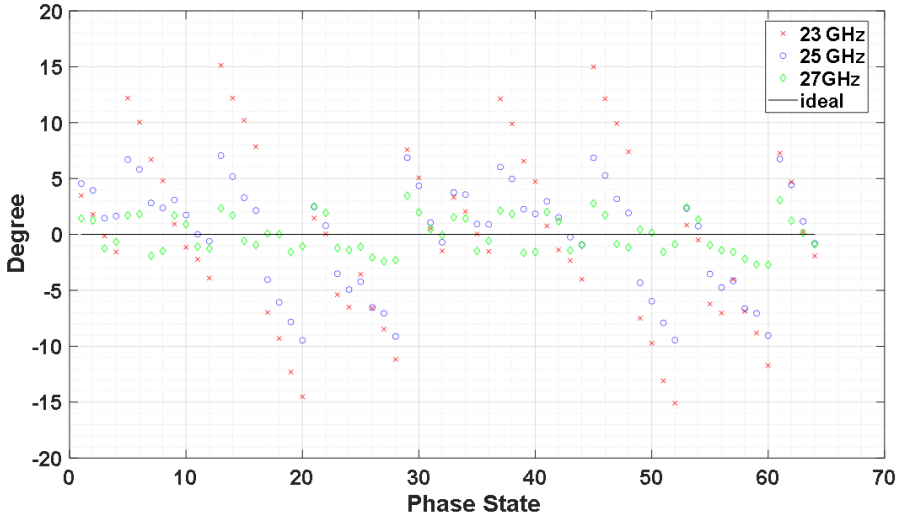

Figure 3.11: Measured phase errors across phase shift states. The mean error at each frequency was removed.

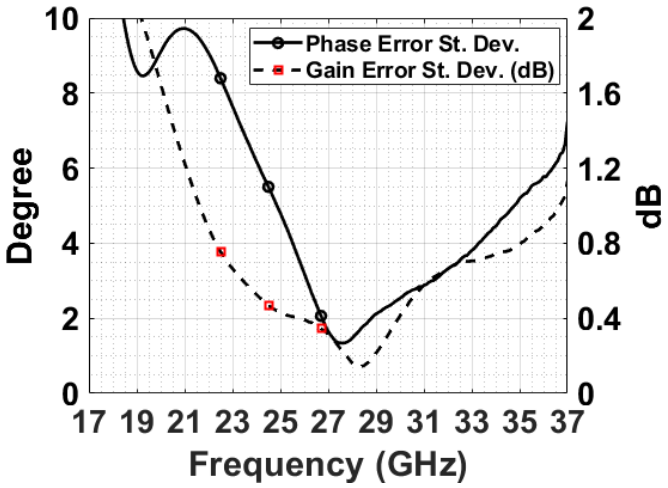

Figure 3.12: The standard deviation of measured gain/phase errors for the phase shift states.

3.3.2 Continuous Wave Power and Efficiency Measurements

The power analysis uses a continuous wave input signal at 25 GHz as a single frequency. The test is to determine the output power, the corresponding DC power consumption, and the gain as the input power varies linearly. The limits of the power linearity are defined when the gain compresses. The efficiency that is used is the drain-efficiency, which is nearly equal to the power-added efficiency due to the significant gain. The biasing conditions of the beamformer were similar to the previous tests, unless mentioned. The measurement uses two reference planes, which are:

- The gain reference plane is the probs tips on the chip pads. This was done using the calibration used in the previous measurements, small signal measurements of the attenuation and phase shifters states.
- The powers were measured using network analyzer receivers. After that, the estimated power losses from the network analyzer to the chip pads were removed. Figure (3.13) illustrates the "thru" measurements of the three ports that are used, and Figure (3.14) depicts the estimated loss at the output and input.
- The DC power consumption includes all the power supplied from the power supplies, specifically the "1.6 V" and "1 V" in the power amplifiers schematics.

Fig 3.15 presents the outcome of the power analysis at typical conditions. The blue dots are the records of the measurements, and the black lines represent the interpolated mean of the measurements. The OP-1dB is 15.5 dBm and the efficiency is 12.5 %. In addition, the OP-4dB is 18 dBm and efficiency is 18.6 %. The maximum measured compressed output power is 18.7 dBm with efficiency of 19.6 %.

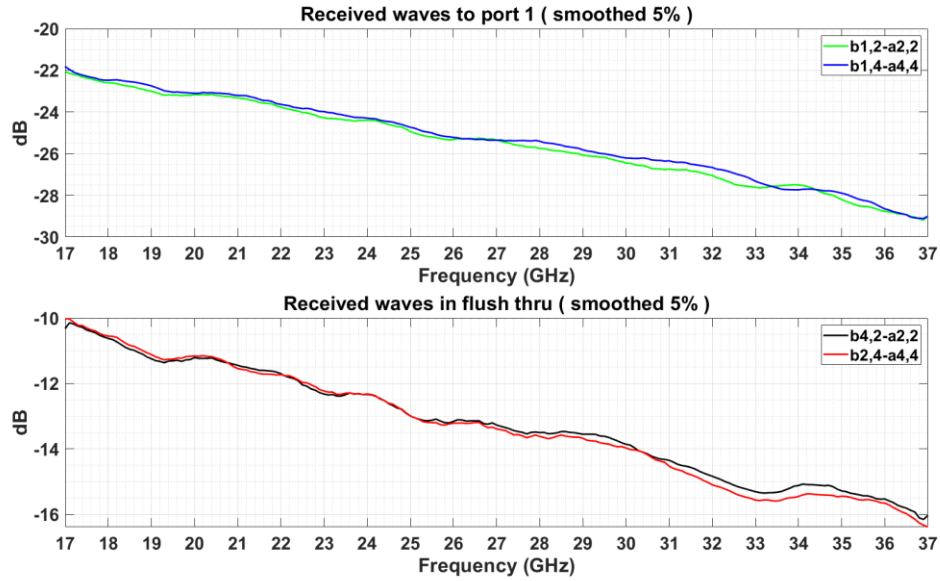

Figure 3.13: Measured “Thrus” between the three network analyzer ports. The symbol ax,y stands for transmitted, or received for b, wave from port’s source y and measured at port’s receiver x.

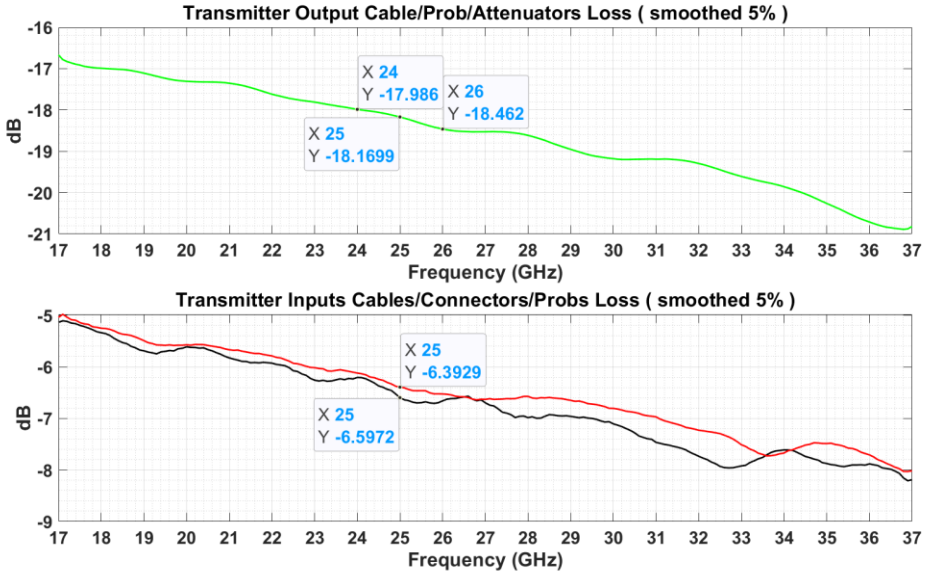

Figure 3.14: The estimated loss of the output and input cables.

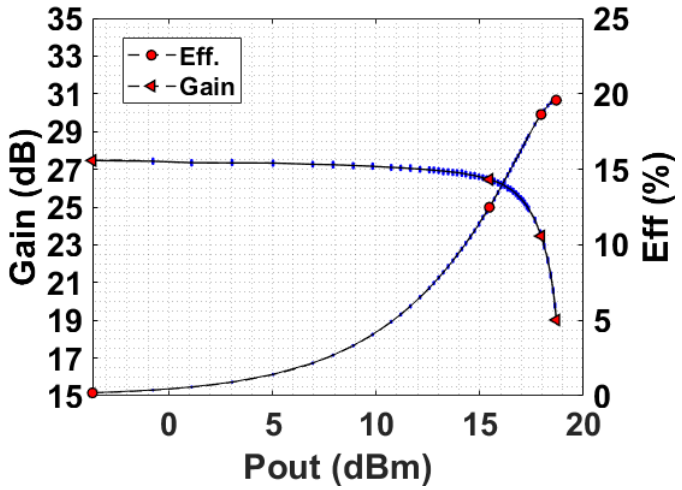

Figure 3.15: Measured gain compression and efficiency. The red markers marks are for the -1/-4 dB compression and min/max points. The blue markers represent the actual measurements.

The test was repeated by varying the "1.6 V" power supplies' voltages from 1.4 to 1.8 V, which includes the biasing as illustrated in figures (3-2,3). Figure (3-16) shows the gain, efficiency, and output power at 1 dB and 4 dB gain compression. The gain increases as the biasing moves the last two stages toward class A while the efficiency decreases. The amplifiers gain experience gain expansion at lower supply voltages, as shown in Figure (3-17). The gain expansion increases the values of the maximum linear power which also increases efficiency. Moreover, with higher supply voltages, the saturation power increases as can be seen from Figures (3-16,17).

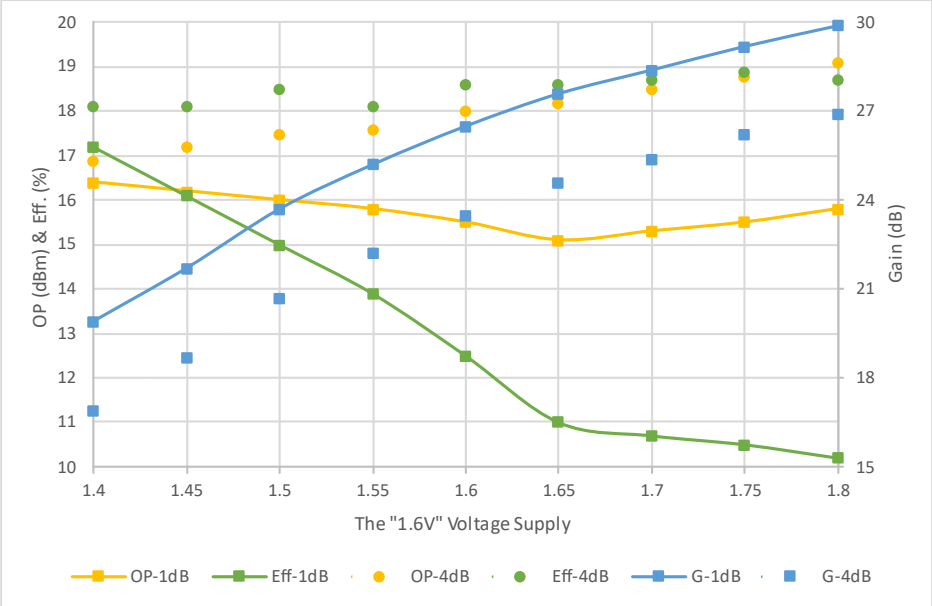

Figure 3.16: Power analysis measurement results for 1 dB and 4 dB compression when the biasing and cascodes with “1.6 V” supply voltages ware varied.

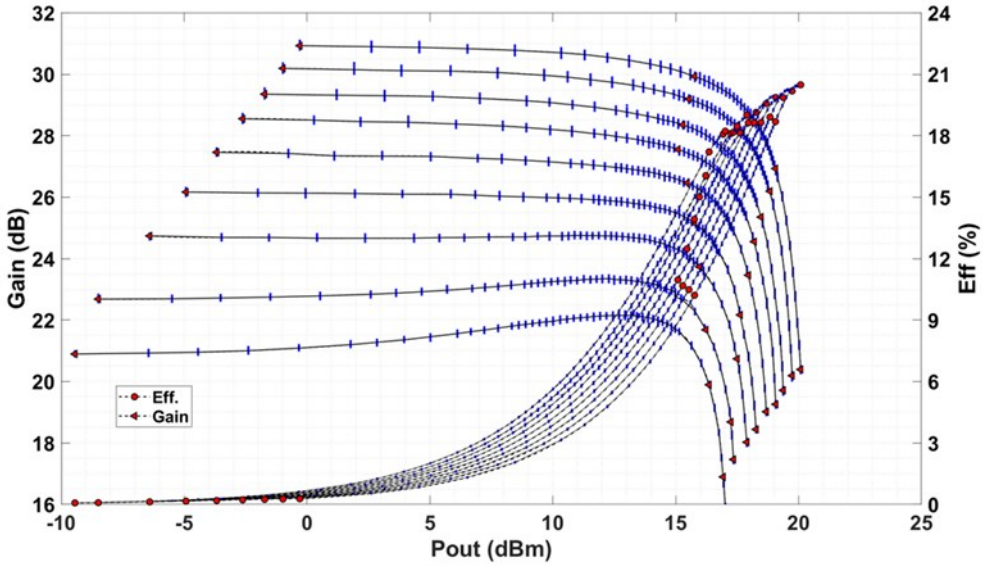

Figure 3.17: Power analysis measurements plots when [1.8:0.05:1.4] V was applied on supply ports named “1.6 V”. The highest voltage corresponds to the highest gain and lowest efficiency curve.

3.3.3 Modulated Signal EVM Measurements

The measurement setup is shown in Figure (3-18). The measurement aims to find the maximum output power that supports about 3 % of Error Vector Magnitude (EVM) for Quadrature Amplitude Modulation (QAM). The input from the signal generators is applied at one of the inputs while the other is connected to an RF cable to an open termination. This input configuration is supposed not to affect the overall measurements since the signal power level at the input has a much smaller power level than the IP-1dB of the first amplifiers. The channel rejects the common mode signal through the channel amplifiers and losses.

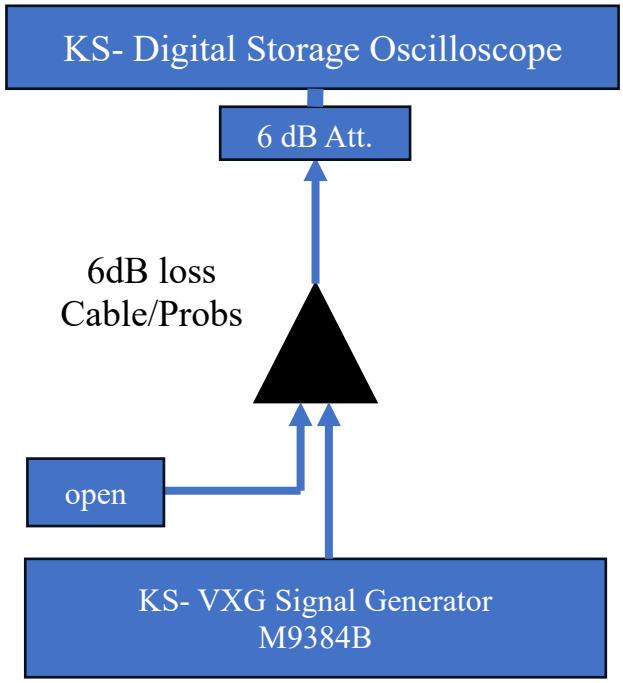

Figure 3.18: The EVM measurement configuration.

There are six tsts that are done for EVM measurements. The first three are under typical supply conditions but for different modulations: 64-QAM-100 MHz for 600 Mbps, 64-QAM-200 MHz for 1.2 Gbps, and 64-QAM-400 MHz for 2.4 Gbps. The last three are for 1.45, 1.6, and 1.75 V voltage supplies while the modulation is kept the same, 64-QAM-100 MHz. “Root Raised Cosine” is the selected measurement filter, with 0.35 as the “alfa.”

3.3.3.1 EVM Measurements Using 64-QAM-100/200/400 MHz Modulations at Typical Supply Conditions

Table (3-2) shows the measurement power sweep for 64-QAM-100 MHz modulation and its associated EVM. Figure (3-19) shows the EVM versus output power for all modulation, and Figures (3-20,21,22) show the bitmap of the Digital Storage Oscilloscope (DSO) at the nearest measurement to 3 % EVM. In Table (3-3), the results are summarized and compared with the efficiency from the continuous wave measurements.

Table 3-2: EVM Measurement sheet of the 64-QAM-100 MHz modulation.

*1	*2	*3	*4	*5		*6	*7	*8
Pin VXG (dBm)	Pin Chip (dBm)	Pout Chip (dBm)	Pout DSO (Hold) (dBm)	Pout DSO (Run) (dBm)	EVM (%)	G (dB)	G2 (dB)	G3 (dB)
-43	-49.5	-27.7	-39.7	-39.8	3.5	21.8	24.8	24.7
-40	-46.5	-24.7	-36.7	-36.8	2.5	21.8	24.8	24.7
-37	-43.5	-21.8	-33.8	-33.7	2	21.7	24.7	24.8
-34	-40.5	-19.8	-31.8	-31.7	1.5	20.7	23.7	23.8
-31	-37.5	-16.9	-28.9	-28.8	1.5	20.6	23.6	23.7
-28	-34.5	-13.6	-25.6	-25.7	1.2	20.9	23.9	23.8
-25	-31.5	-10.5	-22.5	-22.6	1.6	21	24	23.9
-22	-28.5	-7.7	-19.7	-19.6	1.1	20.8	23.8	23.9
-19	-25.5	-4.4	-16.4	-16.5	1	21.1	24.1	24
-16	-22.5	-1.4	-13.4	-13.6	1.3	21.1	24.1	23.9
-13	-19.5	1.9	-10.1	-10.2	1.1	21.4	24.4	24.3
-10	-16.5	4.3	-7.7	-7.9	1.1	20.8	23.8	23.6
-9	-15.5	5.2	-6.8	-7	1.2	20.7	23.7	23.5
-8	-14.5	6.1	-5.9	-6	1.3	20.6	23.6	23.5
-7	-13.5	7	-5	-5.1	1.4	20.5	23.5	23.4
-6	-12.5	8.3	-3.7	-3.9	1.4	20.8	23.8	23.6
-5	-11.5	9.4	-2.6	-2.8	1.8	20.9	23.9	23.7
-4	-10.5	10.6	-1.4	-1.6	2	21.1	24.1	23.9
-3	-9.5	11.6	-0.4	-0.6	2.4	21.1	24.1	23.9
-2	-8.5	12.3	0.3	0.1	3.3	20.8	23.8	23.6
-1	-7.5	13.1	1.1	1	4.6	20.6	23.6	23.5
0	-6.5	14	2	1.9	6.1	20.5	23.5	23.4
1	-5.5	14.7	2.7	2.4	7.8	20.2	23.2	22.9
2	-4.5	15	3	2.9	11.4	19.5	22.5	22.4
5	-1.5	16.4	4.4	4.1	12.9	17.9	20.9	20.6

*1- Power from VXG, as ordered and not measured. *2- Power applied to one input (Calculated). Cable loss to the chip input is 6.5 dB. *3- Chip Output Power (calculated) cable+ Att. Loss is ~12dB. *4- Output Power at DSO input (measured). Equalizer adaptive mode is on Hold. *5- Output Power at DSO input (measured). Equalizer adaptive mode is on Run. *6- G=Pout-Pin. *7- Adding 3dB and Equalizer adaptive mode is on Hold. *8- Adding 3dB and Equalizer adaptive mode is on Run.

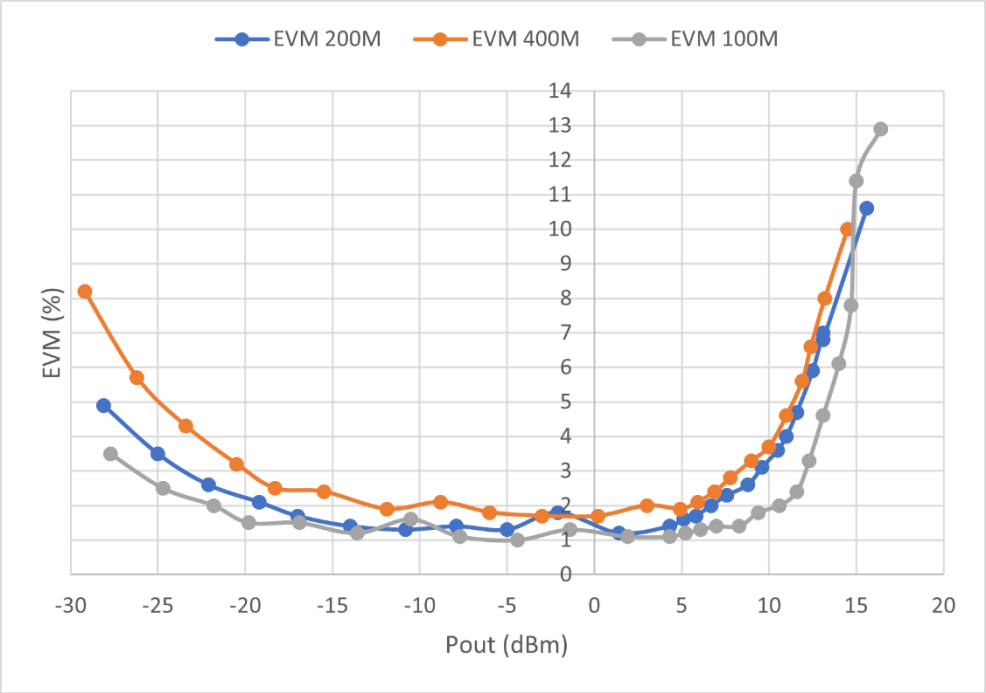

Figure 3.19: Measured EVM versus output power at 64-QAM-100/200/400 MHz.

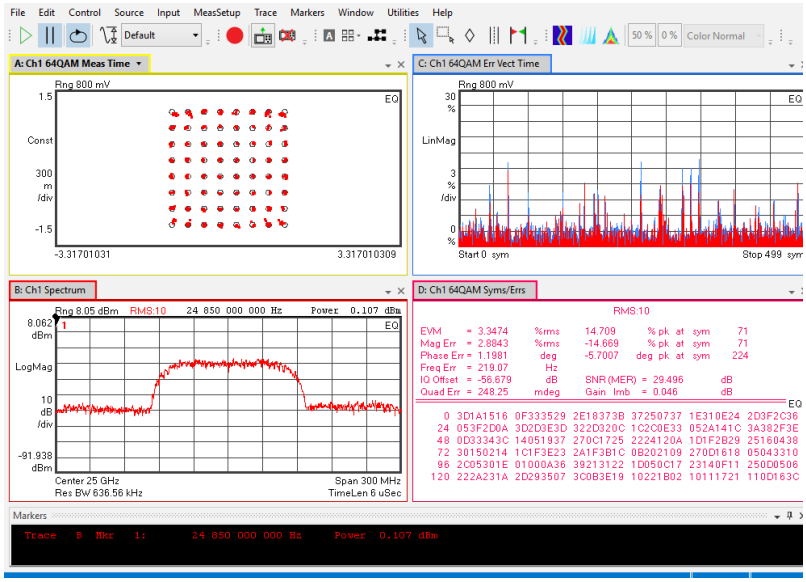

Figure 3.20: Screenshot of the DSO at EVM of 3.4 % while the chip output power is 12.1 dBm (Path loss of 12 dB). The modulation bandwidth is 100 MHz.

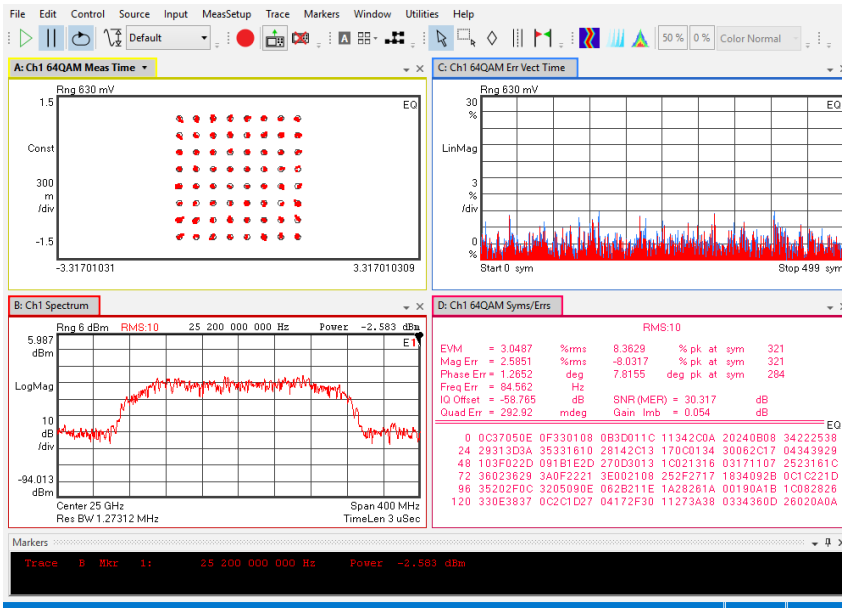

Figure 3.21: Screenshot of the DSO at EVM of 3.1 % while the chip output power is 9.6 dBm (Path loss of 12 dB). The modulation bandwidth is 200 MHz.

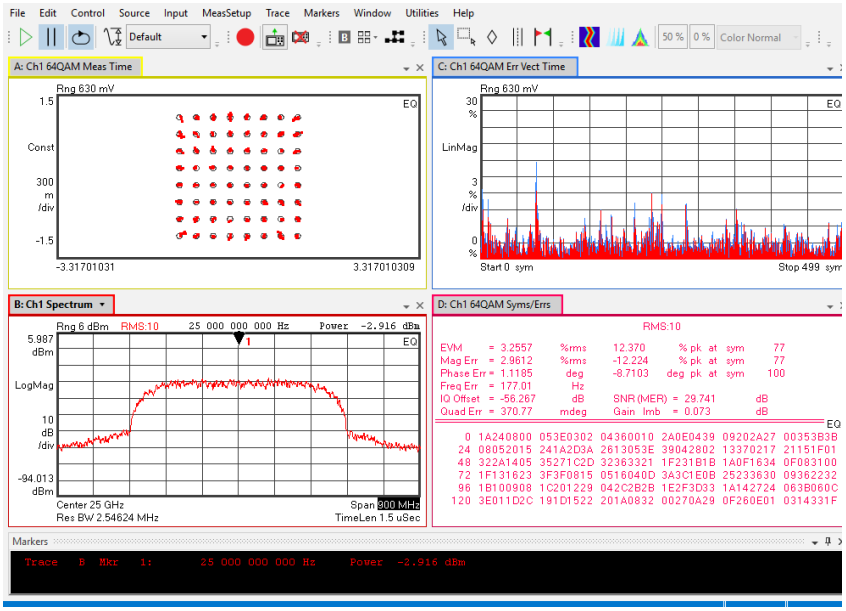

Figure 3.22: Screen shot of the DSO at EVM of 3.3 % while the chip output power is 9.1 dBm (Path loss of 12 dB). The modulation bandwidth is 400 MHz.

Table 3-3: Measurements results summary at 3 % EVM for 64-QAM-100/200/400 MHz modulations at typical conditions.

$f_o = 25$ GHz & $V_{dd} = 1.6$ V				
#	CW Meas.		EVM Meas.	
	Pout (dBm)	Eff (%)	$>$ 3 % EVM	$<$ 3 % EVM
1	8	2.7	-	@64-QAM-400 MHz: EVM= 2.8 %, Pout = 7.8 dBm
2	9	3.4	@64-QAM-400 MHz: EVM= 3.3 %, Pout = 9.1 dBm	@64-QAM-200 MHz: EVM= 2.6 %, Pout = 8.6 dBm
3	10	4.2	@64-QAM-200 MHz: EVM= 3.1 %, Pout = 9.6 dBm	-
4	11	5.2	-	@64-QAM-100 MHz: EVM= 2.4 %, Pout = 11.4 dBm
6	12	6.4	@64-QAM-100 MHz: EVM= 3.4 %, Pout = 12.1 dBm	-

3.3.3.2 EVM Measurements Using 64-QAM-100 MHz Modulation at 1.45/1.6/1.75 V Supply Voltages.

The measurement in this section follows the same setup in the previous section. The difference is while the modulation is kept the same, 64-QAM-100 MHz, the "1.6 V" supply voltage, which includes the biasing of the last two stages, was varied (1.45, 1.6, and 1.75 V). Table (3-4) shows the measurements sheet around 3 % EVM. Figure (3-23) plots the EVM and efficiency versus output power for all the supply voltages, and Figures (3-24,25,26) are the screenshots of the DSO at nearly 3 % EVM for each test. In Table (3-5), The results of this section are summarized and compares it with limits of linearities at compression in continuous wave measurements.

Table 3-4: EVM measurement sheet when the supply voltage is 1.6 V. Notes in Table (3-2) are applied.

Pin VXG	Pin	Pout	Pout DSO	Pout Run	EVM	G	G+3	G2	Idc1	Idc2	Pdc	Pout	Eff
dBm	dBm	dBm	dBm	dBm	%	dB	dB	dB	mA	mA	mW	mW	%
-13	-19.5	1.6	-10.3	-10.4	1.1	21.1	24.1	24.1	4.4	133	217.2	1.4	0.7
-10	-16.5	4.1	-7.8	-7.9	1.1	20.6	23.6	23.6	4.4	135	220.4	2.6	1.2
-9	-15.5	4.7	-7.2	-7.3	1.2	20.2	23.2	23.2	4.4	136	222.0	3.0	1.3
-8	-14.5	5.7	-6.2	-6.3	1.3	20.2	23.2	23.2	4.4	137	223.6	3.7	1.7
-7	-13.5	7.1	-4.8	-4.9	1.5	20.6	23.6	23.6	4.4	139	226.8	5.1	2.3
-6	-12.5	7.9	-4	-4.1	1.6	20.4	23.4	23.4	4.4	141	230.0	6.2	2.7
-5	-11.5	8.8	-3	-3.2	1.9	20.3	23.3	23.3	4.4	143	233.2	7.6	3.3
-4	-10.5	10.2	-1.6	-1.8	2.2	20.7	23.7	23.7	4.4	146	238.0	10.5	4.4
-3	-9.5	11.1	-0.6	-0.9	2.5	20.6	23.6	23.6	4.4	150	244.4	12.9	5.3
-2	-8.5	12	0.3	0	2.9	20.5	23.5	23.5	4.4	154	250.8	15.8	6.3
-1	-7.5	13	1.1	1	3.7	20.5	23.5	23.5	4.4	158	257.2	20.0	7.8
0	-6.5	13.8	2	1.8	4.9	20.3	23.3	23.3	4.4	164	266.8	24.0	9.0
1	-5.5	14.6	2.7	2.6	6.2	20.1	23.1	23.1	4.4	170	276.4	28.8	10.4
2	-4.5	15	3.3	3	7.4	19.5	22.5	22.5	4.4	175	284.4	31.6	11.1
3	-3.5	15.2	3.9	3.2	10.2	18.7	21.7	21.7	4.4	181	294.0	33.1	11.3

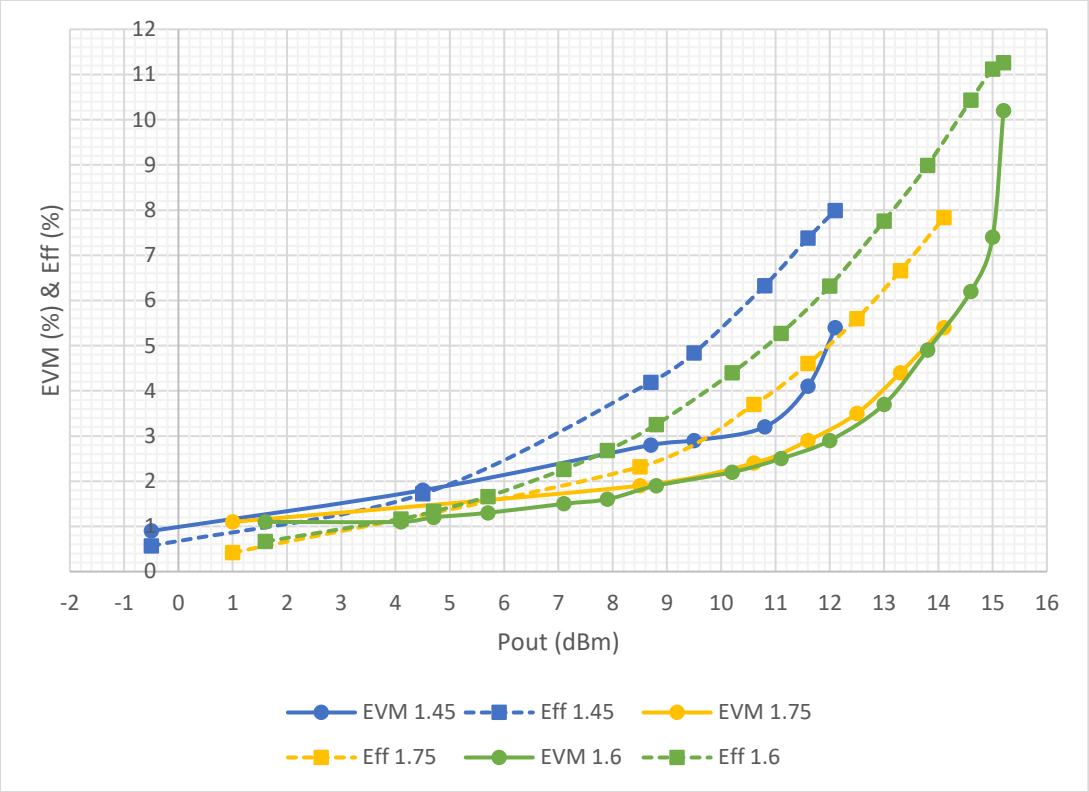

Figure 3.23: The EVM and Efficiency versus output power for power supply's voltages of 1.45, 1.6, 1.75 V. The modulation used is 64-QAM-100 MHz.

Table 3-5: Results summary of EVM and CW measurements at different power supplies.

Supply	64-QAM-100 MHz at 25 GHz			CW Measurements at 25 GHz			
	EVM (%)	Eff (%)	Pout (dBm)	OP-1dB (dBm)	EFF-1dB (%)	OPsat* (dBm)	EFFsat (%)
1.75 V	3.5	5.6	12.5	15.5	10.5	19.7	20.2
1.6 V	3.7	7.8	13	15.5	12.5	18.7	19.6
1.45 V	3.2	6.3	10.8	16.2	16.1	17.4	18.2

*OPsat is the maximum measured output power. Note that OPsat in the table does not have the same gain compression as shown in Figure (3-17).

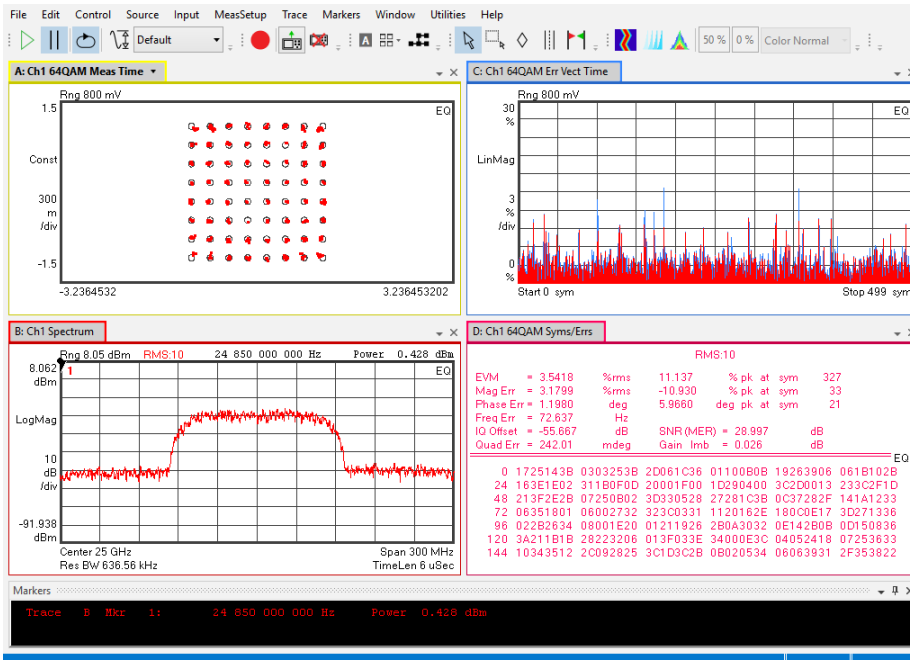

Figure 3.24: Screenshot of the DSO at EVM of 3.5 % while the chip output power is 12.4 dBm (Path loss of 12 dB). This is when the "1.6 V" supply voltage is increased to 1.75 V.

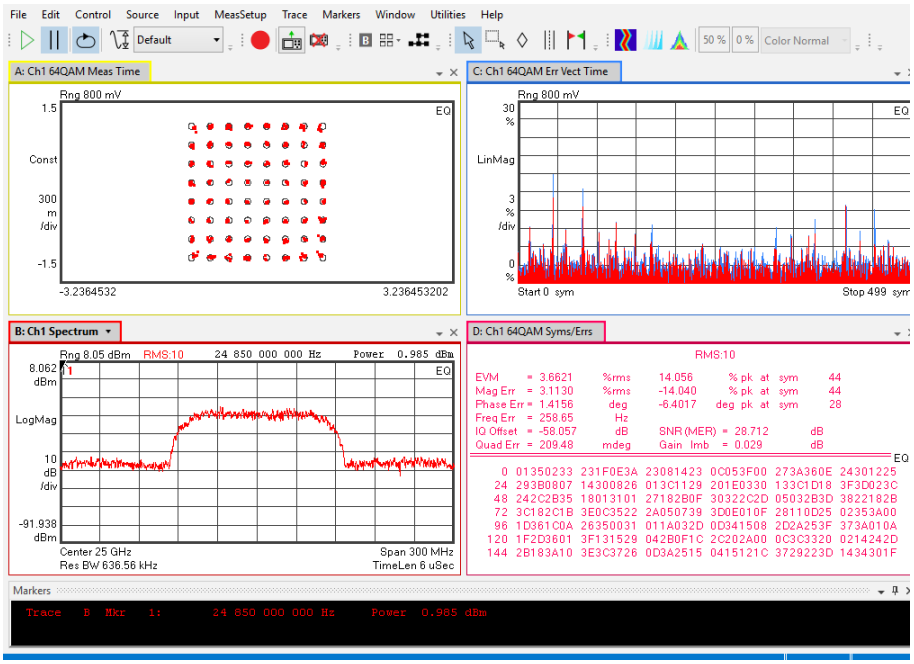

Figure 3.25: Screenshot of the DSO at EVM of 3.7 % while the chip output power is 13 dBm (Path loss of 12 dB). This is when the "1.6 V" supply voltage is kept to 1.6 V.

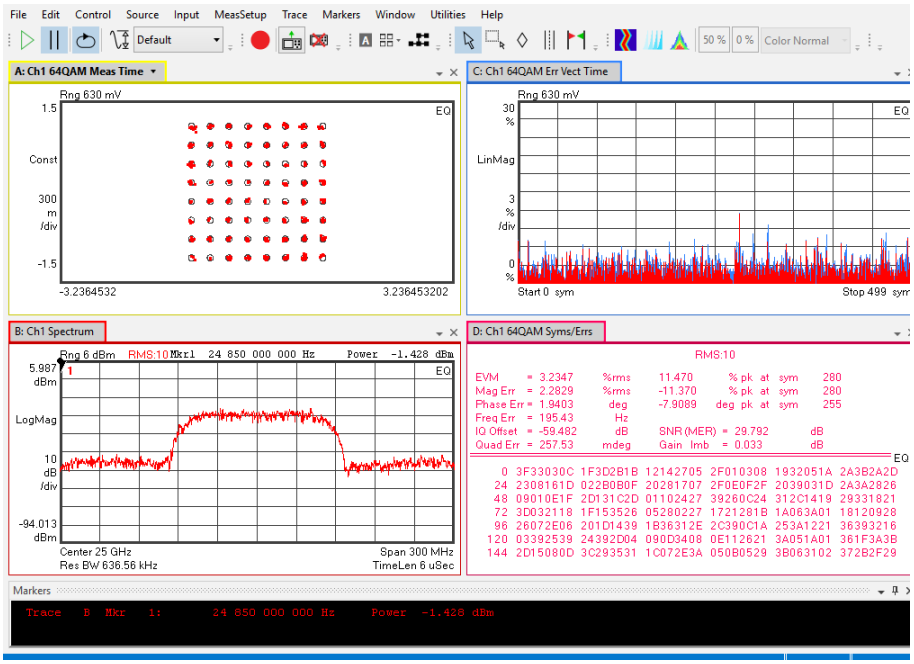

Figure 3.26: Screenshot of the DSO at EVM of 3.2 % while the chip output power is 10.6 dBm (Path loss of 12 dB). This is when the “1.6 V” supply voltage is decreased to 1.45 V.

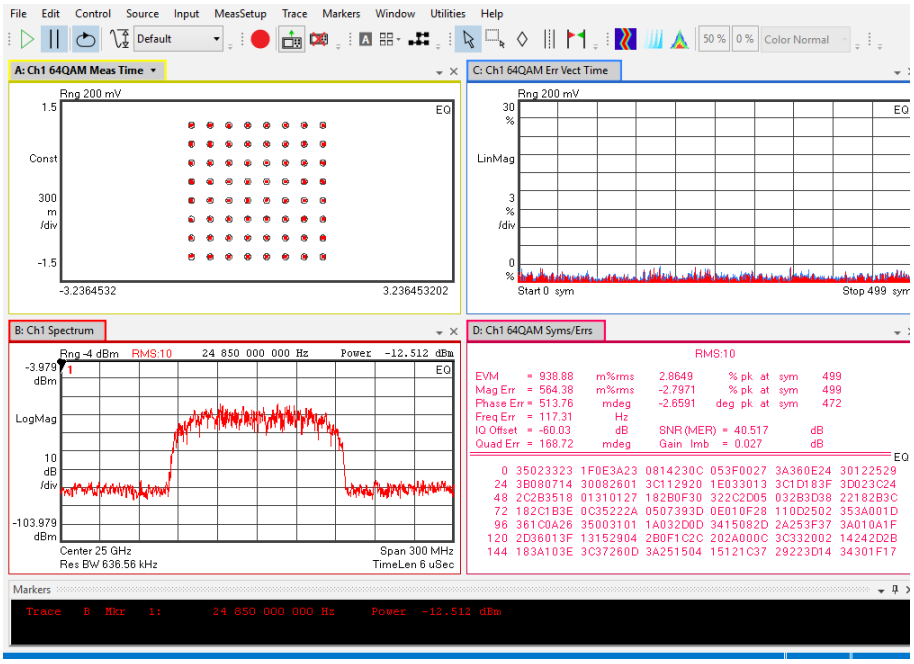

Figure 3.27: Screenshot of the DSO at EVM of 0.94 % (-40.5 dB) while the chip output power is -0.5 dBm (Path loss of 12 dB). This is when the “1.6 V” supply voltage is decreased to 1.45 V.

3.4 Acknowledgements

I thank King Abdulaziz City for Science and Technology for their financial support. I want to thank Global Foundry, Keysight, Cadence, EMX, MATLAB, and many more that I may not be aware of them. Their support extends to many steps of this chapter.

I would like to thank the Ph.D. committee members Prof. Kam Arnold, Prof. Gert Cauwenberghs, Prof. Drew Hall, and Prof. Tzu-Chien Hsueh for their time and academic advice. In addition, I would like to thank the ECE department advisors for their time and advice.

In addition, I would like to thank TICS group members for technical discussions. Special thanks to Dr. Amr Ahmed and Dr. Changtian Wang for their help during Tape-outs. And special thanks to Dr. Omar El-Aassar, Dr. Kream Kibaroglu, and Dr. Qian Ma for their valuable technical discussions.

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Chapter 4 Conclusion

The 22 nm technology was used to implement receive and transmit RF beamformers at Ka band. The following two sections present the conclusion of each beamformer.

4.1 Receiver Beamformer

A Ka-Band receive beamformer with passive phase shifters and attenuators was implemented on 22 nm FD-SOI. The architecture was tested and achieved about 3 dB mean noise figure for different biasing conditions. The power consumed is, typically, 60 mW and it can be lowered to 40 mW. The mean IP-1dB is higher than -21 dBm. The passive attenuators can provide 15.5 dB extra loss with 0.5 dB step with less than 0.3 dB of standard deviation of gain errors. The passive phase shifters have 6 bits with less than 1.5º standard deviation of the phase errors at 27 GHz.

The receive beamformer is compared with other similar beamformers, in terms of architecture and band, in the literature, as shown in Table (4-1). Note that the noise figure and IP-1dB is increased in designs that have a transmit/receive mode switch. Also, the CMOS technologies have an advantage over Bi-CMOS SiGe in terms of temperature stability. However, compound technologies, in general, promise higher performances — for example, it can have higher unity frequency or lower noise figure.

The receive RF beamformers power comparison is mostly dominated by the required IP-1dB. Hence, low noise amplifiers with low power, IP-1dB and Pdc, must optimize the current density to provide the lowest noise figures—by proper device size for fixed current budget. With lower feature length technologies, the reduction of device's maximum allowed voltage requires larger devices' sizes to have the same maximum IP-1dB, and consequently Pdc, in higher feature lengths while keeping the noise figure minimized. That is useful in inductively degenerated common source

networks for noise and power matching since the capacitance (gate or input capacitance) is increased and prevents the requirement to larger input matching components, however adverse effects appear due to layout and in output matching networks.

The measured beamformer kept the noise figure at 3 dB with sufficient gain of 15 dB, at typical conditions. The power consumption, IP-1dB, and OP-1dB are 60 mW, -18 dBm, and -3 dBm (15.8 uW and 0.5 mW). That is with insertion loss of 6-bit phase shifters and 5-bit attenuators of 12.5 dB. In addition, the biasing can be varied for improving a design parameter.

Table 4-1: Design comparison to similar beamformers with different technologies.

Ref.	This Work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Tech.	FD-SOI CMOS 22nm	Bulk CMOS 28nm	Bulk CMOS 40nm	SOI CMOS 45nm	Bulk CMOS 65nm	Bulk CMOS 65nm	Bulk CMOS 65nm	Bi-CMOS SiGe 130nm
IF?	no	yes	no	no	no	no	no	no
Switch?	no	yes	yes	After LNA	yes	no	yes	yes
Note	Single Channel	24-TRX	4-TRX	Common-Leg T/R	Bi-Direc.	8-RX	4-TRX	16-TRX
Freq. (GHz)	24-29	28 (5.5)[b]	28 (1.7)[b]	24-30	25.8-39.2	26.7-30.4	24-28	24-30
G (dB)	Max. Mean[a] 12.6/15.1/15.9/18.2/18.6	16[c] (32-34)[d]	26.3	16	19.2	12[e] 23[f]	27.2	29-30
NF (dB)	Mean[a] @ 27GHz 3.3/2.9/3.1/2.9/3	3.2-4.4[h]	4.5	3.7	3.7	3.8	4.5	3.1-3.9
IP-1db (dBm)	Mean[a] @ 27GHz -18.3/-18/-19.2/-17.2/-17.5	-	[c]	-15	-22.8	-22 (IIP3)	-16.1	-31 to -19
Pdc/Ch (mW)	43/59/71/135/144	42	56.1	54	45	3.4	45	90
G range (dB)	15.5	9[g]	16.4	7.5	8 @28GHz	-	24	8-12
G step (dB)	0.5	1[g]	0.5	0.5	6-bit	-	5-bit	-
(Gain cont.) G error (dB) P error (deg)	@ 25.2GHz 0.23/0.22/0.2/0.22/0.38 4/4.3/4.2/4.4/3.5	- -	0.3 -	<0.8 -	<0.38 -	- -	0.4 1.1	- ±1-±3
Note	standard deviation	-	rms	rms	rms	-	rms	error
P range (deg)	360	360	360	360	360	>360	360	>= 360
P step (deg)	6-bit	3-bit	6-bit	6-bit	6.5-bit	Conti.	>8.8-bit	4-5.6
(Phase cont.) P error (deg) G error (dB)	@ 27GHz 0.85/1/1.3/0.87/0.9 0.22/0.21/0.21/0.19/0.21	- -	0.4 -	<4 -	<1.9 -	0.09 0.14	<0.5 0.3	<1.35 ±0.5
Note	standard deviation	-	rms	rms	rms	rms	rms	rms/error

[a] The mean across Phase Shifters States for bias states 2, 6, 10, 15, and 19 in Table 1.1, [b] 3 dB Bandwidth, [c] The simulated IIP3=-15 dBm, [d] 4 Channels with IF, [e] estimated from figures, [f] Coherent Gain [g]LNA Gain Control [h] For 1-channel measurement.

4.2 Transmitter Conclusion

A Ka-band transmit channel was fabricated on 22 nm FD-SOI from Global Foundry. The channel consists of two-stage power amplifier, three gain amplifiers, 6-bit phase shifters, and 5-bit attenuators of 0.5 dB resolution. The channel was designed to provide saturation power larger than 19 dBm and for efficiency.

The design achieves an efficiency of 12.5 % with OP-1dB of 15.5 dBm at 25 GHz. The channel's last two stages' biasing conditions were varied along with the channel supply and tested under 64-QAM modulation at different bandwidths (100/200/400 MHz). The best efficiency results for the EVM test were at the typical state of bising, where the amplifiers are neither close to class A nor experience gain expansion. For 64-QAM-100 MHz and at an EVM of 3.7 % or -28.7 dB, the beamformer efficiency is higher than 7.5 %. For a continuous wave at 25 GHz test, the efficiency kept increasing to 16.1 % with a reduction to 10 % of all "1.6 V" power supplies' voltage and with cost of lowering the channel gain, specifically the gain of the last two stages.

Table (4-2) presents the design in comparison with similar RF beamformers in different technologies. It should be noted that for similar Psat values, the expected EFF-1dB would be reduced with the reduction of the maximum reliable voltage on a device. That is because the lower maximum reliable voltage devices require the power amplifiers to incorporate more power combination techniques—which usually are not ideal and have loss that reduce the linearity from the maximum desired.

The RF Ka Band transmit beamformer on 22 nm technology reaches to higher than 16 % efficiency with > 22 dB gain when it approaches more toward class B. Additionally, in typical biasing, for 64-QAM-100 MHz, and as can be interpolated from Figure (3-23), when the EVM is at 5.6 % or -25 dB the transmit beamformer efficiency is 9.8 %.

Table 4-2: Transmit beamformer compassion with similar beamformers in different technologies.

Ref.	This work	[8]	[1]	[2]	[6]	[9]	[7]
tech	FD-SOI 22nm	CMOS 28nm	CMOS 28nm	CMOS 40nm	CMOS 65nm	CMOS 65nm	SiGe 130nm
IF	no	yes	yes	no	no	no	no
Switch	no	no	yes	yes	yes	yes	yes
Notes	Single Channel	16-TX	24-TRX	4-TRX	4-TRX	4-TRX	16-TRX
F (GHz)	22.5-26.8	26.5-29.5	28 (8)[e,f]	28 (2.3)[e]	24-28	24-29.5	24-30
Gt (dB)	22.7/27.5/30.2[a]	24-63 [d]	16 [f] 34-44 [d]	44.6	33.1	23 - 25.5	25-31
OP1dB (dBm)	16.2/15.5/15.5	>16	11 [k]	15	>16.1	16-17.6	16
PAE1dB (%)	16.1/12.5/10.5[h]	[b]	10.3 [h,k]	22.1[h]	16.6	20.4	22.1[h]
Psat (dBm)	17.2/18/18.5 @-4dB	18	14[c]	15.7	>18.2	16.8-18	17
PAEsat (%)	18.1/18.6/18.9[h] @-4dB	[b]	20[c] peak	25.2	21.1 peak	20.8 peak	23.3[h]
Pdc (mW) @ Pout (dBm)	Typ:220@(min)	102 @(-)	90 @(-) 122 @11[k] 125[h]@14[l]	143 @15	-	272 @-1dB	180 @(16) 215 @(17)
Selected Modulation (@ EVM) (@ Pout) PAE	64QAM 0.6 Gb/s 100 MHz (@EVM 3.2/3.7/3.5 %) (@EVM -29.8/-28.7/-29) (@10.8/13/12.5 dBm) 6.3/7.8/5.6 %	5G NR OFDM 64QAM 100/800 MHz (@EVM -27 dB) (@9.9 / 9.2 dBm) 8.2/7.2 %	(@EVM -25 dB) 64QAM @SCFDM (@8 dBm) 12 % @OFDM (@6 dBm) 7.5 %	-	64/256QAM 2.4 Gb/s (@EVM 4.8/2.9 %) [f] (@13.5 /10.2 dBm) 8.4/3.5 %	5G NR FR2 OFDM 64QAM 400/800 MHz (@EVM -25 dB) (@10.5/8.9 dBm)	1-Phased array Level 2-For CW: 8dB-backoff PAE> 6 %
G range (dB)	15.5	18 [c]	7 [g]	20.4	24	31.5	20
G step (dB)	0.5	1	1 [g]	2x 6-bits	0.75	0.5	0.25
G error (dB) P error (deg) (Gain cont.)	Min @ 25.2 GHz 0.13 dB <4 deg	-	-	0.3	<0.4 <1.1	0.35 0.8-3.5	-
Note	standard deviation	-	-	resolution	rms	rms	-
P range	360	360	360	360	360	360	>360
P step	6 bits	4 bits	3 bits	6 bits	>8.8 bits	6 bits	4-5.6 bits
P error (deg) G error (dB) (Phase cont.)	Min @ 26.7 GHz 2.1 deg <0.4 dB	-	-	<0.4 <0.3	<0.5 <0.3	1.9 0.4-0.5	<1.35 ±0.5
Note	standard deviation	-	-	rms	rms	rms	rms error

[a] Reported Measurements at 1.45/1.6/1.75 V as shown in Figure (2-15) [b] PA PAE1dB is 29 % and PA PAEsat is 32 % [c] In Single RF Channel [d] Includes IF gain [e] Bandwidth [f] Estimated from figures [g] PA Gain Control [h] Calculated. Efficiency is approximately PAE for high gain. [k] 4-Channels are all on. There is an uncompensated IR drop.

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