UNIVERSITY OF CALIFORNIA SAN DIEGO

Analysis and Implementation of an Internal Signal Amplification Mechanism in Amorphous Silicon

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Materials Science and Engineering

by

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Professor Andrea Tao

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The dissertation of Jiayun Zhou is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

To Jialin

Thanks for growing up with me and carrying half of the darkness.

To Ms. Zhao

Thanks for holding me when I was falling.

To Mr. Yu

Thanks for coming into my life.

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Portions of Chapter 2 include unpublished work on dark current reduction of the a-Si CEP detector by metal oxides, with the efforts of **Zhou, J.**, Yu, Y., Chiu, S.Y., Nomura, K., and Lo, Y.H, and integrated CEP detectors based on the designs of incorporating JFET with a-Si, with the efforts of Zhou, J., Liu, Y.H., Damle, S., and Lo, Y.H. The dissertation author is the primary investigator/first author of the project.

Portion of Chapter 3 reprints the work that has been submitted to Optics Express: **Zhou, J.**, Chiu, S.Y., Miah, M.A.R., Yu, Y., and Lo, Y.H., 2022. Athermalized Carrier Multiplication Mechanism for Detectors Using an Amorphous Silicon Gain Medium. Submitted. The dissertation author is the primary investigator/first author of the paper.

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PUBLICATIONS AND PATENTS

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Xu, Z., Yu, Y., Arya, S., Niaz, I.A., Chen, Y., Lei, Y., Miah, M.A.R., **Zhou, J.**, Zhang, A.C., Yan, L. and Xu, S., 2020. Frequency-and power-dependent photoresponse of a perovskite photodetector down to the single-photon level. *Nano Letters*, 20(3), pp.2144-2151.

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ABSTRACT OF THE DISSERTATION

Analysis and Implementation of an Internal Signal Amplification Mechanism in Amorphous Silicon

by

Jiayun Zhou

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This dissertation reports an internal signal amplification mechanism for light detection, cycling excitation process (CEP). This mechanism relies on the localized bandtail states which

involve Auger excitation process and k-selection rule relaxation. There were many previous works showing attractive characteristics of CEP devices, including high detection efficiency, low noise, high speed, low operation voltage, etc. This work mainly demonstrates the experimental characterization and physical models for the amorphous silicon (a-Si) CEP detectors.

CEP mechanism has the fundamental difference from impact ionization in all APDs. One of the significant differences is its intrinsically athermalized performance. The temperature sensitivity of the standard a-Si CEP detectors from 200 K to 350 K is found to be nearly temperature independent. This athermalized multiplication characteristic in a-Si CEP detectors offers significant advantages over the impact ionization process in conventional APDs. Temperature sensitivity is a key consideration for detector arrays with readout circuits in LiDAR and imaging applications. The athermalized property can tolerate large temperature variations to achieve stable gain and photon detection efficiency, as well as low pixilation noise with the relaxation of precise temperature control.

The detection range of CEP devices can be designed for certain wavelengths by assembling a proper absorption medium. An innovative design of an uncooled high-performance, longwave-infrared quantum detector made of an a-Ge layer and an a-Si layer is demonstrated. The photoexcitation mainly occurs in a-Ge and then the carriers can transport to the a-Si layer for multiplication. This detector has the highest detectivity among the reported room-temperature LWIR quantum detectors and the NEP value sets the world record. This LWIR quantum detector has great potential to meet the performance and cost requirements for many applications: night vision, robotic and machine vision, medical imaging, remote sensing, etc.

Finally, the first stage of the CMOS compatible process development for several CEP detector structures is accomplished. The characterization of a-Si deposition by CMOS foundry

works in parallel with the design of the hybrid process: incorporating CMOS process and laboratory process. The hybrid process flow for both parts has been demonstrated with the sample layout set for singular device designs and pixel arrays.

Chapter 1. Introduction

1.1 Photodetection

Light detection has been widely utilized nowadays. For any optoelectronic system such as imaging, sensing and communication, photodetection is the key step which converts the input optical signal into a signal of another form, mostly electric signal. This process is commonly known as OE conversion. During OE conversion, a photon is absorbed by an absorber and the photon energy can be transferred to emit an electron-hole pair based on the photoelectric effect. Under electric field provided by either external bias or built-in potential, the photo-generated electron-hole pair is drifted and extracted by anode and cathode as photocurrent.

Based on the wavelengths of detection, various types of materials are applied depending on the photon energies and material band gaps. Carrier transportation and photocurrent generation are impacted by device structure and material quality. With fewer heterojunctions, smaller band misalignment and lower density of impurity states, carrier transportation can be smoother. As a result, the efficiency of OE conversion is higher. Overall, the processes of carrier generation by photon absorption, carrier transportation under electric field and extraction of the carriers as terminal current to provide the output signal are related to the photodetection sensitivity, gain, quantum efficiency and noise generation of the devices. Briefly, quantum efficiency and responsivity define the quality of the OE conversion at a particular wavelength; gain determines how strong the signal is amplified by the detector. In the following sessions, multiple types of photodetectors will be introduced and discussed [1-5].

1.2 Photodetectors

1.2.1 Photodiodes

Photodiodes are the key devices in the front end of optical receivers and work as OE converters. They have been attracting increasing attention in both academic and industrial domains in a wide range of applications in image sensing, biomedical and chemical detection, and optical communication [6-8]. Photodiodes are structured based on P-N or P-I-N junctions. Unlike a laser diode or LED diode in which the PN junction is forward biased, the PN junction of a photodetector is reverse biased so that only a very small reverse saturation current flows through the diode without any input optical power. In figure 1.1a, a P-I-N photodiode is shown, with reverse bias applied. Figure 1.1b illustrates the band diagram of the photodiode and how it operates: under reverse bias, most applied voltage drops in the depletion region, which is the intrinsic layer. When the photodiode receives an optical power, photons are absorbed in the depletion region and generate electron-hole pairs. The existing high electric field serves to separate the photogenerated electron-hole pairs fast, while in a neutral n-type or p-type region, the carrier transport is dominated by a diffusion process due to the lack of electric field.

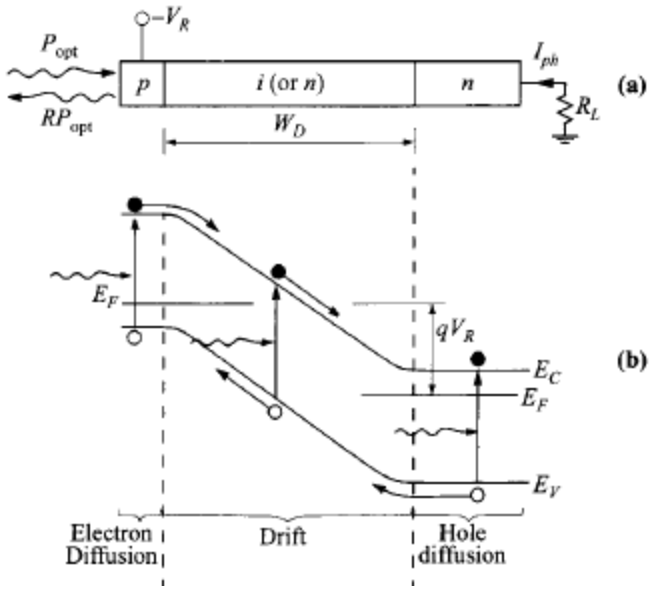

Figure 1.1 Operation of photodiode. (a) Cross-sectional view of p-i-n diode. **(b)** Energy-band diagram under reverse bias [2].

For a typical PN junction based photodetector, there are some general characteristics to be considered and most reported works are aiming to find the optimized properties of photodetectors by improving these characteristics: quantum efficiency, response speed, and device noise.

Quantum efficiency, efficiency of photon absorption in photodetectors, is defined as the number of electron-hole pairs generated per incident photon. The absorption capability of a given semiconductor material has a wavelength range, in which appreciable photocurrent generated is limited. The main mechanism of OE conversion for most photodiodes is band-to-band photoexcitation, and the long-wavelength cutoff is determined by the semiconductor band gap. When the photon energy is lower than the band gap, the absorption can be negligible. Moreover, there is also a short-wavelength cutoff of device photo response, which is due to the very large absorption coefficient, resulting in the radiation absorption too near the surface where recombination is more possible [2]. Therefore, the photo-generated carriers have higher probability of being recombined than drifted and collected by electrodes and contributing to photocurrent.

The response speed of a photodiode is related to the carrier transport time. There are two main carrier transport processes during typical photodiode operation: carrier drift and diffusion. With carriers' drift under electric field being faster than diffusion, the key factors that limit device speed are the drift time in depletion region, diffusion of carriers, and depletion capacitance. As diffusion is a slower process compared to drift, the junction should be formed close to the surface and sufficiently wide so that most photocarriers can be generated within the depletion region and experience drift from the start. However, the depletion layer should not be too wide as the transit-time effect will limit the frequency response. In order to satisfy both conditions: sufficient depletion layer for carrier generation and short transit time, the junction needs to be reverse biased to a sufficiently high level and ensure the carriers to be drifted at their saturation velocities. Besides, the depletion layer width determines its capacitance, which also affects the device speed because an excessive capacitance will contribute to a large time constant.

There are different types of noise in optoelectronic devices. As a result of the high dark current, the noise in photoconductor devices is commonly known as Johnson or thermal noise, generated by the thermal agitation of the charge carriers [9]. The noise current i_j is modeled by,

$$i_j = 4k_B TB/R_c \tag{1.1}$$

where B is the bandwidth of the device and R_c is the resistance of the photoconducting channel.

Thermal noise is usually low in semiconductor photodiodes due to the low dark current at reverse bias. However, there is another source of noise, generation-recombination noise, causing fluctuations in the carrier concentrations. The noise current $i_{GR}$is given by,

$$i_{GR} = \frac{4q\Gamma_G I_0 B}{1+\omega^2\tau^2} \tag{1.2}$$

It's also called shot noise, which can be reduced by operating the devices at low temperature [10]. For photodiode devices, the shot noise is only generated in the depletion region because of the low dark current at reverse bias.

At a low frequency range less than 1kHz, flicker noise arises from surface and interface defects and traps in the bulk of the semiconductor [11]. The spectral noise current is given by,

$$\underline{i_j}^2 \propto \frac{1}{f} \tag{1.3}$$

1.2.2 Avalanche Photodiodes (APDs)

Avalanche photodiodes (APDs) utilize impact ionization, a carrier multiplication process as the internal gain mechanism to achieve high sensitivities. They are operated at high reverse-bias voltages where avalanche multiplication takes place. To better understand the working principle of APDs, the first step is to understand the theory of impact ionization.

In the impact ionization effect in semiconductors, free carriers are accelerated by a high electric field and gain sufficient kinetic energy to "knock out" an electron from the valence band to conduction band. The "high" electric fields required to observe impact ionization are highly dependent on the band gap of the material and temperature. The minimum energy needed for impact ionization is the ionization threshold energy E_i. The ionization rates for electrons and holes, denoted by α and β respectively, are strongly influenced by the threshold energies [12]. The ionization rates are defined as the reciprocal of the average distance along the direction of the electric field, traveled by an electron or hole to create the secondary electron-hole pair, shown in figure 1.2.

Figure 1.2 also illustrates the impact ionization effect in a P-I-N diode based APD under high reverse-bias voltage. The high electric field accelerates photocarriers to high energies. These accelerated primary carriers have certain probabilities to lose kinetic energy and excite secondary

electron-hole pairs to the mobile bands. Secondary e-h pairs are produced and drifted together with the primary carriers. These would lead to more new carriers generated on the way across the depletion region. The avalanche multiplication gain can be expressed as:

$$M = \frac{(1-\frac{\beta}{\alpha})exp[\alpha_n W_D(1-\frac{\beta}{\alpha})]}{1-(\frac{\beta}{\alpha})exp[\alpha_n W_D(1-\frac{\beta}{\alpha})]} \tag{1.4}$$

where W_D is the depletion-layer width and α and β are the electron and hole ionization rates, respectively.

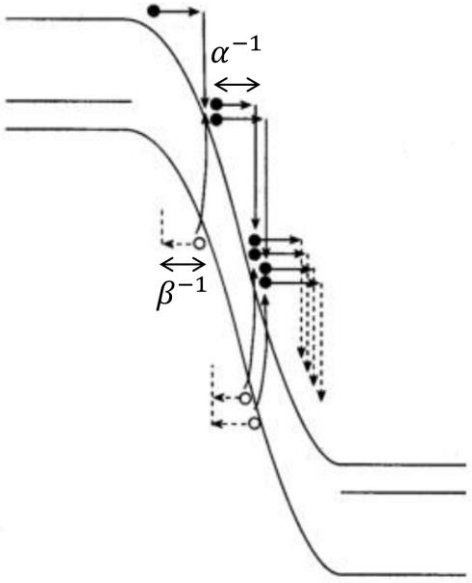

Figure 1.2 Schematic diagram illustration of the carrier multiplication in impact ionization.

In a practical device, the limitation of maximum achievable dc multiplication at high light intensities are the series resistance and the space-charge effect. When the dark current is higher than photocurrent, dark current becomes the limitation of maximum multiplication. Thus, it is important that the dark current is kept as low as possible.

As each newly generated electron-hole pair at a given distance in the depletion region is an independent occurrence and does not experience the same multiplication, the avalanche process

overall is statistical in nature. As a result, the avalanche gain fluctuates, and the excess noise can be described by a noise factor:

$$F(M) = \frac{<M^2>}{<M>^2} = \frac{<M^2>}{M^2} \tag{1.5}$$

The noise factor $F(M)$ has strong relation to the ratio of coefficients $\frac{\beta}{\alpha}$ as well as the low-frequency multiplication gain M, which is expected to be small when the difference of two coefficients is large [5]. Hence, it is desirable to have one carrier dominate during the impact ionization process.

1.2.3 Single Photon Avalanche Diodes (SPADs)

Single photon avalanche diodes (SPAD) are also known as Geiger-mode APDs or G-APDs. They are a class of solid-state photodetectors based on a reverse biased P-N junction in which a photo-generated carrier can trigger an avalanche current due to the impact ionization mechanism. SPAD devices are able to detect low intensity signals down to single photon level and to signal the arrival times of the photons with a jitter of a few tens of picoseconds [13]. It has similar working principles as conventional APDs, while the fundamental difference between them is that SPADs are specifically designed to operate at a reverse bias voltage well above the breakdown voltage. On the contrary, APDs operate at a bias lower than the breakdown voltage. Under this bias, the electric field is sufficiently high that a single charge carrier injected in the depletion layer can trigger a self-sustaining avalanche. After a sub-nanosecond rise-time frame, the photocurrent quickly increases to a macroscopic steady level around mA range. However, once the photon detection completes, the current continues to flow until the avalanche is quenched by lowering the reverse bias voltage down to or below breakdown voltage [14]. To detect another incident photon, the bias voltage needs to be ramped up again above the breakdown voltage.

1.2.4 Phototransistors

Phototransistors are semiconductor devices that sense light levels and alter the current flowing between emitter and collector according to the level of light they receive. Phototransistors and photodiodes can be both used for light detection, while the former are more sensitive in view of the amplification provided by the bipolar transistor structure. On the other hand, the fabrication of a phototransistor is more complicated than that of a photodiode, and the inherent larger area impedes the response speed and degrades its high-frequency performance.

Figure 1.3 shows the cross-sectional structure of an N-P-N bipolar phototransistor (fig. 1.3a), together with its circuit model (fig. 1.3b). Compared to a conventional bipolar transistor, it has a large base-collector junction as the light-collecting element, represented by a parallel combination of a diode and a capacitor shown in the equivalent circuit. The band diagram in figure 1.3c illustrates the process for light detection in a phototransistor device. The photogenerated holes flow to the maximum energy position in the depletion-layer and then are trapped in the base. With holes accumulated, the increasing positive charges in base lowers the energy levels (raises the potential) and thus lowers the energy barrier for electrons to flow from emitter to collector. As a result, a much larger electron current is induced by a small hole photocurrent, which can be defined by emitter injection efficiency γ. It is the dominant gain mechanism shared by both bipolar transistors and phototransistors, provided that the electron transit time through the base is much shorter than the minority-carrier lifetime. Meanwhile, the photogenerated electrons can either travel to the emitter or to the collector based on the location of origin. Hence, the photocurrent induced by photogenerated electrons will either reduce the emitter current or enhance the collector current, by a small amount as the gain is large and the total emitter current or collector current is much higher than the photocurrent.

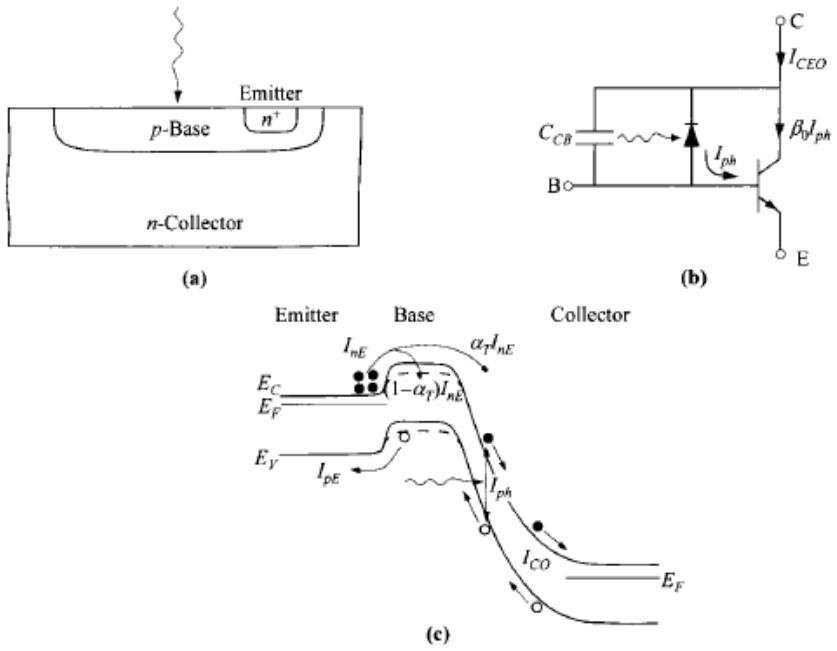

Figure 1.3 (a) Schematic structure of a phototransistor. **(b)** Equivalent circuit. **(c)** Energy-band diagram under bias showing different current components. Dashed lines indicate shift of base potential (open base) under illumination [2].

1.3. Motivation

High sensitivity is always a desired characteristic for optoelectronic systems such as sensing, imaging, LiDAR, and quantum communications. Impact ionization, the prevailing intrinsic mechanism for signal amplification, has been utilized for over 40 years in semiconductors. Based on this, APD has been a popular choice which utilizes the impact ionization mechanism to amplify the photocurrent and thus enhance detection sensitivity. The multiplication factor of APDs increases with the reverse bias voltage and the devices can transition from analog mode to Geiger mode to achieve sensitivity to single photon level input as SPADs. This requires the applied reverse bias to be higher than the breakdown voltage. However, there are some shortcomings for APDs and SPADs intrinsically from impact ionization. The stochastic nature of the carrier multiplication process has generally low energy efficiency (i.e., requires high bias voltage) and produces high excess noise especially in the high gain regime [15-17]. When operated in Geiger mode, the gain

fluctuations give rise to variations in the output response, limiting the dynamic range or photon number resolving capabilities and the photon detection efficiency (PDE). Moreover, temperature sensitivity is a key consideration when SPADs are integrated into an array with readout integrated circuits (ROICs) for LiDAR, imaging or sensing systems. Temperature variations due to the ambient or local environment can cause gain fluctuations and pixelation noise for APDs and PDE fluctuations for SPADs due to the temperature sensitivity of breakdown voltage.

To address the limitations in carrier excitation efficiency and excess noise impede a higher sensitivity and good SNR, a new signal amplification mechanism, cycling excitation process (CEP), has been proposed and demonstrated, which achieves the goals of high sensitivity, high speed response, low excess noise and high energy efficiency.

1.4 Synopsis of Dissertation

As discussed in section 1.3, a novel carrier multiplication mechanism, cycling excitation process (CEP), will be provided and demonstrated in this dissertation. It is found to be most prominent in certain disordered materials such as amorphous silicon (a-Si) [18-20]. Under electric field, these materials display a strong carrier multiplication effect via Auger excitation of electron-hole pairs to the localized states in the bandtails of conduction and valence bands. By relaxing the k-selection rule (i.e., conservation of momentum), CEP detectors possess high gain, high efficiency, and ultralow noise. And it has been implemented in various structures for different applications such as single photon detection, long-wave infrared detection, etc.

In Chapter 2, a new carrier multiplication mechanism, cycling excitation process (CEP), is introduced. The main mechanism of CEP is the carrier excitation from localized states to mobile bands. With abundant localized states and strong electron-phonon interactions as the two key physical insights, CEP effect can be achieved in disordered materials such as amorphous silicon

(a-Si). The fabrication process of a-Si CEP device is introduced so as the DC and AC measurement results. Moreover, to reduce the dark current so as to reduce the device noise, a proposed device structure by adding a thin layer of metal oxides such as Cu_2O and SnO_x is demonstrated.

In Chapter 3, a further investigation of CEP mechanism is demonstrated with temperature dependent characterizations. Under high electric field where high gain happens, field-enhanced tunneling dominates the localized state excitation to sustain the carrier multiplication cycles whereas phonon-assisted excitation plays some roles under low bias and moderate gain. This athermalized property of CEP detectors is unique and offers important advantages over conventional APDs or SPADs because of the relaxed requirements for precision temperature control and reduced pixilation noises due to local temperature variations.

In Chapter 4, a high performance LWIR quantum detector is demonstrated. With a simple structure by using an a-Ge thin layer as absorber for LWIR light and another layer of a-Si as CEP gain media, it shows high detectivity and low noise equivalent power (NEP) at high frequency range (> 100 Hz). Besides, the device is operated at room temperature, unlike most quantum detector for LWIR detection. The proposed physical model is based on the photoexcitation of electrons from bandtail states of a-Ge to mobile states, integrated with CEP amplification mechanism in a-Si layer.

In Chapter 5, first stage of CMOS compatible a-Si CEP device is demonstrated. The corresponding CMOS design, process flow and preliminary results are introduced. The forward path is defined for more CMOS integration development based on a-Si CEP device.

In Chapter 6, the novel light detection mechanism, CEP is summarized and concluded. In addition, a very brief outlook for future projects is discussed.

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Chapter 2. Cycling Excitation Process (CEP)

2.1 CEP in Thin Amorphous Silicon

The cycling excitation effect was first discovered in heavily doped, compensated p-n junctions in 2015 [1,2]. It is an internal signal amplification mechanism that is fundamentally different from impact ionization. CEP has high gain performance at bias voltage as low as 3~5 V and the excess noise factor is 30 times lower than typical avalanche photodetectors [2]. The high efficiency of CEP detectors is found to depend on the assistance of the localized states from the compensated impurities in the p-n junctions. Based on this discovery, we investigated CEP in disordered materials such as amorphous Si (a-Si) in the later works, which naturally have plenty of localized states due to the material nature.

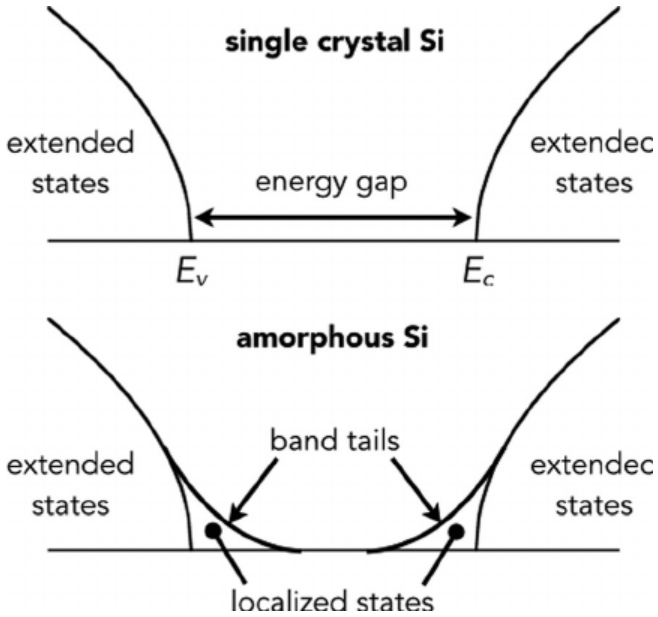

Figure 2.1 Schematic drawing of density of states in single crystal and amorphous silicon [8]. Localized states occur at band tails of a-Si band edges.

The difference of density of states in crystalline and amorphous silicon is shown in the simplified energy band scheme, Fig. 2.1 [3]. E_c and E_v are the conduction band edge and valence band edge. In the crystal silicon, the density of states falls to zero at E_c and E_v strictly as shown in

the upper panel. In contrast, the disorder structure or the tilt atomic bonding of the lattice in amorphous silicon results in the localization of the states. As shown in the bottom panel, there are localized states introduced at the band tails in amorphous silicon. The electron states are not extensive but localized with the exponential decay in the wave function from the conduction and valence band edges. The localized acceptor states near the valence band edges are below fermi level for the intrinsic a-Si, hence usually occupied whereas the donor localized donor states near the conduction band is above fermi level, hence usually empty.

The existence of localized states offers extra scattering sites for electrons/holes in electronic transitions so that the momentum conservation is no longer a restriction during the process. This is one of the main reasons for the high amplification efficiency of the CEP effect [4-6]. CEP is found to be most prominent in a-Si based devices. The basic structure of CEP photodetectors for visible light detection is a thin layer of a-Si (25 nm ~ 60 nm) on a n-type crystalline silicon substrate with ITO as the top electrode. The detailed characterization of this CEP detector will be demonstrated in the next section.

2.2 Standard a-Si CEP Detectors

2.2.1 Device Structure and Fabrication

In this section, I will demonstrate one of the standard CEP detectors based on a 35~40 nm thin a-Si layer as the gain medium. The device layout and cross-section are shown in Fig. 2.2(a,b). It starts from the n-Si substrate with doping concentration around 2e19 cm^{-3}. After solvent clean of the substrate, the native oxide on the surface of the silicon substrate is removed by Hydrofluoric Acid (HF) dip. Right after native oxide removal, the substrate is transferred into a plasma enhanced chemical vapor deposition (PECVD) chamber for a-Si deposition. The thin a-Si layer is formed by 5% SiH_4 diluted in Helium at the temperature of 270 °C. CH_4 gas is also participating in the

deposition for 5% carbon dope in the a-Si material. After deposition of 35~40 nm a-Si, a 100 nm SiO_2 layer is deposited in sequence in the same chamber at the same temperature. This layer of SiO_2 is the etch mask for a-Si etch and will not exist in the final structure. In order to pattern the SiO_2 layer, a photolithography process is followed and a wet etch step by buffered oxide etch (BOE) is used for the oxide etch. A circular shape is designed to avoid the field-crowding issue in the a-Si layer when operating the device. The sample with the patterned SiO_2 mask is then processed by ICP-RIE dry etch for around 12 sec to etch away the a-Si and etch around 30 nm into n-Si substrate as the mesa of the device. The two types of gas, SF_6 and C_4H_8, are introduced in the process for anisotropic etch and the selectivity of SiO_2: a-Si is around 10:1. Residues created during the etching process can be observed under dark field microscopy and RCA clean process (RCA 1 and RCA 2) follows to clean the sidewall of the device mesa and the surface of etched substrate. Afterwards, the SiO_2 mask is removed by BOE wet etch. The next step is to passivate the sidewall of the device. The passivation layer is 40 nm Al_2O_3 by atomic layer deposition (ALD) at the temperature of 250 °C followed by a 200 nm SiO_2 layer by PECVD at the temperature of 270 °C for insulation. Before taking the sample into the ALD chamber, a step of HF dip is introduced to remove native oxide. A second photolithography step follows to pattern these two oxide layers for electrode windows opening: a circular pattern on the device mesa is for the top electrode and other rectangular patterns are for the ground electrode. The oxide is opened by BOE wet etch. Next, the third photolithography step is for a 150 nm indium tin oxide (ITO) layer that is sputtered on top of the a-Si layer to form a transparent top electrode. Finally, the fourth photolithography for electrode contact pads is followed with the Ti/Au deposition by sputtering and lift-off process to form the cathode and anode contacts in a configuration compatible with the ground-signal-ground (GSG) co-planar probe. The fabrication process flow of this device is shown

in Fig. 2.3. The device will be reverse biased by applying negative voltage to the ITO top contact during measurements.

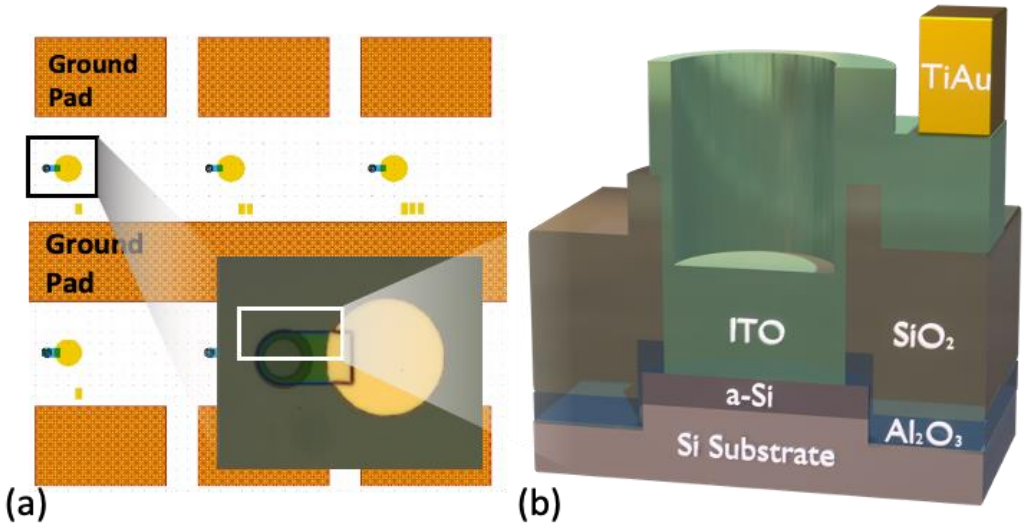

Figure 2.2 (a) Layout of CEP detectors designed for GSG probing and top view of the device; **(b)** Cross-section of the device.

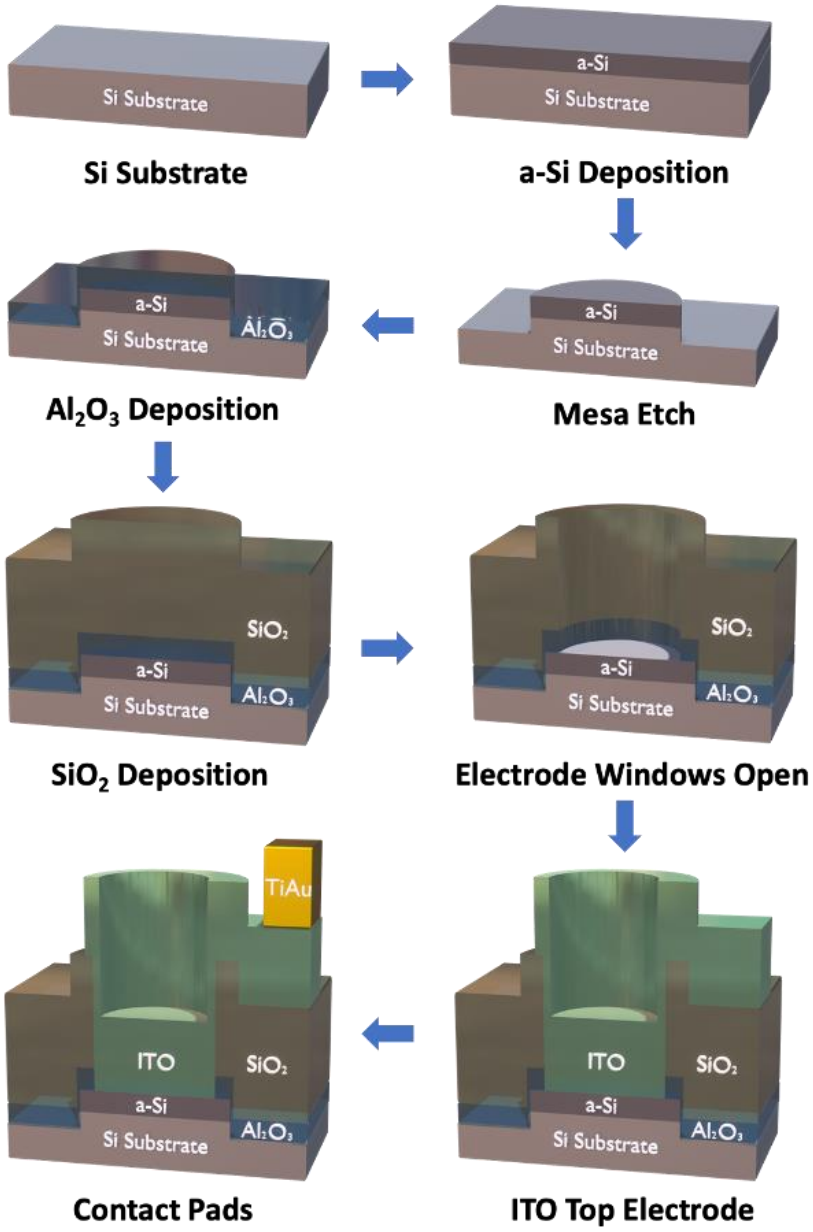

Figure 2.3 Fabrication process flow of a-Si CEP detector

2.2.2 Mechanism

During operation, CEP detectors are reverse biased, and the a-Si amplification layer is under a high electric field. Under the high electric field, disordered materials with plenty of localized states can display a strong carrier multiplication effect via Auger excitation of e-h pairs to the localized states in the band tails of conduction and valence bands. Such a carrier excitation

process can be more efficient than conventional impact ionization because the localized carriers involved in the process relaxes the k-selection rule, the main efficiency limiting factor [7,8]. In other words, in the conventional impact ionization process, the energetic carriers need to follow the rules of conservation of energy and conservation of momentum. In contrast, for CEP in disordered materials, when the energetic electron/hole is in a localized state (small spacing), it no longer has a well-defined crystal momentum and only needs to follow the energy conservation rule. Thereby, the probability of creating the next generation of e-h pairs can be enhanced.

Compared with a typical impact ionization process, for those localized electrons (holes) to contribute to the photocurrent and to gain kinetic energy from the applied field to sustain the cycling excitation process, these localized carriers need to be excited to the mobile bands. The excitation process of the localized carriers can then play the role of internal feedback to suppress gain fluctuations, thus giving rise to low excess noise in both analog mode and Geiger mode [2,4]. The previous studies inferred that the low excess noise of CEP detectors was attributed to electron-phonon coupling, considering CEP as a phonon mediated process [2,4].

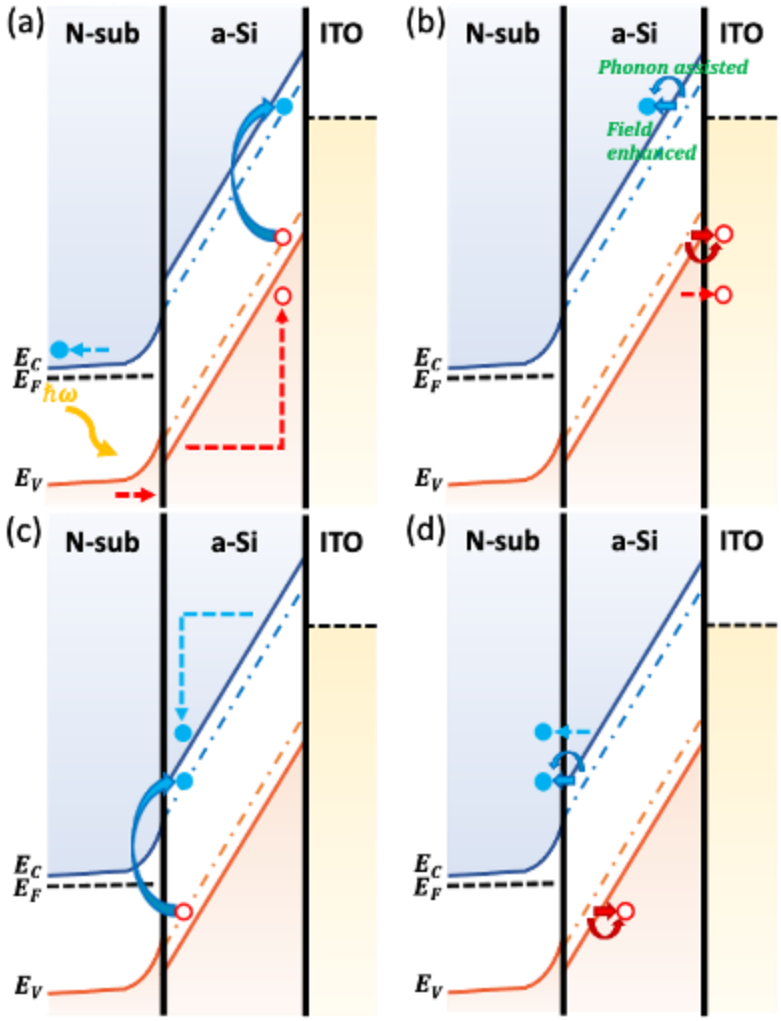

Figure 2.4 Schematic illustration of the carrier multiplication process involving excitation of localized (bandtail) states. (a) hole-initiated generation of e-h pair in localized states, **(b)** excitation of localized states via phonon excitation (temperature dependent) or field-enhanced tunneling (temperature independent), **(c)** electron-initiated generation of e-h pair in localized states, and **(d)** excitation of localized states via phonon excitation or field-enhanced tunneling.

The band diagram of the standard 35~40 nm a-Si CEP detector and the cycling excitation process under reverse bias are shown in Fig. 2.4. Since the a-Si layer is very thin, a limited portion of incident light is absorbed in the layer while the major portion of absorption happens in the n-Si substrate. The photoexcited electrons in n-Si are collected by the electrode while the photoexcited holes enter the a-Si layer to initiate the CEP process. As shown in Fig. 2.4(a), the hole travels along the electric field and acquires sufficient kinetic energy from the applied E-field to excite an

electron-hole pair to the localized states in the band tails, a process that was calculated to have high probability due to relaxation of the k-selection rule [7,8].

As illustrated in Fig. 2.4(b), these localized electrons and holes can contribute to the output signal and sustain the carrier multiplication process only after they are excited to the conduction or valence band. There are two significant mechanisms that can be involved in this excitation process: either phonon assisted absorption or field enhanced tunneling. Phonon assisted absorption is more temperature dependent: more dominated as temperature increases, while field enhanced tunneling is a temperature independent event but relies on the applied electric field. The quantized significance of these two mechanisms in the standard a-Si CEP device is illustrated in Section 3.3.

Similarly, the secondary electron, as soon as being excited from the localized state to the conduction band, can also travel along the a-Si layer and acquire kinetic energy from the applied E-field to excite another electron-hole pair to the localized bandtail states (Fig 2.4(c)) and then the localized carriers can subsequently be excited to the mobile bands via phonon-assisted excitation or field-enhanced tunneling (Fig. 2.4(d)) to keep the cycles of the carrier multiplication process. This continuous carrier multiplication process with the unique contribution of the localized states in the ordered material is the so-called CEP process.

2.2.3 Characterization at Room Temperature: DC and AC

The DC dark current and photocurrent are measured by a source meter connected with two tungsten single probes, one probing on the top electrode contact pad and the other probing on the ground electrode contact pad. The negative bias is applied to the top electrode to reverse bias the standard 35~40 nm a-Si CEP device. As shown in Fig. 2.5, the black lines are dark IVs of multiple devices, and the red curves are photocurrent calculated by subtracting dark current from light-on current at that bias. The active area of the device under test is 12 μm in diameter. The laser for the

incident light has a wavelength of 639 nm and the incident power in this measurement is around 160 nW. The photocurrent at -1 V, I_0, is considered as the primary photocurrent since the photoresponse plateaued when the bias reached -1V. At this bias, the CEP process has not been initiated and the photoresponse is purely from generation of e-h by absorption. The primary quantum efficiency at this bias can thereby be calculated and it was around 2% for this incident light with this amount of power. The gain of the device can also be calculated from the ratio of the photoresponse at a certain bias (V_{app}) and the primary photoresponse, as $I(V_{app})/I_0$, and in this measurement, the DC gain at 4.5 V was around 30.

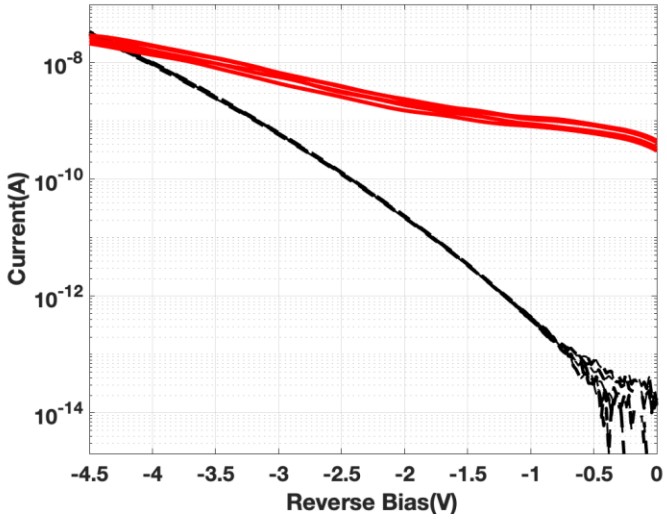

Figure 2.5 DC dark current and photocurrent with the incident light from a 639 nm laser.

The experimental setup for AC device characterization is shown in Fig. 2.6. The setup consists of two parts in general: the illumination system and the signal collection system. For the illumination system, the incident light is provided by a laser diode controlled by a laser driver. A function generator is connected to the laser driver to modulate the waveform during AC measurements. The optical fiber of the laser is connected to a convex lens to focus the laser beam onto the device. The position of the convex lens is flexible in order to adjust the dimension and focus of the beam spot to the sample. There are two beam splitters to both align the laser beam to

the device under test (DUT) and CCD camera as well as transmit the image of devices on the sample to the camera. The objective lens is set up above the sample to magnify the device and further focus the beam spot. The objective lens can be easily changed to another one with a different magnification if needed. The whole illumination system sits on an XYZ positioner. During measurement, one can visualize the devices of the sample, the beam spot on the device, and the probe from the computer connected to the camera. Thereby, one can adjust the beam spot size, align the beam spot to the device photosensitive area, locate and probe the device via this illumination system.

For the signal collection system, a GSG probe in contact with the device cathode and anode is connected to a bias Tee. The DC port of the bias tee is connected to a 200 kΩ resistor and a source meter to apply bias. The AC port of the bias Tee is connected to a low-noise amplifier (LNA) with a 30 dB gain and an RF spectrum analyzer. The incident light is provided by a 639 nm wavelength diode laser modulated at different frequencies sinusoidally by a function generator. At room temperatures, we can measure the bias dependent photoresponse of the device under different applied bias voltages at certain frequencies using an RF spectrum analyzer with 1 Hz resolution bandwidth. The AC gains are still defined the same as those for DC characterization, $I(V_{app})/I_0$.

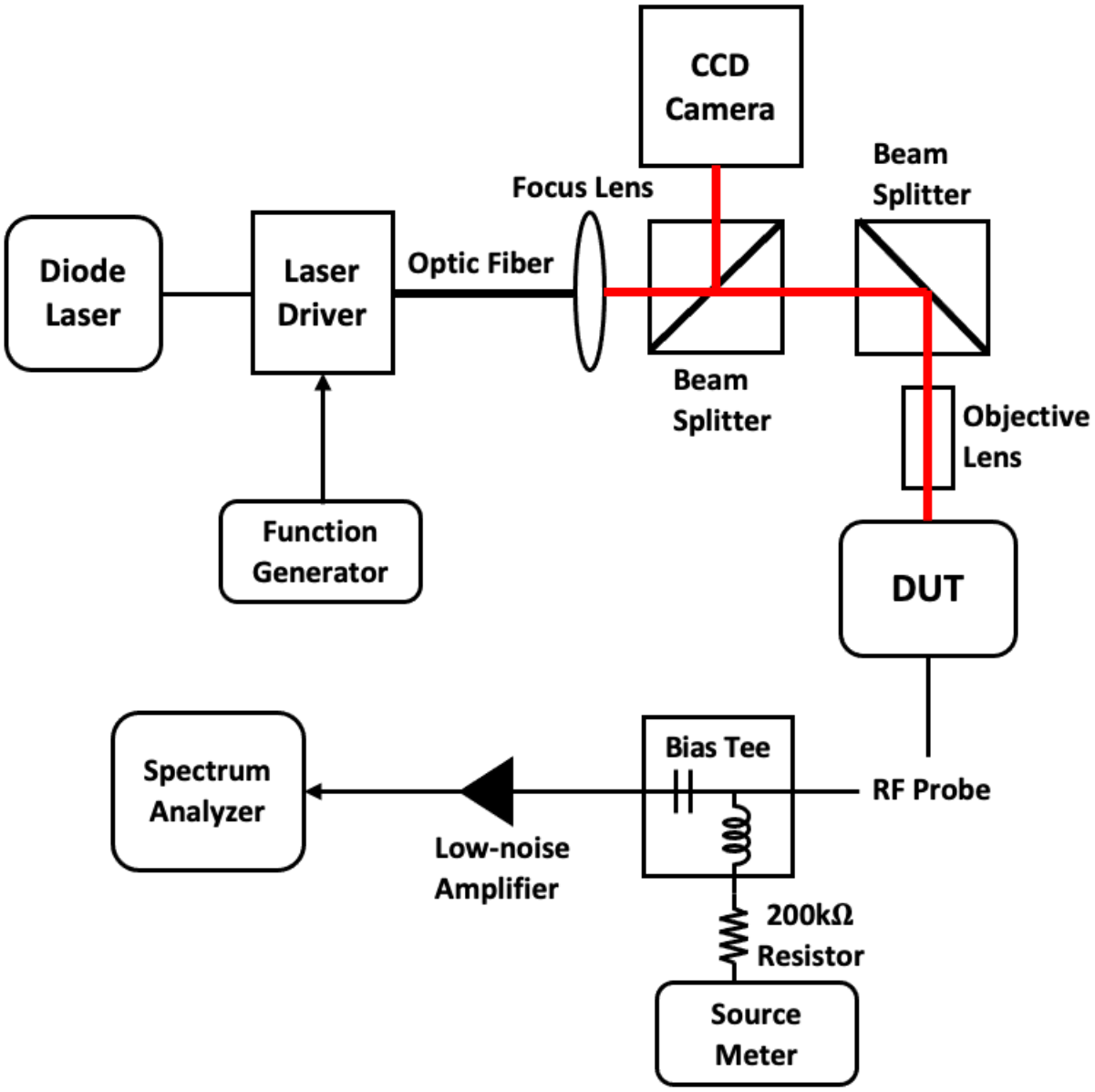

Figure 2.6 Experimental setup for AC characterization at room temperature.

The AC signals are read from the RF spectrum analyzer in the unit of dBm. The reading is then converted to I_{rms} and shown in Fig 2.7(a). Thereby, the corresponding AC gain can be calculated, as shown in Fig 2.7(b). The incident power at these three frequencies is measured to have some difference. This is due to the difference in the waveform generated by the function generator. Nevertheless, the primary quantum efficiency calculated at -1 V is consistent for

different frequencies. We can see that the gain of the device from -1 V to -5 V is also consistent along frequencies.

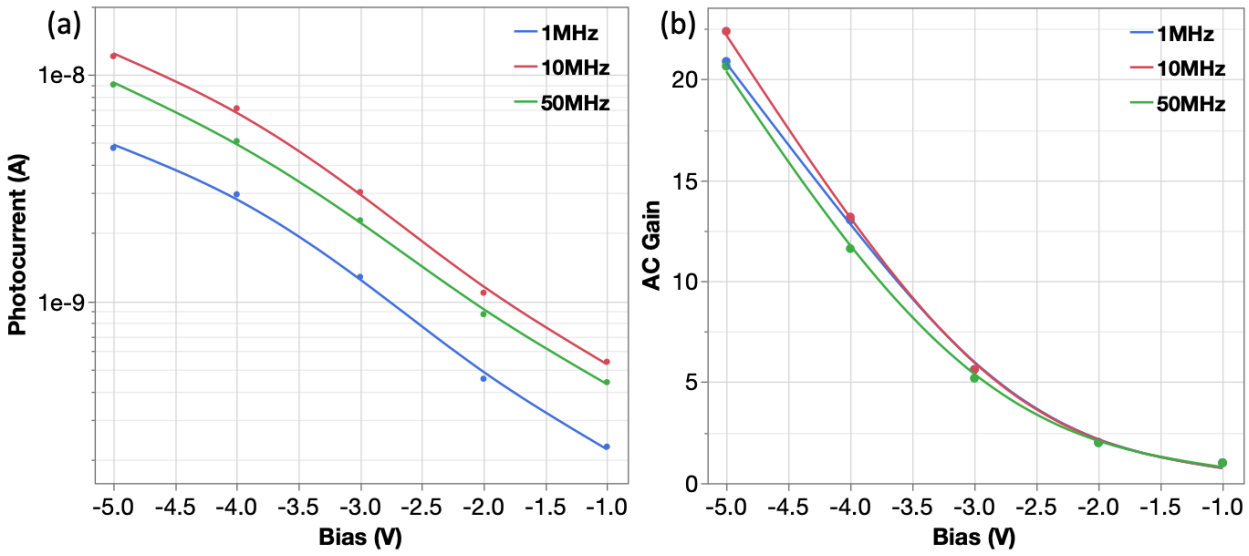

Figure 2.7 AC characterization at room temperature: (a) photocurrent (I_{rms}) and **(b)** gain at 1 MHz, 10 MHz and 50 MHz from -1 V to -5 V.

2.3 Dark Current Reduction in a-Si CEP Detectors

2.3.1 Mechanism

Dark current is a crucial parameter for a single photon detector since the amount of dark current determines the on/off ratio of the signal or the sensitivity of the device. In the a-Si CEP detector, there are many possible paths for its dark current. Fig. 2.8(a) shows the three main paths of dark current in an a-Si CEP detector for both electrons and holes. The curvy path represents thermionic emission, which is dependent on the temperature. The two-step path represents the defect assisted indirect tunneling (Poole-Frenkel effect). The straight path represents the Fowler-Nordheim direct tunneling.

The energy barrier for electrons, ϕ_e, is 0.7 eV, while the energy barrier for holes, ϕ_h, is 1.55 eV. The lower the barrier, the more easily the electrons or holes can transport. Compared with

the barrier height for hole transport, the lower barrier height for electron transport is a more critical parameter for the a-Si CEP detector. In this case, in order to reduce the dark current of the device, an approach can be introducing another layer to increase the electron transport barrier, as shown in Fig. 2.8(b). An extra layer is introduced between a-Si and ITO. There should be two basic requirements for the extra layer: first, the conduction band edge, E_c, of the extra layer is higher than (less negative in a band diagram) that of the a-Si so that a higher energy barrier can be created to block the dark current; and second, the valence band edge, E_v, of the extra layer is also higher than (less negative in a band diagram) that of the a-Si so that the photocurrent with the CEP gain will not be blocked, as shown in Fig. 2.8(c). As shown in Fig. 2.8(c), the electrons after multiplication in the a-Si layer travel along the a-Si into the n-Si substrate to be collected and won't see the extra layer at all. Similarly, the holes after multiplication in the a-Si layer travel along the a-Si into ITO. Even though the holes go through the extra layer, they won't experience any energy barrier in the process. Hence, the idea is that the extra layer can block a substantial part of dark current without affecting the photocurrent and CEP gain.

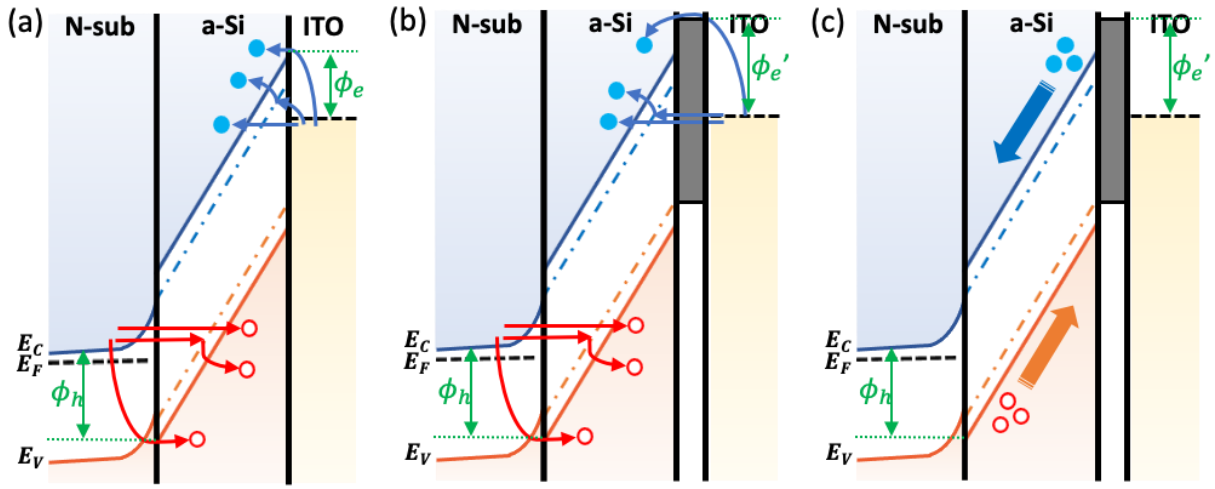

Figure 2.8 (a) Dark current paths in the a-Si CEP device; **(b)** An extra layer to block electron transport paths; **(c)** Electrons and holes after multiplication in a-Si can transport as normal without seeing an extra barrier after inserting the extra layer.

2.3.2 Cu_2O and SnO_x

There are many metal oxides reported to match the requirements of this approach for dark current reduction: Cu_2O, NiO, MnO, SnO_x and so on. The two of the metal oxides I demonstrate in this section are Cu_2O and SnO_x. The electron affinity of Cu_2O is reported to be -3.2 eV and its band gap is 2.1 eV, which can increase the electron transport barrier from 0.7 eV to 1.3 eV without blocking the photocurrent [9]. The other material, SnO_x, is very interesting and reported to vary its electron affinity and band gap depending on the deposition condition, annealing condition, composition and even thickness [10,11,12]. The device structure with the additional metal oxide layer is shown in Fig. 2.9.

The process flow of the device is very similar to that of the standard a-Si CEP device, except performing three more steps after the oxide opening step (etching SiO_2 and Al_2O_3 by BOE). After opening the oxide for the top and ground electrode, the first additional step is photolithography for the metal oxide layer on the top electrode. The pattern of the metal oxide layer is a little larger than the top electrode opening so that it can cover the entire active region of the device. The second additional step is metal oxide deposition: 40nm Cu_2O or 10nm SnO_x by pulsed laser deposition (PLD) and lift-off. The third additional step is annealing. For Cu_2O, the annealing condition is 10 hrs. at 200 °C in ambient and for SnO_x, the annealing condition is 30 min at 260 °C in vacuum RTA chamber. After annealing, the samples continue to two photolithography steps and two depositions by sputtering for the ITO top electrode and Ti/Au contact pads, which are the same steps as the standard a-Si CEP device.

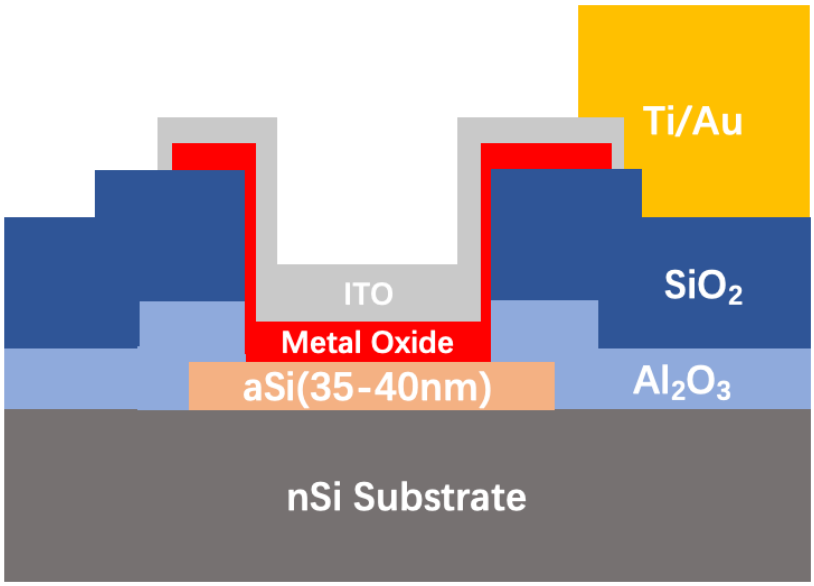

Figure 2.9 Cross-section structure of the a-Si CEP device with a metal oxide layer.

The measurement data is demonstrated in Fig. 2.10 (a,b,c): dark current (black) and photocurrent (red) for the standard 35~40 nm a-Si CEP device (a) without any metal layer; (b) with 40 nm Cu_2O; and (c) with 10 nm SnO_x. The incident light is provided by a 639 nm laser diode with the power of around 160 nW. The photocurrent is the difference between light on current and dark current. Each curve represents IV characteristic for one device. The data is collected by Agilent B1500A which has a noise floor between 10 fA and 100 fA. The data shows that at the bias voltage of -4.5 V, the device with a 40 nm Cu_2O layer has a lower dark current level than the one without the metal oxide for about one order of magnitude, and the device with a 10 nm SnO_x layer has an even lower dark current level that is almost four orders of magnitude lower than the device without metal oxide. Furthermore, by comparing all the three photocurrent, one can see that the devices with either metal oxide layer can achieve the same level of photoresponse as the device without the layer. This experiment proves that this approach of inserting an extra layer with the desired band structure as described to reduce dark current does work well for the a-Si CEP detector.

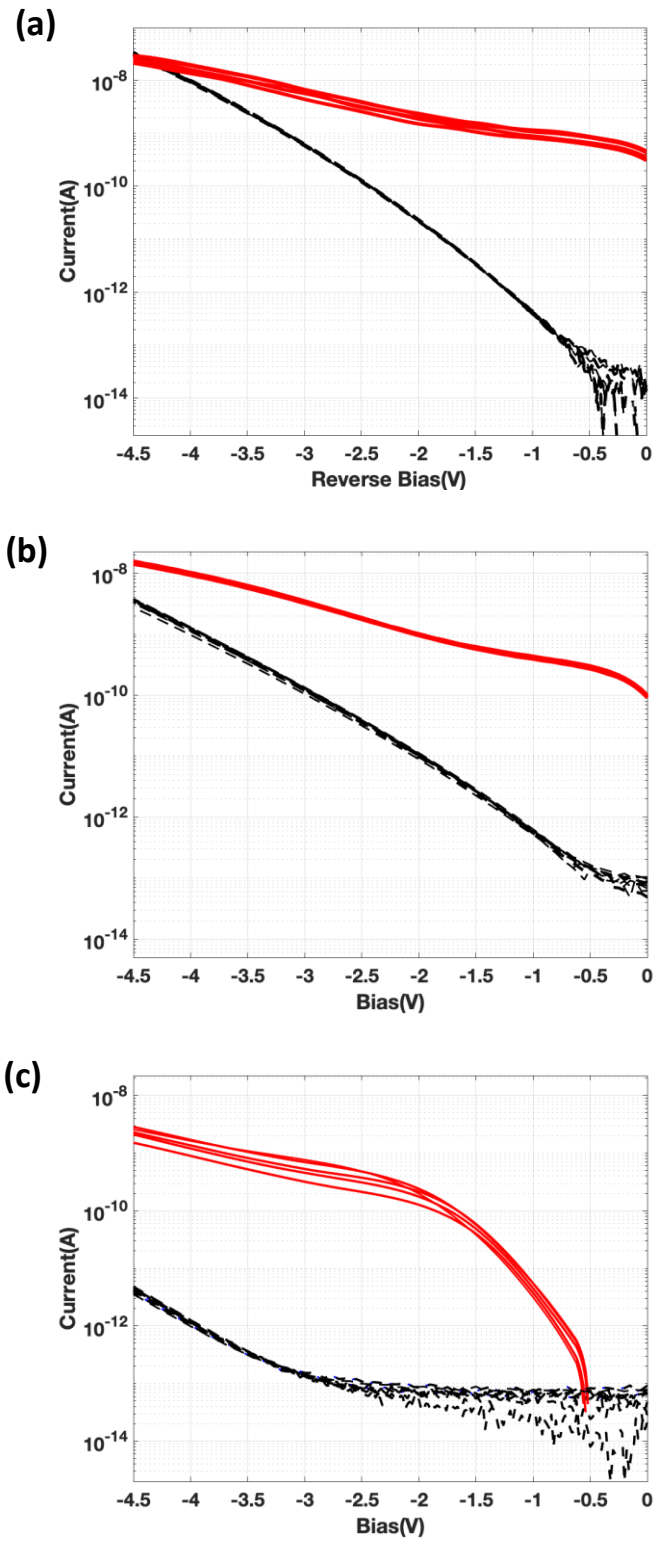

Figure 2.9 Dark current and photocurrent (each curve represents one device) of (a) 35~40 nm a-Si CEP devices; **(b)** 35~40 nm a-Si CEP devices with Cu2O; **(c)** 35~40 nm a-Si CEP devices with SnO_x.

2.4 Integrated CEP Detectors

From section 2.3, we can see one of the advanced characteristics of the CEP detectors is easily compatible with other materials/layers in fabrication. In the last section, we have talked about the metal oxide layers compatible with CEP detectors to reduce dark current. In this section, we will take a look at how CEP detectors can be integrated with other materials to improve the performance of the detector or to facilitate certain applications.

Fig. 2.11 (a,b) shows the structures of two CMOS compatible vertical junction field effect transistors (JFET): (a) NPN JFET and (b) PNP JFET. In the vertical NPN JFET structure, the fixed positive charges in the SiO_2 passivation layer can induce negative charges at the interface of p-Si and SiO_2 and thereby create an inversion channel, which then establishes the n-channel JFET as shown in the circuit diagram. The JFET works together with two back-to-back diodes to generate gain for the detection. Similarly, in the vertical PNP JFET structure, the Al_2O_3 passivation layer can induce positive charges at the interface of n-Si and Al_2O_3 and thereby an n-channel JFET can be created. These vertical JFETs were originally designed as an approach to a high-density retina prosthesis. Al_2O_3

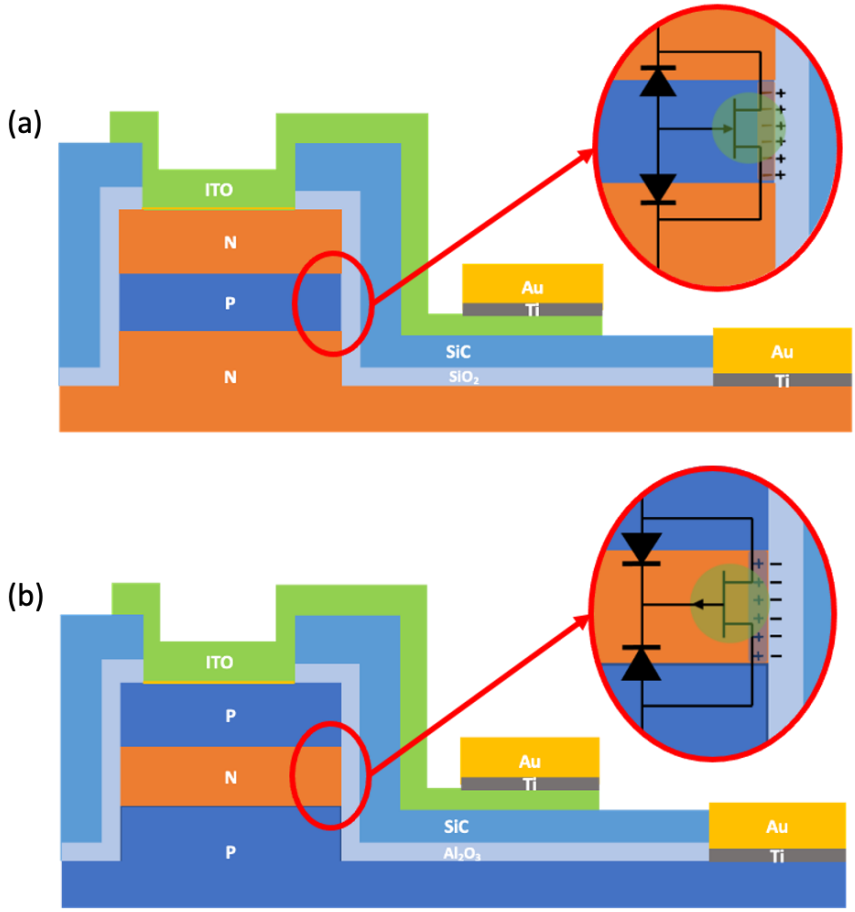

Figure 2.10 (a) A novel design of vertical NPN JFET device; **(b)** A novel design of vertical PNP JFET device

The performance of the NPN JFET is shown in Fig. 2.12 (a,b,c) for dark and light on current, responsivity and detectivity, respectively. A laser diode with the wavelength of 518 nm provides the incident light to the device with three orders of magnitude difference in power between 16 pW and 13 nW. The responsivity, R, is calculated as: $R = (I_{Light\ on} - I_{Dark})/Incident\ Power$

The detectivity, D*, is calculated as:

$D* = R/\sqrt{2\,q\,J_{Dark}}$ where q is the elementary electric charge and J_Dark is the dark current flux:

$J_{Dark} = I_{Dark}/A$ where A is the area of the device.

From the measurement data, we can notice that the device has a higher responsivity at a lower power and the dimmest light it can have a clear response is at the level of 16 pW.

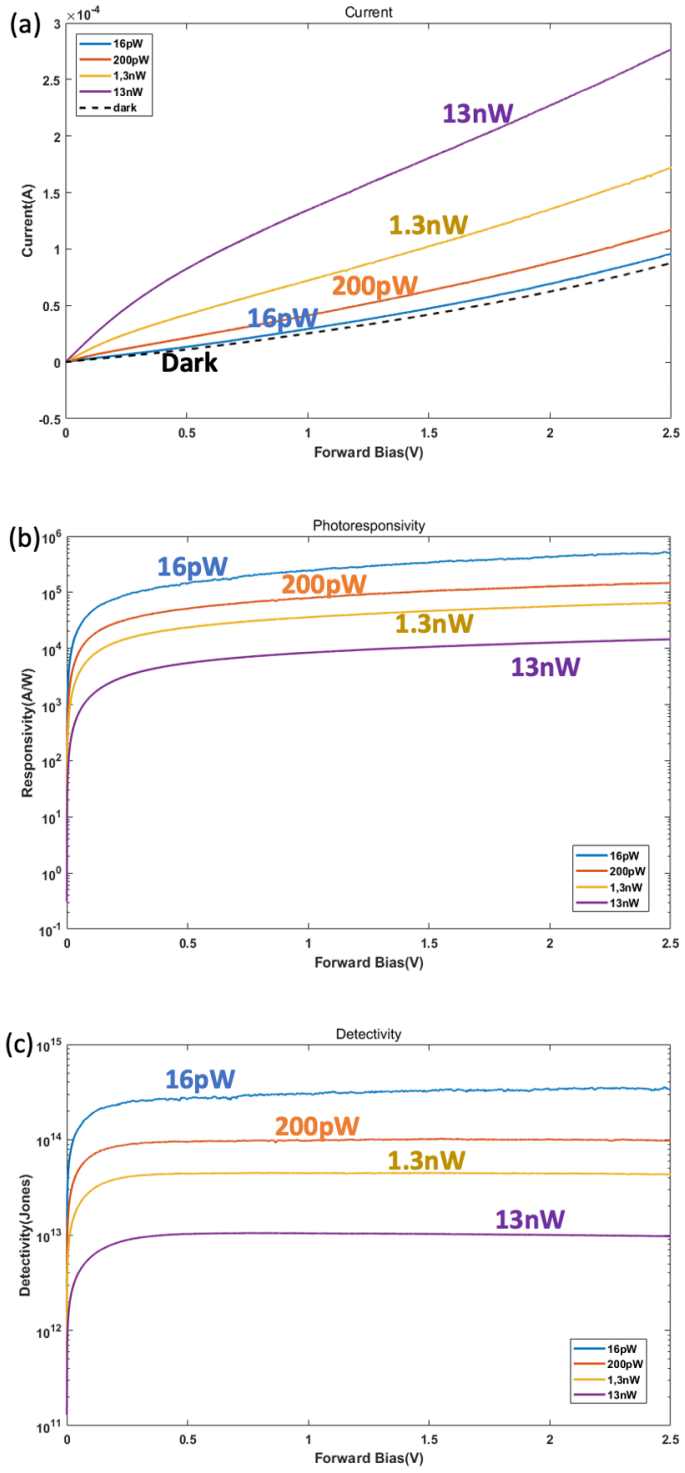

Figure 2.11 Characterization of the vertical NPN JFET: (a) Dark and light on current (A); **(b)** Photo responsivity (A/W); and **(c)** Detectivity (Jones) for different levels of incident laser power with the wavelength of 518 nm.

The characterization of the vertical PNP JFET is shown in Fig 2.13 (a,b,c) for dark current and light on current (A), photoresponsivity (A/W) and detectivity (Jones). The calculation is the same as shown above for the NPN JFET. From this set of measurements, we can see that the PNP JFET has the similar trend in responsivity as the NPN JFET: higher responsivity at lower power. However, this PNP JFET has better performance at lower power compared to the NPN JFET and the dimmest power it can detect can achieve as low as 2 pW, more sensitive than the NPN JFET. The overall best detectivity the PNP JFET can reach is also higher than that of the NPN JFET.

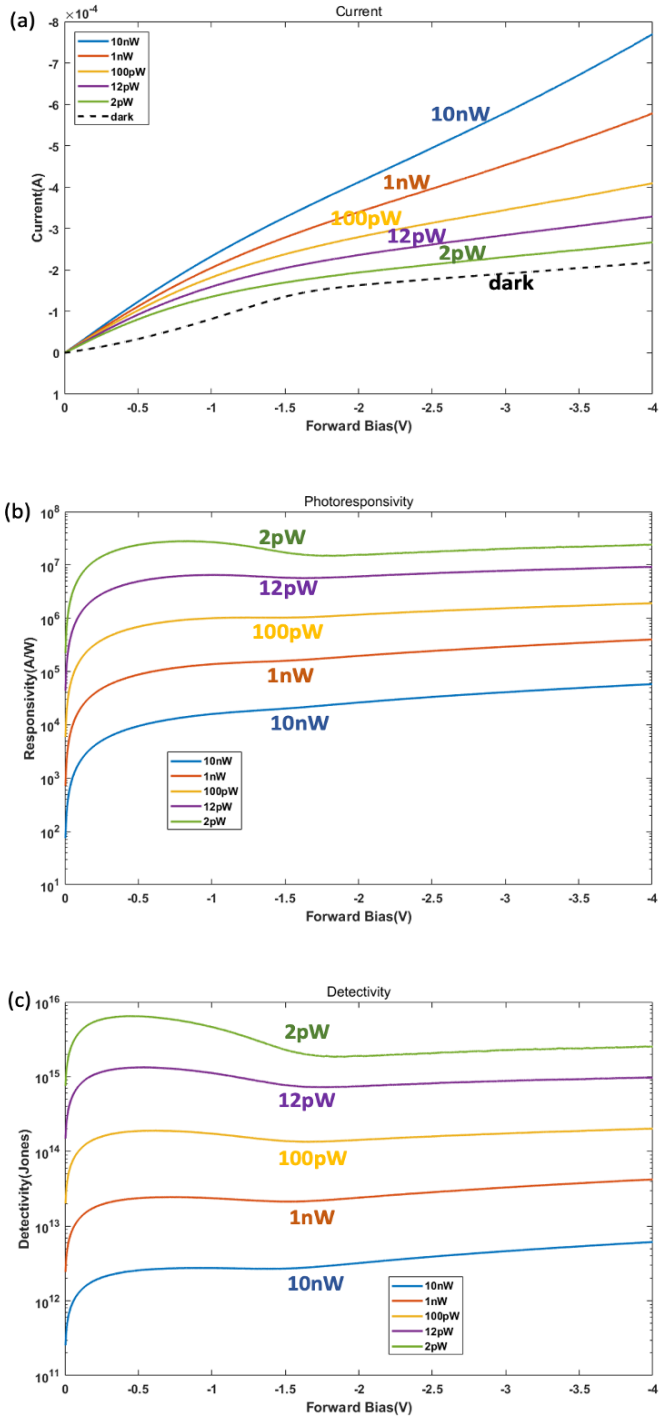

Figure 2.12 Characterization of the vertical PNP JFET: (a) Dark and light on current (A); **(b)** Photo responsivity (A/W); and **(c)** Detectivity (Jones) for different levels of incident laser power with the wavelength of 518 nm.

From the measurement, we can observe that the JFET device has good sensitivity but suffers from very high dark current. This will degrade the image contrast for a retinal prosthesis.

In order to improve the design, we would like to design a third electrode to control the channel to the optimal degree of on/off. Since the photoresponse will also be affected by the channel control, we would like to integrate the CEP detector to improve the gain and create a heterojunction to have positive feedback to modulate these two gain mechanisms. The device structure is shown as Fig. 2.14.

In order to fabricate the device, the first step is to clean the PNP Si Epi by solvents and remove the surface native oxide by HF dip. Afterwards, a 30 nm a-Si layer is deposited on the top by PECVD with the same recipe as the standard a-Si CEP detector. Then, a 200 nm SiO_2 layer is deposited onto the a-Si as the etching mask in the later steps. Then, a photolithography step is performed to pattern the SiO_2 mask which will be dry etched by ICP-RIE etch. With the patterned mask, the a-Si and PNP mesa is wet etched by TMAH solution at 80 °C. The wet etch step is introduced specifically for this structure to replace the dry etching mesa step for other structures in order to minimize the sidewall damage by the dry etch plasma, because experiment in parallel shows that the sidewall damage highly affects the channel induced for the JFET. The total mesa height is about 1700 nm. Then the SiO_2 mask is removed by BOE, and the sidewall is cleaned by RCA clean. A 40 nm Al_2O_3 passivation layer is then formed by ALD. Next, another photolithography step is performed for the third electrode. A 60 nm Ti/Au is deposited by sputtering and then lifted-off to form the third electrode. Afterwards, the second passivation layer, 200 nm SiC, is deposited by PECVD, followed by the third photolithography to pattern the SiC. The photoresist of this step is the mask for dry etching the SiC layer. The dry etch step is for all the three electrodes: top, ground and the third, and purposely over etched into the Al_2O_3. This step is very critical: the etch must be stopped within the Al_2O_3 layer to completely etch the SiC as well as not touch the a-Si layer underneath. After that, the rest of the Al_2O_3 layer is etched away by

BOE. At last, the other two photolithography steps and two depositions are performed for the ITO top electrode and the contact pads for all the three electrodes, similarly as that performed to the standard a-Si CEP device stated previously.

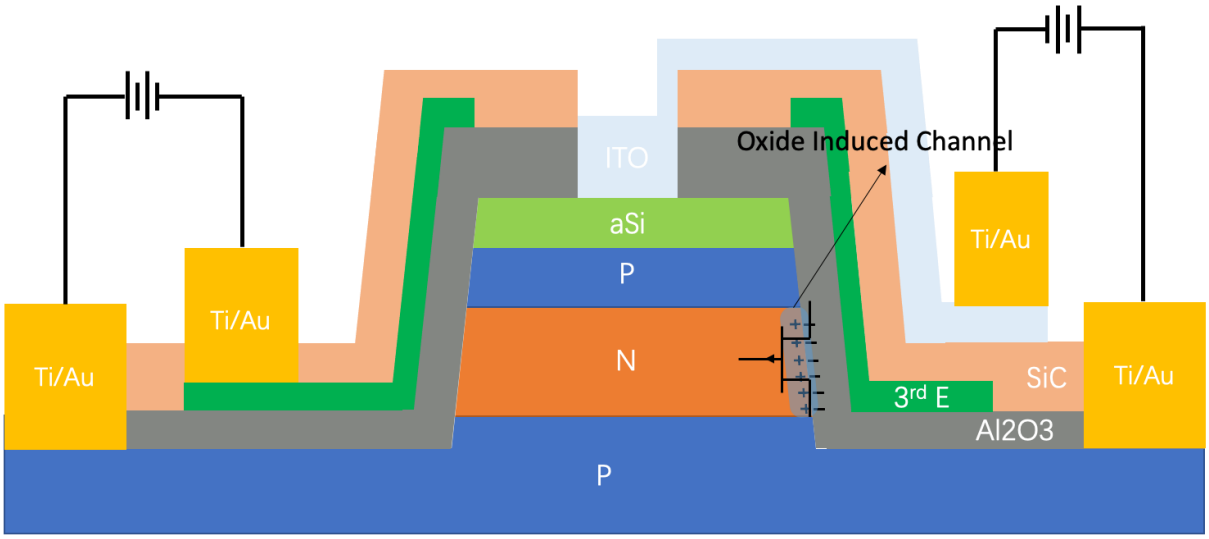

Figure 2.13 Device structure of integrated PNP JFET and CEP detector with the third electrode to control the p-channel.

The characterization of the device is shown in Fig. 2.15 (a,b) at two levels of incident power: 0.5 nW and 50 pW. One can see that by the design of the third electrode, we can control the degree of the channel on. Furthermore, the dark current is reduced about four orders of magnitude compared to the previous two JFETs and can be controlled by the gate electrode. This reduction is mainly due to the change of etch method for the mesa. The damage of wet etch is much less than the dry etch.

In this integrated device, the incident light can be absorbed in both the a-Si layer and the top reverse biased pn junction. The CEP gain by the 30 nm a-Si as well as the photocurrent from the top diode can work together to induce higher voltage across the bottom diode. This induced voltage also modulates the JFET together with the third electrode. The JFET can thereby achieve a higher photoresponse due to both modulations. In the other words, the JFET can give positive feedback to the CEP gain induced voltage. After that, the higher photocurrent generated by the

JFET will later go through the a-Si CEP layer and experience a further amplification. Thus, when the CEP detector is integrated with the JFET in this dual gain design, these two amplification mechanisms not only add gain together but also give positive feedback to each other in the loop. One can see that by applying -2 V of gate to source bias, the photoresponse can increase almost three orders of magnitude with the same incident light. In the real applications, this character is very useful for low illumination power.

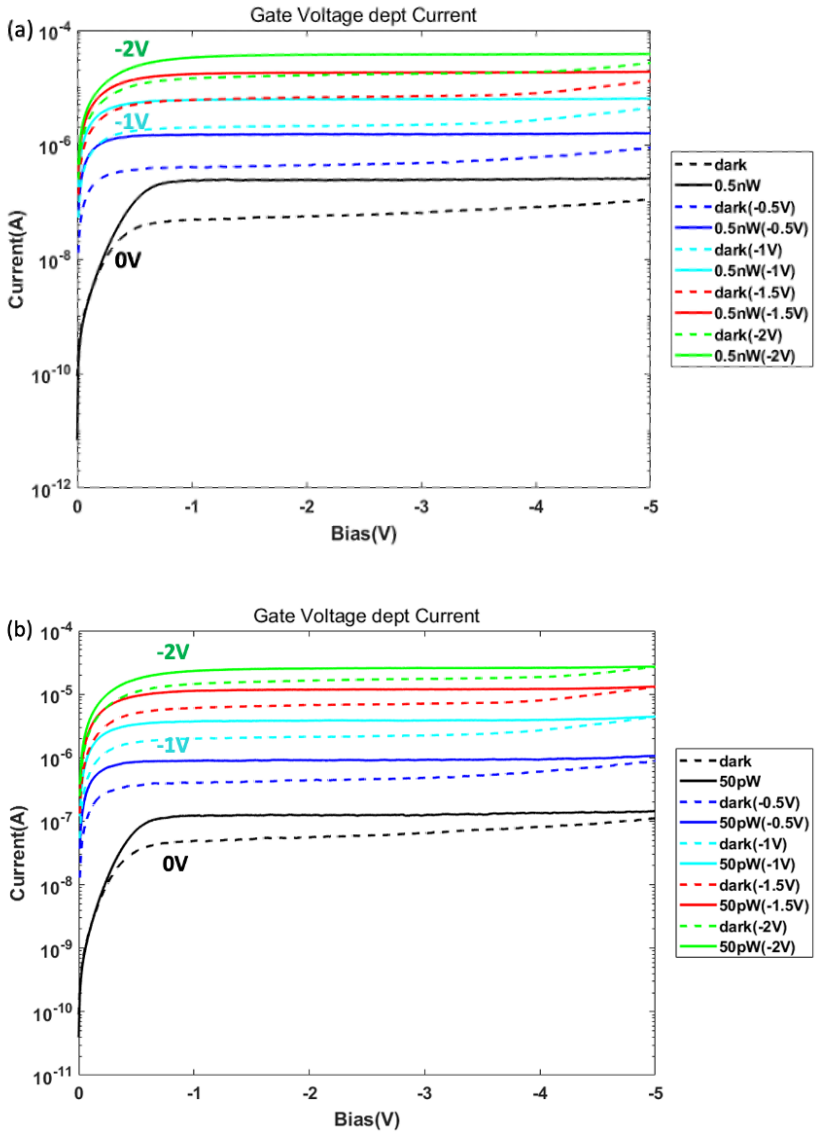

Figure 2.14 (a) Dark current and photoresponse of 0.5 nW incident light; **(b)** Dark current and photoresponse of 50 pW incident light with different gate bias to the third electrode.

In this part, I have demonstrated the work of integrated CEP detectors. The CEP mechanism with naturally decent gain can easily improve the performance of another gain mechanism. The a-Si CEP detector has high compatibility with other devices due to its easy formation process. Furthermore, the a-Si CEP detector has the potential to be compatible with CMOS processes with a low cost, which makes this device even more attractive.

Portions of Chapter 2 include unpublished work on dark current reduction of the a-Si CEP detector by metal oxides, with the efforts of **Zhou, J.**, Yu, Y., Chiu, S.Y., Nomura, K., and Lo, Y.H, and integrated CEP detectors based on the designs of incorporating JFET with a-Si, with the efforts of Zhou, J., Liu, Y.H., Damle, S., and Lo, Y.H. The dissertation author is the primary investigator of the project.

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Chapter 3. Temperature dependent Characterization and analysis of CEP

3.1 Design of Experiments

As mentioned before, temperature sensitivity of gain and breakdown voltage has become a critical concern for focal plane arrays or single photon detector arrays. In all the frameworks on CEP detectors, one significant question is the performance of CEP detectors with respect to temperature changes. In this section, I will demonstrate the investigations on temperature sensitivity of the standard a-Si CEP detectors and the feasibility of athermalized CEP detectors over a wide temperature range for practical applications.

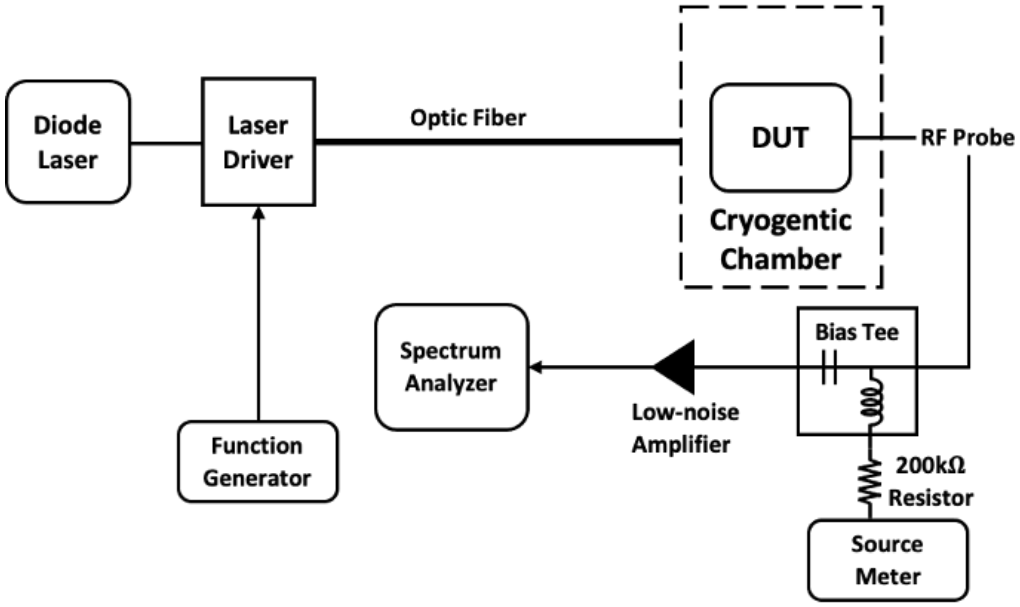

Figure 3.1 Experiment setup for characterization of temperature dependent performance of CEP detectors.

The experimental setup for temperature dependent device characterization is shown in Fig. 3.1. The device was measured in a cryogenic chamber under vacuum between 200 K and 350 K. A GSG probe is probing on the device electrodes: top and ground. For DC characterization, the probe is directly connected to a source meter to apply bias and read the DC current signals. For AC characterization, the probe is connected as the setup for room temperature measurement, to a

bias Tee first. Then a 200 kΩ resistor is connected to the DC port of the bias tee and a source meter followed in the circuit to apply bias. The AC port of the bias Tee is connected to the same LNA with a 30dB gain to amplify the signal from the device and the RF spectrum analyzer to read out the voltage signal. A 639 nm wavelength diode laser applies incident light that is modulated in a sinusoidal waveform at 1 MHz, 10 MHz, or 50 MHz by a function generator.

At given temperatures in the range between 200 K and 350 K, the bias dependent performance of the device at a bias voltage up to -5 V over these frequencies has been characterized using the RF spectrum analyzer with 1 Hz resolution bandwidth. The device for this temperature dependent measurement is still the standard structure: it consists of a thin (35~40 nm) a-Si layer as the gain medium and n+ Si as the light absorption layer. The power of incident light into the device for each single measurement is carefully controlled in a similar amount: the primary photocurrent is all around 100~110 pA at all temperatures.

3.2 Experiment Result and Discussion

Figure 3.2(a) shows the gain calculated from measured photocurrent as a function of temperature at 50 MHz. Each data point represents the photocurrent gain of a device at a certain temperature and applied bias and three devices are measured for each bias and each of the temperatures. The line for each applied bias is a semi log fit performed to $\ln(Gain)$ as a function of temperature, giving the trend in temperature dependence at each bias. Figure 3.2(b) shows the normalized photocurrent gain as a function of temperature. The gain at each temperature was normalized to the gain at 300 K for each applied bias.

From Fig. 3.2, by comparing the trend lines at different applied biases, one can observe that, at lower bias (up to -4 V), there was a trend of slight increase of gain with increasing temperature. When the magnitude of the applied bias in the a-Si multiplication layer was high

enough (e.g., -5 V), the photocurrent gain became almost temperature independent. Furthermore, the slope of each line indicates the strength of temperature dependency at a given bias. There is a clear trend of decrease in the temperature dependence with increasing reverse bias, i.e., the dependence at higher reverse bias is clearly weaker than that at lower reverse bias.

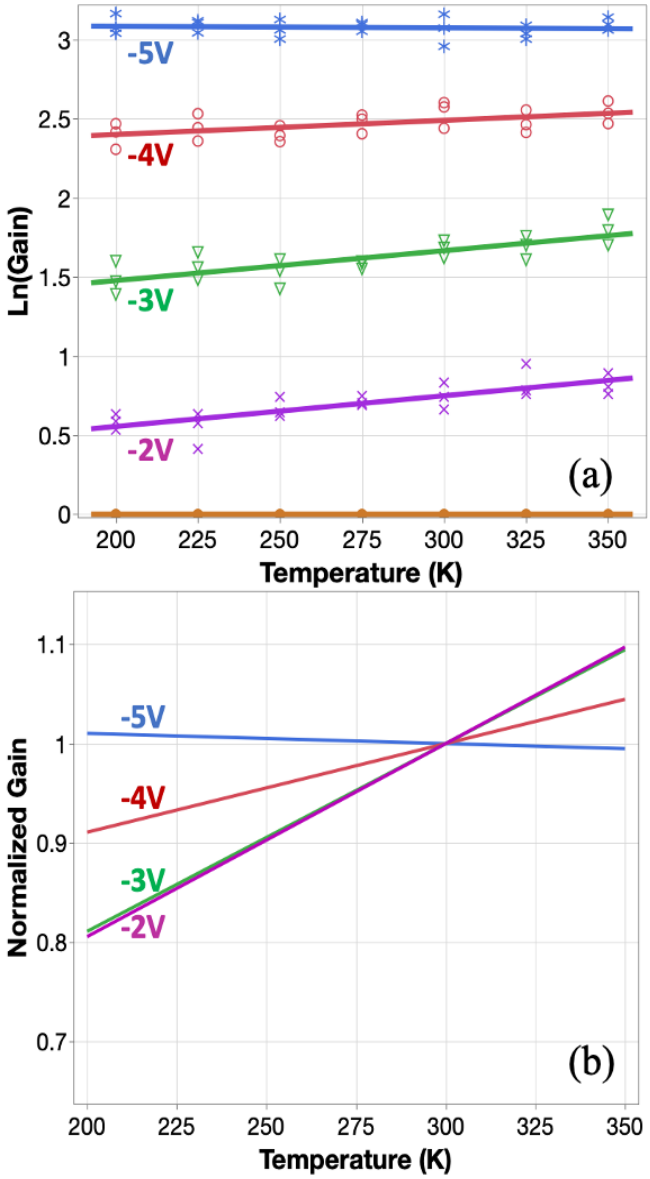

Figure 3.2 (a) Temperature dependent gain measured at 50 MHz and different applied biases; **(b)** Normalized gain at -2 V, -3 V, -4 V and -5 V bias. The gain at each bias was normalized to the gain at 300 K.

Figure 3.3 shows the device gain as a function of the applied bias at 200 K (blue) and 350 K (red) at three different frequencies: 1 MHz, 10 MHz and 50 MHz. Each dot in Fig. 3.3 is the mean value of three measurements and the error bar is the standard deviation. The device shows consistent bias dependent performance over the frequency range of measurement. One can see that the results of temperature dependent measurement are consistent with that of previous room temperature measurements.

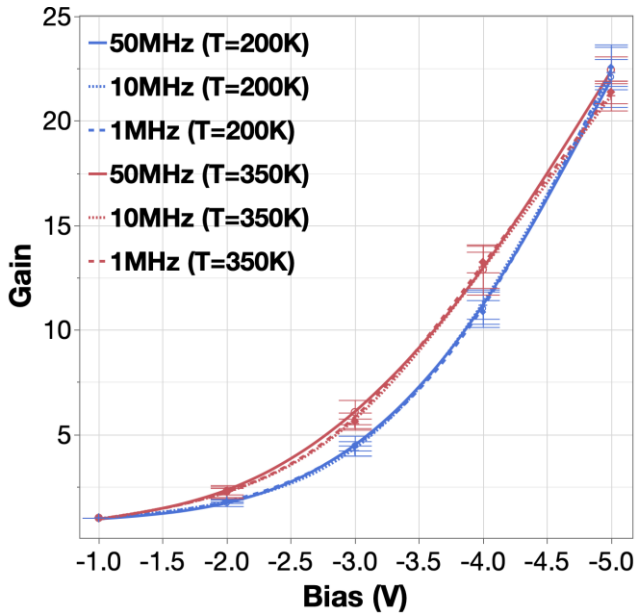

Figure 3.3 Device gain vs. applied bias at two temperatures: 200 K and 350 K and three frequencies: 1 MHz, 10 MHz and 50 MHz.

Temperature dependence of breakdown voltage (V_{bd}) is a key parameter for single photon detectors in Geiger mode. The dark count rate and photon detection efficiency are sensitive to the overbias (i.e., bias above the breakdown). Hence, any change of breakdown voltage with temperature can cause significant device performance variations, especially in a single-photon detector array.

To measure the breakdown voltage, the reverse bias was increased gradually to the value where the gain of the device increased rapidly. We then recorded the breakdown voltage to study

the temperature dependence of the breakdown voltage. Figure 3.4 shows the avalanche breakdown voltage from 200 K to 350 K under 639 nm wavelength illumination. Overall, the breakdown voltages lie between -6.5 V and -6.8 V over a temperature range of 150 K. In contrast to conventional silicon avalanche photodiodes where the breakdown voltage increases with temperature, the breakdown voltage for CEP detectors decreases slightly as temperature rises, which suggests that phonon assisted excitation plays a more significant role than phonon scattering in the cycling excitation process.

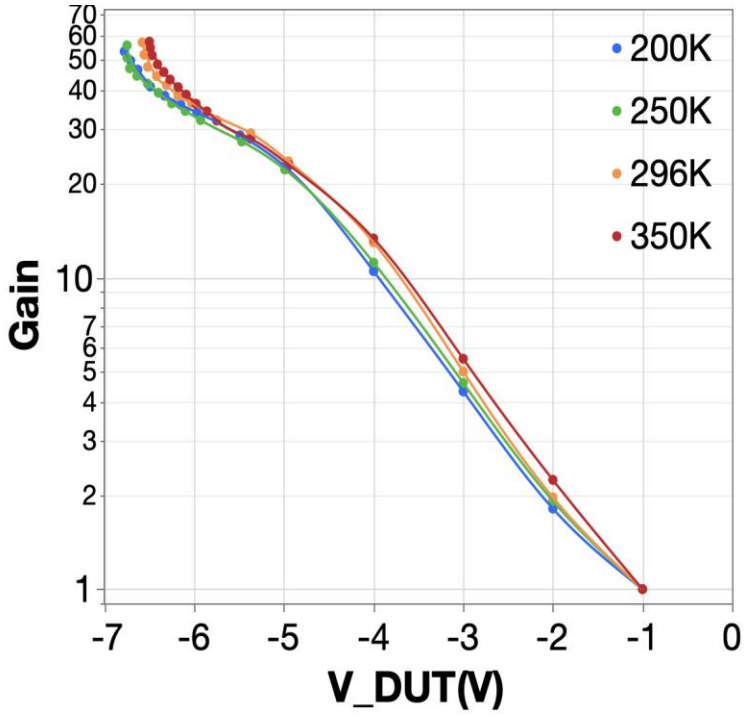

Figure 3.4 Gain vs applied bias at 200 K, 250 K, 296 K, and 350 K. The measurements reach the point close to device breakdown to enable us to extract the breakdown voltage at different temperatures.

People often use breakdown voltage temperature coefficient ($\boldsymbol{\Delta V_{bd}/\Delta T}$) to quantify temperature sensitivity of breakdown voltage. The breakdown voltage temperature coefficients of many common APDs based on different materials, including InAlAs, InP, GaAs, AlInP and Si, as the carrier multiplication layer, are collected in Fig. 3.5 [1-6]. The coefficient of the CEP detector

is also included in the figure. From our experimental result, the coefficient, $\boldsymbol{\Delta V_{bd}/\Delta T}$, for a-Si CEP devices is calculated around -2 mV/K. The magnitude of the value for the CEP detectors is significantly greater than most of the existing APDs. This result strongly suggests that under high applied E-field and high gain value, field-enhanced tunneling becomes the dominant effect to excite the localized electrons (holes) into the mobile bands. The opposite sign of coefficient for the CEP detector to the conventional silicon detectors also reveals the significant difference in mechanisms between CEP and typical impact ionization.

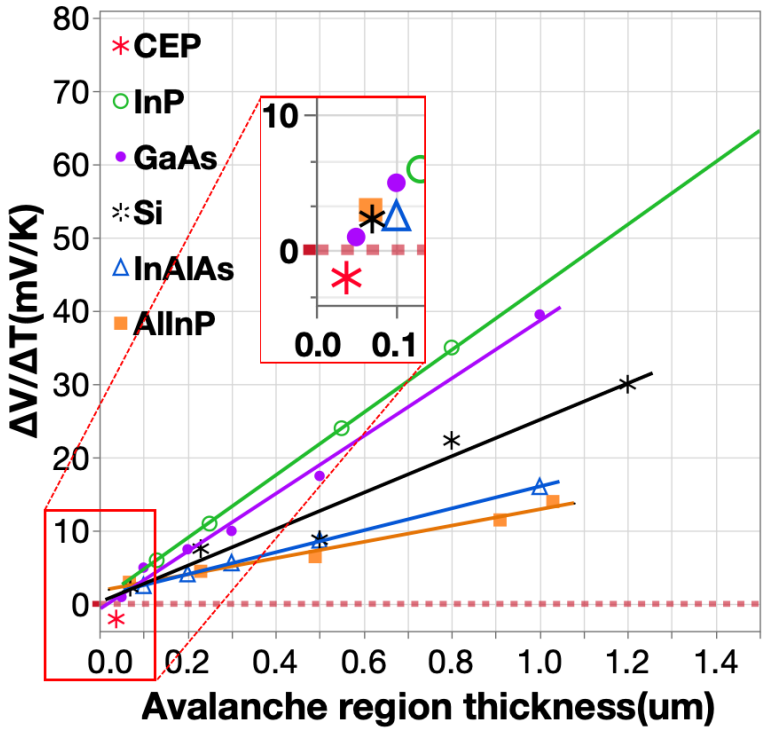

Figure 3.5 Dependence of breakdown voltage temperature coefficient, $\boldsymbol{\Delta V_{bd}/\Delta T}$, on the thickness of carrier multiplication region for CEP detectors (red star) and APDs having different carrier multiplication materials: InP, GaAs, InAlAs, AlInP, and Si reported in other works [1-6].

Through the temperature dependent measurement, the athermalized CEP detectors in a temperature range from 200 K to 350 K have been demonstrated. one can see that under low applied bias, the CEP detectors show some temperature dependent CEP gain over the frequency

range between 1 MHz and 50 MHz. As the applied bias voltage increases and CEP gain reaches a higher value, the temperature dependence of gain decreases with increasing temperature and eventually the CEP gain becomes nearly temperature independent. Furthermore, based on the temperature dependent breakdown voltage measurement, the breakdown voltage of the device shows much less temperature dependence compared with conventional APDs.

In Chapter 2, I have shown the CEP multiplication process in the device band diagram. One can recall that there are two mechanisms that possibly contribute to the step of excitation of the electrons/holes from the localized states to mobile states: field-enhanced tunneling and phonon assisted excitation. From the evidence of the weak temperature dependence of CEP gain and breakdown voltage in the temperature dependent measurements, we can get the indication that the effect of field-enhanced tunneling of localized electrons/holes into the mobile bands is the dominant factor over the phonon assisted excitation under high electric fields. Based on this observation, we can develop methods to quantify the relative importance of field-enhanced tunneling and phonon excitation.

3.3 Physical Model

We assume that the probability of phonon assisted excitation increases as temperature increases while the probability of field enhanced tunneling is insensitive to temperature increases but increases as the electric field increases. Here we can propose a model to elucidate the observed temperature dependence of CEP mechanism and develop a method to quantify the relative importance of phonon assisted excitation and field-enhanced tunneling in excitation of localized carriers into mobile bands to sustain the carrier multiplication process, by relating the ratio of probability between phonon assisted excitation and field enhanced tunneling to the experimental data.

From the previous measurement, the data shows that the temperature dependence of gain decreases with increasing bias voltage and eventually becomes nearly temperature independent when the bias voltage reaches -5 V, corresponding to an electric field of around 1.2 MV/cm. This implies that under a strong enough electric field, field enhanced tunneling is the dominant mechanism for excitation of the localized carriers in the band tails into the mobile bands.

To model the CEP gain, we assume the number of electron-hole pairs created by an energetic electron or hole in the *i-th* cycle is X_i and Y_i, respectively. Hence, the primary energetic carriers generated by the incident photon can be denoted by "0". Then, primary energetic carriers enter the a-Si multiplication region and initiate the first cycle of CEP and create electron-hole pairs that can be denoted by "1". The expression of the CEP amplification factor, G_{CEP} , can be represented as

$$G_{CEP} = 1 + Y_0 + Y_0X_1 + Y_0X_1Y_2 + Y_0X_1Y_2X_3 + \cdots \tag{3.1}$$

where Y_0 is the number of the primary photogenerated holes in n-Si.

For all X's and Y's, their mean values are represented by

$$\langle X_i \rangle = x \ (i = 1,2,3,\dots)$$

$$\langle Y_i \rangle = y \ (i = 1,2,3,\dots)$$

Treating all X's and Y's to be independent random variables, we obtain the mean value of the multiplication factor:

$$G = \frac{1+y}{1-xy} \tag{3.2}$$

Since the CEP mechanism is a two-step process consisting of generation of localized e-h pairs by energetic carriers and excitation of localized carriers to their respective mobile bands, we can represent x and y by the following relations:

$$x = M_e(V)\left[P_p(T) + P_{pt}(T,V) + P_t(V)\right] \tag{3.3}$$

$$y = M_h(V)\left[P_p(T) + P_{pt}(T,V) + P_t(V)\right] \quad (3.4)$$

$M_e(V)\ and\ M_h(V)$ are the average number of the localized e-h pairs produced by an energetic electron and hole, and $[P_p(T) + P_{pt}(T,V) + P_t(V)]$ is the net probability of localized carrier excitation by three mechanisms:

$P_p(T)$: phonon excitation probability, which is temperature dependent.

$P_{pt}(T,V)$: phonon excitation probability with the effect of barrier lowering due to high electric field, which is both temperature and voltage dependent.

$P_t(V)$: field-enhanced tunneling probability, which is voltage dependent.

We can sum up $P_p(T)$ and $P_{pt}(T,V)$ to account for all phonon-assisted excitation processes including barrier lowering (Poole-Frenkel) and call it "temperature related" probability, $P_{tem}(T,V)$. Then:

$$x = M_e(V)[P_{tem}(T,V) + P_t(V)] \quad (3.5)$$

$$y = M_h(V)[P_{tem}(T,V) + P_t(V)] \quad (3.6)$$

In separate experiments, we have found that under high electric field, the ionization coefficient for holes and electrons was comparable for a-Si (i.e., under high field)

For G>>1 (e.g., G>5 for bias higher than -3V), we can approximate G as

$$G = \frac{1+y}{1-xy} \sim \frac{2}{1-xy} \quad (3.7)$$

From (3.5, 3.6, 3.7),

$$G(T,V) \sim \frac{2}{1-M_e(V)M_h(V)[P_{tem}(T,V)+P_t(V)]^2} \quad (3.8)$$

$$P_{tem}(T,V) + P_t(V) \sim \sqrt{\frac{1}{M_e(V)M_h(V)}\left[\frac{G(T,V)-2}{G(T,V)}\right]} \quad when\ G(T,V) \gg 1 \quad (3.9)$$

We use Eq. (3.9) and divide its value by the value at the lowest temperature (e.g., T = 200 K) we have measured, yielding the relation

$$\frac{P_{tem}(T,V)+P_t(V)}{P_{tem}(200K,V)+P_t(V)} = \sqrt{\left[\frac{G(T,V)-2}{G(200K,V)-2}\right]\left[\frac{G(200K,V)}{G(T,V)}\right]} \tag{3.10}$$

At the lowest temperature of 200 K and high enough bias, we have $P_t(V) \gg P_{tem}(200K,V)$ due to the low phonon population so that we can ignore the term $P_{tem}(200K,V)$ in Eq. (3.10). Then Eq. (3.10) can be reduced to

$$\frac{P_{tem}(T,V)}{P_t(V)} = \sqrt{\left[\frac{G(T,V)-2}{G(200K,V)-2}\right]\left[\frac{G(200K,V)}{G(T,V)}\right]} - 1 \tag{3.11}$$

Eq. (3.11) enables us to find the relative importance between tunneling and phonon excitation under different operation conditions that satisfy $G(T,V) \gg 1$. The ratio $\frac{P_{tem}(T,V)}{P_t(V)}$ obtained from the measured data and Eq. (3.11) is plotted in Fig. 3.6.

As shown in Fig. 3.6, at a bias of -3 V, $\frac{P_{tem}(T,V)}{P_t(V)}$ increases as the temperature changes from 200 K to 350 K. However, even at the highest temperature of 350 K, the contribution of phonon excitation is only about 10% of field-enhanced tunneling. As the reverse bias increases from -3 V to -4 V, both the value and the slope of $\frac{P_{tem}(T,V)}{P_t(V)}$ vs. temperature are reduced significantly, indicating that field-enhanced tunneling becomes even more dominant over phonon-assisted excitation under this electric field. Eventually the tunneling process becomes totally dominant at -5 V bias or an applied field of 1.2 MV/cm.

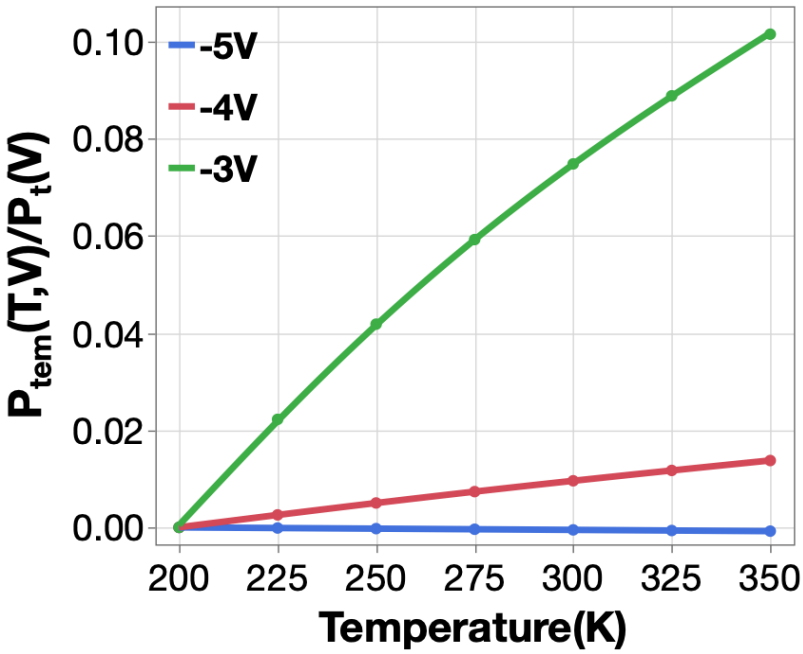

Figure 3.6 Ratio of phonon excitation probability, $P_{tem}(T,V)$ to tunneling probability, $P_t(V)$ as a measure of the relative importance between phonon excitation and field-enhanced tunneling in CEP.

From this study, we confirm a significant and fundamental difference between CEP effect and impact ionization in conventional APDs. For APDs, gain decreases with temperature due to stronger inelastic phonon scattering in crystalline material at higher temperatures, which limits the efficiency for carriers to gain kinetic energy under high temperature, and the same mechanism also causes increase in the breakdown voltage [7]. In contrast, the disordered potential in thin amorphous material favors elastic scattering [8, 9], and above all, the CEP gain is related to the excitation of localized states, mainly governed by the temperature independent tunneling process and with minor contributions from phonon excitation. This fundamental difference gives CEP detectors the athermalized characteristics over a wide temperature range of 150 K.

3.4 Conclusion

In this section, we investigated temperature sensitivity of the cycling excitation process in thin (35-40 nm) a-Si. By analyzing the effect of temperature on the gain and breakdown voltage,

we conclude that under high gain and high applied field, field-enhanced tunneling dominates the localized state excitation to sustain the carrier multiplication cycles whereas phonon-assisted excitation plays some roles under low bias and moderate gain. For high sensitivity and single photon detectors, photodetectors are operated in the high gain regime or biased above breakdown. The unique athermalized property of CEP detectors offer important advantages over conventional APDs or SPADs because of the relaxed requirements for precision temperature control and reduced pixelation noises due to local temperature variations.

Portion of Chapter 3 reprints the work that has been submitted to Optics Express: **Zhou, J.**, Chiu, S.Y., Miah, M.A.R., Yu, Y., and Lo, Y.H., 2022. Athermalized Carrier Multiplication Mechanism for Detectors Using an Amorphous Silicon Gain Medium. Submitted. The dissertation author is the primary investigator/first author of the paper.

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Chapter 4. CEP detectors For Longwave Infrared Range

Long-wave Infrared (LWIR) detection has been widely used in a large number of systems including night vision, thermal sensing, remote sensing, autonomous driving, robotics vision, machine vision, disease detection, and scientific research [1]. Over the past few decades, a large number of LWIR detectors have been demonstrated, including microbolometer [2,3], HgCdTe (MCT) [4], multi-quantum well (MQWIP) or quantum dots (QDIP) [5,6], Type-II superlattice structure (T2SL) [7,8], blocked impurity band (BIB) trap detectors [9,10], and graphene detectors [11]. Based on the operation environment of these LWIR detectors, they can be divided into two groups, uncooled detectors and cooled detectors. Most uncooled LWIR detectors are bolometers which sense the IR induced temperature change, and the output signal can be represented via different transduction mechanisms [12,13]. The biggest limitation of microbolometers is the limited device speed, with the detection bandwidth less than 100 Hz even though they have demonstrated descent room temperature detectivity of ~ 10^9 Jones [2,3]. Apart from the microbolometers, Type-II superlattice (T2SL) structure has demonstrated quantum detection at room temperature. Without cooling down, it has shown broad IR spectrum detection ranging from short-wave infrared (SWIR) to very-long wavelength infrared (VLWIR) light [14,15]. The highest reported TIIS LWIR detectivity is about 6×10^8 Jones with an optical immersion design [7].

Unlike the uncooled LWIR detectors, almost all cooled LWIR detectors are quantum detectors that absorb photons at LWIR wavelengths and generate photoexcited electrons or electron-pairs for photoresponse. The output signal of uncooled LWIR detectors is photocurrent. Photons with LWIR wavelengths usually carry low photon energies, meaning that the materials used as absorption layer in the LWIR quantum detectors should have low bandgaps for electron-hole pairs being excited by input photons. This explains why they need to be operated at low

temperatures as thermally generated carriers could cause high dark current at room temperature. At cryogenic temperature, cooled LWIR detectors show higher performance than uncooled detectors in general. For example, HgCdTe detectors have shown detectivity of Jones at lower than 100 K [4]. Multi-quantum well (MQWIP) or quantum dots infrared photodetectors (QDIP) also achieved detectivity of Jones under ~77 K [6,16,17]. Lastly, BIB trap LWIR detectors using shallow impurity states in highly doped Si or Ge have achieved detectivity as high as Jones, but the devices have to be operated at extremely low temperature (~10 K) or the impurity states would be thermally excited to produce unacceptably high dark current [10].

Both uncooled and cooled LWIR detectors have their shortcomings such as limited frequency response for microbolometers and cooling systems and complicated materials or processing required for most quantum detectors. It is highly desirable to have room temperature LWIR detectors that are easy to fabricate at low cost, and produce high detectivity, low noise equivalent power (NEP) and high frequency response much greater than 100 Hz. In this chapter, we demonstrate a unique design for uncooled LWIR detectors using a combined structure of amorphous germanium (a-Ge) and amorphous silicon (a-Si), both unintentionally doped. The a-Ge layer absorbs LWIR light, and the a-Si layer produces carrier multiplication for high sensitivity via CEP that has been discussed in previous chapters. The device has a very simple structure, is easy and low cost to fabricate, and can operate under room temperature, showing high responsivity (1.7 A/W), high detectivity (6×10^8 Jones), low noise equivalent power ($5\ pW/\sqrt{Hz}$), and high frequency response of greater than 20 KHz, limited by the modulation bandwidth of the CO_2 laser source.

4.1 Device Structure and Fabrication

The device structure is based on the typical a-Si CEP device, by adding another layer of a-Ge with thickness of 100 nm between the light transmission layer and a-Si layer. In addition, the original top ITO layer is replaced by a thin layer (12 nm) of Cr/Au in order for the optical input at LWIR wavelength passing through and being absorbed by a-Ge layer. Detailed fabrication process flow is shown as follows:

A 25 nm thick a-Si layer is deposited at 270°C by plasma-enhanced chemical vapor deposition (PECVD) on a highly n-doped silicon substrate, followed by room temperature sputtering of a 100 nm thick a-Ge layer as the absorption medium. After the a-Si and a-Ge deposition, 30 μm diameter device mesas are photolithographically defined and dry etched with SF_6:C_4F_8. To passivate the mesa sidewall, Al_2O_3 (40 nm) and SiO_2 (200 nm) are deposited by atomic layer deposition at 200 °C and by PECVD at 270 °C, respectively. Finally, an 18 nm Cr/Au layer is deposited to form the top electrode with 10 % transmission at 10.6 μm wavelength light, and a 220 nm Ti/Au layer is further deposited to form the top and ground contact pads. The cross-section and top view of the device structure are shown in figure 4.1.

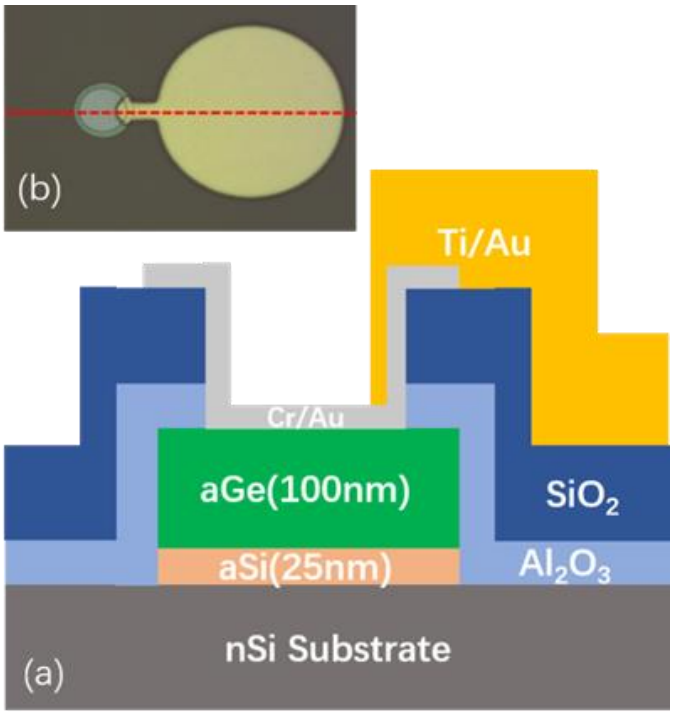

Figure 4.1 (a) Cross-sectional (not to scale) and **(b)** Top view of the device.

4.2 Characterization

The device characterization includes dark current, bias and frequency photoresponse and noise equivalent power (NEP) measurement results. Dark current is measured with a Keysight B2900 source meter with reverse bias range from 0 V to -5 V. The photoresponse is measured by an RF spectrum analyzer, after being amplified by a transimpedance amplifier (TIA). NEP can also be collected from the RF spectrum analyzer. A CO_2 laser (10.6 μm wavelength) is utilized as the LWIR source, with operation frequency of 5 KHz. To measure the device response between 2 Hz and 6 KHz, we use a chopper to modulate the laser which is operated at 100% duty cycle like a CW laser. For high frequency characterization higher than 6 KHz, we modulate the CO_2 laser output at 5 KHz and characterize the output power at higher (up to the 4th) harmonic frequencies as the input optical power. This approach provides the capability for us to extend the range of measurement to 20 KHz. The laser spot on the device surface is 5x5 mm^2, producing an optical

power density of $4\mathrm{mW/cm^2}$. The incident light power is calibrated with a commercial detector (Thorlabs: S401C). All measurements are performed at room temperature.

From the measured photocurrent at 1 Hz resolution bandwidth from an RF spectrum analyzer, we calculate frequency-dependent responsivity ($R = \frac{I_{photo}}{P_{optical}}$), shot noise limited specific detectivity ($D^* = \sqrt{A}R/\sqrt{2eI_{dark}}$), and noise equivalent power ($NEP = \sqrt{A}/D^*$) under different bias voltages. In these expressions, A is the device area, e is magnitude of electron charge, is the CO_2 laser power incident on the device area and is the device dark current.

The photoresponse measurement is done with an input CO_2 laser power of 27 nW. The input optical signal is also modulated at different frequencies from DC to 20 KHz. Figure 4.2 a and b show the bias dependent DC dark current and photo responsivity at 5 KHz respectively. The responsivity plot has a bias range of 2.5 V to 5 V as the photoresponse is too low to be measured reliably at reverse bias lower than 2.5 V.

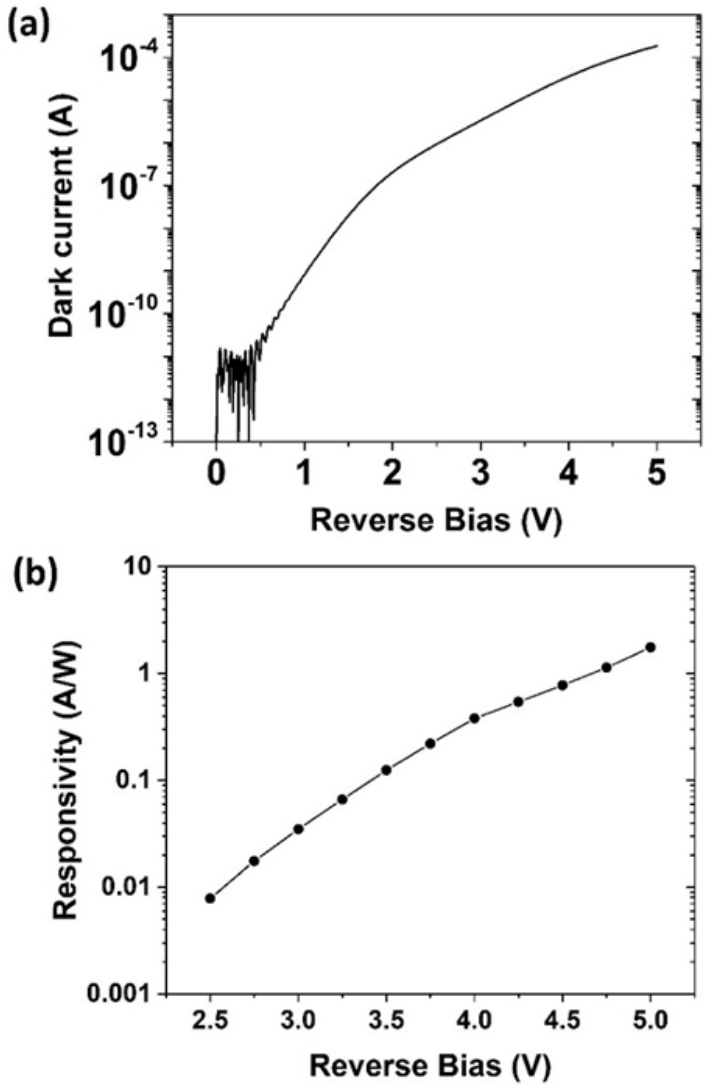

Figure 4.2 Bias dependent (a) DC dark current and **(b)** Responsivity at 5 kHz under 27 nW CO_2 laser illumination.

From the dark current and RF spectrum of the device above 2.5 V, we are able to say that the dominant noise of the device is shot noise. Hence the specific detectivity (D*) and NEP can be calculated based on the equations shown above. For a device with 30 μm diameter active area, we observe the highest specific detectivity of 6×10^8 Jones and the lowest NEP of 5 $pW/\sqrt{Hz}$ at reverse bias 5 V for input optical wavelength of 10.6 μm (Fig. 4.3). Unlike bolometers and thermopiles that measure thermal effects and have limited (usually < 100 Hz) frequency response,

our device can produce high detectivity and low NEP at 20 KHz frequency, which is limited by the input CO2 laser response instead of intrinsic device speed.

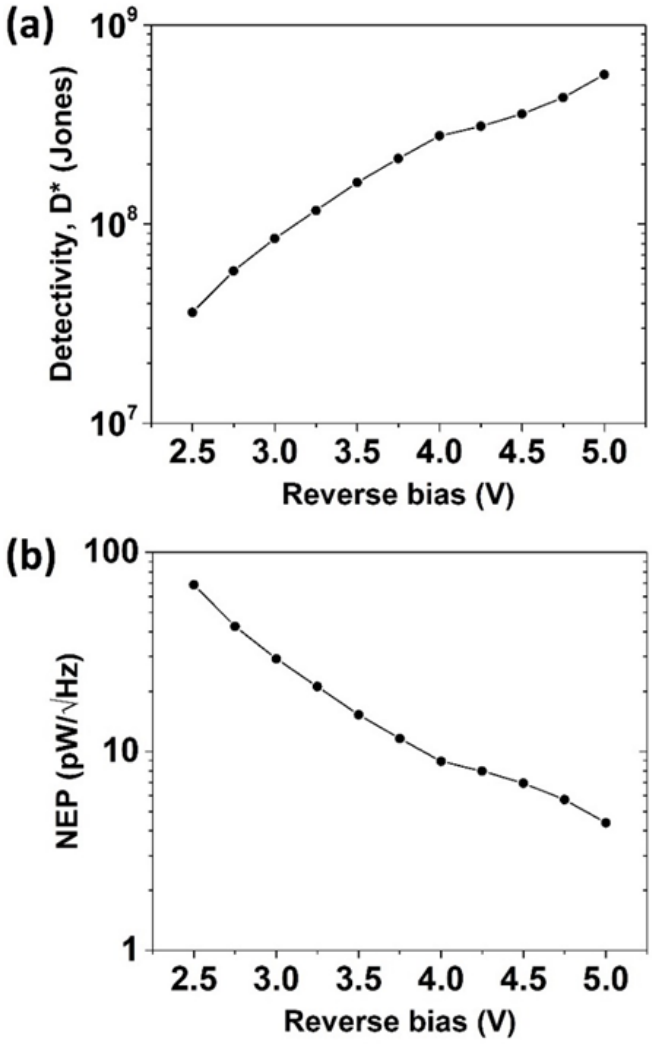

Figure 4.3 Bias dependent (a) Detectivity and **(b)** NEP of the device at 5 kHz

Figure 4.4 shows the frequency dependence of device characteristics from 2 Hz to 20 kHz. We clearly observe that the device characteristics are divided into two regimes according to frequency. At 10 Hz or lower frequency, the device responsivity and detectivity reach 10 A/W and 7×10^9 Jones, which by themselves set a record value for uncooled LWIR detector, but the numbers drop rapidly above 10 Hz, showing the general property of thermal detectors. As a

thermal detector, different materials of the device absorb the CO_2 laser power, causing temperature rise which subsequently increases dark current that is revealed as "photoresponse". However, what is more interesting and important is the higher frequency response of the detector. At higher than 100 Hz and up to 20 KHz, the maximum frequency we have measured, the device shows a photo responsivity of around 1.7 A/W and detectivity of 6×10^8 Jones, and the values are nearly independent of frequency within measurement errors. The results indicate that above 100 Hz, thermal effects vanish because of their slow response, and the device operates under a different mechanism which we will investigate in detail later.

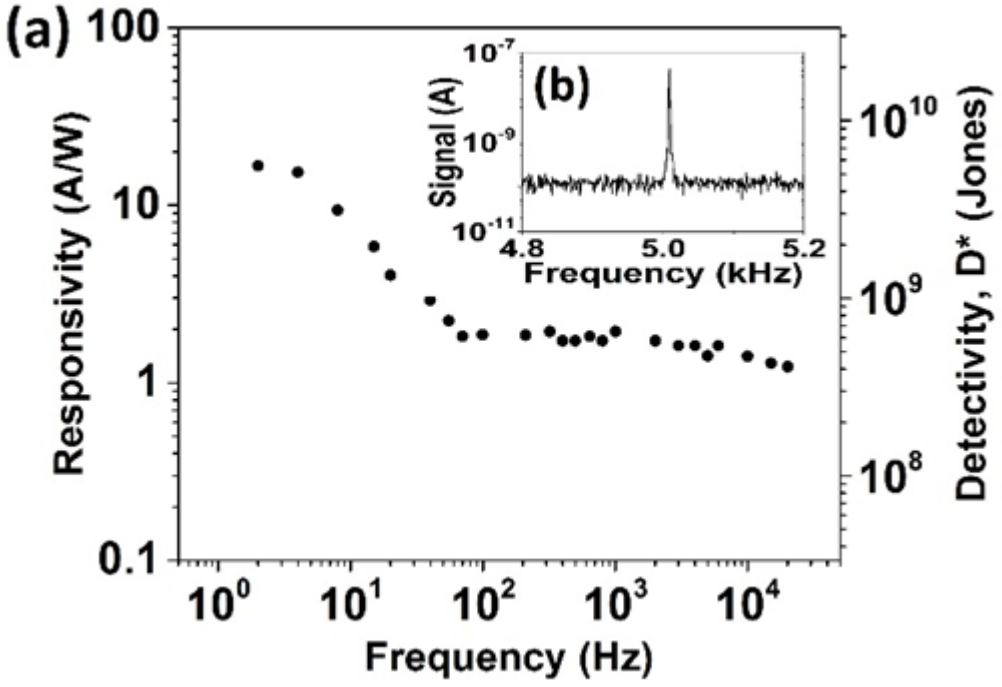

Figure 4.4 (a) Frequency dependent responsivity and detectivity of the device under 5V reverse bias **(b)** Photocurrent trace from RF Spectrum Analyzer at 5kHz laser modulation.

To better convey a comprehensive understanding of the performance of our LWIR detector, table 1 is created to compare our device with other LWIR detectors that operate under room temperature. In spite of its simple structure and fabrication process, our device has shown highly favorable performance in many key metrics. Compared with quantum detectors, our detectors offer

the best room temperature performance and are easiest to fabricate with low cost materials such as a-Ge and a-Si.

Table 4.1 Comparison of NEP (pW/$\sqrt{Hz}$) and specific detectivity, D^* ($\times 10^8$ *Jones*) for different uncooled LWIR detectors

Technology	λ	NEP	D*
Quantum Detectors			
aGe/CEP (*This work*)	10.6	5	6
InAs QDIP [5]	9	N/A	6
MCT PC optically immersed [4]	9–10.6	$> 50^*$	5–1
MCT PVM optically immersed [4]	8–10.6	$> 167^*$	6–2
InAsSb PV [24]	8–11	1600-16000	0.6-0.06
T2SLs InAs/InAsSb on GaAs [7]	10.6	161	5
Type-II PC on GaAs [8]	8 –12	1500*	1.3
Thermal Detectors (Frequency limited to 100Hz)			
VO_2 based Micro Bolometer [2]	8–12	N/A	1.9
$Si_xGe_yO_{1-x-y}$ Micro Bolometer [3]	8–12	N/A	11.9
Ni nano bolometer [25]	>10	8.7	0.15*

*Calculated using reported detectivity or NEP and active device area

4.3 Modeling

Our detector has demonstrated the capability of high frequency photo response up to the laser bandwidth limit of 20 KHz, which suggest that it operates as a quantum detector (i.e., signal produced by photoexcited electrons or electron-hole pairs by absorption of LWIR photons) rather than a thermal detector. The CO_2 laser we used has a wavelength of 10.6 μm, corresponding to photon energy of 117 mV. Hence there are two key questions to answer: 1) what quantum transition(s) is responsible for the device behaviors at this wavelength? 2) what signal amplification mechanism(s) take place to give the device its superior performance. In this section, the proposed physical model will be introduced, and carrier transport equations will be used to analyze the optical excitation pathway and signal amplification mechanism for the LWIR detector.

The hypothesis of the main operation mechanism under high (> 100 Hz) frequency is due to photoexcitation of electrons from the bandtail states to the mobile states of the conduction band of a-Ge. The excited electrons in the mobile states have much greater mobility than those in the bandtail states and can cross the a-Ge/a-Si heterointerface to enter the a-Si layer where a high electric field exists under voltage bias. The a-Si layer provides efficient carrier multiplication via the cycling excitation process (CEP) reported in our earlier publications [19,22,23], producing high responsivity.

Equations (4.1) and (4.2) are continuity equations for electron concentrations in the mobile states of conduction band (n) and in the conduction bandtail (n_t) based on the assumption that photoexcited electrons are generated from electron transition between the bandtail states and the mobile states of conduction band of a-Ge.

$$\frac{dn}{dt} = -n\gamma_n - \frac{n-n_o}{\tau'} + n_t\gamma_t + n_t\sigma G_p \tag{4.1}$$

$$\frac{dn_t}{dt} = -n_t\gamma_t - n_t\sigma G_p - \frac{n_t-n_{to}}{\tau} + n\gamma_n \tag{4.2}$$

where $\gamma_t(\gamma_n)$ is the electron emission (capture) rate from (to) bandtail states to (from) the conduction band, $\frac{1}{\tau}\left(\frac{1}{\tau\prime}\right)$ is the thermal generation-recombination rate between bandtail states (conduction band) to the valence band, σ is the interaction cross section of a bandtail state electron and LWIR photon, and G_p represents the LWIR photon flux. In addition, n_o and n_{to} represent the equilibrium electron concentration in the mobile states of conduction band and in the conduction bandtail of a-Ge, respectively. Hence the relation $n_o\gamma_n = n_{to}\gamma_t$ holds.

To write Eqs. (4.1) and (4.2), we have assumed $\frac{d}{dx}J_n \sim \frac{d}{dx}(env_d) \sim ev_d\frac{dn}{dx} \sim 0$ where J_n represents the electron current density in a-Ge and v_d is the drift velocity of electrons in the mobile

states. Here we have ignored the current contribution by electron hopping over the localized states. We can express v_d in terms of electron transit time t_{tr} and a-Ge thickness d_{aGe} as $t_{tr} = \frac{d_{aGE}}{v_d}$.

Electrons will experience bias-dependent CEP gain in a-Si after crossing the a-Ge/a-Si interface. The energy barrier for the conduction band of a-Ge/a-Si for electrons is small. Hence, we assume 100% electron injection efficiency from the mobile states of conduction band of a-Ge to a-Si. Ignoring the drift velocity difference between electrons and holes in the mobile states of conduction and valence band for simplicity, we can represent the total particle current density, J, as

$$J = J_n G_{CEP} = env_d G_{CEP} \tag{4.3}$$

where J is the sum of the electron current density and the CEP generated hole current density, as illustrated in Fig. 4.5 below.

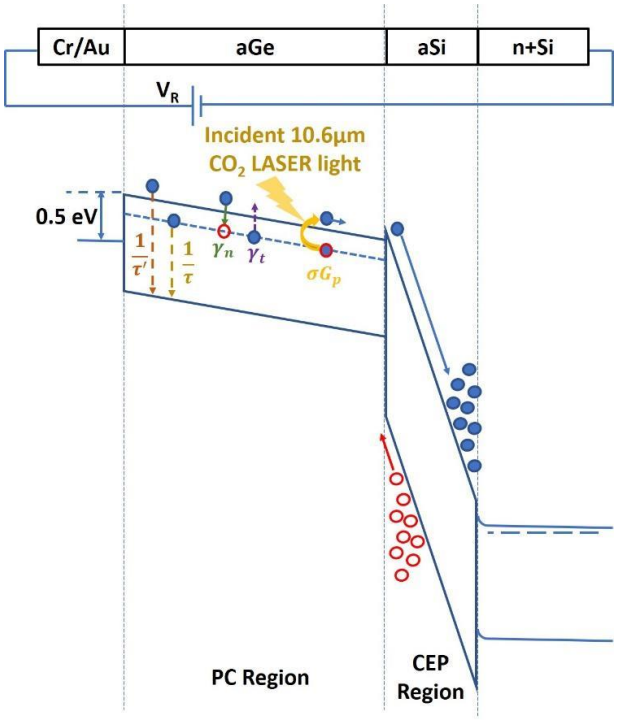

Figure 4.5 Band diagram of the device under reverse bias. Here, $\tau'(\tau)$ represent generation recombination rate from conduction band (bandtail) to valence band, $\gamma_n(\gamma_t)$ are electron capture (emission) rate to (from) bandtail state, σG_p is electron generation rate via photoexcitation of bandtail states by incident LWIR photon flux.

By setting the d/dt terms to be zero for DC analysis and using the relation $n_o\gamma_n = n_{to}\gamma_t$, n can be derived from Eqs. (4.1, 4.2) as

$$n = n_o\left(1 + \sigma G_p \frac{n_{to}}{n_o} t_{life}\right) \tag{4.4}$$

$$t_{life} = \frac{1}{\left(\gamma_n + \frac{1}{\tau_l}\right) + \left(\gamma_t + \sigma G_p\right)\frac{\tau}{\tau_l}} \tag{4.5}$$

where t_{life} is the effective electron lifetime (i.e. the amount of time for an electron to stay in the mobile states of conduction band).

From Eqs. (4.3-4.5), we can find the dark current density (J_{dark}), photocurrent density (J_{photo}), and responsivity (R) as

$$J_{dark} = en_o v_d G_{CEP} \tag{4.6}$$

$$J_{photo} = J - J_{dark} = e\sigma G_p n_{to} t_{life} v_d G_{CEP} \tag{4.7}$$

$$R = \frac{J_{photo}}{h\nu G_p} = \frac{e}{h\nu}\left(\sigma n_{to} d_{aGe}\right)\left(\frac{t_{life}}{t_{tr}}\right) G_{CEP} = \frac{e}{h\nu}\eta G_{PC} G_{CEP} \tag{4.8}$$

To obtain Eq. (4.8), we have used the relations $t_{tr} = \frac{d_{aGE}}{v_d}$ and quantum efficiency $\eta = \sigma n_{to} d_{aGe} \cong \alpha d_{aGe}$ with α being the LWIR light absorption coefficient for a-Ge. The absorption coefficient at 10.6 μm wavelength of undoped a-Ge has been reported to be ~ 100 cm^{-1} [26]. For a thin (100 nm) layer of a-Ge, η is estimated to be in the order of 10^{-3}. This value may be overestimated since part of the measured light absorption is caused by photo excitation of holes from the valence bandtail states to the mobile states of valence band and those mobile holes enter the cathode directly without experiencing CEP gain.

In Eq. (4.8), the responsivity contains two signal amplification terms, the CEP gain produced in a-Si and the photoconductive gain in a-Ge defined by $G_{PC} = \frac{t_{life}}{t_{tr}}$ with t_{life} being the

effective electron lifetime represented by Eq. (4.5) and t_{tr} the electron transit time across the a-Ge layer.

The above model shows that our device can operate as a "quantum detector" in which LWIR light excite electrons from the bandtail states to the mobile states of conduction band. Such excited electrons experience two gain mechanisms in series, the conventional photoconductive gain in a-Ge and the CEP gain in the high field a-Si region. The CEP gain is critical because the photoconductive gain is modest or in some case, negligible in our device. Due to the high density of bandtail states in a-Ge and high phonon emission rate for electrons to fall into the bandtail states from the mobile states, the effective lifetime for electrons to stay in the mobile states is in picoseconds. On the other hand, the low mobility and low E-field in a-Ge (most E-field drops in a-Si layer) produces a transit time of the order of 10ps. As a result, the photoconductive gain $G_{PC} = \frac{t_{life}}{t_{tr}}$ in our device is modest. The device largely relies on the CEP gain to increase its photo responsivity and detectivity.

Figure 4.6 shows the bias-dependent CEP gain under visible (639nm) light excitation from the same device structure without the a-Ge layer. A CEP gain greater than 100 is achieved and its value increases rapidly with the bias voltage. This is consistent with the observed bias dependence of photo responsivity in Fig. 2(b). Therefore, for our device, the CEP gain plays a key role in achieving high responsivity, high detectivity, and low NEP.

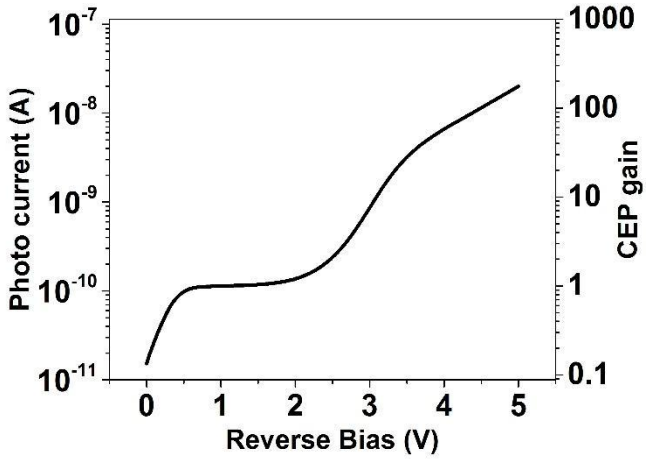

Figure 4.6 Photoresponse (at 639nm wavelength) of a device consisted of an a-Si layer on an n-Si substrate (same structure but without the a-Ge LWIR absorption layer) for characterization of CEP gain.

4.4 Conclusion

A novel design for room temperature LWIR detector has been demonstrated in this chapter. By using a thin layer of a-Ge for light absorption and another layer of a-Si to produce CEP gain for photocurrent amplification, this device shows high detectivity and low NEP as a "quantum detector" instead of "thermal detector". More specifically, at 20 KHz optical modulation, a 30 μm diameter device has shown a detectivity value of 6×10^{8} Jones, which is among the highest detectivity for room temperature LWIR detectors. The device shows a NEP value of 5pW/$\sqrt{Hz}$, the lowest value for all uncooled LWIR detectors. At high frequency (>100 Hz), the proposed operation mechanism is due to photoexcitation of electrons from the bandtail states to the mobile states of the conduction band of a-Ge, integrated with CEP amplification in a-Si layer, contributing to its superior performance. The fast response, room temperature operation, high detectivity, low NEP, and simple and low-cost fabrication process make the device attractive to night vision, machine vision, autonomous driving and many other applications.

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long-wave infrared detector with thin double layers of amorphous germanium and amorphous silicon. *Optics Express*, *27*(25), pp.37056-37064. The dissertation author is the primary investigator/first author of the paper.

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Chapter 5. CMOS Compatible Process Development for CEP detectors

5.1 Amorphous Silicon Deposition by Foundry

In previous chapters, I have demonstrated the fabrication process flows for the a-Si CEP detectors. We can find that the a-Si CEP detectors are very simple structures and easy, low cost to fabricate. In this chapter, I will show the CMOS process compatibility of the a-Si CEP detectors and the procedures of the CMOS compatible process development.

The first step is to calibrate the recipe of a-Si deposition by foundry. Fig. 5.1 is the image from Scanning Electron Microscope (SEM). The recipe of the a-Si deposition in this sample is the standard 35-40 nm a-Si recipe by PECVD, which I used in all those previous structures. The thickness of the a-Si layer is measured as 36.5nm by SEM. Fig. 5.2 is the energy dispersive spectroscopy (EDS) map to identify and quantify the elemental composition of the a-Si layer. There are three elements demonstrated in the figure: silicon (Si), oxygen (O) and nitrogen (N). The oxygen and nitrogen elements are impurities from the PECVD chamber during deposition. Fig. 5.3 shows the quantized composition of these elements. The upper panel is for the bulk area and the bottom panel is for the interface of a-Si and nSi substrate. The oxygen concentration in the bulk area is about 4 %, while it becomes around 8 % at the interface mainly resulting from the native oxide formed right after HF dip of the substrate before taking to the PECVD chamber. It is noticed that the carbon (C) concentration in the bulk area is around 6 %, which is from the C doping by CH4 during deposition and very close to the desired value: 5 %.

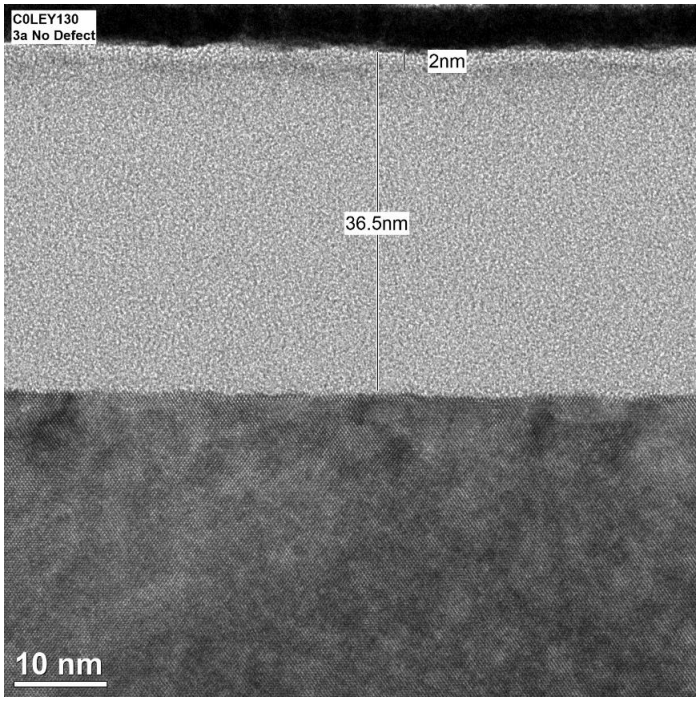

Figure 5.1 SEM of the standard 35~40 nm a-Si recipe by UCSD

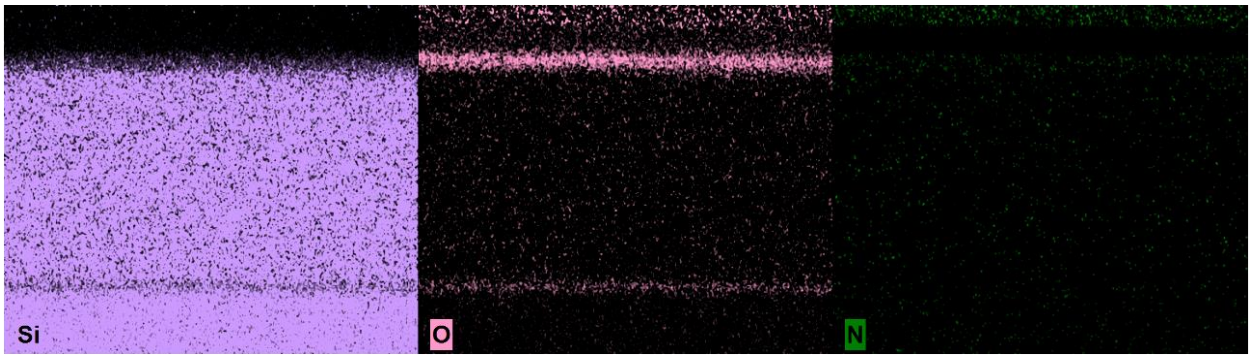

Figure 5.2 EDS map of the standard 35~40 nm a-Si recipe by UCSD (tested by EAG Laboratories)

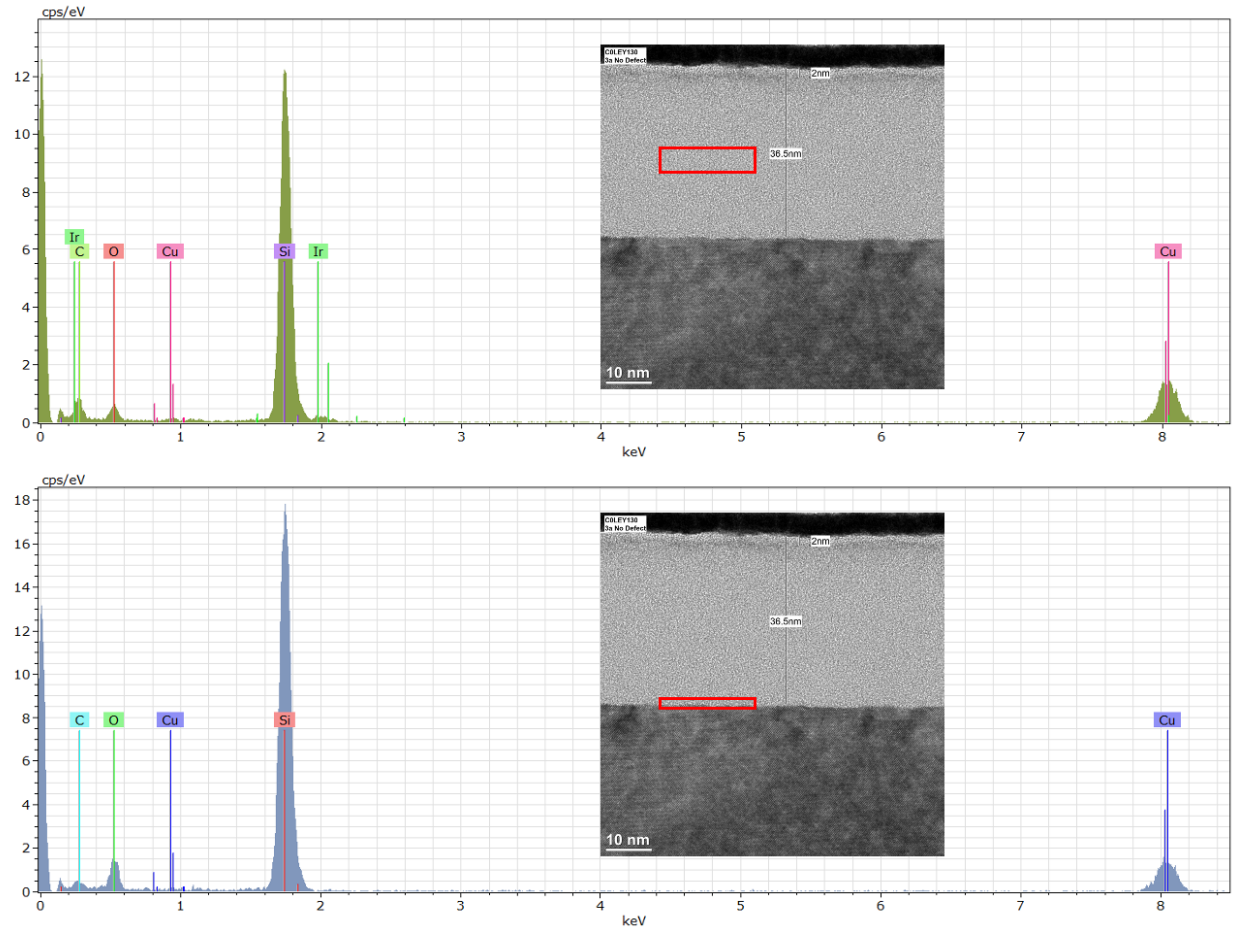

Figure 5.3 EDS spectral of the standard 35~40 nm a-Si recipe by UCSD (tested by EAG Laboratories: *Cu is from TEM grid and Pt/Ga are from EAG capping layers)

Next, I will demonstrate the examinations for the foundry deposited a-Si layers. Fig. 5.4 shows the EDS map of an unexpected “bubble” created by in run#1 test recipe by foundry. The entire area of the wafer with a-Si deposited is covered by these “bubbles” with very high density, approximately 70 %. These “bubbles” created several hundreds of depth on the a-Si surface and the layer in the region having “bubbles” can be peeled off by sonication in acetone solution. By examining the “bubble” by EDS, we can see the “bubble” is a gap between the silicon Epi substrate and another thin silicon layer. Within the gap, there are clusters of silicon atoms and oxide atoms. The a-Si layer was not formed correctly during this process.

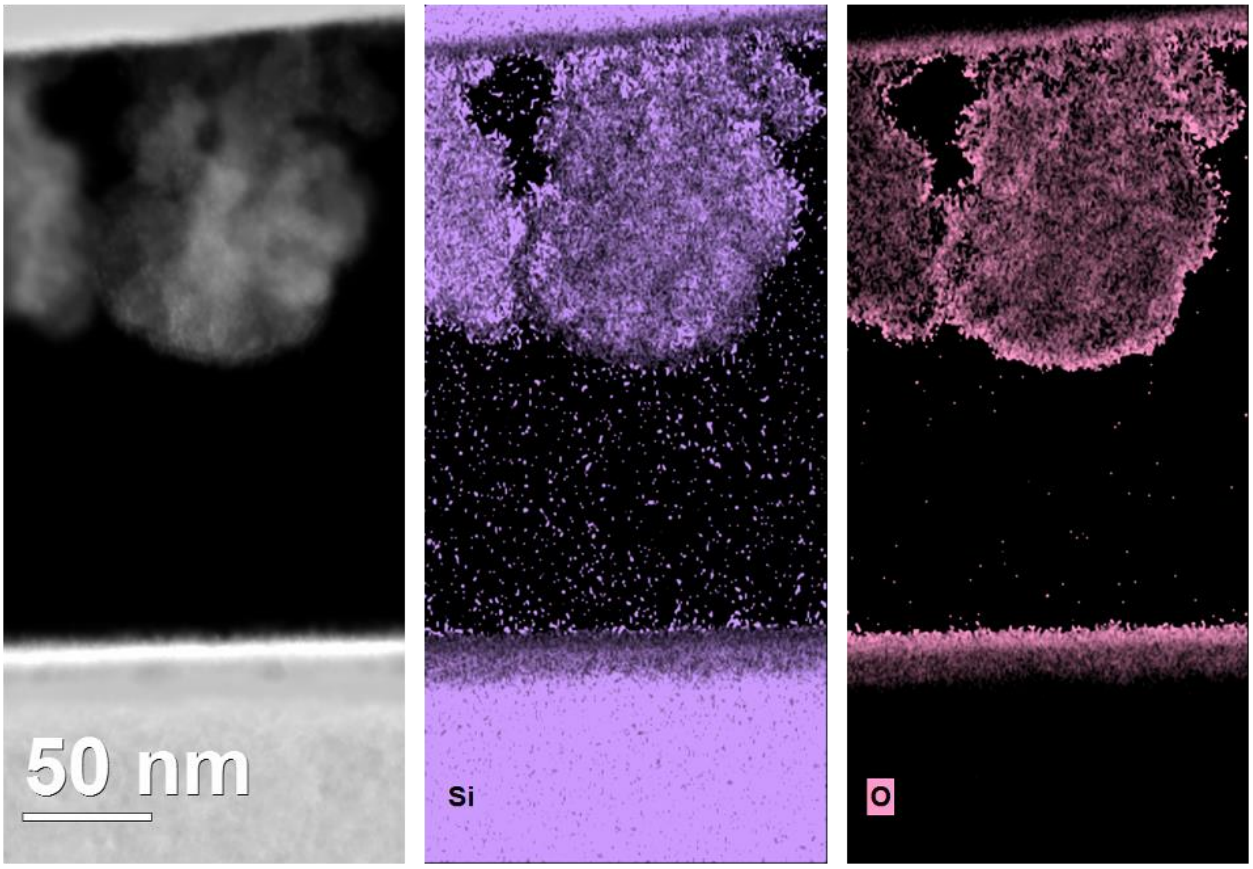

Figure 5.4 EDS map of test a-Si deposition recipe by CMOS foundry with unexpected formation of "bubbles".

In the second test run of a-Si deposition by foundry, changes in recipe were applied for eliminating the "bubbles" in the first run. The "bubbles" were observed to be fewer in this run: lower than 30 % for reference. The EDS map of the a-Si layer in the second run is shown in Fig. 5.5. We observed that there was an extra 12.5 nm oxide layer in between the substrate and a-Si. The amorphous structure of the oxide layer did help the formation of the amorphous structured a-Si. However, the breakdown voltage of the device made by this a-Si layer increased to around 20 V instead of 6 - 7 V for the normal standard a-Si CEP device.

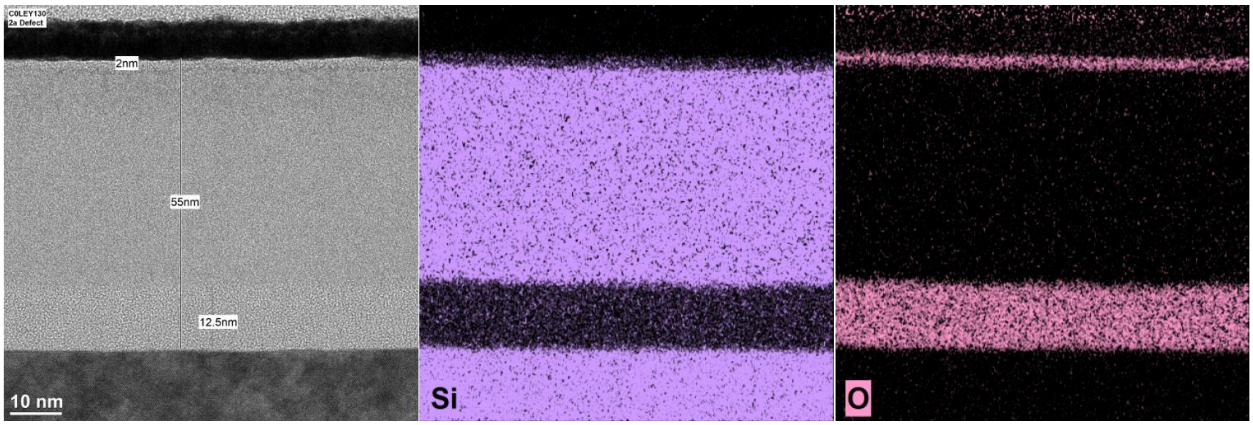

Figure 5.5 EDS map of test a-Si deposition recipe by CMOS foundry with unexpected formation of a 12.5 nm thick extra intermediate oxide layer.

Next is the functional a-Si layer that was deposited by the CMOS foundry, as shown in Fig. 5.6. The SEM image shows that the thickness of this a-Si layer is 44 nm, which is within the acceptable range for a standard a-Si CEP device. The EDS map is shown in Fig. 5.7. As we can see, the oxygen impurities are less than that of the UCSD deposited a-Si. The EDS spectral of the bulk area of this a-Si layer, the upper panel of Fig. 5.8, also shows the lower concentration of the oxygen element. At the interface of this a-Si and its substrate, there is a 1 nm thick oxide layer, which is probably the native oxide similar to that in the UCSD deposited a-Si layer.

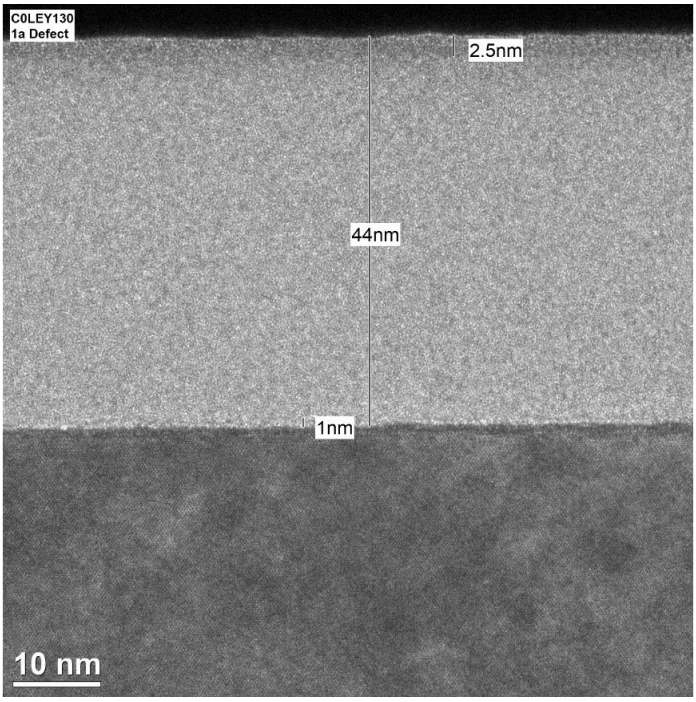

Figure 5.6 SEM of test a-Si deposition recipe by CMOS foundry

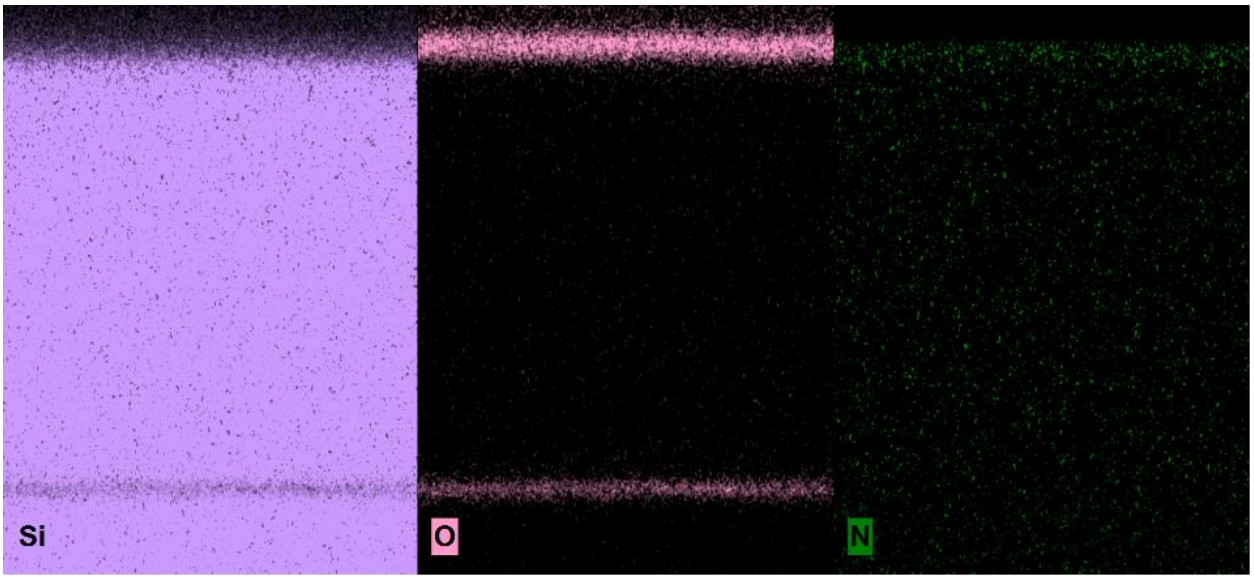

Figure 5.7 EDS map of test a-Si deposition recipe by CMOS foundry (tested by EAG Laboratories)

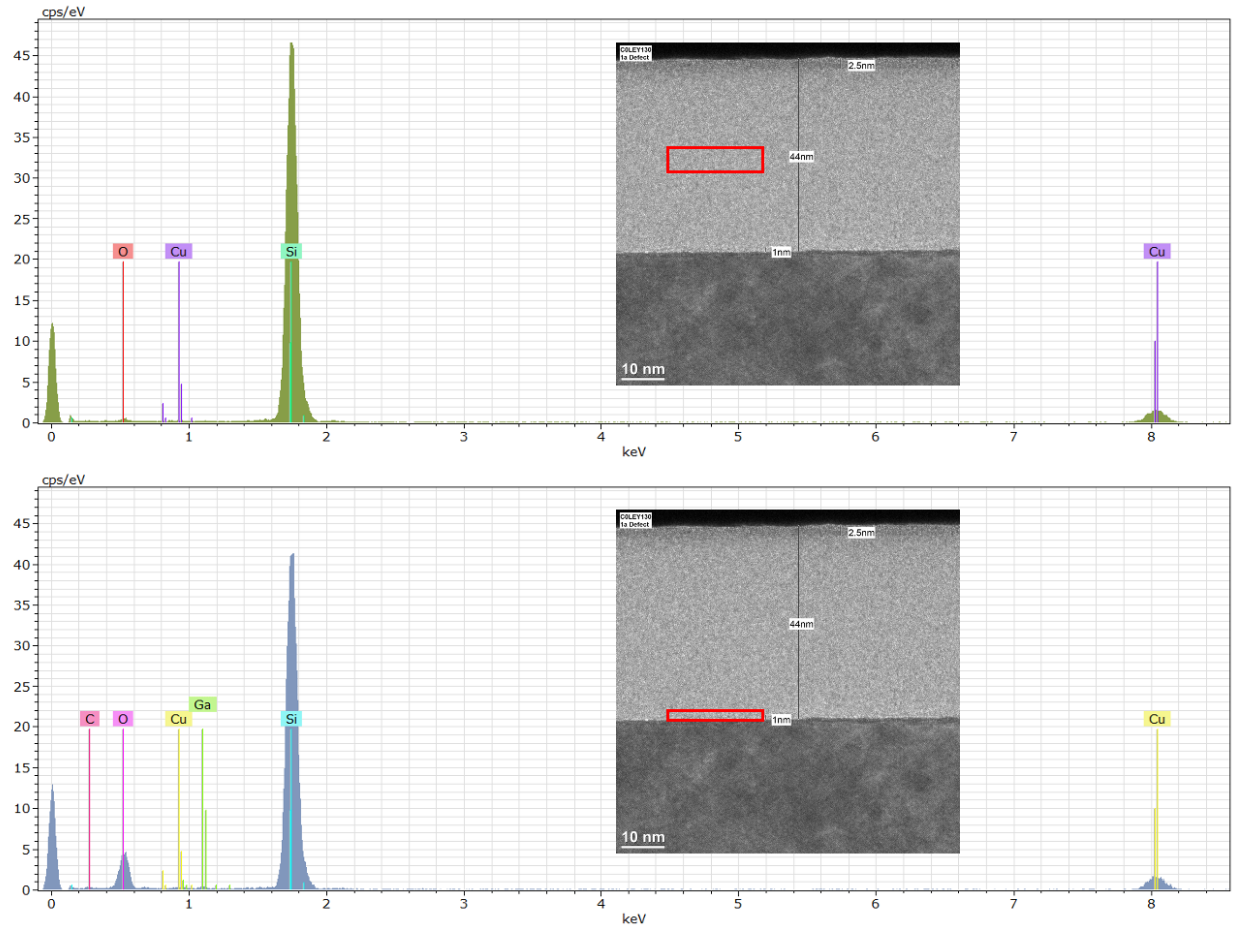

Figure 5.8 EDS spectral of the test a-Si deposition recipe by CMOS foundry (tested by EAG Laboratories: *Cu is from TEM grid and Pt/Ga are from EAG capping layers)

The a-Si CEP devices were fabricated with the a-Si layer deposited by the CMOS foundry. The foundry deposited a layer of a-Si on the Si Epi wafer and then we continued the fabrication following the same process flow as for the standard a-Si CEP device. Figure 5.9 shows the IV characterization of the device. The blue curves are the dark current of several devices and the red curves are the corresponding photocurrent of an incident light with wavelength of 639 nm. The incident power was 180 nW. The dark current characteristic is very close to the a-Si CEP detector shown in Chapter 2. There is a plateau in the photocurrent curve at around 1 V, which is the primary photocurrent. The primary quantum efficiency is around 4 - 5 %. The gain at 4.5 V is

around 200 for this light. Both quantum efficiency and gain of this device can be considered as decent values for going on to the next stage.

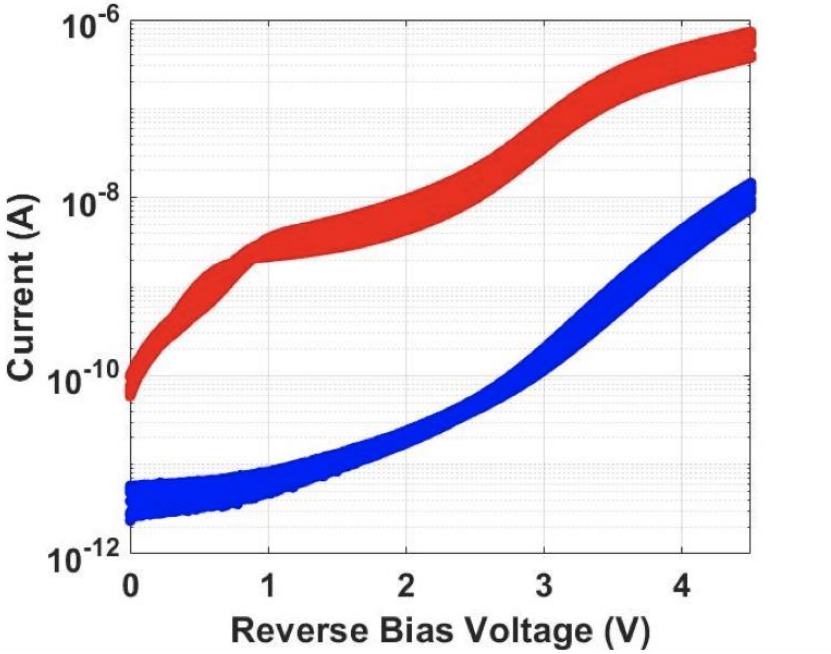

Figure 5.9 I-V characterization of the a-Si CEP device using the a-Si layer deposited by the CMOS foundry.

5.2 Device structure

In parallel with the a-Si calibration, we also designed the device structures of the CEP detectors for the CMOS process. Fig. 5.10 shows four designed device structures: (a) a-Si on nSi; (b) a-Si on pSi; (c) a-Si on PN junction; and (d) a-Si on NP junction. Structure (a) and (b) utilize the N well and P well implantations in the CMOS process, respectively. The doping concentration for the NWELL is around 2e17 - 1e18 cm^{-3} and that for the P well is around 4e17 - 9e17 cm^{-3}. This designed structure is equivalent to the standard a-Si CEP detectors, but with lower substrate doping concentration in order to increase the absorption in the substrate.

Structure (c) and structure (d) incorporate the avalanche gain of the PN junction with the CEP gain of the a-Si. The P well and deep retrograde N well with decreasing doping from middle

to top, form a PN junction. The N well at the side surrounds the PN junction and is connected to the deep N well. Thereby, we can apply bias voltage to the N well around during operation in order to bias the PN junction. Because of the retrograde doping of the deep N well, the N doping between the deep N well and surface, shown in light gray in Fig. 5.10 (c,d), is lower than that at the deep N well, shown in dark gray. Hence, the side PN junction, formed by the P well and the light gray N doped region, requires higher bias voltage to achieve gain than the bottom designed PN junction, formed by the P well and the dark gray deep N well. As a result, the bottom designed PN junction will experience the avalanche gain first and determine the performance of this integrated CEP detector. In the meanwhile, the side PN junction will serve as a guard ring to suppress the current from the side.

Furthermore, the a-Si also serves as a self-quenching or self-recovery layer for the avalanche effect. In the figure, D represents the photosensitive regions of the device, which is at the PN junction. G represents the design of a guard ring with the width of 0.7 μm or 3 μm around the PN junction. These design of integrated CEP detectors with a guard ring is to utilize both the impact ionization and CEP to achieve high multiplication rate and suppress the device noise and thereby facilitate the high frequency measurement.

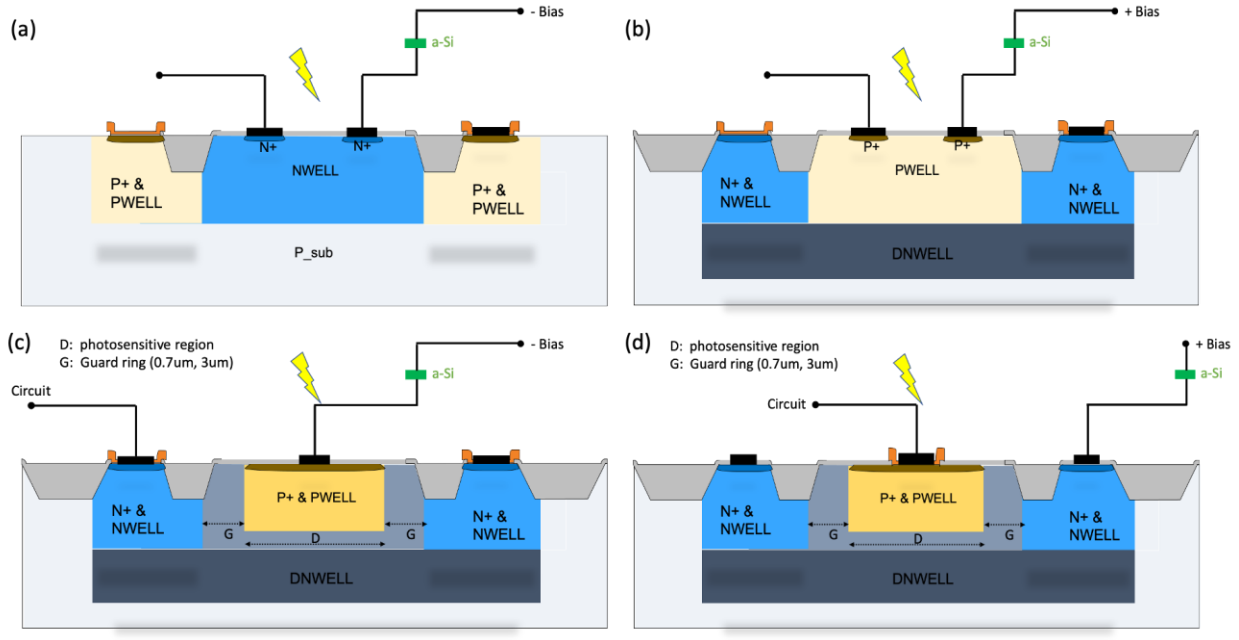

Figure 5.10 CMOS compatible structure designs for CEP detectors: (a) a-Si on N well substrate; **(b)** a-Si on P well substrate; **(c)** Integrated a-Si and PN junction with a design of guard ring; **(d)** Integrated a-Si and NP junction with a design of guard ring.

5.3 Process Design and an Example of Layout Designs

In the first stage of CMOS compatible process development, we designed a hybrid process that incorporates the CMOS process by foundry and the laboratory process by UCSD. The CMOS process will complete the device structure other than the a-Si deposition and the laboratory process will finish up the device with a-Si deposition. In this manner, we are able to exclude the issues caused by the non-ideal a-Si deposition by foundry and test the other part of the structure design.

Figure 5.11 demonstrates an example of the CMOS process part in the hybrid process for structure (d): a-Si on NP junction. First, the retrograde deep N well is formed in the unprocessed p-type wafer by the mask: DNWELL. Second, the active area for the device is defined: the silver trapezoid shallow trench isolation (STI) filled by oxide are the inactive regions and the other areas are the active regions. The active region of the final structure is designed in the center. Third, the N well implantation is formed around the center to connect the deep N well. There are two mask

designs for this step. The first design, 3(a), has the N well mask, NWELL, only and P well mask is generated accordingly. The second design, 3(b), has two masks: NWELL and NWELL2 while the NWELL2 mask is used to block P well implantation and dummy fill. The P well mask for the second design is generated according to these two masks. In this run of hybrid process, we keep both two designs to test the difference in the device performance. Forth, the N+ active implantation is formed at the surface of N well for better contacts to metals later. Fifth, the P+ active implantation is formed at the surface of P well similarly. Sixth, silicide for improving conductivity with metal contacts is formed at the area that is not blocked by the mask marking area. Seventh, a CONTACT mask is designed to remove the dielectric layers precisely at the area of metal contacts for electrodes and deposit TiN/W at the same area for low resistivity metal contacts. The eighth step demonstrates the comprehensive structure of metallization, including 6 metal layers from metal 1 to metal 6 and vias in between. With the metallization step, we are able to design the intercrossed wires for arrays, probing contact areas and other quenching circuits. In the hybrid process design, it should be noticed that some patterns of metal 6 will also be an intermediate substrate for the a-Si CEP layer in the later laboratory process. The last step in the CMOS process part is the passivation layer open (silox): to etch the oxide/nitride on top and open contact windows on metal 6 for the further process and probing. The dimension of the silox window for the a-Si deposition also defines the maximum a-Si active area.

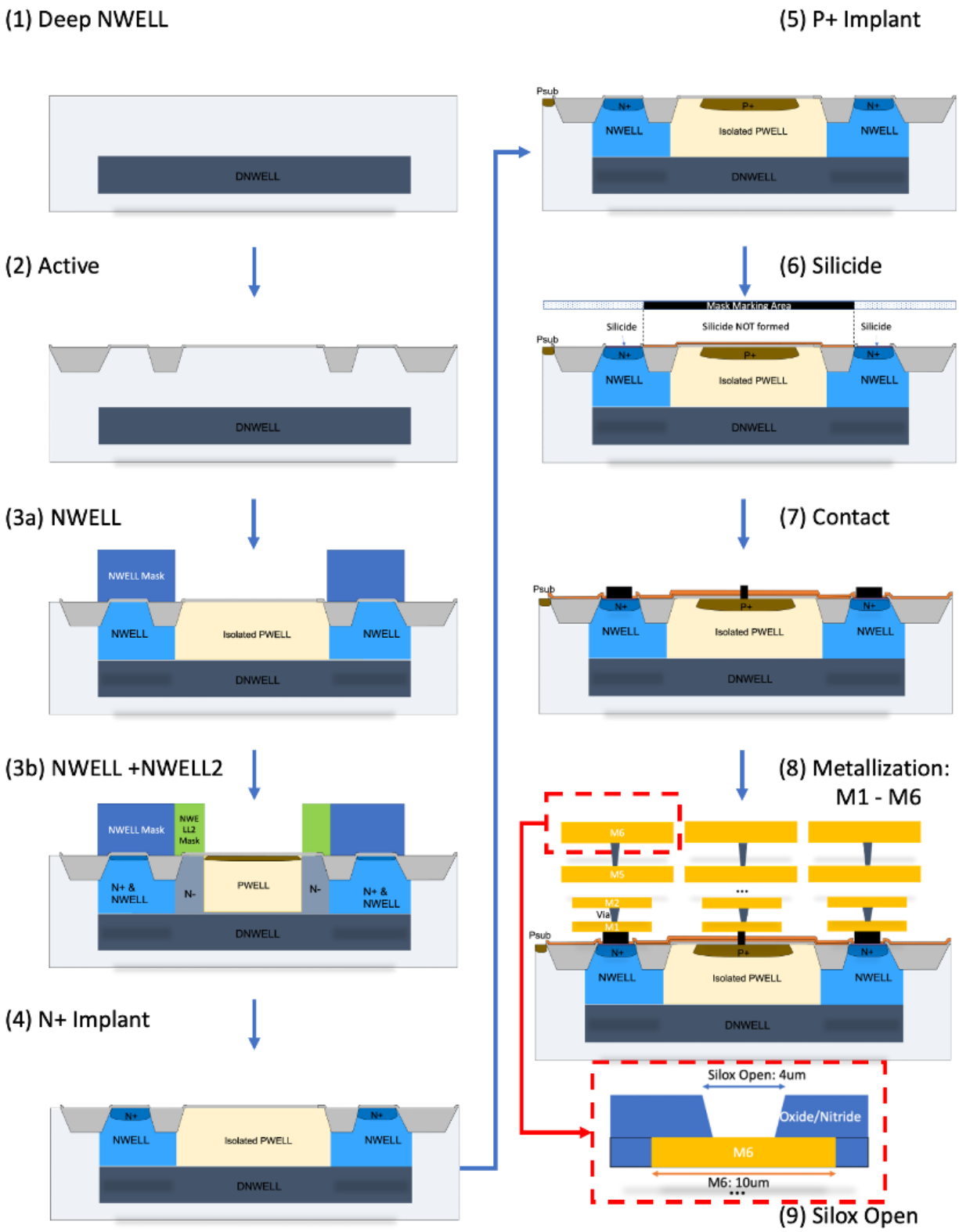

Figure 5.11 Hybrid process: CMOS process flow design for the structure (d): a-Si on NP junction.

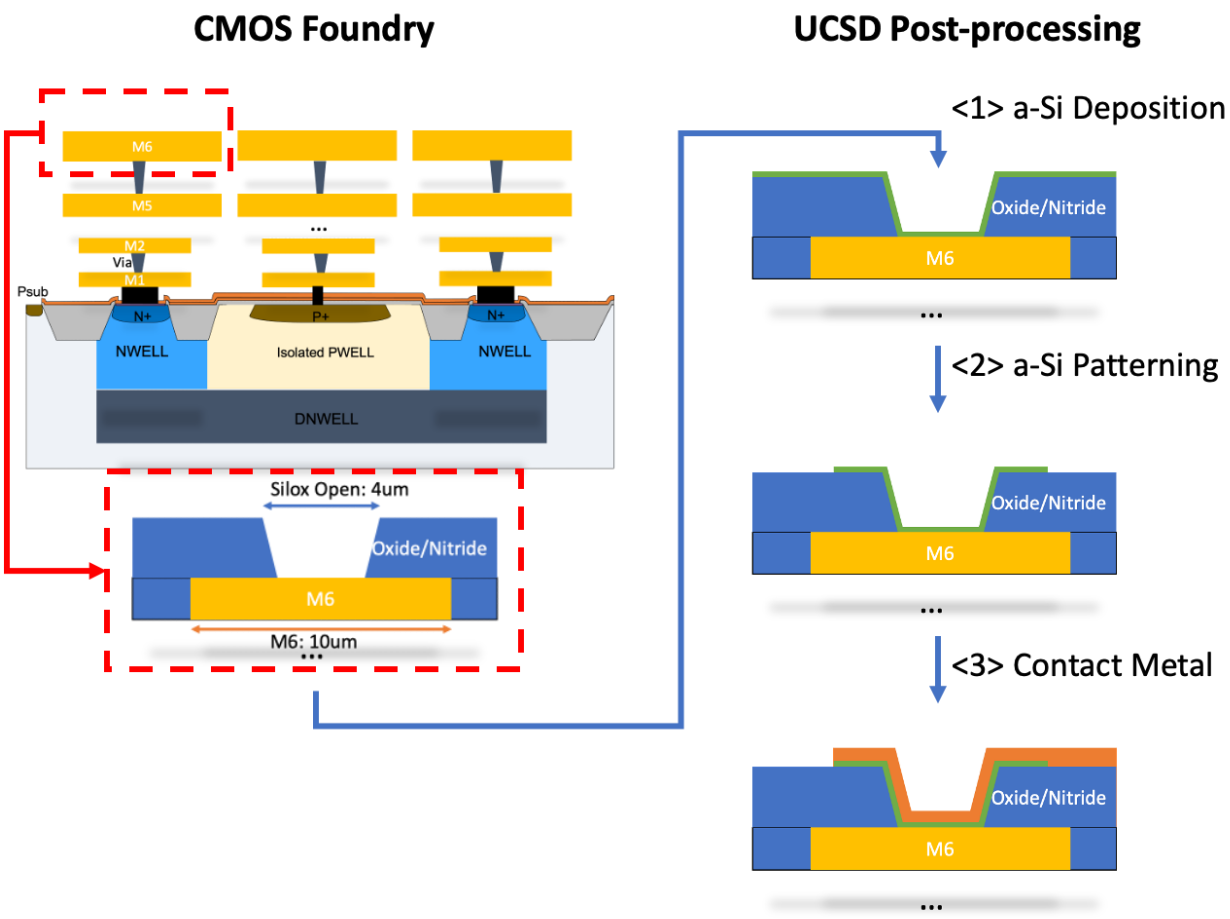

Figure 5.12 Hybrid process: laboratory process flow design for the structure (d): a-Si on NP junction.

Figure 5.12 demonstrates the laboratory part of the hybrid process. The structure made by CMOS foundry is shown on the left and the post-process by UCSD laboratory is on the right. The post-process is basically just depositing the a-Si layer, patterning it and creating a metal top electrode. The a-Si deposition recipe is the same as described in chapter 2 but varies in thickness of a-Si.

Finally, I would like to show a sample layout design for the structure (d): a-Si on NP junction. The layout set of one pixel of the structure designed for the CMOS process in the hybrid process is shown in Fig. 5.13 step by step, from the deep N well to metal 1, as described in the

process flow above. There is an additional mask of a deep trench, which is designed to improve the isolation of pixels in an array. The sample layout set of a singular device (not in array) of the structure (d) designed for the CMOS process part is shown in Fig. 5.14, including the metallization from metal 2 to metal 6 and the passivation layer open. As stated previously, the passivation open will contact the a-Si with metal 6 at bottom and defines the a-Si active area. The passivation open window is designed outside the pixel area without blocking the photosensitive illumination area at the center of each pixel. The contact pads formed by metal 6 are designed for the GSG probe for both DC and AC measurements. The layouts of a singular device (not in array) for the UCSD post-process in the hybrid process is shown in Fig. 5.15. Only two masks are needed for the post-process: one for a-Si patterning and the other for the electrode metals. At last, Fig 5.16 shows the sample layout of a 32-by-32 array of the structure (d) designed for the CMOS process. The active region for a-Si has rotated to the upper right corner of each pixel in order to achieve a higher filing factor. The a-Si in each row will be connected to the corresponding open window at the head of each wire.

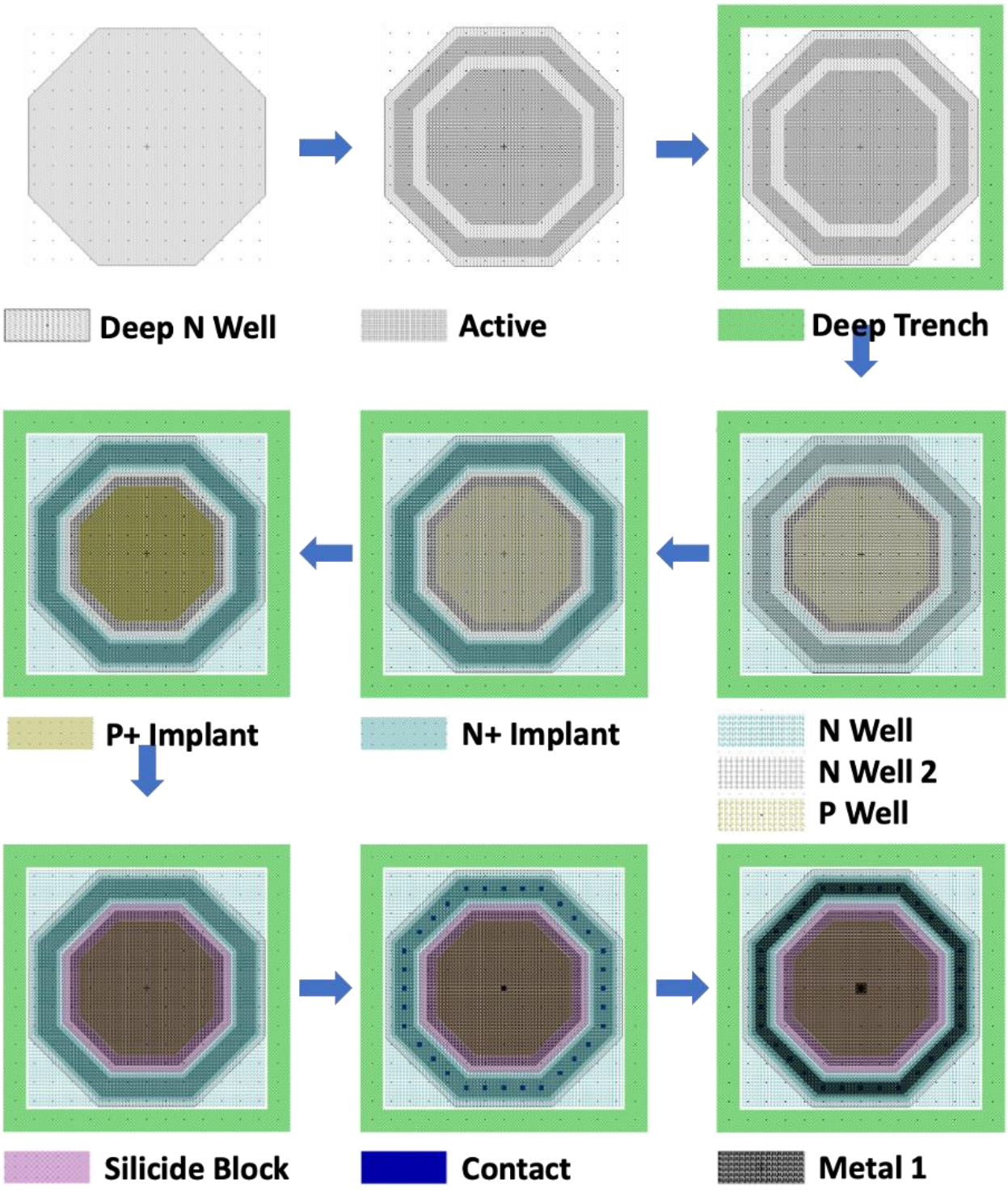

Figure 5.13 A sample layout set of one pixel of the structure (d): a-Si on NP junction designed for the CMOS process in the hybrid process, up to metal 1.

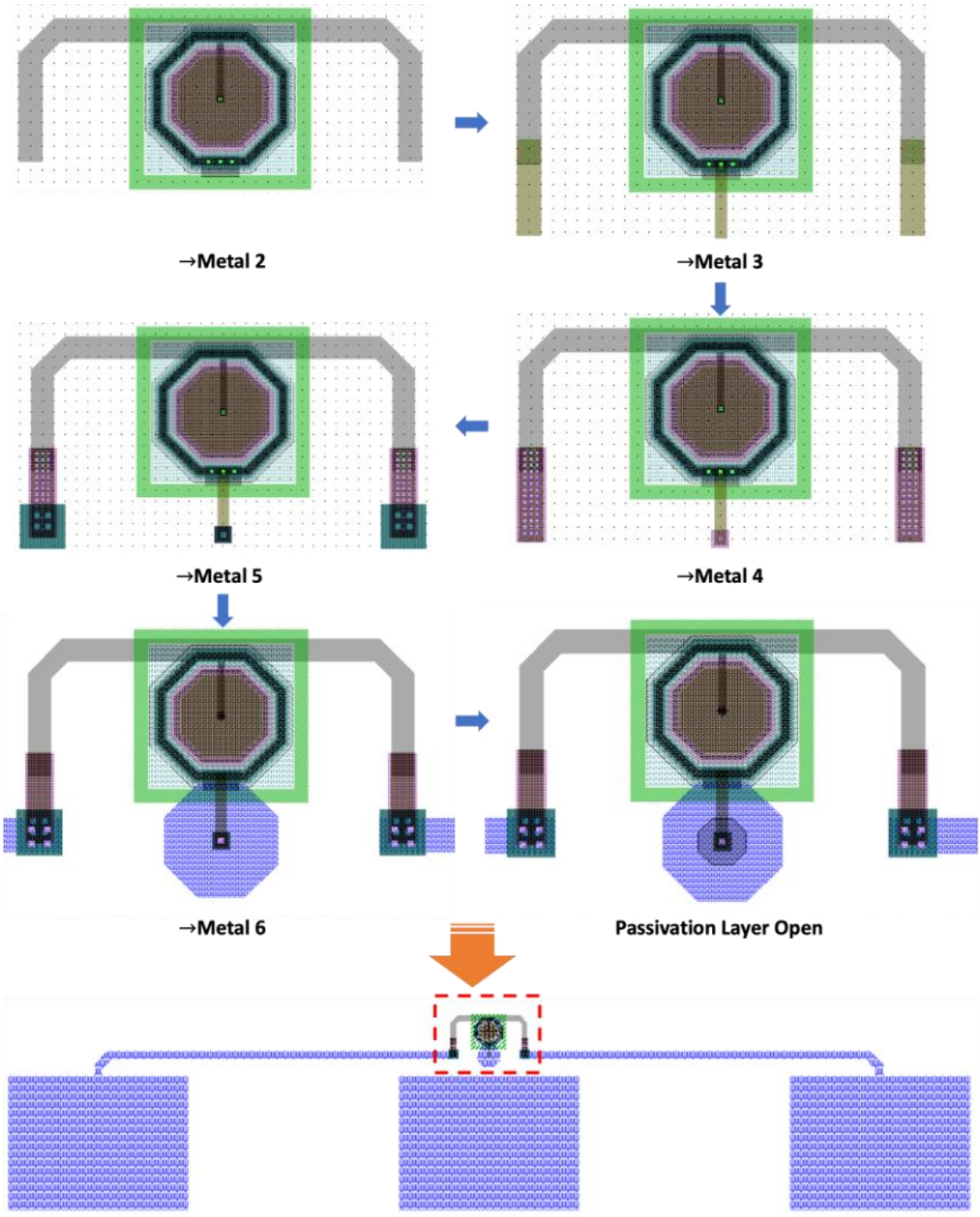

Figure 5.14 A sample layout set of a singular device (not in array) of the structure (d): a-Si on NP junction designed for the CMOS process in the hybrid process, including the metallization from metal 2 to metal 6 and passivation layer open.

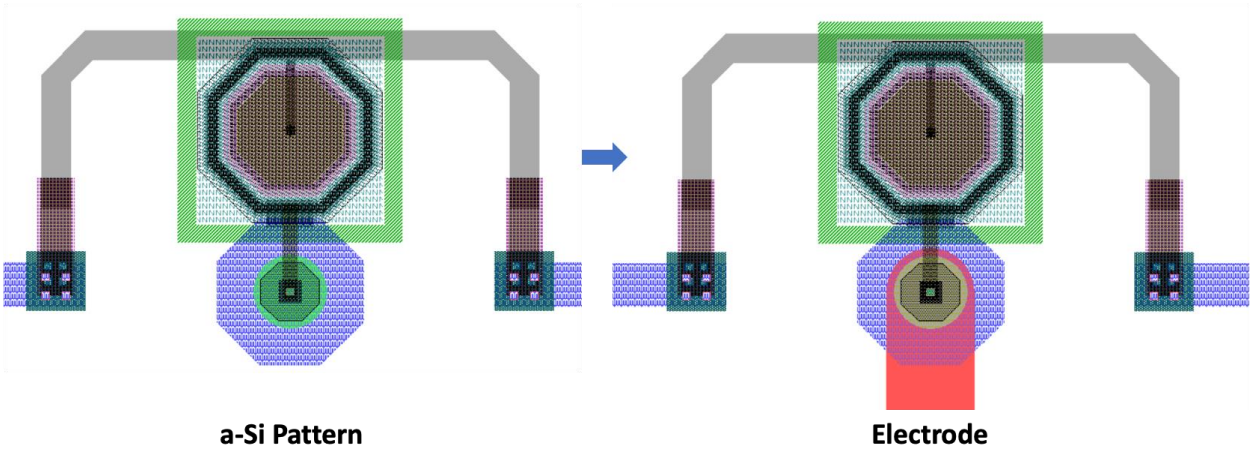

Figure 5.15 A sample layout set of a singular device (not in array) of the structure (d): a-Si on NP junction designed for the UCSD post-process in the hybrid process.

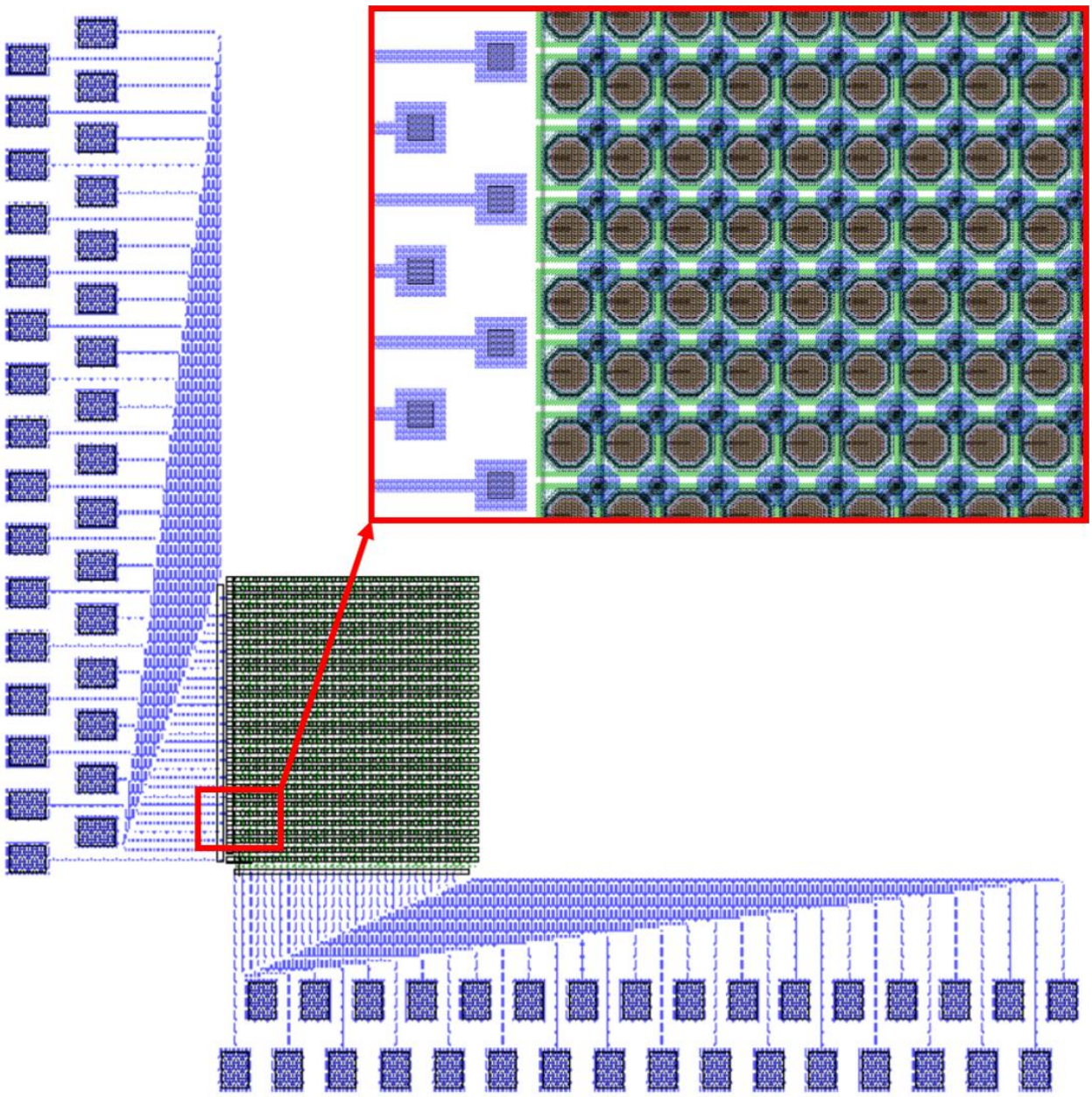

Figure 5.16 A sample layout set of a 32-by-32 array of the structure (d): a-Si on NP junction designed for the CMOS process in the hybrid process.

5.4 Future Work

In this chapter, I have demonstrated the first stage of the CMOS compatible process of CEP detectors. We have tested several a-Si deposition recipes by CMOS foundry and done some characterization of the a-Si layers, including optical microscope, SEM, EDS and device

performance characterizations. In parallel, we have also developed a hybrid CMOS compatible process for several CEP device structures and submitted the layout designs to tape-out.

In the next stage, we should first work with foundry to further improve the a-Si deposition recipe since the a-Si layer deposited by the foundry still contains “bubbles” which lowers the yield of devices. Second, based on the experience and device characterization from the Phase I hybrid process, we should be able to step into a complete CMOS process for the CEP detectors in the near future.

Portion of Chapter 5 is unpublished work of ongoing CMOS compatible process development for a-Si CEP detectors, with efforts of **Zhou, J.**, Miah, M.A.R., Yu, Y., and Lo, Y.H. The dissertation author is the primary investigator of the project.

Chapter 6. Conclusion and Outlook

6.1 Conclusion

In this dissertation, I have demonstrated the experimental characterization and physical models for the standard a-Si CEP detectors as well as other integrated a-Si CEP detectors. The CEP multiplication process utilizes the localized states naturally in the disordered material. So far, most of our CEP detectors are based on a-Si and the material is easily accessible, low cost and CMOS compatible. These characteristics make the a-Si CEP advanced in various integrated designs and applications.

The CEP mechanism is an efficient carrier multiplication process that has many advantages compared to the typical internal multiplication process for single photon detectors: impact ionization. One of the outstanding advantages is the unique intrinsically athermalized property. We have investigated the temperature sensitivity of the standard a-Si CEP detectors from 200 K to 350 K and found the nearly temperature independent characteristic, which is very different from impact ionization. Furthermore, we also developed a model to quantify the relative importance of the two possible mechanisms to excite localized carriers into mobile bands to support the carrier multiplication process.

The athermalized carrier multiplication mechanism in a-Si CEP detectors offers significant advantages over the impact ionization process in conventional APDs or SPADs. Temperature sensitivity is a key consideration for detector arrays with readout integrated circuits in LiDAR and imaging applications. The athermalized property for CEP mechanism can tolerate large temperature variations due to the ambient or local environment and achieve stable gain and photon detection efficiency, as well as low pixelation noise.

Since the a-Si CEP layer has high process compatibility and can collaborate with other absorption layers to amplify the absorbed photogenerated carriers from the absorption layer, we were able to extend the CEP detection wavelength from visible to long wave infrared. I have demonstrated the innovative design of a high performance, uncooled longwave-infrared photodetector made of a thin a-Ge layer and a thin a-Si layer. The photoexcitation mainly occurs between the bandtail states and mobile states of conduction band of a-Ge. Then the photogenerated carriers transport to a-Si CEP layer for multiplication and achieve high responsivity.

The detector has the highest detectivity among the reported room temperature LWIR quantum detectors and the NEP value sets the world record. This longwave infrared quantum detector has great potential to meet the performance and cost requirements for many applications including night vision, autonomous driving, robotic and machine vision, security, medical imaging, remote sensing, etc. It has a broad impact in both research and commercial fields.

Last but not least, I also showed the first stage of the CMOS compatible process development for CEP detectors. The characterization of a-Si deposition by foundry works in parallel with the design of the hybrid process: incorporating CMOS process and laboratory process. The hybrid process flow for both parts has been demonstrated with the sample layout set for singular device designs and pixel arrays. So far, we have successfully submitted the layout designs to foundry for the tape-out.

6.2 Outlook

In the previous work, we have discovered that the CEP mechanism is an efficient and attractive multiplication process for many device designs in various applications. Although in many device designs, we only fabricated the device on a silicon substrate, the same device structure

can also be fabricated on other substrates such as glass, metal and ceramic, by incorporating with a proper absorption medium and the a-Si CEP layer can simply serve as the gain medium.

For the development of a CMOS compatible process for CEP detectors, we can move to the next stage to further idealize the test recipe of a-Si deposition by foundry and then create a completely CMOS compatible CEP detector. Besides, we can design the integrated circuit for the CEP pixels, like an active/passive quenching system, as used in commercial CMOS devices.