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CMOS RF Power Amplifier Design Approaches for Wireless Communications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Sataporn Pornpromlikit

Committee in charge:

Professor Peter M. Asbeck, Chair
Professor Prabhakar R. Bandaru
Professor Andrew C. Kummel
Professor Lawrence E. Larson
Professor Paul K.L. Yu

2010

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The dissertation of Sataporn Pornpromlikit is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2010

DEDICATION

To my family.

EPIGRAPH

”Education is what remains after one has forgotten what one has learned in school.”

— Albert Einstein

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J. Jeong, S. Pornpromlikit, P. M. Asbeck, and D. Kelly, "A 20-dBm linear RF power amplifier using stacked silicon-on-sapphire MOSFETs," in *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 12, pp. 684-686, Dec. 2006.

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ABSTRACT OF THE DISSERTATION

CMOS RF Power Amplifier Design Approaches for Wireless Communications

by

Sataporn Pornpromlikit
Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)
University of California San Diego, 2010
Professor Peter M. Asbeck, Chair

This dissertation focuses on the design of CMOS power amplifiers for modern wireless handsets, where stringent linearity requirements and high power efficiency are difficult to achieve simultaneously. CMOS technology has been an attractive technology for research in fully-integrated transceivers due to its low cost and high-integration capability, as well as its continuously improving high-frequency performance. Its advantages, however, come at the cost of continuously reduced breakdown voltages, low isolation and high power loss in the substrate.

To address these limitations, a stacked-FET design technique is first developed to systematically divide the voltage stress among several transistors connected in series, allowing the use of a larger supply voltage. The voltage swing of each stacked device is added in phase to provide a larger output power to the load without the requirement of a large impedance transformation. To investigate this technique, a fully-integrated 20 dBm RF power amplifier is first implemented using 0.25-μm silicon-on-sapphire MOSFETs. By using triple-stacked FETs, the optimum load impedance for a 20 dBm power amplifier increases to 50 Ω so impedance transformation is not required at the

output. Measurement of a single-stage linear power amplifier shows a small-signal gain of 17.1 dB and a saturated output power of 21.0 dBm with a power added efficiency (PAE) of 44.0% at 1.88 GHz. With an IS-95 code division multiple access (CDMA) modulated signal, the power amplifier shows average output power of 16.3 dBm and PAE of 18.7% with ACPR below -42 dBc.

The concept is then further demonstrated at higher voltage and power level. A single-stage quadruple-stacked-FET linear power amplifier is presented using 0.28-μm 2.5-V standard I/O FETs in a 0.13-μm silicon-on-insulator (SOI) CMOS technology. The PA is designed to withstand up to 9 V of supply voltage before reaching its breakdown limit. The measured PA achieves a small-signal gain of 14.6 dB, a saturated output power of 32.4 dBm, and a PAE of 47% at 1.9 GHz with a 6.5-V supply. Using a reverse-link IS-95 CDMA modulated signal, the PA shows an average output power of up to 28.7 dBm with a PAE of 41.2% while meeting the adjacent channel power ratio requirement. The PA also shows an average output power of up to 29.4 dBm with a PAE of 41.4% while meeting the adjacent channel leakage ratio requirement of an uplink wideband code division multiple access (WCDMA) modulated signal. These performances are comparable to those of GaAs-based power amplifiers.

To fully exploit the advantages of higher-speed CMOS technology and the availability of co-integrated digital circuitry, a digital-intensive transceiver architecture is explored as an alternative in the second part of the dissertation. A single-ended digitally-modulated power amplifier (DPA) is demonstrated in a 0.13-μm 1.2-V SOI CMOS technology, to be used in a multi-standard RF polar transmitter. The amplitude modulation is done by digitally controlling the number of activated unit amplifiers whose currents are summed at the output. The DPA is designed for multi-mode multi-band functionality

by avoiding frequency-selective components, except for the final-stage output matching network. The measured DPA delivers a 24.9-dBm peak output power at 900 MHz with a maximum power efficiency of 62.7%. Similar high-efficiency performance is also exhibited at 1.92 GHz with a reconfigured matching network. By employing a digital pre-distortion technique, the DPA could meet linearity requirements for both the enhanced data rate for GSM evolution (EDGE) and WCDMA standards.

Chapter 1

Introduction

Since introduced to the world more than a century ago when Marconi successfully transmitted radio signals across the Atlantic ocean in 1901, the concept of wireless communications has tremendously evolved and become an integral part of our everyday life, influencing the way people live and interact with one another, thanks to inventions by countless scientists and engineers from many disciplines. Edwin Howard Armstrong's superheterodyne receiver in 1917, the invention of transistor in 1947 by John Bardeen, Walter Brattain and Wiiliam Shockley, Claude Shannon's information theory in 1948, to name a few, contributed greatly to how wireless communication networks and systems are implemented today.

On the electronics side, mobile user devices have become increasingly powerful over the years. Users can now make high-quality calls, read emails, download music and watch live streaming video, all from a single highly-integrated mobile device. The development of integrated circuits, and essentially CMOS technology, is a major reason that the cost of these devices is relatively low and affordable for the public, giving rise to an explosive growth of the mobile phone market in the last few decades. In 2009, there were more that 4 billion mobile subscriptions worldwide [14].

1.1 CMOS Technology and Scaling

CMOS technology has been the predominant technology in digital integrated circuits since it was invented in 1963. As the technology advances in each generation with shrinking transistor dimensions and an increasing production yield, more transistors per unit area, and thus more functionality, can be integrated onto a chip at a lower production cost. It was first observed by Gordon Moore in 1965 that the number of transistors on a single chip doubled every year [15]. In 1975, he updated his prediction to once every two years, which has become the guideline for the industry, as illustrated by the CPU transistor count and feature size trend lines in Fig. 1.1.

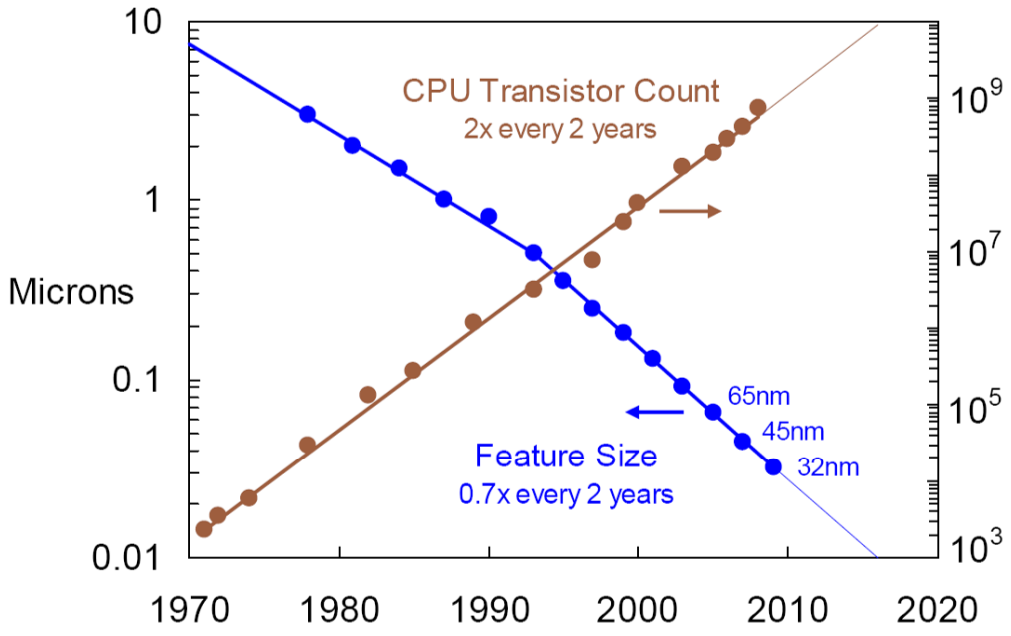


Figure 1.1: CPU transistor count and feature size trend [1].

Classical MOSFET scaling principle was first described by Dennard in 1974 [16]. His constant-field scaling methodology keeps short-channel effects under control

by scaling down the device voltages and the device dimensions, both horizontal and vertical, by the same factor κ so that the electric field remains unchanged. As a result, the circuit speeds up by the same factor and power dissipation per circuit is reduced by κ^2. Moreover, the power density remains unchanged while the power-delay product is improved dramatically by a factor of κ^3.

In reality, however, the oxide field has been increasing over the generations and CMOS technology has been scaled with mixed steps of constant-field and constant-voltage principles due to the standardized power-supply voltage of earlier-generation systems and the tradeoff between leakage current and circuit speed dictated by threshold voltage [17].

Even though CMOS was originally developed purely for digital circuits, it has become an increasingly attractive technology for analog and radio-frequency (RF) circuits over the years due to its cost advantage, high-integration capability and ever-improving high-frequency performance. For example, Intel's 45nm CMOS transistors have f_T and f_{MAX} values of more than 300 GHz. The same process also provides low-leakage transistors, high-voltage high-speed I/O transistors as well as precision resistors, precision capacitors, high-Q inductors and varactors [18].

Recently, analog and RF circuit design in CMOS is widely investigated both in academia and industry, spurred by the possibility of integrating the RF frontend and the digital baseband circuitry onto the same chip. A highly-integrated CMOS RF transceiver would result in a low production cost, a low power consumption, a better noise immunity, and the possibility of using digital signal processing (DSP) to improve RF performance.

1.2 Toward Fully-Integrated CMOS Transceivers

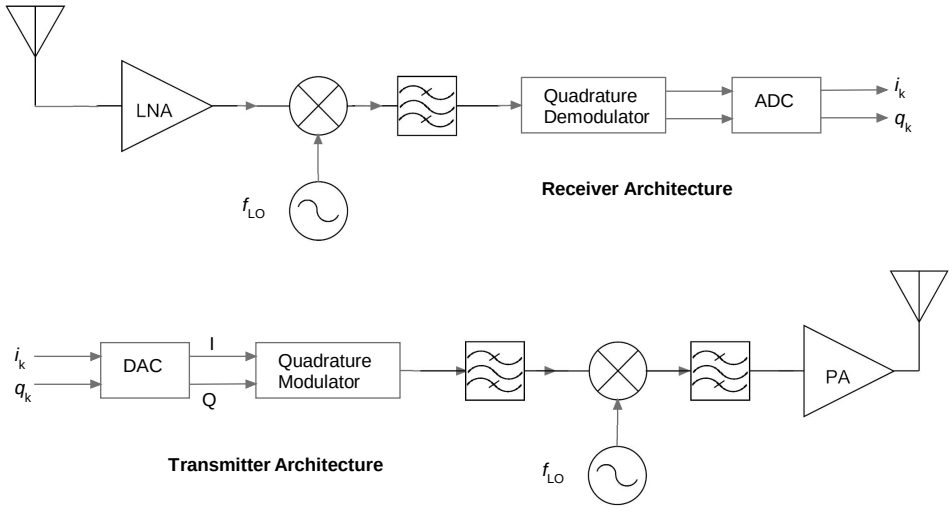


Figure 1.2: A basic radio-frequency transceiver.

A basic architecture of an RF transceiver is shown in Fig. 1.2. The analog portion of the receiver chain takes an RF analog signal and converts it into digital bitstreams. In the transmitter, the digital I/Q signals are converted to an analog signal, then frequency-translated by an up-conversion mixer. The resulting RF signal is finally amplified by a power amplifier (PA) to the required power level before radiated through the antenna.

CMOS technology is used to fabricate virtually all digital VLSI circuits and analog precision circuits, and as of late, many analog/RF frontend functions, such as low-noise amplifier (LNA), mixer, and voltage-controlled oscillator (VCO) have been successfully implemented in CMOS. Power amplifiers, however, are commercially implemented using GaAs-based technologies, either Metal Semiconductor Field Effect Transistors (MESFETs) or Heterojunction Bipolar Transistors (HBTs). The choice of using higher-performance more-expensive technologies is usually necessary for the power

amplifier, which is the most power-hungry component in any wireless transceiver. Integration of power amplifiers in CMOS suffers from two major drawbacks: low substrate resistivity and low breakdown voltages.

Integrating a power amplifier with other transceiver components and digital circuits on the same die can be harmful due to the poor substrate isolation in CMOS. Since many CMOS processes use a low-resistivity silicon substrate, large signals from a power amplifier can be conducted across the substrate and corrupt adjacent circuit blocks. In addition, the low resistivity of substrate results in low-quality factor passive components due to the energy coupled into the lossy substrate. CMOS technology also has much lower breakdown voltages compared to other technologies, especially as the device dimensions scaled down in each generation, limiting usable voltage headroom. These drawbacks eventually result in low output power and poor power efficiency in power amplifier design.

1.3 Power Amplifier Design

Power amplifiers have been traditionally categorized into different classes (A, B, C, D, E, F, etc.) based on factors such as conduction angles, input signal overdrive, and operating current and voltage waveforms. These classes are compared in Table 1.1 in terms of power efficiency and linearity, which are the most significant parameters for power amplifier design. For class A, AB and C, the input signal overdrive is relatively small and the device is operated more as a current source. A simplified schematic is illustrated in Fig. 1.3. In small-signal amplifiers, a conjugate-match load resistance is typically selected to optimize gain. In power amplifiers where large signals are involved, however, physical limits of the device both in terms of voltage and current come into

play. The load resistance can be selected based on the device's load line as shown in Fig. 1.4 to optimize for the the best power and efficiency. The drain voltage of the output transistor swings between ground and $2V_{DD}$ depending on the input power level. The maximum RF output power that a transistor can provide is given by its power triangle,

$$P_{max} = \frac{1}{8} \cdot I_{max} \cdot (V_{max} - V_{min}). \tag{1.1}$$

The drain efficiency (η_d) and the power-added efficiency (PAE), in terms of drain efficiency and power gain G, can be calculated as,

$$\eta_d = \frac{P_{out}}{P_{dc}}, \tag{1.2}$$

$$\begin{aligned} PAE &= \frac{P_{out} - P_{in}}{P_{dc}} \\ &= \eta_d \cdot (1 - \frac{1}{G}). \end{aligned} \tag{1.3}$$

Table 1.1: Comparison of different power amplifier classes

Class	**A**	**AB**	**B**	**C**	**D**	**E**	**F**
Conduction angle (%)	100	50-100	50	<50	50	50	50
Max. efficiency (%)	50	50-78.5	78.5	100	100	100	100
Linearity	Excellent	Good	Good	Poor	Poor	Poor	Poor

A class-A power amplifier is operated in full input and output ranges with no waveform clipping, and thus, provides the best linearity. For class AB, B, and C, the conduction angle is reduced accordingly by lowering the gate bias voltage to trade-off

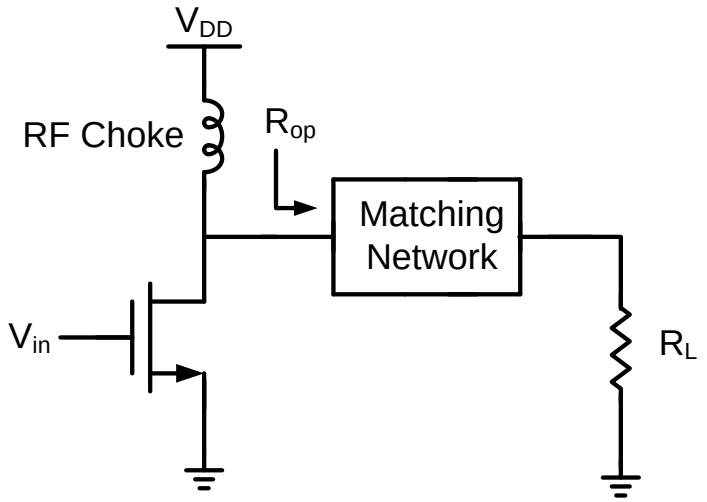


Figure 1.3: A simplified conventional power amplifier schematic.

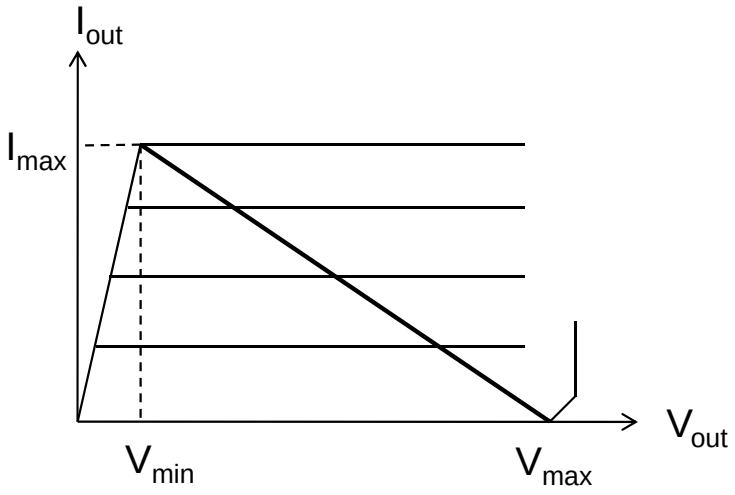


Figure 1.4: A device's load-line match.

linearity for better efficiency, as illustrated in Fig. 1.5. These classes can be referred to as linear-mode, even though linearity becomes relatively poor for a class-C power amplifier due to the severely clipped output signal. The maximum drain efficiency can be calculated as a function of the conduction angle (θ) as expressed in (1.4) [19]. For an ideal class-A power amplifier, assuming a zero on-resistance or zero knee voltage (V_{min} = 0), the maximum drain efficiency is 50% and will be higher for smaller conduction angle. The drain efficiency reaches 78.5% for a class-B power amplifier (θ = 180^o).

$$\eta_d(\theta) = \frac{1}{4}\frac{\theta - \sin(\theta)}{\sin(\theta/2) - (\theta/2)\cos(\theta/2)} \cdot \frac{V_{max} - V_{min}}{V_{max} + V_{min}}. \tag{1.4}$$

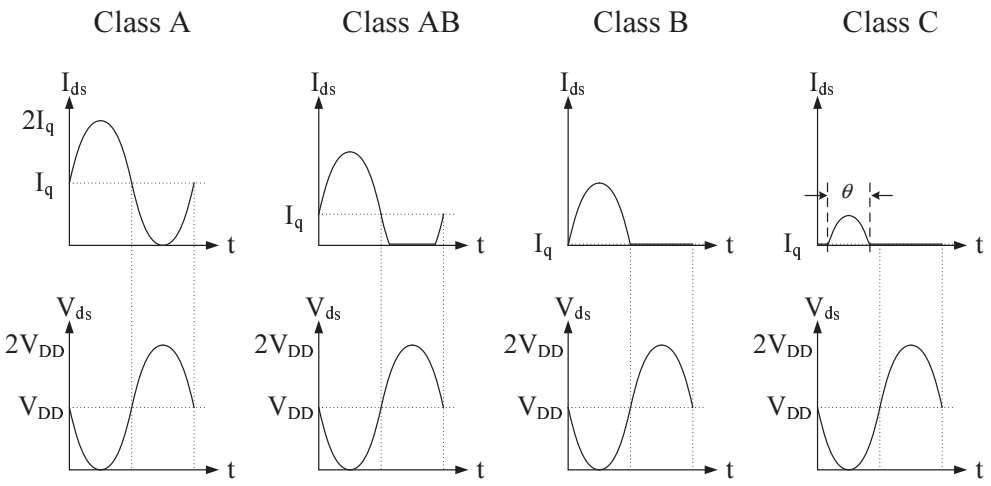


Figure 1.5: Current and voltage waveforms of different linear power amplifiers.

For class D, E, and F, the output transistor is driven with a large input overdrive such that it operates more as a switch, and thus, can be referred to as switching-mode power amplifiers. These classes provide high-efficiency nonlinear power amplification and are differed from one another by operating voltage and current waveforms that can be achieved through circuit topology and harmonic termination. The current and voltage

waveforms of different switching-mode power amplifiers are shown in Fig. 1.6. The main concept is to reduce the overlap between current and voltage waveforms across the switch to minimize power dissipation.

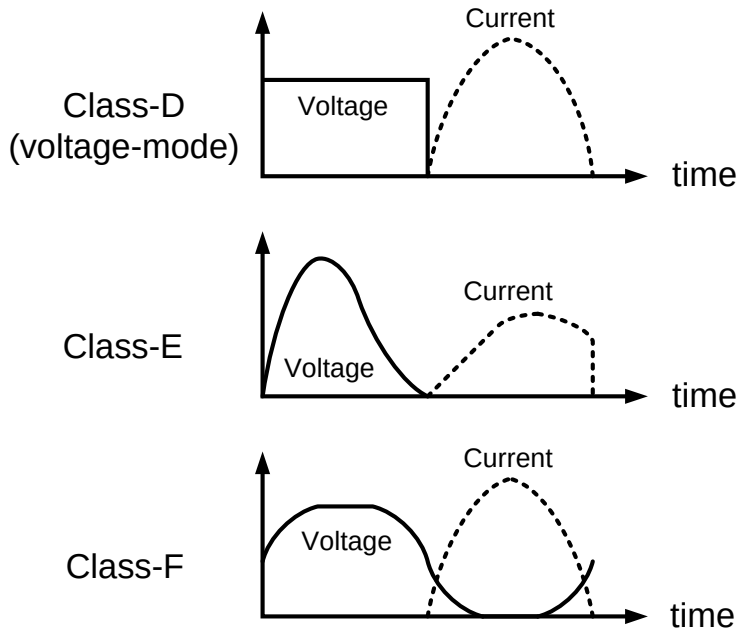


Figure 1.6: Current and voltage waveforms of different switching-mode power amplifiers.

1.4 Wireless Communication Systems

The first- and second- generation mobile communication systems are mainly used for voice communications. While the first-generation systems such as advanced mobile phone service (AMPS) are analog systems, the second-generation systems, introduced in late 1980s, are digital systems. There are several digital standards worldwide such as the global system for mobile communications (GSM), IS-95/98 code-division multiple-access system (CDMA), IS-136 time-division multiple-access system (U.S.

TDMA or D-AMPS), and the personal digital cellular (PDC) system in Japan. Among them, the European-developed GSM has been the most widely used standard in the world. To allow for data, internet, and other connectivities, new technologies such as the general packet radio system (GPRS) and the enhanced data rate for GSM evolution (EDGE) were next introduced as 2.5-generation systems. The third-generation systems such as cdma2000-1x and wide-band code division multiple access (WCDMA) systems, were then introduced in late 1990s, providing high-speed video and multimedia services as well as larger-capacity voice communications.

1.4.1 Digital Modulation and Multiple Access Techniques

Modulation is the process of translating an original baseband signal into a band-pass signal at a high frequency suitable for transmission. In analog systems, this process can be performed by varying amplitude (AM), phase (PM) or frequency (FM) of the high-frequncy carrier. The digital equivalents of AM, PM, and FM are called amplitude shift keying (ASK), phase shift keying (PSK), and frequency shift keying (FSK), respectively. The advantages of digital modulation include greater noise immunity, more robustness to channel impairments, easier multiplexing of voice, data, and image information, and better security. Popular digital modulations are binary phase shift keying (BPSK), *M*-ary phase shift keying (QPSK, OQPSK, etc.), minimum shift keying (MSK), and *M*-ary quadrature amplitude modulation (16 QAM and 64 QAM).

A digital baseband signal can be a binary waveform or a multi-level (*M*-ary) digital signal, where the original binary data stream is subdivided into groups of $log_2(M)$ bits and each group is converted to one of *M* possible levels. Each group of bits is called "symbol" and the symbol rate is reduced from the original bit rate by $log_2(M)$, relax-

ing bandwidth requirements. When choosing a modulation scheme, there are always tradeoffs between power efficiency and bandwidth efficiency (η_{BW}) defined as [20]

$$\eta_{BW} = \frac{R}{BW} \quad \text{bps/Hz}, \tag{1.5}$$

where R is data rate in bits per second and BW is the bandwidth of the modulated RF signal. For example, the GSM system employs a Gaussian pulse shaping minimum shift keying (GMSK) modulation, resulting in a carrier with a constant envelope. This modulation allows for the use of a high-efficiency switching-mode power amplifier. In order to increase the data rate while keeping the same bandwidth, the EDGE system is introduced using an 8-ary PSK modulation to achieve a higher bandwidth efficiency. This modulation, however, results in a varying envelope with approximately a 3.2-dB peak-to-average ratio (PAR), requiring a lower-efficiency linear power amplifier.

Waveforms of digital modulation schemes can be generally expressed in the following complex envelope form

$$M(t) = I(t) + jQ(t) = A(t)e^{j\varphi(t)}, \tag{1.6}$$

$$I(t) = \sum_k I_k p_I(t - kT_s - \tau), \tag{1.7}$$

$$Q(t) = \sum_k Q_k p_Q(t - kT_s - \tau), \tag{1.8}$$

where *I(t)* and *Q(t)* are in-phase and quadrature envelope waveforms, respectively, and can be represented in terms of a two-dimensional constellation diagram. For examples, constellation of QPSK, OQPSK, and π/4-QPSK are illustrated in Fig. 1.7.

The trajectory from one constellation point to another will determine the envelope variations of the output RF signal. Notice that QPSK and OQPSK have a similar constallation diagram. In QPSK, the trajectory can go through the origin of the complex plane, resulting in a changing envelope amplitude. In OQPSK, the quadrature data streams are offset in time by half the symbol period relative to each other so the phase step is only $\pm 90^o$ and consequently the transition through the origin is avoided.

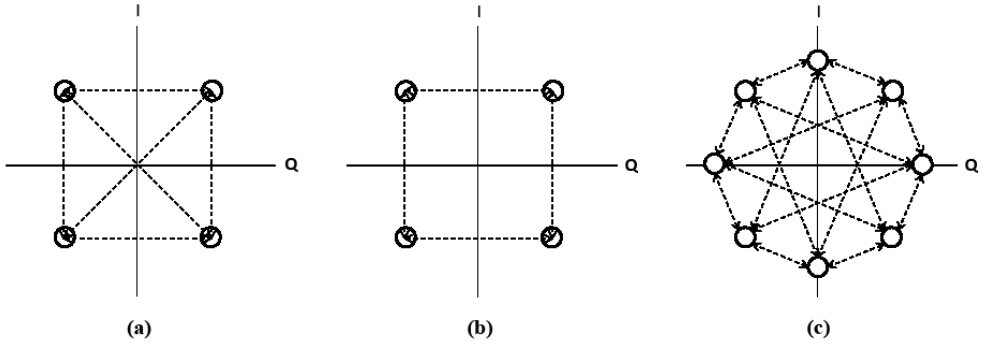


Figure 1.7: Constellation diagrams of (a) QPSK, (b) OQPSK, and (c) π/4-QPSK.

The modulation techniques provide the basis for transmitting signals from a transmitter to a receiver. When multiple transceivers are communicating, multiple access techniques are required. In the most simple case when only two transceivers are talking, two common approaches are time-division duplexing (TDD) and frequency-division duplexing (FDD). In TDD, the same frequency band is used for both transmit path and receive path but the system is alternating in time between transmitting and receiving. In FDD, two different frequency bands are dedicated for the transmit and receive paths with a base station acting as a translator.

Similarly, in the case of two-way communications among multiple transceivers, the frequency band can be partitioned into many channels (frequency-division multiple

access, FDMA), where each channel is assigned to one user, or the same frequency band can be time-shared by each user (time-division multiple access, TDMA). Another popular technique for multiple access is code-division multiple access (CDMA), where each bit of the baseband data is translated to a pre-assigned orthogonal digital code before modulation. As a result of the encoding operation, the baseband data of each user is spread over the entire available bandwidth while the spread spectra of unwanted signals can be viewed as white Gaussian noise due to their low correlation with the assigned code.

1.4.2 Modern Wireless Communication Standards

With an increasing number of emerging mobile applications and a demand for higher data rate and network capacity, it is becoming necessary for each mobile device to support multiple standards. Integrating all the hardware for these standards into the same module, however, is a challenging task due to the complexity and stringent requirements of each modern standard. In this work, we first look at the details of some modern wireless standards and their requirements relevant to uplink transmitter design, as summarized in Table 1.2.

The EDGE system uses the existing GSM infrastructure and licenses. The channel spacing is also 200 kHz, the same as the GSM spectrum, but its data rate is triple that of GSM by using 8PSK modulation. Consequently, the PAR is 3.2 dB, instead of a constant envelope in GSM. The GSM/EDGE standard specifies that the transmitter output meets error vector magnitude (EVM) and spectral mask requirements to avoid blocking the spectrum of neighboring channels. The error vector is defined as the difference between the ideal constellation point and the actual transmitted constellation point. The

Table 1.2: Uplink specifications of some wireless communication standards [3, 13]

Standard	**IS-95**	**GSM/EDGE**	**WCDMA**
Uplink frequency (MHz)	824-849 (1850-1890)	890-915 (1710-1910)	1920-1980
Downlink frequency (MHz)	869-894 (1930-1990)	935-960 (1805-1990)	2110-2170
Modulation	OQPSK	GMSK/$\frac{3\pi}{8}$-8PSK	HPSK
Duplex	Full-duplex FDD	Half/Full-duplex FDD	Full-duplex FDD
Multiple access	DS-CDMA	TDMA	DS-CDMA
Channel data clock rate	1.2288 Mchip/s	270.83 kbit/s	3.84 Mchip/s
Required channel bandwidth	1.25 MHz	200 kHz	5 MHz
Maximum average output power	23-30 dBm	30-33/22-26 dBm (E2 and E3)	24 dBm (Class 3)
Peak-average power ratio	4.5-5.5 dB	0/3.2 dB	3.5 dB
TX. power control range	73-80 dB	30 dB	74-80 dB

RMS value of EVM should be lower than 9% and the peak value of the EVM should be lower than 30%. For the spectral mask, the most critical points are at 400 kHz and 600 kHz offsets, where the relative power needs to be below -54 dB and -60 dB respectively.

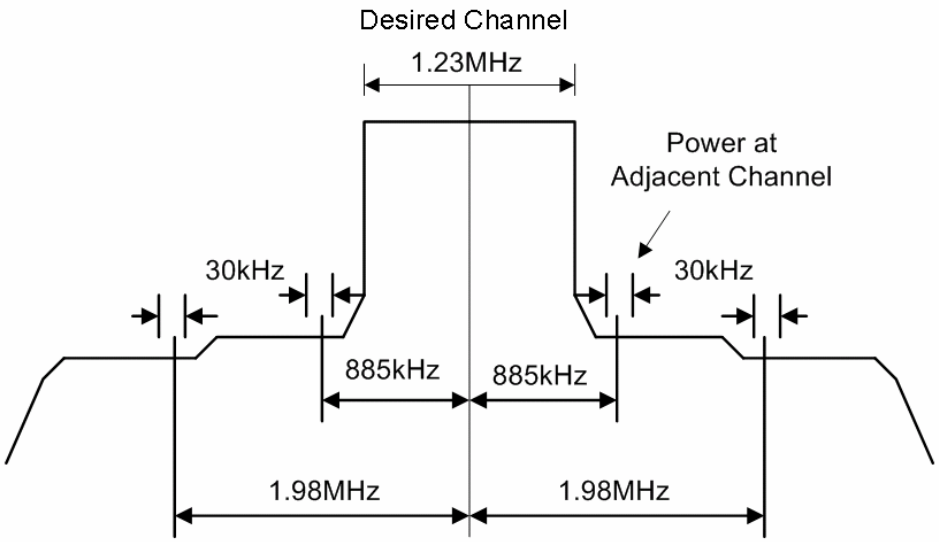


Figure 1.8: ACPR requirement for IS-95 CDMA.

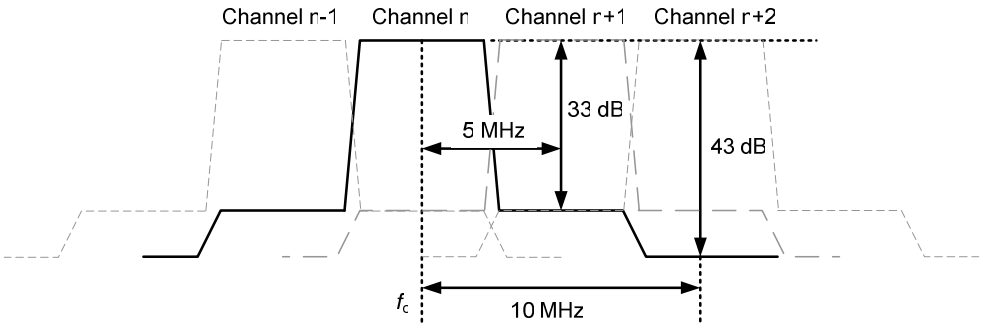


Figure 1.9: ACLR requirement for WCDMA.

The IS-95 CDMA signal occupies a bandwidth of 1.25 MHz and has a PAR of 5.5 dB. The WCDMA has a bandwidth of 5 MHz and a PAR of 3.5 dB with one

data channel active. Moreover, the power control dynamic range specification requires the mobile transmitter to span from full power to -50 dBm. The most stringent linearity requirement for these standards is the adjacent channel power specification, which compares the desired channel power to the adjacent channel power due to noise and distortion from system nonlinearity. Fig. 1.8 and Fig. 1.9 illustrate the adjacent channel power ratio (ACPR) and adjacent channel leakage ratio (ACLR) specifications for the IS-95 and WCDMA standards respectively.

1.5 Digital RF Transmitters

As digital circuits in advanced CMOS technologies are able to operate at higher microwave frequencies, the use of DSP becomes highly attractive in power amplifier and transmitter design. In a fully-integrated CMOS transmitter, DSP techniques can be employed to improve the overall system performance. To fully realize the advantages of higher-speed CMOS technology, the next step is to employ a more digital-intensive or all-digital transmitter architecture, where most or all of the analog building blocks are replaced by digital functionalities. An all-digital solution, in particular, would benefit from the technology scaling as well as provide high configurability to the system.

This research topic has been highly active in recent years, especially in the context of multi-mode multi-band transmitters, which would help facilitate an adoption of new wireless communication standards and provide global-roaming capability in a single mobile device. Multi-standard transmitters are conventionally implemented by combining several discrete transmitters, where each one is designed for a specific standard, increasing complexity and cost of the device. To solve this redundancy problem, several multi-mode polar-based digital transmitter architectures have been proposed in

the literature. Most of the works, however, only deliver a low output power level and still need multiple external power amplifiers for each frequency band.

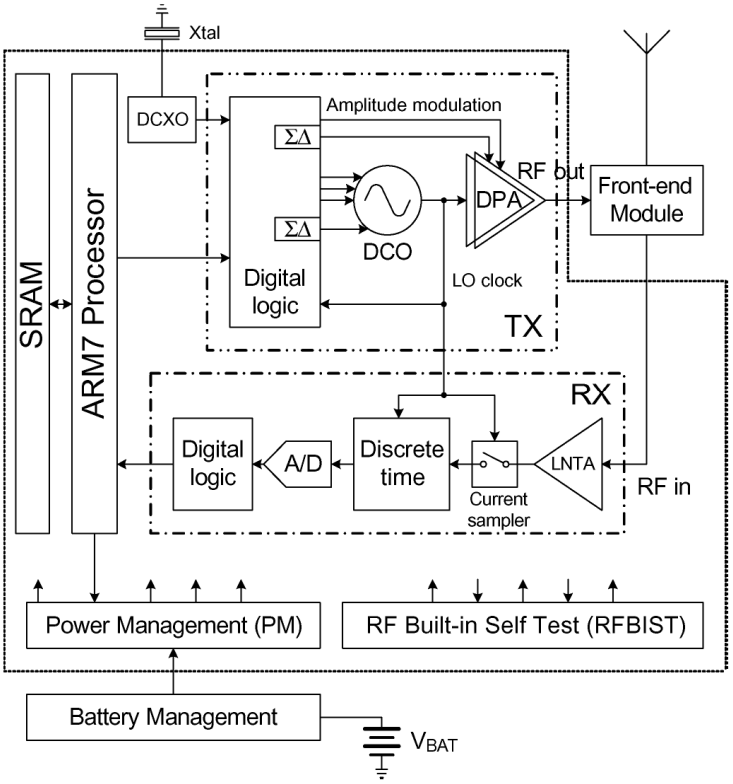


Figure 1.10: An all-digital transmitter for GSM/EDGE [2].

In [2], an all-digital transmitter for GSM and EDGE is proposed as shown in Fig. 1.10. The transmitter utilizes an all-digital PLL to perform the direct frequency modulation while the amplitude modulation is done by regulating the number of active NMOS switches. It meets all the specifications for GSM with a maximum output power of 10 dBm. The EDGE spectral mask is also met with a 10-dBm margin and an RMS EVM of 1.2%.

In [3], a multi-mode direct-digital RF modulator is implemented as shown in

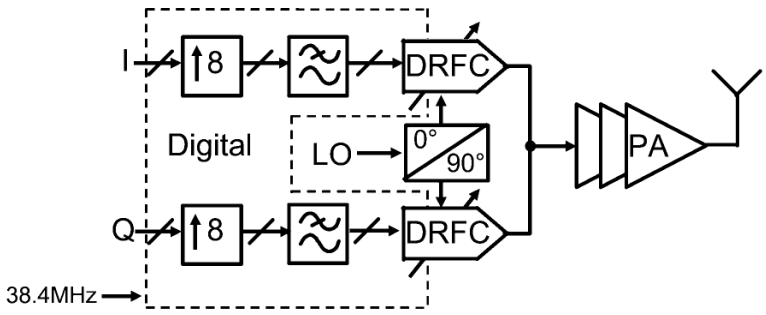


Figure 1.11: A current-steering-based direct-digital RF modulator for WCDMA, EDGE and WLAN [3].

Fig. 1.11. In this work, the digital amplitude control is done using a segmented current steering topology. The transmitted power control range is achieved by controlling the external control voltage of the reference circuitry. The measured transmitter achieves 90 dB of power control range and meets most of the specifications for WCDMA, EDGE and WLAN, providing a maximum output power of 25 dBm with an external high-gain power amplifier module.

In [4], a digitally-modulated CMOS power amplifier for 64-QAM OFDM system is reported as shown in Fig. 1.12, exhibiting a 20-MHz channel bandwidth. The amplitude modulation is done by controlling the number of active unit amplifiers through their cascode stages. Oversampling and four-fold linear interpolation techniques are employed to suppress the spectral images from the discrete-time to continuous-time conversion of the envelope, resulting in a wide bandwidth. A PAE of 6.7% is achieved with an output power of 13.6 dBm for 64QAM OFDM signals.

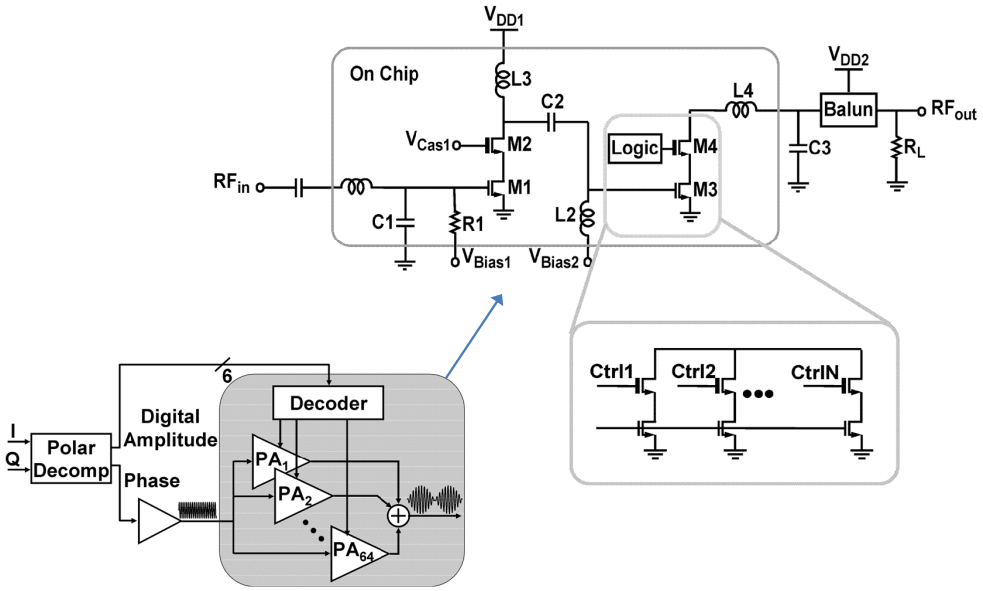


Figure 1.12: A digitally modulated polar power amplifier with a 20-MHz channel bandwidth [4].

1.6 Dissertation Focus and Organization

The main focus of this research work is to explore several design techniques that can enable the implementation of fully-integrated RF power amplifiers in CMOS. As discussed in all previous sections, the power amplifier is a vital part of any wireless transmitter, consuming the most power among all the building blocks. It needs to be designed for the highest power efficiency possible to maximize the mobile device's battery life, while meeting the output power and linearity requirements of targeted wireless communication standards. Moreover, multi-mode multi-band operations should be possible with minimum hardware redundancy. To achieve these objectives, a circuit approach is first developed to overcome the low breakdown problem in CMOS, allowing the benefits of Moore's law to be applied at higher power level than previously possible. A new amplitude modulation scheme is then developed in the later part to simplify

the transceiver architecture, employing the high integration levels attainable in CMOS. The proposed digitally-controlled technique enables direct software programmability of the transceiver output, which can facilitate multi-mode multi-band operations and programmable functionality.

The dissertation consists of four chapters. The background and fundamentals of power amplifier design has been introduced in the first chapter, together with a brief discussion on modern wireless communication standards and their performance requirements related to power amplifier design.

Chapter 2 will focuses on the stacked-FET technique to address the low breakdown problem in CMOS power amplifiers. It begins by discussing breakdown mechanisms in short-channel CMOS devices. The impedance matching network design and the associated loss are then examined to illustrate how a reduced voltage headroom can lead to a lower power efficiency in power amplifiers. Next, existing power combining techniques are reviewed and the stacked-FET topology is proposed as an attractive solution. Finally, the circuit design, implementation and measurement results are presented and discussed.

In chapter 3, a new polar-based digital RF transmitter architecture will be explored for multi-mode multi-band applications. The overall transmitter architecture is first proposed, making use of available RF switches in an advanced silicon-on-insulator CMOS process. Next, the system-level requirements are examined and the circuit design, implementation and measurement results are then discussed in details including possible strategies for achieving power control requirements.

Chapter 4 concludes the whole dissertation.

Chapter 2

Stacked-FET Power Amplifiers

2.1 Introduction

CMOS technology has become a desirable choice for research on single-chip radio transceivers in recent years due to its low cost and high-integration capability. Among other advantages, CMOS power amplifiers (PAs) offer the potential of reducing complexity and cost by enabling the combination of a complete transceiver and digital baseband circuitry on the same chip. However, designing a high-performance RF PA on CMOS remains a challenging task, especially with the on-going technology scaling to deep submicron dimensions [21–23].

The critical issues for CMOS PA design are the low breakdown voltage and high knee voltage of the device, which limit the allowable drain voltage swing. Various breakdown and degradation mechanisms in submicron CMOS include gate oxide breakdown, hot carrier degradation, punch-through and drain-bulk breakdown [6, 24]. The gate oxide breakdown is a catastrophic effect that permanently damages the device while the hot carrier degradation can cause a gradual degradation in the device performance over time. These effects should be avoided by ensuring in the design that the transistor's drain-gate,

gate-source and drain-source voltages (V_{DG}, V_{GS}, and V_{DS}) do not exceed pre-specified values [24]. To obtain high output power, a typical approach is to increase the device size for higher drain current swing, resulting in lower input impedance, and thus, more difficult input matching design. More severely, the required output impedance transformation ratio from the original load impedance to 50 Ω becomes too high, especially for Watt-level output power required in modern wireless applications, resulting in high loss in the output matching network, and thus, low efficiency.

2.2 Breakdown Mechanisms in CMOS

Breakdown occurs in a short-channel MOSFET when the drain voltage relative to the gate voltage and the source voltage exceeds a certain value. The resulting high electric field can lead to various phenomena that cause a performance degradation over time or an eventual device failure. Those phenomena are discussed in this section.

2.2.1 Gate Oxide Breakdown

When a large electric field is applied across an oxide layer, significant electron tunneling can take place. The time-dependent tunneling current usually decreases gradually until the oxide suffers a dielectric breakdown, where the oxide layer permanently loses its property as a good insulator. This phenomena involves many physical mechanisms such as impact ionization in the oxide layer, creation of electron and hole traps in the oxide, electron and hole trapping, and creation of surface states at the oxide-silicon interface [17]. This breakdown process is especially critical in CMOS as the gate oxide thickness is reduced in each process generation. To avoid this failure, it is important to keep the gate-drain and the gate-source voltages below pre-specified values.

2.2.2 Hot Carrier Degradation

Under a large drain-source voltage in a short-channel MOSFET, the electric field across the channel can be extremely high. Electrons gain energy from the field as they move along the channel and possess high kinetic energy close to the drain enough to generate more electrons and holes by impact ionization as shown in Fig. 2.1. These secondary electrons and holes result in substrate current and higher drain current. The substrate current will create a voltage drop that tends to forward-bias the source junction and lower the threshold voltage. As a result, the channel current increases and the positive feedback is triggered. This process usually causes a gradual degradation in device performance but can often result in permanent damage to the MOSFET as hot carriers are injected into the oxide in the gate-drain overlap region. To prevent this degradation process, the drain-source voltage should be kept below a pre-specified value and a large drain current should be avoided when the drain-source voltage is high.

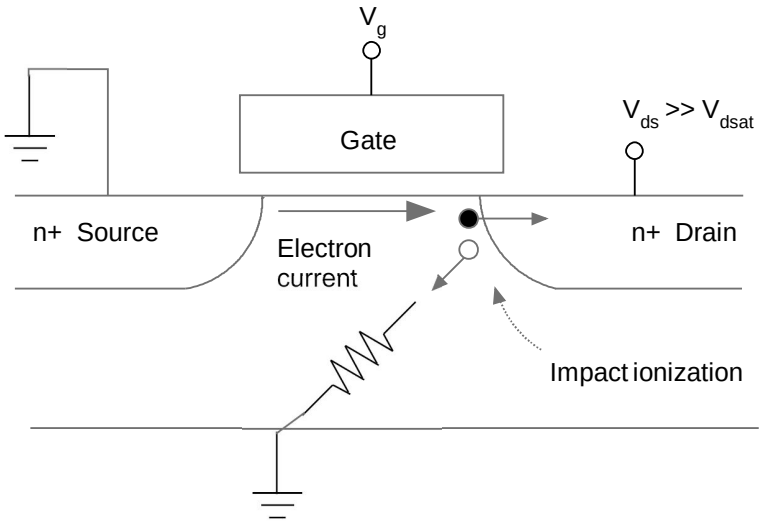


Figure 2.1: Impact ionization at the drain.

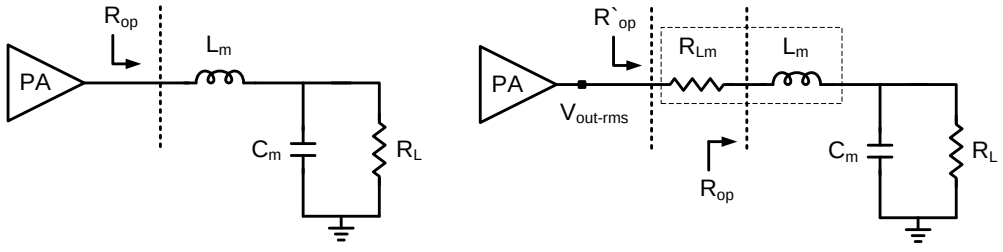
2.2.3 Punch-Through

Punch-through can occur when the drain-bulk depletion region extends all the way to meet the source-bulk depletion region under a large drain-source voltage, resulting in a direct flow of current from drain to source. This process can occur even in an absence of a gate bias voltage and become a significant reliability problem with a shorter channel length.

2.2.4 Drain-Bulk Junction Breakdown

In a standard CMOS process, the bulk is connected to ground or a fixed electrical potential. The drain-bulk junction diode experiences a reverse bias proportional to the drain voltage. Therefore, it is important to limit the drain voltage within the reverse breakdown voltage of the drain-bulk junction diode.

2.3 Impedance transformation and Matching Network Loss



(a) (b)

Figure 2.2: Impedance transformation network: (a) an L-match network and (b) an L-match network with inductor loss.

In RF power amplifier design, it is typically necessary to match a 50-Ω load

to a smaller impedance in order to achieve a larger output power. For a linear power amplifier, the optimal impedance in terms of output power and supply voltage can be expressed as,

$$R_{op} = \frac{1}{8} \cdot \frac{(V_{max} - V_{min})^2}{P_{out}} = \frac{1}{8} \cdot \frac{(2V_{dd} - V_{min})^2}{P_{out}}. \tag{2.1}$$

To provide a 1-W output power with a 1.8-V supply and a knee voltage of 0.5 V, for example, an optimal impedance of 1.2 Ω is required. The optimal impedance becomes even smaller as the breakdown voltage is reduced further in advanced CMOS technology, resulting in high power loss in the matching network. Fig. 2.2(a) illustrates an L-match, which is the most widely used impedance transformation network with a quality factor Q_m defined as

$$Q_m = \sqrt{\frac{R_L}{R_{op}} - 1}, \tag{2.2}$$

and the values of matching components L_m and C_m can be obtained from

$$L_m = \frac{Q_m R_{op}}{\omega} \tag{2.3}$$

$$C_m = \frac{Q_m}{\omega R_L}. \tag{2.4}$$

The power loss of an on-chip L-match network is generally dominated by the loss of the matching inductor, as shown in Fig. 2.2(b), due to its low quality factor Q_L defined as

$$Q_L = \frac{\omega L_m}{R_{Lm}}. \tag{2.5}$$

At the resonance frequency, the optimal impedance becomes

$$R'_{op} = R_{op} + R_{Lm}. \tag{2.6}$$

The total power flowing into the impedance transformation network and the power delivered to the load are

$$P_{in-m} = \frac{V^2_{out-rms}}{R_o p + R_{Lm}} \tag{2.7}$$

$$P_{out-m} = V^2_{out-rms} \frac{R_{op}}{(R_{op} + R_{Lm})^2}. \tag{2.8}$$

Consequently, the efficiency of the matching network and the effective impedance transformation ratio can be calculated as

$$\eta_m = \frac{Q_L}{Q_L + Q_m} \tag{2.9}$$

$$r'_m = \eta_m \cdot \frac{R_L}{R_{op}} = \eta_m \cdot r_m. \tag{2.10}$$

Obviously, the efficiency of an impedance transformation network will depend on both the quality factor of matching components and the intended impedance transformation ratio.

2.4 Power Combining Techniques: Prior Art

Due to the low breakdown voltages in CMOS, achieving a large output power with a single device leads to a high loss in the matching network as discussed in the

previous section. Moreover, the device is usually required to conduct a large drain current, making the power efficiency more sensitive to supply parasitics. An alternative way is to use multiple devices and their power can be combined to reach the required output power. Several approaches exist in the literature that can combine power of multiple devices in parallel. Among them, transformer-based techniques have been widely investigated in recent time with some excellent results [5, 24, 25]. However, most of these techniques are only suitable for nonlinear amplification while on-chip transformers require a large die area. In [5], a fully-integrated CMOS power amplifier was first demonstrated using slab inductors to realize an on-chip distributed active transformer structure (DAT) as shown in Fig. 2.3. It delivers a 2-W output power at 2.4 GHz with a 41% PAE using a 2-V supply.

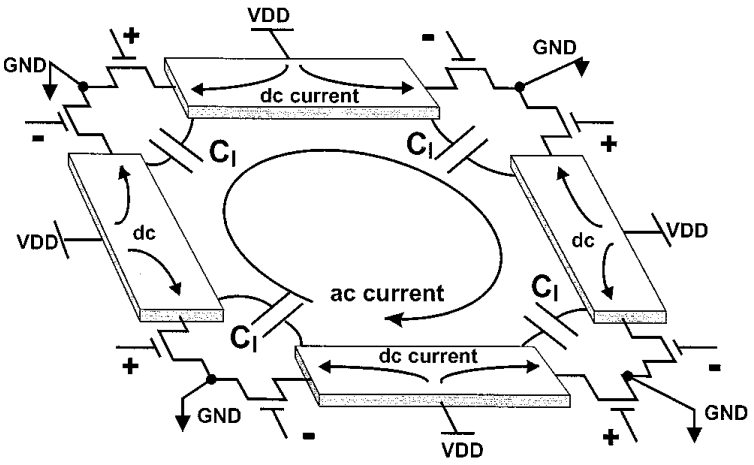


Figure 2.3: Distributed active transformer structure [5].

Alternatively, multiple devices can be combined in series such that the output voltage swing increases while avoiding any device exceeding its breakdown voltage limits. The most basic technique of this type is the cascode configuration, commonly employed to improve gain performance in lower-frequency amplifier design. As shown

in Fig. 2.4, common-source and common-gate transistors are connected in series to allow a larger voltage swing at the drain of the common-gate device. Unfortunately, the voltage stress is not equally divided between the two transistors and the common-gate transistor is stressed more, especially across its drain and gate terminals.

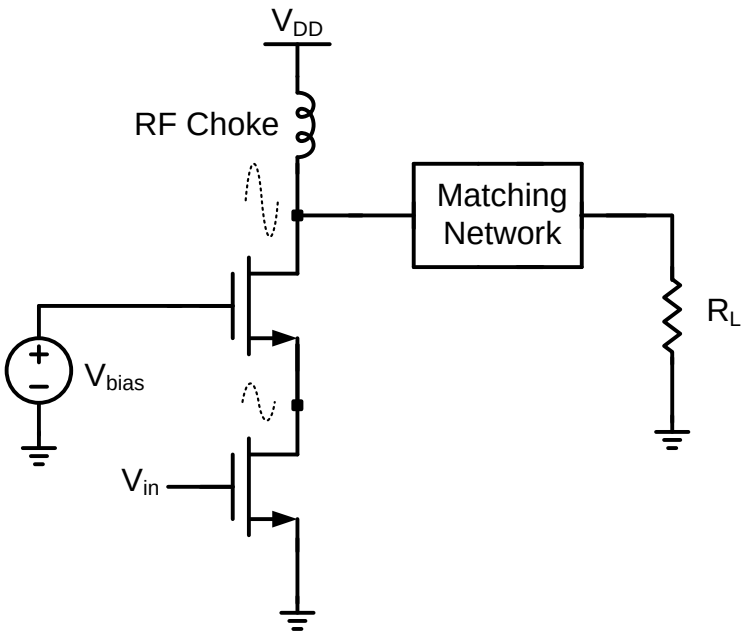


Figure 2.4: Cascode configuration.

To solve the uneven stress problem, a self-biased cascode structure, shown in Fig. 2.5, was presented in [6]. The capacitor C_b is added at the gate of the cascode device to allow an RF swing and the drain-gate feedback resistor R_b is used for biasing as well as providing an attenuated RF swing at the gate due to the low-pass nature of R_b and C_b. The reported power amplifier, fabricated in 0.18-μm CMOS, provides 23-dBm output power with a PAE of 42% at 2.4 GHz using a 2.4-V supply.

To combine more devices in series, one of the earliest proposed techniques is

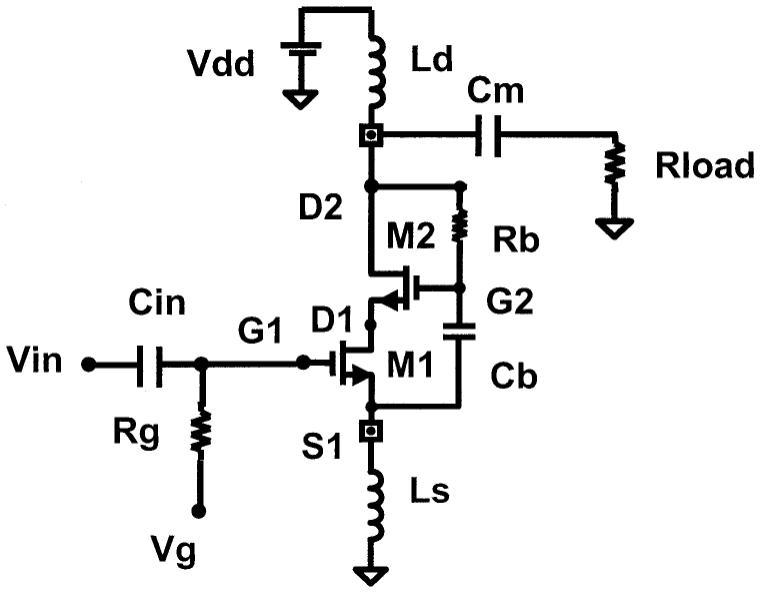


Figure 2.5: A self-biased cascode power amplifier [6].

the bean stalk amplifier proposed by K.J. Dean in 1964. Shown in Fig. 2.6, a ladder of resistors is used to bias and drive several BJT transistors connected in series such that the voltage stress is divided across all devices. This technique, however, is only suitable for low-frequency design since the input signal has to propagate up to the gates of all stacked devices so the devices are not well synchronized to add up in phase, degrading the output power, efficiency, and linearity. For high-frequency high-voltage applications, another technique was presented by Shifrin in 1992, illustrated in Fig. 2.7. A resistive ladder is also used in this structure for DC biasing and only the common-source device is driven by the input. Inductors are used for interstage matching. while capacitors are employed to allow RF swing at the gates of stacked devices. The reported power amplifier delivers an output power of 36 dBm with a 12-dB gain and a 20% efficiency at 4.5 GHz using three FETs [8].

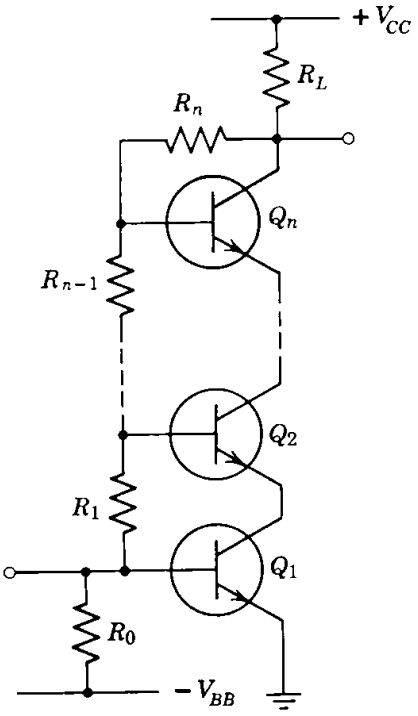


Figure 2.6: Bean stalk amplifier [7].

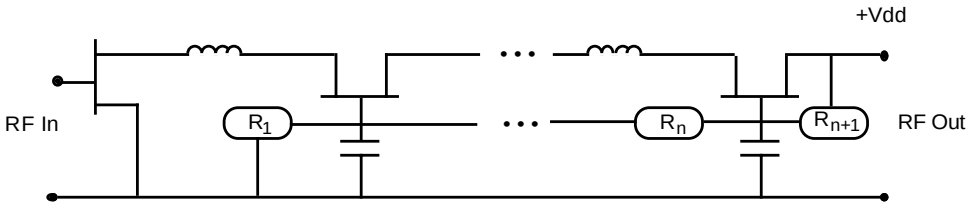


Figure 2.7: Hittite high-voltage power amplifier [8].

In recent years, there have been many more variations of device-stacking techniques investigated in the literature. In [9], a 900-MHz transformer-coupled stacked-FET PA was reported, where on-chip transformers were used in parallel to couple the input signals into series-connected FETs. A similar approach was also demonstrated in HBT with series input feed [10]. These transformer-coupled techniques, illustrated in Fig. 2.8(a) and Fig. 2.8(b), eliminate the synchronization problem found in the bean stalk amplifier, making it more suitable for RF applications, even though, the transformers consume a large die area.

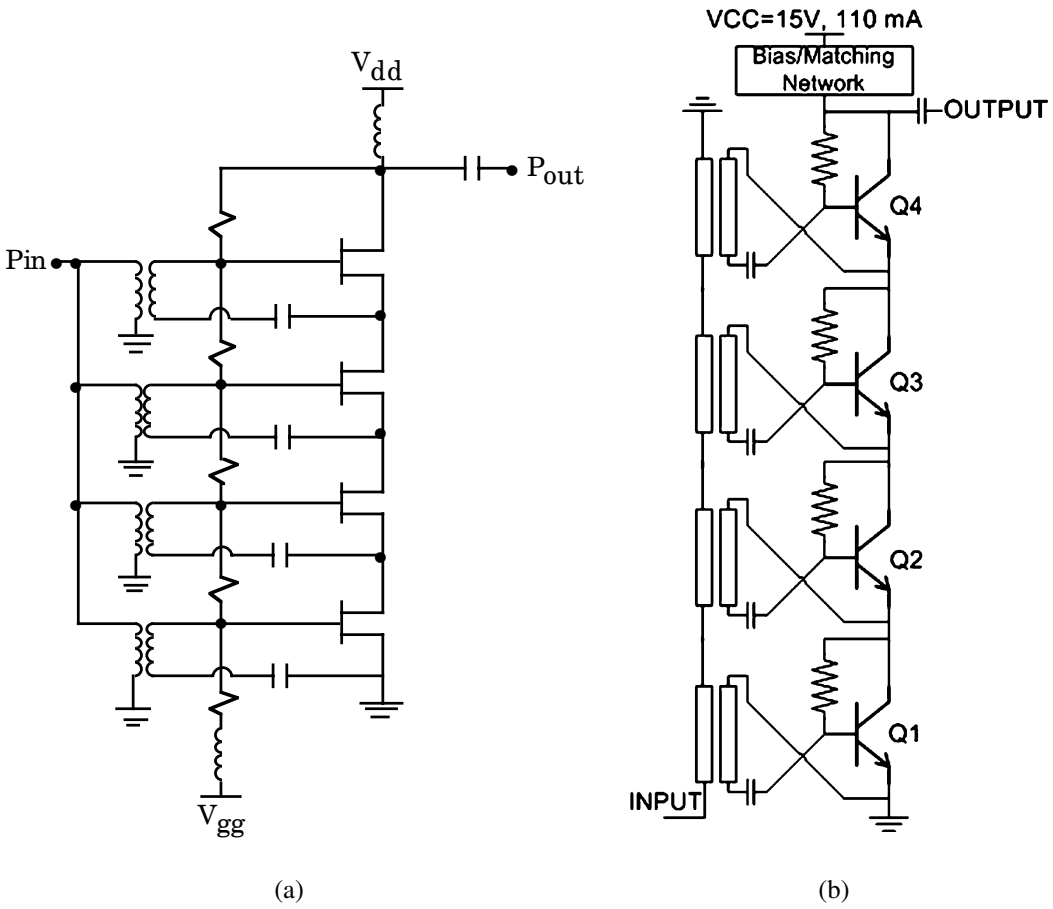


Figure 2.8: Transformer-coupled input-feed techniques: (a) Parallel-input-feed stacked FET PA [9], and (b) Series-input-feed stacked HBT PA [10].

In [11, 26, 27], high-voltage/high-power (HiVP) PAs were presented, where several transistors are connected in series to achieve high output voltage swing. The structure, illustrated in Fig. 2.9, uses feedback shunt resistors together with appropriate capacitive loading of the gate nodes to control voltage swings at the gates of the stacked devices.

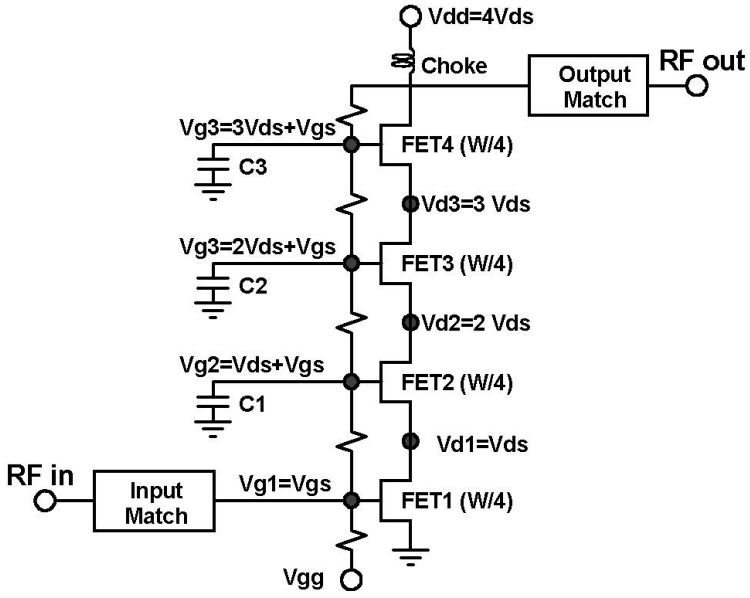


Figure 2.9: A HiVP power amplifier [11].

2.5 Proposed Stacked-FET Design Concept

2.5.1 Basic Operation

The stacked-FET structure used in this work is shown in Fig. 2.10. The circuit is composed of a common-source input transistor and three stacked transistors connected in series so that their output swings are added in phase. Unlike in a cascode configuration

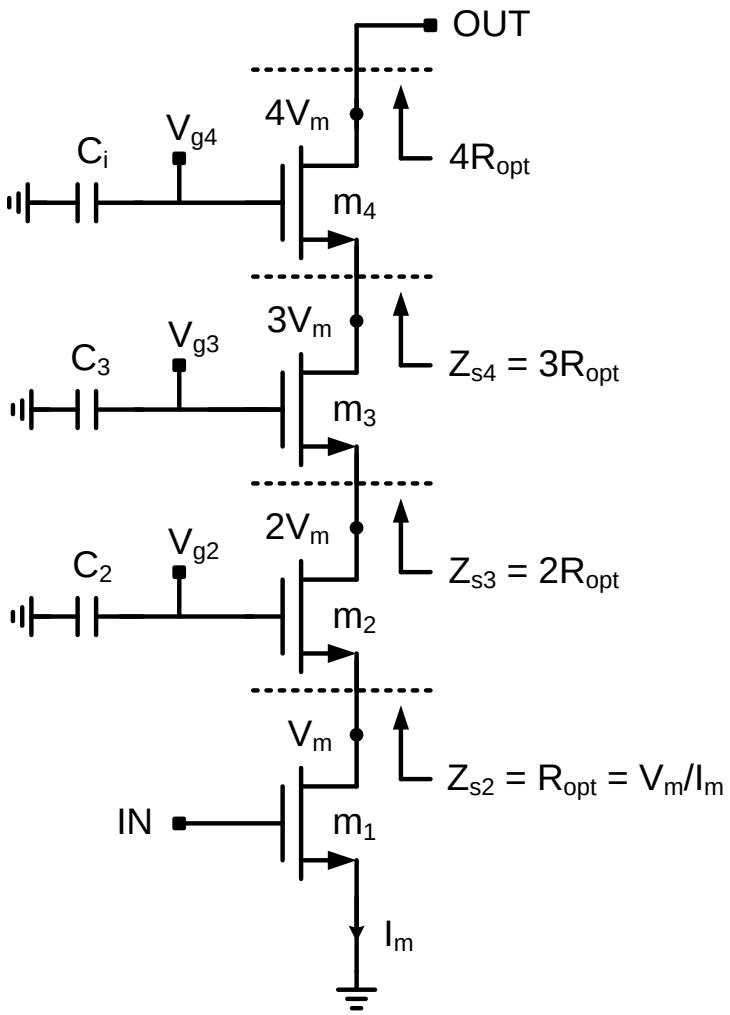


Figure 2.10: Proposed stacked-FET PA basic structure.

where the gate of the common-gate transistor is RF-grounded, a relatively small external gate capacitance (C_2, C_3, and C_4) is introduced to allow an RF swing at the gate of each stacked transistor. The external gate capacitance and the gate-to-source capacitance (C_{gs}) of each stacked transistor form a capacitive voltage divider to produce the proper in-phase voltage swing at the gate and drain. This approach systematically reduces the drain-gate and drain-source voltage swings of both the common-source and common-gate transistors under large signal operation, unlike in a cascode structure where the drain-gate voltage swing of the common-gate transistor becomes the bottleneck [6].

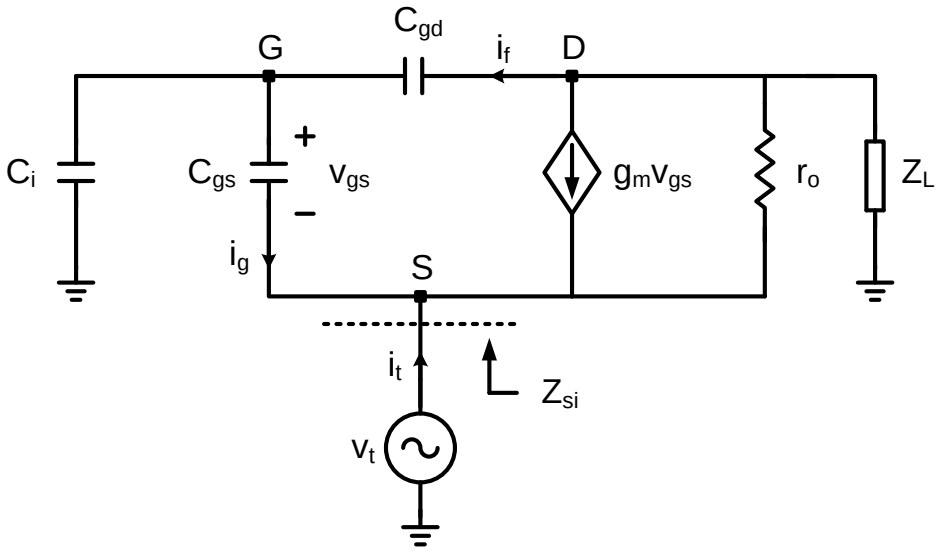


Figure 2.11: Effect of an external gate capacitance on a stacked FET's source input impedance.

A high-frequency stacked FET model is shown in Fig. 2.11, where Z_L is the impedance seen by the drain of the device. Assuming that r_o is large, a test voltage can be applied at the source and it follows from KCL and KVL that

$$v_t = \frac{(i_f - i_g)}{sC_i} - \frac{(i_g)}{sC_{gs}} \tag{2.11}$$

$$-i_t = i_g + \frac{g_m i_g}{sC_{gs}} \tag{2.12}$$

$$-i_f = \frac{g_m i_g}{sC_{gs}} + \frac{(v_{ds} + v_t)}{Z_L} \tag{2.13}$$

$$v_{ds} = \frac{i_f}{sC_{gd}} + \frac{(i_g)}{sC_{gs}} \tag{2.14}$$

$$i_t + i_g - i_f = \frac{(v_t + v_{ds})}{Z_L}. \tag{2.15}$$

From (2.11)-(2.15), the source input impedance Z_{si} of a stacked transistor can be derived as

$$Z_{si} = \frac{v_t}{i_t} = \frac{C_{gs} + C_i + C_{gd}(1 + g_m Z_L + sC_{gs}Z_L + sC_i Z_L)}{(g_m + sC_{gs})(C_{gd} + C_i + sC_{gd}C_i Z_L)}. \tag{2.16}$$

In the low RF frequency range, (2.16) can be simplified by assuming that the feedback current through C_{gd} is negligible and the equation becomes

$$\begin{aligned} Z_{si} &= (1 + \frac{C_{gs}}{C_i}) \cdot (\frac{1}{g_m} \parallel \frac{1}{sC_{gs}}) \\ &\approx (1 + \frac{C_{gs}}{C_i}) \cdot \frac{1}{g_m} \quad \text{for} \quad f_0 << F_t. \end{aligned} \tag{2.17}$$

The small-signal voltage gain of the PA can be derived as

$$\begin{aligned} A_v &= \frac{g_{m1} R_L}{(1 + \frac{sC_{gs2}}{g_{m2}}) \cdot (1 + \frac{sC_{gs3}}{g_{m3}}) \cdot (1 + \frac{sC_{gs4}}{g_{m4}})} \\ &\approx g_{m1} R_L \quad \text{for} \quad f_0 << F_t \end{aligned} \tag{2.18}$$

For a low frequency design where the carrier frequency (f_o) is much lower than the cutoff frequency of the device (F_t), the source input impedance Z_{si} of a stacked

transistor is influenced by the value of the external gate capacitor C_i relative to its gate-source capacitance C_{gs}. Z_{s2}, Z_{s3}, and Z_{s4} are approximately purely-resistive and all four devices in series share the same constant current swing (I_m). The values of external capacitors (C_2 - C_4) should be set such that Z_{s2}, Z_{s3}, and Z_{s4} are R_{opt}, $2R_{opt}$, and $3R_{opt}$, respectively, and the optimum output load impedance is $4R_{opt}$. This ensures that each transistor has the same drain-source, drain-gate, and gate-source voltage swings while the absolute voltage swings with respect to ground increase as one moves up the ladder.

As the operating frequency approaches F_t, the reactive component of Z_{s2}, Z_{s3} and Z_{s4} due to C_{gs} becomes significant. Also notice from Fig. 2.11 and (2.16) that, without assuming a low-frequency operation, Z_{si} is also influenced by Z_L and C_{gd} and Z_L is not necessary purely resistive. In addition, all transistors will see slightly different drain currents due to currents leaking out through C_{gs}. These effects result in more difficult waveform shaping to achieve high-efficiency operation on all transistors simultaneously.

2.5.2 Stacked-FET vs. Parallel

Table 2.1 compares some important parameters of PAs using parallel and stacked-FET configurations. Compared to the n-parallel-FET PA with the same output power and DC power, the n-stacked-FET PA has n times higher voltage gain and power gain. The input and output impedances are n times and n^2 times higher, respectively, resulting in improved input and output matching bandwidths and less power loss in the output matching network.

Table 2.1: Comparison of parallel and Stacked-FET configurations

Parameter	**Unit FET**	**n-Parallel FET**	**n-stacked FET**
Peak Drain Current	I_m	$n \cdot I_m$	I_m
Peak Drain Voltage	V_m	V_m	$n \cdot V_m$
Input Capacitance	C_g	$n \cdot C_g$	C_g
Output Impedance	R_{opt}	$\frac{R_{opt}}{n}$	$n \cdot R_{opt}$
Output Power	$\frac{1}{8} \cdot V_m \cdot I_m$	$\frac{1}{8} \cdot V_m \cdot nI_m$	$\frac{1}{8} \cdot nV_m \cdot I_m$
Voltage Gain	$g_m \cdot R_{opt}$	$ng_m \cdot \frac{R_{opt}}{n}$	$g_m \cdot nR_{opt}$

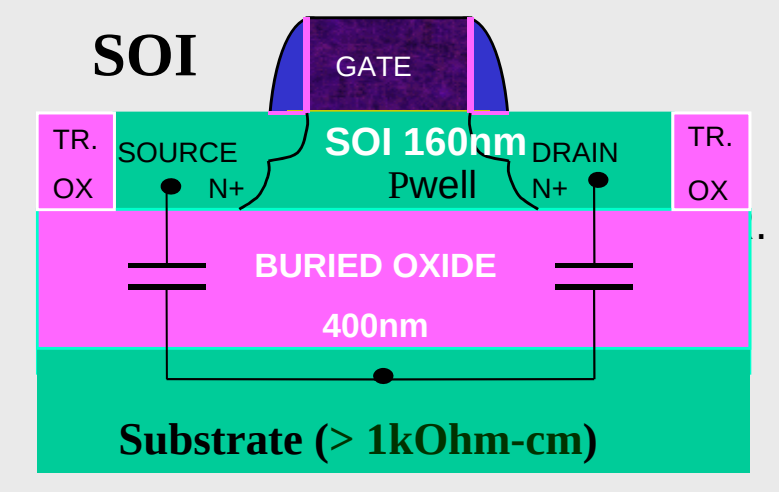


Figure 2.12: Silicon-on-insulator CMOS technology.

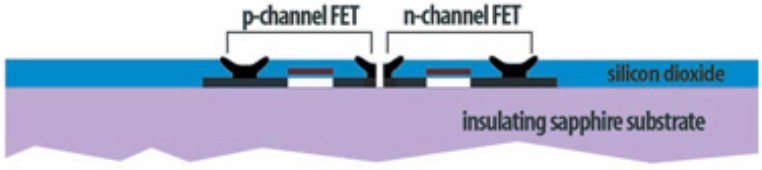


Figure 2.13: Silicon-on-sapphire CMOS technology.

2.6 Alternative CMOS Technologies

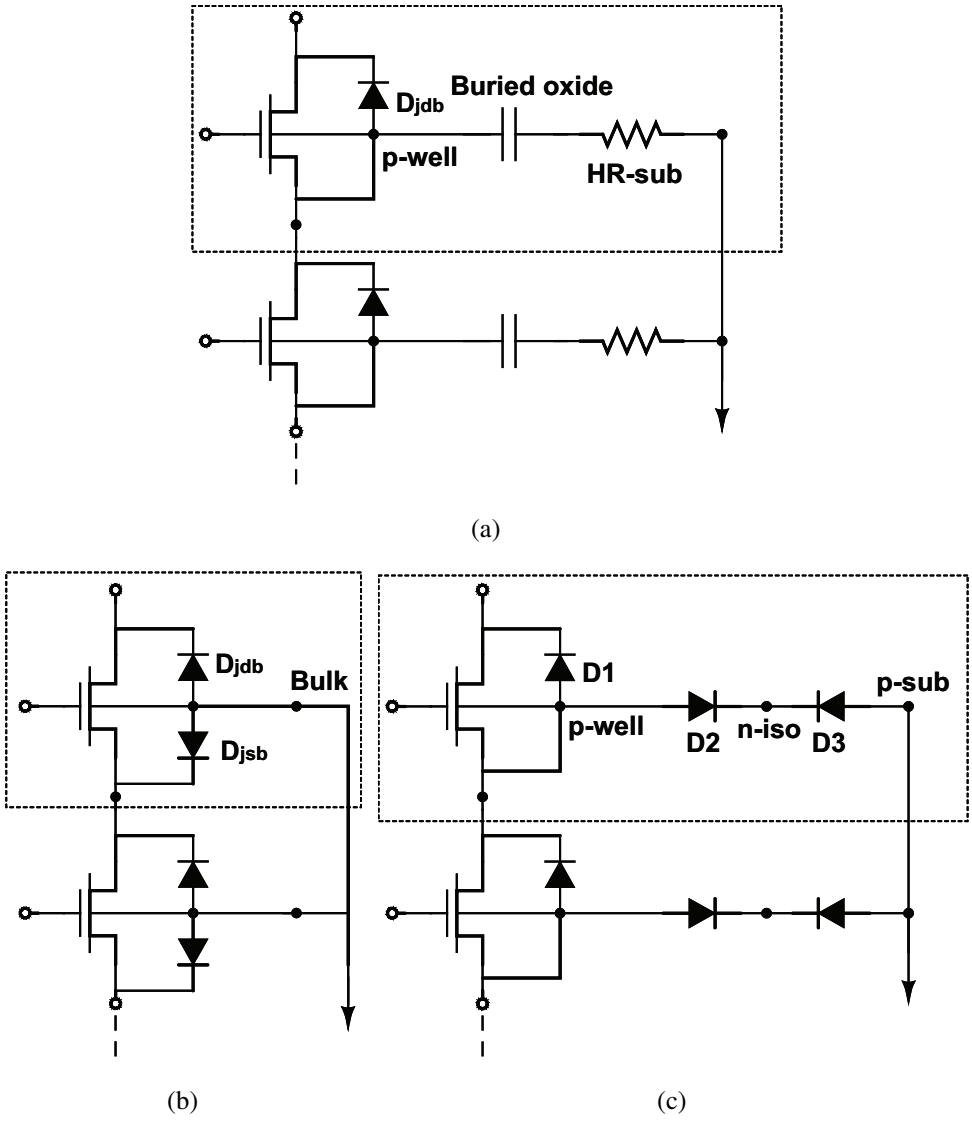


Figure 2.14: Simplified schematics of stacked NMOS transistors using different process technologies: (a) Partially-depleted SOI CMOS used in this work, (b) Bulk CMOS, and (c) Triple-well CMOS.

The partially-depleted silicon-on-insulator (SOI) and silicon-on-sapphire (SOS) CMOS technologies, shown in Fig. 2.14(a) and Fig. 2.13 respectively, used in this work are particularly attractive for the stacked-FET technique due to their lack of body effect

and relatively small parasitic junction capacitance. As shown in a simplified model in Fig. 2.14(a), body effect can be avoided by connecting the p-well of each stacked transistor to its source. By contrast, in bulk CMOS as illustrated in Fig. 2.14(b), source-body capacitance and body effect progressively reduce gain of the transistors in the upper sections of the stack. Moreover, the maximum allowable supply voltage is limited by the breakdown voltage of the drain-bulk junction diode (D_{jdb}). An alternative solution is to use a triple-well CMOS process as shown in Fig. 2.14(c), where the p-well of each transistor can be tied to its source to avoid body effect. The n-iso layer can be tied to the supply voltage to prevent the p-well/n-iso junction diode (D_2) from turning on. It should not be tied to any of the device's terminals due to large capacitance from the n-well to the substrate. The maximum allowable supply voltage is limited in this case by the breakdown voltage of the n-iso/p-sub junction diode (D_3).

2.7 Fully-Integrated Stacked-FET Linear PA Design in SOS CMOS

As a prototype [12], a fully-integrated stacked-FET linear power amplifier was designed at 1.88 GHz using the Peregrine Semiconductor 0.25-μm SOS CMOS process for which the drain-to-source breakdown voltage is 2.75 V. The triple-stacked FET structure used is shown in Fig. 2.15 together with on-chip input matching and gate bias circuit. The resistors R_1-R_4 are used only to provide gate biasing of the three FETs. The external capacitances C_2 and C_3 are determined to enable each drain and source to sustain large voltage swings in a way that each FET has the same drain-source, gate-source and drain-gate voltage swings, as described in the earlier section.

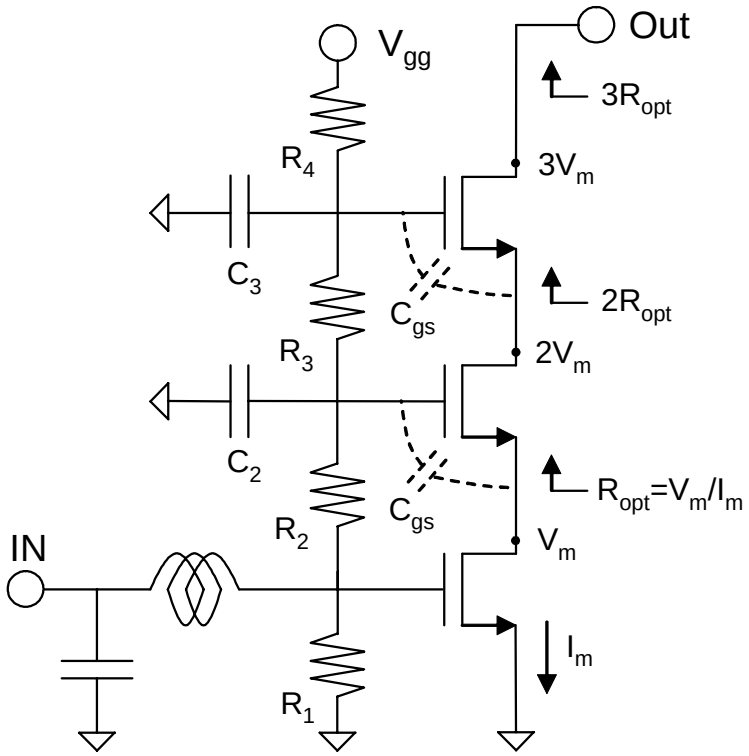


Figure 2.15: Schematic of the fully-integrated triple-stacked FET power amplifier in SOS CMOS [12].

Each FET has the 1.512-mm gate width, so the total gate width is 4.536 mm. For linear operation, the gate bias is set to 0.4 V with drain bias of 3.9 V, so each FET has a drain bias of 1.3 V. The optimum output load impedance for 20 dBm output power is as high as 50 ohm (3Ropt in Fig. 2.15), as a result of the triple stacked FET structure. Therefore, there is no need for output matching circuit. The load impedance would be 5.6 Ω for 20 dBm output power in a parallel FET configuration (9x lower), which requires careful output matching circuit design and causes efficiency reduction due to the high impedance transformation ratio. The input matching is implemented with a high-Q on-chip inductor and capacitor as shown in Fig. 2.15. Fig. 2.16 illustrates the simulated load lines for each FET where the three transistors show the same drain-source and gate-source voltage swing as expected, which is essential for stacked FET power amplifier design, and means that each FET delivers its maximum available power.

A photograph of the fabricated power amplifier is shown in Fig. 2.17. The chip size is 0.6 mm 0.9 mm. The small signal S parameters were measured by on-wafer probing. The bias current was 52 mA which was slightly lower than the design value. The gain is 17.1 dB at 1.88 GHz as shown in Fig. 2.18. The input return loss is better than 15.0 dB between 1.78 GHz and 2.06 GHz.

For the power measurement, the chip was mounted on a coplanar waveguide PCB using Duroid substrate with dielectric constant of 3.38. More than 10 gold wires were bonded to the chip, to minimize inductance between chip ground and the package ground. Off-chip capacitors of 51 pF were placed at input and output to provide a DC block. The drain bias circuit consisted of a quarter-wavelength line with a 33-pF shunt

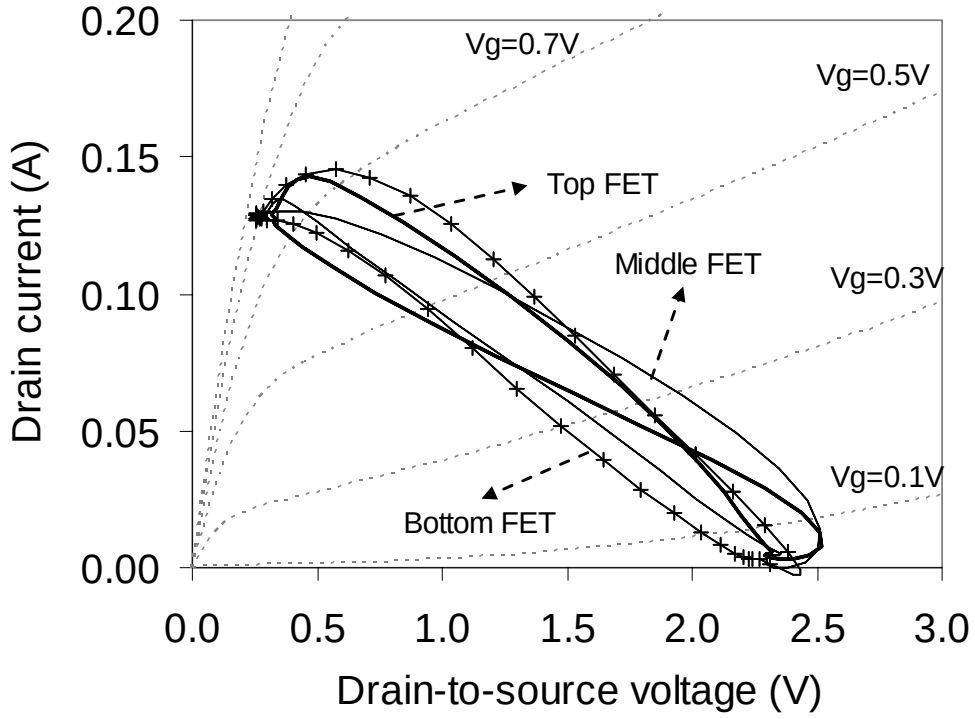


Figure 2.16: Simulated load lines of each FET at the output power of 20 dBm [12].

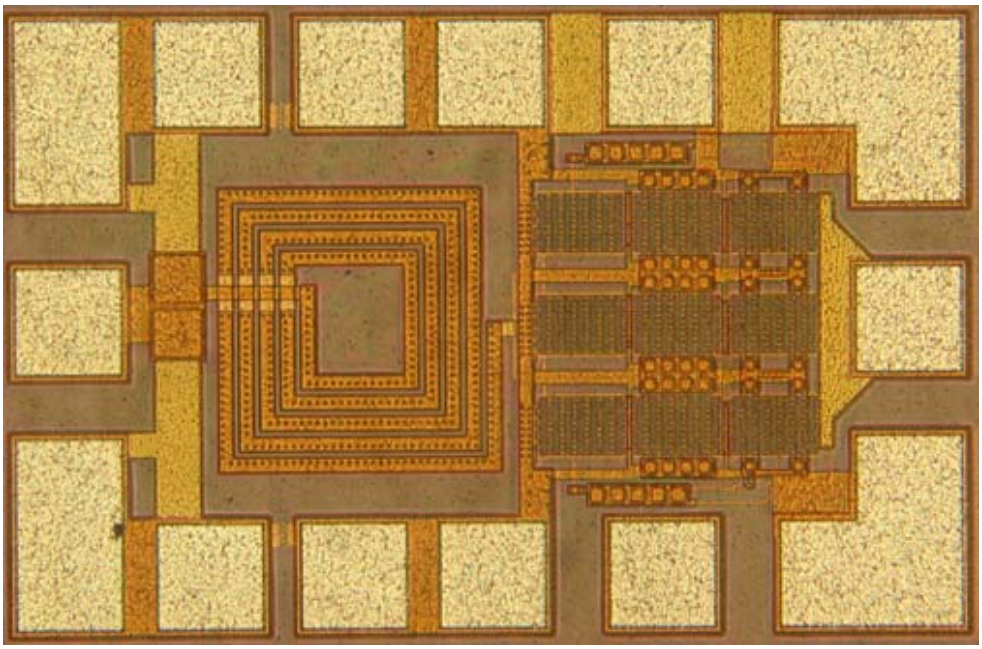


Figure 2.17: Chip photograph of the fabricated SOS power amplifier [12].

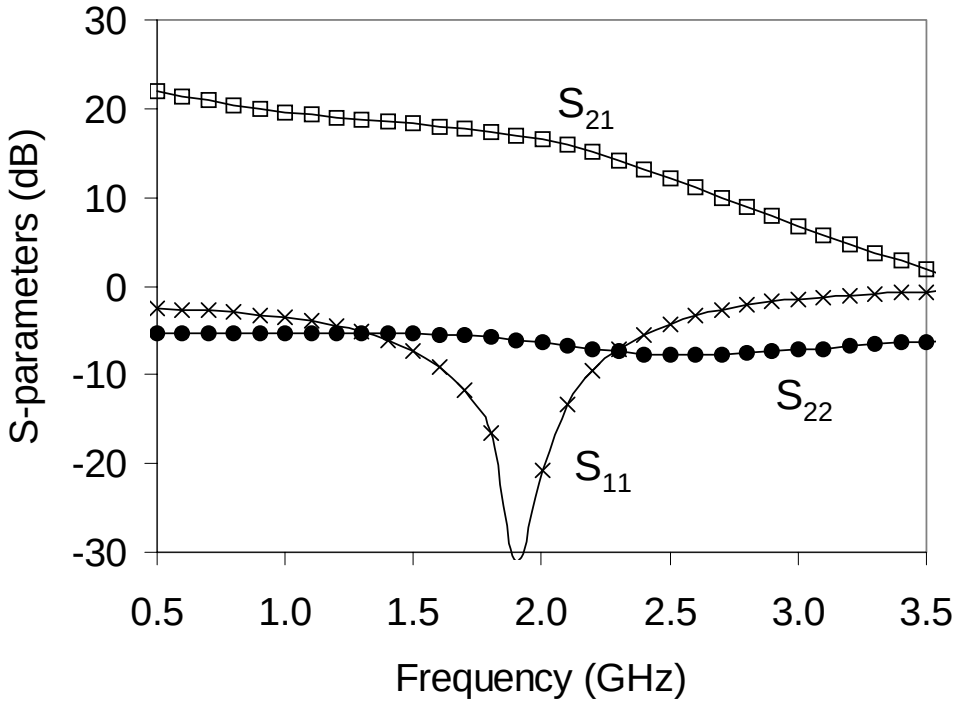


Figure 2.18: Measured S-parameters by on-wafer probing [12].

capacitor providing 2^{nd} harmonic short circuit.

The measured large signal gain and PAE are shown in Fig. 2.19 with corresponding DC current as a function of output power at 1.88 GHz. The amplifier delivers 18.3 dBm output power at 1-dB gain compression point with PAE of 29.2%. The saturated power is 21.0 dBm with the maximum PAE of 44.0%. This high efficiency is attributed to the high load impedance and the reduced knee voltage effect of the stacked FET topology. Using an IS-95 CDMA signal, ACPRs were measured at 885-KHz offset from the center frequency of 1.88 GHz and are shown in Fig. 2.20 together with average PAE as a function of average output power. The difference between upper and lower side ACPRs is within 0.6 dB, indicating low memory effect. The measured ACPR is below -42 dBc (the specification for IS-95 CDMA operation) up to an average output power

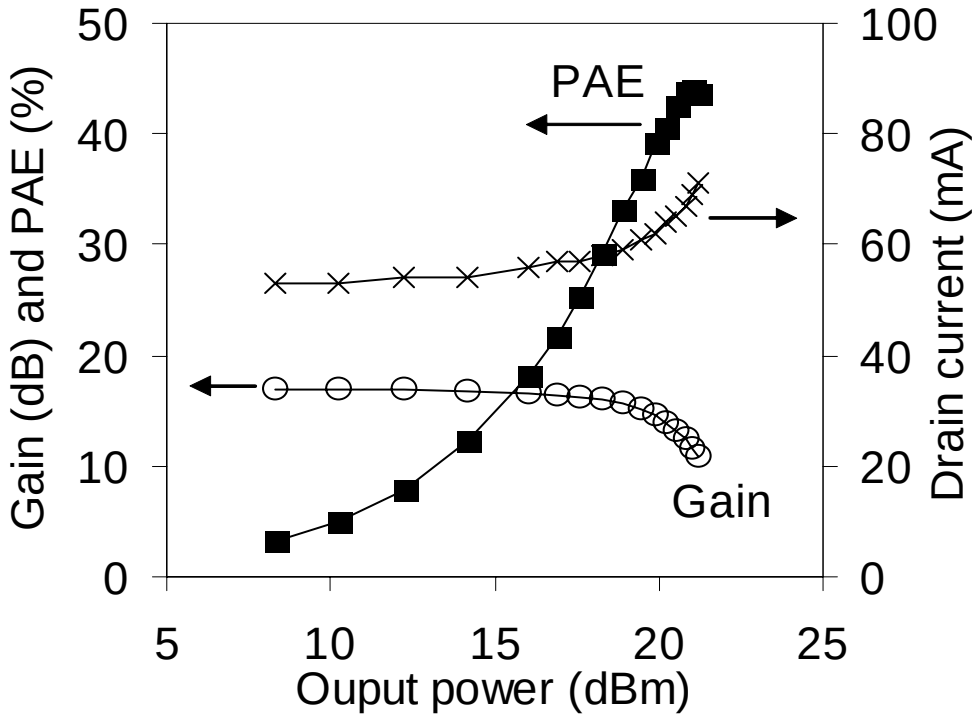


Figure 2.19: Measured gain, PAE and DC drain current as a function of output power with single tone input at 1.88 GHz [12].

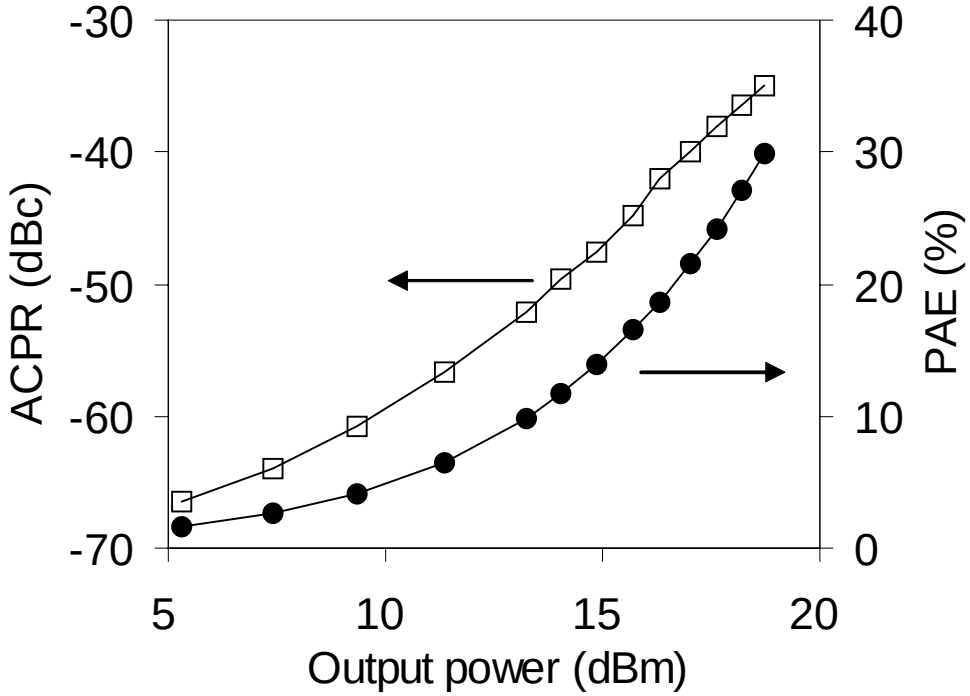


Figure 2.20: Measured ACPR and PAE performance as a function of average output power with IS-95 CDMA input signal [12].

of 16.3 dBm and PAE of 18.7%. These characteristics of linearity and efficiency are in excellent agreement with what would be expected for a class-A amplifier operating with a signal with 4.5-dB PAPR as appropriate for IS-95 CDMA.

2.8 Watt-Level Stacked-FET Linear PA Design in SOI CMOS

To further investigate the application of stacked-FET technology for handset applications, a design effort was undertaken to show higher output power and higher efficiency (at the possible cost of linearity). A single-stage stacked-FET deep class-AB PA was designed to operate primarily at 1.9 GHz using 0.28-μm 2.5-V standard I/O FETs

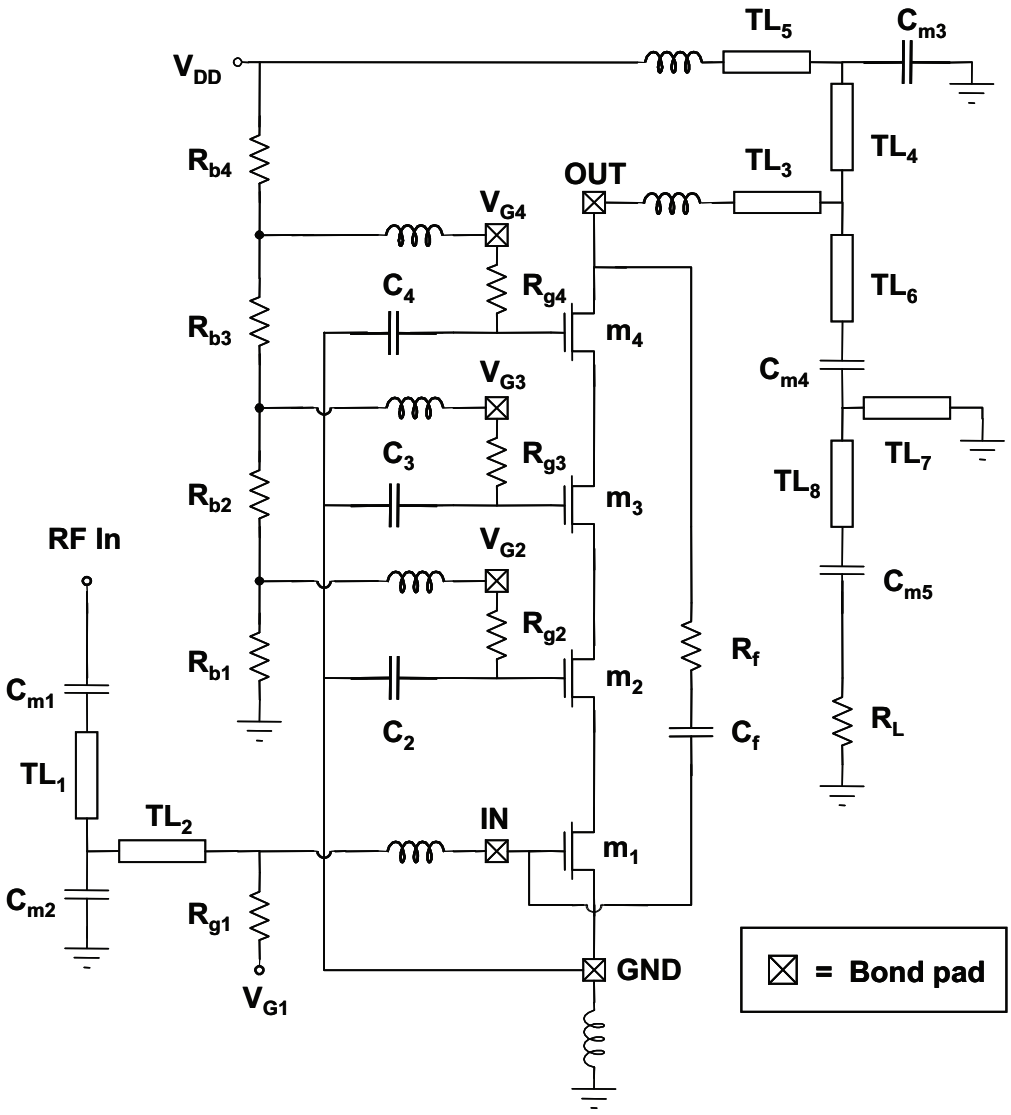


Figure 2.21: Circuit schematic of the single-stage stacked-FET PA.

available in the STMicroelectronics 0.13-μm SOI CMOS process. The overall circuit diagram is shown in Fig. 2.21. Four transistors are stacked in series, based on the topology presented in the previous section. Each transistor has the total gate width of 5 mm, so the total device gate width in the amplifier is 20 mm. To avoid the device breakdown, the drain-to-source voltage of each transistor should be limited to 4.5 V ($V_{ds-breakdown}$ = 5 V), allowing a maximum voltage swing of 18 V at the top drain node with a 9-V drain bias. For a higher margin of safety, the PA was designed to achieve linear amplification up to the required output power under a 6.5-V supply.

The external gate capacitances (C_2 - C_4) are 9 pF, 2.6 pF, and 2 pF, respectively, setting the optimum load impedances seen by each transistor. For flexibility, the gate bias voltages of each stacked device are implemented by an off-chip resistive voltage divider and applied through 1-kΩ on-chip resistors. The R_f-C_f feedback circuit is introduced to improve stability. The simulated Rollett stability factor K is greater than 1 for all frequencies between DC and 50 GHz except for the frequency band from 6.4 GHz to 7.6 GHz, where stability is ensured in the simulation ($|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$) for the designed input and output matching conditions [28].

The optimum output load impedance ($4R_{opt}$ in Fig. 2.10) is 11.5 Ω, which lies in a convenient range to match to 50 Ω over broad bandwidth with high efficiency. The input impedance is 17.5 Ω, a comparatively large value corresponding to that of a single 5-mm transistor. The input and output matching circuits are implemented off-chip in this work to allow opportunities for varying the tuning. A high-pass L-match section, consisted of a series capacitor (C_{m4}) and a short stub (TL_7), was used to transform the external 50-Ω load to the optimum load. The on-board drain bias circuit included a quarter-wavelength microstrip line (TL_4) with a 39-pF shunt capacitor (C_{m3}) to ground,

providing a short circuit at successive even harmonics.

To achieve the highest drain efficiency when the PA is driven into saturation, the drain current can be shaped like a half-sine wave and the drain-source voltage can be shaped like a square wave such that the voltage and the current waveforms do not overlap, minimizing power dissipation in the device. This waveform-shaping scheme can be accomplished ideally by properly terminating odd harmonics with an open circuit and terminating even harmonics with a short circuit. It has also been demonstrated in the literature that properly terminating only the first few harmonics is sufficient to achieve high drain efficiency [29–31]. However, the efficiency improvement is limited in practice by the topmost transistor's drain-source capacitance (C_{ds}) and the bond-wire inductance, which need to be absorbed properly, as well as the fact that each stacked transistor is presented with a different load impedance. Moreover, without proper harmonic terminations at the gate, the input signal is not purely sinusoidal due to the nonlinear C_{gs} [29].

2.8.1 Gate-Bias Setting

Special consideration is needed when setting the gate bias voltages of the stacked devices (V_{G2} - V_{G4}) for a high-voltage design. The DC drain current is determined by the bottom device (m_1) and increases with the RF power level due to the class-AB bias setting. Since the gate bias voltages are fixed by the resistive voltage divider, the source bias voltages of the stacked devices must decrease to accommodate higher DC current, resulting in an early breakdown in the topmost device and an early compression in the bottom device as illustrated in Fig. 2.22(a). A simple solution is to offset the gate bias voltages of the stacked devices properly so that all four devices have equal voltage

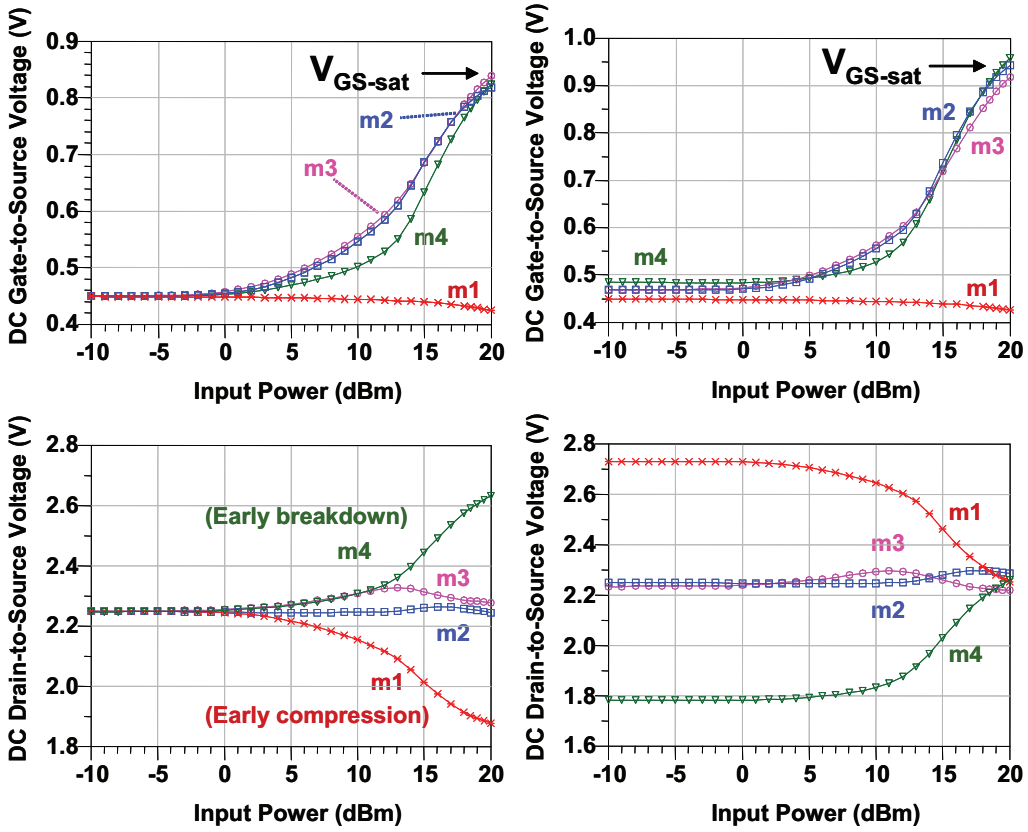
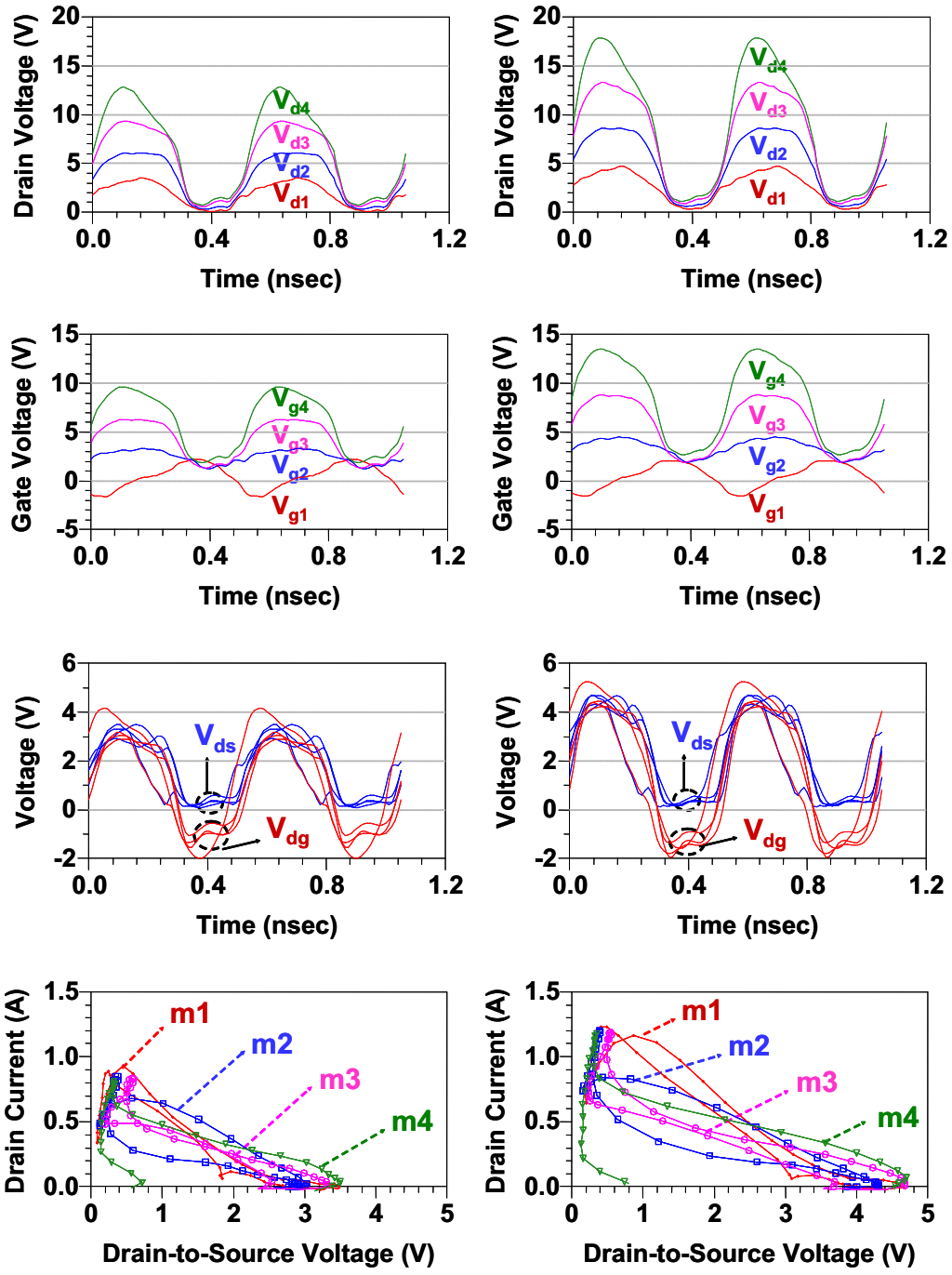


Figure 2.22: Simulated DC gate-to-source voltage and DC drain-to-source voltage of each FET as a function of input power: (a) without gate-bias offsets, and (b) with proper gate-bias offsets.



(a) (b)

Figure 2.23: Simulated drain, gate, drain-to-source, drain-to-gate voltage waveforms and dynamic load lines of each FET at the saturated output power: (a) V_{DD} = 6.5 V, and (b) V_{DD} = 9 V.

headroom close to the saturation point as shown in Fig. 2.22(b), thereby improving operation. For an n-stacked PA, the gate bias voltage of the i-th stacked device should be set as:

$$V_{Gi} = (\frac{i-1}{n})V_{DD} + V_{GSi-sat} \qquad i = 2, 3, ..., n \tag{2.19}$$

where $V_{GSi-sat}$ is the DC gate-to-source voltage of the i-th stacked device at the saturating power. Fig. 2.23(a) and Fig. 2.23(b) show the simulated drain, gate, drain-to-source, drain-to-gate voltage waveforms and dynamic load lines of each FET at the saturating output power under 6.5-V and 9-V supply voltages, respectively, illustrating that V_{gs} and V_{ds} swings for the different devices are close to one another and within the breakdown limit.

Note that the gate bias voltage of the bottom device is not a part of the resistive voltage divider and can be adjusted separately to improve gain flatness for better linearity. A deep class-AB PA can exhibit good linearity over a wide dynamic range with a "sweet-spot" gate bias voltage [31], where gain compression of AM-AM conversion due to decreasing conduction angle is properly compensated by gain expansion due to increasing drain bias current.

2.8.2 Fully-Integrated Design Possibility

One of the main advantages in using the stack-FET technique is the much lower impedance transformation ratio relative to the conventional approach, which makes a low-loss on-chip matching network possible. As an example, if the output matching is done on-chip with an on-chip inductor (Q_{ind} = 12), the drain efficiency factor due to matching network loss can be estimated as:

$$Q_m = \sqrt{\frac{R_p}{R_s} - 1} = \sqrt{\frac{50}{11.5} - 1} = 1.83 \tag{2.20}$$

$$\eta_m = \frac{Q_{ind}}{Q_{ind} + Q_m} \approx 86.8\% \tag{2.21}$$

The on-chip output matching network for a conventional common-source design delivering the same output power level without device stacking (Q_m = 8.28) would yield a drain efficiency factor of only 59.2%. The stacked-FET configuration is clearly an attractive technique for realizing a fully-integrated PA in the absence of low-loss passive components.

2.8.3 Layout Approach

The partial layout diagram of unit cells and interconnects is depicted in Fig. 2.24. One metal layer is dedicated as a ground plane to minimize on-chip ground inductance. A unit cell is composed of four gate fingers with a shared silicon active area, thus effectively producing four stacked FETs. Each finger has its body directly tied to its source. In this way, the body terminals float in phase with the respective sources, thus avoiding the drain-bulk breakdown as well. The drain of the top finger is then connected to one of the large drain lines, which flow from the input side to the output side of the chip in parallel with the gate distribution lines. On the other hand, the source of the bottom finger is connected directly to the ground plane through multiple vias. This distributed layout approach results in a highly compact layout with improved on-chip heat distribution and minimized parasitic components within the structure.

A microphotograph of the fabricated PA is shown in Fig. 2.25, occupying an area

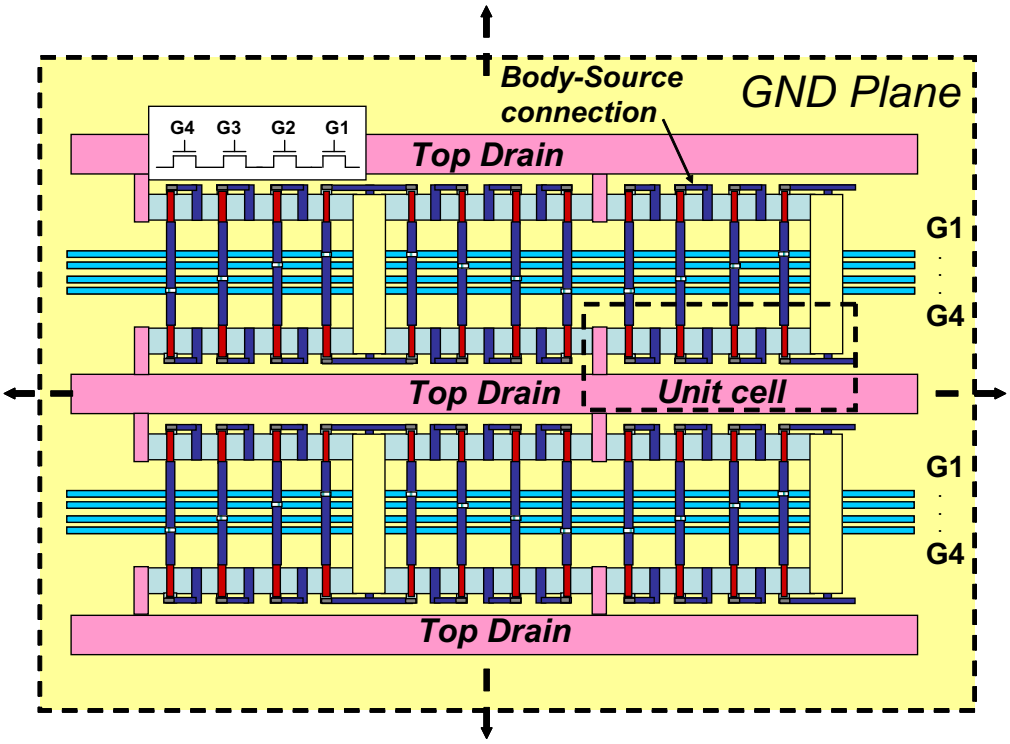


Figure 2.24: Layout diagram of stacked-FET unit cells and interconnects.

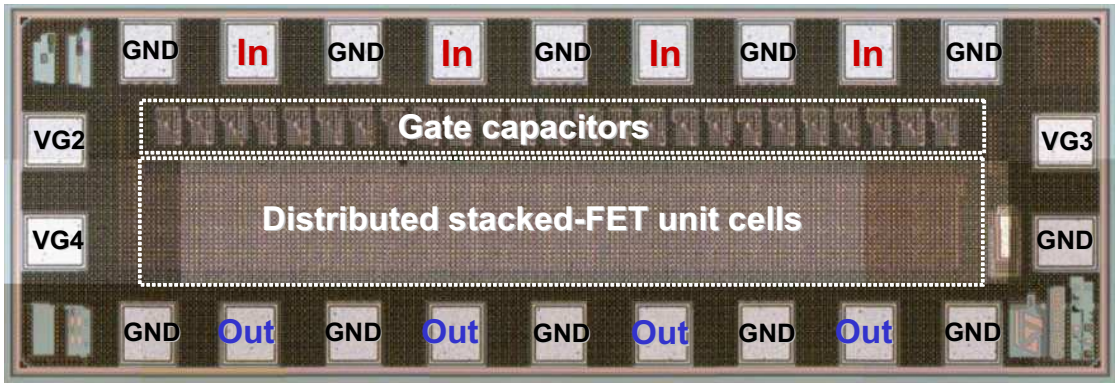


Figure 2.25: Microphotograph of the fabricated stacked-FET PA.

of 0.43 mm x 1.56 mm, including bond pads. The chip is made narrow to minimize drain line inductance and resistance, as well as to minimize the phase difference between the unit amplifier cells closer to the input side and the ones closer to the output side.

For thermal resistance estimation, it can be assumed for simplicity that the power amplifier is a single stripe heat source since device fingers are distributed evenly within an area of 0.172 mm x 1.175 mm and that heat spreads at 45^o into the substrate. The silicon substrate thickness is 350 μm while the buried oxide thickness is 0.4 μm, equivalent to approximately 40 μm of silicon substrate in term of thermal resistance. The overall thermal resistance can be calculated as

$$R_{th} = \frac{1}{2\kappa_{th}} \cdot \frac{1}{L-W} \cdot ln(\frac{W+2h}{L+2h} \cdot \frac{L}{W}) \tag{2.22}$$

where W and L are the width and length of the stripe heat source, h is the substrate thickness, and κ_{th} is the thermal conductivity of the substrate. For a power amplifier delivering 1-W output power with a 50% drain efficiency, the temperature rise relative to the ambient temperature is approximately 4^o.

2.9 Measurement Results

For improved heat flow and reduced bond-wire inductance, the test chip was thinned down to approximately 150 μm of substrate thickness. It was then mounted on a coplanar waveguide PCB with substrate relative dielectric constant of 3.38. Eleven bond pads were used for wire-bonding to the PCB ground. The PCB board was then attached on top of an aluminum block for heat sink as shown in Fig. 2.26. All measurements are

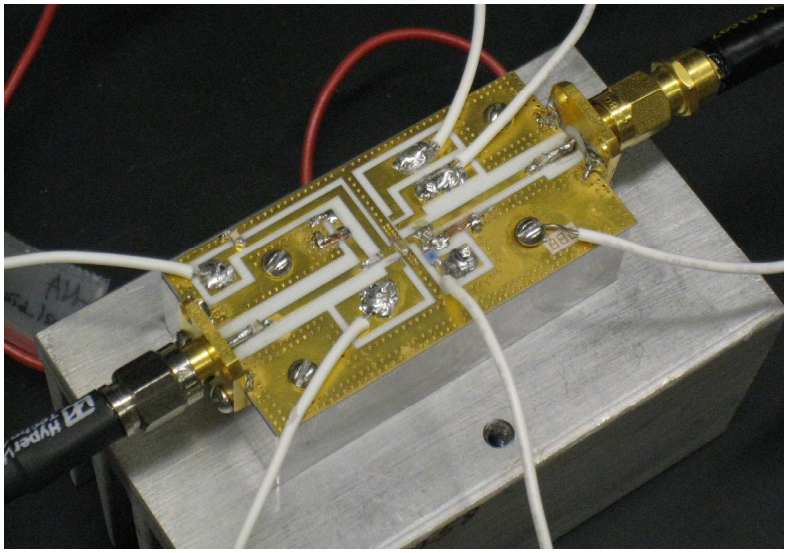


Figure 2.26: A stacked-FET PA test board.

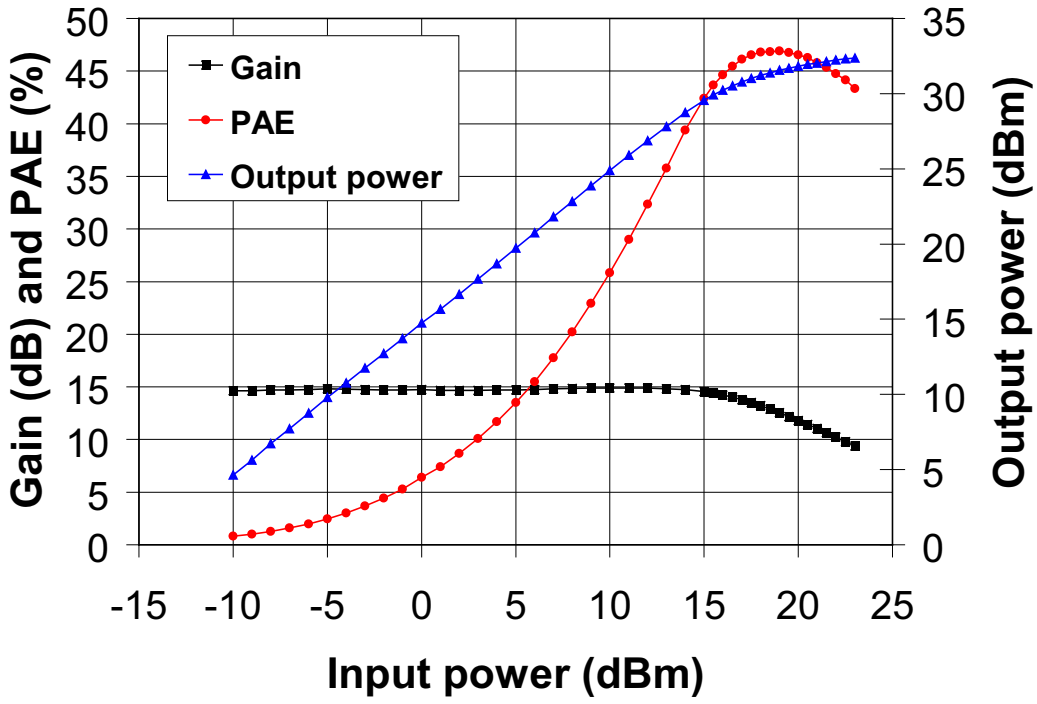


Figure 2.27: Measured gain, PAE, and output power as a function of input power with a CW input at 1.9 GHz.

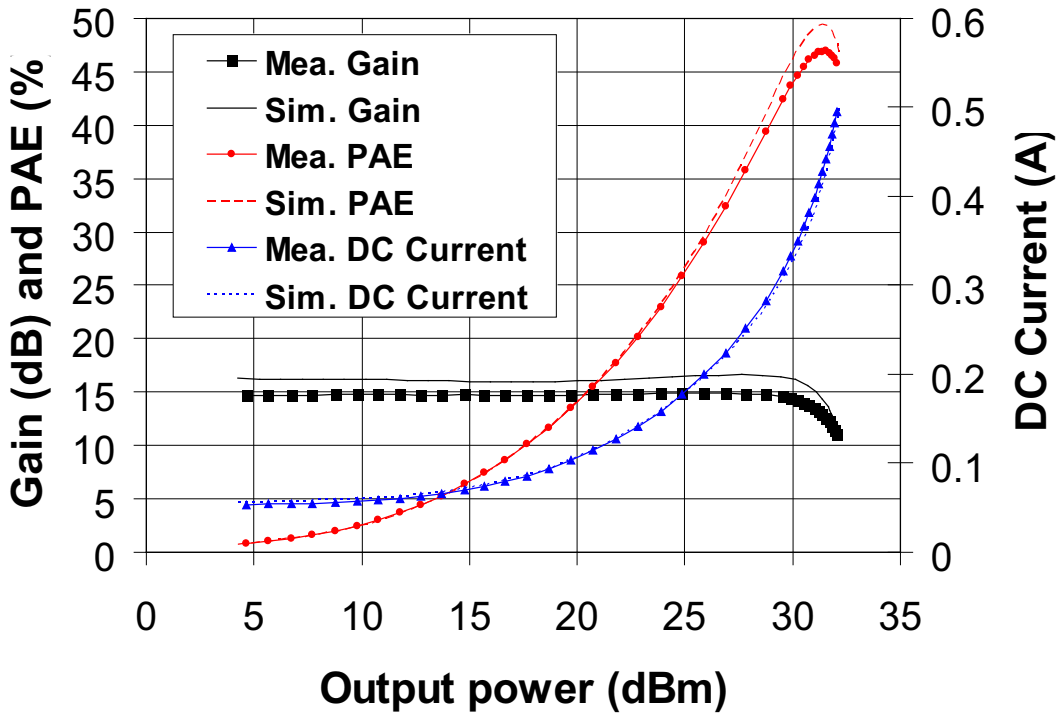


Figure 2.28: Measured and simulated gain, PAE, and DC current as a function of output power with a CW input at 1.9 GHz.

referred to the PCB connectors.

2.9.1 CW Measurements

The PA was tested under a CW input at 1.9 GHz and a supply voltage of 6.5 V. The input bias voltage was 0.42 V, resulting in a bias quiescent current of 54 mA, chosen for the best AM-AM characteristic. The measurement results are illustrated in Fig. 2.27 and Fig. 2.28 in line with the simulated results. The measured small-signal gain is 14.6 dB, with a fairly flat gain roll-off. At the 1-dB compression point, the output power is 30.8 dBm with a 46.1% PAE. A maximum PAE as high as 47% is achieved at a 31.6-dBm output power, whereas the saturated output power reaches 32.4 dBm. High power efficiency (PAE $>$ 40%) is also maintained over a wide range of supply voltages (4.5 V - 9 V) with constant load impedance as shown in Fig. 2.29. To test its robustness under a high supply voltage as designed, the PA was continuously operated at the peak output power, under a 9-V supply. No performance degradation was observed after 1 week.

Fig. 2.30 shows that, with a fixed matching circuitry, the saturated output power is maintained above 31 dBm and the drain efficiency is above 40% for the entire DCS, PCS, and UMTS frequency bands. In addition, the PA was tested in the low frequency band at 900 MHz with a reconfigured matching circuitry. As illustrated in Fig. 2.31, a small-signal gain of 19.3 dB is achieved with a saturated output power of 29.5 dBm and a maximum PAE of 53%.

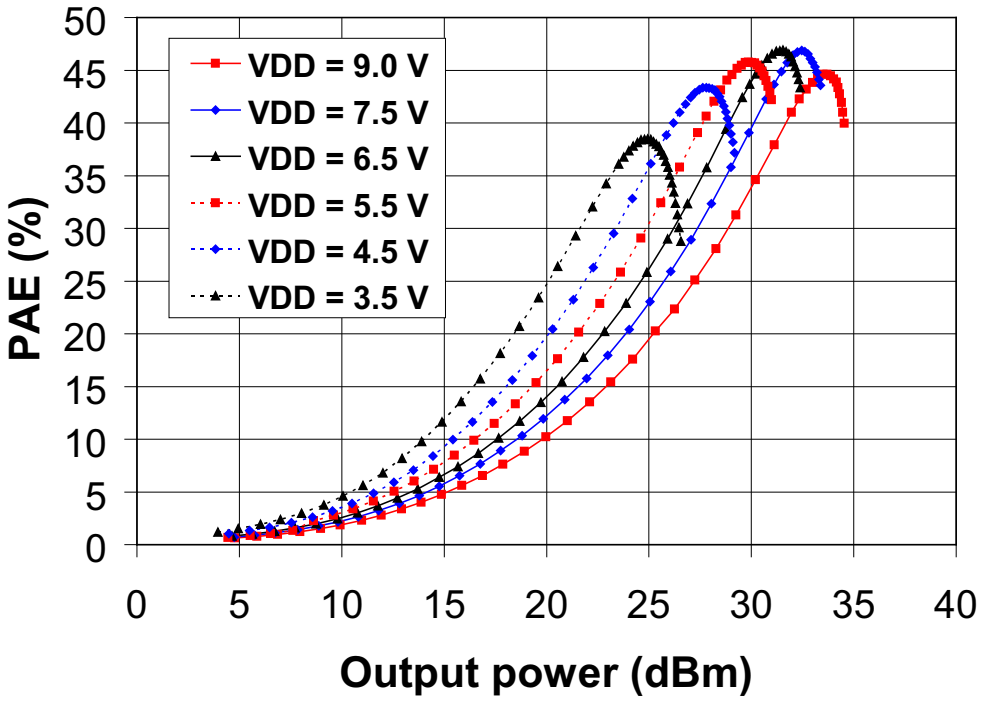


Figure 2.29: Measured PAE as a function of output power with supply voltage variation at 1.9 GHz.

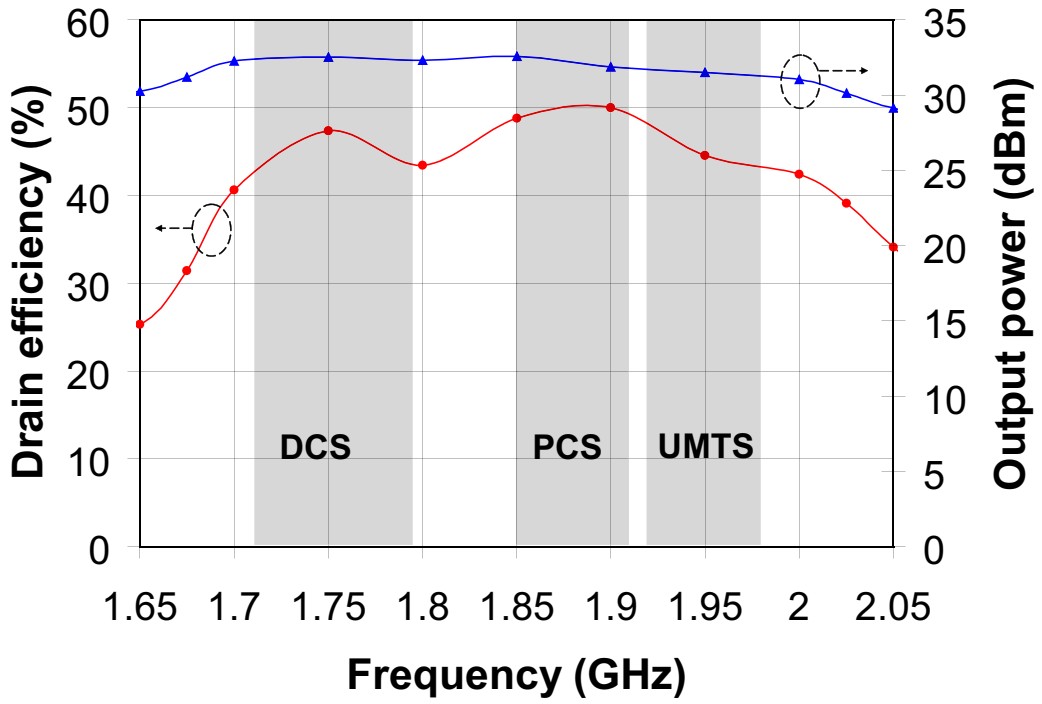


Figure 2.30: Measured drain efficiency and output power at saturation as a function of frequency.

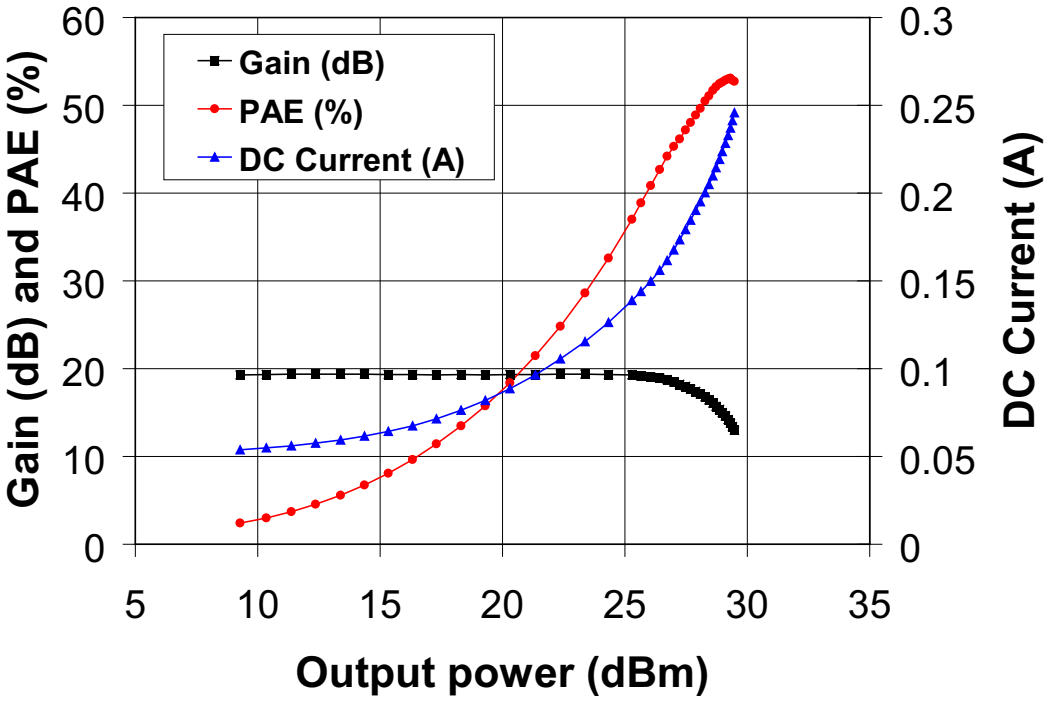


Figure 2.31: Measured gain, PAE, and DC current as a function of output power with a CW input at 900 MHz.

2.9.2 IS-95 Measurements

The power amplifier was tested for performance with CDMA and WCDMA signals as appropriate for handset applications. Fig. 2.32 shows the measured adjacent channel power ratio (ACPR), alternate channel power ratio (ACPR2) and PAE performance of the PA as a function of average output power using a reverse-link IS-95 CDMA signal at 1.9 GHz. The ACPR and ACPR2 were measured at 885-KHz and 1.98-MHz offsets, respectively, from the center frequency. The modulated input signal has a chip rate of 1.2288 Mc/s and a peak-average power ratio (PAPR) of 4.5 dB. The measured ACPR is below the -42-dBc requirement up to an average output power of 28.7 dBm and a PAE of 41.2%. The measured output spectra at P_{out} = 28.7 dBm is shown in Fig. 2.33 where the PAPR is reduced to 3 dB and the ACPR2 is below -58 dBc, meeting the -54-dBc requirement. These results are competitive with current handset power amplifiers available commercially based on GaAs HBT technology.

2.9.3 WCDMA Measurements

Fig. 2.34 shows the measured adjacent channel leakage ratios (ACLRs) and PAE performance of the PA as a function of average output power using an uplink WCDMA signal at 1.9 GHz. The ACLRs were measured at 5-MHz and 10-MHz offsets from the center frequency. The modulated input signal has a chip rate of 3.84 Mc/s and a PAPR of 2.58 dB. The measured ACLR at 5-MHz offset is below the -33-dBc requirement up to an average output power of 29.4 dBm and a PAE of 41.4%. The measured output spectra at P_{out} = 29.4 dBm is shown in Fig. 2.35 where the PAPR is reduced to 2.08 dB

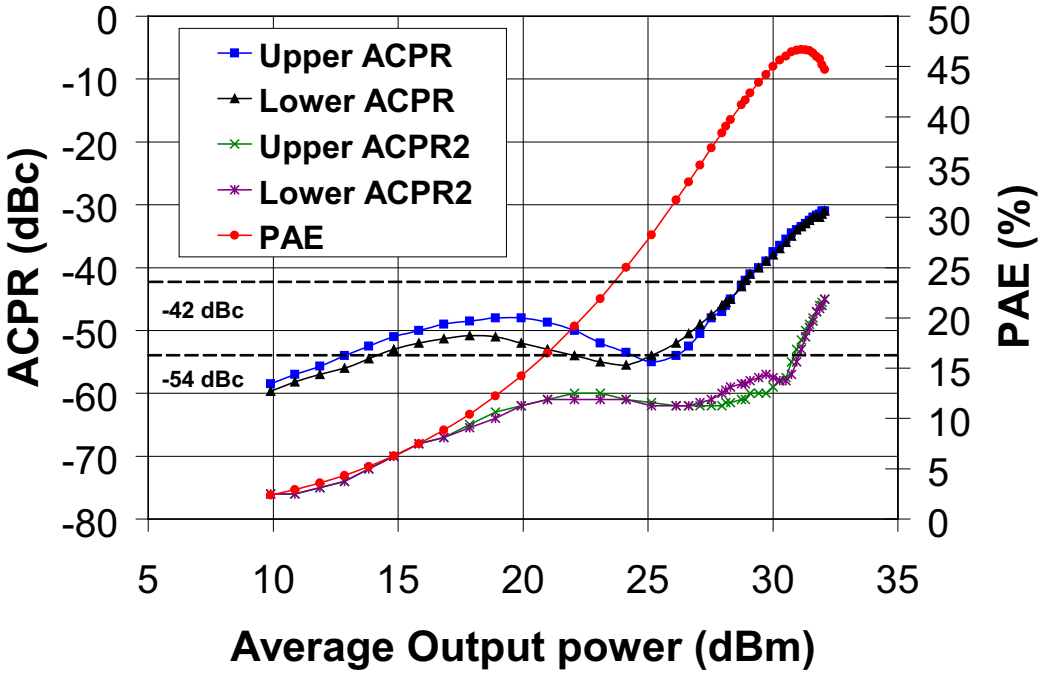


Figure 2.32: Measured ACPR and PAE performance as a function of average output power using a reverse-link IS-95 CDMA input signal at 1.9 GHz.

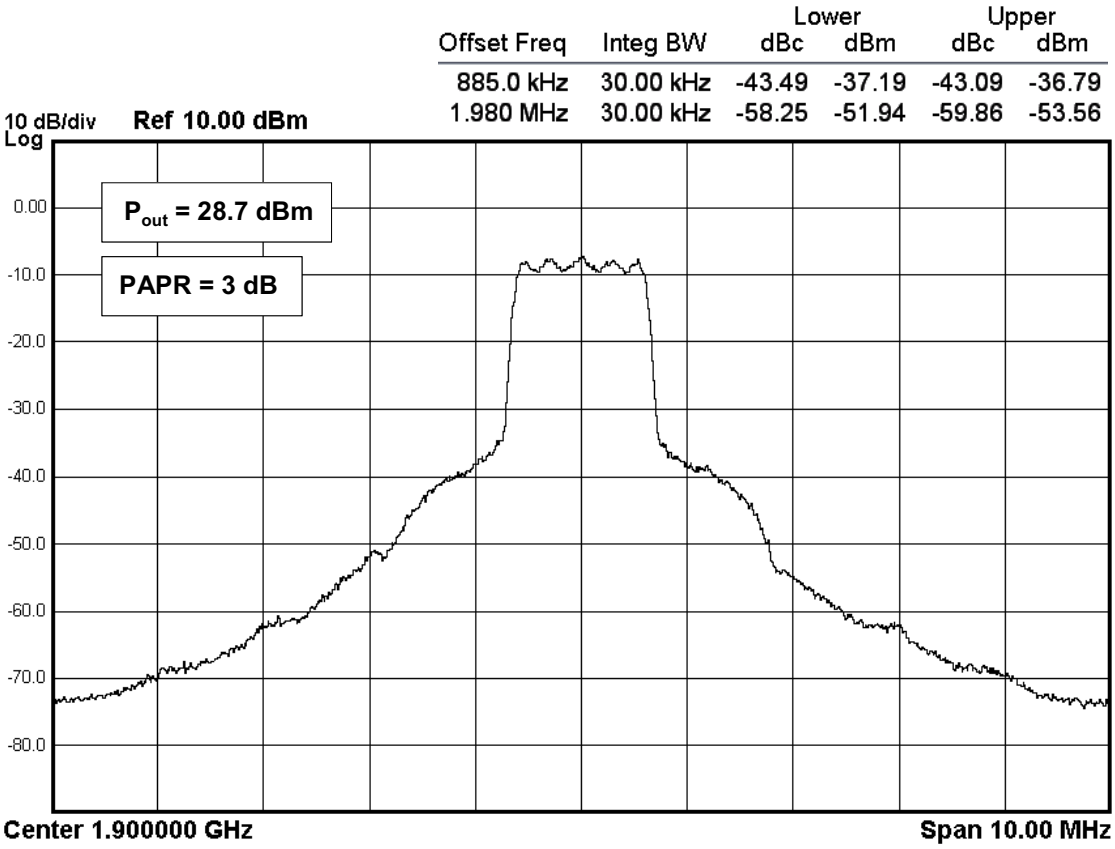


Figure 2.33: Measured IS-95 CDMA output spectra at P_{out} = 28.7 dBm.

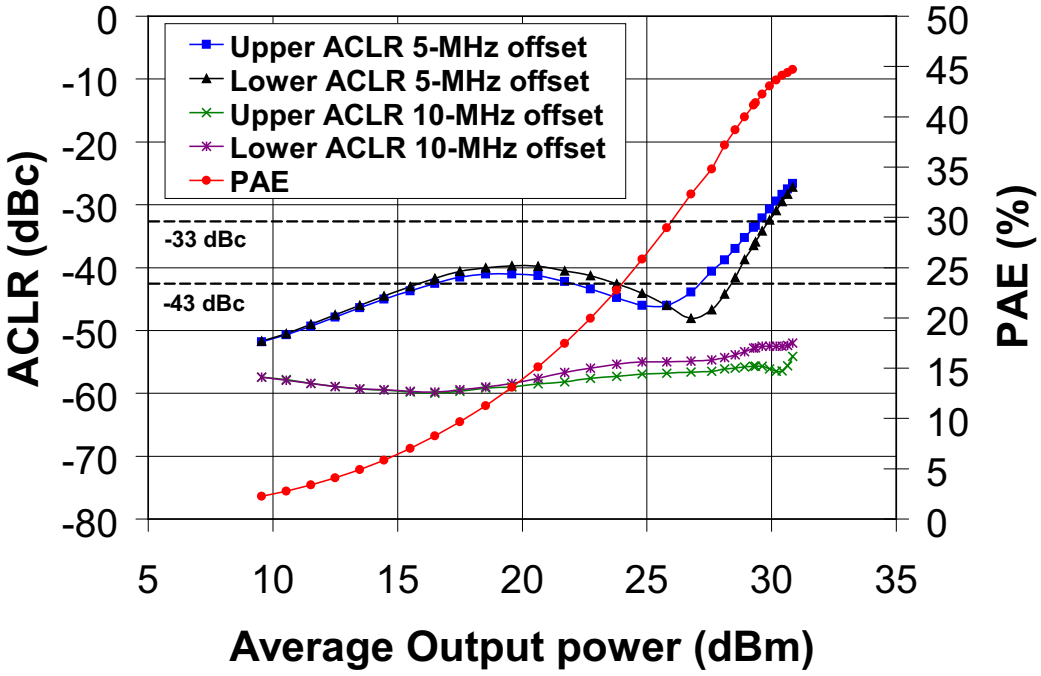


Figure 2.34: Measured ACLRs and PAE performance as a function of average output power using an uplink WCDMA input signal at 1.9 GHz.

and the ACLR at 10-MHz offset is below -52 dBc, meeting the -43-dBc requirement.

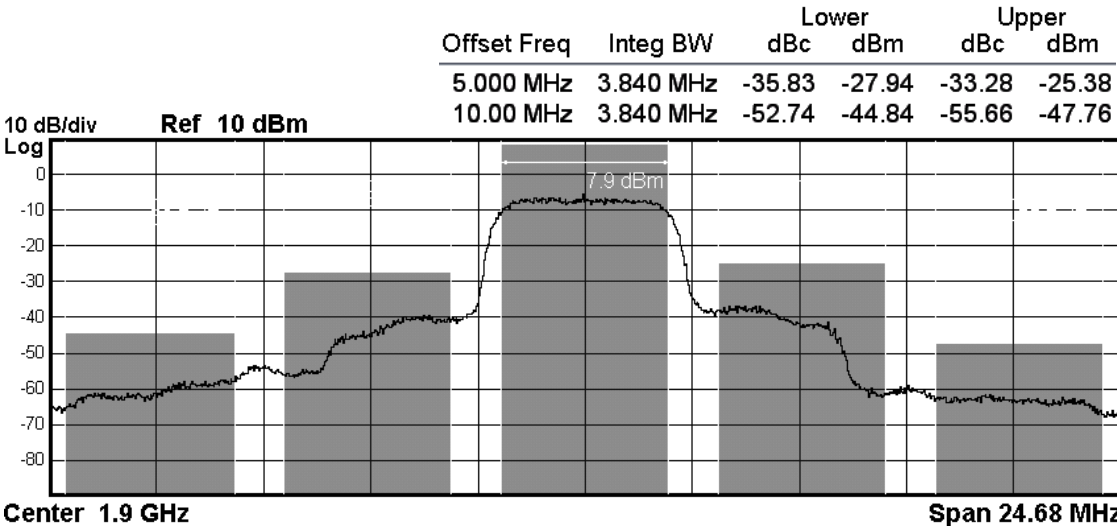


Figure 2.35: Measured WCDMA output spectra and ACLRs at P_{out} = 29.4 dBm.

Table 2.2 compares the performance of recently reported WCDMA power amplifiers for handsets. The implemented CMOS PA clearly exhibits efficiency and linearity performance comparable to those of GaAs-based PAs.

2.10 Summary

A single-stage stacked-FET linear PA has been demonstrated in SOI CMOS providing Watt-level output power in the GHz frequency range using 0.28-μm 2.5-V standard I/O FETs available in a 0.13-μm SOI CMOS technology. To solve the low breakdown voltage problem, the stacked-FET technique is employed to allow the use of higher supply voltage, resulting in a much lower impedance transformation ratio. The implemented SOI CMOS PA achieves 47% maximum PAE and delivers 32.4-dBm saturated output power at 1.9 GHz with a 6.5-V supply. Using a reverse-link IS-95 CDMA

Table 2.2: Performance comparison of recently reported WCDMA handset power amplifiers

Ref.	Technology	P_{out} (dBm)	PAE	Gain (dB)	ACLR @ P_{out}	V_{DD} (V)	Freq. (GHz)	Operating class
Vintola 01 [32]	AlGaAs/GaAs HBT	> 24	$> 27\%$	> 30	-36 dBc @ 26 dBm	3.5	1.95	AB
Jager 02 [33]	InGaP/GaAs HBT	27	38%	22.6	-37 dBc @ 27 dBm	N/A	1.95	AB
Srirattana 03 [34]	GaAs FET	29.7	46%	8.5	-38 dBc @ 28.6 dBm	N/A	1.95	Doherty 3-stage
Deng 05 [35]	SiGe HBT	23.9	31%	5.3	-33 dBc @ 23.9 dBm	3	1.95	AB
Zhang 09 [36]	InGaP/GaAs HBT	28	44.5%	N/A	-38 dBc @ 28 dBm	3.4	1.95	AB
Wang 04 [37]	CMOS 0.5 μm	24	29%	23.9	-35 dBc @ 24 dBm	3.3	1.75	Linearized AB 2-stage
This work	SOI CMOS 0.13 μm	29.4 28.5	41.4% 38.7%	14.6	-33 dBc @ 29.4 dBm -38 dBc @ 28.5 dBm	6.5	1.9	AB Single-stage

modulated signal, the PA shows an average output power of up to 28.7 dBm with a PAE of 41.2% while meeting the ACPR requirement. Using an uplink WCDMA modulated signal, the PA shows an average output power of up to 29.4 dBm with a PAE of 41.4% while meeting the ACLR requirement. A fully-integrated single-stage stacked-FET PA has also been demonstrated in SOS CMOS as a prototype, delivering a maximum output power of 21.0 dBm with the high efficiency of 44.0% at 1.88 GHz. The stacked-FET technique is clearly an attractive solution for designing high-efficiency linear PAs in advanced deep-submicron CMOS technology where the breakdown limit is much lower than the standard supply voltage.

2.11 Acknowledgements

Part of the material in chapter 2 is as it appears in "A 33-dBm 1.9-GHz silicon-on-insulator CMOS stacked-FET power amplifier," S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, in IEEE MTT-S Int. Microwave Symp. Dig., pp. 533-536, Jun. 2009, and "A watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS," S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, in IEEE Trans. Microw. Theory Tech., vol. 58, no. 1, pp. 57-64, Jan. 2010. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.

Chapter 3

Digitally-Modulated Power Amplifiers for Multi-Standard Polar Transmitters

3.1 Introduction

With the continuing development of next-generation wireless communication systems, there has been a great interest in multi-standard transmitters (TXs), which would facilitate a smooth adoption of new standards as well as provide the possibility for global roaming in a single mobile device. To reduce the cost and the system complexity, multi-mode multi-band building blocks that can handle various standards without redundant hardware are attractive. Current high-end smart phones incorporate up to 5 distinct power amplifiers to address the requirements for different communication bands and standards. The ideal solution is to have the whole system, from the digital baseband circuitry to the RF frontends, integrated onto a single CMOS chip. However, the design of a truly multi-standard CMOS TX is highly challenging, especially the integration of a multi-mode multi-band power amplifier since the PA needs to meet the stringent performance requirements of all integrated standards as well as provide highest-efficiency

operation over a wide bandwidth.

Recently, several possible solutions for CMOS multi-mode RF TX systems were reported [2,3,38,39]. The implementations in [2,3,39], however, provide low peak output power and would require one external PA with a large power gain for each frequency band. Moreover, the external PA is usually implemented by employing a conventional linear PA (class-A, AB) with a large power back-off to meet the stringent linearity requirements, resulting in much lower average power efficiency.

Power amplifiers with a polar architecture provide advantages for linear amplification without severely compromising power efficiency. The signal is decomposed into a constant-envelope phase-modulated RF signal and an envelope baseband component, allowing the use of a high-efficiency nonlinear PA to amplify the RF phase signal, while the envelope portion is restored at the output. For greatest flexibility, the envelope signal can be delivered to the PA as a digital signal. This approach is especially promising in the highly-integrated CMOS technology where signal generation and linearity improvement can be achieved through the use of digital signal processing as successfully demonstrated in several papers [2,4,39].

This work aims to develop a high-efficiency digitally-modulated power amplifier (DPA) in a 0.13-μm 1.2-V SOI CMOS technology. The DPA is to be used as the main building block in a proposed multi-standard CMOS RF polar transmitter described in the next section.

3.2 Direct-Digital Multi-standard Polar Transmitter

The concept of polar modulation can be traced back to the Envelope Elimination and Restoration (EER) technique proposed by Kahn in 1952 [40]. In Kahn's EER trans-

mitter, the power amplifier is a separate circuit block from the baseband circuitry and the upconversion mixers. The RF input signal, containing both envelope amplitude and phase modulation, is split into a constant-envelope phase signal and a low-frequency envelope signal by a limiter and an envelope detector, respectively. Both signals are then recombined in the last stage of a high-efficiency nonlinear power amplifier. In a fully integrated transmitter, however, the digital signal processing block can produce the amplitude and phase signals separately. After the recombination, the RF output waveform can be generally expressed in a polar representation as

$$v_{OUT}(t) = Re\{A(t)e^{(j\varphi(t)+j\omega_c(t))}\} = A(t)cos(\omega_c(t) + \varphi(t)) \tag{3.1}$$

where ω_c is the carrier angular frequency.

The envelope signal can be restored conventionally by an amplitude modulator, which modulates the supply voltage according to the envelope signal. Since the envelope signal has a much broader bandwidth than the RF signal, the amplitude modulator is required to have a broad enough bandwidth to avoid distorting the signal. The efficiency-bandwidth tradeoff and linearity of the amplitude modulator will directly affect the overall performance of the transmitter. In this work, we explore an alternative approach that directly uses the digital envelope signal to modulate the amplitude of the RF output without the need for digital-analog conversion and a separate amplitude modulator.

A possible block diagram of the direct-digital polar-based transmitter architecture is depicted in Fig. 3.1. The baseband I and Q signals are up-sampled and then converted into polar amplitude and phase signals in digital domain. The phase information $\varphi(t)$ is used to produce a phase-modulated RF input signal for the DPA. Phase

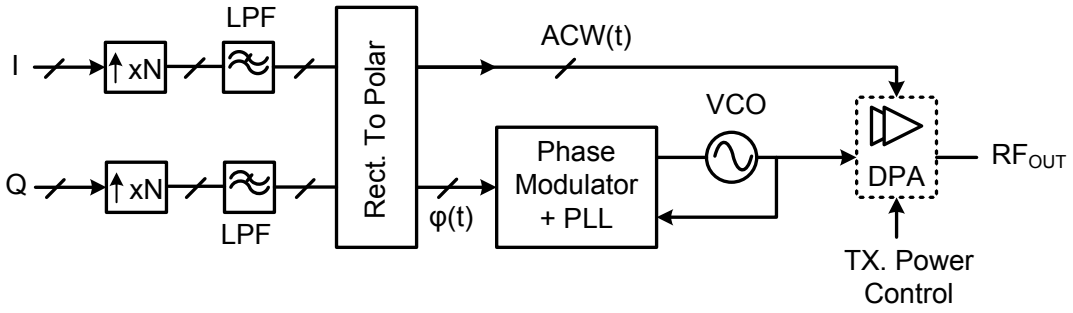


Figure 3.1: Direct-digital polar transmitter architecture.

modulation can be done digitally by an all-digital phase-locked loop (PLL) as proposed in [2]. The envelope signal is provided to the DPA as a 10-bit digital amplitude control word (ACW).

Fig. 3.2 shows the block diagram of the proposed DPA system. The building block integrated in the DPA silicon chip is inside the dotted line. The 7 most significant bits are decoded into a thermometer code and used to control the activation of 127 unit-weighted amplifiers, which are connected in parallel. The amplifiers' output currents are then combined at the drain to form the final RF output. The use of the binary-to-thermometer decoder helps avoid non-monotonic operation due to device mismatch. The 3 least significant bits of the ACW are used to control 3 binary-weighted amplifiers to provide extra resolution. The DPA is designed for multi-mode multi-band functionality by avoiding frequency-selective components, except for the final-stage output matching network, which can be implemented in future research as an on-chip tunable circuit to provide highest power-efficiency for various frequency bands.

The choice of using SOI CMOS technology has several advantages over the standard bulk CMOS. The first is the availability of high-performance RF power switches.

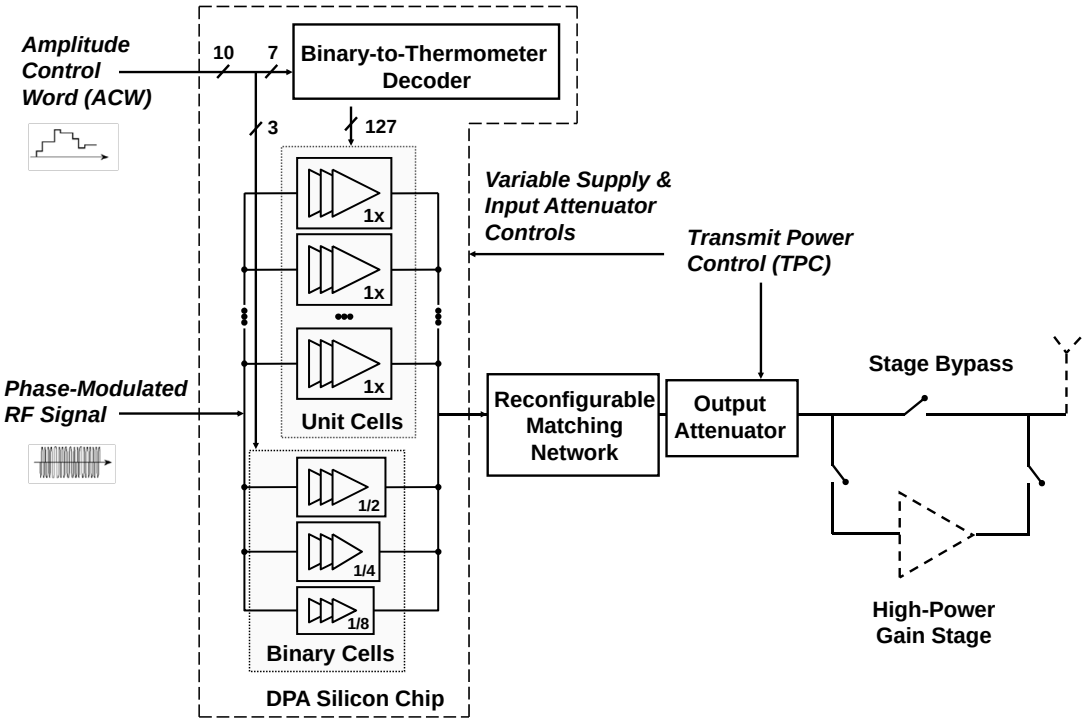


Figure 3.2: Block diagram of the proposed multi-standard DPA.

The high-resistivity substrate of the SOI CMOS also results in lower substrate coupling and lower-loss on-chip passive components. By arranging the RF switches as shown in Fig. 3.2, the DPA can be used to directly drive the antenna up to its full power (25-dBm peak output power) while an extra power amplifier is switched in only when the higher power is required, resulting in much improved average efficiency. An example of a stage-bypass power switch has been reported in [41] on the same SOI CMOS technology, managing up to a 35-dBm input power with less than 0.35-dB insertion loss from 500 MHz through 3 GHz with high linearity.

3.3 System-Level Requirements

3.3.1 Amplitude Resolution and Sampling Frequency

As an envelope amplitude signal is generated in the digital domain, the number of bits used to represent the signal determines the minimum possible white noise floor caused by the quantization error of the signal. Theoretically, the quantization noise improves by 6.02 dB for an additional bit of resolution. In order to meet the ACLR, EVM, and emission mask specifications for both GSM/EDGE and WCDMA with a reasonable margin, system simulations based on an idealized polar transmitter indicate that at least 7-bit resolution is required for amplitude modulation [3, 38]. In this work, the extra 3 least significant bits are also introduced to compensate for the decrease in effective resolution due to the nonlinearity of the amplitude modulation scheme. In [38], simulations were done with a WCDMA signal sampled at 38.4 MHz and an EDGE signal sampled at 26 MHz.

The noise performance can be improved by further increasing the oversampling

ratio. The total quantization noise power is spread over a wider frequency range, resulting in a lower noise floor within the nyquist zone, and as the replicas of the digital signal are generated at offset frequency multiples of the sampling frequency f_{CLK}, the filtering effect of the zero-order hold on those digital images is defined as

$$H(f) = 20 \cdot log(\frac{sin(\pi \cdot \frac{f}{f_{CLK}})}{\pi \cdot \frac{f}{f_{CLK}}}) \tag{3.2}$$

where f is the offset frequency from the carrier.

Fig. 3.3 shows the MATLAB-simulated output spectrum of a WCDMA signal with its envelope component quantized at different resolutions. A 5-bit resolution and a sampling rate of 122 MHz are required to meet the ACLR specifications for WCDMA. Similarly, as shown in Fig. 3.4, an 8-bit resolution and a sampling rate of 125 MHz are required to meet the spectral mask requirement for the EDGE-modulated signal.

The receive-band noise performance is another stringent requirement as the transmitter noise contributes to the sensitivity of the receiver. With 50-dB duplexer attenuation, a receive-band noise level of below -150 dBc/Hz is generally allowed for a practical WCDMA receiver sensitivity performance. To meet this requirement, envelope and phase filtering could be used to remove out-of-band spectral images and quantization noise as shown in Fig. 3.5.

3.3.2 AM/PM Time Alignment

Another critical issue for polar transmitter is the time alignment between amplitude and phase signals. As the two signals follow different paths before recombining at the output, slight time misalignments are often encountered. Such a misalignment will

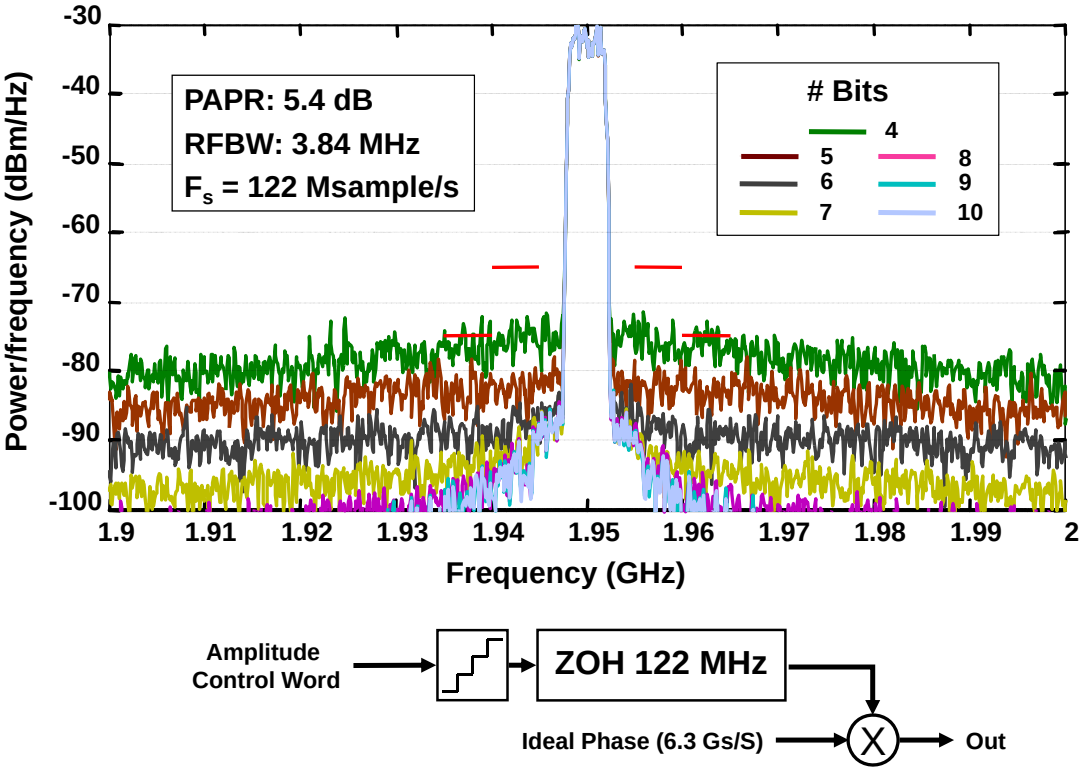


Figure 3.3: A WCDMA signal with the envelope component quantized at different resolutions.

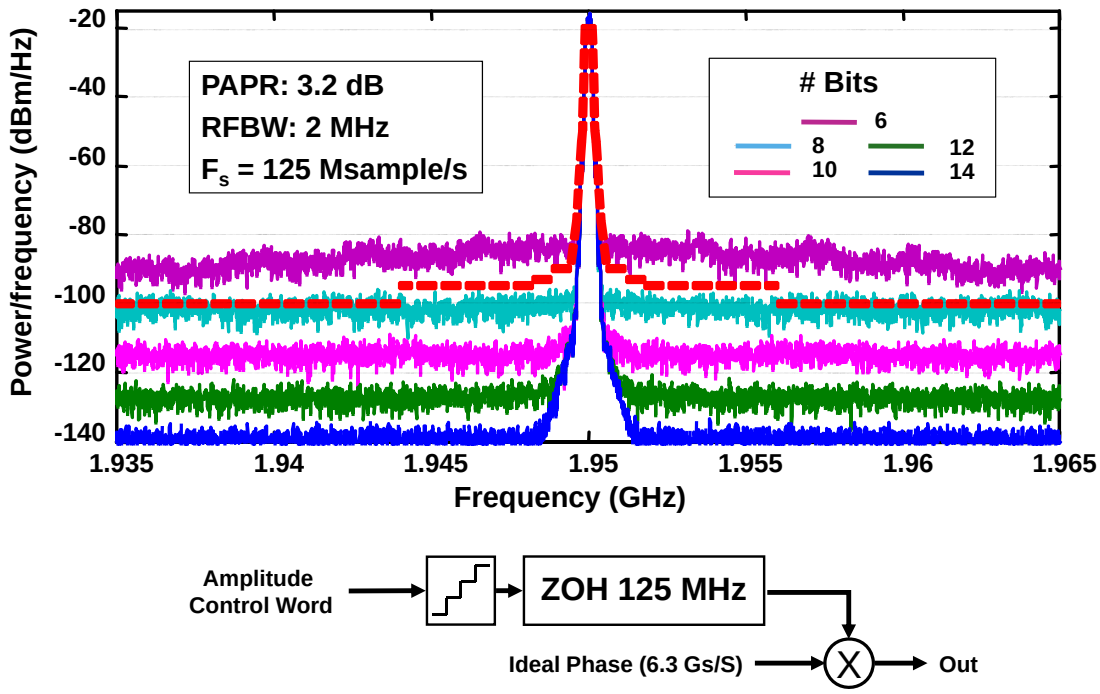


Figure 3.4: An EDGE signal with the envelope component quantized at different resolutions.

result in the appearance of a scaled replica of the wide PM spectrum on both sides of the original signal spectrum, corrupting adjacent channels in the process. For a two-tone signal, the effect of AM/PM misalignment can be theoretically predicted and the third-order intermodulation distortion (IMD_3) can be estimated as

$$IMD_3 = \frac{2}{\pi}(\tau \cdot BW_{RF})^2 \tag{3.3}$$

where τ is the time mismatch between the amplitude and phase paths and BW_{RF} is the bandwidth of the RF signal [38, 42, 43]. In a highly-integrated transmitter, the AM/PM time misalignment is predictable and can be compensated in the digital domain.

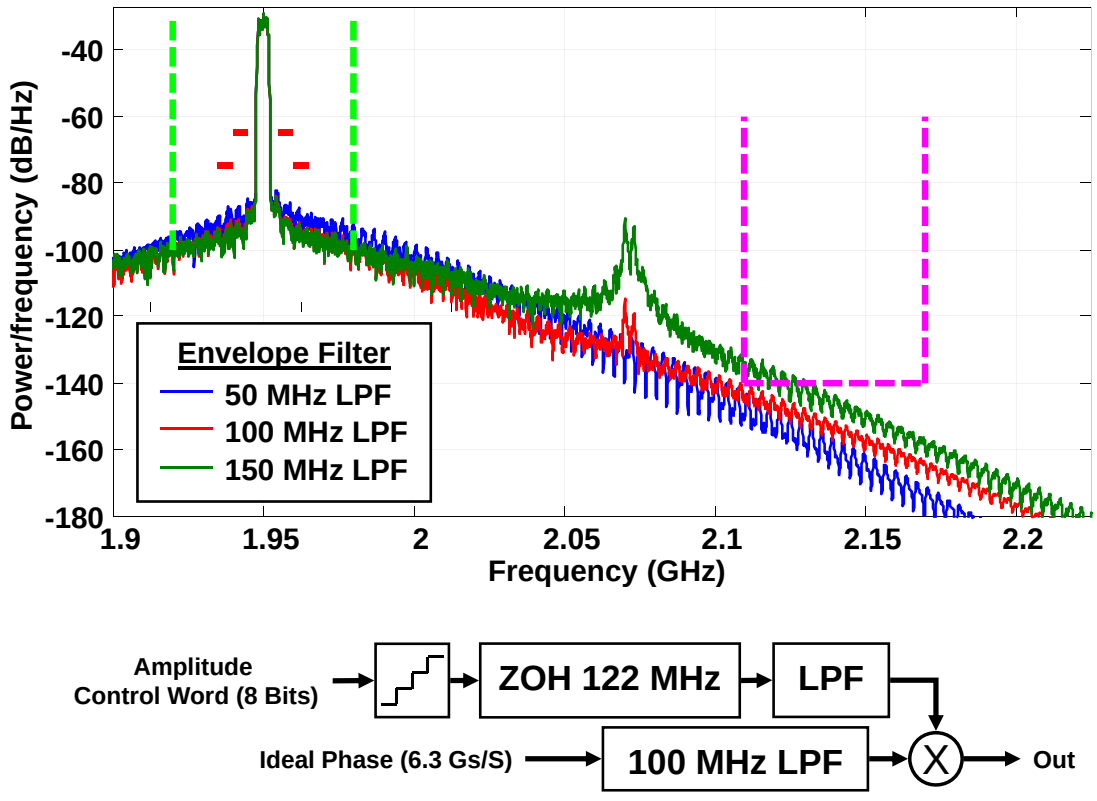


Figure 3.5: Effect of envelope and phase filtering on receive-band noise of a WCDMA signal reconstruction.

3.3.3 Transmit Power Control Requirement

Modern wireless communication standards also require a large transmit power control (TPC) range (70-80 dB for WCDMA and 30 dB for GSM/EDGE) while maintaining a sufficient signal quality. In this work, a transmit power control strategy is proposed as illustrated by Fig. 3.6, where the output power as a function of amplitude control word (ACW) is plotted in simulations at different power control settings. The transmit power control will be achieved by three main components: power supply voltage variation, input attenuator, and output attenuator. Moreover, the amplitude resolution can be reduced to obtain an extra power control range. In fact, power control through amplitude resolution reduction is more power-efficient and preferred over the use of attenuators wherever amplitude resolution is more than strictly needed for modulation as all unused unit amplifiers will be deactivated.

3.4 DPA Circuit Implementation

The simplified schematic of the DPA is illustrated in Fig. 3.7. Only one of the unit amplifiers is shown in detail. The 127 unit amplifiers and the 3 binary-weighted amplifiers are laid out in a rectangular array and connected in parallel by tree-structure input and output interconnects to minimize the phase mismatch. The driver stage of the unit amplifier is composed of a chain of digital inverters ($M2 - M3$, $M9 - M14$) and an input attenuator ($R1$, $C1$, $M15 - M16$), which can be used to reduce the input swing at the final stage through capacitive dividing, thus increasing the overall transmit power control range. Each unit amplifier's activation is controlled by an enable signal (EN), which is decoded from the 10-bit ACW and synchronized through a register. A digital

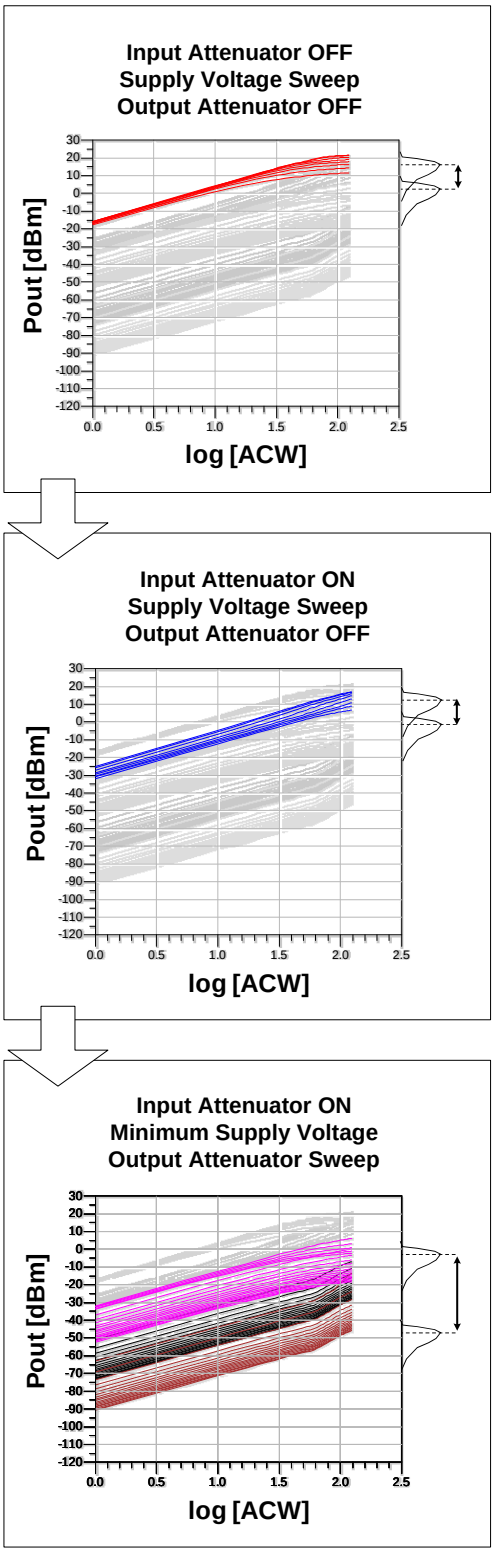


Figure 3.6: Proposed Transmit Power Control Strategy.

AND gate ($M4-M7$) is inserted at the input side of the driver stage. In this way, when the unit amplifier is deactivated, no switching power is consumed. In addition, when EN is low, transistors $M8$ and $M17$ are turned on to further ensure that the final power switch $M1$ is off and all intermediate nodes are in defined states.

Fig. 3.8 shows the circuit diagram of the implemented 10-bit decoder. All 10 bits are first synchronized at the input and the 7 most significant bits (MSBs) are fed to the 7-bit binary-to-thermometer decoder while the 3 least significant bits (LSBs) are kept undecoded to control the 3 binary amplifier cells. The 3 undecoded bits are fed through synchronized delay lines that match the delay of the binary-to-thermometer decoder.

The 7-bit binary-to-thermometer decoder is designed as a row-column matrix decoder [44–46]. The decoding logic consists of two steps. First, the digital input bits are split into two groups and decoded into thermometer-coded signals by a 4-bit row decoder and a 3-bit column decoder. The logic circuit in each matrix cell then determines whether to activate the corresponding unit amplifier based on the row and column positions.

Thermometer code has several advantages over binary-weighted code. When the digital input increases by 1 LSB, only one more unit amplifier is activated. Consequently, the RF output is always increasing as the digital input increases, guaranteeing monotonicity. Moreover, the glitch problem is also much improved. For example, the code transition from '0111111' to '1000000' causes only one more unit amplifier to switch ON in a thermometer-coded system while in a binary-coded system, all unit amplifiers will be switched.

All transistors are 0.13-μm 1.2-V FETs, except for the final power switch, which

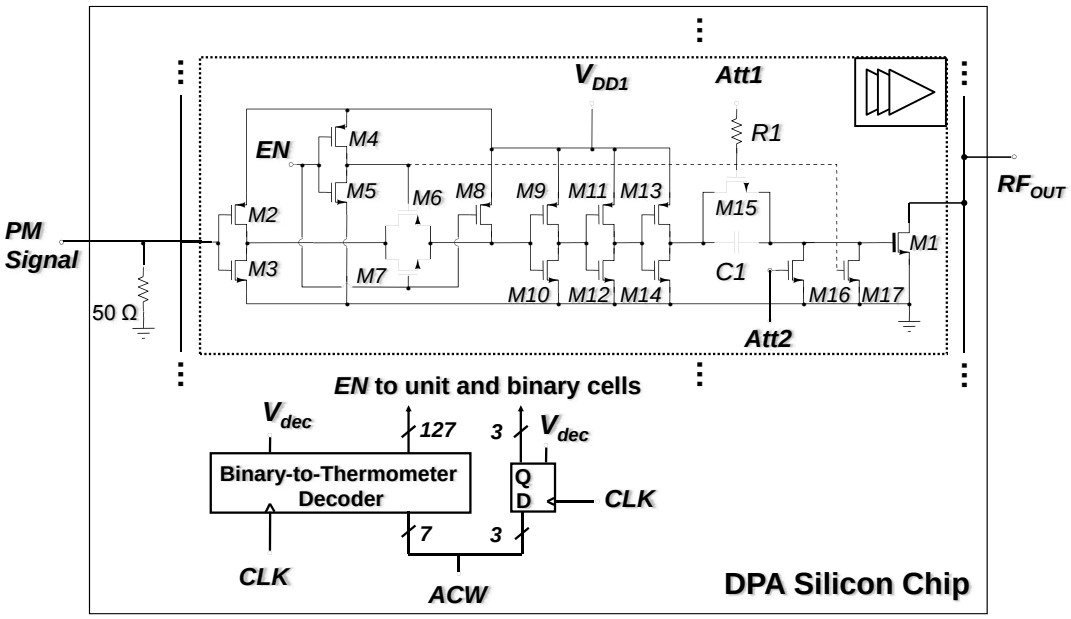


Figure 3.7: Simplified DPA schematic.

is a 0.28-μm 2.5-V standard I/O FET. The supply voltage (V_{DD1}) for the driver stage is 1.2 V, while the final-stage drain bias (V_{DD2}) is varied between 0.5 V and 2.1 V to provide average transmit power control. A 50-Ω termination is placed after the input pad to have defined input impedance and driving power. The input is DC-biased at 0.6 V and an RF input power of at least 5.5 dBm is needed to create a 1.2-V full-swing input signal. In a fully-integrated transmitter system, however, the DPA would be driven directly by the phase-modulated RF output of the PLL.

The amplitude-modulation mechanism of the DPA can be explained by looking at the load line of a unit device (final-stage switch). When activated, the unit device is hard-switched as its input swings between V_{DD1} and ground, and its load line tracks the device I-V curve (V_{GS} = V_{DD1} = 1.2 V) as illustrated by the simulation in Fig. 3.9.

To simplify the analysis, an idealized device model is assumed. When only

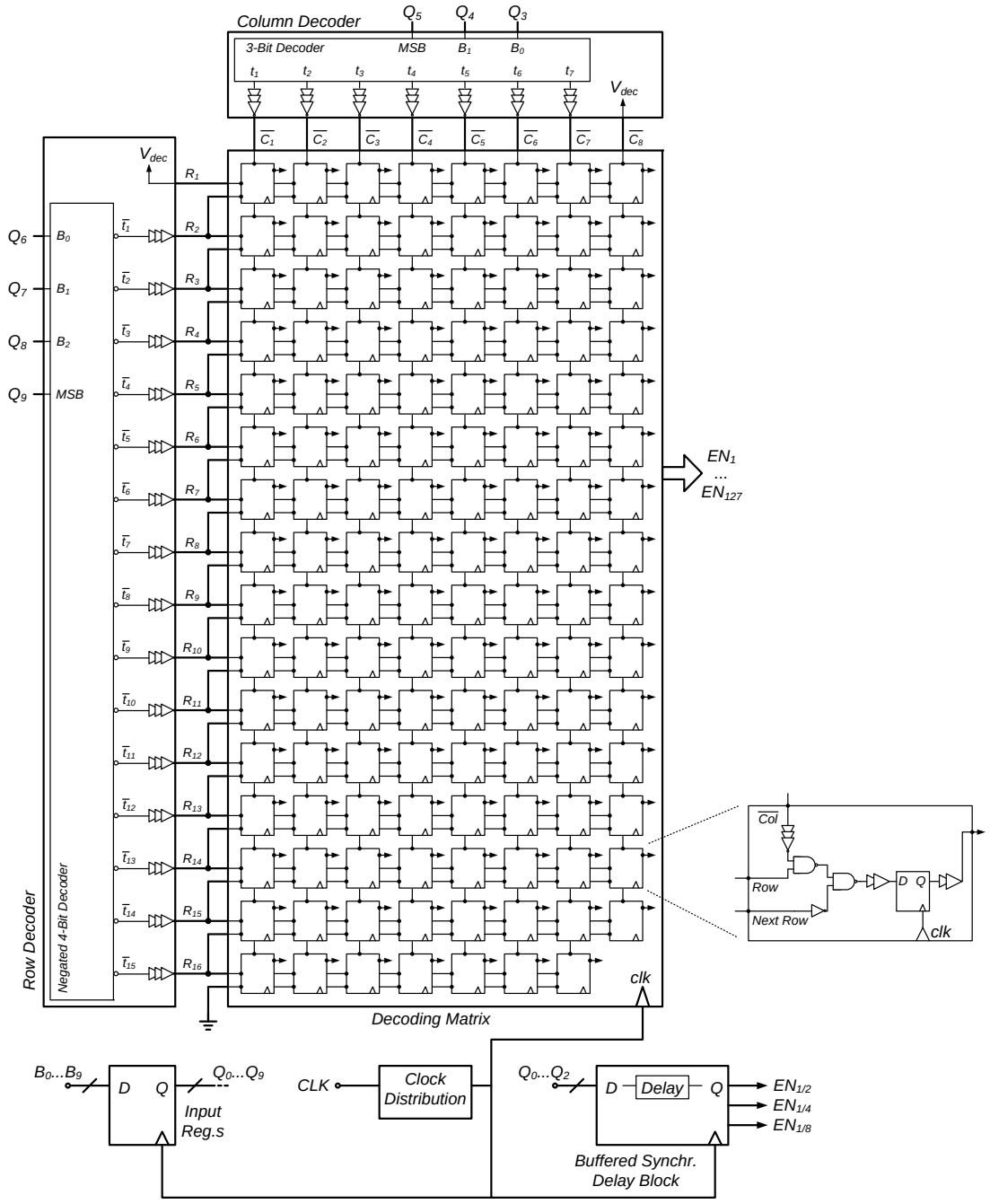


Figure 3.8: A binary-to-thermometer decoder schematic.

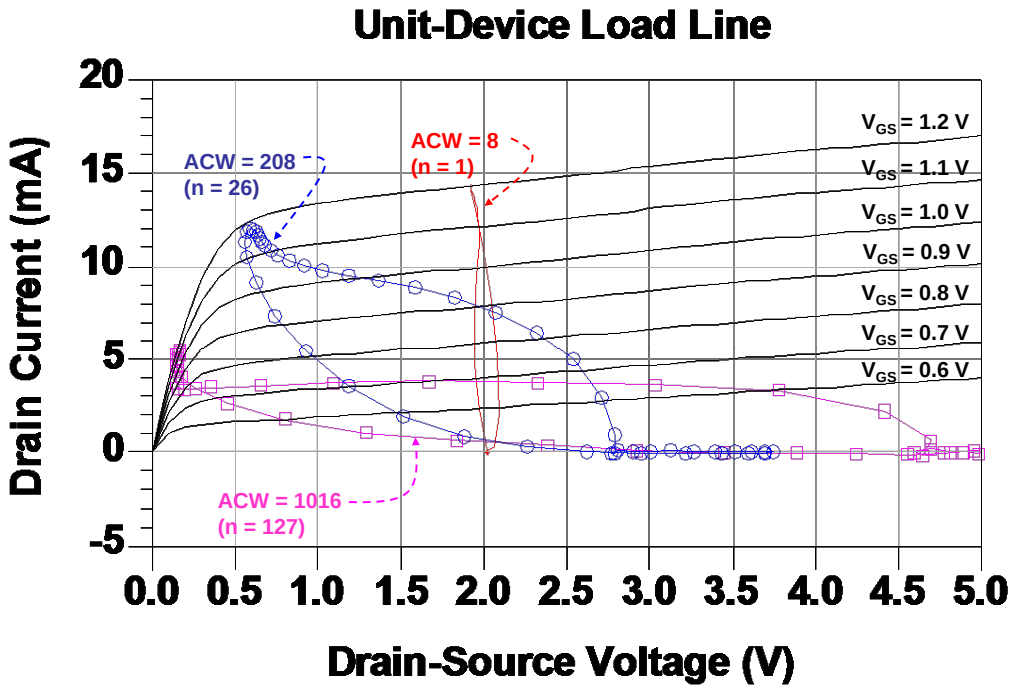


Figure 3.9: Simulated dynamic load line of an activated unit device with increasing ACW at 1.9 GHz.

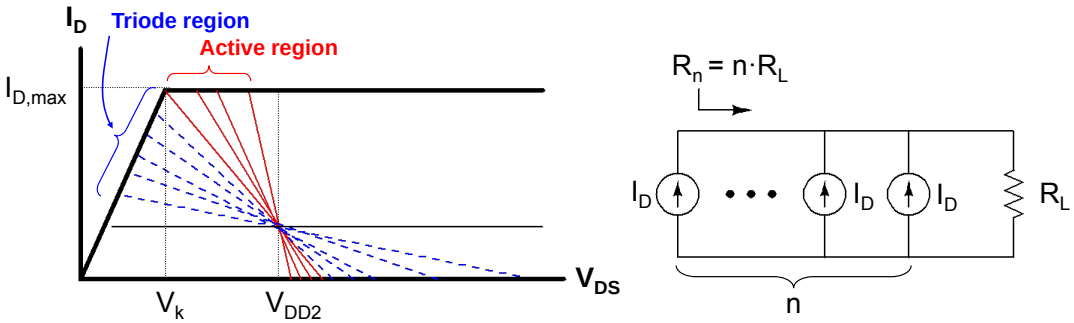


Figure 3.10: Load-pull effect on an activated unit-device load line.

one unit device is activated, the device sees a load resistance R_L and supplies a peak current $I_{D,max}$. As the number of activated unit amplifiers (n) increases, however, each unit device sees a larger load resistance of $n \cdot R_L$ due to the active load-pull effect and the device load line is rotated accordingly as shown in Fig. 3.10. The DPA can be described as operating in two separate regions depending on the number of activated unit devices. When n is small, each unit device operates entirely in its active region and acts as a constant current source. Consequently, the total RF output current is linearly proportional to n. The output power and efficiency can be derived as

$$P_{out} = \frac{1}{8} \cdot (I_{D,max}^2 R_L) \cdot n^2 \tag{3.4}$$

$$\frac{P_{out}}{P_{DC}} = \frac{1}{8} \cdot (\frac{I_{D,max}^2 R_L}{V_{DD2} I_{DC,unit}}) \cdot n \propto \sqrt{P_{out}} \tag{3.5}$$

In the actual devices, however, other device effects such as channel-length modulation introduce AM distortion. When n is large, the unit device will eventually enter its triode region ($V_{DS,min} < V_k$) and the RF current supplied by each device diminishes with the increasing n. As a result, the total output power delivered to the load saturates.

3.5 Layout

A die micrograph of the PA is shown in Fig. 3.11. The chip was fabricated in a 0.13-μm SOI CMOS technology. The total die area is 1.12 x 1.2 mm^2, including pads. A unit amplifier layout is shown in Fig. 3.12, where the driver, the input attenuator and the power devices are highlighted. The phase-modulated RF input signal is distributed to all unit amplifiers in a tree structure as illustrated in Fig. 3.13 to minimize the phase

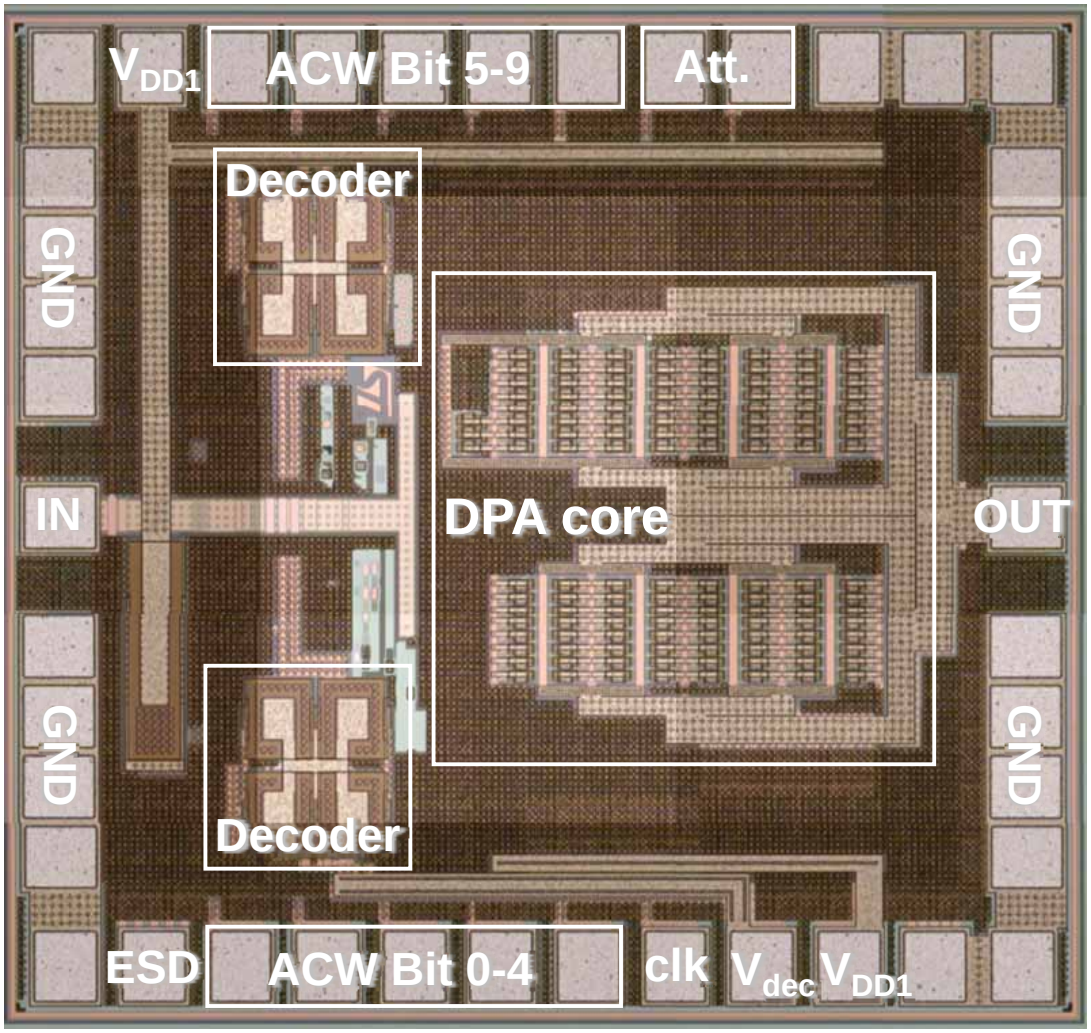


Figure 3.11: DPA chip micrograph.

difference between the unit amplifier cells. Similarly, the RF output lines are combined as shown in Fig. 3.14 using the 2 topmost metal layers.

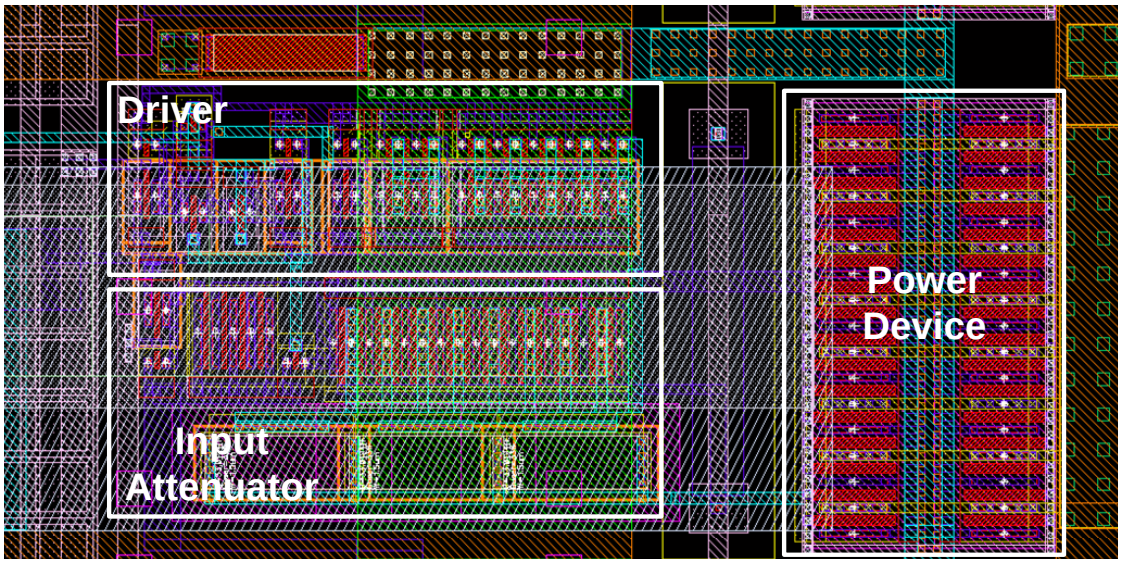


Figure 3.12: Layout of a unit amplifier.

3.6 Experimental results

The chip was mounted directly on a printed circuit board with off-chip output matching components, designed such that the DPA operation approaches a high-efficiency class-E mode. A photograph of the measured DPA board is depicted in Fig. 3.15. The DPA is also designed to operate reliably according to a recent study on FET degradation under RF stress in CMOS PAs [47]. In this case, the peak drain-source voltage is limited to 5 V in the simulation.

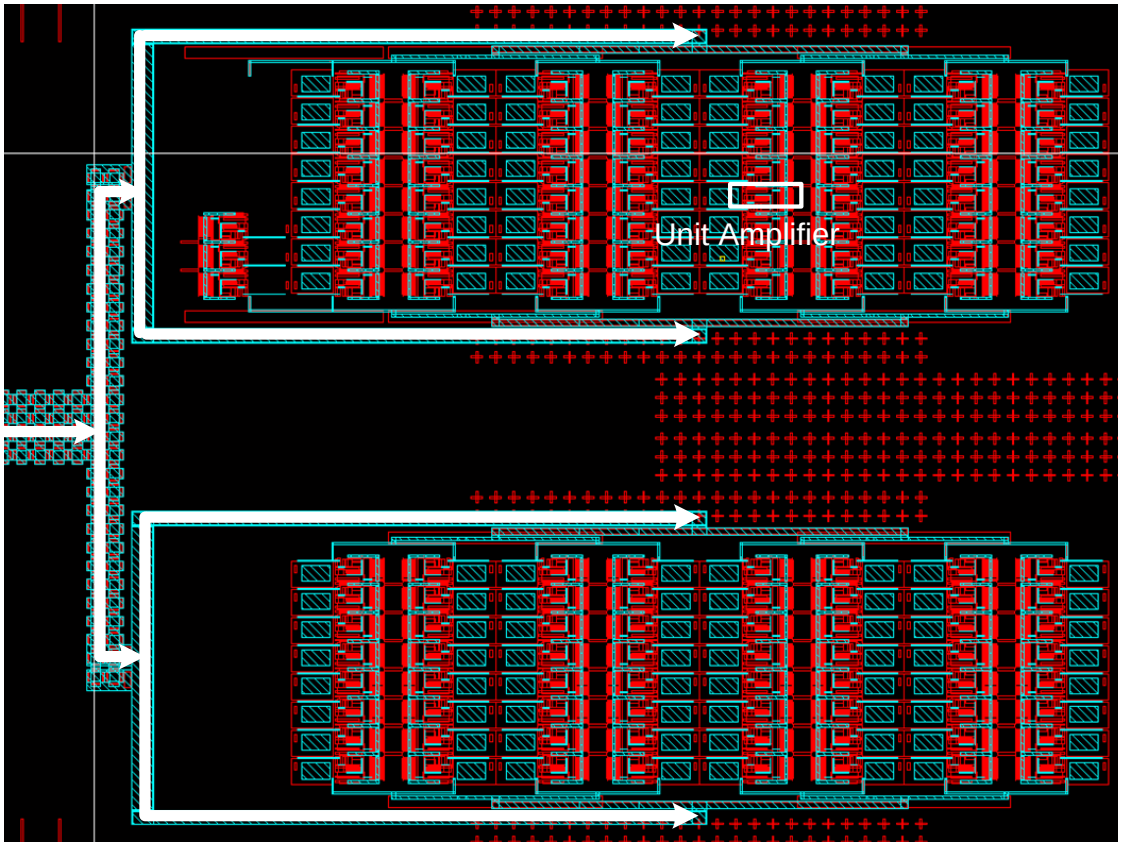


Figure 3.13: Phase-modulated RF input distribution.

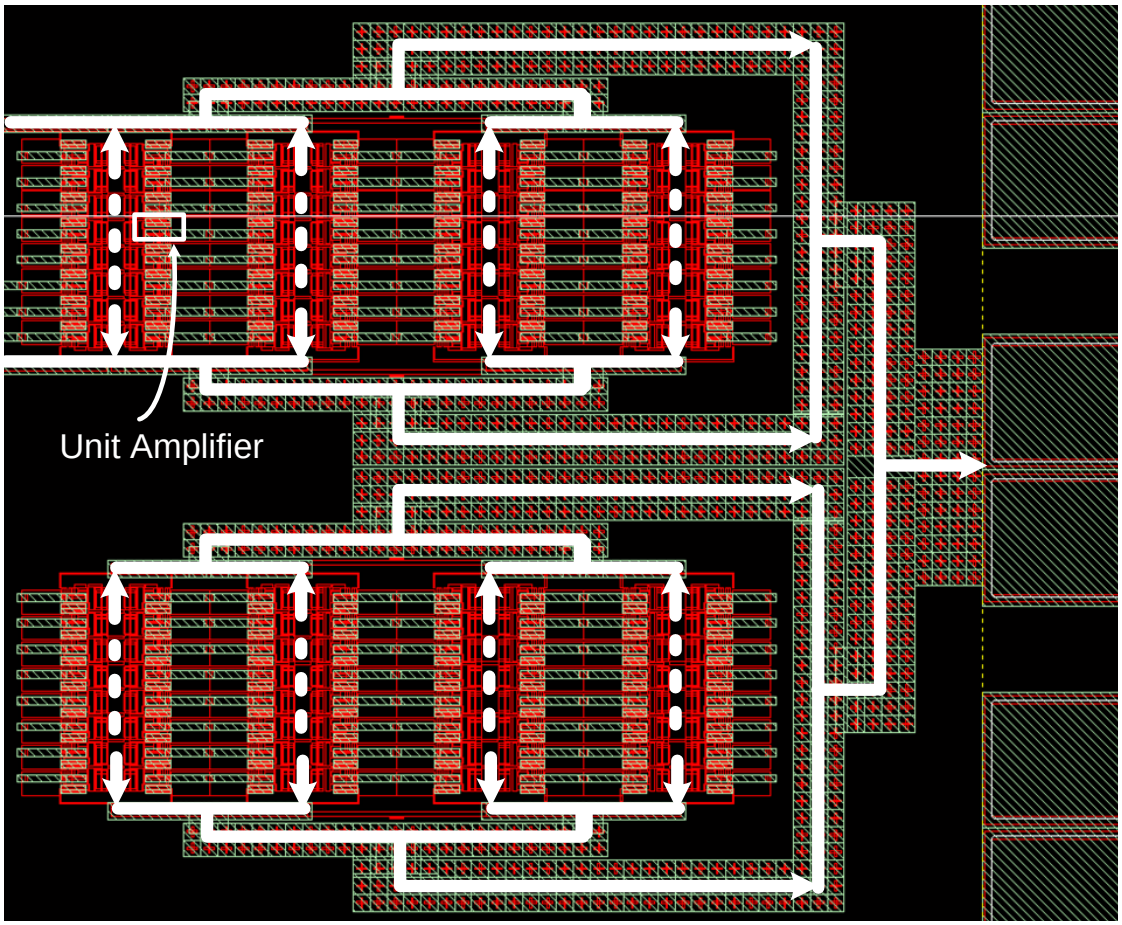


Figure 3.14: RF output combining in a tree structure.

3.6.1 CW measurements

Power measurements were performed under continuous-wave (CW) operation with a 900-MHz carrier frequency and a slowly varying ACW. Fig. 3.16 shows the monotonic variation of output power with ACW. The DPA delivered 24.9-dBm maximum output power with 62.7% maximum power efficiency, as well as achieving 43.9 dB of amplitude modulation (29 dB from the 7 most significant bits). The input attenuator and supply variation together provided approximately 16 dB of transmit power control range.

Fig. 3.17 and Fig. 3.17 illustrate the measured relationship between power efficiency and output power in log-log scale and linear scale, respectively. The power efficiency is approximately proportional to the square root of the output power as described in the previous section.

Traditionally, power amplifiers are characterized both by drain efficiency and PAE, along with gain. In this work, the input signal is a digital signal driven into a 50-Ω load with an overall power of 5.5 dBm. The input impedance would be much higher in an integrated system, and thus, the power dissipated would be very small.

With a large supply voltage and without input attenuation, the amplitude modulation is highly nonlinear due to the device operating in two regions as explained in the previous section. When the input attenuator is activated, however, the amplitude modulation becomes much more linear as the unit devices operate mostly in their active region as current sources. The worst-case phase distortion is measured to be lower than 21^o. Both the amplitude and phase distortions can be corrected in the baseband using an

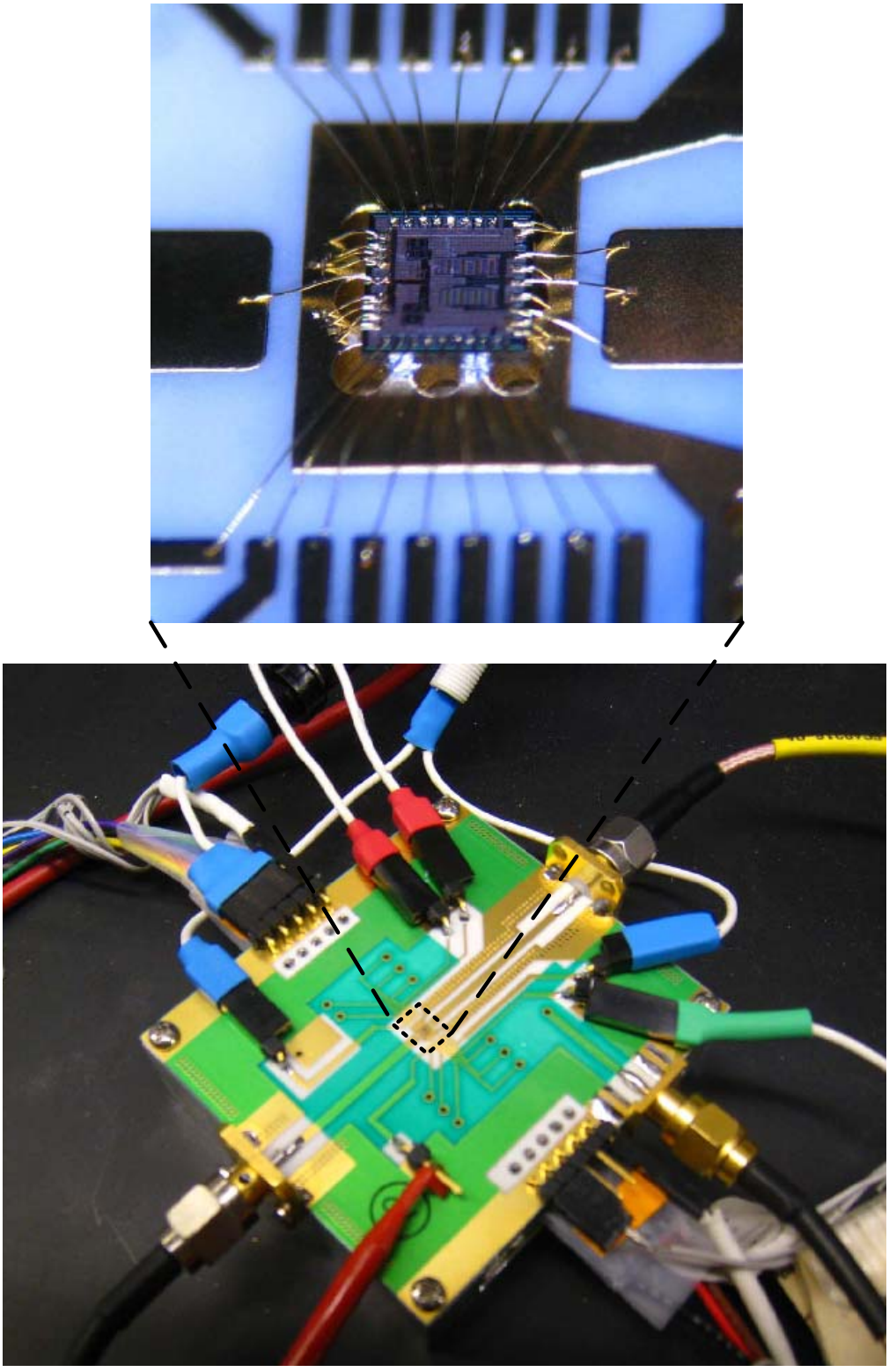


Figure 3.15: The DPA board for measurement.

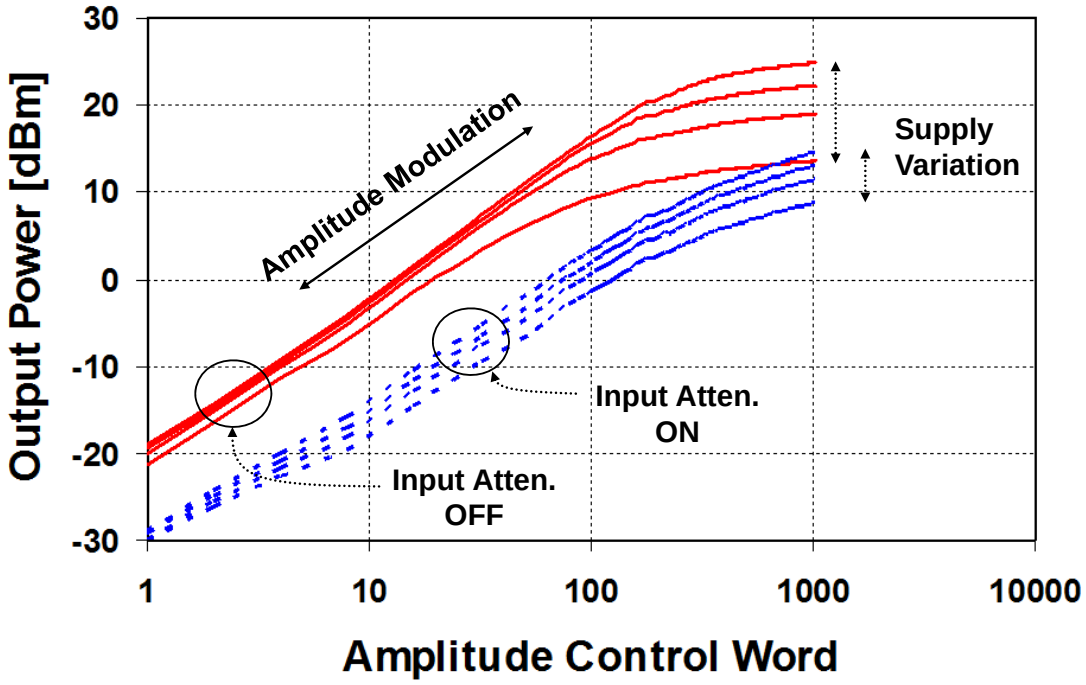


Figure 3.16: Measured output power vs. ACW at 900 MHz. The input attenuator and supply variation provide average transmit power control.

adaptive digital predistortion (DPD).

Similar performance is obtained in the measurement at other carrier frequencies by reconfiguring the output matching network. Moreover, a further simulation shows that it is also possible to design an optimized matching network to achieve relatively high efficiency operation ($>$ 40%) over a very broad bandwidth, albeit with slightly lower output power, as shown in Fig. 3.18. However, this possibility is limited in the measurement due to excessive drain capacitance, which reduces the optimum operating frequency range. With an output matching network optimized at 1.92 GHz, the DPA delivered 23.31-dBm maximum output power with 36.7% overall efficiency.

To linearize the DPA, an ideal digital predistortion system is first simulated in

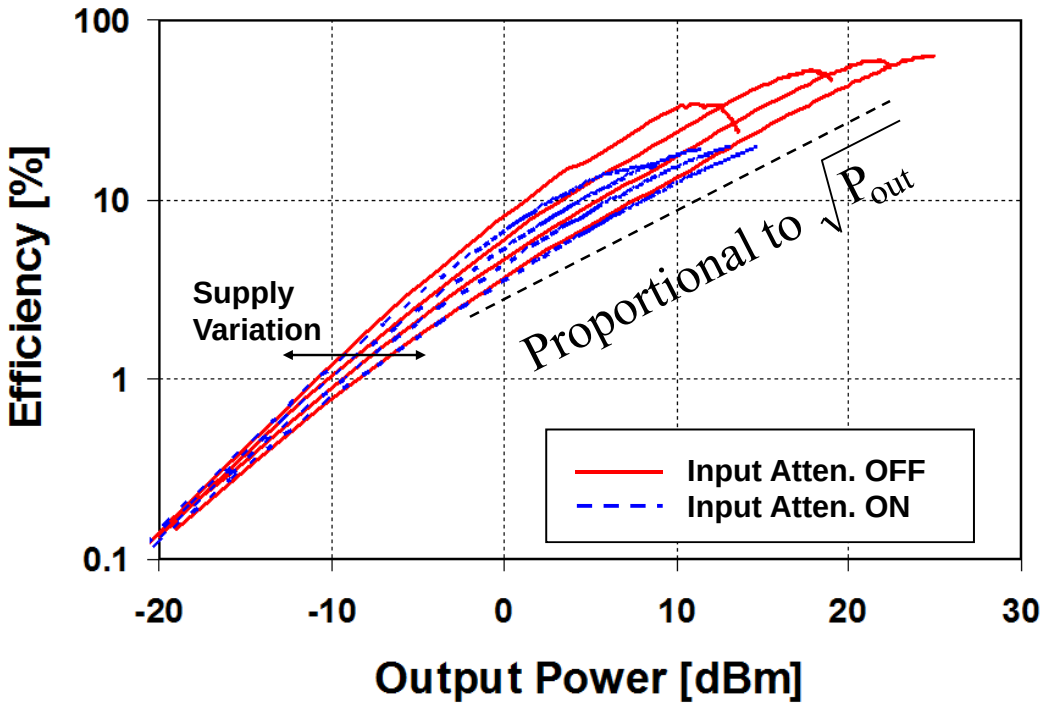


Figure 3.17: Measured efficiency vs. output power at 900 MHz, in log-log scale.

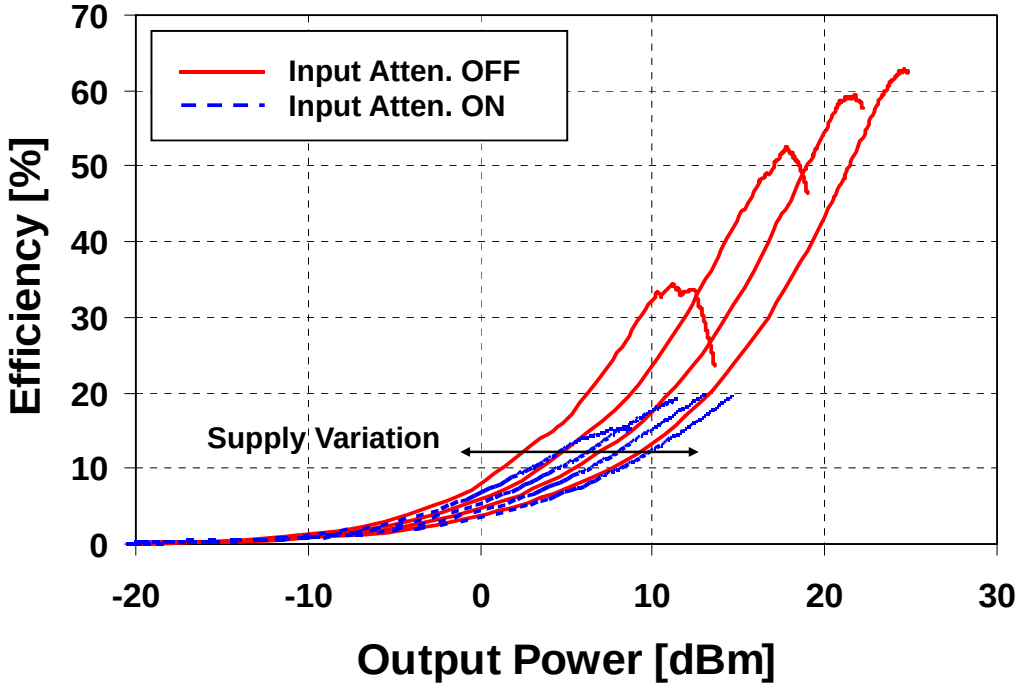


Figure 3.18: Measured efficiency vs. output power at 900 MHz.

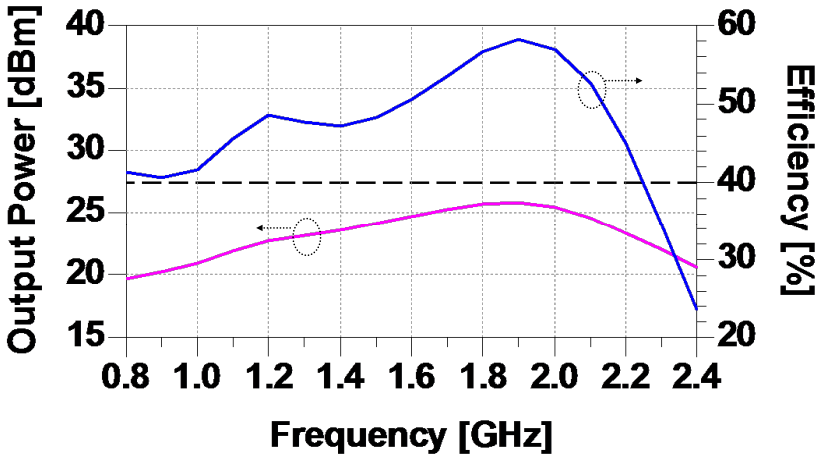


Figure 3.19: Simulated output power and efficiency vs. carrier frequency with a fixed output matching network optimized for a broadband performance.

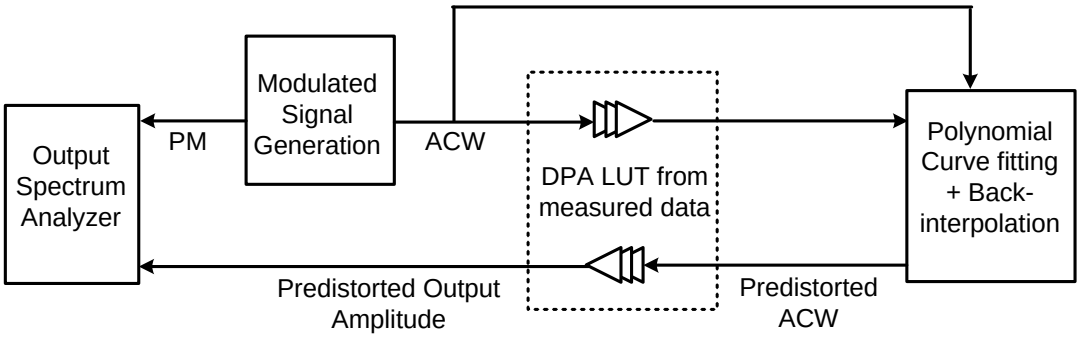


Figure 3.20: Block diagram of the simulated ideal DPD system.

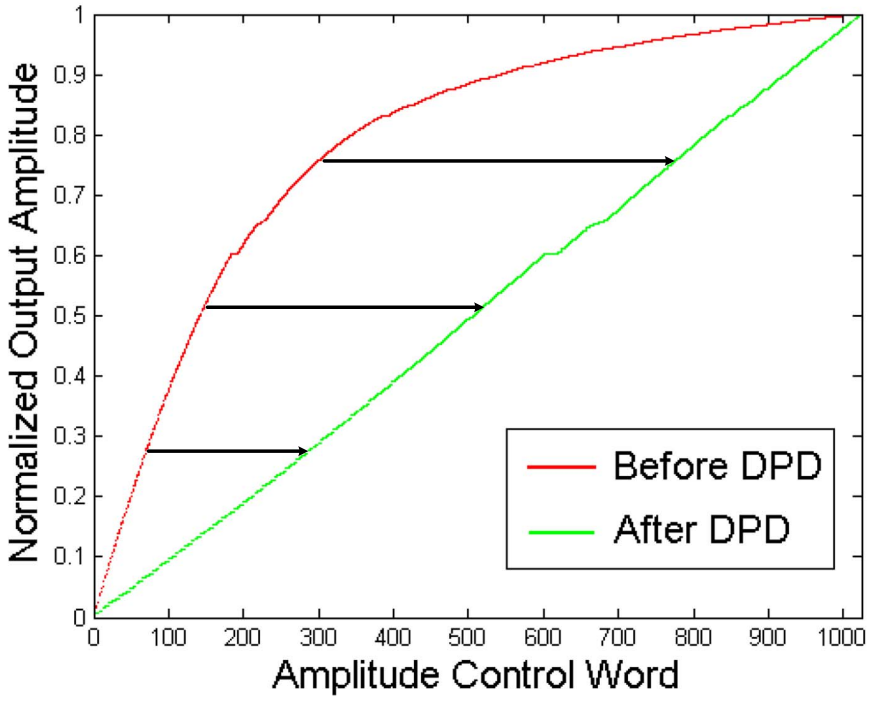


Figure 3.21: ACW-AM characteristic of the DPA, before and after ideal DPD.

MATLAB based on the measured steady-state ACW-AM transfer characteristic of the DPA. The block diagram of the simulated system is illustrated in Fig. 3.20, where only ACW-AM nonlinearity is compensated and ACW-PM characteristic is assumed to be ideal. The simulated ACW-AM characteristic of the DPA before and after ideal DPD is shown in Fig. 3.21 on a normalized linear scale. Notice that the lowest output power range is mapped to a much wider ACW range after the DPD, resulting in a resolution loss; while the resolution is much finer in the highest ACW range.

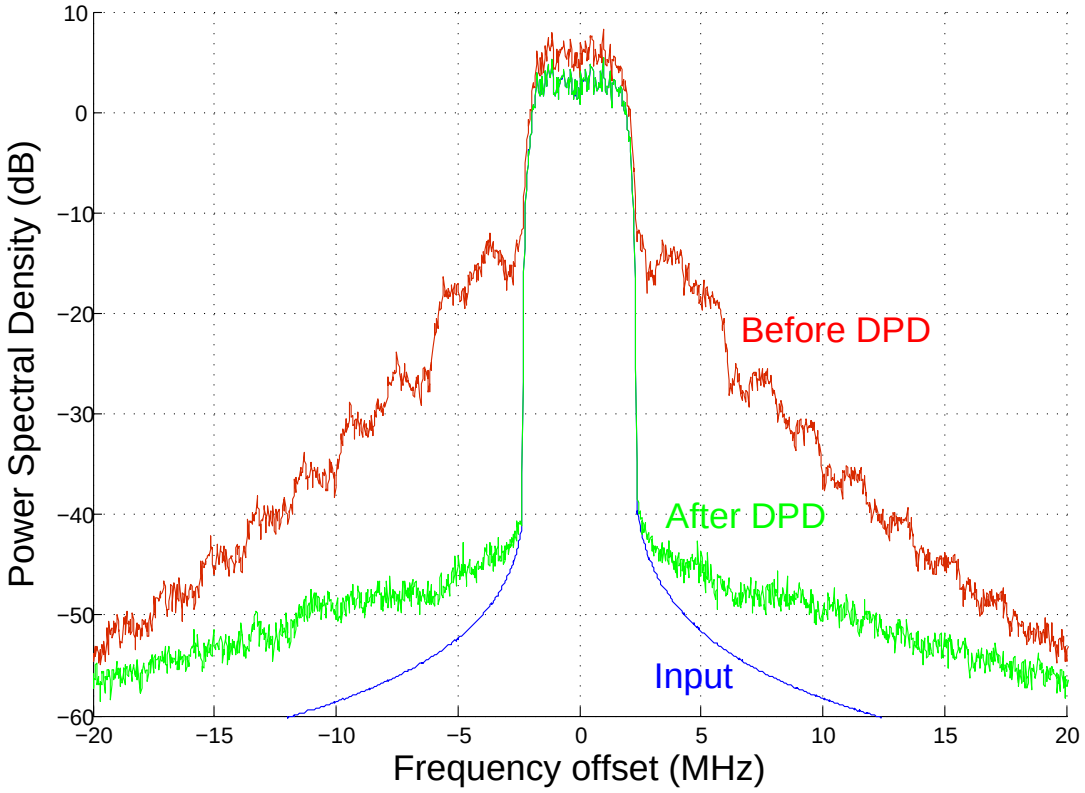


Figure 3.22: Simulated output spectrum of a WCDMA-modulated signal, before and after ideal DPD.

The generated EDGE and WCDMA input signals have PAPRs of 3.3 dB and 3.4 dB, and their simulated output spectra, before and after ideal DPD, are shown in

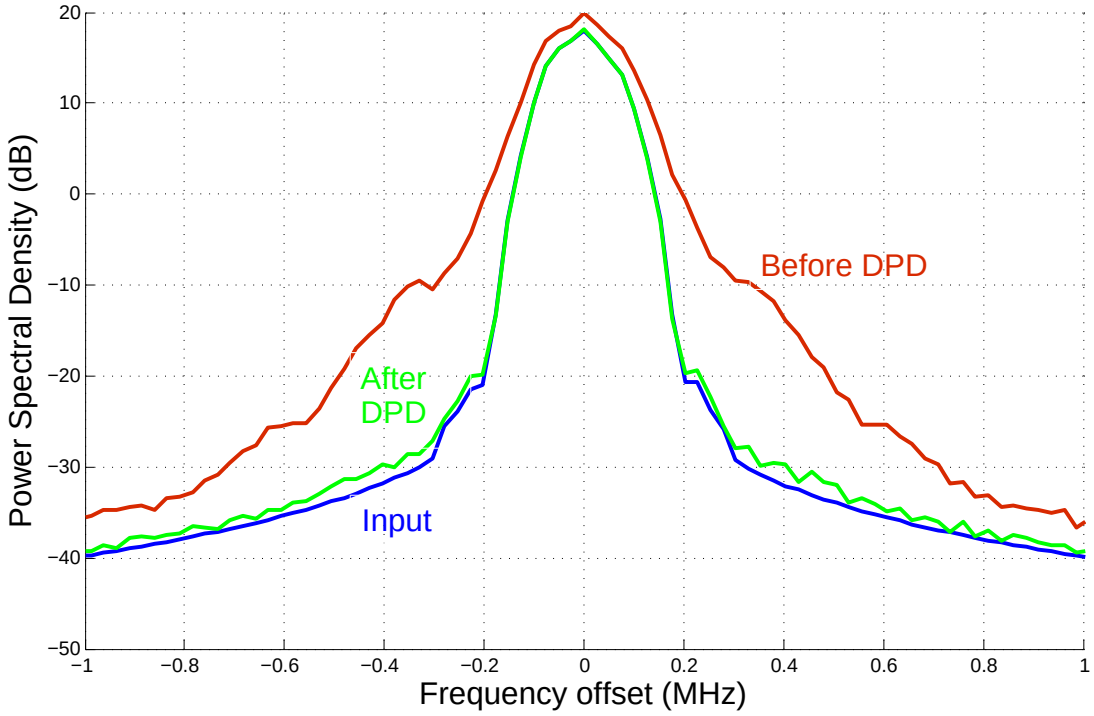


Figure 3.23: Simulated output spectrum of an EDGE-modulated signal, before and after ideal DPD.

Fig. 3.23 and Fig. 3.22, respectively. The EDGE input signal used here, however, is a short-length variation of the real EDGE signal and will not conform to the spectral mask specifications outlined in Chapter 1. The simulations show a 2 dB and a 5-8 dB degradation on the spectral performance for EDGE and WCDMA, respectively, after ideal DPD. These results show that the effective resolution is sufficient to meet the specifications.

3.6.2 WCDMA/EDGE Modulation with Digital Predistortion

Fig. 3.24 shows the demonstration system used to evaluate the performance of the DPA with practical modulated signals. An adaptive digital predistortion (DPD) loop [43] was employed to linearize the amplifier. Some advantages of adaptive DPD are that loop stability is much easier to maintain and it is relatively simple to implement with digital signal processing. The DPD system needs to be adaptive since both the AM-AM and AM-PM distortions can change with different power control settings.

First, the baseband signal is split into AM and PM components, which are time-aligned and predistorted based on the signal fed back from the output. A semi-automatic process is used to obtain accurate time mismatch information between AM and PM components. The AM signal is then fed to the DPA as a 10-bit ACW input. The PM component is used to modulate a 52-MHz digital IF carrier, which is subsequently up-converted, amplified and filtered before being fed to the DPA RF input. The RF output of the DPA is then fed back to the signal-generation system at the input through a down-converter, a low-pass filter, and a digital-IF receiver. The whole system is clocked at 207.36 MHz.

The output spectrum after DPD is shown in Fig. 3.25 for a short-length EDGE

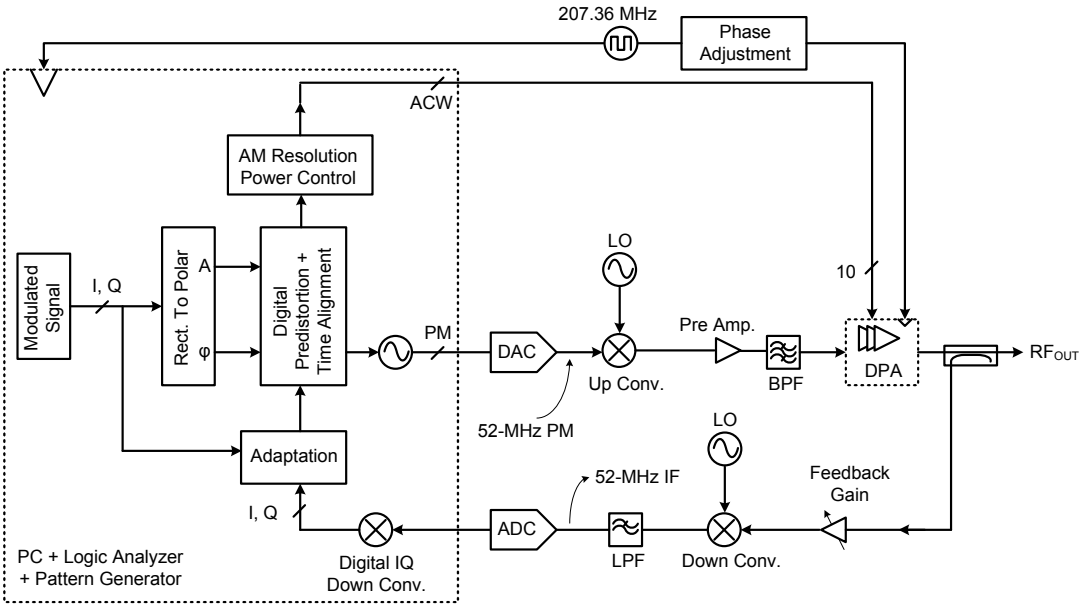


Figure 3.24: Block diagram of the polar modulation and predistortion test setup.

signal at 1.92 GHz. As summarized in Table 3.1, the measured spectral performance after DPD is in line with the simulated performance. The measured output power is 19.98 dBm with 31.83% overall efficiency. The DPA is also tested at 915 MHz, exhibiting a similar spectral performance with a much higher output power and efficiency, as summarized in Table 3.2.

For a WCDMA signal at 1.92 GHz, the measured output power is 19.26 dBm with 30.28% overall efficiency after DPD. The ACLR is -30.3 dBc and -43.32 dBc at 5 MHz and 10 MHz, respectively. The measured ACLR at 5-MHz offset frequency violates the -33-dBc specification due to the limited frequency response of the amplifier-cell commutation. Without sufficient driving power (due to excessive ACW interconnect parasitics), the turn-on and turn-off transients can be relatively slow compared to the envelope rate. The resulting memory effect degrades AM/PM time-alignment accuracy

and DPD performance in WCDMA, where the envelope bandwidth is much larger.

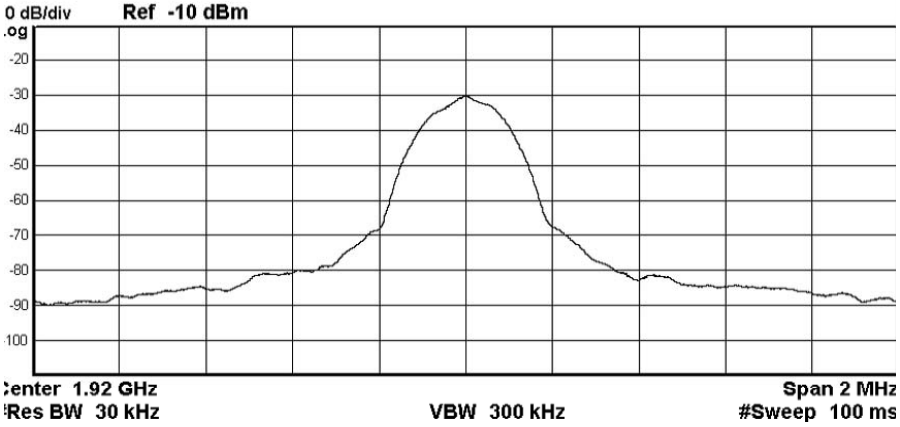


Figure 3.25: Measured EDGE output spectrum after DPD.

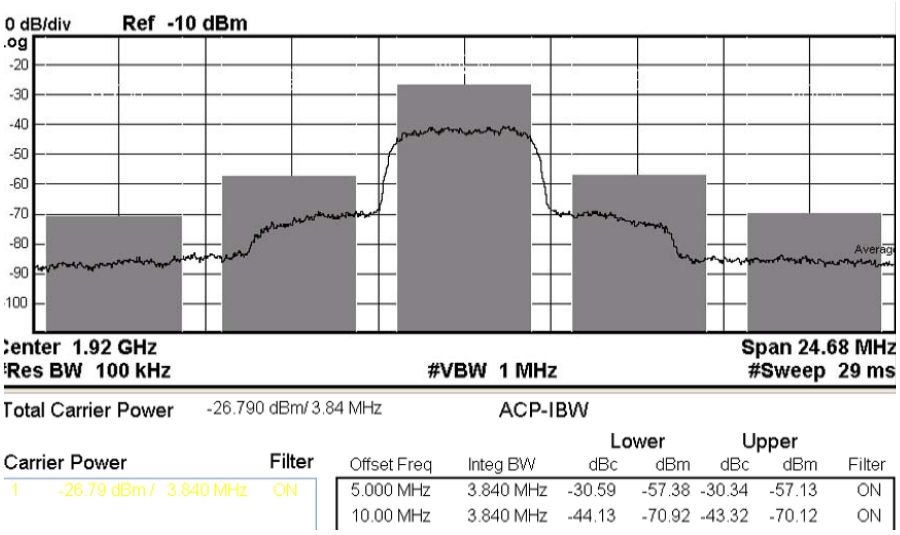


Figure 3.26: Measured WCDMA output spectrum and ACLRs after DPD.

Table 3.1: Simulated and measured EDGE spectral performance comparison.

Relative power after DPD	**400-kHz offset**	**600-kHz offset**
Simulation	-47.7 dBc	-52.9 dBc
Measurement	-52.5 dBc	-54.3 dBc

Table 3.2: Measured RF output power and overall efficiency for EDGE and WCDMA after DPD.

Modulated signal	**RF output power**	**Efficiency**
EDGE (915 MHz)	22.69 dBm	51.75%
EDGE (1.92 GHz)	19.98 dBm	31.83%
WCDMA (1.92 GHz)	19.26 dBm	30.28%

3.7 Summary

A high-efficiency single-ended digitally-modulated power amplifier has been demonstrated in a 0.13-μm 1.2-V SOI CMOS technology. It reliably delivers a 24.9-dBm peak output power with a maximum power efficiency of 62.7% at 900 MHz, as well as exhibits multi-band functionality with a reconfigured matching network. The 10-bit resolution provides more than 40 dB of amplitude modulation; while the integrated input attenuator and supply variation together provide 16 dB of transmit power control range. By employing an adaptive digital pre-distortion technique, the DPA could meet linearity requirements for both the EDGE and WCDMA standards. The implemented DPA, together with the proposed polar architecture, is an attractive solution for the next-generation multi-standard RF transmitter design.

3.8 Acknowledgements

Part of the material in chapter 3 is as it appears in "A 25-dBm high-efficiency digitally-modulated SOI CMOS power amplifier for multi-standard RF polar transmitters," S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, in IEEE RFIC Symp. Dig., pp. 157-160, Jun. 2009. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for this publication.

Chapter 4

Conclusion

4.1 Research Summary

The low breakdown voltage limit is one of the most critical problems in realizing high-efficiency linear power amplifier in CMOS technology, especially with the on-going technology scaling to deep submicron dimensions. A state-of-the-art CMOS device would require a large impedance transformation ratio to deliver enough output power, resulting in high loss in the matching network. As preserving battery life and meeting linearity requirements have been priorities in mobile handsets, power amplifiers are commercially implemented using more expensive GaAs-based technologies. This dissertation proposes a stacked-FET topology as an attractive solution to the breakdown limit problem. The voltage stress is equally divided among several transistors connected in series such that the output voltage swing is added in phase, allowing the use of a much higher supply voltage. Several design issues are highlighted and discussed including proper gate biasing of stacked devices and output matching network design. By using the proposed design technique, excellent power efficiency and linearity performance comparable to those of GaAs-based power amplifiers can be achieved in CMOS

at GHz frequency range. To demonstrate the concept, single-stage stacked-FET power amplifiers are implemented using alternative CMOS processes to avoid the body effect and excessive junction capacitances.

A fully integrated class-A power amplifier is implemented in 0.25-μm SOS CMOS as a prototype, delivering a maximum output power of 21.0 dBm with the high efficiency of 44.0% at 1.88 GHz. By using triple-stacked FETs, the optimum load impedance increases to 50 Ω so impedance transformation is not required at the output. The input matching network is also included on-chip. The amplifier meets the ACPR specification for IS-95 CDMA operation up to an average output power of 16.3 dBm and PAE of 18.7%. To meet the Watt-level output power required in modern standards, a deep class-AB power amplifier has been implemented and investigated using 0.28-μm 2.5-V standard I/O FETs available in a 0.13-μm SOI CMOS technology. The amplifier achieves 47% maximum PAE and delivers 32.4-dBm saturated output power at 1.9 GHz with a 6.5-V supply. Using a reverse-link IS-95 CDMA modulated signal, the amplifier shows an average output power of up to 28.7 dBm with a PAE of 41.2% while meeting the ACPR requirement. Likewise, the amplifier meets the ACLR requirement of the uplink WCDMA with an average output power of up to 29.4 dBm and a PAE of 41.4%. In addition, the amplifier has been tested in the low frequency band at 900 MHz with a reconfigured matching circuitry. A small-signal gain of 19.3 dB is achieved with a saturated output power of 29.5 dBm and a maximum PAE of 53%.

In the second part of the dissertation, a polar-based digital-intensive transceiver architecture is explored for multi-mode multi-band applications. A 10-bit single-ended DPA is demonstrated in a 0.13-μm 1.2-V SOI CMOS technology, where the amplitude modulation is done by digitally controlling the number of activated unit amplifiers

whose currents are summed at the output. The DPA is operated as a pseudo class-E amplifier at full power while its efficiency rolls off with decreasing output power similar to a class-B amplifier. The measured DPA delivers a 24.9-dBm peak output power at 900 MHz with a maximum power efficiency of 62.7%. Similar high-efficiency performance is also exhibited in the high band with a reconfigured matching network. Moreover, by employing an adaptive digital pre-distortion technique, the DPA could meet linearity requirements for both the EDGE and WCDMA standards. This work demonstrates that the possibility of co-integrating high performance digital transistors with the CMOS power amplifier enables multi-band multi-standard applications with the addition of only one extra component in the external matching.

4.2 Future Work

The research work described in this dissertation represents starting points for several future researches and developments. First, the proposed stacked-FET technique provides a mean to achieve high output power with lower loss in matching network due to high impedance transformation. Since the RF input signal only drives the bottom transistor, instead of simultaneously being fed to all series-connected devices, the synchronization problem among devices is eliminated. However, each device will see a different drain current waveform due to current leakage through gate capacitances, especially at high frequency, making it difficult to achieve high efficiency though current and voltage waveform engineering. In fact, waveform shaping through harmonic impedance tuning is already difficult in the stacked-FET structure as the influence of output matching circuitry diminishes down the ladder. To achieve high efficiency, the signal waveform across the drain and source terminals of each device could be carefully

engineered by adding tuning components between the device connections.

In the second part of the dissertation, we show that a compact transmitter can be implemented all in the digital domain with excellent performances. However, a reconfigurable matching network is still necessary to produce a true multi-mode multi-band transmitter system. Moreover, meeting the linearity and the wide transmitted-power control requirements for modern wireless standards is still a challenge. The amplitude modulation of the DPA is intrinsically nonlinear and requires an adaptive DPD system to work properly. In this regard, integrating an adaptive DPD system with the DPA on the same chip could be worthwhile. Other suitable linearization techniques could also be investigated. In addition, automatic time alignment between the amplitude and phase paths is another difficult task that needs to be addressed. For power control, a combination of supply voltage variation, ACW resolution reduction, input and output RF attenuators is proposed in this work to provide transmitted-power control range. Alternatively, other techniques such as Doherty [48] and outphasing power combining [49] can be introduced. In an outphasing configuration, the outphasing angle between the two amplifiers can be employed to provide extra power control range in the low power mode, in addition to the proposed power control strategy. By combining a pair of DPAs to form a complete transmitter, the output power is doubled and the external high-power amplifier could possibly be eliminated. The Doherty DPA is, in itself, another attractive research topic, providing an improved efficiency for a wide power range, which is essential for modern communication standards with high PAPR, while offering digital controllability.

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